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An Actively Balanced Distributed Regenerative Snubber with Reduced Part Count in Multi-Level Power Converters

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***Abstract*—This work presents a distributed regenerative snubber network with reduced part count in multi-level converter designs. The proposed technique utilizes the ordinarily detrimental parasitic commutation loop inductance to harvest C_{OSS}-related energy using a network of high-speed diode-capacitor catching circuits. The proposed approach has several attractive features: First, V_{DS} overshoot is greatly reduced, as with conventional snubber design. Second, the speed of switching transitions may be increased substantially for reduced overlap loss. Third, layout design effort is relaxed, with larger commutation loop geometries expected to improve system performance. Fourth, a soft-charged daisy-chain allows multiple snubbers to sequentially transfer harvested energy to a common collection point with high efficiency. Finally, a single active component is used to resonate recovered energy back into the primary power path resulting in increased converter efficiency. A hardware prototype demonstrates intended operation in a 6-level flying capacitor multilevel (FCML) converter, with measured waveforms illustrating further improvement with modified active balancing control.**

I. Introduction

In order to minimize loss in hard-switched power converter designs, switching transitions are typically kept as short as possible so as to minimize overlap loss. However, fast switching transitions can cause parasitic induced ringing around the power stage's commutation loop (Fig. 1). This ringing imposes a transient voltage overshoot across the complementary switching device's drain-to-source terminals and intrinsic C_{OSS} capacitance, possibly leading to device over-stress and failure. In response, many practical designs prolong turn-on times such that they are much longer than the gate-drive's transient capability, suffering increased overlap loss as a result. This unfavorable trade-off is of particular concern when using high-bandwidth wide band-gap switching devices such as gallium nitride or silicon carbide, where fast switching speeds are possible but often not realized. Subsequently much effort has been put into low inductance commutation loop design, with stray loop inductance on the order of 1 nH reported in high voltage multi-level designs [1]–[3], and sub-nH's reported in low-voltage half-bridge structures when using expensive PCB stackups [4]. However, further loop minimization is ultimately limited by the packaging and size of the components themselves.

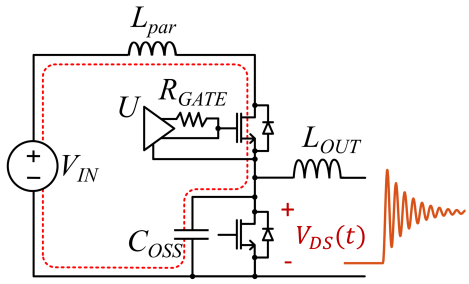

Fig. 1: Commutation loop (dashed) of a half-bridge power stage. The high-side gate driver is depicted with an increased pull-up resistor, R_{GATE}, to slow down switch turn-on time for reduced commutation loop ringing and voltage overshoot on C_{OSS}; the internal output capacitance of the low-side switch.

A. Overshoot Mitigation: Increased Turn-ON time

A simple and cost effective solution to avoid voltage overshoot is to increase the gate driver's pull-up resistance, R_{GATE}. This results in an increase in switch turn-on time by incurring a more gradual transition from $R_{DS,off}$ to $R_{DS,on}$. This acts to dampen the commutation loop with a temporarily increased $R_{DS,on}$, thus protecting devices from voltage overshoot. This approach is straight-forward and effective in diminishing ringing, but comes at the cost of increased overlap loss due to the extended transition time. Therefore a better approach is to first design a commutation loop with decreased parasitic inductance for reduced ringing, before extending turn-on times to the minimum duration required. All of the cited examples above apply this strategy, and while turn-on times are decreased, they are still significantly longer than those achievable if voltage overshoot were to be ignored. As such, the achievable switching speeds of high-bandwidth power devices, such as Gallium Nitride, is often not realized in practice.

Moreover, we note that during a hard-switching transition, even if voltage overshoot were neglected and overlap loss largely eliminated due to an extremely fast turn-on time, $C_{OSS}V_{IN}^2$ Joules of energy would still be dissipated as the C_{OSS} output capacitors of both transistors are re-biased.

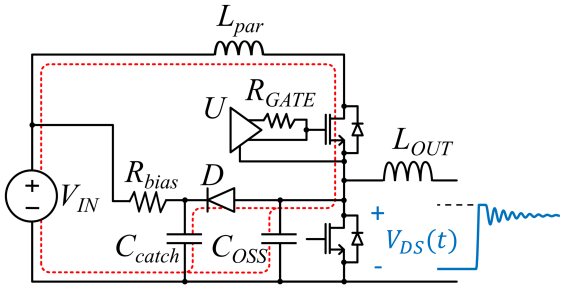

Fig. 2: Half-bridge with dissipative RCD snubber. Once the voltage overshoot on C_{OSS} exceeds the voltage stored on C_{catch}, diode D turns on, effectively clamping further voltage overshoot through the introduciton of additional capacitance.

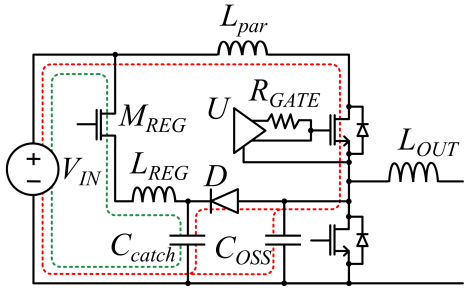

Fig. 3: Half-bridge with example regenerative snubber. Energy recovered by C_{catch} is periodically resonated back to V_{IN} with high efficiency via M_{REG} and L_{REG}.

B. Dissipative Snubbers

An alternative approach to overshoot mitigation is the implementation of snubber circuits [5]. These small assistive circuits increase component count, but can greatly alleviate ringing while facilitating fast turn-on transitions for reduced overlap loss. They find particular use in designs with large components and where a power converter's commutation loop cannot be shrunk any further.

A common snubber is the dissipative resistor-capacitor-diode (RCD) snubber depicted in Fig. 2. By sizing C_{catch} much larger than C_{OSS}, this configuration clamps the maximum V_{DS} voltage of the low-side FET to be close to V_{IN} by temporarily increasing the apparent size of C_{OSS} when the diode conducts. At the moment D turns on, C_{OSS} is charged to V_{IN} and $\frac{1}{2}C_{OSS}V_{IN}^2$ of energy is stored in the commutation loop's parasitic inductance, L_{par}. As time progresses, L_{par} delivers most of this energy onto C_{catch} where it is captured as a result of the diode turning off once current in L_{par} is exhausted. It is important C_{catch} and the diode be placed very close to C_{OSS} so that the snubber can provide an alternative lower impedance path to charge flowing around the primary commutation loop once the diode begins to conduct. Somewhat counter-intuitively, an increased commutation loop inductance, L_{par}, assists with this criteria by slowing the ringing frequency of the loop and minimizing the relative effect of any stray inductance that may be situated between C_{catch} and C_{OSS}. However, should the snubber circuit fail in this case, worse overshoot would be observed due to the loop's increased Q-factor with increased L_{par}.

Stray inductance on the R_{bias} branch is less critical as this path acts to slowly re-balance charge over the remainder of the switching period. That is, R_{bias} ensures that the voltage on C_{catch} nominally returns to V_{IN}, with the captured $\frac{1}{2}C_{OSS}V_{IN}^2$ Joules of ringing energy being dissipated through it. As a result, while this circuit can effectively clamp voltage overshoot — thereby allowing for faster turn-on times — $C_{OSS}V_{IN}^2$ Joules of energy is still dissipated during each hard-switched transition.

C. Regenerative or Non-Dissipative Snubbers

Recognizing the potential to recycle a snubber circuit's captured commutation loop energy, thereby reducing switching loss even further, several snubber variations termed "non-dissipative" or "regenerative" have been proposed (e.g. [6]–[9]). These variations omit resistive elements and instead find a way to direct the recovered $\frac{1}{2}C_{OSS}V_{IN}^2$ energy towards a useful task; usually by reinsertion back into the primary power path. To do so, typically two or more switching elements and a number of passives are required for a given commutation loop.

Most work done thus far on regenerative snubbers has focused on ringing mitigation and energy recovery within a single commutation loop. Today, multi-level converters, such as the flying capacitor multi-level (FCML), have gained interest due to their greatly enhanced passive utilization [10], [11]. As such, there is interest in the development of regenerative snubber solutions that enable effective energy recovery within the plurality of commutation loops present within multilevel power converters, while keeping part count to a minimum.

Rather than implementing repeated independent snubber cells for each commutation loop, in this work we demonstrate the first distributed regenerative snubber solution that mitigates ringing within each commutation loop of an FCML and recycles the aggregate harvested energy using a single active component. As a result, the proposed design reduces voltage overshoot, mitigates overlap loss, alleviates C_{OSS} switching loss, and eases layout design while requiring a minimal number of added components, most of which being low-cost capacitors or diodes.

II. Proposed Distributed Regenerative Snubber

Figure 4 depicts a 6-level FCML converter with the proposed distributed regenerative snubber network attached to the lower half switches: similar to a 2-level buck, in a step-down FCML the primary output inductor facilitates zero-voltage-switching (ZVS) of the lower-half switches and soft-charging of the C_{OSS} capacitance in the top-half switches during high-to-low switching transitions, thereby negating the need for overshoot protection on the top half switches. In step-up or bi-directional applications, the proposed snubber network may be alternatively or additionally applied to the top-half switches. By inserting a string of connecting diodes between each C_{catch}, charge is shared between adjacent C_{catch} capacitors when the associated low-side FETs turn on. As a result of ZVS action (Fig. 5), this charge transfer happens with high efficiency, resulting in a soft-charged daisy-chain that collects each cell's recovered $\frac{1}{2}C_{OSS}V_{DS}^2$ energy on the right-most $C_{catch,5}$. Once there, this energy is periodically resonated onto $C_{fly,4}$ via M_{REG}, effectively directing the recovered energy back into the primary power path for improved converter efficiency.

However, since all of the recovered energy is reinserted onto a single capacitor in the FCML's power stage, a systemic imbalance is incurred that causes the voltages of all flying capacitors to deviate from their nominal bias points (Fig. 10 (b)). This in turn increases $\frac{1}{2}C_{OSS}V_{DS}^2$ energy losses until no net energy is recovered in practice. To surmount this, an active balancing technique termed constant effective duty cycle control

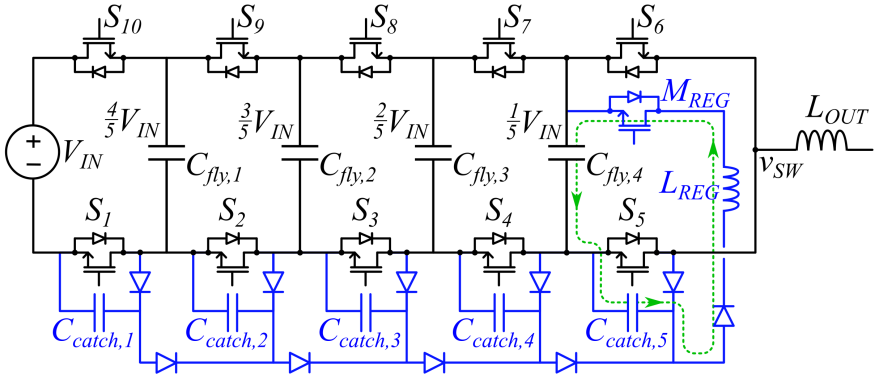

Fig. 4: Schematic of a 6-level FCML buck converter with the proposed distributed regenerative snubber network appended to the low-side switches. A soft-charged daisy-chain of diodes allows each cell's recovered energy to accumulate on the right-most $C_{catch,5}$. There, a single active device, M_{REG}, is used to resonate the recovered energy onto $C_{fly,4}$, thereby reinserting it back into the power path.

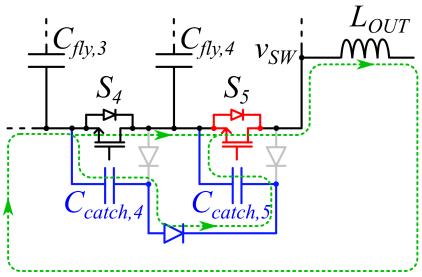

Fig. 5: Example ZVS of S_4 while switch S_5 is turned on. Before S_4 turns on, the primary output inductor L_{OUT} discharges its intrinsic C_{OSS} capacitance. In doing so, L_{OUT} also facilitates a soft-charged energy transferal between $C_{catch,4}$ and $C_{catch,5}$, improving snubber efficiency.

(CEDC) [12] is applied to ensure that the flying capacitors maintain their correct bias points. Once applied, energy is successfully recovered, with the proposed snubber network improving converter efficiency (Fig. 8) in addition to reducing voltage overshoot despite using a very small pull-up resistor within the complementary switch's gate driver ($R_{GATE} = 2\Omega$ in Fig. 7(c)).

III. Hardware Implementation and Measured Results

A hardware prototype, depicted in Fig. 6, was constructed using the components listed in Table I. In contrast to optimized designs, little effort was made to minimize commutation loop size, with intentionally large lateral loops measuring $\sim 200\,\text{mm}^2$ estimated to give tens of nanohenries in parasitic inductance. Conversely, diode-capacitor catching elements were placed as close to switches S_{1-5} as possible, using minimal package sizes for fast transient response. Diodes were sized to have small junction capacitance with respect to their adjacent FET's C_{OSS}, and forward recovery time is prioritized over reverse recovery to keep overshoot to a minimum.

Figure 7(a) depicts measured voltage overshoot and ringing on switch S_1 when $R_{GATE} = 2\,\Omega$. With over 100 % overshoot, this approach would require greatly de-rated switches to function reliably in practice. Fig. 7(b) addresses this by increasing R_{GATE} to $35.7\,\Omega$, significantly reducing voltage overshoot, but increasing full-load losses by 32 % (Fig. 8). The proposed distributed snubber (Fig. 7(c)) achieves the lowest voltage overshoot, while still using a $2\,\Omega$ gate resistor for reduced overlap loss. Subsequently, this case demonstrates the highest efficiency, particularly at light-load where $\frac{1}{2}C_{OSS}V_{DS}^2$ energy recovery has a more significant impact.

Figure 9 depicts the voltage on $C_{catch,5}$, demonstrating the proposed technique's ability to clamp V_{DS} overshoot on S_5 and its ability to collect the energy captured by $C_{catch,1-4}$ through the distributed soft-charged snubber network. Additionally, upon activation of M_{REG}, Fig. 9 depicts the periodic resonant reinsertion of harvested energy onto $C_{fly,4}$. Lastly, Fig. 10(c) depicts the use of CEDC active balancing control, in addition to the proposed snubber network, to ensure that all flying capacitors maintain nominal voltage levels and all switches experience uniform voltage stress.

TABLE I: Component Details

Components	Details	Part Number
S_{1-10}	100 V, 3.2 mΩ GaN-FET	EPC2218
$C_{fly,1-4}$	4 × 2.2 µF, X6S, 450V	C5750X6S2W225K250KA
L_{OUT}	5.5 µH	IHLP5050FDER5R6M01
$C_{catch,1-5}$	10 nF, 0603	CGA3EANP02A103J080AC
D	120 V, 0.9 V @ 100 mA	CMAD4448
M_{REG}	100 V, 73 mΩ GaN-FET	EPC2036
L_{REG}	150 nH	SRP3012TA-R15Y
R_{GATE}	2 Ω, 37.5 Ω, 0402	RK73H1ETTP2R00F CR0402-16W-35R7FT
U	5 V, 7 A / 5 A Gate Driver Level-Shift and Power	LMG1020 ADUM5240

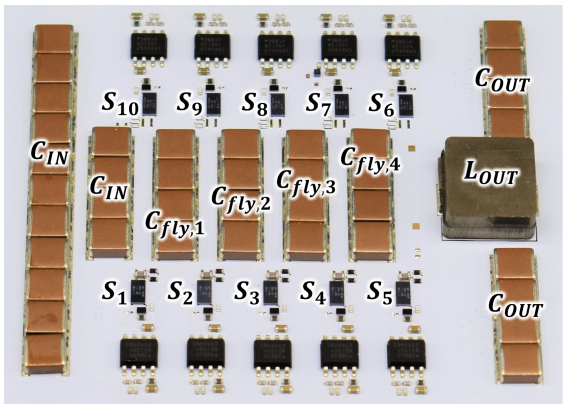

Fig. 6: Photograph of a 6-level FCML hardware prototype (on white soldermask) with primary power stage component locations arranged such that they mirror that of Figure 4.

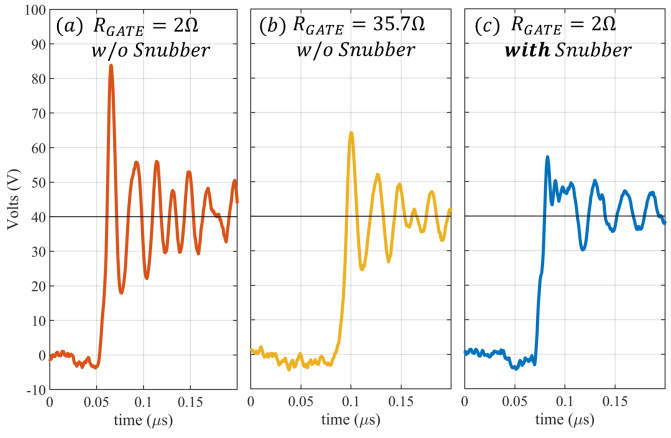

Fig. 7: Measured overshoot on switch S_1 of the 6-level FCML prototype with $V_{IN} = 200\,\text{V}$, $V_{OUT} = 20\,\text{V}$, $f_{SW} = 400\,\text{kHz}$, and nominal $V_{DS,off} = 40\,\text{V}$. (a) $R_{GATE} = 2\,\Omega$ and snubber disabled. (b) $R_{GATE} = 35.7\,\Omega$ and snubber disabled. (c) $R_{GATE} = 2\,\Omega$ and snubber with CEDC enabled. The proposed distributed snubber gives over a 50% reduction in overshoot while retaining a $2\,\Omega$ pull-up resistor for reduced overlap loss.

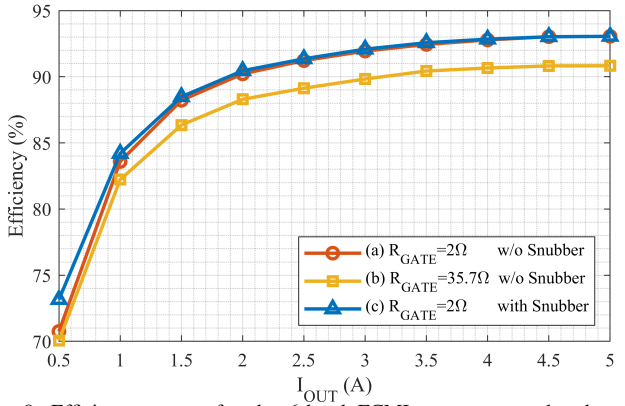

Fig. 8: Efficiency curves for the 6-level FCML prototype under the same conditions as Fig. 7. When $R_{GATE} = 2\,\Omega$, heavy load losses are reduced by 24% due to increased turn-on speeds. With the proposed snubber enabled, this improved efficiency is achieved while simultaneously giving the lowest voltage overshoot (Fig. 7). Additionally, at light load ($I_{OUT} = 0.5$ A) a 2.5% efficiency boost is observed as $C_{OSS}V_{DS}^2$ energy recovery becomes more apparent.

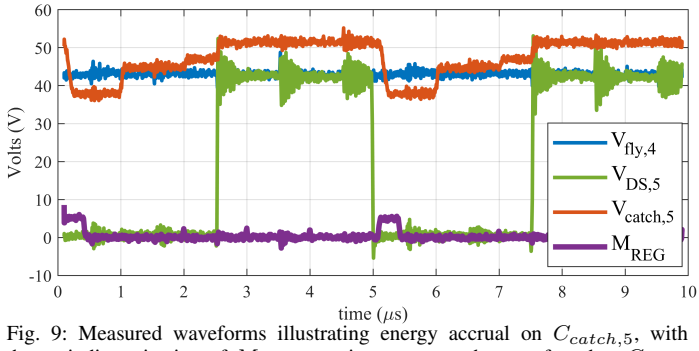

Fig. 9: Measured waveforms illustrating energy accrual on $C_{catch,5}$, with the periodic activation of M_{REG} causing energy to be transferred to $C_{fly,4}$ through resonant action.

IV. Conclusion

This work has demonstrated a distributed snubber network that greatly reduces voltage overshoot while maintaining fast switching transtions for improved converter efficiency. Moreover, C_{OSS} switching energy is effectively recovered through a cascaded diode chain by leveraging existing ZVS conditions within the primary power stage. Furthermore, a single active device and inductor are used to reinsert all recovered energy back into the power path. Last, a constant effective duty cycle (CEDC) control scheme ensures flying capacitors maintain voltage balance despite an asymmetric charge reinsertion.

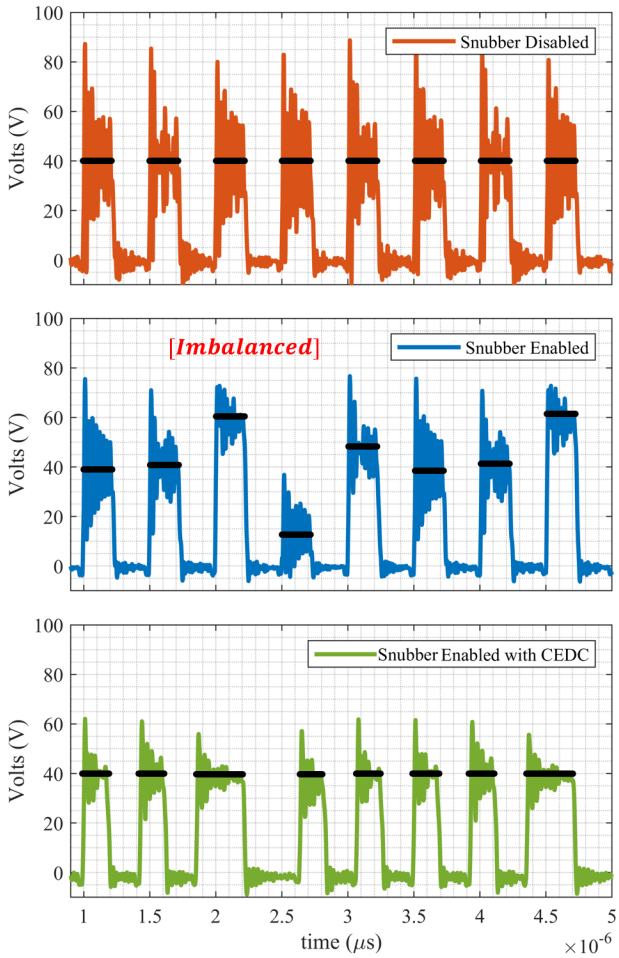

Fig. 10: Measured V_{SW} waveforms of a 6-level FCML performing a 10:1 conversion with $V_{IN} = 200$ V and $R_{GATE} = 2\,\Omega$. (a) snubber disabled, (b) snubber enabled, (c) snubber and active CEDC balancing enabled. Over a 50% reduction in voltage overshoot is observed with fly capacitors actively balanced for evenly distributed switch stress.

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