Title
Site Selective Laser Processing for Flexible and Wearable Electronics with 2D Materials and 2D-like Random Networks

Author
KWON, HYUKJUN

Publication Date
2015

Peer reviewed|Thesis/dissertation

Site Selective Laser Processing

for Flexible and Wearable Electronics with 2D Materials and 2D-like Random Networks

by

Hyuk-Jun Kwon

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Mechanical Engineering

and the Designated Emphasis

in

Nanoscale Science and Engineering

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Costas P. Grigoropoulos, Chair
Professor Liwei Lin
Professor Oscar D. Dubon

Summer 2015

Site Selective Laser Processing

for Flexible and Wearable Electronics with 2D Materials and 2D-like Random Networks

By

Hyuk-Jun Kwon

ABSTRACT

Site Selective Laser Processing

for Flexible and Wearable Electronics with 2D Materials and 2D-like Random Networks

by

Hyuk-Jun Kwon

Doctor of Philosophy in Engineering - Mechanical Engineering

and the Designated Emphasis in Nanoscale Science and Engineering

University of California, Berkeley

Professor Costas P. Grigoropoulos, Chair

Flexible and wearable electronics are envisioned as a future platform of electronics integrated into a variety of emerging technologies from sensing and monitoring to human-inspired applications. Among many fascinated flexible applications, displays are aggressively developing field of research and they are widely connected with transistor platform. Currently, the needs of people are being particular about for mobile phones, portable devices, and even televisions; they require new and more advanced displays. Therefore, the future displays should have high performances, such as low power consumption, ultra-high resolution, high frame rate and robust flexible platform. High-mobility thin film transistors will be a key enabling technology for achieving such performance by reducing the transistor size in the display's active area. Also, they helps to increase aperture ratio, brightness, and frame rates and to decrease bus-line load power consumption.

In this regard, 2D transition metal dichalcogenides have attracted much interest owing to their finite band gap values, rich excitonic dynamics, and even valley polarization (valleytronics) associated with the broken inversion symmetry. Among these 2D materials, molybdenum disulfide (MoS_2) has been considered a channel material for high speed and/or flexible devices and a component material to improve the performance of conventional silicon devices. Furthermore, these layered semiconductors are emerging alternatives to silicon-based electronics. Despite their potentials in electronics and optoelectronics, reliable and stable processing methods are needed for successful transition to practical applications, especially for the flexible/wearable electronics used flexible materials with a low thermal budget (< 200 °C). Typically, used flexible materials cannot be applied conventional high thermal processes, which affect the entire panel including unwanted areas where the high thermal process should be excluded.

For the process having the critical limitations of the flexible/wearable applications, the many features of laser are exactly appropriate; the laser is spatially local selective, air-stable, and widely tunable by varying the duration and intensity of laser irradiation. Moreover, laser process can be digitally controlled by the computer with programmable software. In this dissertation, the proposed approaches (laser annealing, direct laser writing, laser welding, and interference lithography) represent a powerful means to realize high performance flexible devices based 2D materials, especially for MoS_2.

First, I demonstrate that mechanically flexible and optically transparent (more than 81% transmittance in visible wavelength) multilayered MoS_2 thin-film transistors (TFTs) in which the source/drain electrodes are selectively annealed using picosecond laser achieve the enhancement of device performance without plastic deformation, such as boosted mobility, increased output resistance, and decreased subthreshold swing. Numerical thermal simulation for the temperature distribution, transmission electron microscopy (TEM) analysis, current-voltage measurements, and contact-free mobility extracted from the Y-function method (YFM) enable understanding of the compatibility and the effects of pulsed laser annealing process; the enhanced performance originated not only from a decrease in the Schottky barrier effect at the contact, but also an improvement of the channel interface.

Second, through laser direct writing (LDW) method, arbitrary fine patterns are produced for the electrodes as well as defining the channel of TFTs. Also, LDW with ink-jet printing shows the possibility and the potential for the future of flexible/wearable electronics as more versatile process. In addition, interference lithography using phase shift mask allows making periodic nano-scale features, readily.

Furthermore, laser process is also applied to the welding for fabricating mechanically robust and electrically attractive 2D-like random networks. The laser welding is compatible with cost-effective solution process and good for the flexible applications. After the laser welding, the sheet resistance of 2D-like networks created by silver nanowires is significantly improved. Note that the best improvement is around 55 times without any degradation of the electrical performance during cycling bending test.

These various outcomes from the experiments indicate that the site selective laser process can open up opportunities to fabrication of the electrical devices on flexible platforms.

To my parents,
my advisor,
all committee members,
LTL family,
my friends,
and god

Thank you for all of your love, support, and inspiration.
I couldn't have made it without you all.

Table of Contents

LIST OF FIGURES

Figure 6.4 **(a)** Measured stress (σ) - stretch (λ) curve of the specimen of solution based PI and PET (t= 0.105 mm) and **(inset)** fitting Mooney-Rivlin model with experimental data. **(b)** The numerical result on hyperelastic nonlinear stress analysis based on the parameters extracted by the real experimental data when the bending radius was 5 mm. **(c)** Through fitted Mooney-Rivlin model, expected mechanically stable range (green region) of the structure with resect to the radius of curvature of the substrate and **(d)** to thickness of the substrate.

Figure 6.5 Variation of TFT performances of the flexible MoS_2 TFTs under various mechanical stresses. **(a)** Comparison of the transfer characteristics of the flexible MoS_2 TFTs under static bending environments with three different bending radii (flat, r = 10 mm, and 5 mm). **(Inset)** Photograph of the bent MoS_2 TFTs attached on rigid cylinder with pre-defined radius, which was depicted as white dashed arc and arrow. **(b)** Comparison of the transfer characteristics of the flexible MoS_2 TFTs under cyclic bending environments with respect to number of bending (n = 0, 20, 100, and 1000). **(Inset)** Photograph of the flexible MoS_2 TFTs loaded on multi-modal bending tester. Bending radius (r = 10 mm) was depicted as black dashed circle and arrow. Variations of μ_{eff} and V_{TH} of the flexible MoS_2 TFTs as a function of **(c)** static bending radii and **(d)** number of cyclic bending.

LIST OF TABLES

Chapter 1

Introduction

1.1 Flexible Electronics

Flexible has various meanings and many qualities: bendable, wearable, elastic, lightweight, rollable, non-fragile, low cost, and others. In this aspect, we can define that flexible electronics encompasses electronic devices with mutifunctional (e.g. electrical, sensing, photonic, etc.) features using flexible materials (e.g. soft, light, rugged). Nowadays, the boundary of flexible/wearable electronics is wide-open and the field has rapidly developed and moved with pioneering applications for light-weight, portable, and comformable producs such as flexible OLED displays,[1] solar cells and batteries,[2] wearable health patches for personal health-monitoring/therapeutics,[3] and implantable medical devices[4] as shown in **Figure 1.1**.

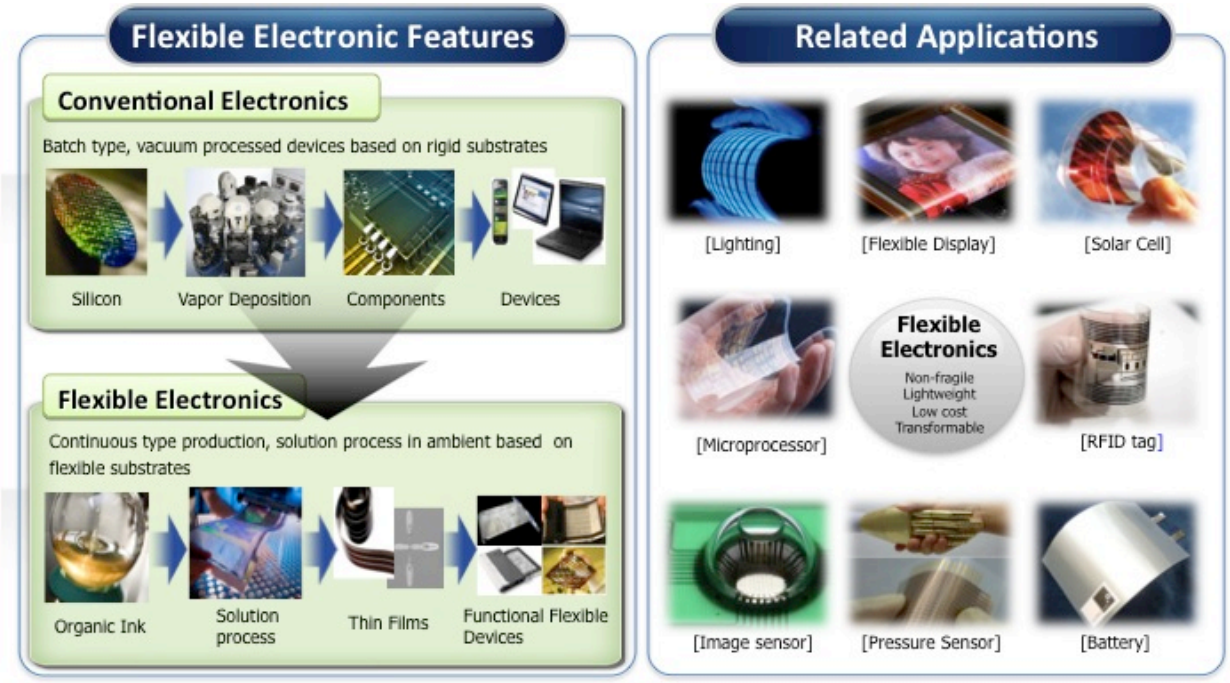

Figure 1.1 New paradigm and platform of flexible/wearable electronics and their various applications including flexible displays, human-inspired electronics, sensors, and energy/power devices. (images from Google search)

In order to produce aforementioned functional applications, an important segment of flexible/wearable electronics is widely connected with thin-film transistor (TFT) platform. Furthermore, among the various applications based on TFT platform, flexible displays are aggressively developing field of research.

1.2 Trends of Flexible Displays

Science fiction (SF) movies and fantasy novels have inspired flexible displays for many years. For example, in the Harry Potter movies, flexible display, daily prophet, appears to be a wizard's fantasy aiming at reading video newspaper. Also, we usually imagine the roll-up display inside a pen or a phone as a future flexible display. In addition, there are a plethora of candidate applications for the next generation displays. Nowadays, the size of the display is getting larger and larger. Therefore, we easily expect the wall can be a display. Moreover, Google already commercially released wearable goggle display named Google glass. Also, display can deliver two-way communication through mirror display or can obtain some information while looking over the transparent display.

However, just a few decades ago when we used bulkly and heavy cathod ray tube (CRT) display (early 1900s), these flexible displays were a dream and imagination in our mind. After that (mid 1900s), invented TFTs shifted the paradigm of the display; flat panel display (FPD) with unparalled featrues (e.g. very thin, lightweight, low-power consumption) created a great sensation. Then, now, many companies and researchers have tried to make a future display platform and to change a picture of our life which does not exist today (see **Figure 1.2**).

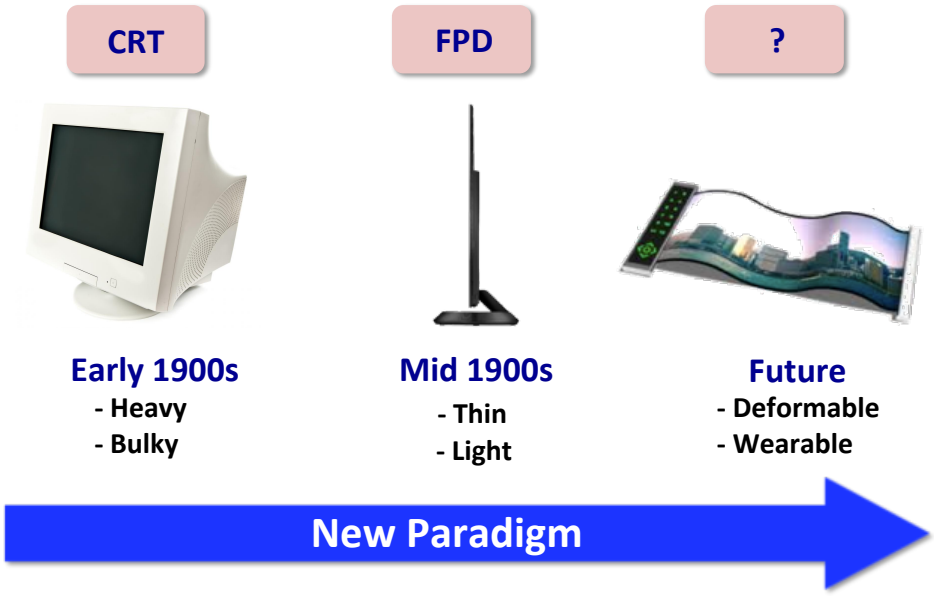

Figure 1.2 Big evolution of display platform and paradigm away from CRT to FPD and to the odd-shaped future flexible display. (images from Google search)

IDTechEx, a knowledge-based consultancy company, offered a more positive forecast for the flexible electronics and displays. **Figure 1.3** shows the market value of flexible electronics versus non-flexible electronics.[5] According to the report, $1 billion (US) of the electronics (7%) was conformal or flexible in 2015 (93% of non-flexible).[5]

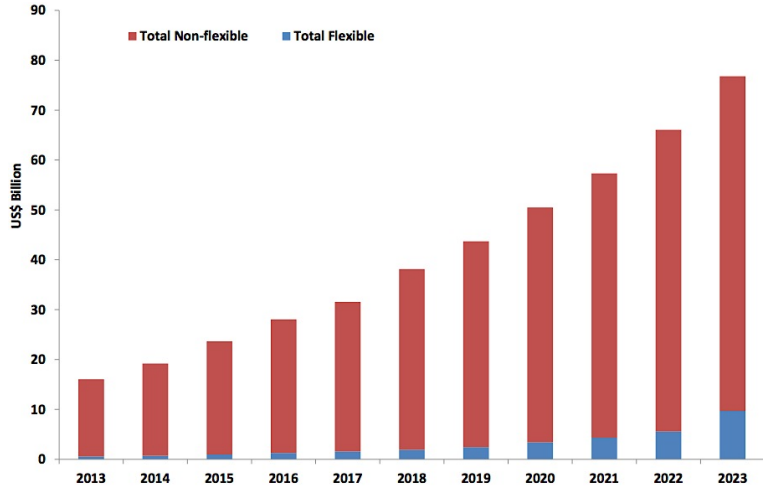

Figure 1.3 Total market value of flexible/conformal electronics versus non-flexible/rigid electronics 2013-2023. (from IDTechEx forecast report)[5]

In 2023, however, the market value of conformal/flexible will raise to $10 billion of the total value (15%, 85% of non-flexible).[5] Moreover, through the following graph (**Figure 1.4**), we can expect that flexible display based on the organic light-emitting-diode (OLED) panel will be $ 6.5 billion (70 %) of the market value and be placed the first among other flexible applications in 2023; the difference will be more evident (the 2nd place: 9% of sensors).[5]

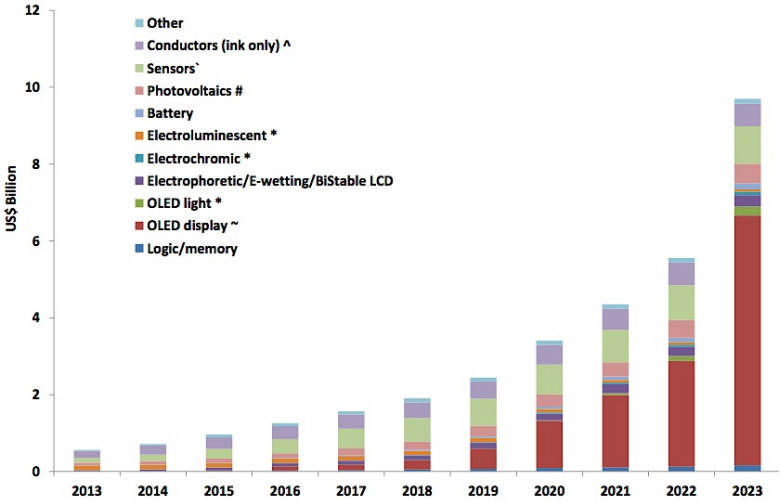

Figure 1.4 Total market value of only flexible/conformal electronics 2013-2023. (from IDTechEx forecast report)[5]

Note that the OLEDs, a special class of LEDs, is manufactured by placing a series of thin layers of organic compounds between two conductors and is primarily based on the principle of electro-phosphorescence, where certain organic molecules are observed to emit light upon application of electric voltage. The OLED is key to many 'Flexible Electronics' applications as it offers many advantages. First of all, it can realize any shape, providing versatility in terms of design. In addition, its structure does not present any cell gap, so that it can achieve the wide viewing angle. The aspect of manufacturing, the OLED process is in good compatibility with flexible substrate which means that it has wide variety of manufacturing options such as roll-to-roll process and printing method.

1.3 Key Component for Displays

For operating displays, numerous components and technologies should be required and supported; displays are a complex system of linked many components. Furthermore, as today the consumers are becoming increasingly specific in their demands such as large size, high resolution, high operating speed, generating vivid colors, low price, and low power consumption, the displays are getting complex and specialized.

Even though the display panels come in various formats (e.g. liquid crystal display (LCD), plasma display panel (PDP), OLED) depending on their intended applications, they can be simply divided into four main parts to function efficiently as illustrated in **Figure 1.5**: (1) a substrate, (2) driving circuit, (3) display module, and (4) supporting films. A detailed explanation will be given in the following section.

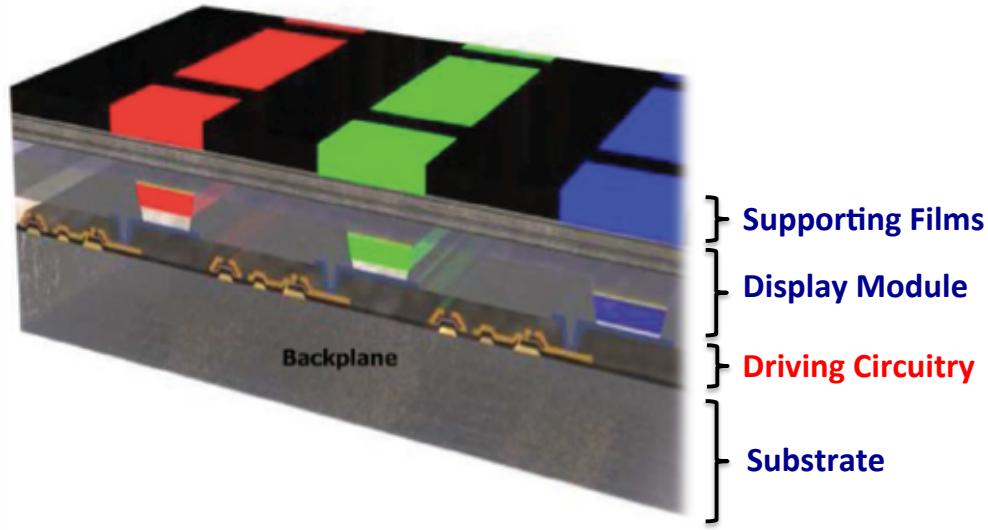

Figure 1.5 Schematic cross-sectional display structure briefly separated by four parts: (1) substrate, (2) driving circuitry, (3) display module, and (4) supporting films. (image from S. Kim and H.–J. Kwon *et al.* Adv. Mat. 2011) [1]

1.3.1 Flexible substrates

The substrate is the starting component for all displays and other components. In an architectural analogy, it is like the land where a house is built. Therefore, it is very important to select the suitable flexible substrates for making the devices in the beginning. Also, depending on which substrates choose to use, it can make the limitations of process temperature and the challenges in terms of compatibility with the other components that need to be integrated onto them.

Table 1.1 summarizes the properties of the general candidates of flexible substrates for flexible applications.[6] The values of the properties come from the commercially available products: polyethylene terephthalate (PET) – Melenix® from DuPont Teijin Films, polyethylene naphthalate (PEN) – Teonex® Q65 from DuPont Teijin Films, poly carbonate (PC) – Lexan® from GE, polyethersulfone (PES) – Sumilite® from Sumitomo Bakellite, and polyimide (PI) – Kapton® from DuPont).

Based on these various candidates of the substrates, PEN substrates are being widely used for the flexible TFT backplanes and OLED display because of the properties, availability, long-term potential, and reasonable cost.[7-9] Although, metal foil has relatively high thermal stability, roughness and electrical isolation are issues. Glass with high transmittance and thermal stability could be a good candidate, however, it has weak flexibility. Note that Corning company now releases flexible Willow® glass, still in progress. Also, PET is very cheap material compared to PI, however, low thermal resistance is a hurdle as the substrate.

	Metal Foil (Stainless Steel)	Glass	Polyethylene terephthalate (PET)	Polyethylene naphthalate (PEN)	Poly carbonate (PC)	Poly ethersulfone (PES)	Polyimide (PI)
Transmission (400-700 nm) (%)	0	92	89	87	90	90	< 70 (Yellow)
CTE (-55 to 85 °C) (ppm/°C)	10	5	~ 15	~ 13	60 ~ 70	~ 54	30 ~ 60
T_g (°C)	~ 1000	~ 600	~ 78	~ 120	~ 150	~ 220	~ 410
Permeability for oxygen and moisture (%)	0	~ 0	0.14	0.14	0.4	1.4	1.8
Young's modulus (Gpa)	~ 200	~ 70	~ 5.3	~ 6.1	~ 1.7	~ 2.2	~ 2.5

Table 1.1 Representative candidates of flexible substrates for flexible applications: metal foil, glass, PET, PEN, PC, PES, and PI. (values in this table are taken from the reference[6])

1.3.2 Driving circuitry: TFTs

For switching and controlling the current like mechanical faucet, the driving circuitry, especially for TFTs, is as important as the aforementioned substrate. As described in **Figure 1.6**, TFT has three electrodes (gate, source, and drain) and two types (*n*-type and *p*-type). For the operating case of *n*-type, a positive gate voltage ($V_{GS} > V_{TH}$, threshold voltage) induces the accumulation of electrons near the dielectric–semiconductor interface, which flows from source to drain via a semiconducting channel material under a positive drain bias ($V_{DS} > 0$) and vice versa (for *p*-type). During the current flow, moving electrons, the gate plays an important function of either blocking or admitting electrons. The design of the TFTs is the most critical factor in determining the quality for attaining high performance of the displays.

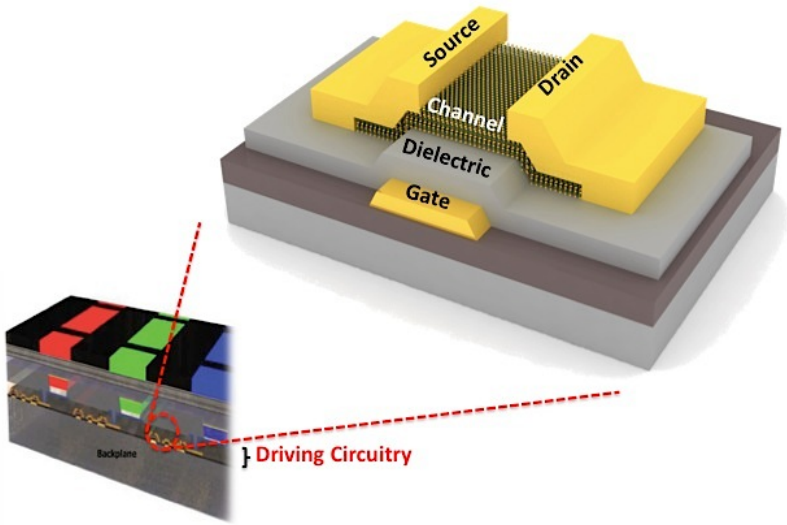

Figure 1.6 Schematic cross-sectional TFT structure with three electrodes: gate, source, and drain. (image from S. Kim and H.–J. Kwon *et al.* Adv. Mat. 2011) [1]

To this day, we are widely using TFTs based on amorphous silicon (a-Si) with low temperature process (<200°C, conventional process: ~300°C) as a channel material for switching devices such as LCD, imagers, and sensors due to the economic cost.[10, 11] However, the technology and trend are moving toward the large-area, transparent, multifunctional and flexible type of displays since OLED panel switched by low-temperature poly-silicon (LTPS) TFTs (process temperature: ~450°C) has been commercialized as shown in **Figure 1.7(a)**. Because poly-silicon has very high mobility compared to a-Si, it is suitable for high current driving device like active matrix OLED display.[12-14] However, the cost is high and fabrication process is quite complex and requires high temperature. Even though the two materials (a-Si, poly-Si) have these issues, they are being considered for flexible display applications because of the well-established knowledge and technologies. On top of that, many scientists and researchers have endeavored to find alternate and more compatible materials for the next generation of channel designs. Therefore, new TFT technologies with other materials (e.g. oxide, organic, carbon nanotube (CNT), nanowire (NW), graphene, etc.) are emerging for the flexible displays.

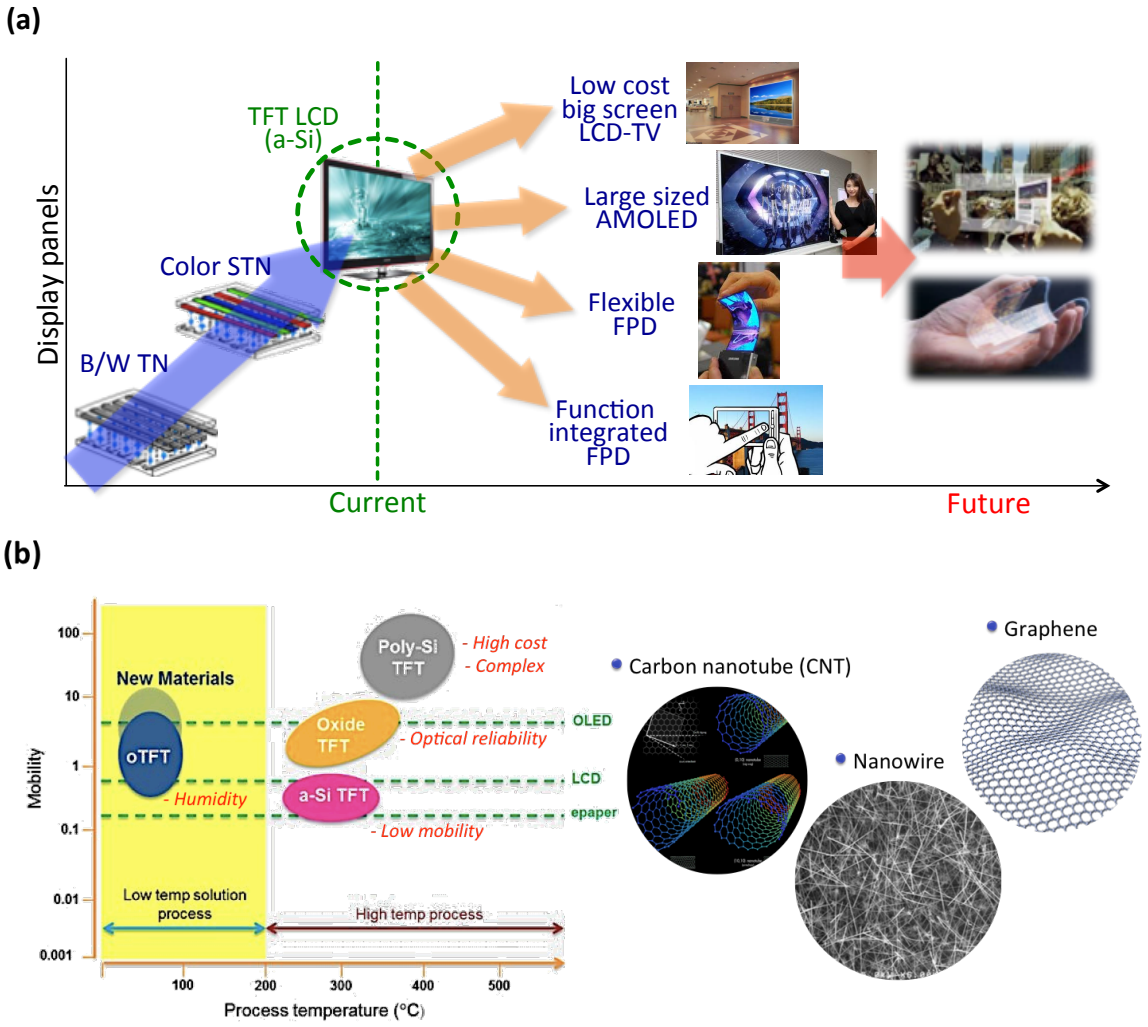

Figure 1.7 (a) Trends of technology of commercialized display panels. Currently, the promise of OLED technology has been to deliver displays that are more visually compelling and power efficient. Furthermore, the resolution and size of displays keeps going up caused by customers' needs. **(b)** TFT technologies and candidates of channel materials by the mobility and process temperature for the next generation flexible displays. (graph from plastic logic company and images from Google search)

Nowadays, oxide TFTs are on the verge of mass production due to their high mobility and low cost. Also, oxide materials such as ZnO,[15] In_2O_3,[16] and SnO_2,[17] have a wide-bandgap which allow to make transparent displays. Through In-Ga-Zn-O (IGZO), compound oxide material, the first flexible transparent TFT on PET was made in 2004.[18] However, the electron mobility of the material is still low (~ 10 $cm^2V^{-1}s^{-1}$) and weak optical reliability is an issue. Organic TFT (OTFT) is also attracting attention for flexible display because organic materials are soluble and low temperature process (~ room temperature). However, because hole mobility is higher than the electron mobility (i.e. OTFTs are *p*-type transistors) in most organic materials. Note that the mass of hole is larger than the mass of electron; electron mobility is usually faster than hole mobility. Therefore, the performance of OTFTs was not

impressive before the introduction of new organic materials and improved fabrication.[19-22] However, still there is much to be resolved such as stability for humidity. **Figure 1.7(b)** summarizes these technologies and materials for TFTs by their mobilities and process temperatures with key issues.

Aside from this, carbon nanotube, nanowire, and graphene are investigated in spite of the many capabilities of the TFTs based on a-Si, LTPS, organic semiconductors, and oxide semiconductors. For 20 years, nano-electronics have been widely studied for switching devices and optoelectronics. Especially, one-dimension (1D) carbon nanotubes[23-25] and nanowires[26] are attractive for thin-film transistor with high mobility. But there are limitations for integrated circuit. One reason is the deviation of device because of the distribution of diameter and chirality in growth. Another reason is the difficulty of aligning in a specific area. For these reasons, in order to overcome these limitations, nano-researchers turn their gaze on 2D graphene because 2D film is easily patterned and aligned with uniform characteristics.[27] After all, 2D graphene opens the door to 2D layer electronics, but has zero-bandgap, it is hard to apply to switching device. In the following, the recent potential candidates with ultra-thin and high mobility will be discussed for flexible and transparent display.

1.3.3 Display module

Display module has a special role in image delivery to the human eye by controlling the light. Today, three main display modules are considered in use: LCD, OLED, and electrophoretic display (EPD). LC has a rod-like molecular structure. Aligned LC molecules modulate the transmission of the light by modifying the angle between the direction of the incident light and LC molecules. Note that TFTs allow switching the orientation of the molecules. And OLED is the self-emissive electroluminescent module depending on an applied electric current of TFTs. Therefore, OLED module does not need backlight source and color filters and the nature of organic is suitable for the flexible display. Lastly, EPD is a reflective bi-stable module like paper. Because of using ambient light, the module is very comfortable to read, even in direct sunlight with low-power consumption. However, it is hard to support images in motion because the response time is still very low (~100 ms) and the reproducibility of desired colors is not good.

1.3.4 Supporting films

Depending on the types of modules, required supporting films are varied due to their features. In the case of LCD, color filters are necessary because the module cannot generate colors. Because OLEDs have the most sensitivity to moisture and oxygen, they should need barrier layer in order to protect the display panel and degradation. Touch, protecting, polarizing, brightness enhanced films are sometimes integrated onto the panel to improve functions.

1.4 Laser Processing for Flexible Displays

Laser processing has been developed steadily and is widely applied in various parts of flexible display now because of its irreplaceable advantages.

Typically used flexible materials, e.g. PEN, PET, and PI, as substrates pose significant manufacturing challenges, since their fabrication sequence must have a low thermal budget (< 200 °C). Therefore, conventional high temperature thermal processes cannot be applied as they affect the entire panel, including unwanted areas where the process should be excluded. **Figure 1.8** shows comparison of the spatial temperature distributions for thermal process and between pulsed and continuous wave (CW) laser source. As is evident in the Figure, the heat-affected zone (HAZ) expands in all directions through heat conduction. However, the HAZ extent is different, depending on whether the laser source is pulsed or CW laser. Consequently, the pulsed laser momentarily induces high temperature, imparting a smaller HAZ. Furthermore, high repetition rate of the irradiated pulses, the temperatures do not drop to the ambient temperature before the next pulse arrives. This leads to heat accumulation.[28] In this respect, the laser processing is a promising technology because it can induce thermal effect at very locally confined small area that needs high temperature without incurring extreme thermal damage to surrounding regions.[29, 30]

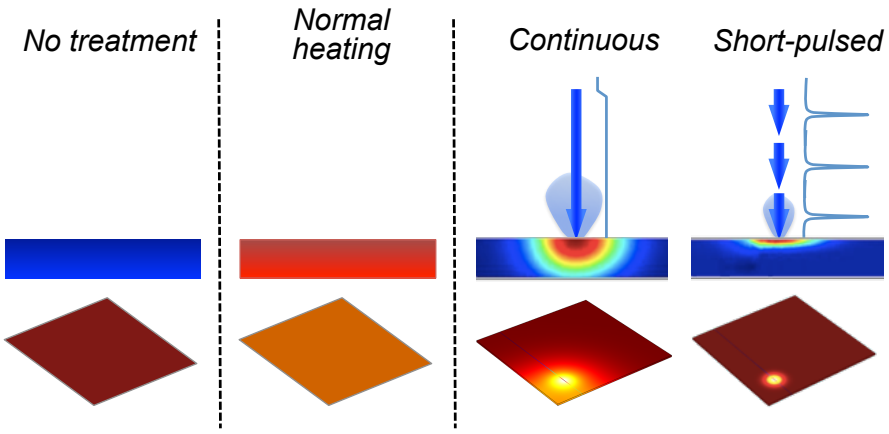

Figure 1.8 The spatial temperature distributions plotted along the surface for conventional thermal annealing as well as continuous laser and pulsed lasers heating.

In the commercially successful flexible AMOLED displays (e.g. Samsung's Galaxy Note Edge, LG Display's G Flex), laser is an indispensable process for their products even though the related processes are costly. Moreover, laser share of total process is on an increasing trend. For example, (1) plastic-based AMOLED displays are operated by excimer-laser-annealed TFTs (ELA-TFTs) on PI substrates. A large area excimer laser beam allows improving crystallinity and properties without thermal damage of the underlying substrate. (2) Secondly, to avoid difficulties presented by the plastic materials for the direct fabrication, the process of the flexible AMOLED displays is performed on the carrier glass. Therefore, at the last step, the structure should be released from the rigid carrier. This lift-off process relies on a laser-irradiation that is

favored for the high throughput. When the laser with the specific wavelength irradiates a special layer that reacts upon exposure, hydrogen gas is generated, and the gas is the driving force to separate the structure with the ELA-TFTs from the original carrier substrate. (3) Thirdly, today many product companies adopt a sapphire glass and even metal case having the great hardness as a protection layer from external factors. However, the strong hardness presents difficulty of direct and clear cutting. The laser solves this issue and achieves high quality of cutting surfaces and lines. (4) Moreover, the laser can be used for panel chamfering or trimming, which is removing unnecessary areas of the panel that has no patterns. Corner chamfering/trimming process by the laser can prevent cracks near the chamfering/trimming lines and can realize a very narrow bezel design of the panel before applying the laser process. (5) Lastly, the laser provides new solutions by allowing the machining and tooling to be micro scale. Because the mobile devices are getting thinner and thinner as the day goes on, the devices should be built to very high standard with close tolerance. Therefore, we need a more precise system and laser is a good candidate in this respect; perhaps it may be a promising way forward.

Likewise, the laser technology discussed earlier and later in this dissertation can enable emerging flexible devices and will pave the way for new fields of flexible electronics not yet imagined.

1.5 Scope of Dissertation

Laser is an essential factor for the flexible display. With regard to further challenges in flexible displays, several other laser technologies, especially for TFTs (driving part, see **Section 1.3.2**), are focused and investigated in the following chapters as summarized in **Figure 1.9**.

Chapter 2 focuses on the 2D semiconductor materials with the formula of MX_2 (M = Mo, W; X = S, Se, Te) composed of vertically stacked layers held together by van der Waals interactions as channel materials and their unique optical and electrical properties. The electrical characteristics of molybdenum disulfide (MoS_2) TFTs are observed and carrier transport mechanism is predicted through variable temperature measurement (from room temperature up to 350 K) and different operating ambient (in air and in a vacuum, ~10^{-5} Torr). Moreover, low-frequency noise measurement supports the immunity of MoS_2 for the effect of chemisorption.

In chapter 3, the irradiation of a pulsed laser with high energy density and short wavelength onto the metal electrodes leads to localized and confined thermal annealing effect without inflicting thermal damage to adjacent structures. This laser annealing effect on the electrical performances of flexible and transparent MoS_2 TFTs is explored through current-voltage measurements and Y-function method (YFM). I also seek to understand in depth the effect of the laser processing on the interface structure and composition by performing cross-sectional high-resolution transmission electron microscopy (HRTEM).

Chapter 4 describes highly enhanced field effect mobility (μ_{eff}) of MoS_2 TFTs through sol-gel processed high-k ZrO_2 insulator, compared to general $MoS_2/SiO_2/Si$ structures.

Furthermore, to avoid costly conventional mask-based photolithography, laser direct writing (LDW) process is employed using a simple set-up for defining the patterns of electrodes.

All non-vacuum and maskless processes for fabricating MoS_2 TFTs are achieved through LDW and ink-jet printing (silver ink) in chapter 5. Self-alignment by difference of surface energy and capillary force allows unshaped ink-jet printed silver (Ag) ink to make well-defined electrode structures. The chapter also describes the use of interference lithography through a phase shift mask (PSM) for producing periodic nano scale patterns.

A large number of groups have struggled to find alternative conductive films as new flexible electrodes superior to indium tin oxide (ITO) that has brittle ceramic properties and is deposited through an expensive vacuum process limiting its further progress. 2D-like random networks of Ag nanowires (NWs) are attracting a lot of attention because of compatibility for cost-effective solution processible mass production and their good electrical conductivity. In chapter 6, as a gate electrode, 2D-like random networks of AgNWs are uniformly formed onto the solution based PI substrate. Then, plasmonic laser welding is employed to enhance interconnection each other like a net or mesh.

Chapter 7 summarizes the key findings and results in this dissertation and research and suggests the direction of future works for the flexible/wearable electronics.

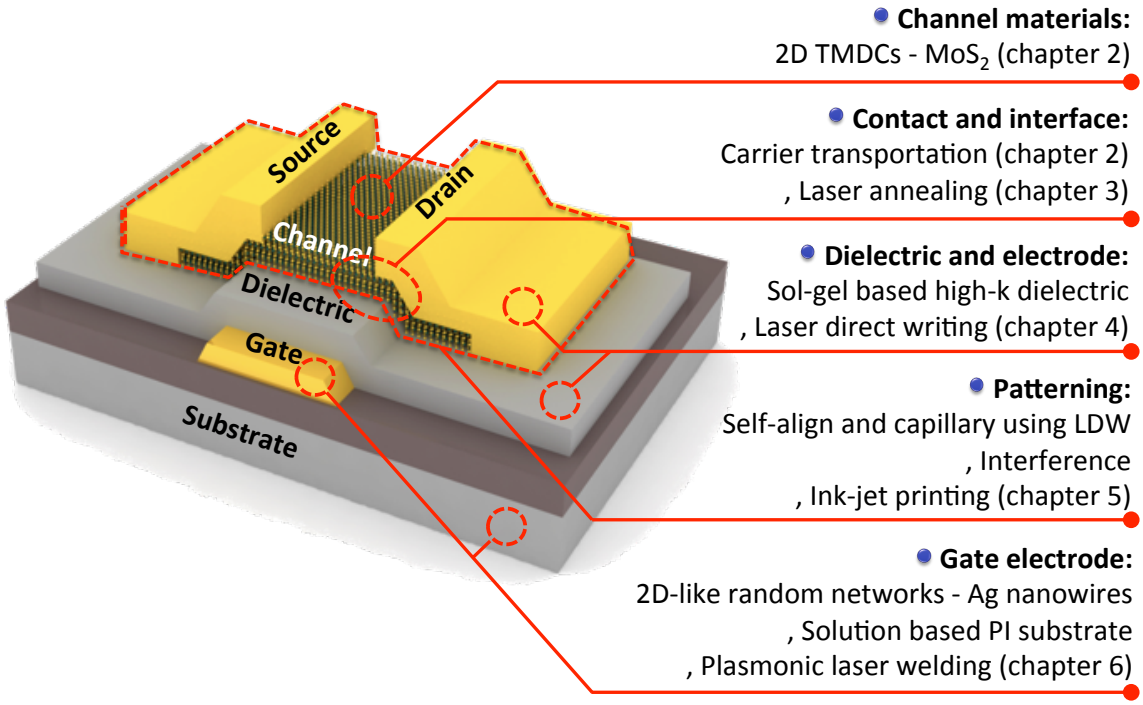

Figure 1.9 Organized schematics for the structure of this research and dissertation, showing the five technical focus areas on the TFTs: (1) 2D channel materials, (2) contact and interface, (3) dielectric and defining electrodes using LDW, (4) maskless small patterning (LDW and interference) with ink-jet printing, (5) 2D-like random networks using Ag nanowires and plasmonic laser welding process for the gate electrode.

Chapter 2

Physical Properties of 2D materials

2.1 2D Transition Metal Dichalcogenides (TMDs)

2D materials are a class of materials with the formula of MX_2 (M (transition metal) = Mo, W; X (Chalcogenide) = S, Se, Te) composed of vertically stacked layers held together by van der Waals interactions like graphene (**Figure 2.1**). The general symmetry structure of TMDs is hexagonal or rhombohedral, and the metal atoms have octahedral or trigonal prismatic coordination.[31]

Graphene, one of the 2D materials has been studied and attracted the most attention culminated in the award of the 2010 Nobel Prize in physics because of its outstanding mechanical, optical, and electrical properties, as well as its processability.[32-34] Despite these excellent properties, graphene's major drawback is its gapless band structure, which makes it difficult to use in electrical switching devices such as transistors. Furthermore, a great amount of effort to achieve a sufficient bandgap has created other issues, increasing fabrication complexity and reducing mobility.[35, 36] However, owing to the advent and the exploration of graphene, 2D atomic layers from other materials can be easily exploited in a extremely short period of time. Therefore, there are a substantial number of reports that demonstrate novel devices for a wide variety of applications and explore their novel properties range from insulating (e.g. hexagonal boron nitride, h-BN) to semiconducting (e.g. MoS_2, molybdenum diselenide $MoSe_2$, tungsten diselenide, WSe_2).[31] The extraordinary properties will be explored more detail in the **Section 2.2**.

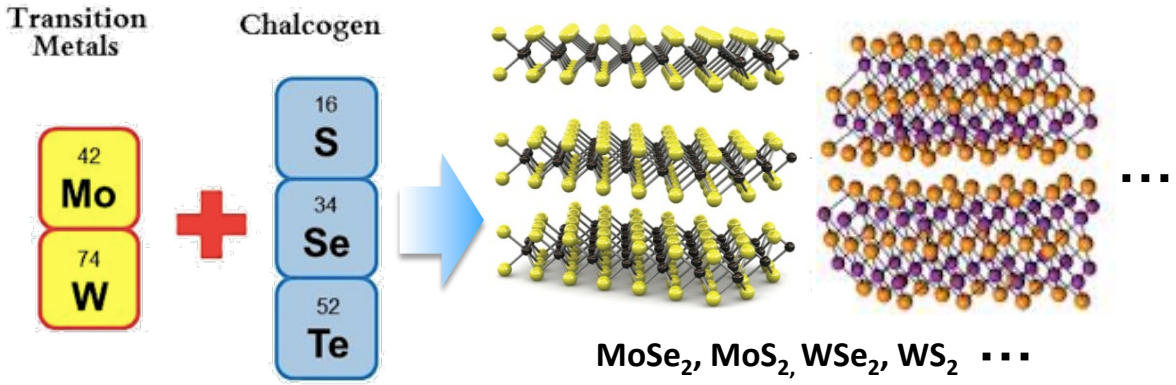

Figure 2.1 Combinations and structures for 2D materials with the formula MX_2, where M is a transition metal element from group IV, V or VI and X is chalcogen. (images from Google search)

2.2 Properties of 2D MoS_2

Among atomic layered 2D TMDs materials, MoS_2 has been widely used in numerous areas and has drawn attention as a promising alternative channel material due to the exotic electrical, optical, and mechanical properties. The electronic and optoelectronic applications of MoS_2 are highly dependent on the electronic properties (e.g. band structure, density of states).

2D MoS_2 has *n*-type semiconducting characteristics with a relatively large bandgap (direct (1.8 eV) or indirect bandgap (1.2 eV) depending on the exact number of atomic layers) compared to zero-gap graphene.[37-40] Note that the band structure of bulk MoS_2 has the top of valence band situated at Γ of the Brillouin zone and the bottom of conduction band halfway between Γ and K (indirect).[38-40] On the other hand, the band structure of single monolayer MoS_2 is situated at K point (direct) as shown in **Figure 2.2**.[38-40] Moreover, the band structure of monolayer MoS_2 is changed by the mechanical strains when 10% of the homogeneous biaxial tensile strain is applied; the bandgap is reduced and manipulated from a direct to indirect and from a semiconductor to metal.[41]

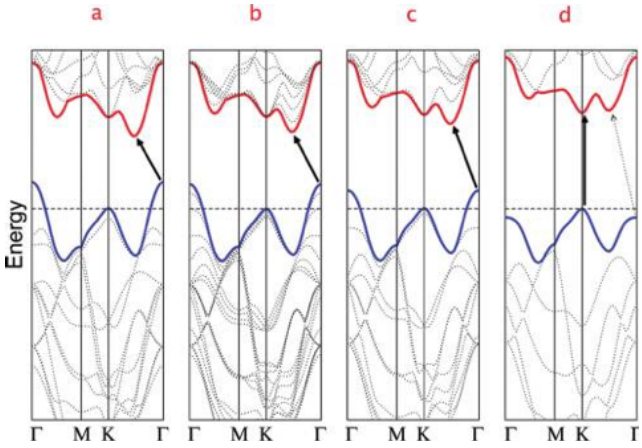

Figure 2.2 Calculated band structures of MoS_2: (a) bulk, (b) quadrilayer, (c) bilayer, and (c) monolayer. The top of valence band (blue) and bottom of conduction band (red) are highlighted. (image from A. Splendiani *et al.* Nano Lett. 2010) [40]

Besides interesting band structure, 2D MoS_2 shows attractive characteristics for the switching devices: high carrier mobility (~200 cm^2/Vs range at high-k hafnium oxide (HfO_2) and room temperature),[37,42] high on/off current ratio (I_{on}/I_{off}, ~10^6),[37,43] low subthreshold swing (SS, ~70mV per decade),[37,43] and absence of dangling bonds.[37] Also, because of 2D nature, MoS_2 with very thin atomic thickness (6.5 Å) can be easy to fabricate complex structure and has good mechanical flexibility. In addition, other distinctive properties are reported: spin Hall effect for valleytronics and spintronics,[44-46] lattice dynamics through two different structures (e.g. 1H-MoS_2, 2H-MoS_2),[47,48] magnetism.[49,50] However, these properties lie beyond the scope of this research and dissertation; I won't go into all properties of MoS_2.

The aforementioned exciting properties of MoS_2 lead to good switching behavior, can be fabricated into transistors using standard top-down nano/micro-fabrication process, and enable strong control of its carrier density by gate bias. Therefore, 2D semiconducting MoS_2 now creates various applications with performance far superior to devices made from current flexible semiconductors (e.g. organic semiconductors, solution-processed inorganic semiconductors): TFTs,[37,43] integrated circuits,[51] and sensors.[52-55]

2.3 Monolayer vs. Multilayer

The monolayer MoS_2 has direct band structure at K point of the Brillouin zone and has direct bandgap in the visible range. Therefore, very strong photoluminescence (PL) and large exciton binding energy are only present in a monolayer; these facts are promising for optoelectronic applications. Several different types of optoelectronic devices have been demonstrated including photodetectors, solar cells, and light emitting devices.[56] Moreover, because of high sensitivity to the strain force and gases (more specifically hydrogen, H_2), there are many sensor applications as well.[52-55]

However, high sensitivity to external surroundings sometimes has negative effects on flexible TFTs for the displays or circuits, which are fabricated and designed strongly and solidly against the external impacts. Except for multilayer MoS_2, it is well known that absorbed molecules on surfaces result in the degradation of the performances of single- or bi-layer MoS_2 transistors.[57,58] In this respect, multilayer MoS_2 appears to be apt for these applications. In addition, a few early reports suggest that multilayer MoS_2 can surpass single-layer MoS_2 in the TFT-based applications because it has a larger density of states and helps to create a larger channel carrier density (i.e. presenting multiple conducting channel), which boosts the current drive of field effect transistors (FETs) made using this system.[43] Also, multilayer is more well suited for practical fabrication process. For example, currently 8 generation (2160 × 2400 mm) or 10 generation (2880 × 3130 mm) glass is applied in the industrial field of the displays; using one 8 generation glass, we can make 6 number of 55 inch display. Monolayer with 1 nm thickness is very hard to make thin film onto such a large glass panel, by the way.

2.4 Effects of Temperature and Ambient Conditions: MoS_2 TFTs

For use in electronics of these multilayer MoS_2 TFTs, unfortunately, the carrier transport mechanism and molecule absorption effects, critically related to transistor performances, has not yet been intensively explored at realistic operating temperatures (the working temperatures of commercial displays rise to +50 °C, and the extended temperatures increase to +85 °C). Even though a few reports have studied on temperature-dependent characteristics, such as the effective Schottky barrier height, these papers only focused on the single- or bi-layer MoS_2 TFTs below room temperature.[59-61] Therefore, I report observed preliminary evidence of the dominant scattering mechanism and the temperature dependent performance of multilayer MoS_2 TFTs.[62]

From the measurements of the temperature-dependent conduction at practical working temperatures (from room temperature up to 350 °K), extracted drop-off rates of the mobility are helpful knowledge to use as the active channel materials of the thermistors. Also, to show the effect of operating ambient on the devices, the electrical characteristics in the linear regime (at low drain voltage, V_D) as a function of operating temperatures in air and in a vacuum (~10^{-5} Torr) are specifically investigated. It exhibits that the multilayer MoS_2 transistors are more stable and less sensitive to ambient, comparing to the very thin monolayer MoS_2 transistors.

2.4.1 Device preparation

Figure 2.3(a) shows a schematic architectural diagram for a fabricated multilayer MoS_2 TFT. A silicon dioxide (SiO_2) dielectric layer with a thickness of 300 nm was deposited by chemical vapor deposition (CVD) on a heavily doped *p*-type Si wafer (resistivity < 5×10^{-3} Ωcm). Multilayer MoS_2 flakes (~50 nm) were mechanically exfoliated from bulk MoS_2 crystals (SPI Supplies, USA), and transferred onto the deposited SiO_2 layer. For the source and drain electrodes, titanium (Ti, 10 nm) and gold (Au, 300 nm) were deposited by electron-beam evaporation and were patterned by conventional ultraviolet (UV) photolithography and lift-off techniques. Ti (~4.3 eV) was selected among the low work function materials because it has been suggested as a good contact for injection into the conduction band of MoS_2.[39] Furthermore, Ti has been suggested since it is a transition metal with *d* orbitals that blend constructively with Mo4*d* states. Therefore, this favorable interface geometry is expected to facilitate good bonding and allow maximized injection at the contacts by increasing the overlap between the states at the interface.[39] Lastly, for reducing the contact resistance and residue, fabricated devices were treated by thermal anneal process at 200 °C in a vacuum furnace for two hours with 100 sccm argon (Ar) and 10 sccm H_2. **Figure 2.3(b)** shows a 3D confocal laser microscope (LEXT OLS4000, Olympus) image of a fabricated multilayer MoS_2 TFT with the bottom gate structure. Measurements using an atomic force microscope (AFM) showed that the thickness of the MoS_2 channel was around 50 nm among the measured devices (inside **Figure 2.3(b)**).

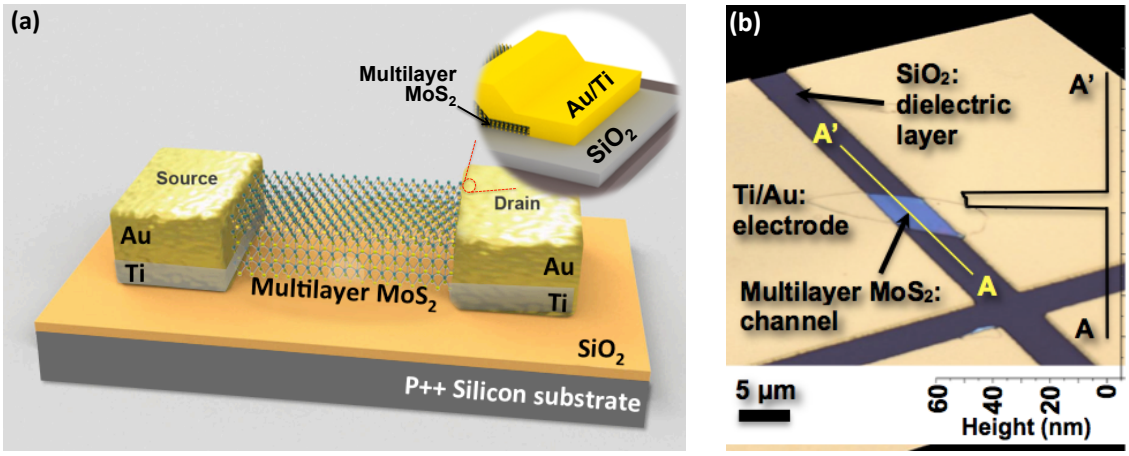

Figure 2.3 Multilayer MoS_2 TFT structure: **(a)** the cross-sectional schematic structure of a multilayer MoS_2 TFT with a 300-nm-thick SiO_2 gate dielectric. **(b)** The top view of a 3D confocal laser microscope image of a multilayer MoS_2 transistor after fabrication.

Figure 2.4(a) shows the drain current (I_D) versus drain voltage (V_D) curves for representative multilayer MoS_2 TFTs with a channel length of 4 μm and width of 5 μm, as a function of V_D in a range from 0 to 30 V with the selected gate voltage (V_G) ranging from -70 to +70 V in steps of 35 V. The fabricated multilayer MoS_2 TFTs exhibited conventional *n*-type behavior with negative threshold voltages (V_{TH}). An on/min current ratio (I_{on}/I_{min}) of ~10^7 and SS of 3.4 V/decade were obtained and the μ_{eff} in the saturation regime ($\mu_{eff\_sat} \approx 10.9$ cm^2/Vs extracted at V_G = -25 V, V_G-V_{TH} < V_D) was evaluated from a linear fitting of the curve of $I_D^{0.5}$ versus V_G at a fixed high drain voltage (V_D = 30.0 V) as shown in **Figure 2.4(b)**. Initially, our device exhibited the square-law behavior at low V_G (-40 V to +15 V), well. However, the device shown saturated I_D for V_G above -15V, even though V_D did not reach V_G-V_{TH}. This notes that other authors have proposed that this strong saturation in output characteristics can partially be explained by the self-heating effect (corresponding to the intermediate regime) before reaching the negative I_D-V_D slope regime (where the self-heating effect is dominant).[63]

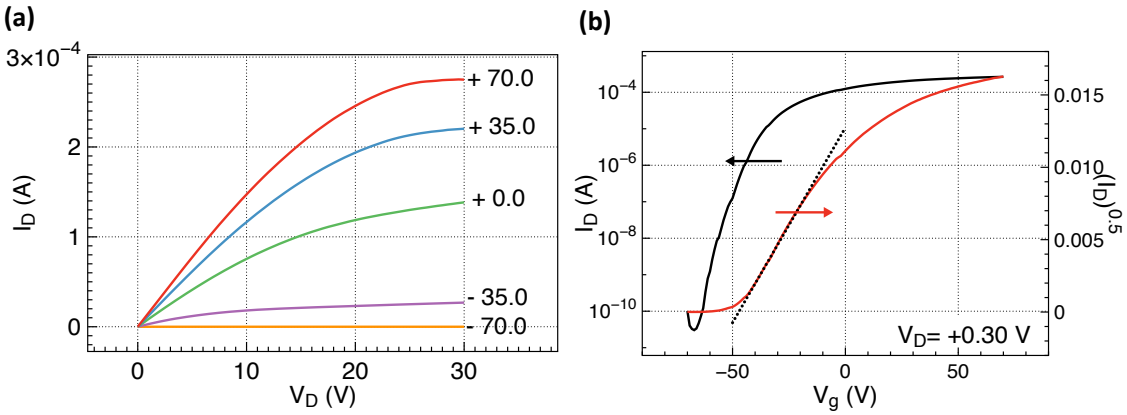

Figure 2.4 Representative electrical characteristics of multilayer MoS_2 TFT at room temperature: **(a)** the plot of I_D-V_D. **(b)** Plots of I_D-V_G (left axis) and $I_D^{0.5}$-V_G (right axis).

2.4.2 Results and discussion

To further understanding the carrier transport mechanisms in multilayer MoS_2 TFTs, I investigated the effect of the ambient conditions (in air and in a vacuum) in combination with the variable operating temperature measurements. The transfer curves, I_D-V_G, were obtained in the linear regime (at a low V_D of 0.1V) to create a uniform charge density in the accumulation layer and the field effect mobility in the linear regime ($\mu_{eff\_lin} \approx 14.0$ cm^2/Vs) was calculated at room temperature by the MOSFET square-law model:

$$\mu_{eff} = \frac{dI_D}{dV_G} C_i \times \frac{1}{V_D} \tag{2.1}$$

where C_i is the insulator capacitance per unit area. Note that Das and others suggested that the maximum potential of back-gated multilayer MoS_2 TFTs with the thickness in the range of 30 ~ 60 nm and Scandium (Sc) contacts would be limited around 50 cm^2/Vs due to involving

interlayer coupling resistances.[64] Therefore, the extracted μ_{eff} both in saturation and linear regimes are lower than that of reported results, but nevertheless we can boost the μ_{eff} through incorporating metals with lower work function (like Sc (3.5 eV)) than Ti (4.3 eV) / Au (5.1 eV) for reducing the Schottky barrier and through a high-k dielectric layer for minimizing the effect on Coulomb electron scattering. The contact resistance factor should be well separated from measured extrinsic characteristics to exploit the transport mechanism inside the MoS_2 semiconductor channel. Here, the Y function method (YFM) was hired to extract the intrinsic low field mobility (μ_0, the maximum available mobility in this system) and contact resistance (R_c):[65-67]

$$Y = \frac{I_D}{\sqrt{G_m}} = \sqrt{\frac{W}{L} C_i \mu_0 V_D} \times (V_G - V_{TH}) \tag{2.2}$$

where C_i is the insulator capacitance per unit area. The μ_0 can be extracted from the slope of Y-function (discussion later in detail). Note that the slope of the plot is 1.42×10^{-4} as shown in **Figure 2.5(a)** and the extracted μ_0 at a low V_{DS} of 0.1 V is 14.6 cm^2/Vs. If the contact effect is dominant, the extracted μ_{eff_lin} should be significantly lower than μ_0 and the non-linear I_D-V_D curves should be presented at low V_D as well. However, μ_0 (14.6 cm^2/Vs) was only 3% more than the extrinsic μ_{eff_lin} (14.0 cm^2/Vs) at the same V_D. Furthermore, the linear I_D-V_D curves were presented clearly at low V_D. Another interesting aspect is that the extracted μ_{eff_lin} (14.0 cm^2/Vs) is higher than μ_{eff_sat} (10.9 cm^2/Vs). First, this may originate from the fringing effect and/or the scattering effect. The fringing currents depend on V_D, the 1:1 aspect ratio of the channel would overestimate the calculated μ_{eff}, particularly when the MoS_2 flakes exceed the contacted channel width. Second, it is well known that the μ_{eff_sat} is commonly less affected by the R_c than μ_{eff_lin}. Therefore, the μ_{eff_lin} should be lower than μ_{eff_sat} in contact resistant dominant system. To investigate this phenomenon more specific, the R_{c_max} (23.4 kΩ) was estimated from the mobility attenuation factor ($\theta = \mu_0 C_i R_c W/L$).[66,67] θ can be extracted by following equation:[65,66]

$$g_m = \frac{\partial I_D}{\partial V_G}, (V_D = const) = \frac{W}{L} C_i \frac{\mu_0}{[1+\theta(V_G - V_{TH})]^2} \times V_D \tag{2.3}$$

From **Equation (2.3)**, we can know that the θ can be calculated from the slope of the plot ($1/g_m^{1/2}$ versus V_G) and the linear fitted slope is 33.16 as shown in **Figure 2.5(b)**. Also, to calculate the channel resistance (R_{ch}) and to compare with R_{c_max}, the total resistance ($R_{total}=R_c+R_{ch}$) was calculated from I_D-V_D curves at low V_D and the obtained R_{total} and R_{ch} were 333.4 kΩ and 310 kΩ, respectively. For double-checking the value of R_{ch}, we directly calculated from induced charge carriers, $R_{ch}=L/(\mu_0 W C_i (V_G - V_{TH}))$ once again. Note that the reconfirmed R_{ch} was ~250 kΩ and both values of R_{ch} are larger than R_c in this system. Therefore, it can be possible that the effect of scattering is more significant than the effect of R_c.[68] I address these features in more depth later with the transconductance (G_m) and the $\mu \sim T^{\gamma}$ law, specifically.

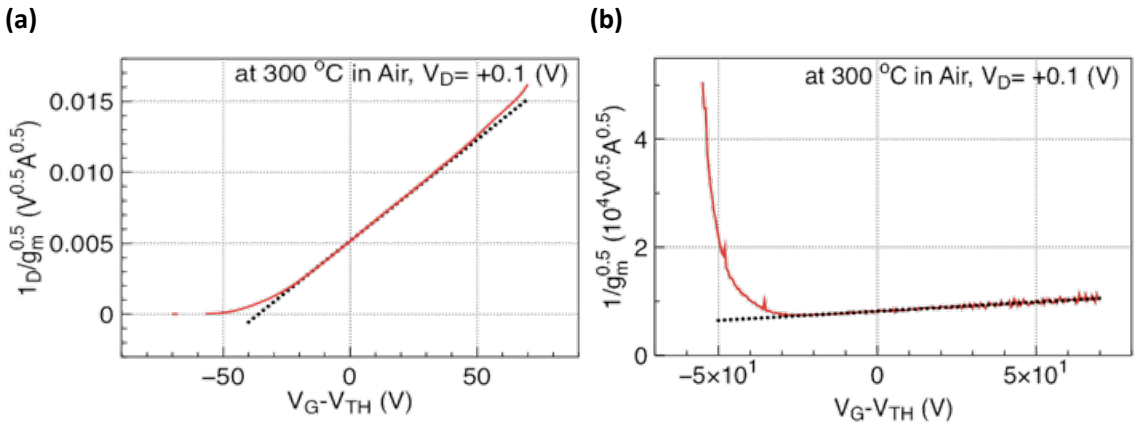

Figure 2.5 (a) The $I_d/g_m^{0.5}$ plot with linear fitting in ambient condition. **(b)** The plot of $1/g_m^{1/2}$ with respect to gate voltage with linear fitting for evaluation of mobility attenuation factor, θ.

To describe the electrical characteristics for the variable operating temperatures, two regimes (green and blue regions) based on the zero temperature coefficient (ZTC) point in the on-state were defined in **Figure 2.6(a)** and **2.6(b)**. At the ZTC gate voltage, the devices exhibit constant DC performance with operating temperature. However, the fabricated TFTs did not show a clear ZTC point. Thus, the minimum point of *dI/dT* was set as a cut-off point to divide the two regimes. Qiu and others reported that a Φ_B was formed between the Ti/Au metal contact and the MoS_2 semiconductor in their research; the structure investigated was the same as our structure.[59] The Schottky barrier height was ~65 meV, which exceeded the thermal emission energy at room temperature.[59,69] Therefore, at low V_G (below V_{TH}), these barriers partially hindered the flow of carriers. However, when the operating temperature increased, the carriers easily overcame these barriers by thermionic emission.[70] This caused I_{min} to rise.

Figure 2.6(c) and **2.6(d)** show that the G_m decreased at high V_G in this device, regardless of measured temperatures. Such G_m decrease might be due to dominant R_c and/or phonon scattering.[65] As V_G increases, the influence of the injection barriers can be reduced, then it has become decreasing the temperature dependence. However, G_m rolled off at high V_G (blue region) as shown in **Figure 2.6(c)** and **2.6(d)**. As discussed in previous section, the scattering effect, which is inversely proportional to the operating temperatures and at high field, was having much effect on our system. To confirm the phonon scattering impact on performances, the output characteristics were investigated as a function of temperatures. Phonon scattering dominated by the $\mu \sim T^r$ law has two different types of phonon scattering corresponding to the exponent parameter (*r*): acoustic phonon scattering ($-1 < r < 0$) and optical phonon scattering ($r < -1$). In our device, the extracted *r*-values in air and in a vacuum are -3.5 and -1.7, respectively. Therefore, we assume that optical phonon scattering is dominant in these systems, similar to other observations.[43,71] Furthermore, at low V_G and above V_{TH} (green region), the drain current seems to be slightly increased due to the dominant negative V_{TH} shift, as shown in **Figure 2.6(a)** and **2.6(b)** as a function of the operating temperature. The combination of increased I_{min} by thermionic emission and reduced I_{on} by phonon scattering contributes to the decreased I_{on}/I_{min} ratio.

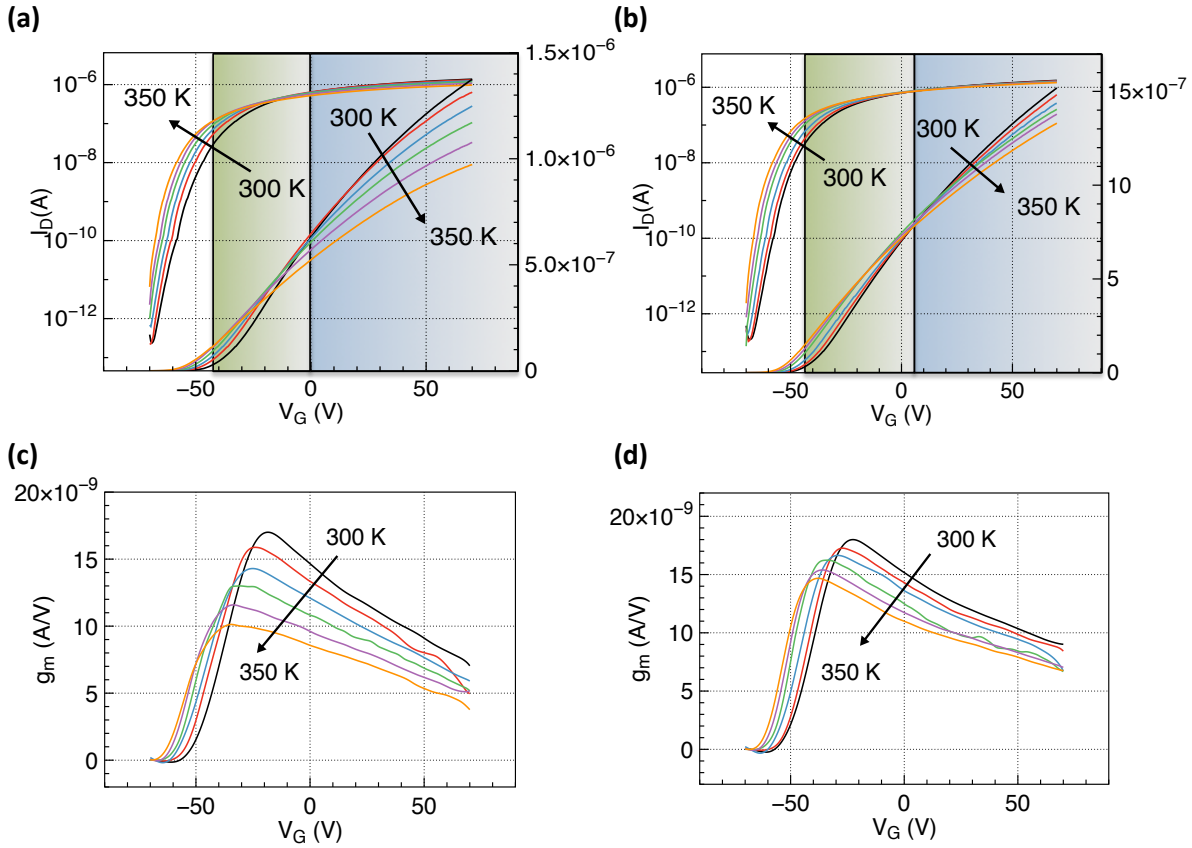

Figure 2.6 The typical I_D-V_G transfer characteristics of the fabricated multilayer MoS_2 transistor at V_{DS} of 0.1 V **(a)** in air and **(b)** in a vacuum at different operating temperatures (T = 300, 310, 320, 330, 340, and 350 K) in both log and linear scales. Transconductance versus V_G curves **(c)** in air and **(d)** in a vacuum at different operating temperatures.

The estimated SS, V_{TH}, μ_{eff_lin}, and μ_o were plotted in **Figure 2.7(a)** and **2.7(b)**, respectively, corresponding to different temperatures and ambient. The estimated SSs are relatively larger than those of the conventional metal oxide FETs due to interface trap density between semiconductor and insulator layers. In addition, aforementioned Φ_B (at low V_G, below V_{TH}) can lead a relatively large SS originated from the tunneling through a barrier.[72] Regardless of the ambient, the SS values are almost same. Even though the thickness of multilayer MoS_2 is around 50 nm, the actual channel is few layer near the bottom. This is why the thicker multilayer MoS_2 TFTs showed less effects of ambient conditions on interface quality as determined by SS values.[73]

Temperature dependent characteristics of V_{TH} are exhibited in **Figure 2.7(a)**. V_{TH} shifts toward the negative direction as the temperature increases. This behavior is observed in most semiconductor systems due to an increase in thermally generated carriers, resulting in a shift in the Fermi level in the semiconductor. The average rate of shift reached -0.32 V/K (300-350 K) regardless of the ambient conditions. Additionally, V_{TH} was higher in air than in vacuum.

One possible explanation is that the oxygen and water molecules on the surface of MoS_2 semiconductors could be adsorbed from the ambient air,[57,59,74] and they could trap the charge carriers from the conduction band. This could make depleted channels and induce a positive V_{TH} shift.[74] Large mobility drop-off rate in air (0.12 cm^2/VsK), comparing to the mobility drop-off rate in vacuum (0.07 cm^2/VsK) was exhibited. The phonon scattering limited mobility have been shown the temperature and the effective electric field dependency.[75] The adsorbed oxygen and water molecules might be attributed to the increased effective electric field and phonon mode, confirmed by the increased parameter *r*. On the other hand, the μ_0 extracted from Y-function shows almost identical values, comparing to extrinsic mobility and drop-off rates, regardless of the operation temperatures in **Figure 2.7(b)**. It can interpret that the transport mechanism of this system can be the phonon scattering of MoS_2 channel, not limited by the R_c. Furthermore, the ratio ($\mu_{eff\_lin\_vacuum}$ / $\mu_{eff\_lin\_air}$) is ~0.95 at 300 K. This is higher than the previously reported values.[57,59,74] This observation is consistent with the fact that the impact of absorbed oxygen and water molecules on the fabricated device performance is weaker than that for thinner MoS_2 layers, because the impact of attached molecules on a semiconductor surface in a bottom-gated device is normally related to the surface to volume ratio.[76]

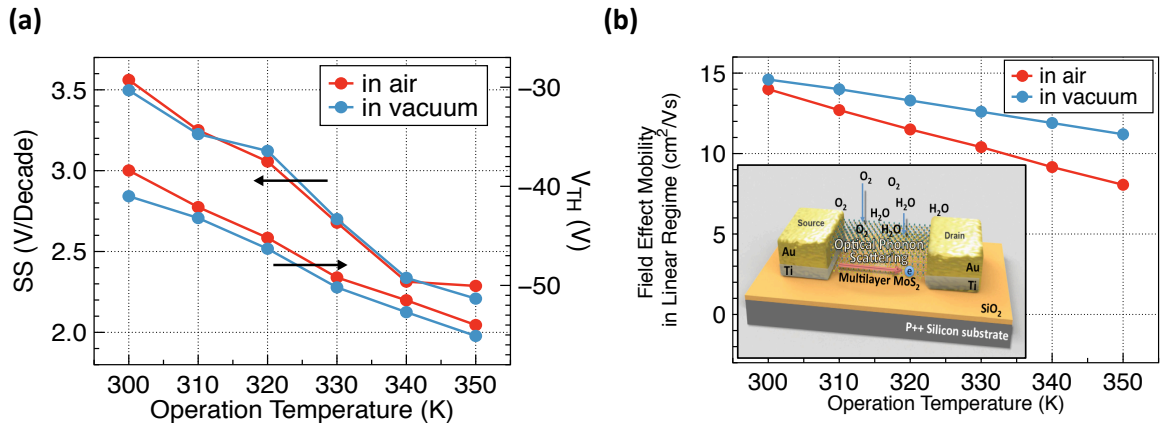

Figure 2.7 The operating temperature dependence of the SS, V_{TH}, and μ_{eff_lin} and μ_0 at V_{DS} of 0.1 V **(a)** in air and **(b)** in a vacuum at different operating temperatures.

2.5 Analysis of Flicker Noise: MoS_2 TFTs

Low-frequency noise (LFN) analysis can help analyze the quality of semiconductors, oxides, and oxide–semiconductor interfaces. This technique measures conductivity fluctuations in the transistor channel; these fluctuations can be caused by mobility fluctuations from phonon scattering or/and Coulombic scattering or by carrier trapping and de-trapping.[77] Electrical noise limits the signal-to-noise ratio (SNR) of a device, particularly for the sensor applications. In such small size regimes, as the surface-to-volume ratio of 2D layered semiconductor devices increases, surface adsorbates and atomic-scale structural fluctuations greatly influence their electronic noise.[78] Many researchers have explored nanostructured devices (0D to 2D) and

investigated their low-frequency electrical noise, where 1/*f* noise (also known as flicker noise) dominates.[79-82]

While 1/*f* noise has been studied in monolayer MoS_2 transistors,[83] electronic noise in devices fabricated from multilayer semiconducting MoS_2 has not yet been explored. To further optimize multilayer MoS_2-based devices, we must better understand their transport mechanisms and semiconductor/dielectric interfacial properties. In this section, I report on the fabrication and performance of multilayer MoS_2 field-effect transistors (FETs) and examine the quality of their interface as well as the energy distribution of carrier trapping/scattering sites by measuring LFN.[84] Based on these observations, I discuss the origin of the 1/*f* noise in these devices.

2.5.1 Device preparation

Figure 2.8(a) shows a cross-sectional schematic of a multilayer MoS_2 FET. To fabricate these FETs, a 300-nm-thick SiO_2 dielectric layer was first deposited by thermal chemical vapor deposition on a heavily doped *p*-type Si wafer (resistivity < 5×10^{-3} Ω·cm). Bulk MoS_2 crystals (SPI Supplies, USA) were mechanically exfoliated to obtain the multilayer MoS_2 flakes. These flakes were transferred onto the SiO_2 layer to form a semiconducting channel. The source and drain were Ti/Au electrodes (10/300 nm) deposited by electron-beam evaporation at room temperature. To pattern the source and drain, conventional UV photolithography and lift-off was used. A confocal laser microscope (LEXT OLS4000, Olympus) was used to image the structure, as shown in **Figure 2.8(b)**. The thickness of the exfoliated MoS_2 channel was 40–50 nm, measured by AFM, as shown in **Figure 2.8(c)**.

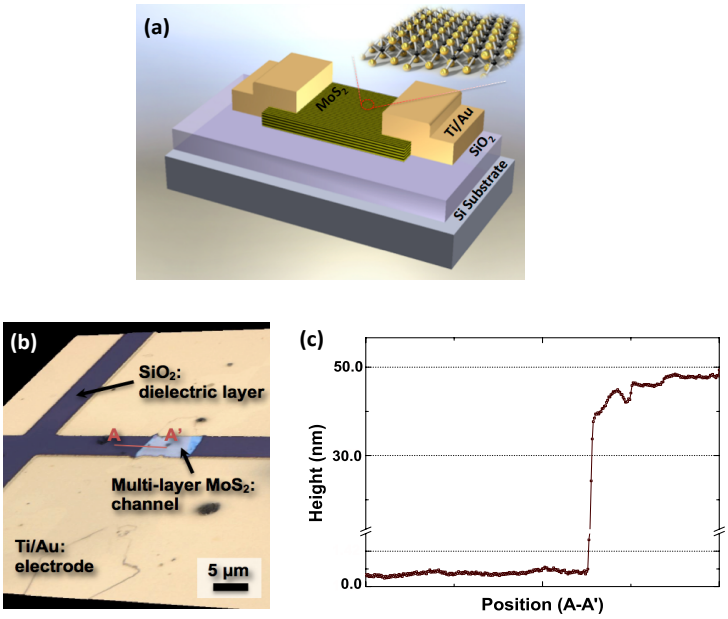

Figure 2.8 Structure of the multilayer MoS_2 FET: **(a)** Cross-sectional schematic of a multilayer MoS_2 FET with a 300-nm-thick SiO_2 gate dielectric. **(b)** Top-view 3D confocal laser micrograph of a fabricated multilayer MoS_2 transistor (L_{ch} = 5 μm, W = 6.9 μm). **(c)** AFM height profile of a mechanically exfoliated multilayer MoS_2 flake (shown in (b) as the A'–A region, marked by an arrow).

I measured the 1/*f* noise in the power spectral density (PSD) of the drain current in the multilayer MoS_2 FETs in the following way. The current fluctuation across the device was amplified with a low-noise transimpedance amplifier (BTA9812B), and the 1/*f* noise was characterized by a spectrum analyzer (HP 35670A). DC bias for the TFTs during the 1/*f* noise measurement is provided by a semiconductor parameter analyzer (HP 4156) through low pass filters (f_{3dB} = 1 Hz). **Figure 2.9(a)** and **2.9(b)** shows the transfer and output characteristics of the MoS_2 FETs. The transistors exhibited good switching behavior ($I_{on}/I_{off} > 10^5$), and the linear relationship between the drain current and voltage (**the inset of Figure 2.9(b)**) demonstrates that the effect of the source/drain Φ_B was minimal. The PSD was measured in linear mode operation to more uniformly distribute the carriers along the channel. The measured linear mobility was 20.27 $cm^2V^{-1}s^{-1}$. All electrical measurements were performed in air at room temperature.

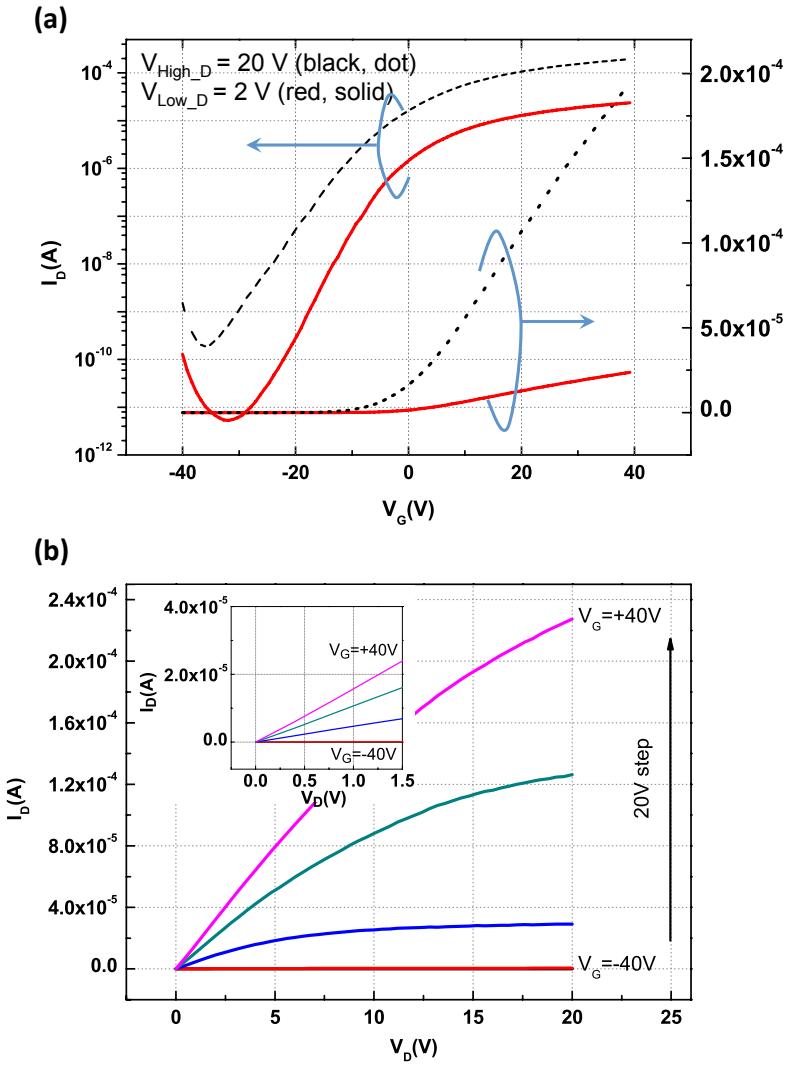

Figure 2.9 Representative characteristics of the multilayer MoS_2 FETs for various drain and gate voltages: **(a)** Transfer characteristics and **(b)** output characteristics; the inset shows the output characteristics in the linear region.

2.5.2 Results and discussion

Figure 2.10(a) shows the measured normalized drain-current PSD of the FETs after background chamber noise is subtracted. The gate bias ranged from −15 V to 25 V over 5 V increments, a wide enough range to cover various operation regions, from the sub-threshold region to the fully ON region. It is important to cover these operation regions because carrier transport and noise characteristics are affected by changes in the active trap distribution, which is modulated by Fermi level shifts. In these FETs the noise decreased monotonically with frequency, matching typical LFN behavior ($1/f^{\gamma}$).

By carefully analyzing the measured noise, though, I found that γ depended on the gate bias, as shown in **Figure 2.10(b)**. At negative gate bias (i.e., lower than V_{TH} in this device), γ was >1, but as V_{GS} increased and became greater than V_{TH}, γ decreased and eventually stabilized to ≈ 0.9.

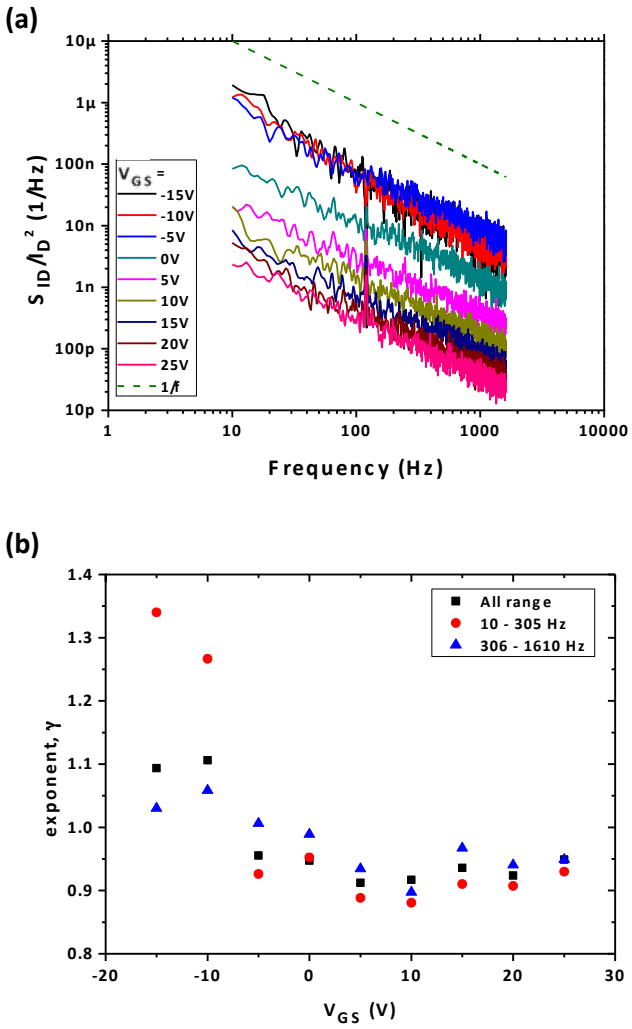

Figure 2.10 (a) Normalized drain-current PSD of multilayer MoS_2 TFTs at various gate biases and a constant drain bias of 2 V, measured from 10 to 1610 Hz in 1 Hz increments. **(b)** Values of the γ exponent from $1/f^{\gamma}$, extracted from the PSD results in (a).

To improve the accuracy of the extracted value, I extracted γ from the normalized PSD over full and partial ranges of the measured frequencies, but all measured data had the same trend. The γ exponent is an important parameter that is closely related to the trap distribution, an origin of flicker noise.[85-87] D'yakonova et al. showed how $1/f$ noise is connected to the structural quality of the semiconductor used; they found that, as more structural defects were introduced to gallium arsenide (GaAs) by uniaxial stress, the noise level of the FET increased and the slope of the *1/f* noise became steeper. Dimitriadis et al. showed in their LFN measurements of polycrystalline silicon TFTs that γ changes with gate bias. In McWhorter's carrier number fluctuation (Δn) model in single-crystalline silicon MOSFETs, the $1/f$ noise was computed by the summation of Lorentzian distributions at different roll-off frequencies; this noise originated from spatially uniformly distributed traps within the gate oxide with different tunneling depths during the trapping/de-trapping process, which was later observed in nanoscale silicon MOSFETs as random telegraph noise.[88-91] These results revealed that if the distribution of relaxation times is non-uniform, the overall noise deviates from the ideal $1/f$ PSD relationship. For example, if slow traps dominate, then lower frequency noise will be amplified, increasing the slope; if fast traps dominate, the reverse occurs. McWhorter's carrier number fluctuation model, modified based on the origin of traps, agrees well with the data measured in the current letter from the multilayer MoS_2 FETs. Our device contained active slow traps at low gate bias, increasing γ, although the exact origin of these traps is unknown. As V_G increased the Fermi level shifted, filling the slow traps and decreasing γ, which eventually saturated at ≈ 0.95.

This result can be supported in other ways. For example, the Hooge parameter (α_H) shown in **Equation (2.4)** is closely related to the degree of the *1/f* noise being studied.

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H}{N_{total}} \frac{1}{f^\gamma} \tag{2.4}$$

where S_{ID} is the drain-current noise PSD, I_D is drain current, and N_{total} is the total number of free carriers in the sample. Based on N_{total}, defined as $C_{ox}(V_G - V_{TH})/q$, where C_{ox} is the total gate capacitance considering area, V_G is the gate-source voltage, and q is the elemental charge, α_H was extracted as shown in **Figure 2.11(a)**. Even when defining V_{TH} in various ways, the trends remained the same. α_H was extremely large in the subthreshold region and drastically decreased as the gate bias increased until it matched V_{TH}. This result supports that the amount of active traps which cause the carrier number fluctuation decreases more significantly below V_{TH} since the increased gate bias fills traps; it agrees with the change of the exponent value aforementioned. Note also that α_H gradually decreased as the gate bias increased, even after the γ exponent stabilized beyond a zero bias. Studies have shown that the α_H can depend differently on gate bias.[81,92] As suggested by the carrier number fluctuation model, we observed that α_H monotonically decreased as V_G increased, rather than remaining constant, as suggested by the mobility-fluctuation model.

Note, in **Figure 2.10(a)** and more clearly in **Figure 2.11(b)**, the change in normalized drain-current noise PSD with gate bias (and thus with drain current). This behavior shows that the normalized PSD, an indicator of the relative strength of the drain current noise to the DC drain current signal, was fairly constant at low drain current and gate bias (the sub-threshold

region) and began decreasing monotonically as the gate bias increased, increasing the SNR. Based on detailed analyses by Ghibaudo and Ghibaudo et al.,[93,94] the drain current spectral density can be described in terms of contributions from Δn and mobility fluctuation ($\Delta\mu$) noise:

$$S_{ID} = g_m^2 S_{Vg} + g_d^2 S_{Vd}, or\ \frac{S_{ID}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{Vg} + \frac{g_d^2}{I_D^2} S_{Vd} \quad (2.5)$$

The form of this equation illustrates how the carrier fluctuation is linked to the gate voltage spectral density (S_{VG}) by carrier trapping/de-trapping in the g_m as well as how the drain-current PSD is correlated through the output conductance (g_d). Therefore, if the Δn mechanism dominated, it would affect the first term of **Equation (2.5)**.[95] **Figure 2.11(b)** shows similar trends for both normalized noise and g_m^2/I_D^2, supporting the dominance of the Δn model in these devices.

However, it has recently been reported that the main noise mechanism in single-layer MoS_2 transistors is the mobility fluctuation based on the analysis of extracted $1/A$ parameter, which also explains how the α_H is affected by gate bias.[81,83] Note that A parameter is defined from the equation $S_{ID}=A\cdot(I^n)/(f^\gamma)$, where n is the empirically obtained value from Sangwan *et al*.[83]

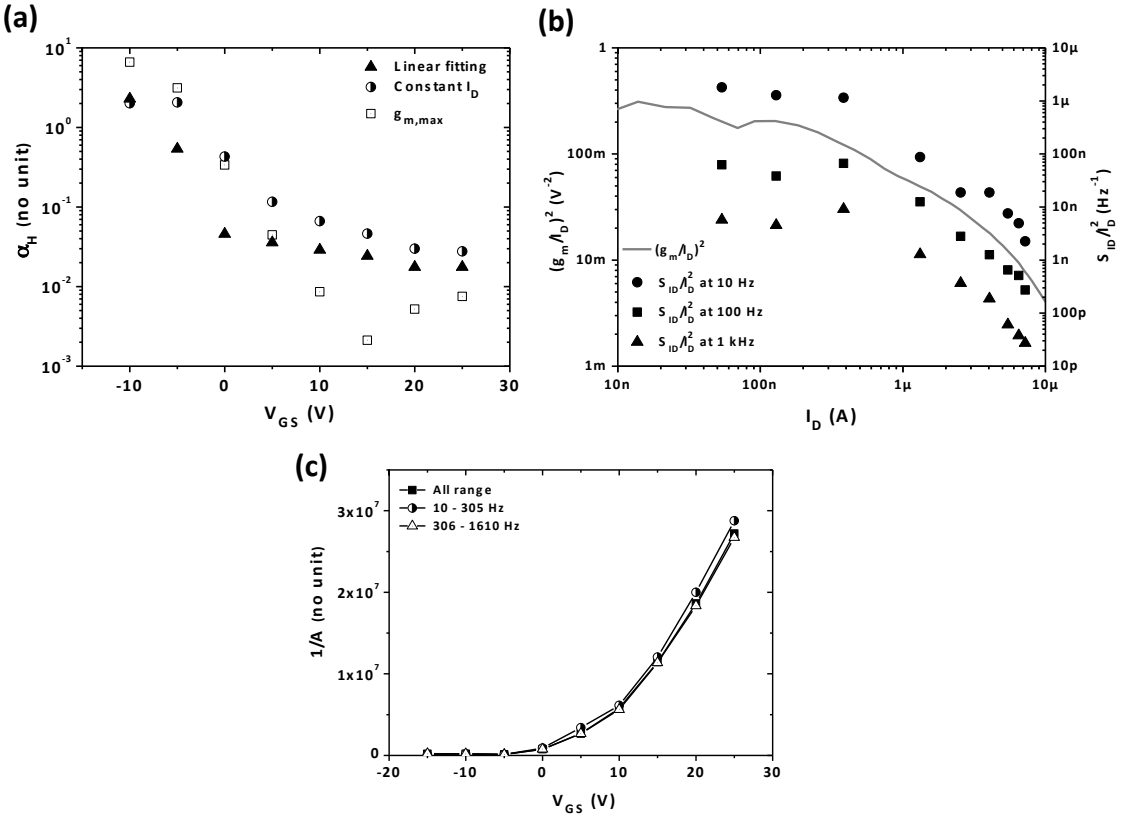

Figure 2.11 (a) The α_H as a function of gate bias. **(b)** $(g_m/I_D)^2$ and normalized drain-current PSD (S_{ID}/I_D^2) as functions of I_D at various frequencies. **(c)** The $1/A$ parameter as a function of gate bias.[81,95]

For the multilayer MoS_2 FETs, our analysis of the $1/A$ parameter (**Figure 2.11(c)**) over a broad operation region exhibited a super-linear or near-quadratic relationship with gate bias, an expected behavior if the $1/f$ noise is dominated by Δn. In this multilayer MoS_2 FETs, the α_H in ambient conditions in the fully ON regime was on the order of 10^{-2}; this value is comparable to that measured from single-layer MoS_2 FETs under vacuum and far better than that measured from single-layer MoS_2 FETs in air.[83] The additional layers of MoS_2 on top of the first layer at the gate–dielectric interface may have prevented surface adsorbates from significantly affecting the transistor channel.

2.6 Summary

The electrical characteristics of the multilayer MoS_2 transistors at real operating temperatures (from room temperature to 350 K) were shown, and the impact of ambient conditions on device performance was revealed. By comparing μ_{eff} of the transistors with increasing operating temperatures, I determined that μ_{eff} was limited by phonon scattering at high operating temperatures and was augmented by thermionic emission and generation at low gate voltages, thus reducing I_{on}/I_{off}. These channel mobility drop-off rates in air and in a vacuum reached 0.12 cm^2/VsK and 0.07 cm^2/VsK, respectively; the rate of degradation is steeper in air than in a vacuum due to boosted phonon mode by the adsorbed oxygen and water molecules. Note that the adsorbed oxygen and water created more defect sites or impurities in the MoS_2 channel, which can lead another scattering of the carriers. In addition, at room temperature, ambient conditions had little influence on the current density and μ_{eff} of multilayer MoS_2 channels compared to those of single or thinner MoS_2-based transistors. This is because the multilayer MoS_2 had a smaller surface to volume ratio, thus limiting the effect of surface states on the transport in the underlying channel.

On top of that, the LFN of mechanically exfoliated multilayer MoS_2 transistors was studied. I found that the $1/f$ noise was dominated by carrier number fluctuation. However, I was not able to determine the origin of the active traps, particularly the slow traps left unfilled at low gate biases. These traps must be further studied to optimize the fabrication of these devices in order to improve their carrier transport and SNR. The LFN characteristics of the current multilayer MoS_2 FETs in air were far better than those reported for single-layer MoS_2 FETs in air based on the much smaller α_H of our multilayer MoS_2 FETs, which provides an additional benefit of using multilayer structures; The multilayer MoS_2 structure had better noise immunity than a single-layer in air.

Chapter 3

Pulsed Laser Annealing for Flexible/Transparent MoS_2 TFTs

3.1 Metal-Semiconductor Junctions: Contacts

To realize the proper electrical characteristics of FET, the quality of the contact and interface must be improved because they can substantially distort the extracted mobility, especially for materials with low densities of states like MoS_2, which has been considered a channel material for high speed and/or flexible devices and a component material to improve the performance of conventional Si devices. In other words, for achieving high performance MoS_2 TFTs, we should consider metal-MoS_2 junctions, which are indispensable to the structure of TFTs, because non-ideal electric contacts on MoS_2 can form Φ_B at the junctions, and the undesirable contacts can hamper the inherent electrical characteristics of MoS_2.[53,96,97]

In order to reduce R_c and Φ_B between metal electrodes and MoS_2, various efforts have been reported and suggested: doping,[98] the use of scandium metal with a low work function,[64] and thermal annealing.[37] However, there are challenges and limitations to move forward in flexible electronics technologies. The doping stability of highly doped interfaces significantly limits their commercial feasibility since the chemical doping effect decreases gradually over time. Furthermore, scandium metals have little commercial appeal because they have been classified as a rare earth element and difficulties have been encountered in the preparation of metallic scandium. In addition, conventional high-temperature thermal processes are not compatible with commonly used flexible substrates (e.g., PEN, PET) because of their low thermal budget (< 200 °C). Since conventional thermal annealing affects the entire wafer, heat can also damage to the components or sensitive parts where thermal effects should be avoided; high thermal annealing processes could lead to deformation in plastic substrates. Therefore, we need other alternative methods to solve the issues.

3.2 Pulsed Laser Annealing

Unlike conventional thermal annealing, which affects the entire panel including unwanted areas in which the annealing process should be excluded, the irradiation of a pulsed laser with high energy density and short wavelength onto a metal electrode leads to the thermal annealing effect in a small, locally confined area that requires high temperature without extreme thermal damage (see **Section 1.4** for detailed explanations).[29]

Despite these fascinating features, the laser annealing process has been employed to different fields and applications. For examples, pulsed laser annealing has previously been used for mitigating the lattice damage caused by ion implantation of dopant atoms in semiconductors. However, in these earlier studies, the laser annealing technique was only applied to rigid applications and to conventional semiconducting materials (Si and germanium, Ge).[99-101]

In this chapter, the pulsed laser annealing process is introduced and suggested as a promising technology, especially for the flexible/wearable applications. Also, the effects of pulsed laser annealing of the metal contacts in MoS_2 transistors using picosecond ultra-fast pulsed laser with high-repetition rate (80 MHz) are investigated.[102,103]

3.3 Model of Thermal Analysis for Pulsed Laser Annealing

3.3.1 Ultra-fast electron dynamics

Profound understanding of ultra-short laser pulse induced temperature field requires detailed knowledge of the fundamental interactions between laser light (photons) and matter (electron and phonon systems). In metals, initially electrons primarily absorb the photon energy of the laser. For example, in the Au film with the thickness of 400 nm, the optical absorption depth is about 16.3 nm.[104] The electron system temperature rises instantaneously in response to the applied photon flux. Thermalized hot electrons diffuse into the material and transfer their energy to the lattice (within $10^{-12} \sim 10^{-10}$ s) until the electron and lattice temperatures equilibrate through electron-phonon coupling. This equilibration occurs within the pulse for pulse lengths in the range 10 to 60 ps.[105] Note that this thermal equilibrium time of the electron and lattice is about 40 ps (for Au).[106] Therefore, the temperatures of electron and lattice are different during the single pulse duration (12 ps) applied in the experiment. Consequently, the hot electron diffusion length is deeper than both the optical absorption depth and the heat diffusion length $\delta = \sqrt{4 \cdot \alpha \cdot dt}$ (where δ is the depth of heat penetration, α is the diffusivity of materials, and *dt* is the pulse duration).

In order to obtain a more accurate predictive solution, the two-temperature model (TTM) could be applied in this transient non-equilibrium case.[107] However, the TTM model that is by itself an approximation of the Boltzmann transport equation has been widely used to understand the origin of ultra-short electron dynamics under single laser pulse excitation of

width 10^{-15} ~ 10^{-12} s. Prediction of the transient temperature distribution induced by high repetition rate pulsed laser over a long time scale as in this system by using the TTM poses a significant challenge due to the required prohibitively long computing time. In this 80 MHz repetition rate case, we have to compute the TTM system of equations over 80,000,000 pulses in order to analyze only one second. Although the amplitude of the ps duration temperature spikes would be smaller by the TTM model, the heat accumulation that is driven by thermal diffusion would not differ from the presented thermal model prediction. In essence, the heat accumulating regions would stay the same, with the upper limits of the superposed temperature field envelopes.

3.3.2 Computation of temperature distribution

The temperature distribution was calculated by 3D Finite-Difference Methods using COMSOL Multiphysics at a specific position when picosecond pulsed laser source is applied under this experimental condition. The equilibrium temperature approximation is adopted since it reduces the required computational cost. As previously noted, the assumption of equilibrium temperature would overestimate the transient temperature. However, the approximate thermal solution shows good agreement with the results of real laser damage test (see **Figure 3.3(c)** at the **Section 3.4.3** in detail).

To calculate the approximated temperature distribution inside laser-heated Au electrode, the following heat flow equation is used:

$$\rho C_p \frac{\partial T}{\partial t} - \nabla(\mathrm{k}\nabla\mathrm{T}) = Q(x,y,z), \tag{3.1}$$

where ρ is the density, C_p is the specific heat, k is the thermal conductivity, and Q is the heat source term. In the volumetric heating with a Gaussian laser beam case, the heat source term is expressed as:

$$Q(x,y,z) = \mathrm{Q}_0\left(1\text{-}\mathrm{R}_\mathrm{c}\right).\frac{A_c}{2\pi\sigma_x\sigma_y} e^{-\left[\frac{(x-x_0)^2}{2\sigma_x^2}+\frac{(y-y_0)^2}{2\sigma_y^2}\right]}.e^{-A_c z} \tag{3.2}$$

where Q_0, R_c, A_c, and $\sigma_{x,y}$ indicate the total input power, the reflection coefficient, the absorption coefficient, and pulse *x, y* standard deviation, respectively. Note that for the accuracy of the analysis, thermal properties of the electrodes used as absorption layer were temperature dependent thermo-physical properties. However, the material properties, R_c and A_c, are assumed to be constants. In addition, the thermal properties of multilayer MoS_2 was included in this analysis by using the experimental values of previous report.[108]

3.4 Effects of Pulsed Laser Annealing I: Flexible Multilayer MoS_2 TFTs

The effects of selective annealing of Ti/Au metal contacts in MoS_2 transistors on plastic substrates using picosecond ultra-fast pulsed laser with high-repetition rate (80 MHz) are investigated. Analyses with the numerically predicted temperature computation, current-voltage characteristics, transmission electron microscopy (TEM), and YFM are performed to prove the effects as well.

3.4.1 Device preparation

The fabrication begins with the ion-assisted deposition (IAD) of a 100-nm-thick indium thin oxide (ITO) bottom electrode on a plastic substrate at room temperature (**Figure 3.1(a)**). Subsequently, stacked gate dielectric layers are composed of an atomic-layer-deposited (ALD) aluminum oxide, Al_2O_3 film (50 nm) and a sputter-deposited SiO_2 layer (250 nm) (**Figure 3.1(b)**). Next, multilayer MoS_2 flakes are mechanically exfoliated from bulk MoS_2 crystals (SPI Supplies, USA) and transferred to the deposited SiO_2 layer (**Figure 3.1(c)**). AFM measurements show the thickness of MoS_2 channels is in the range of 30-80 nm. Here, I note that the thickness of MoS_2 was measured using an AFM (Digital Instruments-Veeco, USA). For forming the well-established contacts with MoS_2 semiconducting material, Ti was selected among the low work function materials because the favorable interface geometry of Ti allows bonding and the electronic density of states (DOS) at the Fermi level to maximize through increasing the overlap between states at the interface.[39] Strong interconnections result in narrow and low potential barriers to maximize current injection. Ti (10 nm) and Au (300 nm) layers as source and drain electrode contacts are patterned by conventional photolithography and lift-off technique and deposited by electron-beam evaporation at room temperature (**Figure 3.1(d)**).

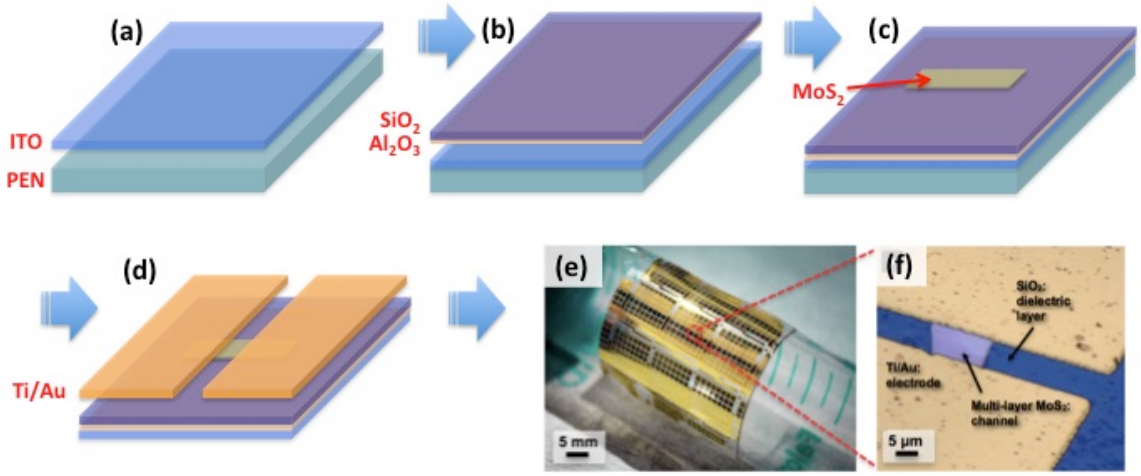

Figure 3.1 (a-d) Schematic fabrication process for bottom-gated multilayer MoS_2 TFTs on flexible PEN substrate. **(e)** Photograph of flexible multilayer MoS_2 transistors on a plastic substrate showing mechanical flexibility. **(f)** The 3D confocal laser microscope image of multilayer MoS_2 transistors with ALD Al_2O_3 / SiO_2 gate dielectric on the flexible PEN substrate.

Figure 3.1(e) shows our proof-of-concept bottom-gated MoS_2 TFTs on a flexible DuPont PEN substrate. 3D confocal laser microscope (Olympus, LEXT OLS4000) was used to obtaining 3D images of completely fabricated multilayer MoS_2 FETs in **Figure 3.1(f)**.

3.4.2 Pulsed laser annealing system

After device fabrication, the electrode contact region with MoS_2 is irradiated using a commercial neodymium-doped yttrium vanadate (Nd:YVO_4) picosecond pulsed laser from Newport (wavelength: 355 nm, pulse width based on full width at half maximum: 12 ps, pulse repetition rate: 80 MHz) and 39× objective lens with 0.5, numerical aperture. The laser beam is focused on the edge of the contacts as charge injection across contacts between bulk and thin-film materials usually occurs from the contact edge.[109] The irradiated laser with short wavelength of the laser beam (355 nm) is efficiently absorbed at Au electrode.[110] The focused laser beam has a Gaussian beam shape of 1.5 μm diameter at $1/e^2$ of peak irradiance along the propagation direction. The Gaussian laser-beam intensity within the focal plane has the form, $I(r) = I_0 \exp(-2r^2/w_e^2)$, where w_e is the radius of the laser focus defined by $I(w_e) = I_0/e^2$, $w_e = \sqrt{2}w_0$ as shown in **Figure 3.2(a)**. The target sample was placed on a high- resolution x-y positioning stage (Aerotech). The top surface of Au electrode is aligned with z = 0 and the Gaussian laser beam moves over the surface at a specific speed, 10 μm s^{-1} along a prescribed path. The pulsed laser utilizes high peak power ($P_{peak} = E / \Delta t$, where E is energy contained in every pulse is constant), which is calculated based on measured average power ($P_{avg} = E/T = Ef$, where $f = 1/T$ is repetition rate). Moreover, a computer simultaneously operated laser power, scan speed of the stage, optical shutter, and beam path during the annealing process (**Figure 3.2(b)**).

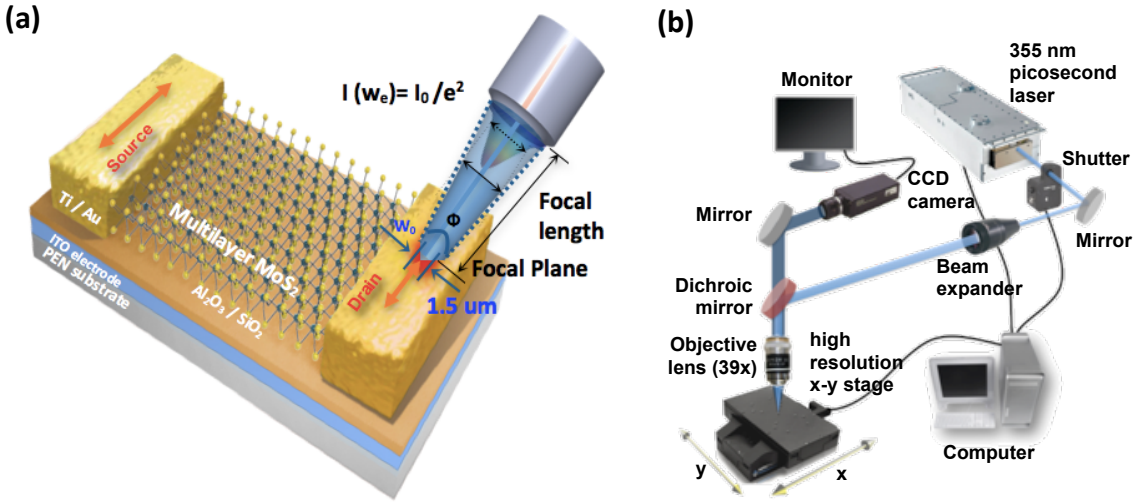

Figure 3.2 (a) Gaussian beam intensity distribution and its shape near the focal plane. $2W_0$ is the beam waist, Φ is the beam divergence angle, and 1.5 μm beam diameter based on the $1/e^2$ intensity. The picosecond laser irradiation with a Gaussian beam profile is focused and scanned along the edge of the source and drain electrodes. **(b)** The schematic view of the optical setup for picosecond laser annealing.

3.4.3 Temperature distribution

Based on the aforementioned model (see **Section 3.3** for detailed explanations), the temperature distributions at the contact and the interface during laser annealing by numerical analysis are investigated as follows.

a. Contact (between metal and semiconductor)

Figure 3.3(a) shows that the generated heat is dissipated primarily to the underlying structure by conduction with relatively minor loss to air by convection. The interested temperatures are at the top of the Au electrode labeled as "A" (at the top of Au film) and the bottom labeled as "B" (at the interface of the Au electrode and the MoS_2 channel) as shown in **Figure 3.3(a)**.

They are plotted as a function of time in **Figure 3.3(b)** (the scanning speed of laser = 10 μm s^{-1}). As picosecond laser pulses were irradiated directly at the surface of the Au electrode the temperature dramatically increased in very short time periods (~12 ps), producing sharp temperature spikes (**the inset of Figure 3.3(b)**). Because of the high repetition rate (80 MHz) of the irradiated pulses, the temperatures do not drop to the ambient temperature before the next pulse arrives.[28] This leads to heat accumulation (indicated by green regions). The elevated temperature from the heat accumulation effects was a key factor in inducing laser annealing at the location "B". Therefore, the temperature distribution consists of high frequency and picosecond-duration spikes superposed on a continuous base as shown in **the inset of Figure 3.3(b)**. I calculate the temperature distribution for average laser powers of 18.3 mW (orange region) and 43.0 mW (blue region); 18.3mW makes the best reduction of R_c (see **Figure 3.5(b)** of the next **Section 3.4.4**, in detail) and 43.0 mW is the initial power of damage based on real experimental results (**Figure 3.3(c)**).

The effect of the high frequency transients by an ultra-short pulsed laser lasted till the time of 0.2 s. (while location "A" is directly irradiated by the moving Gaussian laser beam). At the moment when the center of laser beam was placed right on the middle of "A" (0.075 s), the temperature exhibited significant variation, depending on the laser power. For the laser power of 43.0 mW, the temperature exceeded the melting point of Au (1330 K) as indicated by the orange region in **Figure 3.3(b)**. Such a high temperature may inflict thermal damage on the Au contacts. However, the induced temperature by the laser power of 18.3 mW is 533 K (blue region in **Figure 3.3(b)**). This is a comparable temperature with those of thermal annealing used in previous studies to improve device performance,[37,43,111] as well as with our experimental results detailed in subsequent sections of this paper. At this time, the Au film endured substantial temperature difference between its top and bottom surfaces, implying that the Au film helped protect the bottom of the film surface from strong sharp and high intensity irradiance. Since the position "A" was completely outside the pulsed laser beam beyond 0.2 s, the effect of these high peaks faded due to diffusion. Therefore, the top and bottom temperatures converge and cool down completely (~ 2.6 s) as shown in **Figure 3.3(b)**.

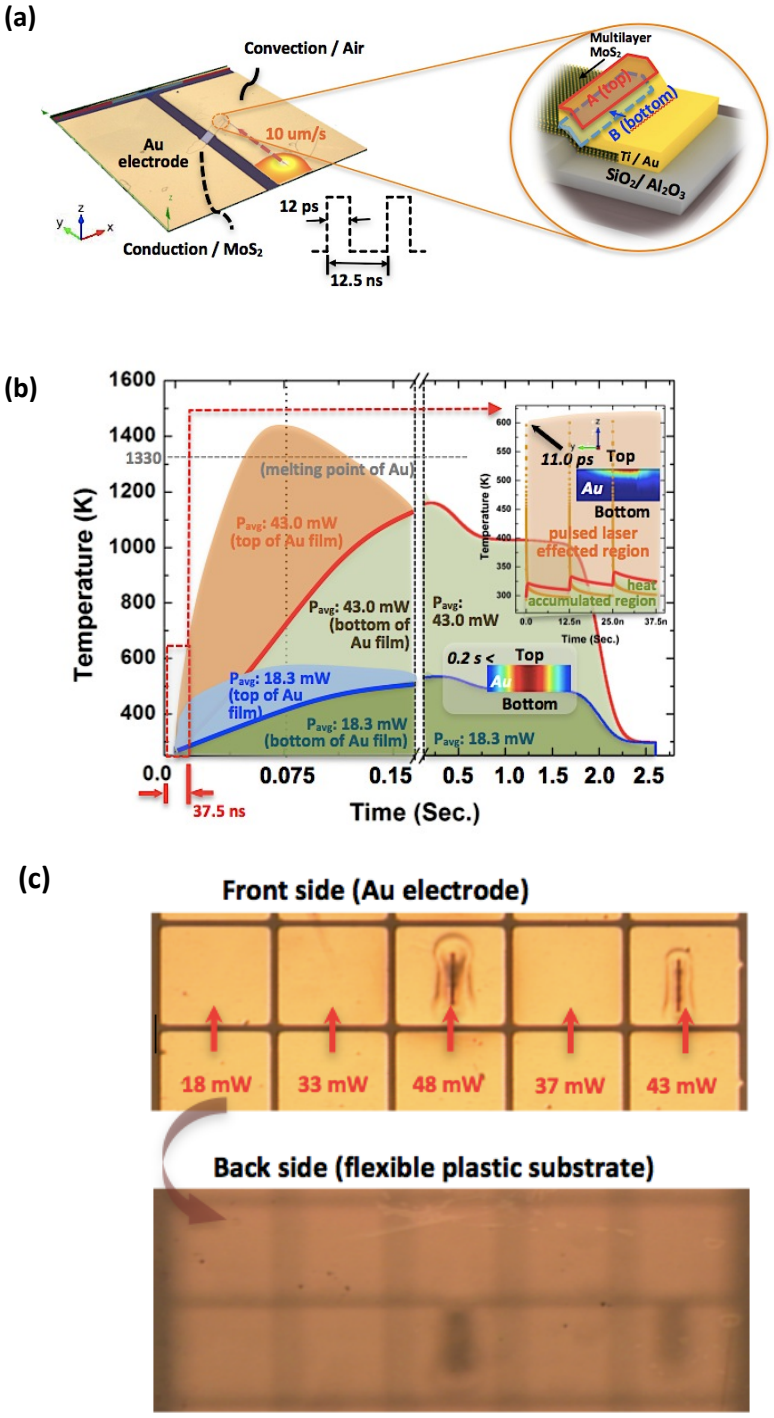

Figure 3.3 Numerical results calculated by finite-difference methods (FDM) for the temperature distribution under picosecond-pulsed laser source. **(a)** The spatial temperature distribution along the surface when picosecond pulsed laser is applied onto the Au electrode surface in contact with air and ALD Al_2O_3 / SiO_2 dielectric layer. **(b)** The temperature of Au electrode versus exposure time at the specific points "A" (the top of Au film) and "B" (the interface of the Au electrode and the MoS_2 channel) in (a) irradiated by the center of the laser beam. The 37.5 ns window (not on scale in the horizontal time axis) is depicted in the insert. **(c)** The optical images of the front and backside of laser-irradiated Au contacts on a flexible plastic substrate. Au contacts irradiated with laser power > 40 mW show severe damage.

The valid range of laser power that allows laser processing to be compatible with plastic substrates can be tested by irradiating laser beams on the Au contacts. **Figure 3.3(c)** shows the optical images of laser-irradiated Au contacts on plastic substrate. In agreement with the numerical analysis, the laser with its power > 40 mW severely damages the Au electrode.

b. Interface (between semiconductor and dielectric layer)

The electrical performance of fabricated MoS_2 TFTs is mostly decided by the quality of the MoS_2 film and the interface. Since the non-ideal interface can generate several types of traps impeding the flow of electrons, therefore, we should consider not only semiconductor but also interface as well.

Generated heat by laser absorption at the top surface could affect the interfaces by heat conduction as well as the contact. Therefore, thermal analysis is needed to expand into the interfaces. Note that interested interfaces are between channel and dielectric layer (point 2) and between dielectric and substrate layer (point 3) in **Figure 3.4(a)**. In the previous **Section 3.4.3.a**, point 1 (contacts, the first focused area) is already analyzed and the generated temperature was around 533 K, which is high enough for effective laser annealing.[102] As shown in **Figure 3.4(b)**, at point 2, the reached heat around 480 K (~210 °C) is not low to ignore because the temperature has enough to make thermal anneal effect, according to other reports.[37,43] Unfortunately, I cannot obtain the result measured directly to confirm the effect on the interfaces. However, I've tried to verify the impact on the interfaces indirectly through the new approach, YFM (see the **Section 3.4.7**). Point 3 shows that the reached heat, 365 K (~90 °C) can be below the thermal resistance of PEN substrate (~170 °C). Therefore, we can know and expect that there is no thermal damage after laser process; I already proved it through the laser experiment (**Figure 3.3(c)**).

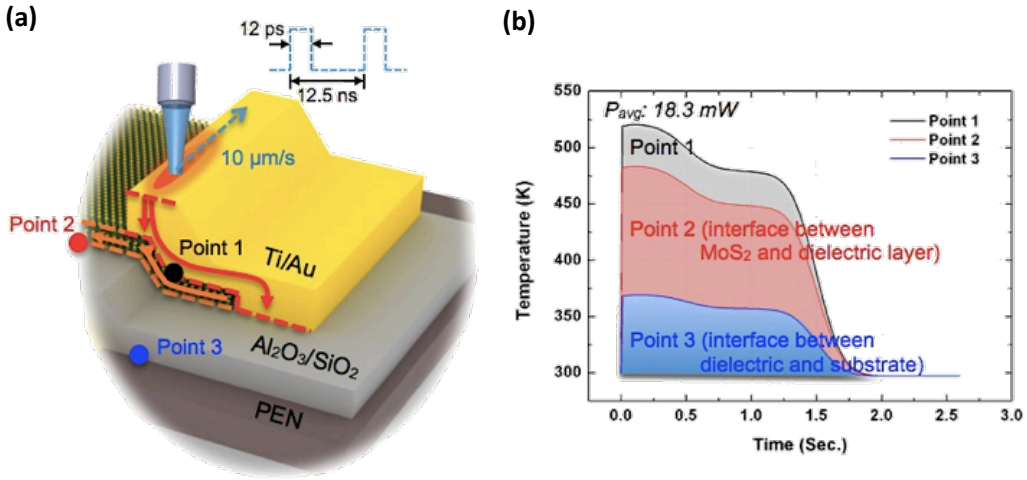

Figure 3.4 (a) Spatial schematic images of laser irradiated Au contacts at a speed of 10 μm/s on a flexible PEN substrate and three points of interest: point 1 (the interface between the contact and MoS_2), point 2 (the interface between MoS_2 and the dielectric layer), and point 3 (the interface between the dielectric layer and the substrate). **(b)** Numerical thermal analysis of temperature distribution versus exposure time at the three specific points when a picosecond pulsed laser was applied and scanned onto the top surface (Au) at ambient conditions.

3.4.4 Current-voltage measurement (2-terminal): contact resistance

To investigate the effect of laser annealing on the R_c of MoS_2 transistors, the MoS_2 TFTs on SiO_2 (250 nm)/p^+-Si wafers are used as test vehicles and measure the I_D-V_D characteristics at the floating gate voltage before and after laser annealing. To see the effect of laser power on the R_c, the changes in normalized R_c (R_CW; W: width of the contact) after laser annealing are calculated based on the model shown in **Figure 3.5(a)**. The total resistance (R) between source and drain of the MoS_2 transistor is given by:[112]

$$R = R_S \frac{d}{W} + 2R_C, \tag{3.3}$$

where R_S is MoS_2 sheet resistance and d is the distance between contacts. The contact resistance R_C is given by:[112]

$$R_C = \frac{\rho_C}{WL_T} \coth(\frac{L}{L_T}), \tag{3.4}$$

where ρ_C is the interface resistivity, L is the length of contact, and L_T is transfer length ($L_T = (\rho_C/R_S)^{1/2}$). If we assume $L > 1.5L_T$, **Equation (3.4)** becomes:[112]

$$R_C \approx \frac{\rho_C}{WL_T}. \tag{3.5}$$

If the change in R_S is negligible after laser annealing, the change in resistance is given by:

$$\Delta R = R_{After} - R_{Before} = 2\Delta R_C. \tag{3.6}$$

From **Equation (3.5)**,

$$\Delta R_C = \frac{1}{W} \Delta(\frac{\rho_C}{L_T}). \tag{3.7}$$

Then, **Equation (3.6)** becomes:

$$\Delta R = \frac{2}{W} \Delta(\frac{\rho_C}{L_T}) \tag{3.8}$$

Rearranging **Equation (3.8)** gives:

$$\Delta(\frac{\rho_C}{L_T}) = \frac{W}{2} \Delta R \tag{3.9}$$

From **Equation (3.7)**, **Equation (3.9)** is equal to ΔR_CW, the changes in normalized R_C after laser annealing. Then, ΔR_CW can be calculated, based on the estimated parameters.

Among five different laser powers between 5 mW and 40 mW, the normalized $\Delta R_C W$ in **Figure 3.5(b)** shows that 18.3 mW provides the greatest reduction in $R_C W$. If the laser power is too low, the laser irradiation does not increase the temperature enough to affect the contact behavior. On the other hand, if the laser power is too high, the annealing temperature becomes so high that it possibly starts the deterioration of the contact behavior. It needs to be mentioned that the $R_C W$ values of MoS_2-metal contacts reported in literature scatter in the range of 3.3-80 Ω·mm.[43,60,113,114] Although I could not obtain an absolute value of $R_C W$ within the given experimental conditions, a consistent reduction of R_c in various MoS_2 transistors after laser annealing at 18.3 mW demonstrates the robustness and reproducibility of the this method. I will discuss this issue further through YFM (see the **Section 3.4.7**).

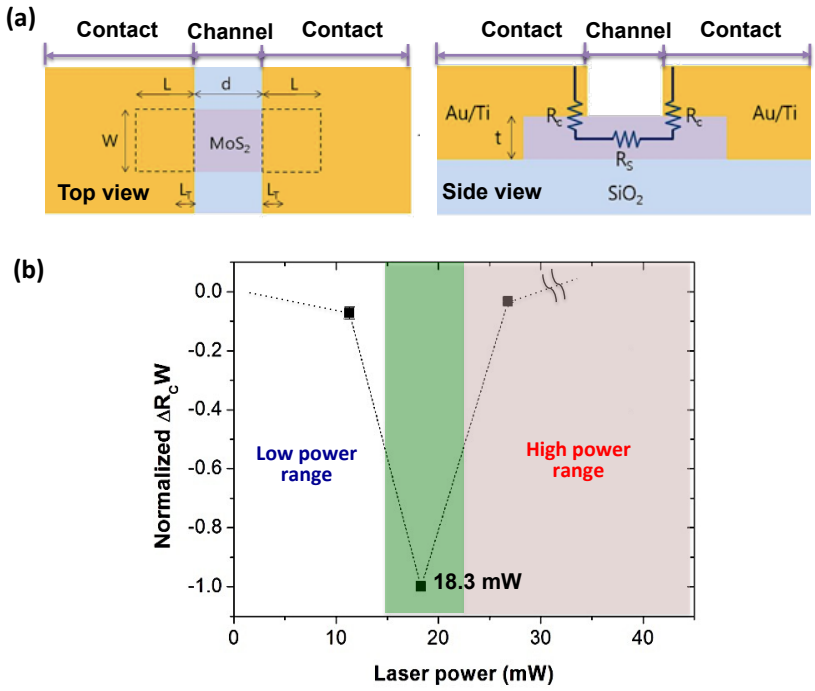

Figure 3.5 Effects of laser annealing on the R_c of multilayer MoS_2 transistors fabricated on Si wafers. **(a)** Schematic device configuration with an equivalent circuit model. **(b)** The reduction of R_c per width after laser annealing normalized with respect to that of 18.8 mW ($\Delta R_c W = (R_c W)_{After} - (R_c W)_{Before}$). V_{ds} = 1 V and scan speed = 10 μm s^{-1}.

3.4.5 Electrical performance

The effects of laser annealing on device performance of MoS_2 TFTs on flexible PEN substrates are investigated. The thickness of the MoS_2 flake of our representative device (t_{ch}) is ~50 nm, and the back gate oxide thickness (t_{ox}) is ~300 nm (SiO_2 (250 nm) and Al_2O_3 (50 nm)). **Figure 3.6(a)** and **3.6(b)** show the log- and linear-scale I_D-V_G characteristics for the same MoS_2 TFTs, measured before (black circles) and after laser annealing (red circles) with a power of 18.3 mW). Following selective laser annealing on contacts in MoS_2 TFTs, transistor performance metrics, including I_{on}/I_{off}, $\mu_{eff} = Lg_m/(WC_{ox}V_{ds})$, SS, output resistance

(R_o), and voltage-gain for transistor (A_v), were improved. The I_{on}/I_{off} after laser annealing was observed as > 10^6 without a change in I_{off}. μ_{eff} extracted from **Figure 3.6(b)** increased almost two-fold after laser annealing (from 24.84 cm^2 $V^{-1}s^{-1}$ to 44.84 cm^2 $V^{-1}s^{-1}$). Here, L, g_m, W, C_{ox} are channel length (L = 7 μm), transconductance, channel width (W = 7.75 μm), and oxide capacitance, respectively. The value of μ_{eff} observed in our MoS_2 TFTs exceeds those reported in previous MoS_2 TFTs on flexible substrates (4.7-24 cm^2 $V^{-1}s^{-1}$) as well as in organic TFTs or a-Si TFTs on flexible plastic substrates (< 1 cm^2 $V^{-1}s^{-1}$).[114-116] Statistically, μ_{eff} of the tested MoS_2 TFTs increased from ~15±10 cm^2 $V^{-1}s^{-1}$ to ~35±10 cm^2 $V^{-1}s^{-1}$ after laser annealing. No dependence on channel thickness was observed within the given experimental conditions. **Figure 3.6(c)** shows I_D-V_D with magnification for the low V_D range (from 0 V to 0.4 V) before (open circles) and after laser annealing (solid circles). At the same V_G-V_{TH}, the laser annealing results in Ohmic behavior in linear regime and higher current saturation. Following laser annealing, R_o significantly increased to 0.42 MΩ at V_G-V_{TH}= 20 V, which is three times higher than values for as-fabricated devices.

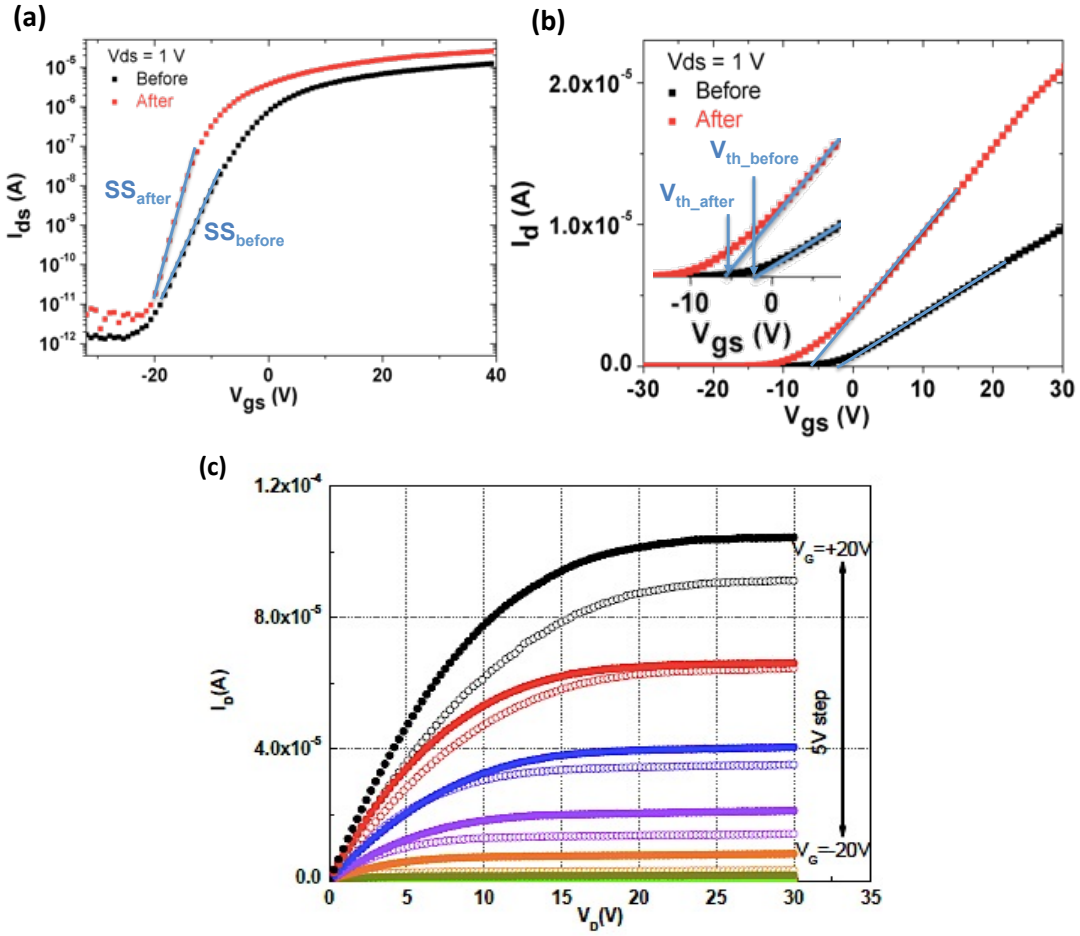

Figure 3.6 The enhanced performance of a representative flexible MoS_2 transistor by the selective laser annealing of contacts. **(a)** The log-scale I_D-V_G characteristics for a MoS_2 transistor (L = 7 μm) before and after laser annealing at V_D = 1 V. **(b)** the I_D-V_G in linear-scale. **(c)** The I_D-V_G characteristics of the MoS_2 transistor before (open circle) and after (solid circle) laser annealing. V_G ranges from -10 to 15 V in 5 V steps.

The most prominent effect of laser annealing is the self-gain ($A_v = g_m R_o$) in MoS_2 TFTs, which exhibits six-fold increase due to enhancement of g_m and R_o. For supporting the results and further investigation, I will examine the effect of the laser annealing through the cross-sectional TEM image (see **Section 3.4.6**) and YFM (see **Section 3.4.7**) in the next section.

3.4.6 TEM analysis at the contacts: Schottky barrier

Figure 3.7(a) shows the schematic energy band diagram for the MoS_2 transistor with Ti/Au metal electrodes in the isolating system. When the metal and semiconductor contact each other, Φ_B between metal contacts and a semiconductor is formed (**Figure 3.7(b)**, in thermal equilibrium of which I_D-V_D (at V_G = 0 V) characteristics). And the existence of Φ_B, thermionic emission and/or tunneling will allow electron transport during transistor operation. According to Das *et al*., thermionic emission and tunneling though Schottky barrier limit the charge injection during off- and on-state of MoS_2 transistors, respectively.[64] The dominant mechanism that reduced R_c in **Figure 3.5** is not clear as the gate was floated during the measurement of source-drain current. However, the significant increase of the on-current after laser annealing in **Figure 3.6** suggests that laser annealing increases the tunneling current across the Φ_B. Since the tunneling current will exponentially increase with $N_D^{0.5}$, where N_D is carrier concentration,[117] the decreased R_c after laser annealing is probably due to the reduced tunneling barrier width (**Figure 3.7(c)**), which could be resulted from the increased carrier concentration at the interface.

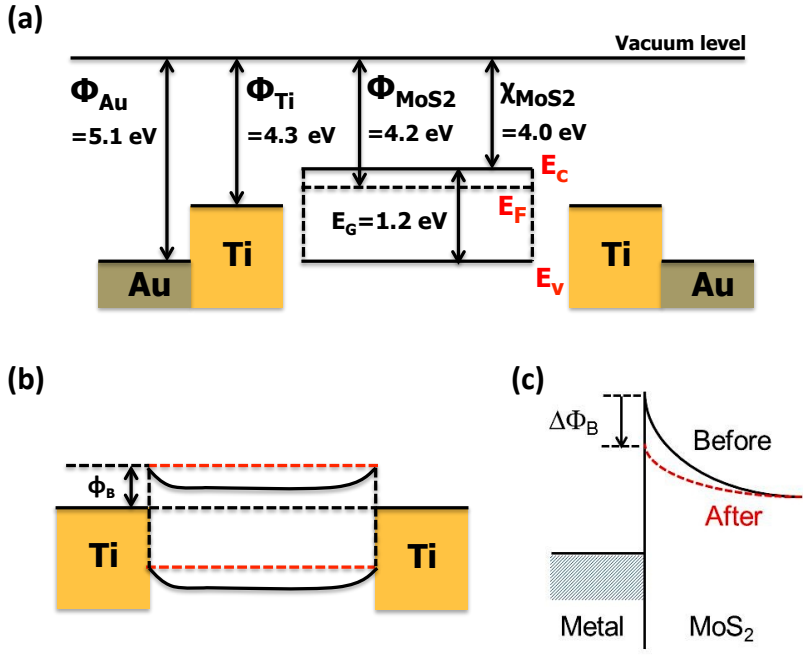

Figure 3.7 (a) Schematic energy-band diagrams of multilayer MoS_2 transistors with a Schottky barrier at the isolation and **(b)** at equilibrium. Note that Φ is work function of metal; Φ_B is Schottky barrier; χ is electron affinity. **(c)** Schematic band diagram of the metal-MoS_2 junction illustrating the reduction of the Schottky barrier width after laser annealing.

This explanation is supported by the cross-sectional TEM image shown in **Figure 3.8**. Through the TEM images before and after, there are several possible explanations for reducing the R_c and enhancing electrical performances. The first possibility is removing unintentional interfacial layers, which make interface trap. That means that increasing contact adhesion then, reducing the resistance of the interface. The second possible explanation is a mixture layer. It is not clear which mechanism makes a mixture layer, however, the mixture layer is conspicuously formed after laser annealing process. This observation is consistent with the reports that Ti forms a mixture layer with MoS_2 by placing Ti atoms between the neighboring S planes of MoS_2 and that thermal annealing at 300 °C induces solid-state diffusion in Ti thin film.[118,119] As Ti-doped MoS_2 becomes more conductive due to increased *n*-type doping,[120] the reduction of tunneling barrier width by the formation of a Ti-MoS_2 mixture layer at the interface is thought to be the dominant mechanism of the decreased R_c after laser annealing.

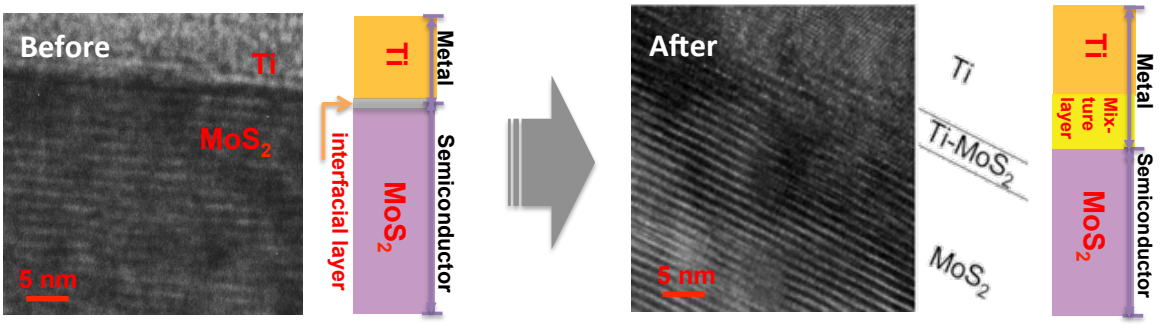

Figure 3.8 Cross-sectional TEM images showing the mixture layer at the interface after laser annealing.

3.4.7 Y-function method: intrinsic mobility

For evaluation of the mobility, presently μ_{eff} is widely used, but it includes a variety of additional effects existing in transistors, especially for effect of R_c. Here, note that μ_{eff} differs from the intrinsic mobility without contact factor. Therefore, the contact factor and effect should be separated from the intrinsic characteristics of the TFTs. To extract it, transfer-line method (TLM) is commonly employed among several methods: gated four-probe measurement and Kelvin probe force microscopy (KFM).[121-125] However, TLM requires several sets of transistors with various channel length. Therefore, I apply for YFM that can provide to be a simple and powerful method to evaluate the low-field mobility, intrinsic mobility (μ_0) without R_c influence.[66]

Figure 3.9(a) shows the schematic architecture of our flexible multilayer MoS_2 TFTs on the PEN substrate (DuPont Teijin Films, USA) as a test sample for the YFM. And a proof-of-concept demonstration of a completely fabricated flexible multilayer MoS_2 FET rolled up in a curved shape and an optical microscope image from the top of the device (**Figure 3.9(b)**). Here, I note that fabrication processes and laser annealing method are the same with previous **Section 3.4.1** and **3.4.2**.

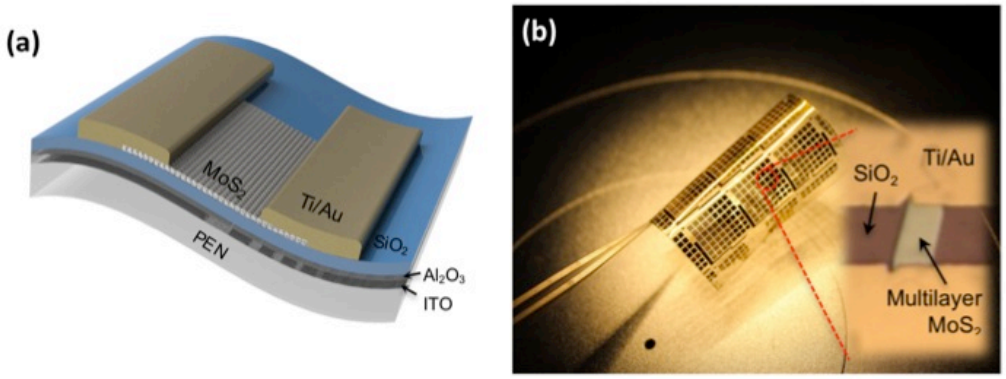

Figure 3.9 (a) Cross-sectional schematic structure of multilayer MoS_2 FETs with a 300-nm-thick SiO_2 gate dielectric. Picosecond laser irradiation with a Gaussian beam profile is focused and scanned along the edge of the source and drain electrodes. **(b)** Top-view of the optical microscope image for multilayer MoS_2 FETs after fabricating completely.

At room temperature and in air, the as-fabricated MoS_2 TFT (before laser treatment) exhibited acceptable switching behavior (I_{on}/I_{off} of ~ 1.99×10^7), a SS of ~ 4.05 V/decade, μ_{eff_lin} of ~ 19.59 $cm^2V^{-1}s^{-1}$, and typical *n*-type behavior with negative V_{TH}, and a normally ON-state for the device. Following laser annealing, electrical performances were enhanced including output characteristics of: increased I_{on}/I_{off} of ~ 2.70×10^8 without a change in I_{off}, reduced SS of ~ 3.06 V/decade, an improved μ_{eff_lin} of ~ 45.91 $cm^2V^{-1}s^{-1}$ (over twice), and strong saturation at I_D-V_D (**Figure 3.10(a)** and **3.10(b)**) These results are in agreement with the previous experiments (**Section 3.4.5**).

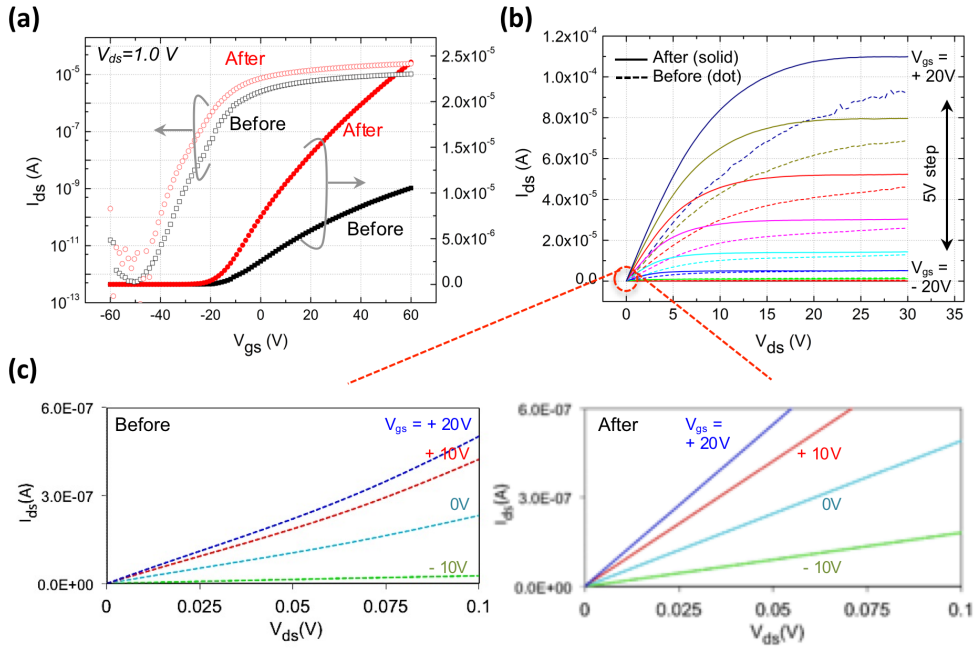

Figure 3.10 (a) Transfer characteristics (I_D-V_G) for the flexible MoS_2 transistor in log-scale (left) and linear-scale (right) before and after laser annealing at V_D = 1 V. **(b)** Output characteristics (I_D-V_D) before (dot) and after (solid) laser process. **(c)** Magnifications (before and after) for the low V_D range from 0 to 0.1 V.

Furthermore, as shown in **Figure 3.10(c)**, I observed a non-linear output curve in a very low V_D regime (from 0 to 0.1 V) due to the Φ_B between the MoS_2 and Ti/Au electrodes before the laser process. However, after laser annealing, the curve exhibited linear characteristics, indicating a Schottky to Ohmic contact transition. This can allow increased electrical conductivity of the interface through the reduction of R_c by reducing the barrier effect. To confirm the results, I will examine the effect of the laser annealing through the YFM.

The YFM is based on the I_D-V_G relation in the linear region, as below:

$$I_D = g_{ds} \times V_D = \frac{W}{L} Q_{ch} \mu_{eff} \times V_D \tag{3.10}$$

where g_{ds} is the channel conductance, μ_{eff} is the effective mobility, and Q_{ch} is the channel charge per unit area. Then, we consider the θ ($=\theta_0+\theta^*$), including the contribution from the channel interface (θ_0) and the R_c ($\theta^*=\mu_0 C_{ox} R_c W/L$). Therefore, the I_D can be written as,

$$I_D = \frac{W}{L} C_{ox} (V_G - V_{TH}) \frac{\mu_0}{1+\theta(V_G - V_{TH})} \times V_D \tag{3.11}$$

Considering the definition of the transconductance ($g_m = \partial I_D / \partial V_G, V_D = const.$) and μ_{eff} ($= Lg_m/(WC_{ox}V_D)$), the Y function can be defined as

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_D} \times (V_G - V_{TH}) \tag{3.12}$$

in order to eliminate θ. Note that **Equation (3.12)** is independent of R_c, which is assumed to be constant. It can be seen from **Equation (3.12)** that μ_0 could be extracted from the slope of the Y function, as shown in **Figure 3.11(a)**. Using slopes obtained before (5.9×10^{-4}) and after (6.6×10^{-4}) laser annealing, the values of μ_0 are extracted. **Figure 3.11(b)** shows the comparison of the μ_0 and the peak μ_{eff} at the same V_D, +1.0 V. Before the laser process, a large discrepancy (48.18%) exists between μ_0 (37.80 $cm^2 V^{-1}s^{-1}$) and μ_{eff_lin} (19.59 $cm^2 V^{-1}s^{-1}$). However, after laser annealing, the discrepancy (2.95%) is greatly reduced: μ_0 (47.31 $cm^2 V^{-1}s^{-1}$) and μ_{eff_lin} (45.91 $cm^2 V^{-1}s^{-1}$). To further investigate the laser effects, we extracted the values of θ, and estimated R_c by the following equations:

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=const} = \frac{W}{L} C_{ox} \frac{\mu_0}{[1+\theta(V_G - V_{TH})]^2} \times V_D \tag{3.13}$$

For obtaining θ, **Equation (3.13)** can be rewritten as,

$$\frac{1}{\sqrt{g_m}} = \sqrt{\frac{1}{G_m V_D}} \{\theta(V_G - V_{TH}) + 1\} \tag{3.14}$$

where $G_m = (W/L)\mu_0 C_{ox}$ is the transconductance with the μ_0. From **Equation (3.14)**, the values of θ for as-fabricated (1.0×10^{-2}) and after laser annealing (6.3×10^{-3}) can be obtained by the linear fitted slopes (before: ~ 17 and after: ~ 9.6) of the $1/g_m^{0.5}$-V_G curve, as shown in **Figure**

3.11(c). Through the known values of θ, the upper bound of R_c (R_{c_max}) can be calculated when I assume that the influence of θ_0 is negligible. Therefore, the contact effect mainly contributes to θ, and extracted values of R_{c_max} are 28.9 kΩ and 14.6 kΩ, respectively, before and after the laser process.

Furthermore, μ_0 is slightly increased (20.10%) before and after the laser treatment. Since μ_0 is not affected by the contact factor, one of the possible reasons for this could be that the quality of the interface is enhanced. The traps between semiconductors and insulators play a critical role in determining the device performance, and the reduced interface trap concentrations were confirmed by the deceased SS values. To reconfirm the results, I roughly estimated the values of channel resistance (R_{ch}) by using the relation $R_{ch}=L/(\mu_0 WC_{ox}(V_G-V_{TH}))$ before and after laser annealing. The obtained values of R_{ch} were 85.34 kΩ (before) and 61.18 kΩ (after), respectively. The results of decreasing R_{ch} by the laser process support and agree well with the enhanced interface conditions I described above.

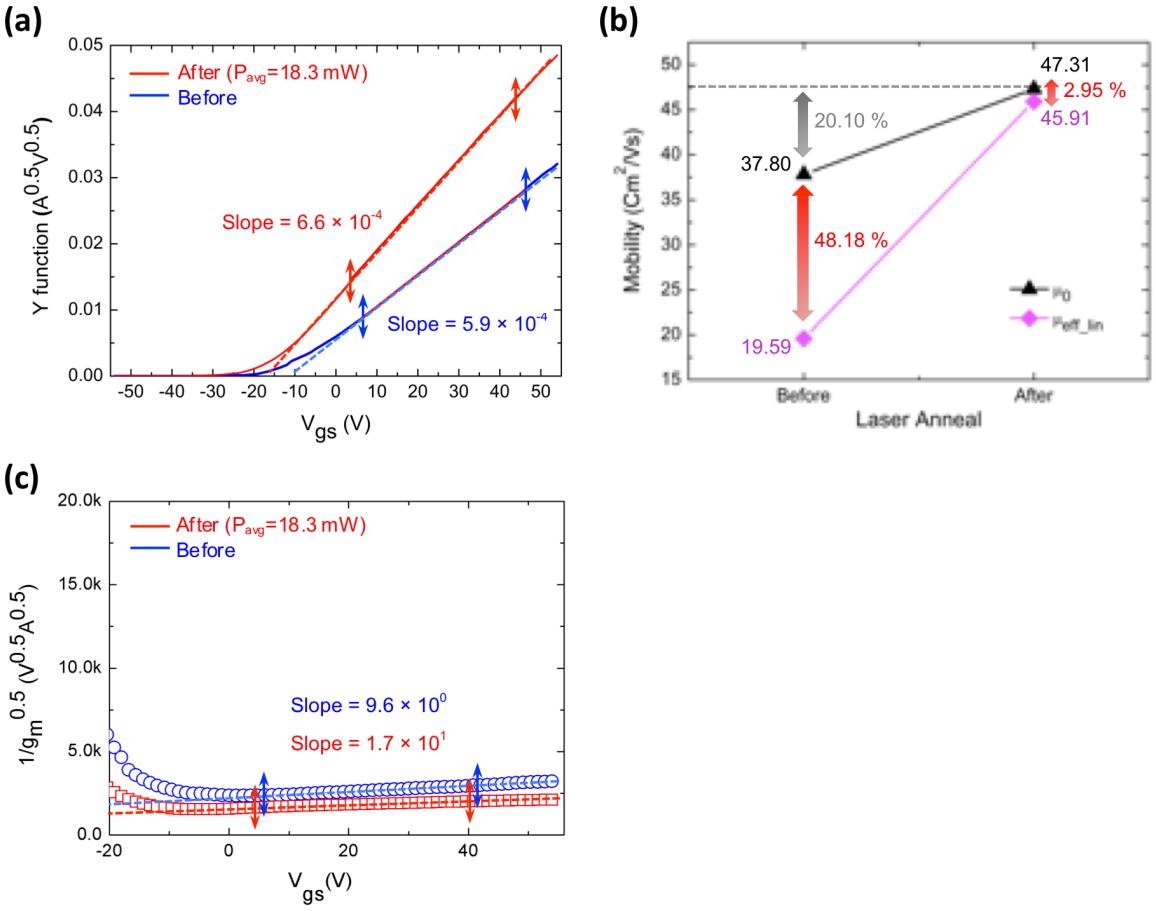

Figure 3.11 Y-function and evaluation of electrical parameters before and after the laser process. **(a)** Plots of Y-function with respect to V_G and the linear fitting in the strong accumulation region for obtaining the slope. **(b)** Comparison of the μ_0 and μ_{eff_lin} before and after the laser process. **(c)** Plots of $1/g_m^{0.5}$ with respect to the V_G and their slopes in the straight line fitting for extraction of the mobility attenuation factor (θ).

Also, through the comparison with R_{c_max} and R_{ch}, I have evidence that the diminishing discrepancy between the μ_{eff_lin} and μ_0 originates from the reduced contact and channel resistance by the laser annealing process. This indicates that the laser annealing process employed is the critical factor involved in enhancing the TFT performance by improving the contact conditions and promoting the interface quality without thermal damage to plastic substrates.

3.5 Effects of Pulsed Laser Annealing II: Transparent Multilayer MoS_2 TFTs

The growing desire for a next-generation display has given rise to persistent attempts and efforts to demonstrate optically transparent TFTs. For a transparent display, a fully transparent thin-film transistor will play an essential role to achieve high transmittance because the TFT backplane in the display has been one of the major factors of reduction in transmittance. In this regard, various new classes of nano-materials, such as single-walled CNT or oxide NWs, with transparent electrodes have been proposed to achieve ultra-high optical transparency and superior electrical performance due to these one-dimensional semi- conductors of molecular thickness.[126-131] Despite the significant progress, a critical weakness remains and must be further improved in their commercial integrated circuit. The challenges to reach a commercial display require a novel nano-semiconductor to achieve optical transparency, high-mobility and amenability to a large-area growth technique.

Therefore, in this section, transparent multilayer MoS_2 TFTs with ITO for the back-gated electrode and indium zinc oxide (IZO) for the source/drain electrodes are explored. Also, In order to realize the high performance of the transparent MoS_2 transistor, selective laser annealing enables the achievement of superb interfacial characteristics between the IZO electrode and MoS_2 material contact surface and is also useful for a reduction in R_c.

3.5.1 Device preparation

Figure 3.12(a) presents a 3D schematic illustration of the transparent multilayer MoS_2 TFT with a back-gated structure in a cross-sectional view. The ITO glass with a ITO thickness of 200 nm and a sheet resistance of 10–15 Ω sq^{-1}, respectively, was used as the back-gated electrode of the TFTs. A 300 nm thick SiO_2 as the gate dielectric was deposited on the ITO glass by plasma-enhanced chemical vapor deposition (Low Stress PECVD, SLP-730 by Unaxis) at 350 °C. Mechanically exfoliated multilayer MoS_2 from bulk MoS_2 (SPI supplies, USA) is transferred on the SiO_2 layer. Then, the IZO layer with a thickness of 100 nm as the source/drain electrodes was deposited by sputtering. The IZO source/drain electrodes with various channel lengths were fabricated using conventional photolithography and the etching method.

Figure 3.12(b) shows the transmission spectra (Agilent 8453 UV–vis Spectrophotometer) of transparent MoS_2 TFTs on the glass substrate and on the ITO glass in the 300–900 nm

wavelength range. The $1\times1cm^2$ area contains 2240 transistor patterns, and about 92% of the area is covered with IZO electrodes. It should be noted that multilayer MoS_2 flakes were randomly distributed in our device configuration. However, the active layer of each TFT in the driving circuitry (for example, six transistors and two capacitors) occupies very limited space in the whole display panel. Also, the overall transmittance of the patterned active layer (e.g. discontinuous layer structure) would be correlated with the summation of each active area. In addition, the reduction of transmittance due to the signal line between the TFT circuit and light-emitting component also plays the important role of estimating the optical transparency of the display panel. Therefore, the device configuration could evaluate the potential optical transparency of transparent TFT arrays, which have a similar area of the total active layer. The averaged transmittances of our transparent MoS_2 TFTs and ITO glass were ~81% and ~87%, respectively, in the visible wavelength range. The transmittance of MoS_2 TFTs was almost comparable to that of ITO glass in the wavelength range of 450–650 nm, which was most sensitive to response of the human eye.

An optical microscope image (Olympus BX51M) of the transparent MoS_2 TFTs on printed texts is presented in **Figure 3.12(c)**. I can clearly identify the texts through the MoS_2 TFTs as well as through the colored IZO electrodes. Also, **Figure 3.12(c)** shows a single TFT that consists of a multilayered MoS_2 flake between the IZO source/drain electrodes.

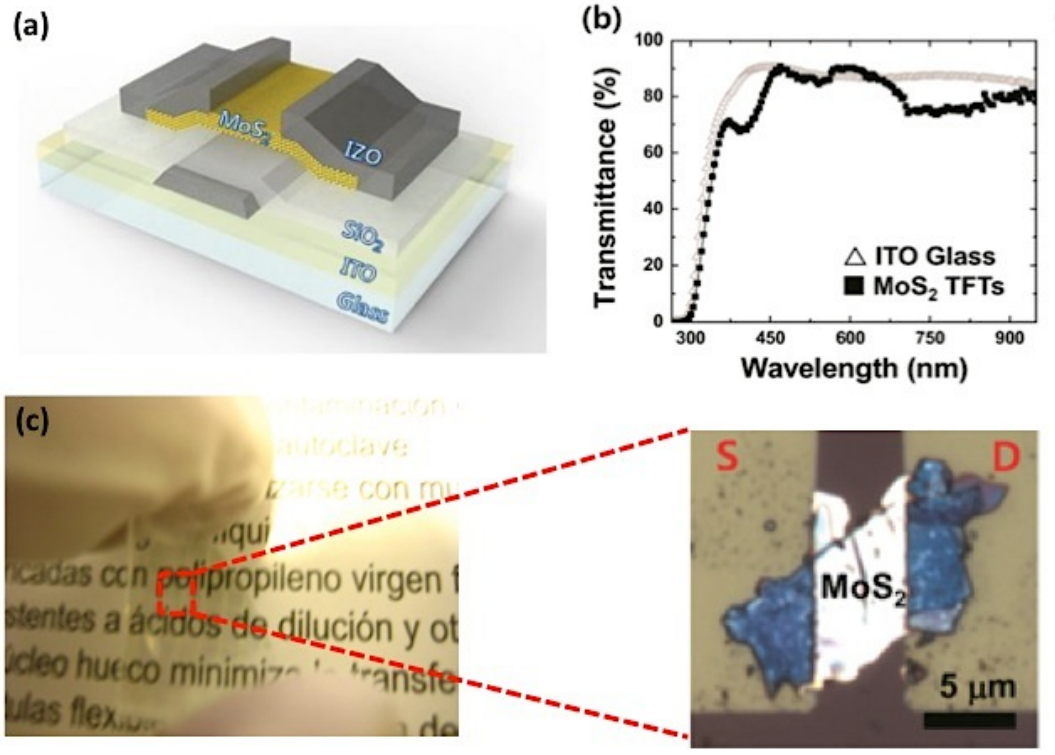

Figure 3.12 (a) 3D cross-sectional schematic view of the transparent multilayered MoS_2 TFT. The dashed red line indicates atomic arrangements and a layered structure in multilayer MoS_2. **(b)** Transmission spectra of the ITO glass (Δ) and the transparent MoS_2 TFTs (■) in the visible wavelength range. **(c)** Optical microscope image of the transparent MoS_2 TFTs on the printed texts and magnified optical microscope image of a single TFT consisting of a MoS_2 flake between the IZO source and drain electrodes.

3.5.2 Results and discussion

During the laser annealing process, the short wavelength (355nm) helps the transparent electrode efficiently absorb more energy from the incident light of the laser. The 100 nm thickness of IZO showed 30–36% transmittance at 355 nm;[132] 64–70% of the laser energy would be absorbed in the IZO electrodes, and the rest of the energy might reach, and be absorbed in, the MoS_2 layer. The details of the experimental conditions were reported earlier (**Section 3.4.2**).

The I_D–V_D characteristic curves of the transparent MoS_2 TFT as two-terminal devices (gate was grounded, i.e. at $V_G = 0$ V) before and after laser annealing are compared in **Figure 3.13**. The I_D–V_D characteristic curves of the pristine (before laser annealing) transparent MoS_2 TFT showed typical *n*-type diode-like behavior, and the current level of the device was dramatically increased after laser annealing treatment. In order to investigate the change of the charge transport due to the laser annealing, the I_D–V_D characteristic curves of the transparent MoS_2 TFT ($V_G = 0$ V) were re-plotted using the logarithmic scale, as shown in the inset of **Figure 3.13**. For pristine transparent MoS_2 TFT, two distinct regimes, depending on the slopes of the I_D at $V_G = 0$ V, were observed. In a low-biased region, the I_D increased linearly ($I \propto V$), indicating the Ohmic conduction due to the thermionic emission. However, the I_D increased quadratically ($I \propto V^2$) in the high-biased region, which could be explained through the space charge limited current model.[133] I reported on the decrease of the Schottky barrier width in the picosecond laser annealed MoS_2 TFT with Ti/Au electrodes, which resulted in the reduction of the R_c between MoS_2 and the metal electrodes.[102] The enhancement of the current level and the change of the slopes in the log-log plot of the I_D–V_D characteristic curves suggested that charge carriers would be more effectively injected from the IZO electrode to the MoS_2 active layer due to the laser annealing process, which well agreed with the previous reports.[102,133]

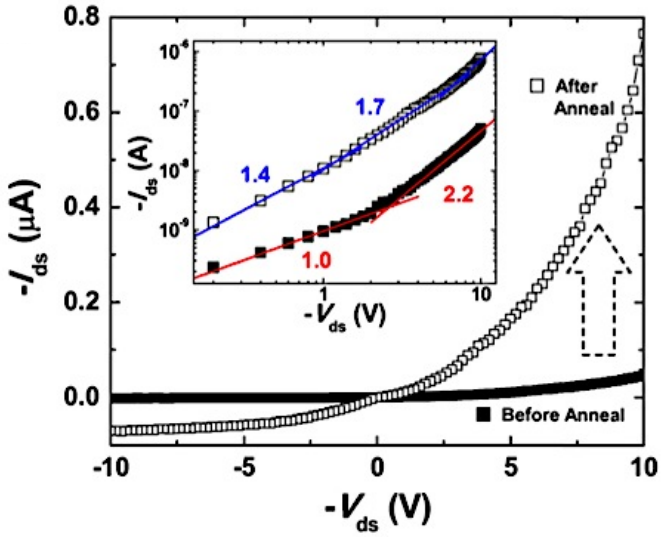

Figure 3.13 Comparison of the I_D–V_D characteristic curves of transparent MoS_2 TFT at $V_G = 0$ V before (■) and after (□) laser annealing. Inset: I_D–V_D characteristic curves of transparent MoS_2 TFT ($V_G = 0$ V) using the logarithmic scale.

Figure 3.14(a) and **3.14(b)** show the comparison of transfer and output characteristic curves of the transparent MoS_2 TFT with respect to the laser annealing process. It is noted that the electrical characteristics were measured in the same MoS_2 TFT for investigating the effects of the laser annealing treatment. As shown in **Figure 3.14(a)**, the μ_{eff} ($=Lg_m/WC_{ox}V_D$) of as-fabricated MoS_2 TFT was calculated as 1.4 cm^2 V^{-1} s^{-1} in the linear region (V_D = 1 V). It has been known that there exists a large Φ_B (~0.7 eV) between IZO and MoS_2 due to high work function of IZO (~5 eV), which can severely restrict electron transport at source/drain contacts. Recently, Hinkle and co-workers reported that electronic properties of multilayered MoS_2 could be significantly varied with spatial point even within same sample.[134] Depending on the stoichiometric variation of sulfur to molybdenum ratio, the intrinsic defects of the natural MoS_2 could be categorized into S-rich (S : Mo = 2.3 : 1) and S-deficient (1.8 : 1) species, which would result in *p*-type and *n*-type characteristics, respectively.[134,135] The S-deficient defects were estimated to metallic-like properties with relatively low effective work function, which leaded to the inhomogeneous interface between IZO and MoS_2. Though relative low density of 0.1–5%, lowering of the Schottky barrier height due to the S-deficient defects could be attributed by considering a parallel conduction model.[134] The *n*-type behaviors of the electrical properties, observed in **Figure 3.13** and **3.14**, indicated that S-deficient defects would be dominant in MoS_2 active layer in our transparent TFT. Das *et al*., reported that the Fermi levels of metals with high work functions, such as nickel (Ni, 5.0 eV) and platinum (Pt, 5.9 eV), were also pinned in the conduction band edge of MoS_2.[64] So, the *n*-type behavior of transparent MoS_2 TFTs could also be attributed to the Fermi level pinning between MoS_2 and IZO.[64]

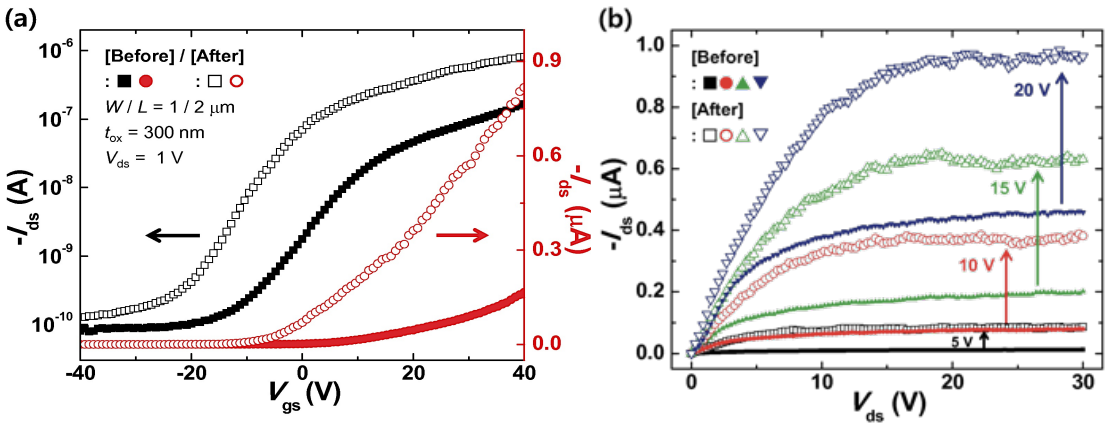

Figure 3.14 (a) Transfer characteristic (V_G–I_D) of the transparent MoS_2 TFT as V_D = 1 V before (solid) and after (open symbols) laser annealing. The L and W were equal to 2 and 1 μm, respectively. **(b)** Output characteristic (V_D–I_D) curves of the transparent MoS_2 TFT with different gate biases (V_G = 5, 10, 15, and 20 V) before (solid) and after (open symbols) laser annealing.

The laser annealing treatment allowed about five-fold enhancement of the I_{on} while the I_{off} levels of the device were not much changed. The I_{on}/I_{off} of the laser annealed device approached to ~10^4. After the laser annealing treatment, the μ_{eff} of the device was three-fold increased (4.5 cm^2 V^{-1} s^{-1}). Based on the output characteristic curves of the MoS_2 TFT shown

in **Figure 3.14(b)**, the improvement of the contact behavior in low V_D region and robust current saturation at high V_D region were observed after laser annealing. The enhancement of the TFT performances due to the laser annealing treatment was in good agreement with the results shown in **Figure 3.13**. It has been known that composition of IZO film is changed over 300 °C,[136] which can induce at IZO-MoS_2 interface by laser annealing. It seems to be oxygen poor environments in the bottom of IZO electrode at IZO-MoS_2 interface, in which oxygen deficient defect can be produced by heat generated through laser annealing. The conductivity of interfacial side in IZO electrodes would increase due to these oxygen deficient defects resulting in the reduction of R_c between IZO and MoS_2.[137,138]

3.6 Summary

A laser enabled the achievement of superb interfacial characteristics between metal and semiconducting material contact surfaces, resulting in reduced R_c and improved interfacial morphology. An analysis of the temperature distribution, based on finite difference methods, enabled understanding of the compatibility of our picosecond laser annealing for flexible PEN substrates with low thermal budget (< 200 °C)

The mechanical flexible MoS_2 TFTs in which the source/drain electrodes were selectively annealed using picosecond laser annealing achieved the enhancement of device performance without plastic deformation, such as higher mobility (from 24.84 to 44.84 $cm^2V^{-1}s^{-1}$), increased output resistance (0.42 MΩ at $V_G - V_{TH} = 20$ V, a three-fold increase), a six-fold increase in the self-gain, and decreased SS. TEM analysis and current–voltage measurements suggested that the reduced R_c resulted from the decrease of Schottky barrier width at the MoS_2–metal junction. To estimate the laser annealing effect on device performance more clearly, YFM was used to extract R_c, μ_0, and the relationship between them. On the basis of the comparison between the μ_{eff} (including contact effects) and μ_0 (excluding contact effects) extracted from the YFM before and after laser annealing, the results are indicated that enhanced performance results from not only the improved contacts but also an increase in interface quality. Note that the enhanced contact has a much greater effect than improving interface quality.

Furthermore, the performances of optically transparent (more than 81% transmittance in the visible wavelength range) multilayered MoS_2 TFTs with the IZO electrodes also were improved; the μ_{eff} and the I_{on}/I_{off} approached up to 4.5 $cm^2V^{-1}s^{-1}$ and ~10^4, respectively. Even taking into account the high work function of IZO, the transparent MoS_2 TFTs exhibited quite moderate electrical performances because of the intrinsic defects in natural MoS_2, which would play a role in lowering the Φ_B.

These results demonstrate that selective contact laser annealing can be an attractive technology for fabricating low-resistance metal–semiconductor junctions, providing important implications for the applications of high-performance 2D semiconductor FETs in flexible electronics.

Chapter 4

Non-vacuum and Maskless Laser Direct Writing for MoS_2 Transistor of Enhanced Mobility with Sol-gel ZrO_2 High-k Dielectric

4.1 Laser Direct Writing (LDW)

Conventional photolithography in the micron or sub-micron range using multiple masks has achieved contributions of enormous impact that have been driving continual improvement. Nevertheless, commercially available lithography systems presume high capital investment, implying that alternative low cost equipment should be considered. LDW is one of the very strong candidates to answer these demands.[139,140]

LDW is maskless process that offers compact and flexible optical elements. A key advantage of the maskless lithography is the ability to change lithography patterns frequently from one run to the next, without incurring the cost of generating a new mask. Note that the process is programmable; we can easily make and design arbitrary 2D patterns with smooth features through computer-controlled programs without complicated process for producing the masks. Also, LDW enables non-vacuum working environment and physically non-contact process between the tool and the material of interest.

4.2 High-k Dielectric Materials

Among the parameters for evaluating the fabricated devices, the mobility plays a critical role to promote the performance of devices and circuitry. The μ_{eff} decides not only DC characteristics, directly, but also AC characteristics related to the cut off frequency. Up to now, many approaches have suggested to promote this property. First, controlling the work function of source and drain electrodes is one strategy to minimize transport barriers.[64] Second, selective laser annealing or thermal annealing allows improving the R_c at metal-semiconductor junctions as well as the interface between 2D TMDCs and dielectric layer.[37,43,102,103] Last, by adopting high-k metal oxide insulators, the phonon scattering can be suppressed and the interface quality between insulator and semiconductors can be improved. [37,114]

In particular, sol-gel processed metal oxide high-k such as Al_2O_3 or ZrO_2 has been investigated because it is possible to form high quality metal oxide insulator without relying to costly conventional vacuum processes based on the deposition tools and at the same time deliver enhanced μ_{eff}.[141]

4.3 Sol-gel ZrO_2 of MoS_2 Transistor Fabricated by LDW

The MoS_2 FETs with high-k insulator could help decrease the operation voltage and to realize smaller and thinner devices. Critically, by suppressing Coulomb scattering in MoS_2 channel, it is possible to realize the low power device operation with increased gate control and drain current.[37,142,143] Up to now, ALD technique has been used to deposit sub-100 nm thick and uniform metal oxide insulator.[144-146] Unfortunately, low deposition rate and high cost precursors make its use impossible in industry.

In this section, I demonstrate a) highly boosted performance of MoS_2 TFTs on sol-gel processed high-k ZrO_2 insulator and b) a patterning process for source/drain electrodes is conducted by LDW techniques.

4.3.1 Device preparation

High-k ZrO_2 insulators were formed based on sol-gel process. Before forming ZrO_2 layers, commercial ITO deposited glass substrates were cleaned with acetone, methanol, and DI water, sequently. Zirconium (IV) acetylacetonate was purchased from Aldrich and used as received. 0.487g of Zirconium (IV) acetylacetonate was dissolved in 10 ml ethanol with 0.1 *mol* mono-ethanolamine as the stabilizer. Ultra-sonication over 1 hour in air yielded stable and clear precursors. The prepared ZrO_2 thin film was formed on 10 min UV/ozone treatment ITO glass substrates (**Figure 4.1(a)**). Multiple coatings were performed for obtaining 70 nm thick ZrO_2 film. Drying was applied at 300 ^oC for 1 min in air between each spin coating step. High temperature sintering was conducted at 500 ^oC for 1 hour in O_2.

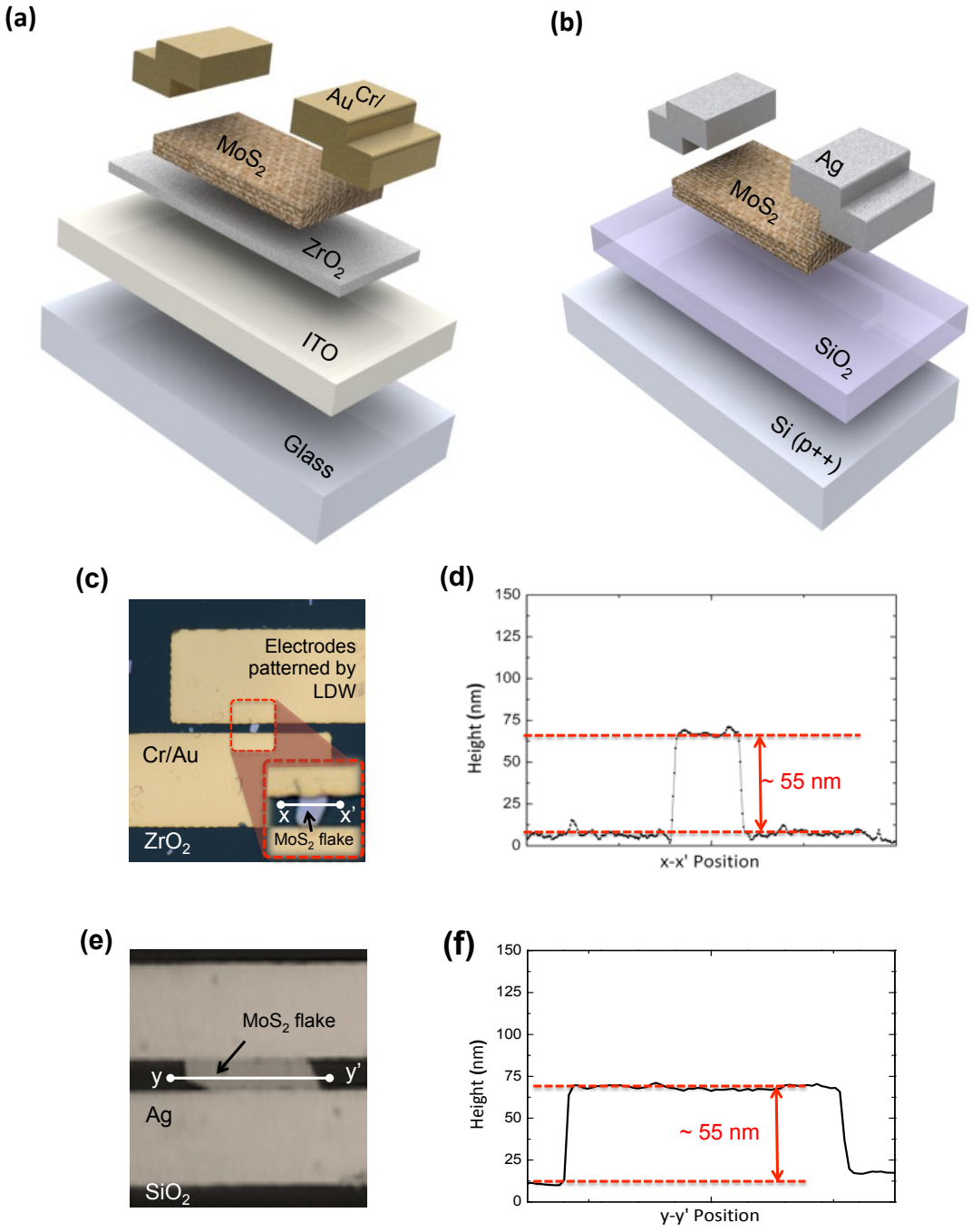

Figure 4.1 Multilayered MoS_2 FETs structures. The cross-sectional schematic structure of fabricated multilayered MoS_2 FETs **(a)** with solution based sol-gel high-k ZrO_2 gate dielectric on the ITO electrode and **(b)** with a 300 nm thick SiO_2 gate dielectric on the silicon substrate. **(c)** The top-view of the confocal laser microscope image for fabricated MoS_2 FETs with the sol-gel ZrO_2 and Cr/Au electrodes drawn by LDW. Note that a channel width and length are 2 μm and 2 μm, respectively. **(d)** Surface profile for x-x' position of MoS_2 channel on the sol-gel ZrO_2 with the thickness of ~ 55 nm measured by AFM. **(e)** The top-view of the optical microscope image for fabricated MoS_2 FETs with SiO_2 and Ag electrodes drawn by LDW. Note that the reference device has a channel length of 2 μm and a width of 7 μm. **(f)** 2D AFM topography of MoS_2 flake placed on SiO_2 with ~ 55 nm thick.

The formed ZrO_2 insulators were confirmed by X-ray powder diffraction (XRD) spectra in **Figure 4.2(a)**; the XRD peaks are well matched with the reference of ZrO_2 structure and show we show the formation of high quality crystalline. And the extracted dielectric constant was ~22 at 20 Hz. However, trap-related dispersive effects make the change of the dielectric constant; it decreased slightly as the frequency increased to 100 kHz (**Figure 4.2(b)**).

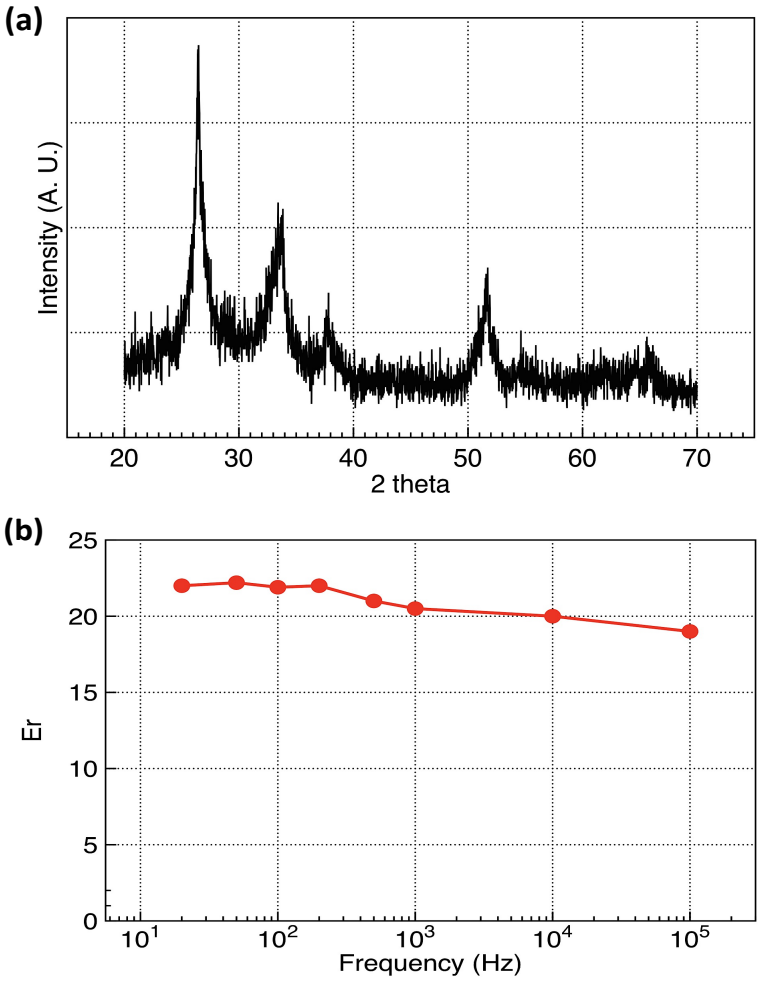

Figure 4.2 (a) The XRD spectra of the sol gel processed ZrO_2 layer, processed at 500°C for 1 hour in O_2. **(b)** The dielectric constant of sol gel processed ZrO_2, corresponding to frequency.

To investigate the ZrO_2 impact on the performance of TFTs, I also fabricated reference devices on thermally grown SiO_2 (100 nm)/Si (P^{++}) substrates as shown in **Figure 4.1(b)**. For the semiconducting channel, multilayered MoS_2 films were exfoliated both on sol-gel processed ZrO_2 insulator/ITO/Glass substrates and on thermally processed SiO_2/Si substrate as reference (**Figure 4.1(a), and 4.1(b)**). Note that the thicknesses (measured by AFM) of formed multilayer MoS_2 flakes onto the sol-gel ZrO_2 and SiO_2 dielectric films are ~ 55 nm (see **Figure 4.1(c) - 4.1(f)**).

After depositing positive photoresist (Fujifilm, OiR-906-12, i-line) with thickness of ~ 1.2 μm by spin coating at 2000 rpm for 60 sec, the LDW technique was employed to form windows for the source and drain electrodes. After making the LDW patterns, the Ag (50 nm) or Chrome (Cr, 5 nm)/Au (50 nm) source and drain electrodes were deposited by thermally evaporation technique, followed by lift-off process. The electrical characteristics of fabricated MoS_2 TFTs with different structures were measured with an Agilent 4155 semiconductor parameter analyzer at room temperature in air.

4.3.2 LDW lithography and behavior

Figure 4.3(a) shows a schematic image of our LDW lithography system. A laser source with a maximum power of 3.5 W at 355 nm wavelength was used for the exposure. The applied beam power was of the order 1.5 μW manipulated by combining a half-wave plate and a polarizing beam splitter (PBS). The irradiated laser beam was focused through infinity corrected objective lens (Mitutoyo, numerical aperture (NA)=0.5, focal length=2 mm, and magnification=100×).

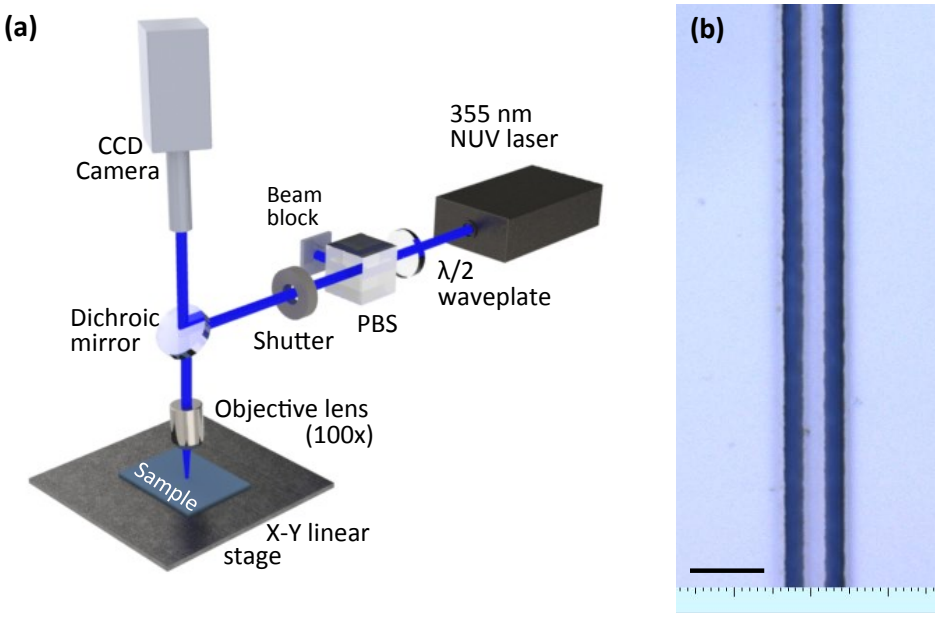

Figure 4.3 LDW lithography system. **(a)** Schematic diagram of the experimental optical setup for LDW process. **(b)** The top-view of a confocal laser microscope image of line patterns of positive photoresist (i-line) through moving the linear stage with the speed of 20 μm/s after the process of LDW and development. The patterned line width is 2.2 μm and scale bar is 10 μm.

I note that there are various laser beam delivery configurations, including fixed focusing objectives and mirrors, galvano-metric scanners, optical fibers, liquid-core waveguides, or water jets.[140] In this experiments, I used a fixed and high magnification objective lens to create fine patterns as well as to observe small objects through the camera. Focused laser beam through the objective lens induced a photochemical reaction into the spin-coated photoresist, and the sufficiently exposed area became soluble in the developer, resulting in a

positive image. As shown in **Figure 4.3(b)**, the desired patterns with the line width of ~ 2.2 μm was achieved by moving the substrate with a scanning speed of 0.02 mm/s mounted on the motion-control stage (Aerotech, ANT95, translation resolution ~ 10 nm). The shape of the patterns is only limited by the degrees of freedom and resolution of the apparatus.

To better understand LDW lithography and to control the shape of the patterns, we have performed the series of experiments with different laser power (0.5, 5.0, and 50.0 μW) and scan speeds of the stage (0.001, 0.01, 0.1, 1.0, and 10.0 mm/s). **Figure 4.4(a)** shows the variation of the positively patterned single line on the Si/SiO_2 substrate after the LDW lithography and development processes. The results indicate that the morphology of LDW lithography was determined from the relation between laser power and exposure time that is manipulated by the scan speed. As the laser power increases, the scan speed can be faster, however the shape of patterns become more sensitive to irregular mechanical translation (e.g. acceleration, deceleration) and the ambient conditions (e.g. vibration). To elucidate these factors, I measured the morphology of the top surface as well as the cross sectional surface profiles through a 3D confocal laser microscope (Olympus, LEXT OLS4000) as shown in **Figure 4.4(b)** and **4.4(c)**.

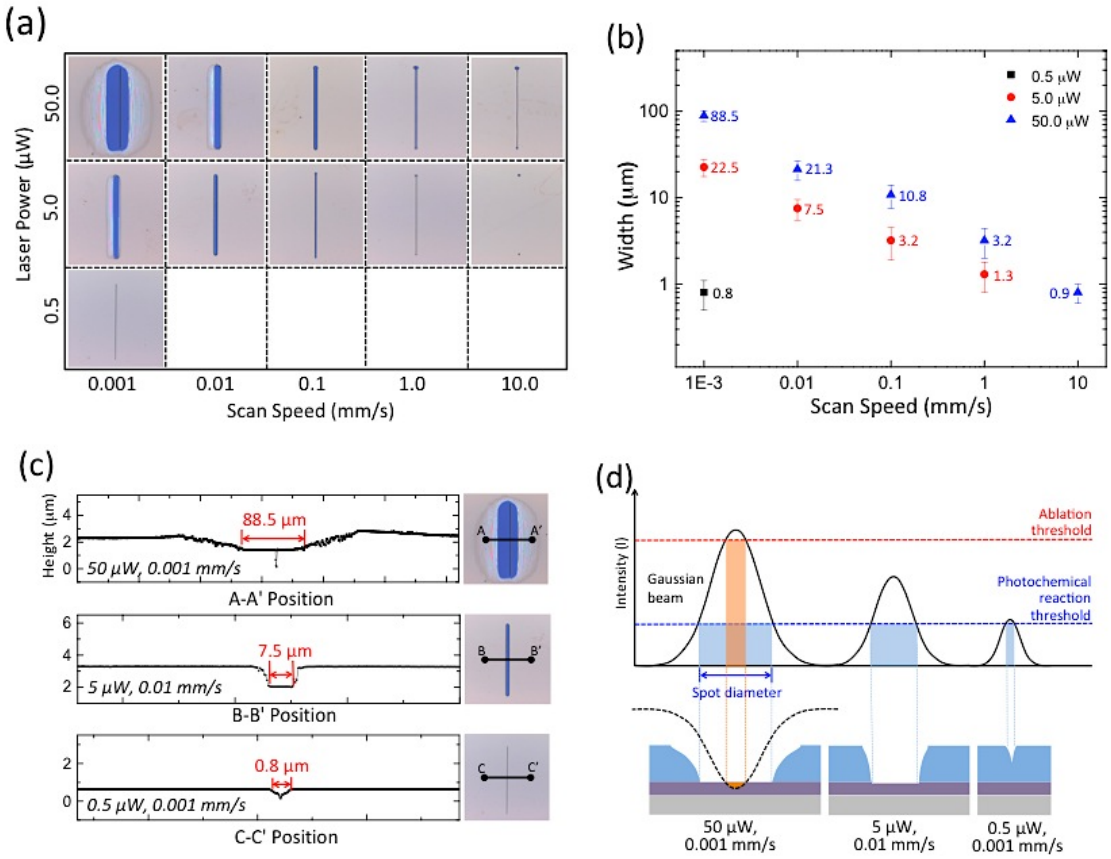

Figure 4.4 Various LDW lithography behaviors. **(a)** Comparison of the positively patterned geometry for different laser power and scan speed on the Si/SiO_2 substrate and **(b)** their quantitative measurements of the line width with the linear trend. **(c)** Cross sectional profiles of the representative three patterns **(d)** with different intensities of the laser: superfluous, moderate, and insufficient exposure conditions.

In the LDW lithography system, the TEM_{00} has been used and irradiated with a Gaussian shape. The intensity of the Gaussian laser-beam within the focal plane has the form, $I(r) = I_0 \exp(-2r^2/w_e^2)$, where w_e is the radius of the laser focus defined by $I(w_e) = I_0/e^2$, $w_e = \sqrt{2}w_0$, producing a linear on a logarithmic scale line width trend. The width can be tuned from over 20 μm to below 1 μm by modulating the laser power and scan speed (**Figure 4.4(b)**). However, each condition for the LDW lithography has different cross-sectional surface profiles as shown in **Figure 4.4(c)**. For example, a superfluous exposure case (50 μW, laser power and 0.001 mm/s, scan speed) made not only considerably wide line patterns (~ 90 μm) with a gentle slope, but also the ablated damage to the substrate because the excess energy (over ablation threshold) contributed to the ablation process and consequently, more energy was absorbed the underlying substrate and the beam profile which possessed the edge of the Gaussian energy distribution reflected the patterns with the slow grade side walls as a footprint (**Figure 4.4(d)**). Here, I note that this fact can negatively affect the next lift-off process. These facts force to face the limitations to increase power and speed. On the other hand, an insufficient exposure condition (0.5 μW, laser power and 0.001 mm/s, scan speed) was not enough to make patterns because the intensity just closed the photochemical reaction threshold (**Figure 4.4(d)**).

Laser power of 5.0 μW and scan speed of 0.01 mm/s created good patterns with a precipitous drop along the rim of the patterned lines. Additional experiments defined a well-suited condition: laser power of 1.5 μW and scan speed of 0.02 mm/s. Note that the obtained line width is ~ 2.2 μm with vertical walls (**Figure 4.3(b)**).

4.3.3 Electrical performance

Figure 4.5 shows representative electrical characteristics of the fabricated MoS_2 TFT on SiO_2/Si substrates with a channel length of 2 μm and a width of 7 μm. Also, the relationship between I_D and V_D with selected biased V_G is denoted in **Figure 4.5(a)**. All curves showed saturated I_D, as a function of V_D in the range from 0 to 15.0 V, with V_G ranging from -15.0 to +15.0 V in steps of 5.0 V. However, the fabricated MoS_2 TFTs no longer exhibit the ideal transistor saturation when V_G is below than 0 V (**Figure 4.5(a)**). This inability to saturate, called as the 'kink' effect, is normally observed in short channel devices.[147] Especially, the kink effect was revealed when V_G is lower than V_D. This originates from that for high V_D, as the channel current is accelerated by lateral high electric field, to support enough energy for carriers to generate the electron-hole pair by impact-ionization. Also, the fabricated MoS_2 TFT shows the conventional *n*-type semiconductor behavior with negative V_{TH}. Especially, at low V_D, the linear relationship between the I_D and V_D is revealed. The Φ_B between electrodes and semiconductor is the critical factor reducing the major carrier transport and decreasing the μ_{eff} in linear regime (μ_{linear}).[64] The relationship between the I_D and V_G with low V_D and high V_D is illustrated in **Figure 4.5(b)**. The extracted μ_{linear} and $\mu_{saturation}$ are 20.1 cm^2/Vs and 19.4 cm^2/Vs, respectively. The μ_{linear} and $\mu_{saturation}$ are evaluated by using the simple FET model described in **Equation (4.1)** and **(4.2)**:

$$\mu_{linear} = \frac{g_m L}{C_i W V_D} \tag{4.1}$$

$$I_D = \frac{W \mu_{saturation} C_i (V_G - V_{TH})^2}{2L} \tag{4.2}$$

Here, $g_m = dI_D/dV_G$ is the transconductance and W and L are the channel width and length, respectively. C_i is the unit area capacitance. The extracted μ_{linear} is close to the $\mu_{saturation}$ because of the Ohmic contact between electrodes and semiconductors. The deposited Ag electrodes, whose work function is ~ 4.5 eV, are suitable for *n*-type MoS_2 transistors compared to Ti/Au electrodes.

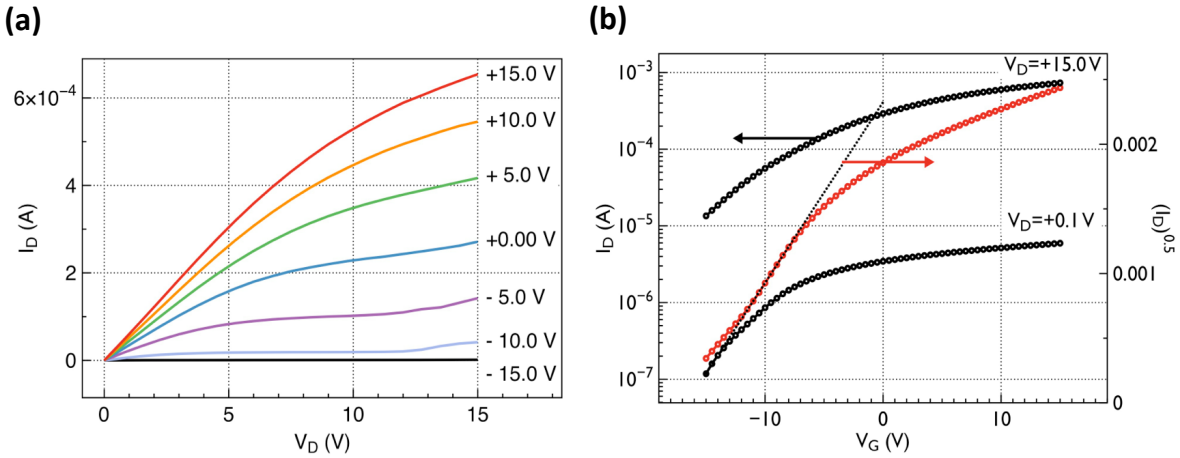

Figure 4.5 The representative electrical characteristics of fabricated MoS_2 TFT on SiO_2 at room temperature: **(a)** the plot of I_D-V_D; and **(b)** plots of I_D-V_G (left axis) and $I_D^{0.5}$-V_G (right axis) at V_D = +15.0 V and +0.1 V, respectively.

Figure 4.6 shows electrical characteristics of the fabricated MoS_2 TFT on sol-gel processed ZrO_2 insulators with Cr/Au source and drain electrodes. In a first attempt, Ag source and drain electrodes were deposited. Unfortunately, at low operation voltage (below 1.0 V), conductive filaments were formed between the bottom electrode (ITO) and Ag electrodes through the sol-gel processed ZrO_2 insulator. Therefore, the fabricated MoS_2 devices did not exhibit transistor characteristics. This might be due to Ag diffusion from the Ag electrode, when low voltage was biased through electrodes.[148] For this reason, Cr/Au electrodes were selected as the source and drain electrodes instead of Ag electrodes.

Figure 4.6(a) shows the relationship between the I_D and V_D of the fabricated MoS_2 TFTs on sol-gel processed ZrO_2, as a function of V_D in the range from 0 to +3.0 V, with V_G ranging from -3.0 to +3.0 V in steps of 1.0 V. These devices have a channel length of 2 μm and a width of 2 μm. By employing high-k insulators (dielectric constant: ~ 22.0 at 20 Hz), I could

reduce the operation voltages. Also, unlike the case of SiO_2 low-k insulator, vertical strong electric field can suppress the aforementioned kink effect and the relationship between I_D and V_D at low V_D did not show the linear relationship. Note that the work function of Cr is ~ 4.5 eV. The extracted μ_{linear} and $\mu_{saturation}$ were 20.8 cm^2/Vs and 50.1 cm^2/Vs, respectively, reflecting the Φ_B (**Figure 4.6(b)**). It is well known that the R_c usually affect less the $\mu_{saturation}$ than the μ_{linear}.[62] In addition, the relationship between I_D and V_D, at low V_D, did now show the ideal linear relationship anymore. Comparing to MoS_2 TFTs on SiO_2/Si substrates, the μ_{eff} was enhanced more than ~ 2.5 times.

Up to now, a high-k dielectric layer was normally used to minimize the effect on Coulomb electron scattering.[37,43,114] Additionally, the interface quality between insulators and semiconductors is important in order to realize the high performance devices.[114] In the case of MoS_2 TFT on sol-gel processed high-k insulator, the μ_{eff} enhancement can be ascribed to the interface properties between MoS_2 and dielectric layer. In this case, the interface trap density (D_{it}) is employed to estimate the interface quality using the equation:[149]

$$D_{it} = \frac{C_i}{q}\left(\frac{qSS}{KTln10} - 1\right) \tag{4.3}$$

Here, q is the electron charge, SS is the subthreshold swing, and T (300 K) is the measurement temperature. By using the sol-gel processed ZrO_2 insulator, the estimated swing value is reduced from 7.1 V/decade to 0.7 V/decade. The extracted the values of D_{it} are 2.55×10^{13} $cm^{-2}eV^{-1}$ (for MoS_2/SiO_2 stacks) and 1.87×10^{13} $cm^{-2}eV^{-1}$ (for MoS_2/ZrO_2 stacks), respectively. The improved interface quality leads to the μ_{eff} enhancement.

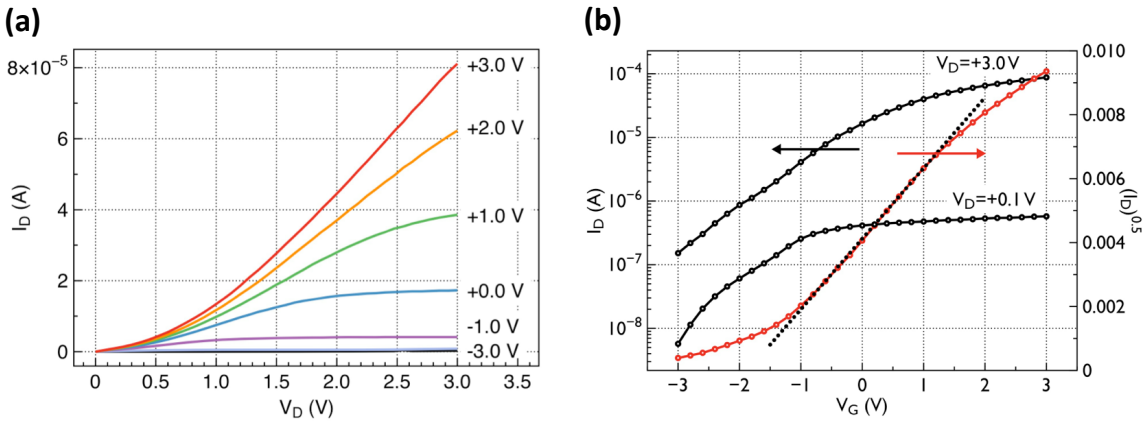

Figure 4.6 The representative electrical characteristics of fabricated MoS_2 TFT on sol-gel processed ZrO_2 at room temperature: **(a)** the plot of I_D-V_D; and **(b)** plots of I_D-V_G (left axis) and $I_D^{0.5}$-V_G (right axis) at V_D = +3.0 V and +0.1 V, respectively.

4.4 Summary

In summary, LDW enables arbitrary placement and geometry control of lift-off windows for fabricating metal electrodes with small feature size (~ 1 μm). The short channel effects were observed from the MoS_2/SiO_2 device with a channel length of 1 μm.

To suppress the strong field, thin high-k ZrO_2 insulator was used. Without using conventional vacuum based deposition process, I deposited high-k ZrO_2 insulator by sol-gel process. By employing sol-gel high-k ZrO_2, the interface quality improved dramatically, leading to μ_{eff} enhancement in the saturation regime (~ 2.5 times) at low voltage operation below 3.0 V; I reported highly boosted μ_{eff} (=50.1 cm^2/Vs, ~ 2.5 times) of MoS_2 TFTs through sol-gel processed high-k ZrO_2 (~ 22.0) insulator, compared to general $MoS_2/SiO_2/Si$ structures (μ_{eff}=19.4 cm^2/Vs).

This process allows precise and flexible control with reasonable resolution (up to ~ 10 nm), depending on the system and enables fabrication of arbitrarily patterned devices that are impractical to make via conventional methods. Taking advantage of continuing developments in laser technology that offer substantial cost decrease, LDW may emerge as a promising technology. Also, sol-gel processed metal oxide high-k ZrO_2 is possible to form high quality metal oxide insulator without using the costly conventional vacuum processes based on the deposition tools and to deliver boosted μ_{eff}.

Chapter 5

Laser-Induced Fine Patterns and Ink-Jet Printing Process for MoS_2 Transistors

5.1 Fine Patterns through Laser

In a direct write approach, aforementioned LDW lithography in resists can enable the simplification of the process and system at reduced costs; the desired structures and patterns are directly built without the use of masks (see **Section 4.1** for detailed explanations). Therefore, LDW techniques can be utilized in a wide range of applications; they allow fabrication of passive electronic components and interconnections and applications in tissue engineering and array-based biosensors.[139] It is noted that there are many different LDW approaches, each with its own merits and faults.

For finer features, e-beam and focused ion beam are considered as attractive methods. The techniques allow for the site-specific nano-machining to unprecedented levels of precision and accuracy but they are subject to low throughput. Also, DUV/X-ray exposure is a potential approach for ultra-high resolution lithography, but is quite involved in terms of equipment hardware. Confinement of optical energy to small dimensions can be achieved by coupling laser irradiation to near-field scanning optical microscopes (NSOMs).[150] Moreover, ultrafast laser (e.g. femtosecond laser) radiation drives nonlinear absorption in nominally transparent materials. Through this photo-polymerization method that is based on multiple-photon absorption, 3D stereo-lithographical structures can be formed with nano-scale feature size.

Aside from feature resolution, important challenges are scalability and throughput. Therefore, for creating high feature density structures with critical nano-scale dimensions, interference lithography is capable of fabricating patterns with 100 nm periodicity on 10 cm^2 areas.[151] In addition, in order to overcome the serial direct writing by a single probe, a probe array scheme through a digital mirror display (DMD) array and piezo-scanners has been developed at vastly increased throughput.[152]

In this chapter, among various laser-assisted direct writing processes, single line-by-line laser scanning techniques in positive and negative photo-sensitive polymer materials are dealt with to define the patterns of the electrodes of MoS_2 transistors. Moreover, interference lithography is briefly described and performed for the small length scale.

5.1.1 Line-by-line laser scanning

In the **Section 4.3.2**, line-by-line LDW lithography was already described and investigated. A basic configuration of the line-by-line laser processing is accomplished by implementing precision translation system on a single platform (see **Figure 4.3**). Note that the LDW system that I used in this research is exactly same as the LDW setup in the **Section 4.3.2**. In that case, positive photoresist, which was dissolved within illuminated area during development, was applied as photo-sensitive materials.

I also tested and applied the negative photoresist (SU-8 series, MicroChem), whose non-illuminated area dissolved. The behavior of line-by-line LDW process was the opposite of the positive photoresist; the laser-scanned area was embossed as shown in **Figure 5.1**. However, depending on the laser power, the width, height, and even the profile of remaining resist are dissimilar. The departures are because Gaussian beam profile of the laser is changed according to the intensity (**Figure 5.2**).

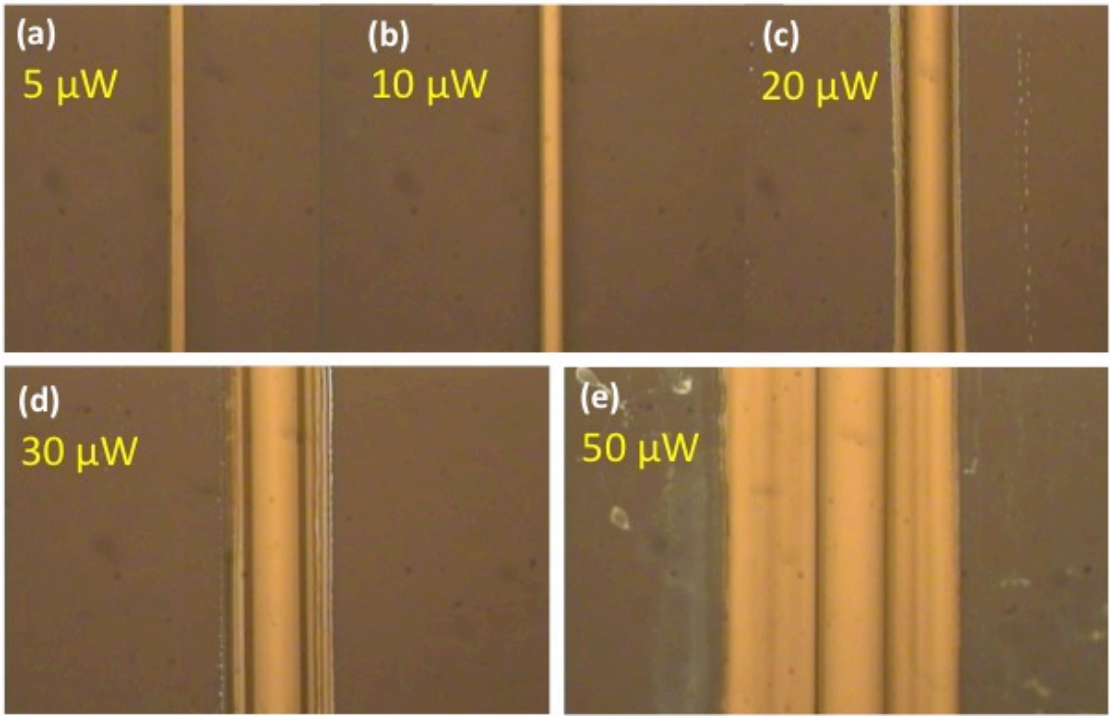

Figure 5.1 Optical microscope images of SU-8 photoresist after the LDW lithography and development. Different laser powers (**(a)** 5.0, **(b)** 10.0, **(c)** 20.0, **(d)** 30.0, and **(e)** 50.0 μW) are irradiated with 0.005 mm/s of the fixed scan speed, 355 nm of wavelength through 20 X of objective lens.

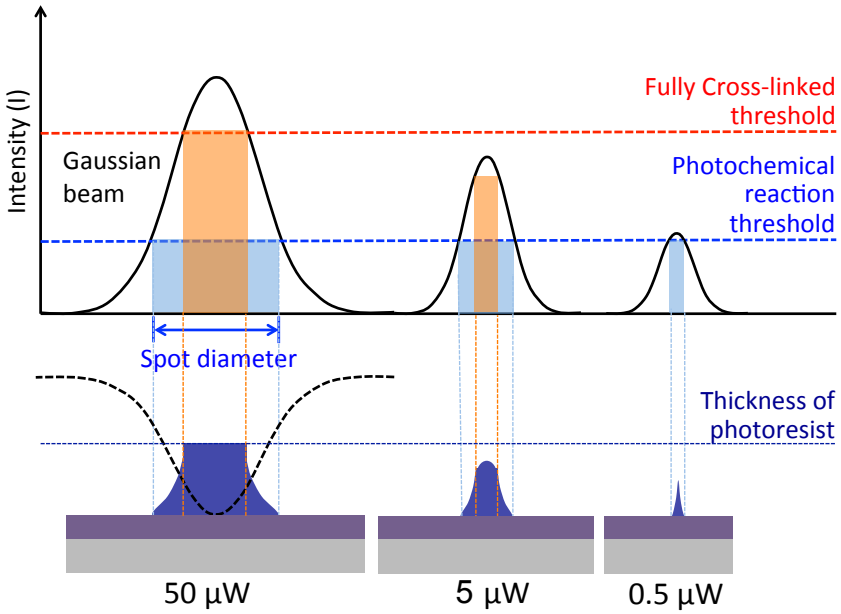

Figure 5.2 LDW lithography behaviors for the negative photoresist, SU-8. The representative three different cases with respect to the intensities of the laser: superfluous, moderate, and insufficient exposure conditions.

At 50 μW, the excess energy (over fully cross-linked threshold) contributed to make enough polymerization reaction and consequently, complete structure (the height of the structure is the same with the thickness of the photoresist) was created and the beam profile which possessed the edge of the Gaussian energy distribution reflected the patterns with the slow grade side walls as a footprint in **Figure 5.2**. The case of 5 μW, even though the structure was not fully polymerized (the height of the structure is slightly smaller than the thickness of the photoresist), gave clear pattern without any residues. Therefore, I conducted experiments once again to find more specific conditions (the correlation between laser power and scan speed) in the range of 5 μW. In addition, the profiles of the resist were measured after the development.

Figure 5.3 shows the variation of the negatively patterned single line on the Si/SiO_2 substrate after the LDW lithography and development processes. The morphologies of top surface were measured through a 3D confocal laser microscope (Olympus, LEXT OLS4000). The negative photoresist (SU-8 2005) was spin coated at 5000 rpm and the formed thickness of the photoresist was around 4.0 μm. The results indicate that the morphology of LDW lithography was determined from the irradiated dose of the laser (the exposure time manipulated by the scan speed). As the scan speed increases, the shape of patterns suggests undeveloped structures, and then the weak structures were destroyed during the development or wet rinse process; in determining the appropriate dose of the photoresist, the laser power and scan speed of the stage have the trade-off relationship.

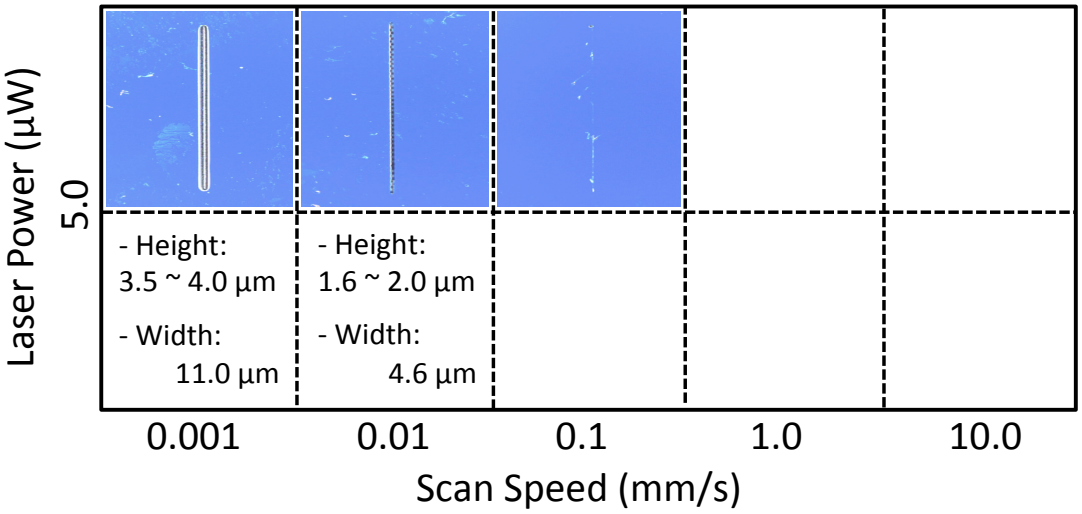

Figure 5.3 Comparison of the negatively patterned geometry for the different scan speed (fixed laser power: 5.0 μW) on the Si/SiO_2 substrate. Note that spin-coated (at 5000 rpm) photoresist is SU-8 2005 with 4.0 μm of the thickness.

In this research, 5 μW of the laser power and 0.005 mm/s of scan speed yield good results as shown in **Figure 5.1(a)**. Also, according to the test on the coated thicknesses of SU-8 2000 series (2002, 2005), SU-8 2002 and 3000 rpm of the spin speed are selected because of the stable aspect ratio. Through the photoresist and coating condition, around 1.5 μm thickness was formed.

5.1.2 Interference lithography

The reduction in the length scale brings challenges in the fabrication process. Interference lithography emerged as one of the solution. Interference is the interaction of two or more coherent waves to create a new wave pattern, periodically; in 1801, Thomas Young established and demonstrated the phenomena through the double slit experiment. The interference lithography is recording these spatially periodic patterns into a photo-sensitive media. The process is fast and low-cost and can realize very small periodic nano-patterns at large area through various methods.

Since Humphrey Lloyd described the interference using a mirror in 1843, the Lloyds' Mirror platform has been used for a lithography system. However, the exposure area (a few cm^2) is limited because of size of the mirror; making optically flat and big size mirrors without any tiny defects are very expensive and difficult. Also, dust particles attached on the mirrors distort the interference patterns. Another interferometer setup is using a split dual beam having same beam path length. The difference of the beam path length has to be within the coherence length of the beam source. However, this system is very sensitive to airflow resulting in the fluctuated patterns. The use of the phase-shift mask (PSM) makes the interference patterns with smaller pitch below the exposure wavelength. When a beam passes through a specific periodic structure (the binary phase grating), the beam can be diffracted

into multiple orders. Then, the diffracted beams generate periodic interference patterns. Even though this method requires more expense for making the PSM, it is still the mostly used and attractive technique because of the very simple setup, easier alignment, robust environment (reducing stability requirements), and adaptable lower coherence sources (e.g. ultraviolet laser, pulsed laser).

For resolution enhancement, different types of PSM are suggested. Conventional mask is binary (either 100 or 0 % transmittance), however, the distance of the patterns is reduced, the resolution is limited (patterns merge). For this reason, alternating PSM (AltPSM) and embedded attenuated PSM (EAPSM) are suggested to improve the contrast of the projected image of the mask as shown in **Figure 5.4**.[153] AltPSM has etched parts of the quartz substrate for inducing a 180° phase shift of the light (**Figure 5.4(b)**). Similarly, in the case of EAPSM (**Figure 5.4(c)**), the light goes through the partially transparent material (the desired transmission is typically 5–15%), and then the phase is shifted to 180°, instead of etched area filled with air like AltPSM. However, unwanted leakage (5-15%) can obstruct high resolution. Therefore, AltPSM is favored as resolution enhancement technologies even though fabricating uniform and accurate mask is difficult, and repairing the defects or the inspection is complicated.[153]

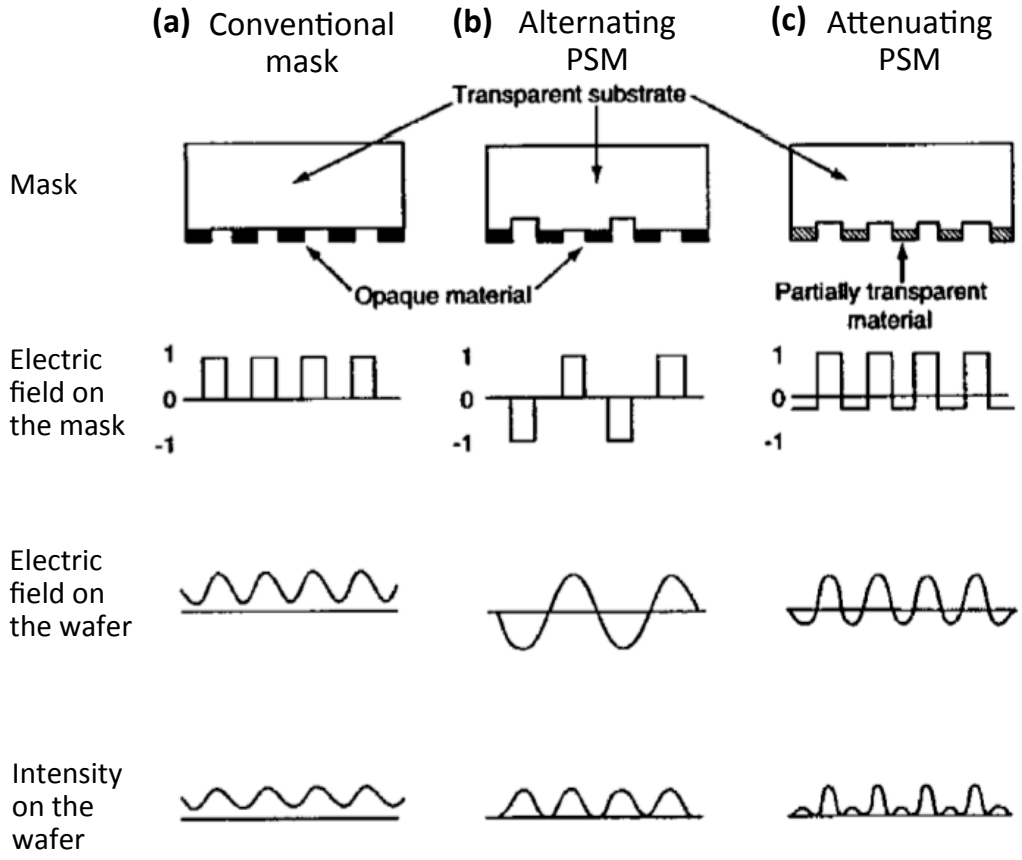

Figure 5.4 Comparison of various types of PSMs: **(a)** conventional, **(b)** alternating, and **(c)** attenuating PSMs. (image from C. Pierrat *et al.* Appl. Opt. 1995) [153]

For creating high-resolution line-space patterns, AltPSM is employed and demonstrated. **Figure 5.5** shows the top view of fabricated AltPSM (Toppan Inc.) with 350 nm of the width (for clear area, S) and 300 nm of the width (for dark area, L). In this case (350/300), pitch is 650 nm (=S+L= 350+300) and duty ratio (=L/pitch=300/650) is 0.46. Note that typically in semiconductor lithography using AltPSM, 193nm AAPSM masks with low duty ratio (i.e. the space is larger) are used. The tolerances of the phase shift and the patterns are 180°±8~10° and ±10%, respectively. Also, the etch depth (d) is 337.4 nm±5% and decided by $\Delta\Phi = 2\pi(n-1)d/\lambda$, where n is refractive index of the quartz and Φ is the phase of the light.

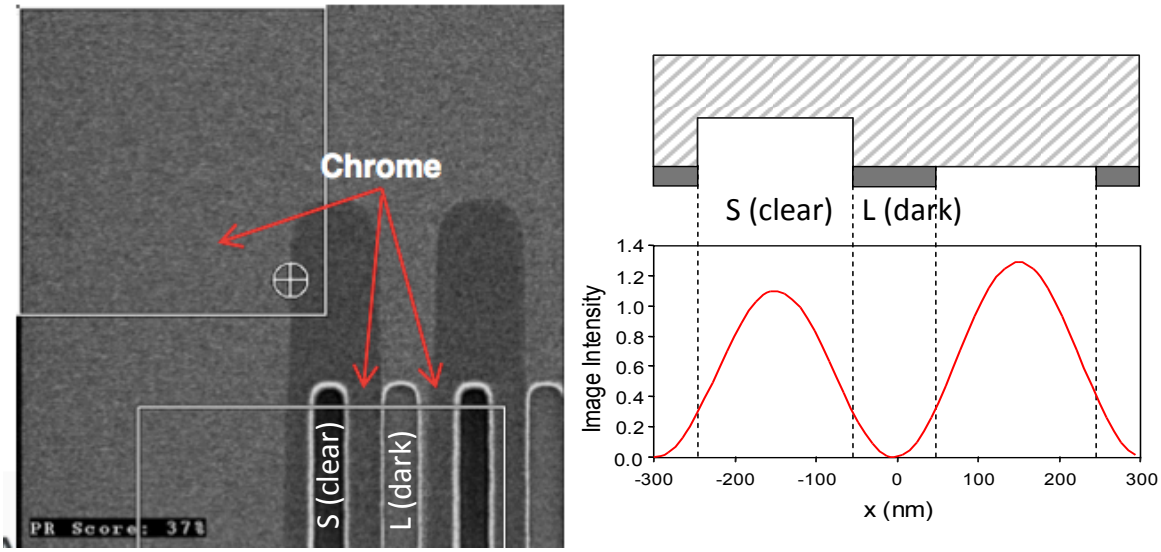

Figure 5.5 Top-View of SEM image for AltPSM with 350 nm of the width (for clear area, S) and 300 nm of the width (for dark area, L). Note that schematic cross-sectional image (right) is not a real scale; it is the example for understanding easily.

Depending on the incident angle of the laser beam, the dominant interfering orders vary. When the beam irradiates onto the AltPSM at Littrow angle ($\theta_L=\arcsin(\lambda_0/2\Lambda_{PM})$, where λ_0 is the illuminated wavelength and Λ_{PM} is the pitch of the grating of AltPSM), only the 0th order interfered with the −1st order and spatial pitch created at substrate (i.e. patterns) is equal to the pitch of the phase mask grating.[154] On the other hand, when light impinges at normal angle, the overlap of the three beams having the diffracted order -1st (>35%), 0th (<5%), +1st (>35%))[155,156] forms a static interferogram as shown in **Figure 5.6**. The expected pitch of the pattern can be calculated by the general diffraction equation:

$$\Lambda_{PM} = \frac{m\lambda_0}{\sin\left(\frac{\theta_D}{2}\right) - \sin(\theta_i)} \tag{5.1}$$

where m is number of others, θ_D is the angle of diffracted beam, and θ_i is the angle of incident light. In case that a single beam incidents and +1st and -1st orders are mainly dominant for creating the interference patterns. **Equation (5.1)** can be reduced by

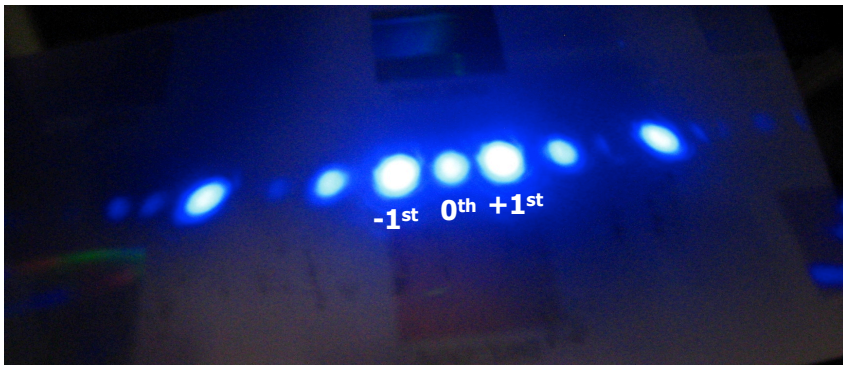

Figure 5.6 Optical photo image of diffracted beams with several orders after the light incidents at normal angle and passes through the AltPSM.

$$\Lambda_g = \frac{\lambda_0}{2\sin\left(\frac{\theta_D}{2}\right)} = \frac{\lambda_0}{2\frac{\lambda_0}{\Lambda_{PM}}} = \frac{\Lambda_{PM}}{2} \tag{5.2}$$

where Λ_g is the pitch of the grating of generated patterns. According to **Equation (5.2)**, the pitch of interference patterns is exactly half the value of the pitch of the AltPSM and it is independent of the incident wavelength.

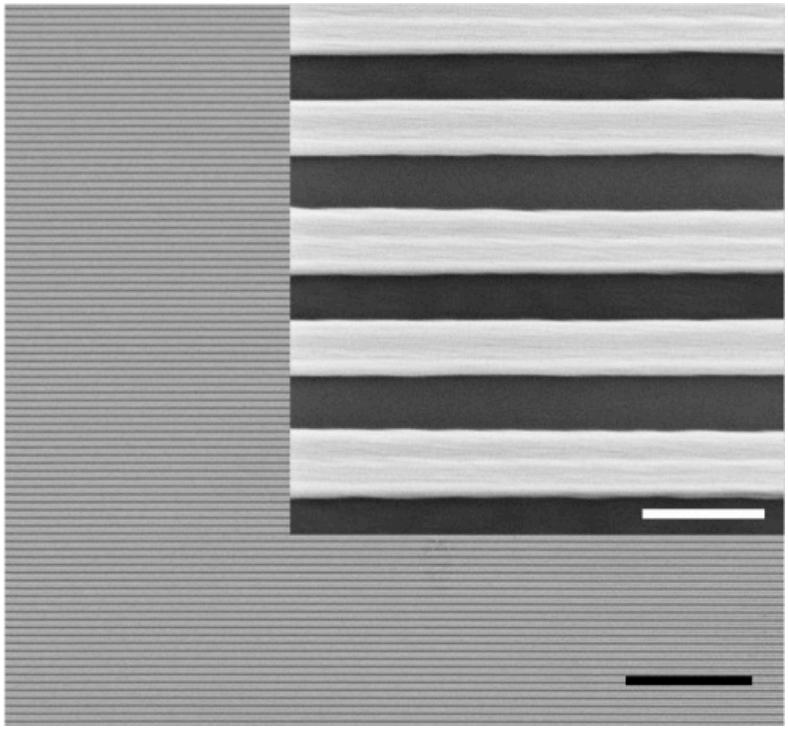

Figure 5.7 SEM images of the line-space patterns created by interference lithography using AltPSM. Note that the scale bars are 20 μm and 500 nm (inset).

To prove the theoretical prediction, the interference lithography using the AltPSM described above (see **Figure 5.5**) is performed. Based on the design of the mask, expected line-space pattern is of 149.5 nm line width with spacing of 175.5 nm. However, the real experimental result is somewhat different as shown in **Figure 5.7**. 325 nm wavelength of He-Cd continuous laser (KIMMON, Ltd.) is irradiated onto the positive photoresist (Fujifilm, OiR-906-12, i-line) coated surface. After the interference lithography and development, line-space patterns are created periodically. Dissolved line (black area in **Figure 5.7**) width is ~ 200 nm and the remaining untouched space (white area in **Figure 5.7**) is ~ 400 nm. The values are slightly larger than expected values. The deviation could come from non-parallel mask and substrate, from incident angle of the light different than normal, or from overdevelopment. However, high-resolution (smaller than the pitch of the mask and the wavelength) patterns are definitely obtained through AltPSM.

5.2 Ink-Jet Printing Process

Printed electronics technology has attracted considerable interest for realizing low-cost, low-temperature, flexible, and large-area electronic systems such as TFTs with uses in applications (e.g. displays, radio-frequency identification tags, microelectomechanical Relays, inverters).[157-162] Although printed TFTs have shown drastically improved electrical characteristics in recent years,[163-165] further improvement is still needed with respect to power-consumption, environmental stability, SS, and I_{on}/I_{off}.

For making printed devices, ink-jet, screen, roll-to-roll including flexography, off-set, and gravure processes are the most encountered as printing technologies. However, there is no best printing method because of dimensional and geometrical considerations of the target surfaces and fluidic and wetting characteristics of the inks. Among the printing methods, ink-jet printing is more versatile, compatible with variety of substrates and materials; it can also print on shaped objects.

Because of these many benefits, ink-jet printing process is employed for making the electrodes. Depending on the type of photoresists, capillary and self-alignment help to control ink-jet printed nano-ink. They are also investigated in this section.

5.2.1 Capillary with positively laser patterned geometry

Using the LDW lithography (see **Section 4.3.2**) and positive photoresist (OiR-906-12, Fujifilm, i-line), line patterns are created, and then a Ag nano-particle based ink (CCI-300, Cabot Corp.) is jetted out onto the patterns. The fabricated patterns are filled with inkjetted Ag ink to form the electrodes using the Dimatix printer (Fujifilm). At this time, the line patterns act as a channel and capillarity between the channel and the ink is the driving force in **Figure 5.8**. However, as shown in **Figure 5.8**, the range and behavior of filled ink are different under certain circumstances. Therefore, we need to understand the relationship between capillary and the geometry of the channel.

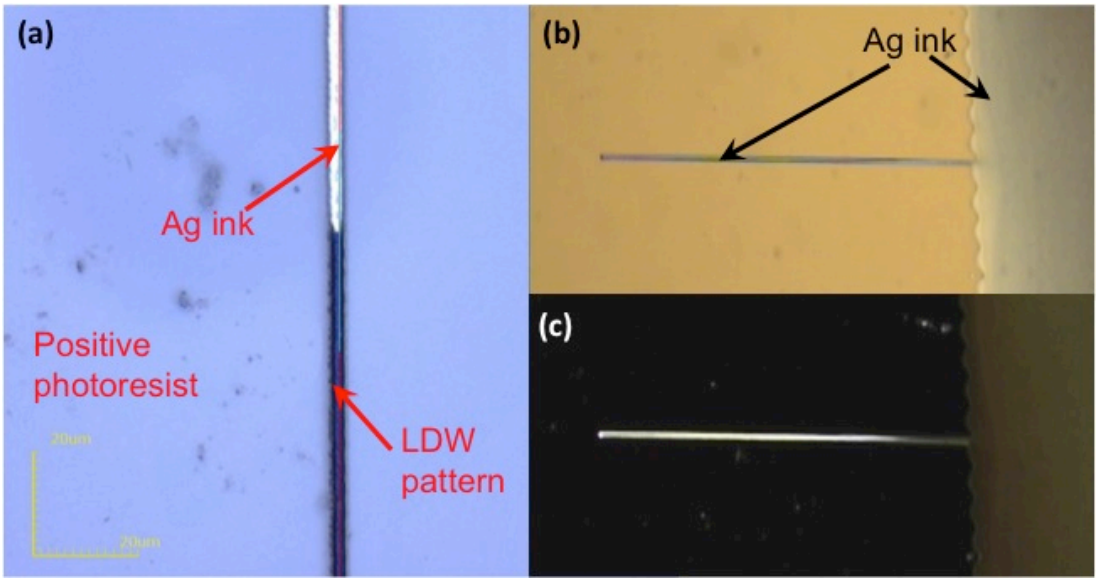

Figure 5.8 (a) The top-view of a confocal laser microscope image of line patterns of positive photoresist and partially filled Ag ink after the process of LDW and ink-jet printing of Ag ink. **(b)** Optical microscope image of completely filled Ag ink under the bright field (BF) and **(c)** the dark field (DF).

As the patterned channel is open at the top, the volume flow rate (Q) is expressed in the open channels:[166,167]

$$Q = \frac{1}{\eta}\frac{\Delta P}{R_f} \tag{5.3}$$

where η is the viscosity of the ink, ΔP is the difference of pressure between the fronts of the ink and the air. R_f is the flow resistance given by:[166,167]

$$R_f = \frac{12L}{R_h^2 A}(1 - 1.3553a + 1.9467a^2 - 1.7012a^3 + 0.9564a^4 - 0.2537a^5) \tag{5.4}$$

where L is the filled length of channel, R_h is the hydraulic radius of the channel, and A is cross-sectional area of the channel. Moreover, *a* is the aspect ratio defined as height (*h*)/width (*w*) (if $h \leq w$) within the range ($0 \leq a \leq 1$).

To increase the magnitude of Q for the printed Ag ink inside the channel, R_f should be reduced (**Equation (5.3)**). In addition, among many variables, *a* is a very sensitive factor to decrease the value of R_f based on **Equation (5.4)**. Therefore, *a* should be increased in order to lessen R_f. However, increasing *h* related to the thickness of the channel is subject to limitation because of the speed of spin coater and fixed material properties of the photoresist, especially for the viscosity. Therefore, creating small *w* is the best or only way to boost the Q, effectively.

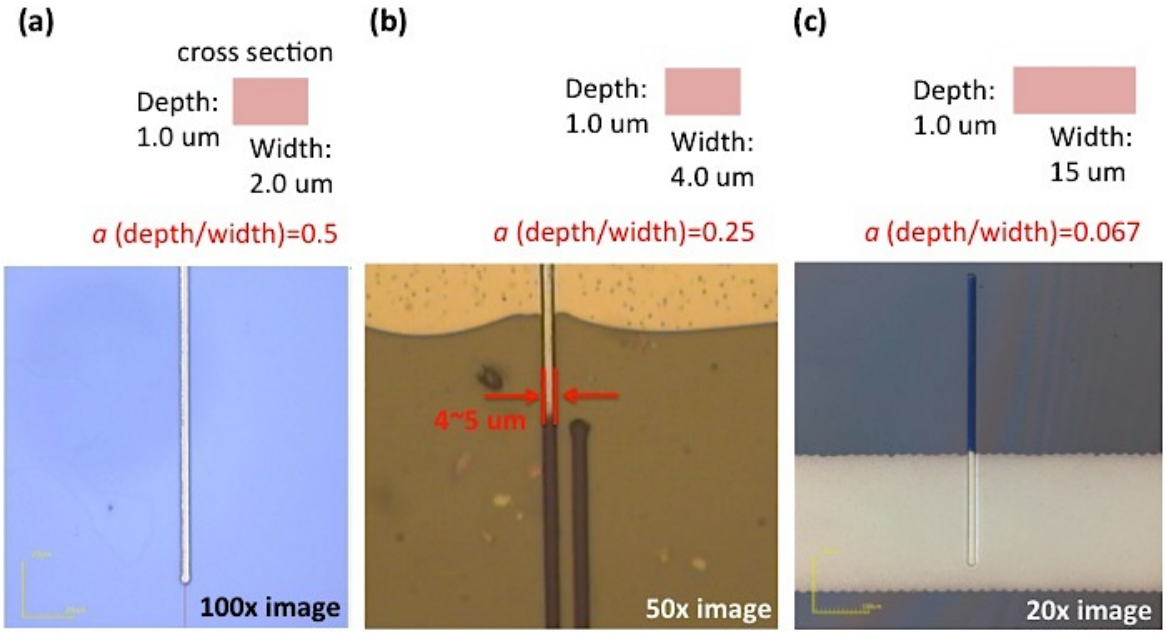

Figure 5.9 The top-view images of line patterns with varying width of the channel using positive photoresist and filled Ag ink after the process of LDW and ink-jet printing. The thicknesses of spin-coated photoresist are the same (~ 1.0 μm), however, the widths are different: **(a)** 2.0 μm, (a = 0.5), **(b)** 4.0 μm, (a = 0.25), **(c)** 15.0 μm, (a = 0.067).

Figure 5.9 shows the results of capillary effect with respect to the width of the channel. As the results, increasing a (as decreasing w) is effectively reflected in the value of R_f; to make enough capillary force, a should be 0.5 or higher (i.e. w must be smaller than 2.0 μm in **Figure 5.9(a)**). Note that the photoresist with 1.0 μm of the thickness is formed by spin coating process at 2000 rpm; when lower than 2000 rpm, the uniformity of the thickness of the photoresist becomes worse.

Based on the experimental result, filling the channel with Ag ink is carried out successfully as shown in **Figure 5.10**. Even though the filled length was relatively long (mm scale), the empty patterns or channels were filled with the ink completely. After the ink-jet printing, the filled ink sintered at 180 ℃ for 30 min at a hot plate for improving electrical conductivity and connections.

Also, the profile of the filled ink is measured by 3D confocal laser microscope (LEXT OLS4000, Olympus). Because of high surface energy of the photoresist, the contact angle between the photoresist and Ag ink is below 90°; the capillary force pulls the ink into the top of the channel. Therefore, the ink inside the channel forms a concave meniscus (**Figure 5.10**).

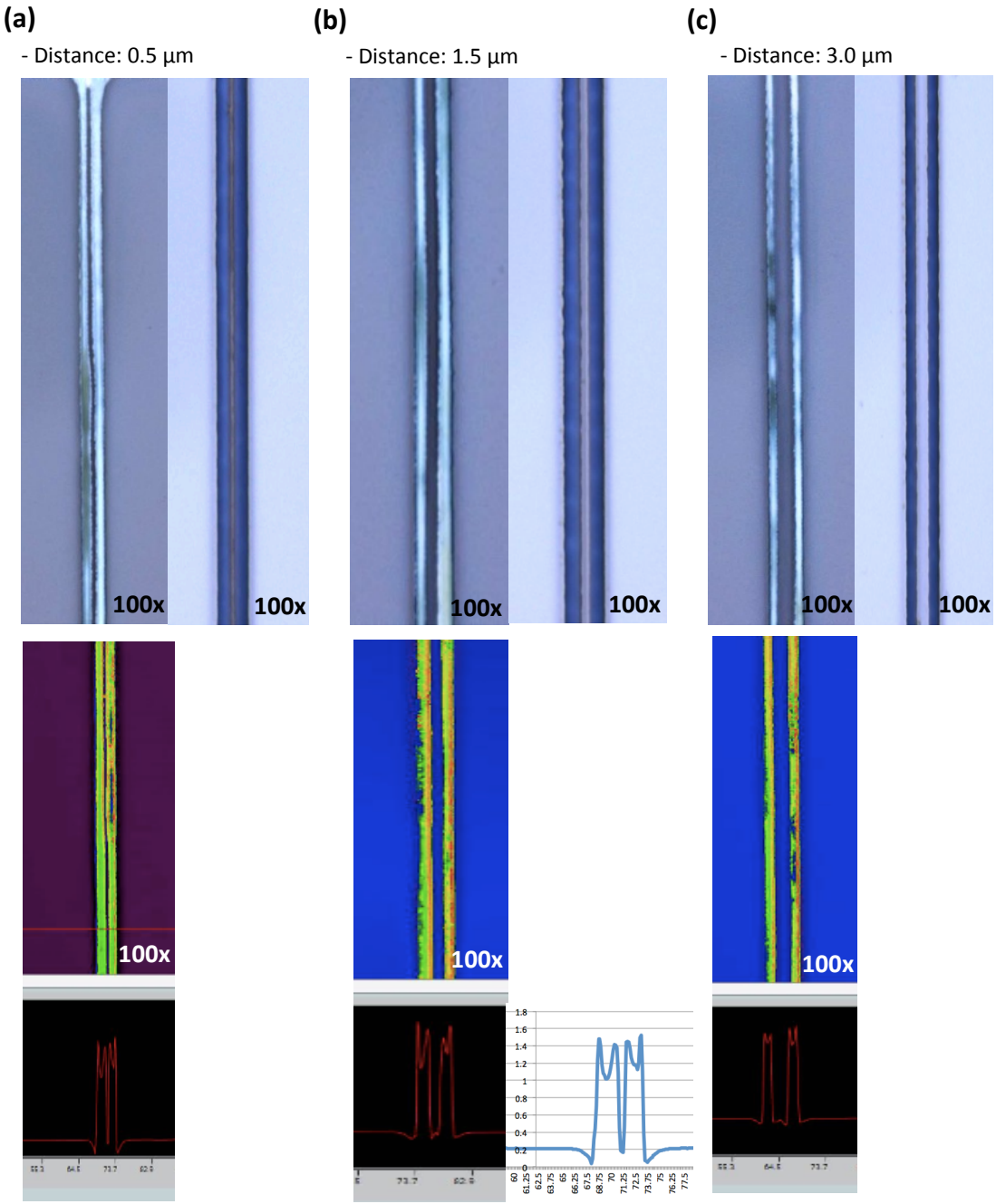

Figure 5.10 The top-view images and cross-sectional profile measured by 3D confocal laser microscope for filled line patterns (various distances of the channel: **(a)** 0.5 µm, **(b)** 1.5 µm, **(c)** 3.0 µm) with Ag ink after the process of LDW and ink-jet printing. Note that the thicknesses of spin-coated photoresist are ~ 1.0 µm.

5.2.2 Self-align through negatively laser patterned geometry

Based on aforementioned conditions (5.0 μW of the laser power, 0.005 mm/s of scan speed, 3000 rpm of spin speed for forming around 1.5 μm thickness using SU-8 2002) in the **Section 5.1.1**, a wall or barrier is built as shown in **Figure 5.11**.

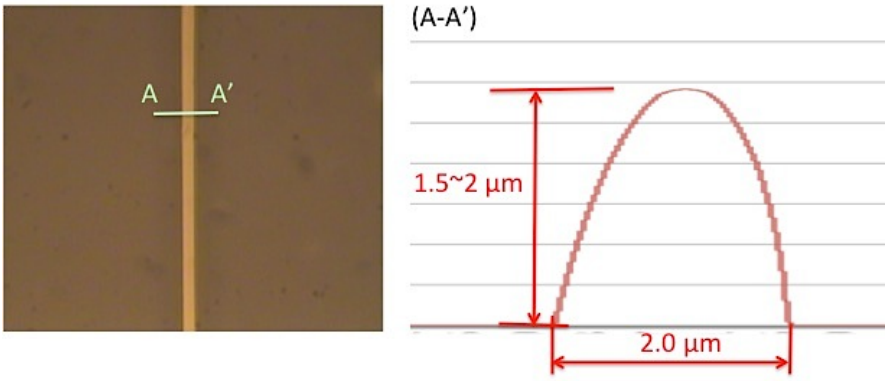

Figure 5.11 The top-view images and cross-sectional profile measured by 3D confocal laser microscope for the negatively patterned wall.

After building the wall, ink-jet printing using the Ag ink is performed over the wall in **Figure 5.12(a)**. Jetted Ag ink can be split into two parts because of high wall compared to the thickness of the printed ink and different surface energies between the wall and the ink. Also, the sintering process (at 180 °C for 30 min at a hot plate) helps the ink divide into two sections clearly because different thermal expansions can generate cracks at weak spots where a very thin ink is smeared due to the height of the wall and the surface energy (**Figure 5.12(b)**).

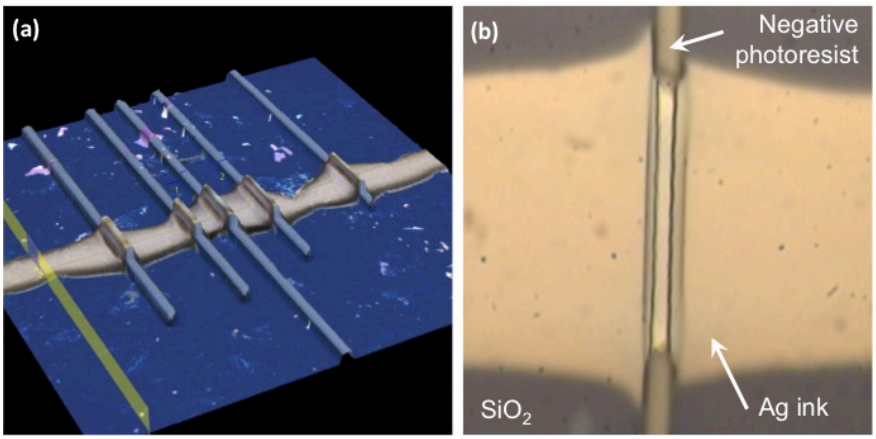

Figure 5.12 (a) 3D confocal laser microscope image and **(b)** magnified top-view image for the negatively patterned wall and printed Ag ink over the walls after the process of LDW and ink-jet printing of Ag ink.

5.3 MoS_2 Transistors

Through the laser-induced fine patterns (using the positive and negative photoresists) and ink-jet printing process, multilayered MoS_2 Transistors are fabricated. Moreover, the capillarity for the positive photoresist and self-alignment for the negative photoresist allow forming source and drain electrodes. **Figure 5.13(a)** and **5.13(b)** schematically explain the fabrication process for MoS_2 TFTs using the capillary and the self-alignment.

5.3.1 Device preparation

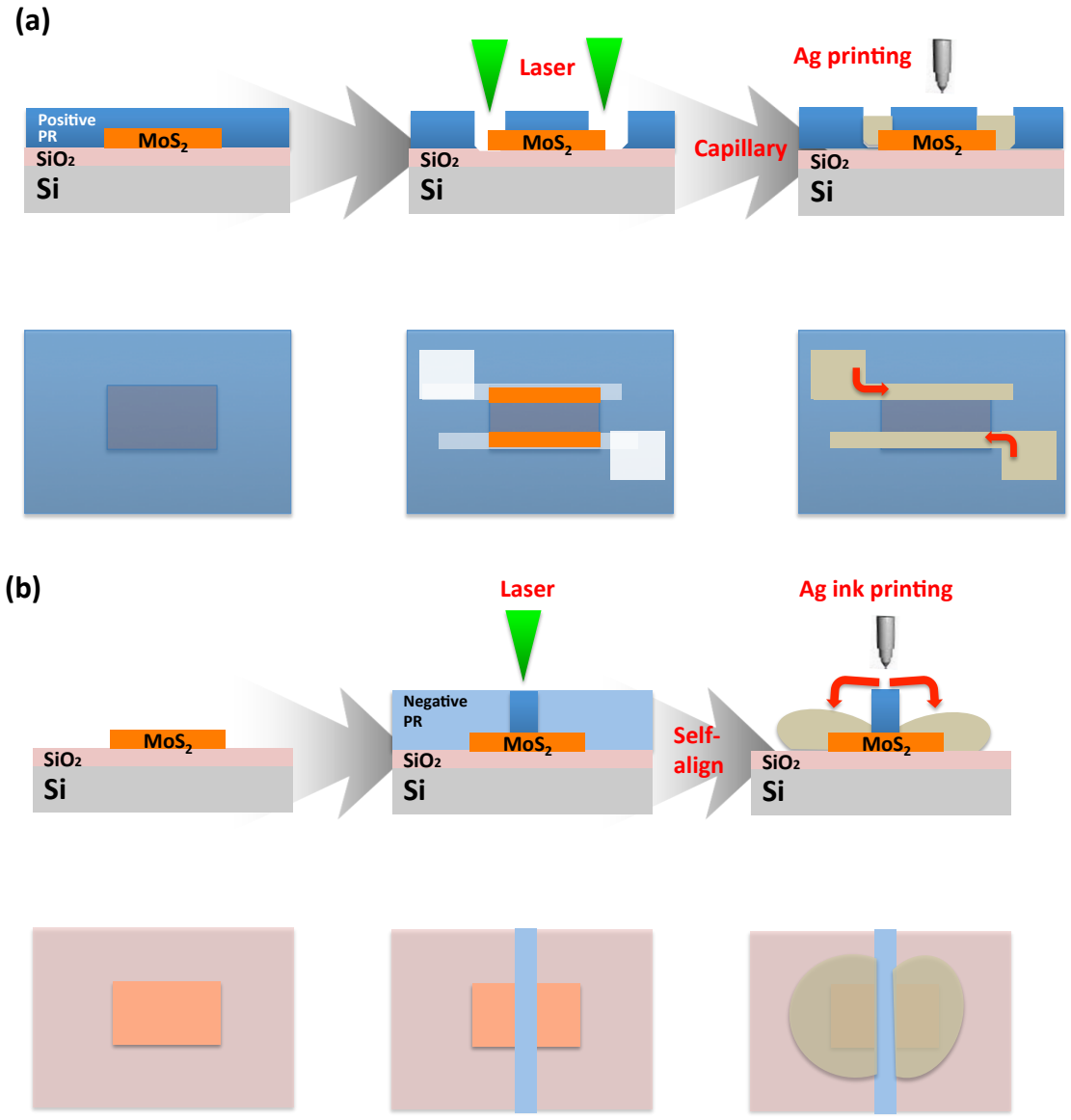

Figure 5.13 Schematic fabrication process for MoS_2 TFTs **(a)** using the positive photoresist and capillary and **(b)** using the negative photoresist and self-alignment with ink-jet printed Ag ink.

At the beginning, a 100-nm-thick SiO_2 was deposited CVD on a heavily doped *p*-type Si substrate (resistivity < 5×10^{-3} Ω·cm) as a gate dielectric layer. Then, MoS_2 flakes were mechanically transferred from bulk MoS_2 crystals (SPI Supplies, USA) on the deposited dielectric layer. After that, the positive (OiR-906-12, Fujifilm) or negative (SU-8 2002, MicroChem) photoresist was formed by spin coating process at 2000 rpm for the positive photoresist and at 3000 rpm for the negative photoresist. Note that the formed thicknesses of positive and negative photoresist were ~1.0 μm and ~1.5 μm, respectively (see **Section 5.2.1** and **5.2.2** for detailed process condition). The LDW lithography allowed creating concave patterns (positive) as the channels and convex patterns (negative) as the walls. The formed patterns played an important role in making the source/drain electrodes through capillarity and self-alignment. **Figure 5.14(a)** and **5.14(b)** show the completed MoS_2 TFTs using different types of photoresist and methods. After the ink-jet printing process, jetted Ag inks were sintered at 180 °C for 30 min at a hot plate for reducing the resistance and boosting electrical conductivity.

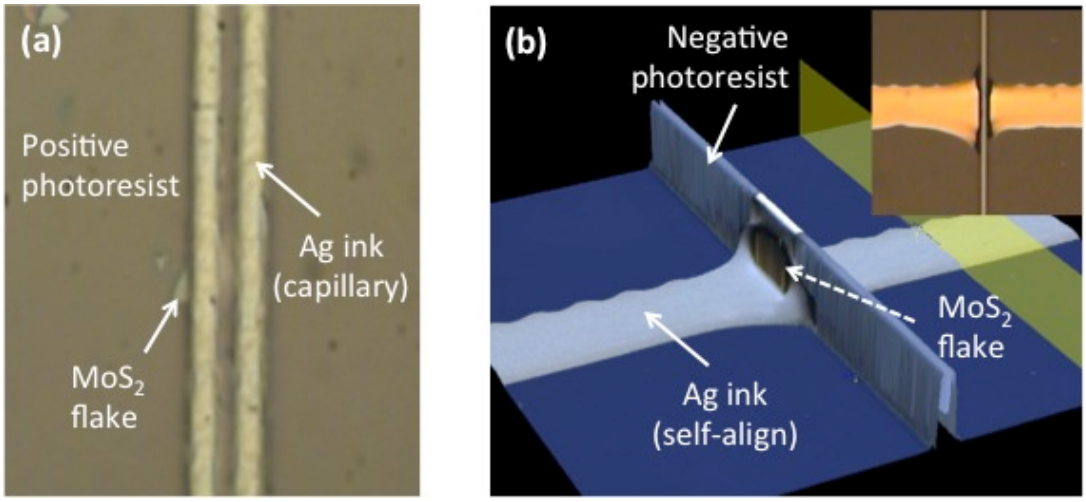

Figure 5.14 The optical images of fabricated MoS_2 TFTs **(a)** using the positive photoresist and capillary (Note that the representative device has a channel length of 2 μm and a width of 4 μm) and **(b)** using the negative photoresist and self-alignment with ink-jet printed Ag ink (Note that a channel length and a width are 2 μm and a width of 2 μm).

5.3.2 Electrical performance

The electrical characteristics of the devices fabricated by the positive photoresist with capillary and by the negative photoresist with self-alignment are examined.

Figure 5.15(a) and **5.15(b)** show the log- (left) and the linear-scale (right) I_D-V_G curves of representative MoS_2 TFT with the source/drain electrode formed by capillarity (V_D=0.1 V in **Figure 5.15(a)** and V_D=5.0 V in **Figure 5.15(b)**). The device has a channel length of 2 μm and a width of 4 μm. Note that the thickness of MoS_2 flake is around 55 nm.

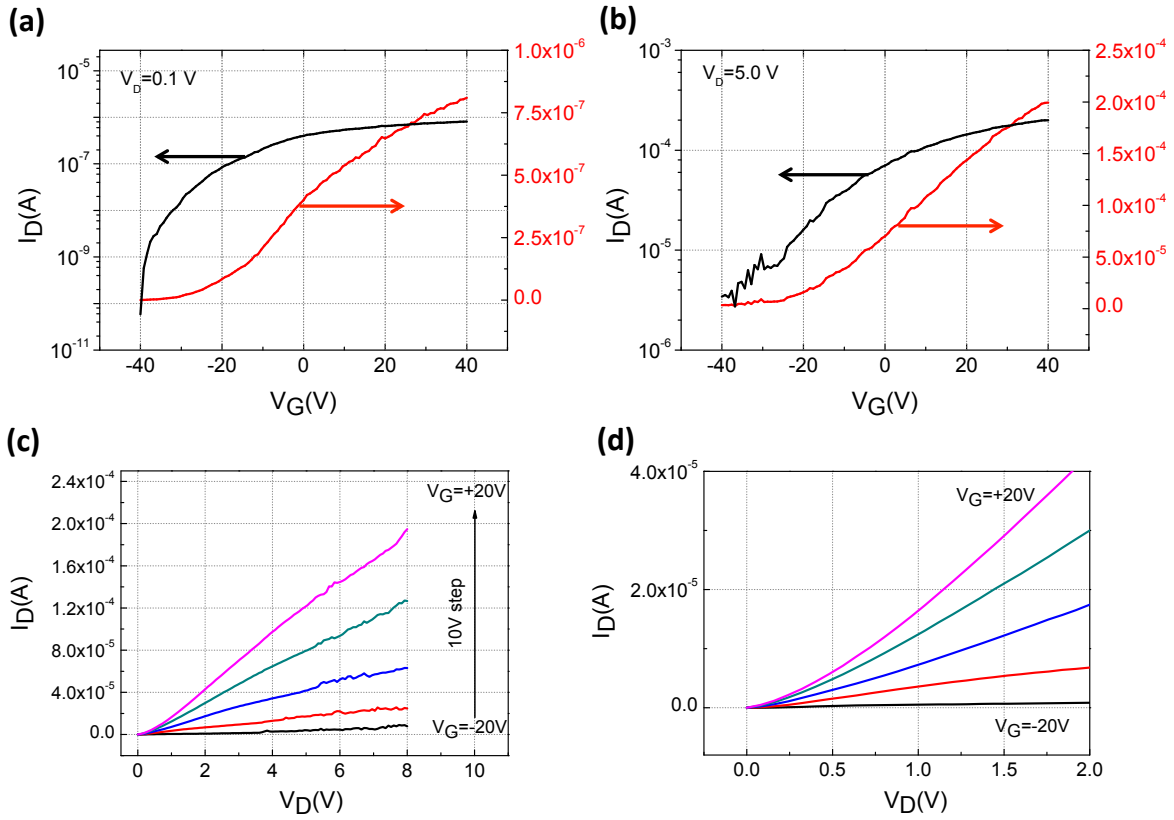

Figure 5.15 Device performance of MoS_2 TFTs with the Ag electrodes formed by capillary and positively patterned channels. **(a)** Transfer characteristics (I_D-V_G) for the representative MoS_2 transistor in log-scale (left) and linear-scale (right) at V_D = 0.1 V and **(b)** at V_D = 5.0 V. **(c)** Output characteristics (I_D-V_D) in the range of V_D from 0 V to 8 V with 10 V step of V_G (from -20 V to 20 V). **(d)** Magnifications for the low V_D range from 0 to 2.0 V.

At room temperature and in air, the as-fabricated MoS_2 TFT exhibited acceptable switching behavior (I_{on}/I_{off} of ~ 10^4), a SS of ~ 2.54 V/decade, μ_{eff_lin} of ~ 2.87 $cm^2V^{-1}s^{-1}$, and typical *n*-type behavior with negative V_{TH}, and a normally on-state for the device at low V_D (=0.1 V). At high V_D (=5.0 V), electrical performance changed: I_{on}/I_{off} of ~ 10^2, SS of ~ 7.0 V/decade, μ_{eff_sat} of ~ 11.75 $cm^2V^{-1}s^{-1}$. As shown in **Figure 5.15(c)** and **5.15(d)**, the I_D-V_D in a range from 0 to 8 V for the selected V_G (from -20 to +20 V in 10 V increments) was plotted. In this plot, a non-linear output curve in a very low V_D regime (from 0 to 2.0 V) was observed due to the Schottky barrier between the MoS_2 and ink-jet printed Ag electrodes.

Also, the MoS_2 TFTs with a channel length of 2 μm and a width of 2 μm are fabricated by self-alignment method. In **Figure 5.16**, the electrical performance of representative device exhibits similar characteristics to the above-mentioned transistor. At low V_D (=0.1 V), I_{on}/I_{off} of ~10^3 and a SS of ~3.72 V/decade were obtained and μ_{eff_lin} of ~10.18 $cm^2V^{-1}s^{-1}$ was extracted by the MOSFET square-law model (**Figure 5.16(a)**). This value (~10.18 $cm^2V^{-1}s^{-1}$) is much higher than the previous device (~ 2.87 $cm^2V^{-1}s^{-1}$) with the electrodes formed by capillarity because the self-aligned Ag electrodes have much wider width (~50 μm) than the width of the electrodes created by capillarity (~2 μm); the self-aligned Ag electrodes have

large injecting area (more than 10 times). Moreover, at high V_D (=5.0 V), I_{on}/I_{off} (~10^3) slightly increased and μ_{eff_sat} (~24.97 $cm^2V^{-1}s^{-1}$) was evaluated from a linear fitting of the curve of $I_D^{0.5}$ versus V_G (**Figure 5.16(b)**). Furthermore, from the I_D-V_D in Figure 5.16(c) and 5.16 (d), non-linear output characteristics were shown like the previous device. However, unlike the previous device, this device did not exhibit the square-law behavior from the intermediate regime. The self-heating effect can help understand and explain partially this phenomenon.[63] Here, I note that another similar trend was already observed in the **Section 2.4**.

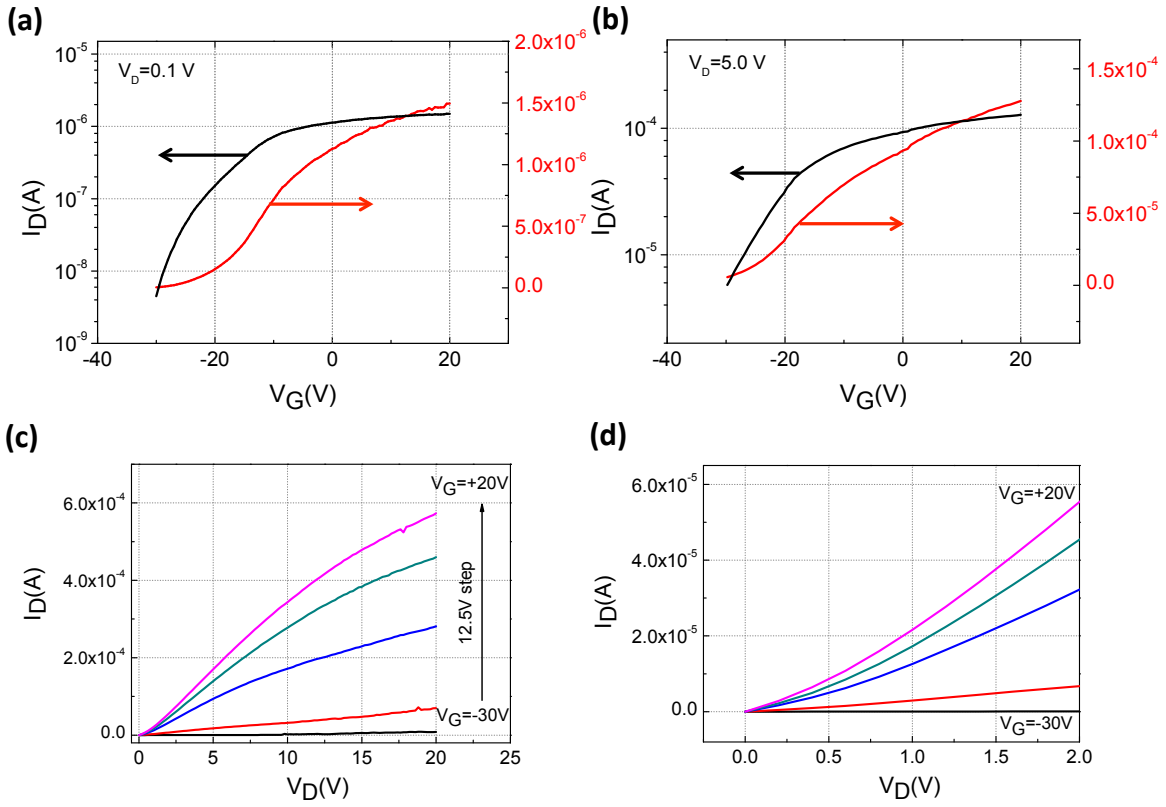

Figure 5.16 Device performance of MoS_2 TFTs with the Ag electrodes formed by self-alignment and negatively patterned walls. **(a)** Transfer characteristics (I_D-V_G) for the representative MoS_2 transistor in log-scale (left) and linear-scale (right) at V_D = 0.1 V and **(b)** at V_D = 5.0 V. **(c)** Output characteristics (I_D-V_D) in the range of V_D from 0 V to 20 V with 12.5 V step of V_G (from -30 V to 20 V). **(d)** Magnifications for the low V_D range from 0 to 2.0 V.

Commonly, extracted parameters of both devices, especially for the μ_{eff}, are relatively lower than previous MoS_2 TFTs having well-treated electrodes and contacts. One of the possibilities of changing the electrical behavior is the Φ_B or large R_c. The plots in **Figure 5.15(d)** and **5.16(d)** confirm that the Φ_B is formed at the contact between the ink-jetted Ag electrodes (as a metal) and the MoS_2 flakes (as a semiconductor). Furthermore, the solution-based ink could make unintended interfacial layer at the contact, such as an atomic vacuum gap, fully uncapped particles, or undissolved materials. For these reasons, the MoS_2 TFTs with ink-jet printed Ag electrodes exhibited relatively low electrical performance by comparison with previous MoS_2 TFTs. However, this does not mean that the printing process

is useless and unnecessary. Despite shortcomings, the printing process is still drawing particular attention because of potentially low cost, compatibility with flexible substrates, and ability to deposit unique features. Moreover, the performance of printing process has improved steadily with the development of printable materials.

5.4 Summary

In this chapter, laser-induced fine patterns were built using the positive or negative photoresists. Depending on the type of the photoresist, concave channels (positive) or convex walls (negative) were created. The formed patterns played an important role in making and defining the source/drain electrodes while solution-based Ag inks were printed over the patterns. Also, the capillary force helped fill the concave channel and the self-alignment allowed making two (source/drain) electrodes at a time.

Through laser-assisted fine patterns and ink-jet printing process, MoS_2 TFTs were fabricated. And as-fabricated devices exhibited tolerable electrical performances in the linear and the saturation regime. However, because of the particle features of the printed Ag ink, the formed electrodes had relatively high electrical resistance and low conductivity compared to its own bulk material. Nonetheless, it is enough to show the possibility and the potential for the combination of the direct laser lithography and the printing process. Moreover, the research into this subject is ongoing and developing incessantly. Therefore, I expect that these technologies may have a marked impact on the future of flexible/wearable electronics as the indispensable processes.

Chapter 6

Laser Welded 2D-like Random Networks for Robust Flexible MoS_2 Transistors

6.1 2D-like Random Networks of AgNWs

A large number of groups have attempted to find alternative conductive films as new flexible electrodes superior to ITO that has brittle ceramic properties and requires expensive vacuum deposition process. Therefore, several other candidates have been studied and introduced: highly conductive PEDOT:PSS,[168-170] metal grids,[171] graphene,[172-175] CNT,[176,177] nanotube–polymer composites,[178-180] and AgNW meshes.[181-185]

Among the suggested materials, 2D-like random networks of AgNWs are attracting a lot of attention because of the compatibility for cost-effective solution processible mass production and their good electrical conductivity; silver is 50 or 100 times more conductive than ITO. This difference in conductivity allows the material to cover only a few percent of the surface to achieve equivalent electrical properties. This fact can create improving transparency and cost efficiency as well. Comparing material costs, the price of indium (primary component of ITO: > 90% typically) and silver over the past 5 years has been roughly equivalent. Thus, the 50 or 100 times reduction due to the higher electrical conductivity of silver directly translates into a similar reduction in material cost relative to ITO sputtering targets. For these reasons, Cambrios Technologies provided the first high-volume commercially available wet-processed transparent conductive films.

6.2 Laser Welding on 2D-like Random Networks

2D-like random networks of AgNWs (Seashell Technologies) having average length of 35 μm and average diameter of 40 nm are made. Supplied AgNWs were dispersed by the polar groups in isopropyl alcohol (IPA), carrier fluid, without any surfactant coatings, such as polyvinylpyrrolidone. Note that silver concentration measured by thermo gravimetric analysis was around 5.3 mg/mL.

To create a flexible conductive layer, vacuum filtration method was employed because it can minimize the agglomeration of nanowires by using very small quantities of nanowires (25 μL) and deposit them uniformly onto the PI substrate. Filtrated AgNWs were interconnected like a net or mesh (circle shape with 40 mm diameter). To enhance the electrical property, laser beam with 532 nm wavelength (Solo I Nd:YAG, New Wave) was subsequently irradiated onto the film.

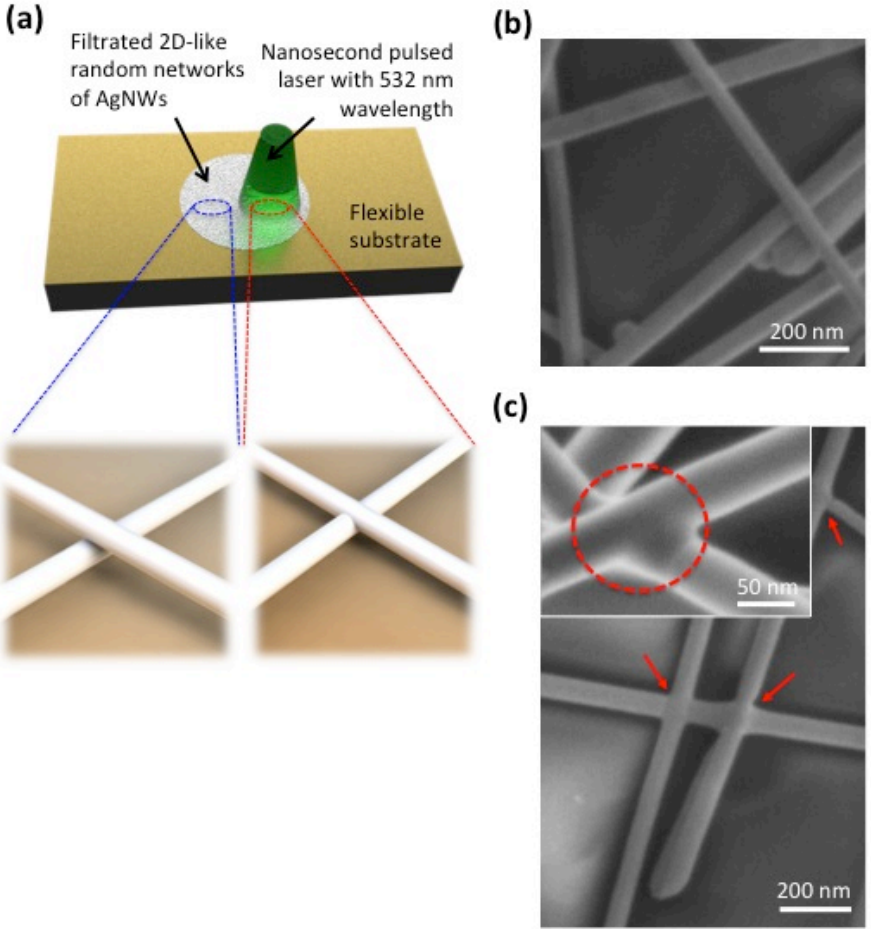

Figure 6.1 (a) The schematic concept of laser welding process for metal AgNW network on the PI substrate formed by filtration method. **(b)** SEM image of as-prepared AgNW random networks before the laser welding process and **(c)** after the laser treatment (red arrows indicate the laser welded junctions). Note that at magnified image (inset), laser welded part is observed in evidence.

Figure 6.1(a) illustrates the schematic concept of the laser welding process for the 2D-like random networks of AgNWs. In this research, as-prepared 2D-like AgNWs networks showed unfavorable electrical sheet resistance, 480 ~ 550 Ω/□, due to weak physical contact between nanowires (in **the left-bottom inset of Figure 6.1(a)**). Here, I note that even though different sheet resistance can be produced by tuning the nanowire diameter, length, and surface coverage of nanowires,[186-188] I applied laser process under ambient condition to enhance the electrical properties of the interconnected wires (in **the right-bottom inset of Figure 6.1(a)**), without controlling the dimension or the number density of AgNWs.

After the laser welding process, the sheet resistance was drastically reduced by 10 ~ 15 Ω/□; these values were almost 37 or 55-fold lower than for the as-prepared samples. To confirm this finding, I took SEM images before and after laser irradiation as shown in **Figure 6.1(b)** and **6.1(c)**. The results clearly indicate that the laser process induced fusion (red circles) at the NW junctions (**Figure 6.1(c)**) in contrast tp the as-prepared NW junctions (**Figure 6.1(b)**). The features of laser welding process for creating the interconnected mesh are well described by considering the plasmonic effect at AgNW junctions that form a naturally small air gap. The concentrated photon source induces localized heat spreads into the NWs due to their high thermal conductivity.[189,190] The small gaps at the NW junctions enable selective and effective focusing of light and heating (hot enough to melt the NWs) at the contact. I could find evidence of the locally generated plasmonic effect generated in the small gap configuration from the morphological changes of the NWs. As shown in the inset of **Figure 6.1(c)**, after the laser illumination, the morphology of only the NW junction substantially changed; NWs slightly melted and joined via welding. On the other hand, the morphology of NWs away from the junction did not change unlike in the junction proximity. If the thermal distribution were uniform on the NWs, morphological changes would be observed over their entire lengths. Therefore, this laser welding process was different from conventional, uniformly distributed thermal heating. The locally generated plasmonic effect can also prevent damage to low thermal budget plastic substrates.

6.3 Robust Flexible MoS_2 Transistors on the Solution Based PI Substrate with Laser Welded 2D-like Random Network Electrodes

The carrier substrate was used for incorporating the flexible device into a conventional TFT fabrication procedure, including photolithography, metallization, lift-off/etching and post-thermal treatment. A thin layer of poly(vinyl alcohol) (PVA) coated on the carrier substrate is adopted as a sacrificial layer, which not only provides simple and facile detaching process by dissolving the PVA layer in water, but also enables large-scale integration.[191]

Moreover, in comparison with the another detachment technique based on excimer laser treatment, which requires highly expensive apparatus as well as generates potential damages to

devices originated from burnt residue, no harm is induced during the PVA-based procedure and guarantees the success of fabrication. PI layer is one of the best suitable materials among the flexible substrate candidates, such as polymethyl methacrylate (PMMA), PEN and PET, because of its fascinating physical properties, especially decomposition temperature of 600 °C.[192,193] The ability to endure high temperature enables flexible devices to undergo thermal post-processing (e.g. annealing, welding). In contrast, devices built with aforementioned materials are inappropriate because their melting point are lower than the process temperature.[37,43,53] In addition, the tensile strength of PI is 350 MPa with elongation up to 100% of its original length, making it an appropriate flexible substrate.[194]

6.3.1 Device preparation

Figure 6.2(a)-(c) shows a schematic illustration of the fabricating procedure and perspective structure of our flexible multilayer MoS_2 TFTs array.

0.1 g of PVA (MW~6000 99+% hydrolyzed, Sigma Aldrich) was dissolved in 10 mL of deionized water (DI Water). The PVA aqueous solution was spin-coated on a Si/SiO_2 carrier substrate at 2000 rpm for 30 s, and annealed at 110 °C for 90 s. For a flexible substrate, PI solution was spin-coated on the Si/SiO_2/PVA substrate at 3000 rpm for 30 s and baked at 90 °C for ~5 min. Then, Si/SiO_2/PVA/PI substrate was thermally solidified in ramp oven at 350 °C for 30 min (**Figure 6.2(a)**).

2D-like random AgNW networks as the bottom gate electrode was transferred by filtration method and plasmonic laser welding process was performed (see **Section 6.2**). The organic material (SU-8 2000.5, MicroChem) was used as a gate insulator (GI), instead of the conventional oxide-based counterparts, in order to increase the flexibility of MoS_2 TFTs. The organic GI was formed by spin-coating SU-8 2000.5 onto the gate electrode, followed by baking at 110 °C for 10 min and 130 °C for 1 min, respectively. Then, a 20-nm-thick amorphous Al_2O_3 was deposited by ALD (Lucida D100) with trimethylaluminum as a Al precursor and H_2O as an oxygen precursor, respectively. The high-k Al_2O_3 could exhibit remarkable insulating capability with high capacitance as well as also compensate poor adhesion between hydrophobic organic surface and metal electrodes / multilayer MoS_2 active layer. Mechanically exfoliated multilayer MoS_2 flakes were transferred onto the Al_2O_3 layer. After e-beam evaporation of Ti/Au (20/50 nm) layers, source and drain electrodes were fabricated by using conventional photolithography and etching techniques as shown in **Figure 6.2(b)**.

Finally, for the separation of the flexible MoS_2 TFTs fabricated onto the PI substrate from the carrier substrate, PVA sacrificial layer was dissolved in DI water at room temperature for 30 min, schematically shown in **Figure 6.2(c)**. **Figure 6.2(d)** shows a photograph of the bent MoS_2 TFTs array on the flexible PI substrate, which was successfully fabricated by above procedures and multilayer MoS_2 flake placed between electrodes was clearly identified in **the inset of Figure 6.2(d)**. Transparent PET film with a thickness of 100 μm, as a protective as well as supportive layer for the flexible MoS_2 TFTs, was laminated beneath the PI layer with the aid of acrylate resin based pressure sensitive adhesive.

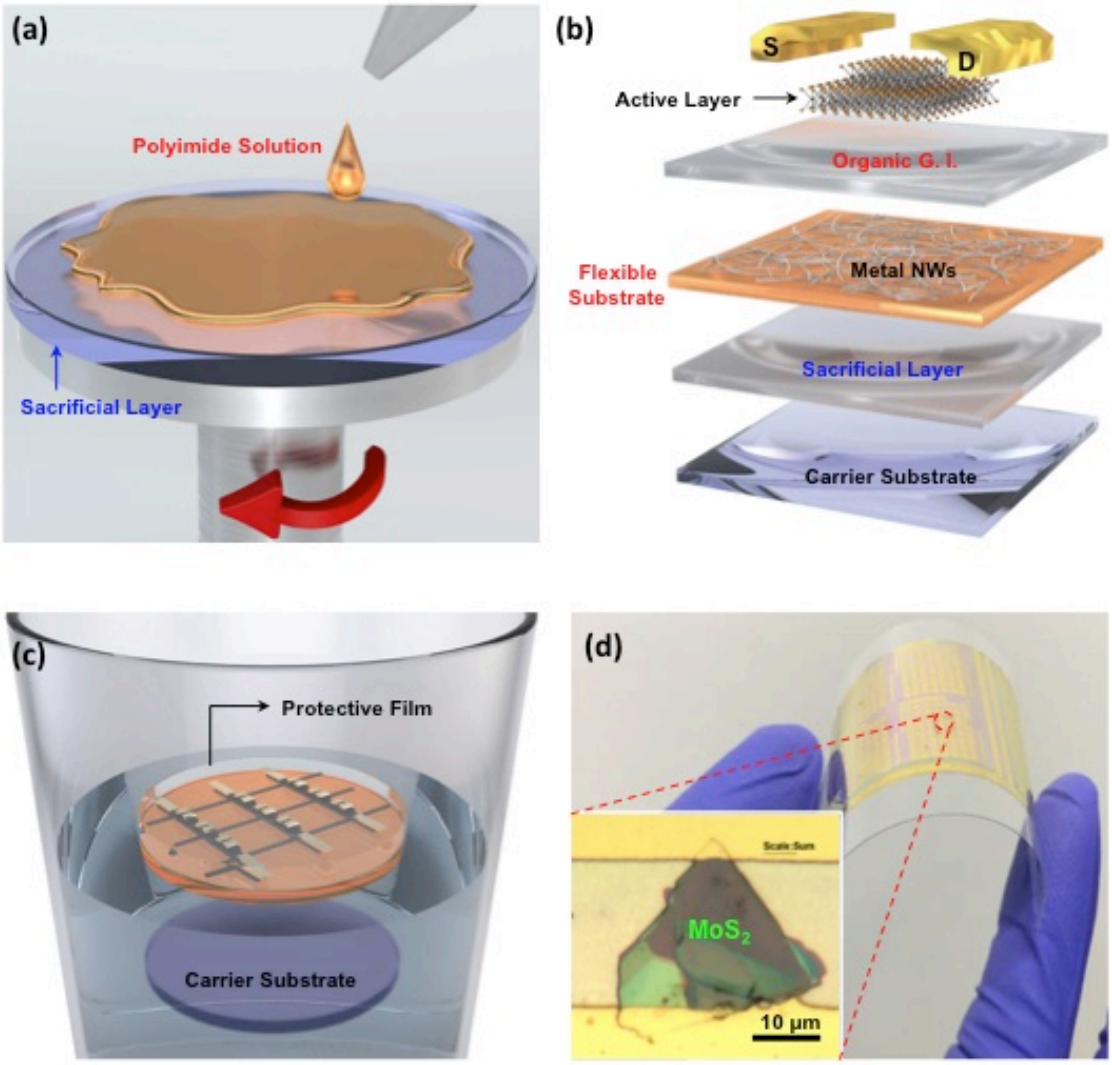

Figure 6.2 Flexible multilayer MoS_2 TFTs. **(a)** Schematic illustration of fabricating flexible substrate from PI solution. **(b)** Flow chart of the fabrication procedure including sacrificial layer, flexible substrate, and organic gate insulator. **(c)** Schematic illustration of detaching flexible TFTs from carrier substrate. **(d)** Photograph of bent flexible MoS_2 TFTs array. PET protective film was laminated under the PI flexible substrate. (Inset) Optical microscope image of multilayer MoS_2 active channel in single TFT.

6.3.2 Electrical performance

Figure 6.3 presents the current-voltage characteristics of the as-detached MoS_2 TFT on the PI substrate under the initial flat (*i.e.*, not bent) condition. The thicknesses of multilayer MoS_2 and double-layered GI are estimated to be 95 nm and 620 nm, respectively. As shown in the I_D–V_G characteristic curve of **Figure 6.3(a)**, our flexible MoS_2 TFT exhibits a typical *n*-type behavior,[64,195] and relatively high current I_{on}/I_{off} more than 5×10^5. It should be noted that GI with double-layered structure composed of organic SU-8 and ALD Al_2O_3 provides outstanding barrier properties, which could attribute the high performance of our devices. A

maximum value of μ_{eff} reaches up to 141.3 $cm^2\ V^{-1}s^{-1}$ in linear region (V_D = 1 V), which was calculated from $\mu_{eff} = Lg_m / WC_{GI}V_D$, where L and W are channel length (22.59 μm) and width (5.33 μm), g_m is expressed by ($g_m = \frac{\partial I_{ds}}{\partial V_{gs}}|_{V_{ds}=1\ V}$), and C_{GI} is total capacitance of double-layered GI, respectively. The multilayer MoS_2 TFTs fabricated by using the double-layered GI show much higher mobility than those of only ALD Al_2O_3 used as GI.[37,43,53] Fuhrer *et al.*, reported analogous results by comparing MoS_2 TFTs on PMMA as GI with those on SiO_2.[196] The about one order of magnitude higher mobility of MoS_2 TFT on PMMA was attributed to the long-range dielectric screening effect,[143] which was well agreed with our results. Output (I_D–V_D) characteristic curves of the same device are presented in **Figure 6.3(b)**. Ohmic contacts between the active layer and source/drain electrodes were established, as seen in the linear behavior at low V_D regime. Also, the robust current saturation due to the pinch-off environments at high V_D regime indicates good performances of our flexible MoS_2 TFT.

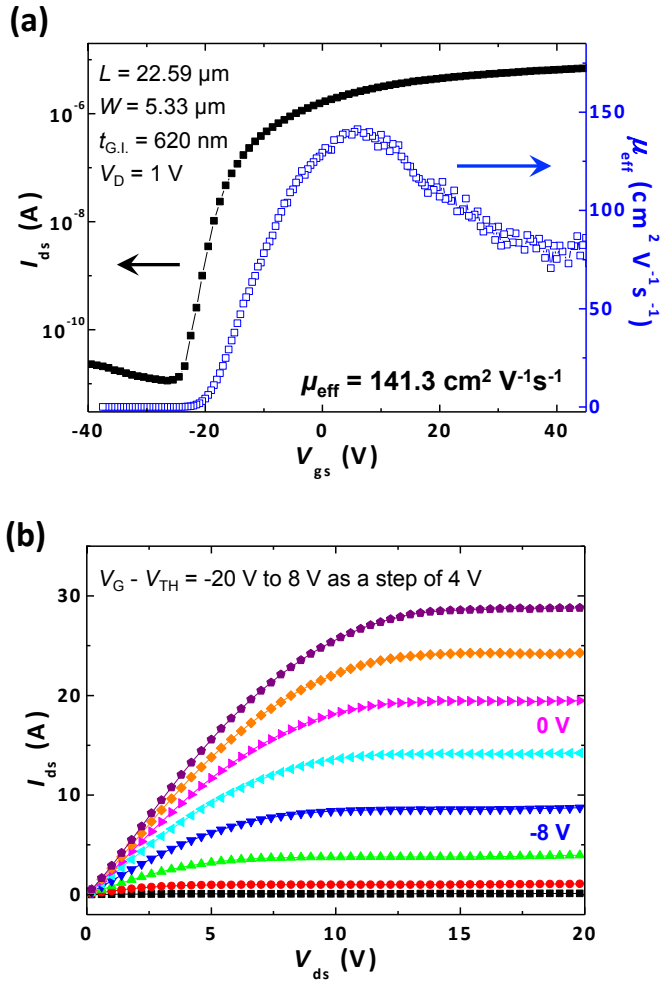

Figure 6.3 Electrical properties of flexible MoS_2 TFT at initial flat condition. **(a)** I_D–V_G curve and μ_{eff} of the flexible MoS_2 TFT at V_D = 1 V. **(b)** I_D–V_D curve of the same TFT under different gate biases (V_G – V_{TH} = -20 V to 10 V as a step of 4 V).

6.3.3 Mechanical flexibility

a. Numerical simulation (hyperelastic nonlinear analysis)

To investigate the flexible sturcture, hyperelastic nonlinear stress analysis was performed through COMSOL Multiphysics. The mechanical behavior of hyperelastic materials (e.g. PI, PEN, PET, polymer, or rubber-like materials) is expressed in terms of strain energy potential. Furthermore, to predict the behavior of the hyperelastic materials, many different models, which dissimilarly define the strain energy function, have been suggested.[197] Therefore, we need to compare different hyperelastic models with real experimental data through the curve fitting.

Figure 6.4(a) shows measured stress (σ) - stretch (λ) curve of the specimen with the thickness (*t*) of 0.105 mm made from solution based PI and PET for the bending and cycling test corresponding measured values of stress representing force per unit area and engineering stretch representing relative elongation,

$$\lambda = \frac{(L_0+\Delta L)}{L_0} = 1 + \varepsilon \tag{6.1}$$

where ε is the engineering normal strain. From the experimental data, ultimate tensile stress of 46.6×10^6 N/m^2 was observed at the maximum elongation of 43%. Also, within the interested and moderate strain range (<10%), Mooney-Rivlin model was a good match for our experimental data as shown in the inset of **Figure 6.4(a)**. The two-parameter Mooney-Rivlin model assumes that the local strain energy density in an incompressible material is a simple function of local strain invariants. For uniaxial loading, the nominal stress-stretch behavior for the Mooney-Rivin model, is given by:

$$\sigma = \frac{F}{A_0} = 2(C_{10} + \frac{C_{01}}{\lambda})(\lambda - \frac{1}{\lambda^2}) \tag{6.2}$$

where A_0 is the cross-section area of the test specimen, L_0 is original length of the specimen. The two-parameters, C_{10} and C_{01}, are material parameters which are determined by fitting the model (**Equation (6.2)**) to the experimental data (blue dot in **the inset of Figure 6.4(a)**).

Through the model, I described a cross section of the flexible substrate that imitated the experimental specimen mounted on the mechanical bending tester as shown in **Figure 6.4(b)**. The computational result shows that the generated internal stress distribution of the deformed specimen; the outer surface is in tension and the inner surface is in compression based on the neutral plane where the material is not under stress (**Figure 6.4(b)**). When the bending radius (*r*) was 5 mm, generated maximum tensile stress at the outmost area (interface between AgNW networks and PI substrate) was 4.38×10^6 N/m^2 with the strain of 0.2 %.

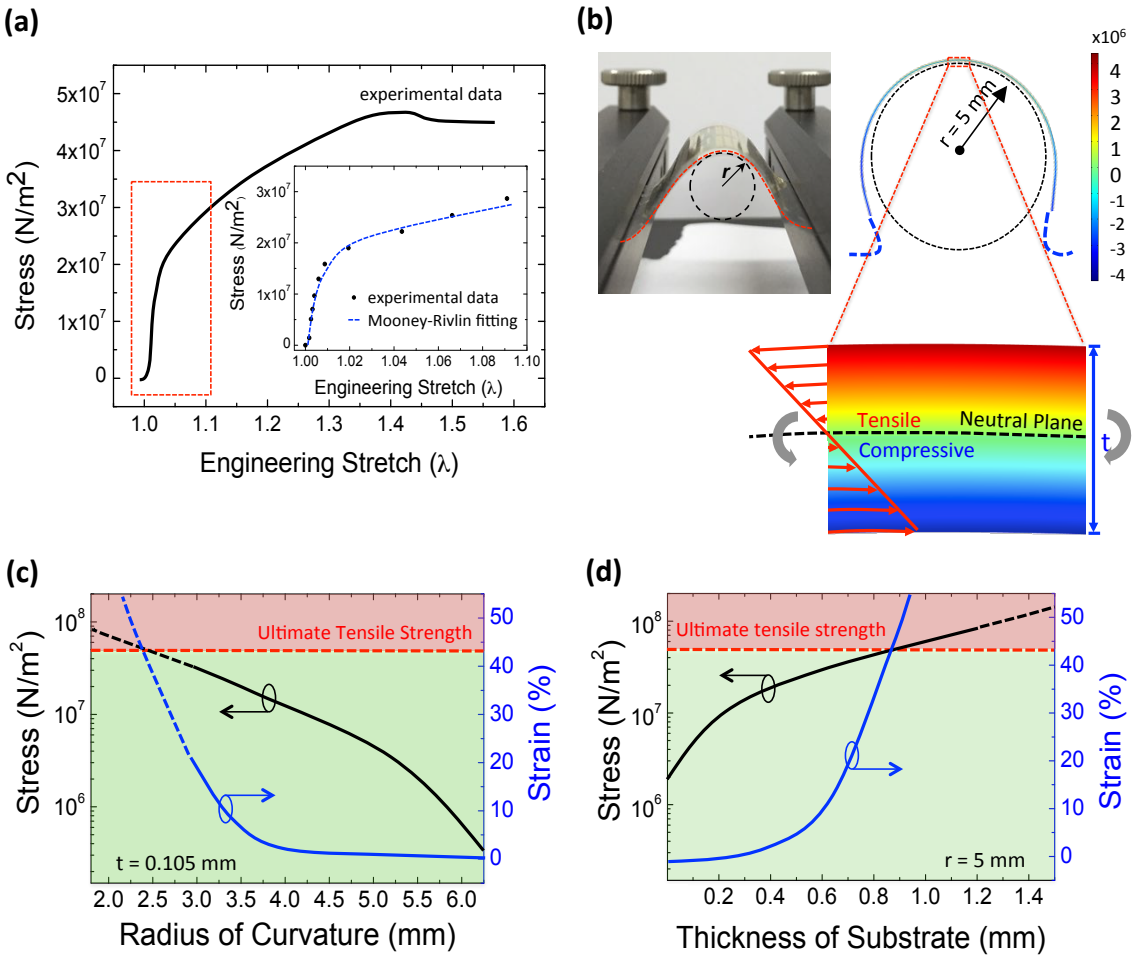

Figure 6.4 (a) Measured stress (σ) - stretch (λ) curve of the specimen of solution based PI and PET (t= 0.105 mm) and **(inset)** fitting Mooney-Rivlin model with experimental data. **(b)** The numerical result on hyperelastic nonlinear stress analysis based on the parameters extracted by the real experimental data when the bending radius was 5 mm. **(c)** Through fitted Mooney-Rivlin model, expected mechanically stable range (green region) of the structure with resect to the radius of curvature of the substrate and **(d)** to thickness of the substrate.

I note that the very thin substrate and its robust mechanical properties reduced the effective applied strains on the laser welded AgNW networks as well as MoS_2 film to values below 1 %. This suggests stability against bending. To understand their correlations in detail, we studied the bending radius-generated stress relation and the thickness-stress relation of the flexible structure.

As shown in **Figure 6.4(c)**, we can expect that the flexible structure could endure the generated stress at specific conditions (green region, $r > 2.5$ mm at $t = 0.105$ mm) where the stress is under the failure stress (46.6×10^6 N/m^2) and elongation (43 %). Note that the result of analysis based on the Mooney-Rivlin model could be not accurately guaranteed against relatively large strain range (marked with dotted lines). Also, when t increases over 0.8 mm (at $r = 5$ mm), the structure can be destroyed (**Figure 6.4(d)**). Hence, to remain in

mechanically stable state, the generated stress should be below the ultimate tensile strength (red region). I also consider thicknesses and mechanical properties of the additional indispensable layers and structures (e.g. dielectric, semiconductor, electrodes, etc.) for making functional devices. When ductile materials like metals, which have very low elastic region (only 0.2 or 0.3% strain), are used as electrodes or others, the structures become vulnerable to bending stress or force and more prudent design is needed. Therefore, laser welded AgNW networks can be a promising approach not only for flexible, but also even for stretchable electronics.

b. Mechanical bending tolerance test

For investigating solid tolerance of our flexible MoS_2 TFTs array against various mechanical stresses, two kinds of tensile stresses were applied to the flexible TFTs array parallel to their active channels, for examples, static and cyclic modes of upward bending, as shown in **the insets of Figure 6.5(a)** and **6.5(b)**, respectively.

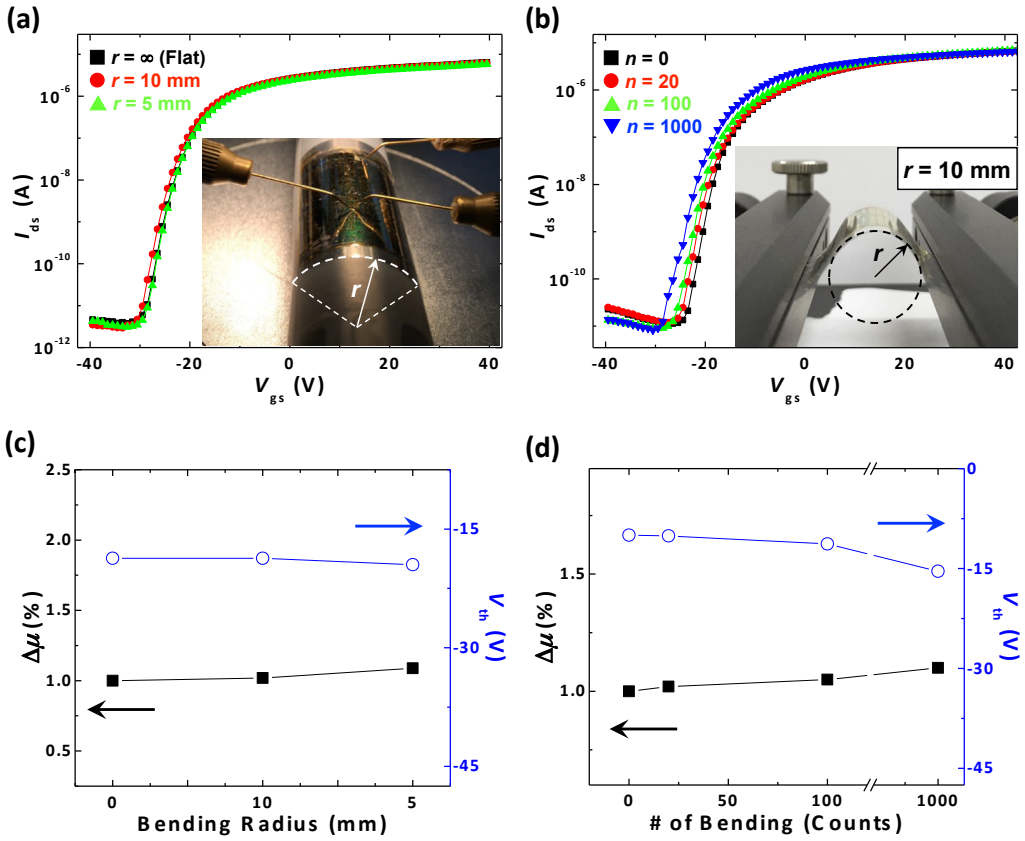

Figure 6.5 Variation of TFT performances of the flexible MoS_2 TFTs under various mechanical stresses. **(a)** Comparison of the transfer characteristics of the flexible MoS_2 TFTs under static bending environments with three different bending radii (flat, r = 10 mm, and 5 mm). **(Inset)** Photograph of the bent MoS_2 TFTs attached on rigid cylinder with pre-defined radius, which was depicted as white dashed arc and arrow. **(b)** Comparison of the transfer characteristics of the flexible MoS_2 TFTs under cyclic bending environments with respect to number of bending (n = 0, 20, 100, and 1000). **(Inset)** Photograph of the flexible MoS_2 TFTs loaded on multi-modal bending tester. Bending radius (r = 10 mm) was depicted as black dashed circle and arrow. Variations of μ_{eff} and V_{TH} of the flexible MoS_2 TFTs as a function of **(c)** static bending radii and **(d)** number of cyclic bending.

For static bending, the flexible MoS_2 TFTs array was attached onto the surface of rigid cylinders with pre-defined radii (r = 10 mm and 5 mm), and electrical properties were investigated under bending (**the inset of Figure 6.5(a)**). For cyclic bending, the number of bending as well as its radius was controlled by using a multi-modal bending tester (Covotech Co., Ltd), as shown in **the inset of Figure 6.5(b)**. Radii under the cyclic bending were determined through tangential contact of rigid cylinder with different dimensions, and the change of the electrical properties due to the cyclic bending was measured under re-flat condition.

It has been known that when an elastomeric slab is bent with arbitrary radius r, there exists a neutral mechanical plane (i.e. stress-free zone) in the geometric mid-plane.[198-200] Lamination of a 100-μm-thickness PET film beneath the PI substrate enables the down-shift of neutral mechanical plane in our flexible MoS_2 TFTs array, which could lie within tensile-stress zone. As a result, flexibility of our devices can be investigated under much harsher environment.

Figure 6.5(a) compares the I_D-V_G curves of the MoS_2 TFTs array under flat and statically bent conditions. The I_D-V_G curves of the MoS_2 TFT with bending radii of 10 and 5 mm did not change significantly with respect to that of flat condition. As shown in the **Figure 6.5(c)**, the variation of the mobilities ($\Delta\mu$ (%) = $|\mu_{bending} - \mu_{flat}| / \mu_{flat}$) due to bending with r = 10 and 5 mm were estimated to be 1.9% and 8.8%, respectively. The V_{TH} of the MoS_2 TFT under flat condition was -18.7 V. For a r of 10 mm, V_{TH} just remained its initial value, and was shifted negatively to -19.5 V with decreasing r down to 5 mm.

Figure 6.5(b) shows the comparison of the transfer characteristics of another MoS_2 TFTs array under the cyclic bending environments. As number of bending (n) increased, the entire I_D-V_G curves were slightly shifted toward negative V_G. However, the I_{on}/I_{off} almost maintained as same level of ~10^5. The $\Delta\mu$ (V_{TH}) due to the cyclic bending with n of 20, 100, and 1000 were 2% (-10.1 V), 5% (-11.3 V), and 10% (-15.4 V), respectively (**Figure 6.5(d)**). It should be noted that thin Al_2O_3 layer played an important role in our flexible TFTs array, which could enhance the adhesion between GI and S/D electrodes as well as active layer. The flexible MoS_2 TFTs array without Al_2O_3 layer just exhibited much poorer transistor performances at same bending conditions.

6.4 Summary

To realize highly mechanically robust flexible MoS_2 TFTs, laser welded 2D-like random AgNW networks (as a gate electrode), solution based-PI laminated PEN film (as a substrate), and the organic material (SU-8 2000.5) with atomic layered Al_2O_3 as a gate insulator were employed.

Laser welding process induced plasmonic effect across the small gaps of the AgNW junctions. Because of this effect, the NWs fused only at the junctions and the morphologies of other parts except the junction did not considerably change. SEM images before and after laser

irradiation supported this supposition. After the laser welding process, the sheet resistance significantly improved (from 480 ~ 550 Ω/□ to 10 ~ 15 Ω/□, almost 37 ~ 55-fold differences).

Also, the fabricated device with flexible dielectric layer combining organic and inorganic materials on the solution based PI exhibited fascinating electrical behavior as well as mechanical stability. Analysis by numerical computations on the bending stress and bending tests at the static and cycling conditions indicated that the MoS_2 transistors having the specific dielectric layer, the solution based PI substrate, and laser welded 2D-like random network electrodes were very robust and had large flexibility. Moreover, these results demonstrate the feasibility of plasmonic laser welding process with potentially important technical implications on fabricating robust flexible applications; the employed laser welding is a powerful approach to enhance the electrical and mechanical qualities of flexible electrodes.

Chapter 7

Conclusions

7.1 Concluding Remarks

Much progress has been made in flexible, stretchable electronics. Flexible and stretchable electronics represent a critical frontier in the transformation of rigid, tabletop micro/nano electronics into portable, wearable systems that can be integrated into a variety of emerging technologies from sensing and monitoring to human-inspired applications. Many conventional structures, materials, and processes are not compatible with flexible/stretchable device layouts. These requirements pose significant challenges that require a new, adaptive paradigm for the low-thermal budget (<100 °C) and functional components on a lightweight and inexpensive flexible platform. These advances are arguably most useful in displays, including televisions—the anticipated shift to flexible, stretchable displays can be considered an extension of the current trend toward miniaturization, in which CRT have been supplanted by FPDs—but it continues to expand into other applications. Currently, users require new and more advanced displays for mobile phones, portable devices, and even televisions. To meet future demands, the driving electronic circuitry of displays must have high performance, low power consumption, ultra-high resolution, high frame rate (high driving speed), and robust flexible platform. Therefore, developing flexible transistors with high μ_{eff} will be a key to satisfying these requirements, as increasing brightness and decreasing bus-line load power consumption.

In this regard, TFTs based on a 2D series of TMDs with a formula of MX_2 (M = Mo, W; X = S, Se, Te), had invested for in-depth understanding of various important aspect of flexible/wearable electronics over the several chapters as candidate materials and platform to extend Si technology.

In **Chapter 2**, the carrier transport and the impact of the operating ambient conditions on back-gated multilayer MoS_2 FETs with a thickness of ~50 nm were studied at their realistic working temperatures and under different ambient conditions (in air and in a vacuum of $\sim 10^{-5}$ Torr). Increases in temperature cause increases in I_{min} (likely due to thermionic emission at defects), and result in decreased I_{on} at high V_G (likely due to increased phonon scattering). Thus, the I_{on}/I_{min} ratio decreases as the temperature increases. Moreover, the ambient effects with working temperatures on μ_{eff} were investigated. The adsorbed oxygen and water created more defect sites or impurities in the MoS_2 channel, which can lead to additional scattering of the carriers. In air, the adsorbed molecules and phonon scattering caused a reduction of the μ_{eff}, significantly. These channel mobility drop-off rates in air and in a vacuum reached 0.12 cm^2/VsK and 0.07 cm^2/VsK, respectively; the rate of degradation is steeper in air than in vacuum due to boosted phonon mode by the adsorbed oxygen and water molecules.

Also, using LFN analysis, the qualities of the semiconductor, oxide, and oxide–semiconductor interface of back-gated multilayer MoS_2 transistors were examined. I also investigated the mechanism of the LFN and extracted γ exponents from the LFN behavior, $1/f^{\gamma}$; the value of γ was >1 at negative gate bias because of active slow traps. As V_G increased, the slow traps were filled and thus γ decreased, stabilizing at ≈0.95. Various other parameters extracted from the LFN indicated that the carrier number fluctuation (Δn) model was the dominant origin of the LFN. The multilayer MoS_2 structure had better noise immunity than a single-layer case in air.

In **Chapter 3**, selective annealing of source/drain electrodes in MoS_2 TFTs on mechanically flexible substrates by a picosecond laser achieved enhanced device performance without damaging the plastic substrates. An analysis of the temperature distribution, based on FDM, confirmed the compatibility of our picosecond laser annealing procedure with the flexible substrate as well as improvement in contact with the channel interface. Flexible MoS_2 TFTs with laser-annealed contacts are especially promising for use in low-power operation (low SS), high-speed devices (higher mobility), with amplification of self-gain (the fully saturated I_D). Analysis by FDM simulations, measurement of I–V characteristics, and TEM strongly suggest that the significant enhancement in performance metrics originates from a decrease in the Schottky barrier width between the Ti/Au metal and the semiconducting MoS_2. Moreover, to confirm the effects and to study in-depth, the extraction of contact-free mobility from the YFM were performed. First, extracted SS values decreased. Secondly, μ_0, and μ_{eff_lin} both increased. At the same time, the gap between R_c and R_{ch}, and μ_0 and μ_{eff_lin} was significantly reduced. These data indicate that the interface quality between the MoS_2 channel and insulator was improved. In addition, reduced contact barriers lead to a minimization in the resistance of major carrier injection and make it possible to approach the ideal μ_0 and μ_{eff_lin}.

On top of that, the picosecond laser annealing treatment was selectively applied onto the contact regions between MoS_2 and IZO source/drain electrodes of transparent (>81% of transmittance in visible wavelength range) multilayered MoS_2 TFTs. As a result, the electrical performances including μ_{eff}, I_{on}/I_{off}, SS, and R_c were boosted. These results demonstrate that picosecond laser annealing is an attractive technology for realizing high performance flexible and transparent MoS_2 TFTs in analog/digital integrated circuits.

In **Chapter 4**, the LDW lithography using a simple set-up for defining the patterns was introduced in order to avoid costly conventional photolithography system. The LDW system was non-vacuum and maskless process. Arbitrary patterns can be freely created by computer-controlled programs. Using the LDW with positive photoresist, the source/drain electrodes for MoS_2 TFTs were defined and formed on the randomly scattered MoS_2 flakes. Also, sol-gel processed high-k ZrO_2 (~ 22.0) dielectric layer helped boosting the electrical performance (e.g. μ_{eff}, SS) through suppressing Coulomb electron scattering and reducing the interface trap concentration.

In **Chapter 5**, for making fine patterns, different approach of the LDW and interference lithography based on AltPSM were demonstrate. The range of the size of created patterns was from 2.0 μm to 200 nm. The patterns formed by the LDW lithography process were used as channels or barriers depending on the type of the photoresist when MoS_2 TFTs were fabricated through ink-jet printing technique. To make the source/drain electrodes, Ag nanoparticle ink was printed over the patterns formed on top of the MoS_2 flakes. In case of using the positive photoresist, the concave patterns were produced and the channel-like patterns were filled with ink-jetted Ag nanoparticle ink by capillary force. However, in case of the negative photoresist, convex patterns were created on the middle of MoS_2 flakes and barrier-like patterns divided the printed Ag ink into two electrodes (source and drain) by self-alignment phenomena. The LDW lithography and inkjet printing technology were successfully applied for the MoS_2 TFTs, which exhibited quite moderate electrical performance. These results indicate that the technologies can have potential possibilities for applications in future flexible/wearable electronics and facilitate the cost-effective fabrication process.

Lastly in **Chapter 6**, laser welding on 2D-like AgNW random networks as a gate electrode, solution-based PI as a flexible substrate, and organic SU-8 as a dielectric layer were carried out to provide highly mechanically robust flexible structure and electrically high performance device. Laser induced a plasmonic and localized thermal effect at the junctions of AgNWs because the junction has very tiny nano-gaps, which enhance the optical field intensity. SEM images and electrical behavior (e.g. sheet resistance, electrical conductivity) supported the laser welding process was different from the normal heating process (blanket heating, over the entire specimen) and the locally generated plasmonic effect of the laser welding also can well match with the plastic substrates with low thermal budget. In addition, solution-based PI and organic SU-8 could enable building the structure and platform solidly. Through numerical computation based on the real experimental data (stress-stretch curve of the specimen, PI laminated on PEN film) and bending test at static and cyclic modes, significantly unchanged electrical performances of the geometry designed from the simulation were obtained and realized. Showing mechanical tolerances of the flexible structure composed of laser welded 2D-like AgNW random network, solution-based thin PI, and organic insulator suggest potential technical implications on fabricating highly flexible applications with a TFT platform.

Still, the flexible/wearable electronics and their technology stay stuck in the lab scale for many years. As a matter of fact, the present reality is high cost, low throughput, complex and difficult manufacturing, unstable performance (low reliability), and even an unclear market. However, the fact that TFT LCD replaced the bulky CRT platform and changed paradigm did not happen in such a distant past. Furthermore, the fact that much larger-sized LCDs and

AMOLED TV are commercially available today was certainly not anticipated in terms of price and technologies only a few years ago. Therefore, I strongly believe that we could see tremendous changes in the flexible/wearable electronics in the near future. Also, I hope that these tiny results derived from the research will contribute a little to change the paradigm.

7.2 Future Works

There are several key challenges that lie ahead before the transistors based on 2D layered semiconductors can be integrated into flexible/stretchable circuits. The key challenges include inaccessibility of large area growth/coverage of layered semiconductors, non-uniformity between devices, high contact resistance between metal electrodes and semiconductors, and the system integration with flexible substrates.

These challenges give rise to the several future works. Here I identify key technical focus works. Currently, as 2D materials beyond graphene, the TMD layered semiconductors are widely investigated for fabricating TFTs. The development of flexible 2D TMD TFTs with pulsed laser processes will allow us to overcome the technical limits of the for next generation display devices. In this dissertation, even though I have already made significant progress (**Chapter 3**), understanding in-depth of the fundamental mechanism on the pulsed laser annealing process is required to provide more clear evidence.

Controlled production of crystalline MoS_2 by laser is still challenging. Fundamental understanding, especially on morphological evolution by laser-induced crystallization is crucial for taking full advantage of this technology. Even though several methods for epitaxial deposition of crystalline semiconductors have been well established, there is still demand for heterogeneous integration on foreign materials that do not allow epitaxial growth. Nanosecond laser beam processing using either a large area excimer or a high repetition-scanning beam will be used to anneal the 2D TMDC films in order to improve crystallinity and properties. It is important to note that thermal isolation can be handled promptly since the thermal penetration corresponding to microsecond heating will be of micron order. A thin dielectric layer (e.g. SiO_2) can thus serve as an effective thermal barrier, preventing damage to the underlying substrate. The specimen geometrical configuration significantly affects the induced temperature field development. For instance, should the crystallizing area be too large, the heat diffusion cannot reach the boundary area and the crystallization process will produce polycrystalline grains. An important feature is the narrow neck through which the single crystal is fed to the pixel. This processing scheme may be adapted to the annealing of dichalcogenide thin films.

Furthermore, in **Chapter 4** and **Chapter 5**, the LDW lithography process was applied for the rigid platform even though the process has big benefits for the flexible platform. Therefore, the application of flexible devices and the system integration with flexible substrates will be necessary. Also, through interference patterns with the ink-jet printing process, wire grid polarizer (WGP) which fine patterns (nano-scale) are required can be possible application.

Other challenges to manufacturing flexible electronics are requirements imposed on the switching and driving circuitry with mechanical/electrical stability (robust, reliable, and flexible) on bending/folding substrate. Therefore, more mechanically robust structures are needed. In this respect, in **Chapter 6**, laser welded 2D-like random AgNW networks were developed as flexible electrodes. However, the uniformity was not acceptable because each junction or location has different conditions (e.g. the number of NWs, thickness, defects); the thickness or roughness of 2D-like random networks based on the NWs is quite uneven. To make and improve the uniformity of the networks, planarization process is required. The use of surface embedded NW networks is one of the approaches for the planarization. Through solution based PI and water soluble PVA, surface embedded NW networks will be formed. The laser welding process is expected to impart strong adhesion between NWs as well as between NW and substrate.

For further applications of flexible/wearable electronics, optoelectronic device applications (e.g transistors, photo-detectors, electroluminescent devices and sensors) will be considered because of the unique optical (e.g. direct band gap for monolayer) and electrical properties of 2D TMDC materials. Monolayer semiconducting TMDCs, which have direct band gaps in the visible range, large exciton binding energies, and strong photoluminescence, are promising for optoelectronic applications.

References

[1] S. Kim, H. J. Kwon, S. Lee, H. Shim, Y. Chun, W. Choi, J. Kwack, D. Han, M. Song, S. Kim, S. Mohammadi, I. Kee, and S. Y. Lee, "Low-Power Flexible Organic Light-Emitting Diode Display Device," *Advanced Materials,* vol. 23, no. 31, pp. 3511-3516, 2011.

[2] D. Kuang, J. Brillet, P. Chen, M. Takata, S. Uchida, H. Miura, K. Sumioka, S. M. Zakeeruddin, and M. Gratzel, "Application of highly ordered TiO2 nanotube arrays in flexible dye-sensitized solar cells," *ACS Nano,* vol. 2, no. 6, pp. 1113-1116, 2008.

[3] D. H. Kim, N. Lu, R. Ma, Y. S. Kim, R. H. Kim, S. Wang, J. Wu, S. M. Won, H. Tao, A. Islam, K. J. Yu, T. I. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H. J. Chung, H. Keum, M. McCormick, P. Liu, Y. W. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, and J. A. Rogers, "Epidermal electronics," *Science,* vol. 333, no. 6044, pp. 838-843, 2011.

[4] J. Viventi, D. H. Kim, J. D. Moss, Y. S. Kim, J. A. Blanco, N. Annetta, A. Hicks, J. L. Xiao, Y. G. Huang, D. J. Callans, J. A. Rogers, and B. Litt, "A Conformal, Bio-Interfaced Class of Silicon Electronics for Mapping Cardiac Electrophysiology," *Science Translational Medicine,* vol. 2, no. 24, 24ra22, 2010.

[5] R. Das, and P. Harrop, "Printed, Organic & Flexible Electronics Forecasts, Players & Opportunities," *IDTechEx Report*, 2013.

[6] K. R. Sarma, *Chaper 4 Amorphous Silicon: Flexible Backplane and Display Application*, New York: Springer, 2009.

[7] G. B. Raupp, N. Colaneri, S. M. O'Rourke, J. Kaminski, D. R. Allee, S. M. Venugopal, E. J. Bawolek, D. E. Loy, C. Moyer, S. K. Angeno, B. P. O'Brien, D. Bottesch, S. Rednour, R. Blanchard, M. Marrs, J. Dailey, and K. Long, "Flexible display technology in a pilot line manufacturing environment," in Army Science Conference, Orlando, FL, 2006.

[8] G. Raupp, "Active matrix TFT technology development and pilot line manufacturing for reflective and emissive flexible displays," in Proceeding of USDC Flexible Displays & Microelectronics Conference & Exhibit, Phoenix, AZ, 2007.

[9] K. R. Sarma, C. Chanley, S. Dodd, J. Roush, J. Schmidt, G. Srdanov, M. Stevenson, G. Yu, R. Wessel, J. Innocenzo, M. O'Regan, W. A. MacDonald, R. Eveson, K. Long, H. Gleskova, S. Wagner, and J. C. Sturm, "Flexible active matrix OLED using 150°C a-Si TFT backplane," in Proceedings of the SPIE, pp. 180–191, 2003.

[10] H. Gleskova, and S. Wagner, "DC-gate-bias stressing of a-Si : H TFTs fabricated at 150 degrees C on polyimide foil," *IEEE Transactions on Electron Devices,* vol. 48, no. 8, pp. 1667-1671, 2001.

[11] S. H. Won, J. H. Hur, C. Bin Lee, H. C. Nam, J. K. Chung, and J. Jang, "Hydrogenated amorphous silicon thin-film transistor on plastic with an organic gate insulator," *IEEE Electron Device Letters,* vol. 25, no. 3, pp. 132-134, 2004.

[12] P. M. Smith, P. G. Carey, and T. W. Sigmon, "Excimer laser crystallization and doping of silicon films on plastic substrates," *Applied Physics Letters,* vol. 70, no. 3, pp. 342-344, 1997.

[13] M. Wu, K. Pangal, J. C. Sturm, and S. Wagner, "High electron mobility polycrystalline silicon thin-film transistors on steel foil substrates," *Applied Physics Letters,* vol. 75, no. 15, pp. 2244-2246, 1999.
[14] R. S. Howell, M. Stewart, S. V. Karnik, S. K. Saha, and M. K. Hatalis, "Poly-Si thin-film transistors on steel substrates," *IEEE Electron Device Letters,* vol. 21, no. 2, pp. 70-72, 2000.
[15] R. L. Hoffman, B. J. Norris, and J. F. Wager, "ZnO-based transparent thin-film transistors," *Applied Physics Letters,* vol. 82, no. 5, pp. 733-735, 2003.
[16] C. H. Seager, D. C. McIntyre, W. L. Warren, and B. A. Tuttle, "Charge trapping and device behavior in ferroelectric memories," *Applied Physics Letters,* vol. 68, no. 19, pp. 2660-2662, 1996.
[17] M. W. J. Prins, K. O. GrosseHolz, G. Muller, J. F. M. Cillessen, J. B. Giesbers, R. P. Weening, and R. M. Wolf, "A ferroelectric transparent thin-film transistor," *Applied Physics Letters,* vol. 68, no. 25, pp. 3650-3652, 1996.
[18] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, no. 7016, pp. 488-492, 2004.
[19] C. D. Dimitrakopoulos, and P. R. L. Malenfant, "Organic thin film transistors for large area electronics," *Advanced Materials,* vol. 14, no. 2, pp. 99-117, 2002.
[20] J. H. Schon, C. Kloc, and B. Batlogg, "On the intrinsic limits of pentacene field-effect transistors," *Organic Electronics,* vol. 1, no. 1, pp. 57-64, 2000.
[21] Y. Diao, B. C. Tee, G. Giri, J. Xu, H. Kim do, H. A. Becerril, R. M. Stoltenberg, T. H. Lee, G. Xue, S. C. Mannsfeld, and Z. Bao, "Solution coating of large-area organic semiconductor thin films with aligned single-crystalline domains," *Nature Materials,* vol. 12, no. 7, pp. 665-671, 2013.
[22] Y. Yuan, G. Giri, A. L. Ayzner, A. P. Zoombelt, S. C. Mannsfeld, J. Chen, D. Nordlund, M. F. Toney, J. Huang, and Z. Bao, "Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method," *Nature Communications,* vol. 5, 3005, 2014.
[23] S. H. Hur, O. O. Park, and J. A. Rogers, "Extreme bendability of single-walled carbon nanotube networks transferred from high-temperature growth substrates to plastic and their use in thin-film transistors," *Applied Physics Letters,* vol. 86, no. 24, 243502, 2005.
[24] E. Artukovic, M. Kaempgen, D. S. Hecht, S. Roth, and G. GrUner, "Transparent and flexible carbon nanotube transistors," *Nano Letters,* vol. 5, no. 4, pp. 757-760, 2005.
[25] T. Takenobu, T. Takahashi, T. Kanbara, K. Tsukagoshi, Y. Aoyagi, and Y. Iwasa, "High-performance transparent flexible transistors using carbon nanotube films," *Applied Physics Letters,* vol. 88, no. 3, 033511, 2006.
[26] X. F. Duan, C. M. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldman, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature,* vol. 425, no. 6955, pp. 274-278, 2003.
[27] F. Schwierz, "Graphene transistors," *Nature Nanotechnology,* vol. 5, no. 7, pp. 487-496, 2010.
[28] S. M. Eaton, H. B. Zhang, and P. R. Herman, "Heat accumulation effects in femtosecond laser-written waveguides with variable repetition rate," *Optics Express,* vol. 13, no. 12, pp. 4708-4716, 2005.

[29] N. Misra, L. Xu, Y. L. Pan, N. Cheung, and C. P. Grigoropoulos, "Excimer laser annealing of silicon nanowires," *Applied Physics Letters,* vol. 90, no. 11, 111111, 2007.

[30] D. Lee, H. Pan, S. H. Ko, H. K. Park, E. Kim, and C. P. Grigoropoulos, "Non-vacuum, single-step conductive transparent ZnO patterning by ultra-short pulsed laser annealing of solution-deposited nanoparticles," *Applied Physics a-Materials Science & Processing,* vol. 107, no. 1, pp. 161-171, 2012.

[31] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nature Nanotechnology,* vol. 7, no. 11, pp. 699-712, 2012.

[32] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science,* vol. 306, no. 5696, pp. 666-669, 2004.

[33] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature,* vol. 438, no. 7065, pp. 197-200, 2005.

[34] C. Berger, Z. M. Song, T. B. Li, X. B. Li, A. Y. Ogbazghi, R. Feng, Z. T. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics," *Journal of Physical Chemistry B,* vol. 108, no. 52, pp. 19912-19916, 2004.

[35] X. L. Li, X. R. Wang, L. Zhang, S. W. Lee, and H. J. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science,* vol. 319, no. 5867, pp. 1229-1232, 2008.

[36] L. Y. Jiao, L. Zhang, X. R. Wang, G. Diankov, and H. J. Dai, "Narrow graphene nanoribbons from carbon nanotubes," *Nature,* vol. 458, no. 7240, pp. 877-880, 2009.

[37] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnology,* vol. 6, no. 3, pp. 147-50, 2011.

[38] A. Kuc, N. Zibouche, and T. Heine, "Influence of quantum confinement on the electronic structure of the transition metal sulfide TS_2," *Physical Review B,* vol. 83, no. 24, 245213, 2011.

[39] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically Thin MoS_2: A New Direct-Gap Semiconductor," *Physical Review Letters,* vol. 105, no. 13, 136805, 2010.

[40] A. Splendiani, L. Sun, Y. B. Zhang, T. S. Li, J. Kim, C. Y. Chim, G. Galli, and F. Wang, "Emerging Photoluminescence in Monolayer MoS_2," *Nano Letters,* vol. 10, no. 4, pp. 1271-1275, 2010.

[41] P. Johari, and V. B. Shenoy, "Tuning the Electronic Properties of Semiconducting Transition Metal Dichalcogenides by Applying Mechanical Strains," *ACS Nano,* vol. 6, no. 6, pp. 5449-5456, 2012.

[42] R. Fivaz, and E. Mooser, "Mobility of Charge Carriers in Semiconducting Layer Structures," *Physical Review,* vol. 163, no. 3, pp. 743-755, 1967.

[43] S. Kim, A. Konar, W. S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J. B. Yoo, J. Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, and K. Kim, "High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals," *Nature Communications,* vol. 3, 1011, 2012.

[44] D. Xiao, G. B. Liu, W. X. Feng, X. D. Xu, and W. Yao, "Coupled Spin and Valley Physics in Monolayers of MoS_2 and Other Group-VI Dichalcogenides," *Physical Review Letters,* vol. 108, no. 19, 196802, 2012.

[45] W. X. Feng, Y. G. Yao, W. G. Zhu, J. J. Zhou, W. Yao, and D. Xiao, "Intrinsic spin Hall effect in monolayers of group-VI dichalcogenides: A first-principles study," *Physical Review B,* vol. 86, no. 16, 165108, 2012.

[46] H. L. Zeng, J. F. Dai, W. Yao, D. Xiao, and X. D. Cui, "Valley polarization in MoS_2 monolayers by optical pumping," *Nature Nanotechnology,* vol. 7, no. 8, pp. 490-493, 2012.

[47] C. Ataca, M. Topsakal, E. Akturk, and S. Ciraci, "A Comparative Study of Lattice Dynamics of Three- and Two-Dimensional MoS_2," *Journal of Physical Chemistry C,* vol. 115, no. 33, pp. 16354-16361, 2011.

[48] H. L. Zeng, B. R. Zhu, K. Liu, J. H. Fan, X. D. Cui, and Q. M. Zhang, "Low-frequency Raman modes and electronic excitations in atomically thin MoS_2 films," *Physical Review B,* vol. 86, no. 24, 241301, 2012.

[49] H. Pan, and Y. W. Zhang, "Edge-dependent structural, electronic and magnetic properties of MoS_2 nanoribbons," *Journal of Materials Chemistry,* vol. 22, no. 15, pp. 7280-7290, 2012.

[50] Y. F. Li, Z. Zhou, S. B. Zhang, and Z. F. Chen, "MoS2 Nanoribbons: High Stability and Unusual Electronic and Magnetic Properties," *Journal of the American Chemical Society,* vol. 130, no. 49, pp. 16739-16744, 2008.

[51] B. Radisavljevic, M. B. Whitwick, and A. Kis, "Integrated Circuits and Logic Operations Based on Single-Layer MoS_2," *ACS Nano,* vol. 5, no. 12, pp. 9934-9938, 2011.

[52] H. Li, Z. Y. Yin, Q. Y. He, H. Li, X. Huang, G. Lu, D. W. H. Fam, A. I. Y. Tok, Q. Zhang, and H. Zhang, "Fabrication of Single- and Multilayer MoS_2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature," *Small,* vol. 8, no. 1, pp. 63-67, 2012.

[53] W. Choi, M. Y. Cho, A. Konar, J. H. Lee, G. B. Cha, S. C. Hong, S. Kim, J. Kim, D. Jena, J. Joo, and S. Kim, "High-Detectivity Multilayer MoS_2 Phototransistors with Spectral Response from Ultraviolet to Infrared," *Advanced Materials,* vol. 24, no. 43, pp. 5832-5836, 2012.

[54] J. Lee, P. Dak, Y. Lee, H. Park, W. Choi, M. A. Alam, and S. Kim, "Two-dimensional Layered MoS_2 Biosensors Enable Highly Sensitive Detection of Biomolecules," *Scientific Reports,* vol. 4, 7352, 2014.

[55] E. W. K. Koh, C. H. Chiu, Y. K. Lim, Y. W. Zhang, and H. Pan, "Hydrogen adsorption on and diffusion through MoS_2 monolayer: First-principles study," *International Journal of Hydrogen Energy,* vol. 37, no. 19, pp. 14323-14328, 2012.

[56] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, and M. C. Hersam, "Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides," *ACS Nano,* vol. 8, no. 2, pp. 1102-1120, 2014.

[57] W. Park, J. Park, J. Jang, H. Lee, H. Jeong, K. Cho, S. Hong, and T. Lee, "Oxygen environmental and passivation effects on molybdenum disulfide field effect transistors," *Nanotechnology,* vol. 24, no. 9, 095202, 2013.

[58] L. Kou, A. Du, C. Chen, and T. Frauenheim, "Strain engineering of selective chemical adsorption on monolayer MoS_2," *Nanoscale,* vol. 6, no. 10, pp. 5156-5161, 2014.

[59] H. Qiu, L. J. Pan, Z. N. Yao, J. J. Li, Y. Shi, and X. R. Wang, "Electrical characterization of back-gated bi-layer MoS_2 field-effect transistors and the effect of ambient on their performances," *Applied Physics Letters,* vol. 100, no. 12, 123104, 2012.

[60] H. Liu, A. T. Neal, and P. D. D. Ye, "Channel Length Scaling of MoS_2 MOSFETs," *ACS Nano,* vol. 6, no. 10, pp. 8563-8569, 2012.
[61] B. Radisavljevic, and A. Kis, "Mobility engineering and a metal–insulator transition in monolayer MoS_2," *Nature materials,* vol. 12, no. 9, pp. 815-820, 2013.
[62] H. J. Kwon, J. Jang, S. Kim, V. Subramanian, and C. P. Grigoropoulos, "Electrical characteristics of multilayer MoS_2 transistors at real operating temperatures with different ambient conditions," *Applied Physics Letters,* vol. 105, no. 15, 152105, 2014.
[63] J. T. Lin, K. D. Huang, and C. L. Wu, "An Alleviated Self-Heating Poly-Si Thin-Film Transistor Built on Noncontinuing Buried Insulator," *Electrochemical and Solid-State Letters,* vol. 10, no. 3, pp. H107-H110, 2007.
[64] S. Das, H. Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High performance multilayer MoS_2 transistors with scandium contacts," *Nano Letters,* vol. 13, no. 1, pp. 100-105, 2013.
[65] Y. Xu, T. Minari, K. Tsukagoshi, J. A. Chroboczek, and G. Ghibaudo, "Direct evaluation of low-field mobility and access resistance in pentacene field-effect transistors," *Journal of Applied Physics,* vol. 107, no. 11, 114507, 2010.
[66] G. Ghibaudo, "New Method for the Extraction of MOSFET Parameters," *Electronics Letters,* vol. 24, no. 9, pp. 543-545, 1988.
[67] H. Y. Chang, W. N. Zhu, and D. Akinwande, "On the mobility and contact resistance evaluation for transistors based on MoS_2 or two-dimensional semiconducting atomic crystals," *Applied Physics Letters,* vol. 104, no. 11, 113504, 2014.
[68] S. J. Park, D. Y. Jeon, L. Montes, S. Barraud, G. T. Kim, and G. Ghibaudo, "Sidewall mobility and series resistance in a multichannel tri-gate MOSFET," *Semiconductor Science and Technology,* vol. 28, no. 6, 065009, 2013.
[69] A. D. Franklin, and Z. Chen, "Length scaling of carbon nanotube transistors," *Nat Nanotechnol,* vol. 5, no. 12, pp. 858-862, 2010.
[70] W. F. Yang, S. J. Lee, G. C. Liang, R. Eswar, Z. Q. Sun, and D. L. Kwong, "Temperature Dependence of Carrier Transport of a Silicon Nanowire Schottky-Barrier Field-Effect Transistor," *IEEE Transactions on Nanotechnology,* vol. 7, no. 6, pp. 728-732, 2008.
[71] K. Kaasbjerg, K. S. Thygesen, and K. W. Jacobsen, "Phonon-limited mobility in *n*-type single-layer MoS_2 from first principles," *Physical Review B,* vol. 85, no. 11, 115317, 2012.
[72] E. J. Tan, K. L. Pey, N. Singh, G. Q. Lo, D. Z. Chi, Y. K. Chin, L. J. Tang, P. S. Lee, and C. K. F. Ho, "Nickel-silicided Schottky junction CMOS transistors with gate-all-around nanowire channels," *IEEE Electron Device Letters,* vol. 29, no. 8, pp. 902-905, 2008.
[73] A. Rolland, J. Richard, J. P. Kleider, and D. Mencaraglia, "Electrical-Properties of Amorphous-Silicon Transistors and Mis-Devices - Comparative-Study of Top Nitride and Bottom Nitride Configurations," *Journal of the Electrochemical Society,* vol. 140, no. 12, pp. 3679-3683, 1993.
[74] K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T. Y. Kim, W. K. Hong, S. Hong, and T. Lee, "Electric Stress-Induced Threshold Voltage Instability of Multilayer MoS_2 Field Effect Transistors," *ACS Nano,* vol. 7, no. 9, pp. 7751-7758, 2013.
[75] D. S. Jeon, and D. E. Burk, "Mosfet Electron Inversion Layer Mobilities - a Physically Based Semi-Empirical Model for a Wide Temperature-Range," *IEEE Transactions on Electron Devices,* vol. 36, no. 8, pp. 1456-1463, 1989.

[76] Z. Y. Fan, D. W. Wang, P. C. Chang, W. Y. Tseng, and J. G. Lu, "ZnO nanowire field-effect transistor and oxygen sensing property," *Applied Physics Letters,* vol. 85, no. 24, pp. 5923-5925, 2004.

[77] C. Kayis, J. H. Leach, C. Y. Zhu, M. Wu, X. Li, U. Ozgur, H. Morkoc, X. Yang, V. Misra, and P. H. Handel, "Low-Frequency Noise Measurements of AlGaN/GaN Metal-Oxide-Semiconductor Heterostructure Field-Effect Transistors With HfAlO Gate Dielectric," *IEEE Electron Device Letters,* vol. 31, no. 9, pp. 1041-1043, 2010.

[78] A. Bid, A. Bora, and A. K. Raychaudhuri, "Observation of large low-frequency resistance fluctuations in metallic nanowires: Implications on its stability," *Physical Review B,* vol. 72, no. 11, 113415, 2005.

[79] C. Kurdak, J. Kim, A. Kuo, J. J. Lucido, L. A. Farina, X. Bai, M. P. Rowe, and A. J. Matzger, "1/f noise in gold nanoparticle chemosensors," *Applied Physics Letters,* vol. 86, no. 7, 073506, 2005.

[80] S. Y. Ju, P. C. Chen, C. W. Zhou, Y. G. Ha, A. Facchetti, T. J. Marks, S. K. Kim, S. Mohammadi, and D. B. Janes, "1/f noise of SnO_2 nanowire transistors," *Applied Physics Letters,* vol. 92, no. 24, 243120, 2008.

[81] M. Ishigami, J. H. Chen, E. D. Williams, D. Tobias, Y. F. Chen, and M. S. Fuhrer, "Hooge's constant for carbon nanotube field effect transistors," *Applied Physics Letters,* vol. 88, no. 20, 203116, 2006.

[82] G. X. Liu, S. Rumyantsev, M. S. Shur, and A. A. Balandin, "Origin of 1/f noise in graphene multilayers: Surface vs. volume," *Applied Physics Letters,* vol. 102, no. 9, 093111, 2013.

[83] V. K. Sangwan, H. N. Arnold, D. Jariwala, T. J. Marks, L. J. Lauhon, and M. C. Hersam, "Low-Frequency Electronic Noise in Single-Layer MoS_2 Transistors," *Nano Letters,* vol. 13, no. 9, pp. 4351-4355, 2013.

[84] H. J. Kwon, H. Kang, J. Jang, S. Kim, and C. P. Grigoropoulos, "Analysis of flicker noise in two-dimensional multilayer MoS_2 transistors," *Applied Physics Letters,* vol. 104, no. 8, 083110, 2014.

[85] H. K. Kang, L. Jagannathan, and V. Subramanian, "Measurement, analysis, and modeling of 1/f noise in pentacene thin film transistors," *Applied Physics Letters,* vol. 99, no. 6, 062106, 2011.

[86] N. V. D'yakonova, M. E. Levinshtein, and S. L. Rumyantsev, "Naure of the bulk 1/f noise in GaAs and Si" *AIP Conference Proceeding,* vol. 285, pp. 593-598, 1993.

[87] C. A. Dimitriadis, J. Brini, G. Kamarinos, and G. Ghibaudo, "Characterization of low-pressure chemical vapor deposited polycrystalline silicon thin-film transistors by low-frequency noise measurements," *Japanese Journal of Applid Physics,* vol. 37, no. 1, pp. 72-77, 1998.

[88] M. J. Uren, D. J. Day, and M. J. Kirton, "1/F and Random Telegraph Noise in Silicon Metal-Oxide-Semiconductor Field-Effect Transistors," *Applied Physics Letters,* vol. 47, no. 11, pp. 1195-1197, 1985.

[89] A. P. van der Wel, E. A. M. Klumperink, L. K. J. Vandamme, and B. Nauta, "Modeling random telegraph noise under switched bias conditions using cyclostationary RTS noise," *IEEE Transactions on Electron Devices,* vol. 50, no. 5, pp. 1378-1384, 2003.

[90] K. K. Hung, P. K. Ko, C. M. Hu, and Y. C. Cheng, "Random Telegraph Noise of Deep-Submicrometer MOSFETs," *IEEE Electron Device Letters,* vol. 11, no. 2, pp. 90-92, 1990.

[91] Z. M. Shi, J. P. Mieville, and M. Dutoit, "Random Telegraph Signals in Deep-Submicron N-MOSFETs," *IEEE Transactions on Electron Devices,* vol. 41, no. 7, pp. 1161-1168, 1994.
[92] L. K. J. Vandamme, X. S. Li, and D. Rigaud, "1/F Noise in Mos Devices, Mobility or Number Fluctuations," *IEEE Transactions on Electron Devices,* vol. 41, no. 11, pp. 1936-1945, 1994.
[93] G. Ghibaudo, "Analytical Modeling of the Mos-Transistor," *Physica Status Solidi a-Applied Research,* vol. 113, no. 1, pp. 223-240, 1989.
[94] G. Ghibaudo, O. Roux, C. Nguyenduc, F. Balestra, and J. Brini, "Improved Analysis of Low-Frequency Noise in Field-Effect Mos-Transistors," *Physica Status Solidi a-Applied Research,* vol. 124, no. 2, pp. 571-581, 1991.
[95] K. K. Hung, P. K. Ko, C. M. Hu, and Y. C. Cheng, "A Unified Model for the Flicker Noise in Metal Oxide-Semiconductor Field-Effect Transistors," *IEEE Transactions on Electron Devices,* vol. 37, no. 3, pp. 654-665, 1990.
[96] Y. Yoon, K. Ganapathi, and S. Salahuddin, "How Good Can Monolayer MoS_2 Transistors Be?," *Nano Letters,* vol. 11, no. 9, pp. 3768-3773, 2011.
[97] I. Popov, G. Seifert, and D. Tomanek, "Designing Electrical Contacts to MoS_2 Monolayers: A Computational Study," *Physical Review Letters,* vol. 108, no. 15, 156802, 2012.
[98] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-Performance Single Layered WSe_2 p-FETs with Chemically Doped Contacts," *Nano Letters,* vol. 12, no. 7, pp. 3788-3792, 2012.
[99] A. E. Bell, "Review and Analysis of Laser Annealing," *RCA Review,* vol. 40, no. 3, pp. 295-338, 1979.
[100] P. Baeri, S. U. Campisano, G. Foti, and E. Rimini, "Melting Model for Pulsing-Laser Annealing of Implanted Semiconductors," *Journal of Applied Physics,* vol. 50, no. 2, pp. 788-797, 1979.
[101] R. F. Wood, and G. E. Giles, "Macroscopic Theory of Pulsed-Laser Annealing .1. Thermal Transport and Melting," *Physical Review B,* vol. 23, no. 6, pp. 2923-2942, 1981.
[102] H. Kwon, W. Choi, D. Lee, Y. Lee, J. Kwon, B. Yoo, C. P. Grigoropoulos, and S. Kim, "Selective and localized laser annealing effect for high-performance flexible multilayer MoS_2 thin-film transistors," *Nano Research,* vol. 7, no. 8, pp. 1137-1145, 2014.
[103] H. J. Kwon, S. Kim, J. Jang, and C. P. Grigoropoulos, "Evaluation of pulsed laser annealing for flexible multilayer MoS_2 transistors," *Applied Physics Letters,* vol. 106, no. 11, 113111, 2015.
[104] M. Bonn, D. N. Denzler, S. Funk, M. Wolf, S. S. Wellershoff, and J. Hohlfeld, "Ultrafast electron dynamics at metal surfaces: Competition between electron-phonon coupling and hot-electron transport," *Physical Review B,* vol. 61, no. 2, pp. 1101-1105, 2000.
[105] B. Luther-Davies, A. V. Rode, N. R. Madsen, and E. G. Gamaly, "Picosecond high-repetition-rate pulsed laser ablation of dielectrics: the effect of energy accumulation between pulses," *Optical Engineering,* vol. 44, no. 5, 051102, 2005.
[106] A. Chimmalgi, C. P. Grigoropoulos, and K. Komvopoulos, "Surface nanostructuring by nano-/femtosecond laser-assisted scanning force microscopy," *Journal of Applied Physics,* vol. 97, no. 10, 104319, 2005.
[107] S. I. Anisimov, and B. Rethfeld, "On the theory of ultrashort laser pulse interaction with a metal," *Proceedings of SPIE,* vol. 3093, pp. 192-203, 1997.

[108] J. Y. Kim, S. M. Choi, W. S. Seo, and W. S. Cho, "Thermal and Electronic Properties of Exfoliated Metal Chalcogenides," *Bulletin of the Korean Chemical Society,* vol. 31, no. 11, pp. 3225-3227, 2010.
[109] F. Leonard, and A. A. Talin, "Electrical contacts to one- and two-dimensional nanomaterials," *Nature Nanotechnology,* vol. 6, no. 12, pp. 773-783, 2011.
[110] M. Gadenne, V. Podolskiy, P. Gadenne, P. Sheng, and V. M. Shalaev, "Plasmon-enhanced absorption by optical phonons in metal-dielectric composites," *Europhysics Letters,* vol. 53, no. 3, pp. 364-370, 2001.
[111] M. Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, and E. D. Williams, "Atomic structure of graphene on SiO_2," *Nano Letters,* vol. 7, no. 6, pp. 1643-1648, 2007.
[112] D. K. Schroder, *Semiconductor material and device characterization*, 3rd ed., Piscataway, NJ: Wiley, 2006.
[113] W. S. Hwang, M. Remskar, R. S. Yan, T. Kosel, J. K. Park, B. J. Cho, W. Haensch, H. L. Xing, A. Seabaugh, and D. Jena, "Comparative study of chemically synthesized and exfoliated multilayer MoS_2 field-effect transistors," *Applied Physics Letters,* vol. 102, no. 4, 043116, 2013.
[114] H. Y. Chang, S. Yang, J. Lee, L. Tao, W. S. Hwang, D. Jena, N. Lu, and D. Akinwande, "High-Performance, Highly Bendable MoS_2 Transistors with High-K Dielectrics for Flexible Low-Power Systems," *ACS Nano*, vol. 7, no. 6, pp. 5446-5452, 2013.
[115] J. Pu, Y. Yomogida, K. K. Liu, L. J. Li, Y. Iwasa, and T. Takenobu, "Highly Flexible MoS_2 Thin-Film Transistors with Ion Gel Dielectrics," *Nano Letters,* vol. 12, no. 8, pp. 4013-4017, 2012.
[116] J. Yoon, W. Park, G. Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W. K. Hong, B. H. Lee, and H. C. Ko, "Highly flexible and transparent multilayer MoS_2 transistors with graphene electrodes," *Small,* vol. 9, no. 19, pp. 3295-300, 2013.
[117] S. M. Sze, *Physics of semiconductor devices*, 2nd ed., New York: Wiley, 1981.
[118] D. G. Teer, "New solid lubricant coatings," *Wear,* vol. 251, pp. 1068-1074, 2001.
[119] M. Kitada, N. Shimizu, and T. Shimotsu, "Amorphous Phase Formation in Ti/Ni Bilayer Thin-Films by Solid-State Diffusion," *Journal of Materials Science Letters,* vol. 8, no. 12, pp. 1393-1394, 1989.
[120] J. H. Kang, D. Sarkar, W. Liu, D. Jena, and K. Banerjee, "A Computational Study of Metal-Contacts to Beyond-Graphene 2D Semiconductor Materials," *2012 IEEE International Electron Devices Meeting (IEDM)*, 2012.
[121] P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson, "Contact resistance extraction in pentacene thin film transistors," *Solid-State Electronics,* vol. 47, no. 2, pp. 259-262, 2003.
[122] T. Minari, T. Nemoto, and S. Isoda, "Temperature and electric-field dependence of the mobility of a single-grain pentacene field-effect transistor," *Journal of Applied Physics,* vol. 99, no. 3, 034506, 2006.
[123] P. V. Pesavento, R. J. Chesterfield, C. R. Newman, and C. D. Frisbie, "Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature," *Journal of Applied Physics,* vol. 96, no. 12, pp. 7312-7324, 2004.
[124] I. Yagi, K. Tsukagoshi, and Y. Aoyagi, "Direct observation of contact and channel resistance in pentacene four-terminal thin-film transistor patterned by laser ablation method," *Applied Physics Letters,* vol. 84, no. 5, pp. 813-815, 2004.

[125] L. Burgi, H. Sirringhaus, and R. H. Friend, "Noncontact potentiometry of polymer field-effect transistors," *Applied Physics Letters,* vol. 80, no. 16, pp. 2913-2915, 2002.
[126] S. Kim, S. Ju, J. H. Back, Y. Xuan, P. D. Ye, M. Shim, D. B. Janes, and S. Mohammadi, "Fully Transparent Thin-Film Transistors Based on Aligned Carbon Nanotube Arrays and Indium Tin Oxide Electrodes," *Advanced Materials,* vol. 21, no. 5, pp. 564-568, 2009.
[127] S. Kim, S. Kim, J. Park, S. Ju, and S. Mohammadi, "Fully Transparent Pixel Circuits Driven by Random Network Carbon Nanotube Transistor Circuitry," *ACS Nano,* vol. 4, no. 6, pp. 2994-2998, 2010.
[128] F. Sajed, and C. Rutherglen, "All-printed and transparent single walled carbon nanotube thin film transistor devices," *Applied Physics Letters,* vol. 103, no. 14, 143303, 2013.
[129] S. Ju, J. F. Li, J. Liu, P. C. Chen, Y. G. Ha, F. Ishikawa, H. Chang, C. W. Zhou, A. Facchetti, D. B. Janes, and T. J. Marks, "Transparent active matrix organic light-emitting diode displays driven by nanowire transistor circuitry," *Nano Letters,* vol. 8, no. 4, pp. 997-1004, 2008.
[130] D. S. Hecht, L. B. Hu, and G. Irvin, "Emerging Transparent Electrodes Based on Thin Films of Carbon Nanotubes, Graphene, and Metallic Nanostructures," *Advanced Materials,* vol. 23, no. 13, pp. 1482-1513, 2011.
[131] D. Chen, Z. Liu, B. Liang, X. F. Wang, and G. Z. Shen, "Transparent metal oxide nanowire transistors," *Nanoscale,* vol. 4, no. 10, pp. 3001-3012, 2012.
[132] H. M. Kim, S. K. Jung, J. S. Ahn, Y. J. Kang, and K. C. Je, "Electrical and optical properties of In2O3-ZnO films deposited on polyethylene terephthahate substrates by radio frequency magnetron sputtering," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 42, no. 1, pp. 223-227, 2003.
[133] M. A. Lampert, "Simplified Theory of Space-Charge-Limited Currents in an Insulator with Traps," *Physical Review,* vol. 103, no. 6, pp. 1648-1656, 1956.
[134] S. McDonnell, R. Addou, C. Buie, R. M. Wallace, and C. L. Hinkle, "Defect-Dominated Doping and Contact Resistance in MoS_2," *ACS Nano,* vol. 8, no. 3, pp. 2880-2888, 2014.
[135] W. Zhou, X. L. Zou, S. Najmaei, Z. Liu, Y. M. Shi, J. Kong, J. Lou, P. M. Ajayan, B. I. Yakobson, and J. C. Idrobo, "Intrinsic Structural Defects in Monolayer Molybdenum Disulfide," *Nano Letters,* vol. 13, no. 6, pp. 2615-2622, 2013.
[136] M. P. Taylor, D. W. Readey, M. F. A. M. van Hest, C. W. Teplin, J. L. Alleman, M. S. Dabney, L. M. Gedvilas, B. M. Keyes, B. To, J. D. Perkins, and D. S. Ginley, "The Remarkable Thermal Stability of Amorphous In-Zn-O Transparent Conductors," *Advanced Functional Materials,* vol. 18, no. 20, pp. 3169-3178, 2008.
[137] M. Fujii, Y. Ishikawa, R. Ishihara, J. van der Cingel, M. R. T. Mofrad, M. Horita, and Y. Uraoka, "Low temperature high-mobility InZnO thin-film transistors fabricated by excimer laser annealing," *Applied Physics Letters,* vol. 102, no. 12, 122107, 2013.
[138] S. E. Ahn, H. J. Ji, K. Kim, G. T. Kim, C. H. Bae, S. M. Park, Y. K. Kim, and J. S. Ha, "Origin of the slow photoresponse in an individual sol-gel synthesized ZnO nanowire," *Applied Physics Letters,* vol. 90, no. 15, 153106, 2007.
[139] D. B. Chrisey, "Materials processing - The power of direct writing," *Science,* vol. 289, no. 5481, pp. 879-881, 2000.
[140] C. B. Arnold, and A. Pique, "Laser direct-write processing," *MRS Bulletin,* vol. 32, no. 1, pp. 9-12, 2007.

[141] J. Jang, R. Kitsomboonloha, S. L. Swisher, E. S. Park, H. Kang, and V. Subramanian, "Transparent High-Performance Thin Film Transistors from Solution-Processed SnO_2/ZrO_2 Gel-like Precursors," *Advanced Materials,* vol. 25, no. 7, pp. 1042-1047, 2013.

[142] D. Jena, and A. Konar, "Enhancement of carrier mobility in semiconductor nanostructures by dielectric engineering," *Physical Review Letters,* vol. 98, no. 13, 136805, 2007.

[143] C. Jang, S. Adam, J. H. Chen, E. D. Williams, S. Das Sarma, and M. S. Fuhrer, "Tuning the Effective Fine Structure Constant in Graphene: Opposing Effects of Dielectric Screening on Short- and Long-Range Potential Scattering," *Physical Review Letters,* vol. 101, no. 14, 146805, 2008.

[144] H. Kim, P. C. McIntyre, and K. C. Saraswat, "Effects of crystallization on the electrical properties of ultrathin HfO_2 dielectrics grown by atomic layer deposition," *Applied Physics Letters,* vol. 82, no. 1, pp. 106-108, 2003.

[145] S. Kamiyama, T. Miura, and Y. Nara, "Electrical properties of ultrathin HfO_2 films for replacement metal gate transistors, fabricated by atomic layer deposition using $Hf(N(CH_3)(C_2H_5))_4$ and O_3," *Applied Physics Letters,* vol. 87, no. 13, 132904, 2005.

[146] H. C. Lin, P. D. Ye, and G. D. Wilk, "Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al_2O_3 on GaAs," *Applied Physics Letters,* vol. 87, no. 18, 182904, 2005.

[147] A. Valletta, P. Gaucci, L. Mariucci, G. Fortunato, and S. D. Brotherton, "Kink effect in short-channel polycrystalline silicon thin-film transistors," *Applied Physics Letters,* vol. 85, no. 15, pp. 3113-3115, 2004.

[148] J. Jang, F. Pan, K. Braam, and V. Subramanian, "Resistance Switching Characteristics of Solid Electrolyte Chalcogenide Ag_2Se Nanoparticles for Flexible Nonvolatile Memory Applications," *Advanced Materials,* vol. 24, no. 26, pp. 3573-3576, 2012.

[149] X. M. Zou, J. L. Wang, C. H. Chiu, Y. Wu, X. H. Xiao, C. Z. Jiang, W. W. Wu, L. Q. Mai, T. S. Chen, J. C. Li, J. C. Ho, and L. Liao, "Interface Engineering for High-Performance Top-Gated MoS_2 Field-Effect Transistors," *Advanced Materials,* vol. 26, no. 36, pp. 6255-6261, 2014.

[150] S. Arcidiacono, N. R. Bieri, D. Poulikakos, and C. P. Grigoropoulos, "On the coalescence of gold nanoparticles," *International Journal of Multiphase Flow,* vol. 30, no. 7-8, pp. 979-994, 2004.

[151] T. A. Savas, M. L. Schattenburg, J. M. Carter, and H. I. Smith, "Large-area achromatic interferometric lithography for 100 nm period gratings and grids," *Journal of Vacuum Science & Technology B,* vol. 14, no. 6, pp. 4167-4170, 1996.

[152] H. Pan, D. J. Hwang, S. H. Ko, T. A. Clem, J. M. J. Frechet, D. Bauerle, and C. P. Grigoropoulos, "High-Throughput Near-Field Optical Nanoprocessing of Solution-Deposited Nanoparticles," *Small,* vol. 6, no. 16, pp. 1812-1821, 2010.

[153] C. Pierrat, and S. Vaidya, "Required Optical Characteristics of Materials for Phase-Shifting Masks," *Applied Optics,* vol. 34, no. 22, pp. 4923-4928, 1995.

[154] P. Muller, Y. Jourlin, C. Veillas, G. Bernaud, Y. Bourgin, S. Tonchev, and O. Dellea, "On-the-fly writing of a long grating phase mask," *Optical Engineering,* vol. 50, no. 3, 038001, 2011.

[155] Y. Qiu, Y. L. Sheng, and C. Beaulieu, "Optimal phase mask for fiber Bragg grating fabrication," *Journal of Lightwave Technology,* vol. 17, no. 11, pp. 2366-2370, 1999.

[156] M. Melo, and P. V. S. Marques, "Fabrication of Tailored Bragg Gratings by the Phase Mask Dithering/Moving Technique," *Photonic Sensors,* vol. 3, no. 1, pp. 81-96, 2013.
[157] A. C. Arias, J. Daniel, B. Krusor, S. Ready, V. Sholin, and R. Street, "All-additive ink-jet-printed display backplanes: Materials development and integration," *Journal of the Society for Information Display,* vol. 15, no. 7, pp. 485-490, 2007.
[158] T. Kawase, T. Shimoda, C. Newsome, H. Sirringhaus, and R. H. Friend, "Inkjet printing of polymer thin film transistors," *Thin Solid Films,* vol. 438, pp. 279-287, 2003.
[159] V. Subramanian, J. M. J. Frechet, P. C. Chang, D. C. Huang, J. B. Lee, S. E. Molesa, A. R. Murphy, and D. R. Redinger, "Progress toward development of all-printed RFID tags: Materials, processes, and devices," *Proceedings of the IEEE,* vol. 93, no. 7, pp. 1330-1338, 2005.
[160] E. S. Park, Y. H. Chen, T. J. K. Liu, and V. Subramanian, "A New Switching Device for Printed Electronics: Inkjet-Printed Microelectromechanical Relay," *Nano Letters,* vol. 13, no. 11, pp. 5355-5360, 2013.
[161] S. J. Chung, M. A. Ul Karim, M. Spencer, H. J. Kwon, C. P. Grigoropoulos, E. Alon, and V. Subramanian, "Exploitation of the coffee-ring effect to realize mechanically enhanced inkjet-printed microelectromechanical relays with U-bar-shaped cantilevers," *Applied Physics Letters,* vol. 105, no. 26, 261901, 2014.
[162] S. Chung, M. A. U. Karim, H. J. Kwon, and V. Subramanian, "High-Performance Inkjet-Printed Four-Terminal Microelectromechanical Relays and Inverters," *Nano Letters,* vol. 15, no. 5, pp. 3261-3266, 2015.
[163] S. Chung, M. Jang, S. B. Ji, H. Im, N. Seong, J. Ha, S. K. Kwon, Y. H. Kim, H. Yang, and Y. Hong, "Flexible High-Performance All-Inkjet-Printed Inverters: Organo-Compatible and Stable Interface Engineering," *Advanced Materials,* vol. 25, no. 34, pp. 4773-4777, 2013.
[164] A. Valletta, A. Daami, M. Benwadih, R. Coppard, G. Fortunato, M. Rapisarda, F. Torricelli, and L. Mariucci, "Contact effects in high performance fully printed p-channel organic thin film transistors," *Applied Physics Letters,* vol. 99, no. 23, 233309, 2011.
[165] S. H. Kim, K. Hong, W. Xie, K. H. Lee, S. P. Zhang, T. P. Lodge, and C. D. Frisbie, "Electrolyte-Gated Transistors for Organic and Printed Electronics," *Advanced Materials,* vol. 25, no. 13, pp. 1822-1846, 2013.
[166] M. F. Naccache, and P. R. S. Mendes, "Heat transfer to non-Newtonian fluids in laminar flow through rectangular ducts," *International Journal of Heat and Fluid Flow,* vol. 17, no. 6, pp. 613-620, 1996.
[167] W. Ryu, Z. B. Huang, J. S. Park, J. Moseley, A. R. Grossman, R. J. Fasching, and F. B. Prinz, "Open micro-fluidic system for atomic force microscopy-guided in situ electrochemical probing of a single cell," *Lab on a Chip,* vol. 8, no. 9, pp. 1460-1467, 2008.
[168] U. Lang, E. Muller, N. Naujoks, and J. Dual, "Microscopical Investigations of PEDOT:PSS Thin Films," *Advanced Functional Materials,* vol. 19, no. 8, pp. 1215-1220, 2009.
[169] J. Ouyang, Q. F. Xu, C. W. Chu, Y. Yang, G. Li, and J. Shinar, "On the mechanism of conductivity enhancement in poly (3,4-ethylenedioxythiophene): poly(styrene sulfonate) film through solvent treatment," *Polymer,* vol. 45, no. 25, pp. 8443-8450, 2004.

[170] Y. J. Xia, and J. Y. Ouyang, "Salt-Induced Charge Screening and Significant Conductivity Enhancement of Conducting Poly(3,4-ethylenedioxythiophene): Poly (styrenesulfonate)," *Macromolecules,* vol. 42, no. 12, pp. 4141-4147, 2009.
[171] B. Y. Ahn, D. J. Lorang, and J. A. Lewis, "Transparent conductive grids via direct writing of silver nanoparticle inks," *Nanoscale,* vol. 3, no. 7, pp. 2700-2702, 2011.
[172] J. B. Wu, H. A. Becerril, Z. N. Bao, Z. F. Liu, Y. S. Chen, and P. Peumans, "Organic solar cells with solution-processed graphene transparent electrodes," *Applied Physics Letters,* vol. 92, no. 26, 263302, 2008.
[173] Q. Zhang, X. J. Wan, F. Xing, L. Huang, G. K. Long, N. B. Yi, W. Ni, Z. B. Liu, J. G. Tian, and Y. S. Chen, "Solution-processable graphene mesh transparent electrodes for organic solar cells," *Nano Research,* vol. 6, no. 7, pp. 478-484, 2013.
[174] G. Eda, G. Fanchini, and M. Chhowalla, "Large-area ultrathin films of reduced graphene oxide as a transparent and flexible electronic material," *Nature Nanotechnology,* vol. 3, no. 5, pp. 270-274, 2008.
[175] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J. H. Ahn, P. Kim, J. Y. Choi, and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature,* vol. 457, no. 7230, pp. 706-710, 2009.
[176] M. Kaempgen, G. S. Duesberg, and S. Roth, "Transparent carbon nanotube coatings," *Applied Surface Science,* vol. 252, no. 2, pp. 425-429, 2005.
[177] K. A. Watson, S. Ghose, D. M. Delozier, J. G. Smith, and J. W. Connell, "Transparent, flexible, conductive carbon nanotube coatings for electrostatic charge mitigation," *Polymer,* vol. 46, no. 7, pp. 2076-2085, 2005.
[178] Z. B. Yu, X. F. Niu, Z. T. Liu, and Q. B. Pei, "Intrinsically Stretchable Polymer Light-Emitting Devices Using Carbon Nanotube-Polymer Composite Electrodes," *Advanced Materials,* vol. 23, no. 34, pp. 3989-3994, 2011.
[179] F. M. Blighe, Y. R. Hernandez, W. J. Blau, and J. N. Coleman, "Observation of percolation-like scaling - Far from the percolation threshold - In high volume fraction, high conductivity polymer-nanotube composite films," *Advanced Materials,* vol. 19, no. 24, pp. 4443-4447, 2007.
[180] S. De, P. E. Lyons, S. Sorel, E. M. Doherty, P. J. King, W. J. Blau, P. N. Nirmalraj, J. J. Boland, V. Scardaci, J. Joimel, and J. N. Coleman, "Transparent, Flexible, and Highly Conductive Thin Films Based on Polymer - Nanotube Composites," *ACS Nano,* vol. 3, no. 3, pp. 714-720, 2009.
[181] J. Y. Lee, S. T. Connor, Y. Cui, and P. Peumans, "Solution-processed metal nanowire mesh transparent electrodes," *Nano Letters,* vol. 8, no. 2, pp. 689-692, 2008.
[182] S. De, T. M. Higgins, P. E. Lyons, E. M. Doherty, P. N. Nirmalraj, W. J. Blau, J. J. Boland, and J. N. Coleman, "Silver Nanowire Networks as Flexible, Transparent, Conducting Films: Extremely High DC to Optical Conductivity Ratios," *ACS Nano,* vol. 3, no. 7, pp. 1767-1774, 2009.
[183] A. R. Madaria, A. Kumar, F. N. Ishikawa, and C. W. Zhou, "Uniform, Highly Conductive, and Patterned Transparent Films of a Percolating Silver Nanowire Network on Rigid and Flexible Substrates Using a Dry Transfer Technique," *Nano Research,* vol. 3, no. 8, pp. 564-573, 2010.
[184] L. B. Hu, H. S. Kim, J. Y. Lee, P. Peumans, and Y. Cui, "Scalable Coating and Properties of Transparent, Flexible, Silver Nanowire Electrodes," *ACS Nano,* vol. 4, no. 5, pp. 2955-2963, 2010.

[185] A. R. Madaria, A. Kumar, and C. W. Zhou, "Large scale, highly conductive and patterned transparent films of silver nanowires on arbitrary substrates and their application in touch screens," *Nanotechnology,* vol. 22, no. 24, 245201, 2011.
[186] J. Lee, P. Lee, H. Lee, D. Lee, S. S. Lee, and S. H. Ko, "Very long Ag nanowire synthesis and its application in a highly transparent, conductive and flexible metal electrode touch panel," *Nanoscale,* vol. 4, no. 20, pp. 6408-6414, 2012.
[187] S. M. Bergin, Y. H. Chen, A. R. Rathmell, P. Charbonneau, Z. Y. Li, and B. J. Wiley, "The effect of nanowire length and diameter on the properties of transparent, conducting nanowire films," *Nanoscale,* vol. 4, no. 6, pp. 1996-2004, 2012.
[188] S. K. Duan, Q. L. Niu, J. F. Wei, J. B. He, Y. A. Yin, and Y. Zhang, "Water-bath assisted convective assembly of aligned silver nanowire films for transparent electrodes," *Physical Chemistry Chemical Physics,* vol. 17, no. 12, pp. 8106-8112, 2015.
[189] E. C. Garnett, W. S. Cai, J. J. Cha, F. Mahmood, S. T. Connor, M. G. Christoforo, Y. Cui, M. D. McGehee, and M. L. Brongersma, "Self-limited plasmonic welding of silver nanowire junctions," *Nature Materials,* vol. 11, no. 3, pp. 241-249, 2012.
[190] S. Han, S. Hong, J. Ham, J. Yeo, J. Lee, B. Kang, P. Lee, J. Kwon, S. S. Lee, M. Y. Yang, and S. H. Ko, "Fast Plasmonic Laser Nanowelding for a Cu-Nanowire Percolation Network for Flexible Transparent Conductors and Stretchable Electronics," *Advanced Materials,* vol. 26, no. 33, pp. 5808-5814, 2014.
[191] G. A. Salvatore, N. Münzenrieder, C. Barraud, L. Petti, C. Zysset, L. Büthe, K. Ensslin, and G. Tröster, "Fabrication and Transfer of Flexible Few-Layers MoS_2 Thin Film Transistors to Any Arbitrary Substrate," *ACS Nano,* vol. 7, no. 10, pp. 8809-8815, 2013.
[192] M. Hasegawa, and K. Horie, "Photophysics, photochemistry, and optical properties of polyimides," *Progress in Polymer Science,* vol. 26, no. 2, pp. 259-335, 2001.
[193] M. C. Choi, Y. Kim, and C. S. Ha, "Polymers for flexible displays: From material selection to device applications," *Progress in Polymer Science,* vol. 33, no. 6, pp. 581-630, 2008.
[194] S. Bertolazzi, J. Brivio, and A. Kis, "Stretching and Breaking of Ultrathin MoS_2," *ACS Nano,* vol. 5, no. 12, pp. 9703-9709, 2011.
[195] J. Kwon, Y. K. Hong, H. J. Kwon, Y. Jin Park, B. Yoo, J. Kim, C. P. Grigoropoulos, M. Suk Oh, and S. Kim, "Optically transparent thin-film transistors based on 2D multilayer MoS_2 and indium zinc oxide electrodes," *Nanotechnology,* vol. 26, no. 3, 035202, 2015.
[196] W. Bao, X. Cai, D. Kim, K. Sridhara, and M. S. Fuhrer, "High mobility ambipolar MoS_2 field-effect transistors: Substrate and dielectric effects," *Applied Physics Letters,* vol. 102, no. 4, 042104, 2013.
[197] H. J. Kwon, H. Shim, S. Kim, W. Choi, Y. Chun, I. Kee, and S. Lee, "Mechanically and optically reliable folding structure with a hyperelastic material for seamless foldable displays," *Applied Physics Letters,* vol. 98, no. 15, 151904, 2011.
[198] M. Ohring, *The Materials Science of Thin FIlms*, San Diego: Academic Press, 1992.
[199] D. H. Kim, J. H. Ahn, M. C. Won, H. S. Kim, T. H. Kim, J. Song, Y. Y. Huang, Z. Liu, C. Lu, and J. A. Rogers, "Stretchable and Foldable Silicon Integrated Circuits," *Science,* vol. 320, no. 5875, pp. 507-511, 2008.
[200] D. Kim, G. Shin, Y. J. Kang, W. Kim, and J. S. Ha, "Fabrication of a Stretchable Solid-State Micro-Supercapacitor Array," *ACS Nano,* vol. 7, no. 9, pp. 7975-7982, 2013.