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Heteroepitaxial Thick GaN Layers and Vertical High-Power Devices by Selective Area MOCVD Growth

A dissertation submitted in partial satisfaction of

the requirements for the degree Doctor of Philosophy

in

Materials Science and Engineering

by

Atsunori Tanaka

Committee in charge:

Professor Shadi A. Dayeh, Chair
Professor Peter M. Asbeck
Professor Prabhakar R. Bandaru
Professor William Trogler
Professor Charles Tu
Professor Paul K. Yu

2019

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The Dissertation of Atsunori Tanaka is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2019

DEDICATION

To my parents

TABLE OF CONTENTS

Signature Page iii

Dedication iv

Table of Contents v

List of Figures viii

List of Tables xiii

Acknowledgement xiv

Vita xviii

Publications xviii

Conferences xx

Field of study xxi

Abstract of the Dissertation xxii

Chapter 1 Motivation and Challenges for Vertical GaN High Power Devices on Si 1

1.1 Introduction 1

1.2 Background of Wide Bandgap Power Device 2

1.2.1 Advantages of GaN Over Si-Based Power Device 2

1.2.2 Pros and Cons of Lateral and Vertical Power Devices 6

1.2.3 Requirement for Vertical Power Device 8

1.3 Challenges for GaN Vertical Power Device on Si 10

1.3.1 Thickness limitation due to Thermal Mismatch Between GaN and Si 11

1.3.2 Unintentional Doping of GaN in MOCVD and Selective Area Growth (SAG) 16

1.4 Overview of the Dissertation.......... **17**

1.5 References.......... **18**

Chapter 2 A Comprehensive Analysis of GaN Selective Area Growth: Size Effects and Influence on Light Extraction from GaN Light Emitting Diodes.......... **21**

2.1 Introduction.......... **21**

2.2 Experimental Details.......... **23**

2.3 Generic Geometric Effects in SAG GaN on c-Sapphire.......... **24**

2.3.1 Gallium Adatom Diffusion Length on GaN Surface.......... 29

2.3.2 Diameter Dependent Vertical Growth Rate.......... 31

2.3.3 Spacing Dependent Vertical Growth Rate.......... 33

2.3.4 Spacing Dependent Lateral Growth Rate, Facet Length and Facet Evolution.......... 35

2.3.5 Time Dependent Facet Evolution.......... 37

2.4 Enhancement of LED Light Extraction by Tailoring Array Pattern Structure.......... **38**

2.5 Conclusion.......... **46**

2.6 Acknowledgements.......... **46**

2.7 References.......... **47**

Chapter 3 Si Complies with GaN to Overcome Thermal Mismatches for the Heteroepitaxy of Thick GaN on Si.......... **51**

3.1 Introduction.......... **51**

3.2 Optimization of SAG Mask Design for Thick GaN Growth.......... **52**

3.3 Cracking Mechanism of SAG GaN-on-Si.......... **55**

3.3.1 Time Dependent Growth of SAG GaN on Si.......... 55

3.3.2 Stress Relaxation by Facet Evolution.......... 56

3.3.3 Stress Measurement by Micro Raman Spectroscopy.......... 60

3.4 Tangential Stress in GaN/Si Interface and Cracking in Si substrate.......... **63**

3.4.1 Observation of Cracking in Si substrate....63

3.4.2 Substrate Engineering to Accommodate the Tangential Stress....68

3.5 Material Quality Improvement by Thick GaN Growth....71

3.6 Demonstration of Vertical GaN MISFET on Si....73

3.5 Conclusion....77

3.6 Acknowledgements....77

3.7 References....78

Chapter 4 Structural and electrical characterization of thick GaN layers on Si, GaN, and engineered substrates....80

4.1 Introduction....80

4.2 Experimental Detail....82

4.3 Evaluation of Defect Densities as a Function of Thickness for Each Substrates....84

4.4 Evaluation of SAG Electronic Properties by Schottky Barrier Diode Characterization....90

4.4.1 Current, Capacitance -Voltage Characteristics of SBDs on Each Substrates....90

4.4.2 Geometrical Effect of Dislocation Densities and Ideality Factors....99

4.4.3 Effect of Geometrical FCarrier Concentration and Sample Holder on the Carrier Concentrations....102

4.4.3 Breakdown Characteristics of GaN SBDs on QST substrate....105

4.5 Conclusion....107

4.6 Acknowledgements....107

4.7 References....108

LIST OF FIGURES

Figure 1.1 Schematic illustration of (a) lateral AlGaN/GaN HEMT and (b) GaN current-aparture-vertical-electron-transistor(CAVET). 6

Figure 1.2 Breakdown voltage vs drift region doping concentration for each drift layer thickness from 1 to 100 μm.[11] 8

Figure 1.3 **(a)** Stress in GaN film as a fuction of the thickness. The AlGaN buffer layer thickness decrease the increment of tensile stress generation. **(b)** Critical thickness of GaN for cracking as a function of buffer layer thickness.[18] 12

Figure 1.4 Process sequence for the laser lift -off of 2” GaN membranes. **(a)** Laser lift-ff of the GaN film from sapphire; **(b)** sapphire removal; **(c)** deposition of a ~3mm thick layer of thermoplastic adhesive at 120 °C; **(d)** peel-off of the silicone elastomer.[19] 13

Figure 1.5 **(a)** Microscope image of as-grown LEDs layer on patterned Si substrate. **(b)** Top-view SEM image of GaN on patterned Si substrate.[20] 15

Figure 1.6 Microscope image of SAG GaN/AlN/Si. **(a)** GaN film grown without grid mask. **(b)** GaN grown on 500 μm wide square windows with 200 μm wide masks. **(c)** GaN grown on 200 μm square windows with 10 μm wide masks.[21] 15

Figure 2.1 Photomask design for SAG GaN on 2 inch wafer.. 22

Figure 2.2 Top view SEM images of the SAG GaN structures for different mask openings (a) 80 μm, (b) 150 μm, (c) 350 μm, and (d) 450 μm for edge-to-edge spacings in the range of 20 μm to 450 μm. 25

Figure 2.3 45°-angled SEM images of the SAG GaN structures for different mask openings (a) 80 μm, (b) 150 μm, (c) 350 μm, and (d) 450 μm for edge-to-edge spacings in the range of 20 μm to 450 μm. Strong vertical growth rate enhancement was observed for all diameters and spacings. 26

Figure 2.4 Surface profilometry on the grown structure with (a) fixed spacing at 20 μm and (b) fixed diameter at 350 μm. (c) The heights of the grown structures as a function of the mask diameters and (d) the inverse of the mask diameters; the inset highlights the large diameter region of the plots. 28

Figure 2.5 (a) Edge heights for the grown structures. (b) The lateral overgrowth lengths and (c) the facet lengths as a function of the mask spacings. The facet lengths are defined as the average length of the six sides of the grown hexagon base. (d) Schematic illustration of the collection area contributing to the vertical growth 34

Figure 2.6 Facet evolution with the mask geometry as was observed by SEM. The triangles represent the grown structure with six complete well-developed facets and the crosses represent the grown structure with at least one rough sidewall. 36

Figure 2.7 Top-view SEM image of the samples with 80 μmD and 150 μmS with different growth time. 37

Figure 2.8 Schematic illustration of the device structure for (a) non-faceted SAG LED and (b) well-faceted SAG LED. Optical microscope images of (c) non-faceted and (d) well-faceted and their emitting images in (e) and (f) respectively. The mask geometries are the same, 350 μmD and 80 μmS for each structure. 39

Figure 2.9 Current-voltage characteristics of (red line) non-faceted LED and (black line) well-faceted LED with (a) linear scale and (b) log scale. 40

Figure 2.10 (a) Electroluminescence of the SAG LED samples with/without well-developed facets at 10 mA injection current. Electroluminescence of (b) well-faceted LED and (d) non-faceted LED with different currents. (c) Integrated EL intensities of well-faceted/non-facet LED with different current densities. 41

Figure 2.11 Angled view SEM images of (a) well-faceted and (c) non-faceted samples and their cross-sectional cut areas. The cross-sectional HRTEM images at the edge locations of (b) well-faceted and (d) non-faceted samples. 43

Figure 2.12 Cross-sectional TEM images of (a),(c) well-faceted and (b), (d) non-faceted MQW structures near the center of the structures. (a) and (b) show the uniform growth of three cycles of InGaN MQWs. (c) and (d) are zoomed-in images of (a) and (b), respectively. 44

Figure 3.1 **(a)** Thermal stress distribution at the GaN/Si interfaces with different mask designs showing the lowest stress maxima for the circular mask. **(b)** Top view optical microscope images of the SAG GaN grown to have 10 μm at the center of the structure. The GaN with triangular and squared patterns severely cracked as predicted in Fig. 3.1 (a). 54

Figure 3.2 Top-view optical microscope images of SAG GaN with different growth time. The thicker GaN shows well-developed hexagonal facets and no crack whereas the thin GaN shows severe cracks and facets have not developed yet. 55

Figure 3.3 **(a)** Cross-sectional HR-TEM images at the edge of hexagonal facets. The sidewall facet and top surface planes are identified by FFT patterns in the bottom-left inset. **(b)** Illustration of hexagonal crystal structure (not showing inter-lattice atoms). 57

Figure 3.4 **Major crack plane determination by SEM.** Angled view SEM image of diced GaN disk in <1010> direction. The crack propagates straight down to the substrate and ~60° intersections, indicating the crack plane is in (1010) and propagate in the <2110> directions. 57

Figure 3.5 **TEM sample preparation.** SEM images of FIB cut and lifting of TEM slab by omniprobe. FIB cuts were perpendicular to the hexagonal facets {0111} in (**a**) and to the major crack{0110} planes in (**b**) to reveal the relationship between crack directions and facets. 58

Figure 3.6 **Crack plane determination by TEM.** 59

Figure 3.7 Stress relaxation due to hexagonal facets. Top view microscope images and Raman Shift of **(a, c)** thin GaN disk and **(b, d)** thick GaN disk as a function of X, distance from the disk center. The dashed line indicates the reference peak for non-stressed GaN E2H(568 cm^{-1})..61

Figure 3.8 Stress relaxation mechanism in crack-free GaN-on-Si by facet formation........62

Figure 3.9 (a) Evolution of thermal stress during cooling down from 1050 to 100 °C. The solid black lines are the original GaN disk location at the growth temperature. **(b)** Cross-sectional view of thermal stress simulation of SAG GaN with/without Si base etched. The stress peaks at the interface of hexagonal vertices were eliminated by removing Si under the SAG GaN. 63

Figure 3.10 Elimination of tangential cracking in Si. **(a,b)** Optical/SEM images of thick SAG GaN on Si with no Si etch. Cracking can be clearly observed in the base Si in a tangential fashion. (**c,d)** Optical/SEM images of Si-etched thick SAG GaN on Si with no cracking in either GaN or Si. 64

Figure 3.11 (a) Angled view SEM images of FIB cut GaN disk without isotropic etch. **(b,c)** Peeling issue in dense SAG GaN on Si array. Angled view SEM images of highly packed SAG GaN disk arrays (dot-to-dot spacing 20 μm). The high packing density led to severe cracking and eventual peel off for the GaN disk from substrate. 65

Figure 3.12 Mapping of rotational stress components, ∂_{xy}. Top view **(a-d)** and angled view **(e-h)** of mesh pattern for different geometries used in all simulations. **(i-l)** Mapping of stress tensors at the interface of GaN/Si with anisotropic elastic matricies.................................66

Figure 3.13 Angled-view SEM images of Si etched SAG GaN disk before **(a)** and after **(b,c)** growth..68

Figure 3.14 Substrate engineering for crack elimination in Si. (a) Top view microscope image and **(b)** angled view SEM image showing no cracking from both images. **(c)** Angled view SEM image of FIB cut GaN disk with proper base Si etching...70

Figure 3.15 Millimeter scale SAG GaN growth on Si. (a,b,c) Angled view SEM images of 1mm, 1.2mm, and 1.6mm diameter GaN disks showing no cracking in GaN-on-Si post 3 hours of GaN growth. **(d)** Cross-sectionl SEM images from 1.4mm diameter GaN on Si showing a thickness of 5 μm. 70

Figure 3.16 Threading dislocation density reduction in thick GaN disk. (a,b) L-R Cross-sectional images of GaN-on-Si by SEM, bright field TEM, dark field TEM at two-beam condition with g=[0001] and dark field TEM with g=[1120] for 10 μm thick (**a**) and 18 μm thick (**b**) GaN layers.. 72

Figure 3.17 Dislocation selective etching. (a) Top view microscope image after etching **(b)** Top view SEM image near the center of the disk where most dislocations were found.............72

Figure 3.18 **(a)** Schematic structure of GaN-on-Si vertical MISFET on 19 µm SAG GaN layer. **(b)** Cross-sectional SEM image of the trench-gate region. **(c)** Linear (blue) and log (red) scale transfer I-V characteristics (I_{DS}-V_{GS}) and gate leakage (I_G-V_{GS}) at V_{DS} = 1V **(d)** Output I-V characteristics (I_{DS}-V_{DS}) at different gate voltages in steps of 2V......................................75

Figure 3.19 **Threshold voltage shift.** Linear transfer characteristics (I_{DS}-V_{GS}) at V_{DS} = 1V with different voltage sweep direction...76

Figure 4.1 Top view SEM images of GaN surface after defect selective etching. Linear reduction of defect densities was observed in GaN-on-Si and GaN-on-QST with increasing the thicknesses. The GaN-on-GaN samples did not show any surface pits after the etching. The scale marker is 10 µm...86

Figure 4.2 Cross sectional TEM images under the Schottky contact (g = [0001]). The width of the imaged sections is 10 µm and the scale bar is 5 µm. The inset for the 5 µm thick GaN-on-QST is a larger field of view TEM image that shows the interface with the Si layer (white arrow) and the location of the pre-grown planar GaN layer (red arrow) prior to SAG. 89

Figure 4.3 Linear and semi-log scale I-V characteristics of GaN-on-Si SBDs with different thicknesses of (a) 5 µm, (b) 10 µm, (c) 15 µm, and (d) 20 µm. The red axis shown in the right side is the linear scale axis...93

Figure 4.4 Linear and semi-log scale I-V characteristics of GaN-on-QST SBDs with different thicknesses of (a) 5 µm, (b) 10 µm, (c) 15 µm, and (d) 20 µm. The red axis shown in the right side is the linear scale axis...95

Figure 4.5 Linear and semi-log scale I-V characteristics of GaN-on-GaN SBDs with different thicknesses of (a) 5 µm, (b) 10 µm, (c) 15 µm, and (d) 20 µm. The red axis shown in the right side is the linear scale axis...96

Figure 4.6 Linear and semi-log scale I-V characteristics of the best SBDs for any given SAG thickness and on all studied substrates for (a) GaN-on-Si, (b) GaN-on-QST, (c) GaN-on-GaN. (d) Comparison of the best performance devices from all three types of substrates. 98

Figure 4.7 3D color map of etch pit counts for each dot in the SAG arrays on the GaN-on-Si and GaN-on-QST...100

Figure 4.8 3D color map of ideality factors of each dot in the SAG arrays for the GaN-on-Si, GaN-on-QST and GaN-on-GaN. 101

Figure 4.9 3D color map of carreir concentration of each dot in the SAG arrays for the GaN-on-Si, GaN-on-QST and GaN-on-GaN. 103

Figure 4.10 **(a)** A picture showing MOCVD growth chamber. The sapphire holder is to prevent deposition of materials on the susceptor surface. Carrier concentration mapping of SAG GaN on QST **(b)**before and **(c)**after the removal of the sapphire holder. 104

Figure 4.11 Breakdown characteristics of GaN-on-QST SBDs fabricated on 20 μm thick drift layers with different carreir concentrations. All the SBDs have no edge termination........ 106

LIST OF TABLES

Table 1.1 Material properties of wide bandgap semiconductors in comparison with those of Silicon[4,6,7] 3

Table 1.2 Implications of the usual substrate materials for the GaN-epitaxy (data relative to the GaN properties.[6] 10

Table 2.1 Diffusion lengths for selected different mask geometries 30

Table 2.2 MQW thicknesses of the well-faceted and non-faceted LED at different points of the structures; center, edge and sidewall of the structure. These thicknesses were measured from TEM images and averaged over 10 lines for each point. 45

Table 4.1. Substrate and buffer layer details and properties. 83

Table 4.2 GaN-on-Si SBD characteristics. 93

Table 4.3 GaN-on-QST SBD characteristics. 95

Table 4.4 GaN-on-GaN SBD characteristics 96

Table 4.5 SBD breakdown characteristics for GaN-on-QST substrates with different carrier concentrations. 106

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1. MRS Fall Meeting & Exhibit "Heteroepitaxy of Thick GaN layers on Si and Improvement of electrical/Material Characteristics by Defect Annihilation", **November 2018 (MRS graduate student silver award)**
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4. 59th Electronic Materials Conferences "Selective Area Growth and Characterization of over 15um thick Vertical GaN Diodes on Si", **June 2017**
5. 15th International Conference on Advanced Materials "When GaN and Si Tango, Thermal Mismatches are Overcome for Thick GaN- on-Si Vertical Power Devices", **August 2017 (Award for Encouragement of Research)**
6. 58th Electronic Materials Conferences "Strain Engineering for over 10 μm Thick Crack-Free GaN Growth on Si for High Power Applications", **June 2016**
7. Lawrence Symposium on Epitaxy "Beyond 10 μm Thick Crack-Free GaN Growth on Si for High Power Device Application", **February 2016**
8. 43rd Conference on the Physics & Chemistry of Surfaces & Interfaces "Beyond 10 μm Thick Crack-Free GaN Growth on Si for High Power Device Application", **January 2016**
9. 47th International Conference of Solid State Devices and Materials "Beyond 10 μm Thick Crack-Free GaN Growth on Si for High Power Device Application", **September 2015**
10. Two presentation: 57th Electronic Materials Conferences "Beyond 10 μm Thick Crack-Free GaN Growth on Si for High Power Device Application" and "Size Effects on the Selective Area Growth of GaN on Sapphire", **June 2015**

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3. UCSD-NSYSU Bilateral Symposium " When GaN Tangoes with Si, Thermal Mismatches are Overcome for Thick GaN-on-Si Vertical Power Device", **November 2017**

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Heteroepitaxial Thick GaN Layers and Vertical High-Power Devices by Selective Area MOCVD Growth

by

Atsunori Tanaka

Doctor of Philosophy in Materials Science and Engineering

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Gallium nitride (GaN) is now widely used in commercial white Light Emitting Diodes (LEDs) thanks to the emergence of high-brightness GaN blue LEDs in 1990s. In addition to its application in solid-state lighting, GaN has been also vowed as a strong contender for next-generation high power and frequency devices due to its high critical electric field (3.3 MV/cm) and high mobility of the 2-dimensional electron gas (2DEG) at the aluminum gallium nitride

(AlGaN)/GaN interface. Lateral AlGaN/GaN high-electron-mobility-transistors (HEMTs) have been available as commercial off-the-shelf devices since 2005. However, with the demand for even higher power at reduced chip area and cost and with better thermal management at high currents, vertical device architectures have emerged as the chosen structure to meet these demands.

But vertical devices that can hold high power require thick and high quality GaN layers. Recent developments of bulk GaN substrate growth technologies allowed vertical GaN device with thick drift layer to be more feasible. However, GaN substrate technology is challenged with cost, reliability and uniformity issues even at the currently commercially available 2" (diameter) substrates. Therefore, GaN vertical power devices on cheap substrates without compromising the GaN material quality remains to be of great interest. Si substrates with their fab-scale integrated circuit technology can propel the development of commercial vertical high power GaN devices. The biggest challenge for realizing thick GaN layers on Si to hold high voltage in the vertical direction is the large thermal and lattice mismatch between GaN and Si that leads to cracking of the GaN layers beyond only a few micrometers.

In major part of this dissertation, we will focus on the epitaxy techniques of thick crack-free GaN layers on Si by selective area growth (SAG) and the fabrication of vertical GaN switches. The epitaxy technique developed in this work resulted in crack-free thick GaN layers on Si that are of high quality with low dislocation densities and low background doping in order to sustain high breakdown voltages. The developed processes hold the potential to significantly advance the fundamental electronic materials research in power devices and their efficient system level integration.

Chapter 1

Motivation and Challenges for Vertical GaN High Power Devices on Si

1.1 Introduction

Modern human life and our societies are currently dependent on energy, more specifically electricity even at the personal level. Much effort has been made to implement green energies as electrical power generation for realizing a sustainable society. The energy production using renewable energies led mainly by solar cells has been attracting attention from various fields for decades. Concurrent with this development, energy losses in power conversion process by present Si-based power devices is known to be 10-20 % due to limitation in the physical properties of the Si material itself.[1] The energy loss in inefficient power electronic devices almost equated with the US renewable energy consumption in 2018.[2] Therefore, the pursuit of effective power conversion systems in parallel with renewable energy generation is equally important for enabling an energy saving society. To make drastic improvement in power conversion, it is inevitable to substitute Si with other higher performing materials and to pursue innovations at all levels of device

development and packaging of power electronics as well as at the circuit and magnetics levels of power conversion modules.

1.2 Background of Wide Bandgap Power Device

1.2.1 Advantages of GaN Over Si-Based Power Device

For high power and high frequency operation, the power device should have short carrier transit time τ between the source to drain spacing l in switching field-effect transistor (FET) devices. On the contrary, applicable voltage becomes lowered since the electric field is inversely proportional to the spacing, which results in lowering the breakdown voltage. The breakdown voltage for impact ionization can be expressed using critical electric field, E_c,[3,4]

$$B_V = E_c \cdot l \tag{1-1}$$

The cutoff frequency, which is the frequency at which the enegy (Gain) of the system begins to reduce, is described using carrier saturation velocity, v_{sat},

$$f_T = \frac{1}{2\pi\tau} = \frac{v_{sat}}{2\pi l} \tag{1-2}$$

Therefore, we can define the trade-off relationship between the breakdown voltage and the cutoff frequency, f_T as:

$$B_V \cdot f_T = \frac{E_c \cdot v_{sat}}{2\pi} \tag{1-3}$$

The eq. (1-3) is independent of the device spacing and defined only by materials properties. Therefore, this index is often used as one of the FOM (figure of merit) of the materials for high frequency devices, which is called Johnson's FOM(JFOM).[5]

Table 1.1 Material properties of wide bandgap semiconductors in comparison with those of Silicon[4,6,7]

Parameter	Silicon	4H-SiC	GaN	Diamond
E_g, eV	1.12	3.26	3.39	5.47
E_c, MV/cm	0.23	2.2	3.3	5.6
μ_n, cm^2/Vs	1400	950	800/1700[a]	1800
v_{sat}, cm/s	1.0×10^7	2.0×10^7	2.7×10^7	2.0×10^7
ε_r	11.8	9.7	9	5.7
JFOM	1	20	40	50
BFOM	1	500	1300/2700[a]	9000

[a] Significant difference between the bulk/the 2DEG

As shown in **Table 1.1**, the critical electric field, E_c is typically larger for wide band gap materials since impact ionization would not take place till the hot carriers gain the energy exceeding that of the bandgap to generate electron-hole pairs. This is why wide bandgap semiconductors are suitable for high-frequency and high-power device applications. Among these wide bandgap semiconductors, silicon carbide (SiC)-based power metal-oxide FETs (MOSFETs) have been already commercialized and started to replace some Si-based power modules in electric vehicles thanks to earlier development of SiC wafer technology. However, SiC also suffers from low effective channel mobility, which limits the FOM. GaN similarly possesses higher bandgap and therefore higher critical electric field, but what is distinctive about GaN is that it also has the

highest saturation velocity of GaN materials is estimated to be higher than other wide bandgap semiconductor materials due to the relatively large energy separation of electrons between the conduction band Γ and L minima that reduces intervalley scattering and sustains the high electron velocity and mobility at high electric fields. Therefore, GaN is more suitable for high-frequency and high-power applications. As a reference, the normalized JFOM of Si, SiC, GaN and diamond materials are approximately 1, 20, 40 and 50 calculated from material properties in **Table 1.1** using eq. (1-3).

For vertical high voltage device, another expression for trade-off relationship between on-resistance, R_{on} and B_V is suggested depending on the doping in the drift layer. The trade-off relationship can be expressed using drift region doping concentration,, in drift region and the depletion width under the critical electric field,

$$E_C = \frac{qN_d}{\varepsilon_r} W_d \tag{1-4}$$

The blocking voltage under the critical electric field is simply written as follows.

$$B_V = \frac{1}{2} E_c W_d \tag{1-5}$$

Since the resistance of the epitaxial drift layer, R_{on} is obtained using eq. (1-4) and eq. (1-5),

$$R_{on} = \frac{W_d}{q\mu_n N_d} = \frac{4B_V^2}{\mu_n \varepsilon_r E_C^3} \tag{1-6}$$

The denominator of the eq. (1-6), $\mu_n \varepsilon_r E_C^3$, is independent of device dimension and is also used as another index of power device FOM, Baliga's FOM(BFOM) of the material, which is a measure for the material dependence of the on-resistance of unipolar devices.[8] The normalized BFOMs of Si, SiC, GaN and diamond materials are approximately 1, 500, 1300 and 9000 calculated from **Table 1.1.**

Thus, GaN-based devices have desirable properties for the high-power amplification in microwave and millimeter-wave frequency range as well as vertical high-voltage devices that significantly outperform Si-based power devices. According to calculated JFOM and BFOM, diamond seems to possess superior material properties to GaN but the epitaxy of diamond is still developing, and the control of the conductivity in diamond remains to a fundamental issue.[9] Therefore, GaN is today the front contender for next generation high power electronics.

1.2.2 Pros and Cons of Lateral and Vertical Power Devices

Similar to the material selection for high power devices, device architecture is also important to bring out full potential of materials. **Figure 1.1** shows the two typical device architectures for high power device applications. Today, lateral AlGaN/GaN HEMT devices are already in market and used for RF device applications. The main advantage of the lateral devices is that they can be easily integrated onto Si substrate by epitaxial growth since the GaN thickness does not have to be too thick to increase the breakdown voltage and is traditionally accomplished by increasing the lateral gate-to-drain separation. However, increasing the gate-to-drain distance impairs transit time, as shown in eq. (1-2) and also chip size increases with breakdown voltage in lateral devices. Thus, the lateral architecture is suitable for high frequency devices but for very high breakdown voltage, the device structure needs to be modified.

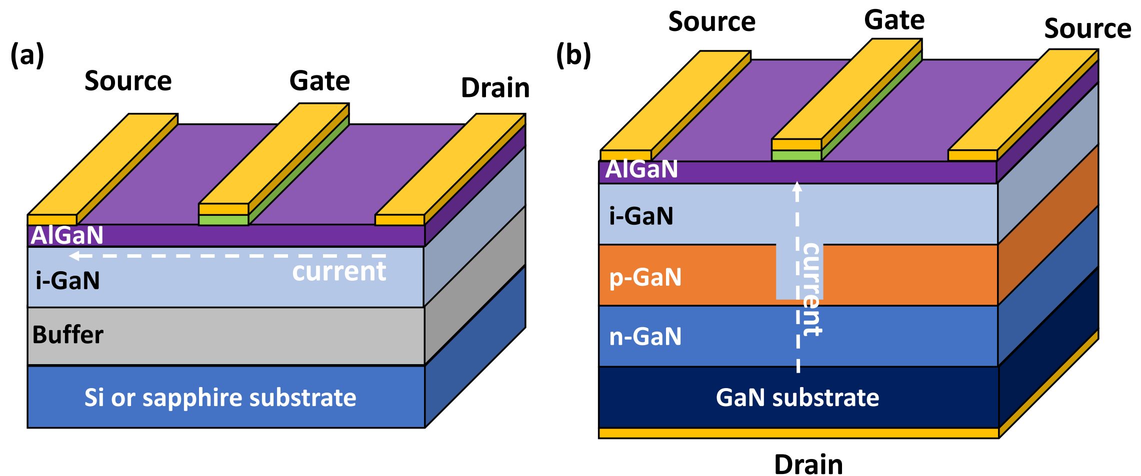

Figure 1.1 Schematic illustration of (a) lateral AlGaN/GaN HEMT and (b) GaN current-aperture-vertical-electron-transistor(CAVET).

Figure 1.1 (b) shows GaN vertical power device structure, where the current flows vertically from the source and is extracted by the drain contact at the bottom of wafer. With this device architecture, the voltage is held across the film and the breakdown voltage can be increased simply by increasing the thickness of the drift layer without compromising the chip area. Also the vertical current conduction alleviates the current collapse which remains a challenge in GaN HEMT devices due to current conduction near the interface of AlGaN/GaN.[10] Therefore, the vertical architecture is more suitable for high voltage and high current application. The challenge, however, is that the growth of sufficiently thick epitaxial GaN film on Si is extremely difficult, as will be discussed in section 1.3.1.

1.2.3 Requirement for Vertical Power Device

In vertical devices, to simultaneously enable a low on-resistance, fast switching, and high breakdown voltage, the drift layer n-type doping has to be low at a level around 1×10^{16} cm^{-3} or lower and has to be sufficiently thick. **Figure 1.2** shows relationship between doping concentration and breakdown voltage as a function of drift layer thickness.[11] It can be noted that the breakdown voltage cannot be larger than 120 V if the carrier concentration is higher than 1×10^{17} cm^{-3} regardless of the thicknesses of the drift layer. This is because the strong electric field needs to be held across the thickness and the depletion region thickness decreases with impurity concentrations.

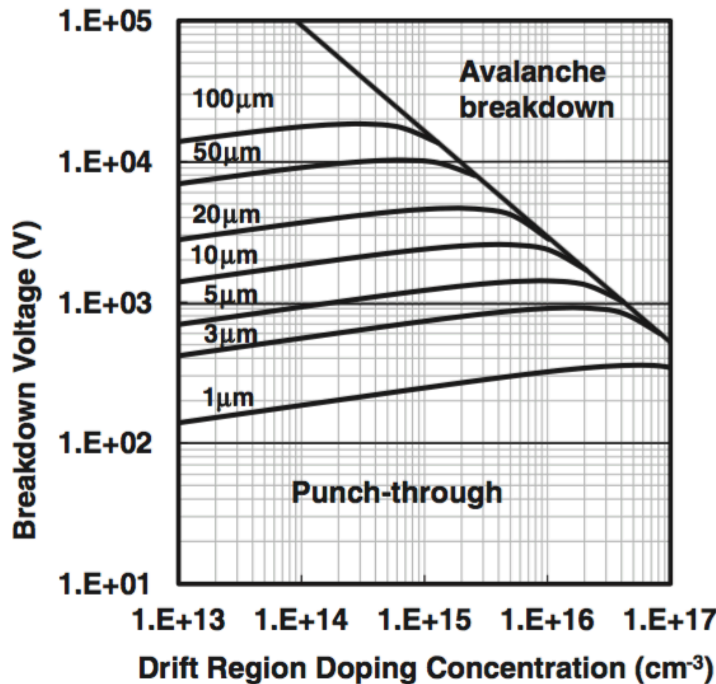

Figure 1.2 Breakdown voltage vs drift region doping concentration for each drift layer thickness from 1 to 100 μm.[11]

The breakdown voltage is typically chosen to be as twice as high than maximum voltage of the high voltage module. For example, electric vehicles (EVs) use many power modules such as DC-DC boost converter to drive the main motor at maximum voltage of 650V which requires the breakdown voltage to be higher than 1.25 kV. A compressor in the air conditioner is driven by an inverter with the battery voltage of 200–300V which requires 400-600 V of breakdown voltages. Therefore, if the GaN power modules are used in EVs, doping concentrations that are less than cm^{-3} are required. In addition, for breakdown voltage devices higher than higher than 1kV, the thickness has to be more than 10 μm. Both of these requirements are very challenging for heteroepitaxial GaN and are the main focus of this dissertation.

1.3 Challenges for GaN Vertical Power Device on Si

As discussed in section 1.2.3, GaN high power vertical devices require (i) thicknesses greater than at least 10 μm to hold 1kV and (ii) carrier concentration lower than 1×10^{16} cm^{-3} to provide sufficient depletion layer thickness to hold the voltage. Recent trend for GaN high power devices are the use of bulk GaN substrate thanks to the development of many wafer growth techniques.[12–14] The dislocation density of the GaN wafer is now becoming lower than 10^6 cm^{-2} and the subsequent growth of GaN drift layers by MOCVD enabled very thick and low carrier concentration GaN for vertical power devices.[15,16] However, as shown in **Table 1.2**, the cost of bulk GaN is still 1000 times higher than Si which is still very expensive for GaN to be employed in utility tools. Therefore, integration of GaN to cheap substrates is the long-cherished goal for the power device community.

In this section, we will discuss the fundamental issues of GaN-on-Si hetero-integration for meeting the vertical power device requirements.

Table 1.2 Implications of the usual substrate materials for the GaN-epitaxy (data relative to the GaN properties.[6]

Substrate	Bulk GaN	4H-SiC	Sapphire	Silicon
Lattice mismatch	none	+3.5%	-16%	-17%
Thermal mismatch	none	+33%	-25%	+116%
Electrical resistance	low	low[a]	∞	low[a]
Thermal resistance	same	0.3 [a]	3	0.9
Available wafer size	2”(3”)	4”(6”)	Up to 8”	any
Cost, $/cm^2	100	10	1	0.1

[a] Only non-conductive interface for successful heteroepitaxy of GaN

1.3.1 Thickness limitation due to Thermal Mismatch Between GaN and Si

Si is the most technically developed wafer and is also available with cheap price in market. Therefore, the ultimate goal is always to integrate newly materials on the Si substrate. The MOCVD growth of GaN on Si has been extensively studied and many issues were solved such as melt backing, which is caused by strong reaction between Ga and Si at high temperature, and lattice mismatches.[17] However, as shown in **Table 1.2**, a huge difference in coefficient of thermal expansion(CTE) between GaN and Si (+116% relative to the GaN) results in severe cracking in the film if the thickness exceeds 5 μm on top of Si[17] which is not thick enough for high voltage device applications.

The typical approach to overcome the mismatch is using well optimized AlGaN/AlN buffer layer to intentionally induce compressive stress to the film at the growth temperature. Once the growth is finished at tempeatures exceeding 1000 $^{\circ}$C, as the whole GaN-on-Si system cools down, the GaN film experiences tensile stress due to the CTE mismatch. As a result, the residual stress at the room temperature can be close to initial values due to the intentionally introduced and stress-compensating layers. Raghavan and Redwing summarized the relationship between stress and thickness under different buffer layer conditions. (**Figure 1.3**).[18] They achieved crack-free 1 μm thick GaN on Si with using a graded 1 μm thick AlGaN buffer. However, achieving a thickness greater than 10 μm is very challenging with this technique.

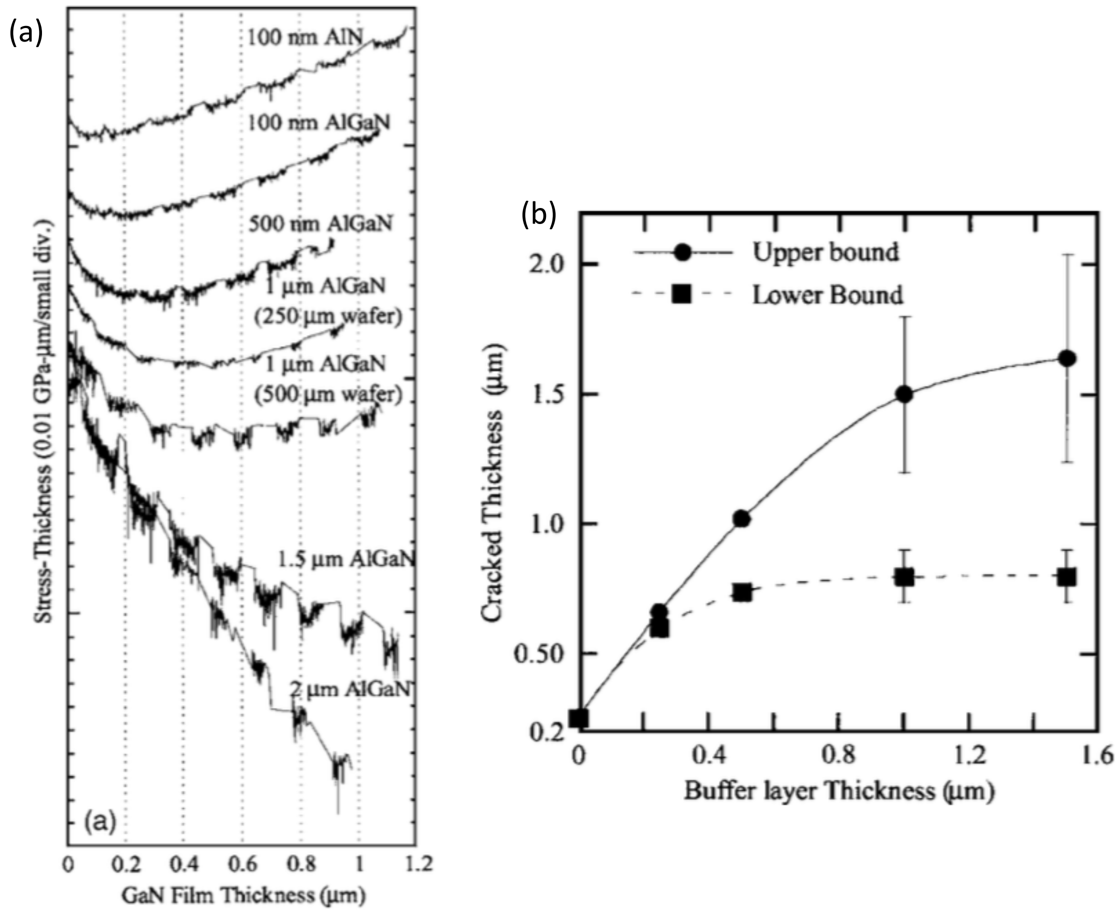

Figure 1.3 **(a)** Stress in GaN film as a fuction of the thickness. The AlGaN buffer layer thickness decrease the increment of tensile stress generation. **(b)** Critical thickness of GaN for cracking as a function of buffer layer thickness.[18]

Another alternative to integrate GaN on Si is to grow the thick GaN film on a different substrate (donor) and to perform wafer bonding to a host Si substrate. Misky et al demonstrated a successful lift-off of GaN film from sapphire substrate using laser excitation.[19] The GaN and sapphire were separated due to the thermal decomposition of GaN at the laser focal point (typically the GaN/sapphire interface) and the GaN film is transferred to silicone elastomer. This process can also be used for producing a free standing GaN wafer and they succeeded in lift-off of 300 µm GaN from the sapphire substrate. However, since this is a physical lift off from the sapphire wafer, it impairs surface condition of GaN which will be extremely important for high power applications.

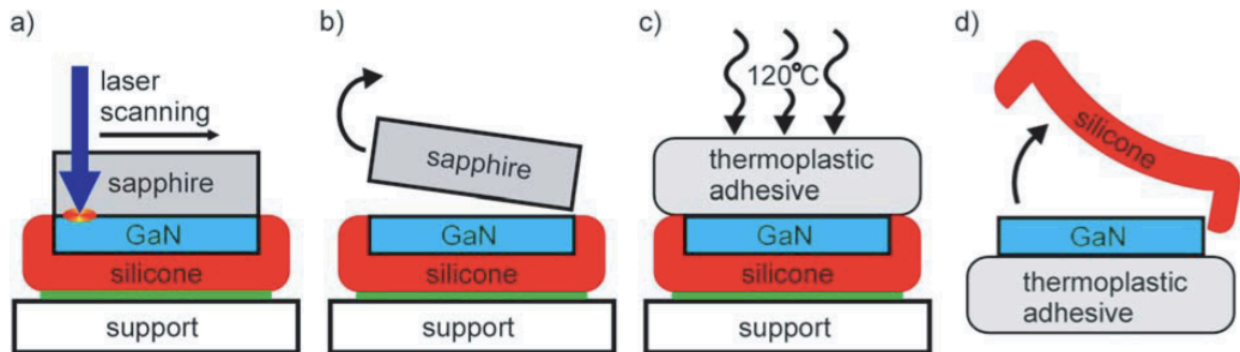

Figure 1.4 Process sequence for the laser lift -off of 2” GaN membranes. **(a)** Laser lift-ff of the GaN film from sapphire; **(b)** sapphire removal; **(c)** deposition of a ~3mm thick layer of thermoplastic adhesive at 120 °C; **(d)** peel-off of the silicone elastomer.[19]

Selective area growth(SAG) technique has also been used for GaN device application especially for LEDs. SAG is carried out typically by depositing a dielectric layer followed by making openings in the region where GaN is to be grown. Because the area of GaN is smaller and continuous over the whole wafer, wafer bowing effect due to thermal mismatch can be minimized in SAG GaN. Kei-Mei Lau et al have demonstrated using SAG a 2 µm thick crack free GaN blue LED in an area of 300 µm × 300 µm on Si.[20] Honda et al. reported 1.5 µm thick crack free SAG GaN on Si with 200 µm × 200 µm.[21] They observed cracking in 500 µm × 500 µm window for the same thickness of GaN, which indicates that the critical thickness of crack free GaN is dependent on the SAG GaN area. However, again these thicknesses are still much smaller than that required for vertical power devices. Despite these advances, it was still very difficult to integrate over 10 µm GaN on Si without introducing damage on the surface. However, among these techniques, SAG has not been extensively studied especially for device applications beyond those for LEDs. One interesting observation that we noticed through these literature reviews is that the crack formation of SAG GaN film generally nucleated at the corner of square widows which have been extensively used in SAG GaN growth in previous work (**Figure 1.5** and **1.6**). This observation motivated us to revisit the SAG mask shapes which are optimal for minimizing stress at the SAG interface (Chapter 3). Therefore, in this dissertation, we focus on SAG GaN to achieve thick and crack free GaN on Si to meet the high-power device requirements.

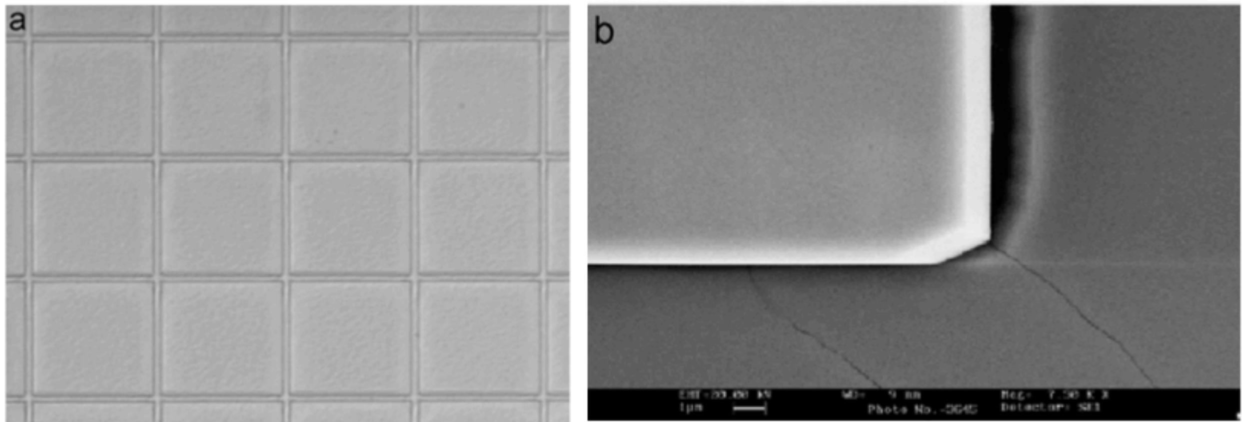

Figure 1.5 (a) Microscope image of as-grown LEDs layer on patterned Si substrate. **(b)** Top-view SEM image of GaN on patterned Si substrate.[20]

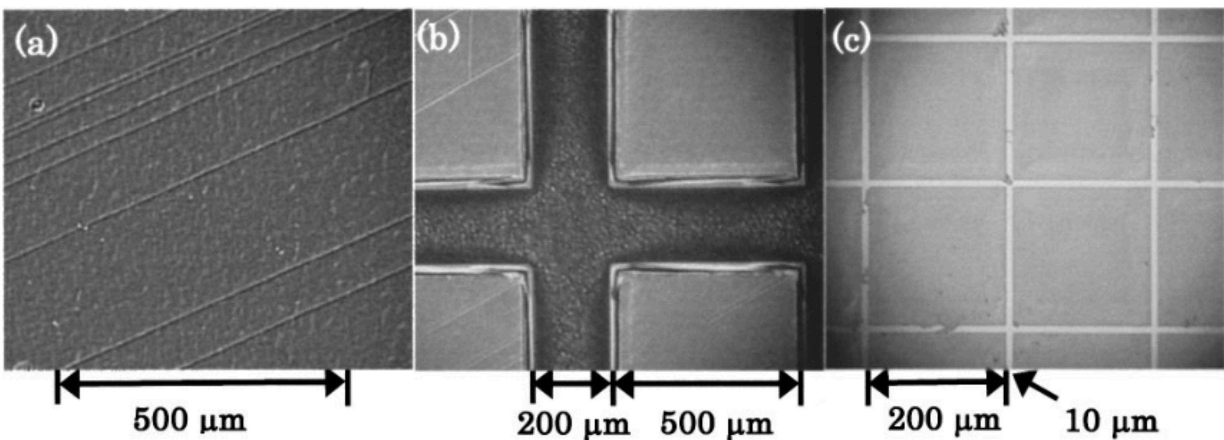

Figure 1.6 Microscope image of SAG GaN/AlN/Si. **(a)** GaN film grown without grid mask. **(b)** GaN grown on 500 µm wide square windows with 200 µm wide masks. **(c)** GaN grown on 200 µm square windows with 10 µm wide masks.[21]

1.3.2 Unintentional Doping of GaN in MOCVD and Selective Area Growth (SAG)

Similar to the thickness, the carrier concentration in power device applications is extremely important because it affects both of device on- and off-characteristics. For GaN growth, unintentional doping (UID) of GaN is a very well-known issue and the origin still has been under investigation. Because of the UID of GaN, MOCVD grown GaN is always n-type doped at a range between 1×10^{15} cm^{-3} to 1×10^{18} cm^{-3} depending on the growth conditions and substrates. In 1960s, it was believed that n-type doping was associated with nitrogen vacancies in GaN because of the vapor pressures of nitrogen required to stabilize GaN at high temperatures.[22] By early 1980s, Seifert et al. showed that the carrier concentration is dependent on oxygen impurities in nitrogen sites in GaN, O_N, and it could be reduced by improving the purity of the NH_3 source material.[23] Later, Neugebauer and Van de Walle argued using first-principles calculations that the nitrogen vacancies in GaN cannot explain the carrier concentration present in unintentionally doped GaN film that was higher than 10^{18} cm^{-3}.[24] They concluded that the source of high carrier concentration is from Si and O impurities incorporated during GaN growth. Today, the origin of the unintentional doping is believed to be associated with Si and O impurities either from the chamber, source gases or substrate materials. For even decreasing the carrier concentration lower than 1×10^{16} cm^{-3}, co-doping technique is used to compensate the donor type impurities with acceptor type impurities such as carbon or iron.[25,26] However, one needs to be careful of the concentration of the carbon impurities since it also increases the leakage current.[27]

UID in SAG GaN is more severe and complicated because SiO_2 and SiN_x is typically used as growth masks and decomposed at high growth temperature. In selective area growth, the source of impurities is typically attributed to (i) impurities incorporated from the regrowth interface after opening SiO_2 window[28], (ii) diffusion of Si and O atoms from the SAG mask or substrate.[29–34] If

only these two are the source of impurities in SAG GaN, increasing GaN thickness should result in low carrier concentration at the surface of GaN since both of the sources are confined near the regrowth interfaces.

Thus, we can assume that increasing thickness of GaN-on-Si would also benefit lowering carrier concentration of the GaN which are desirable for vertical power devices.

1.4 Overview of the Dissertation

The ultimate goal of the work conducted for the preparation of this dissertation is to fabricate GaN vertical power devices on Si with the drift layer thickness exceeding 10 µm, which may also result in low carrier concentration of the film due to reduction of impurity incorporations.

In chapter 2, we discuss systematic mechanistic studies of SAG GaN. The growth mask with different spacings and diameters enabled us to study geometrical effects on SAG GaN growth thickness, facet evolution and lateral growth rate. The chapter is concluded with the application of SAG GaN technique to enhance light extraction of GaN-based LEDs.

Chapter 3 documents the main results of this dissertation in which we discuss approaches to achieve thick GaN on Si using the knowledge acquired from the chapter 2. We associated the cracking mechanism in SAG GaN-on-Si to hexagonal growth facet evolution and strain-sharing with crack-planes and successfully grew 19 µm thick GaN-on-Si. The thick growth of GaN also helped annihilate threading dislocations and enabled GaN vertical metal-semiconductor-insulator-FET (MISFET) for the first time on a Si substrate.

In chapter 4, we performed additional systematic experiments to study phenomenon of dislocation annihilation as a function of GaN thickness on different substrates, namely GaN, Si

and QST. The systematic experiments revealed that the number of dislocations reduced with thicknesses. We fabricated vertical Schottky diodes on all substrate types and we achieved 400 V breakdown voltage on the QST substrate. We found that the background carrier concentration was not dependent on the thickness and was influenced by the placement location in the SAG pattern. At the time of writing of this dissertation, the control over the background concentration in SAG remains to be a challenge and further studies need to be conducted to understand the origin of impurities in SAG GaN.

This dissertation covers critical aspects of the GaN research from development of material growth to the fabrication and characterization of test device structures and to the fabrication and analysis of fundamental device properties in GaN devices.

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Chapter 2

A Comprehensive Analysis of GaN Selective Area Growth: Size Effects and Influence on Light Extraction from GaN Light Emitting Diodes

2.1 Introduction

The selective area growth (SAG) of III-V compound semiconductor materials has been studied for decades because of its numerous advantages in controlling the growth structure and morphology.[1–6] Most notably, SAG allows the reduction of threading dislocations at the grown surface by trapping and bending with lateral overgrowth[5,7–12] and it allows accommodation of thermal stresses during heteroepitaxial growth.[13,14] The SAG of arsenide and phosphide III-V materials has been analyzed quite extensively but less studies were reported for nitride materials except for nano-scale mask openings and spacings.[6,7,9,15–21] The interest in submillimeter scale heteroepitaxy and SAG have witnessed recently increased interest for large scale integration of light emitting diodes (LEDs)[22–24] and the development of high power devices.[25–31] It is therefore timely to conduct detailed and systematic studies of the SAG of GaN in submillimeter scale mask

openings. The deep understanding of geometric effects for SAG is necessary for the application to versatile devices, particularly when device scaling and their array density become relevant.

In this work, we conducted SAG GaN in oxide masks in previously unexplored geometries of circular openings with 20 μm to 450 μm diameters and edge-to-edge spacings on a 2” c-plane sapphire wafer (**Figure 2.1**). With systematic observation by scanning electron microscopy (SEM) and thickness profilometry, we characterized the SAG GaN on sapphire both qualitatively and quantitatively using mass-transport limited growth models. To exploit the morphological control attained here at different opening diameter and spacing, we fabricated GaN/InGaN quantum well LEDs and demonstrated 2.5 times enhanced light extraction with carefully engineered structures.

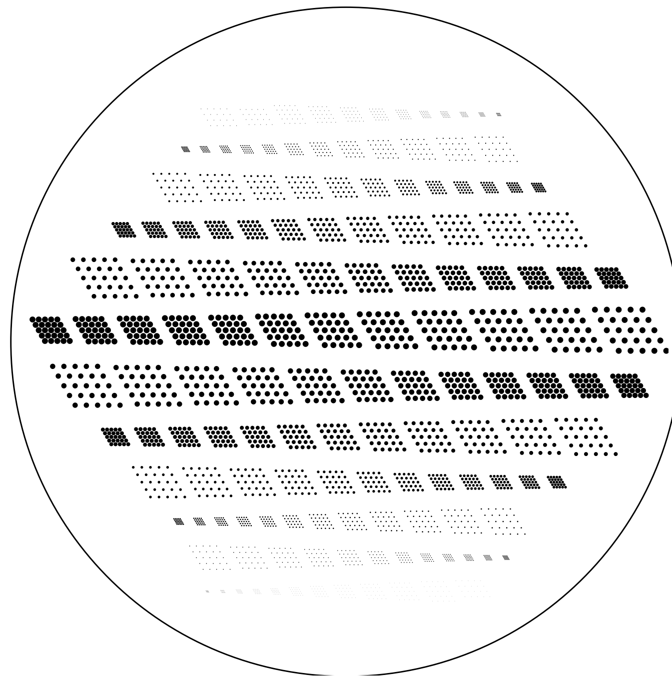

Figure 2.1 Photomask design for SAG GaN on 2 inch wafer. These arrays of circular patterns consist of 12 different edge-to-edge spacings for each of 12 different diameter dots, resulting in 144 different array patterns in total. The patterns on the photomask can fit in a single 2 inch wafer, which provides a side-by-side comparison for all investigated parameters and allows us to minimize experimental sampling errors.

2.2 Experimental Details

For the growth of SAG GaN films, we utilized a 3 x 2" Thomas Swan/Axitron close-coupled showerhead (CCS) metal-organic chemical vapor deposition (MOCVD) system with trimethylgallium (TMGa) and ammonia precursors, and H_2 carrier gas. To circumvent surface preparation effects on nucleation in different size/spacing patterns, we first grew a 1 μm thick GaN buffer layer on a single 2-inch c-Al_2O_3 (sapphire) wafer. A 200 nm thick SiO_2 layer was then deposited on the wafer surface by plasma enhanced chemical vapor deposition (PECVD) at 350 °C and conventional photolithography then followed in order to pattern 144 different hexagonal arrays of circular openings, which consist of combinations of 12 different mask openings and edge-to-edge spacings (**Figure 2.1**). The mask openings and spacings in SiO_2 were varied from 20 μm to 450 μm, and were etched by a diluted buffered oxide etch (BOE) with a 6:1 volume ratio of 40 % NH_4OH in water to 49% HF in water. The exposed GaN surface was treated with hydrochloric acid (HCl) solution (36 - 38 %) at 60 °C for 3 min in order to remove native gallium oxides (Ga_xO_y).[32] We carried out the SAG on these wafers at a temperature of 1050 °C which was calibrated at the susceptor surface, and a chamber pressure of 100 mbar for 1 hour. A V/III ratio of 2250 was employed for the SAG, which corresponds to a planar growth rate of 1 μm/hour on 2-inch c-Al_2O_3 (sapphire) wafer. This mask pattern allowed us to eliminate sample-to-sample fluctuations of the growth and consider only geometrical effects on GaN SAG. The morphologies of the grown structures were characterized by scanning electron microscope (SEM) and Dektak surface profilometer. In addition, the growth for different times with fixed growth conditions was conducted to observe facet evolution with time.

Post growth rate, dopant, and metal-contact optimization, and to demonstrate the engineering aspects of our geometric SAG studies, we tailored the growth structure to control the

morphologies of InGaN/GaN multiple quantum well (MQW) blue LEDs that exhibited greater light extraction effects. Their electroluminescence(EL) characteristics were determined using a DU420A-OE Andor charge coupled device (CCD) camera mounted on an Oriel instrument cornerstone 260 motorized 1/4m monochromator and using a National Instruments interface control board with Labview automated measurements. The high-resolution transmission electron microscopy (HRTEM) characterization was performed in an FEI Tecnai F30 300 kV microscope for the well-faceted and non-faceted samples for investigating the MQW structures.

2.3 Generic Geometric Effects in SAG GaN on c-Sapphire

We first systematically characterized the SAG GaN with different mask openings and spacings by top-view(**Figure 2.2**) and glanced angle(**Figure 2.3**). The 45° angled-view SEM images showed strong size and spacing dependence of the vertical growth rate manifesting clear geometrical effects in the SAG GaN on sapphire at such submillimeter scales. For a given opening diameter, the overall height of the GaN structure was increased with increasing mask spacing accompanied by a significant increase in the dot edge height. A concave shaped surface morphology evolved as the mask spacing was increased. The dot edges always exhibited larger heights than the center indicating more adatom arrival and incorporation at the mask edges. Similarly, for a given spacing, the heights of the SAG GaN structure decreased with increasing the mask diameter.

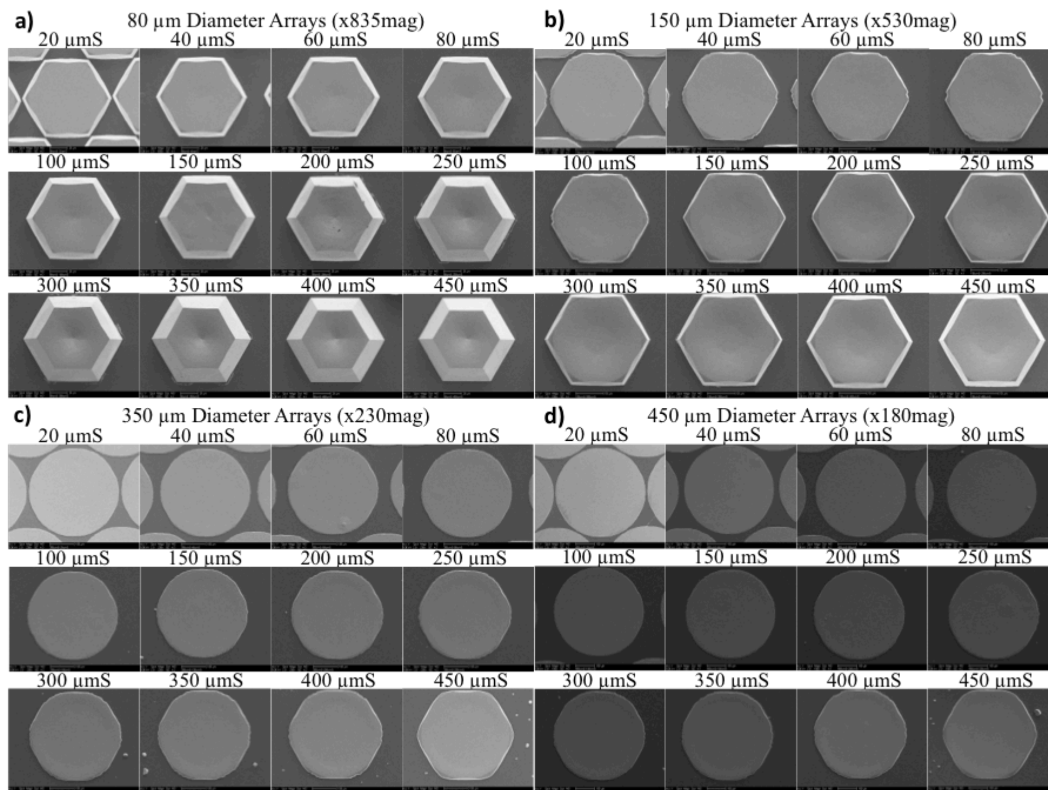

Figure 2.2 Top view SEM images of the SAG GaN structures for different mask openings (a) 80 μm, (b) 150 μm, (c) 350 μm, and (d) 450 μm for edge-to-edge spacings in the range of 20 μm to 450 μm.

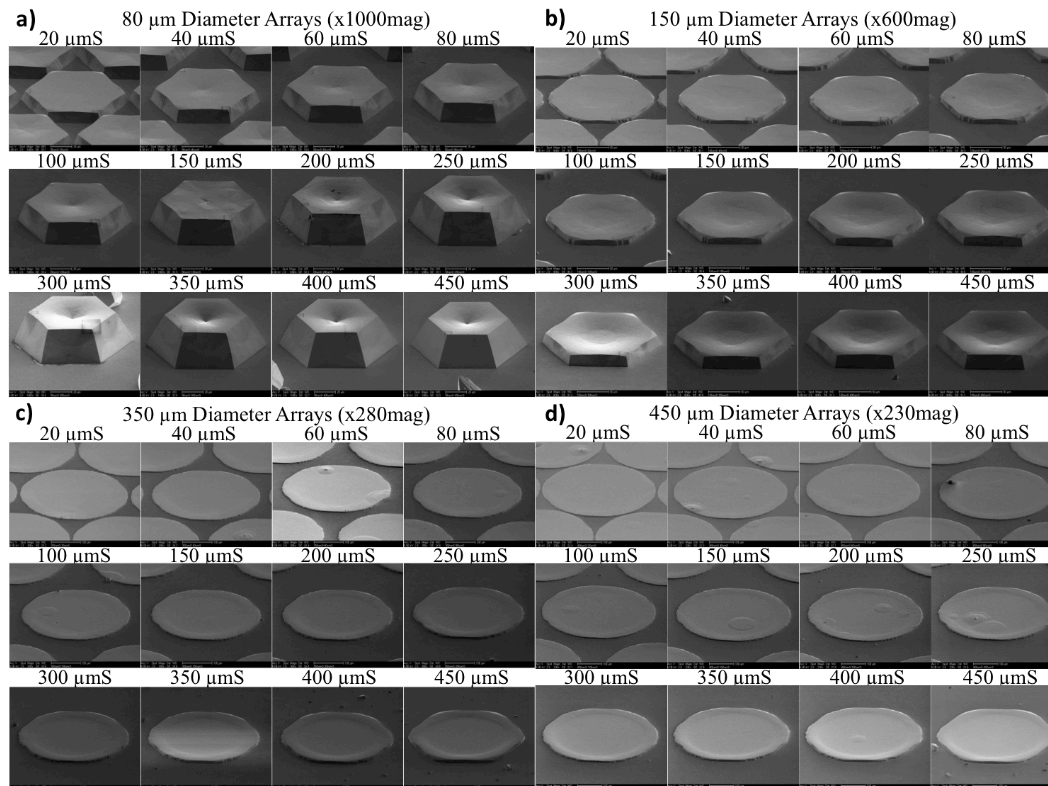

Figure 2.3 45°-angled SEM images of the SAG GaN structures for different mask openings (a) 80 µm, (b) 150 µm, (c) 350 µm, and (d) 450 µm for edge-to-edge spacings in the range of 20 µm to 450 µm. Strong vertical growth rate enhancement was observed for all diameters and spacings.

For quantitative comparison, the heights of the grown structures were measured by surface profilometry and plotted with respect to mask dot diameters and spacings in **Figure 2.4**. To eliminate pattern array edge effects, we chose for our analysis the center dot from each of the 5x5 hexagonal array patterns and measured the dot height profile along with $<1\bar{1}00>$ direction. From the fixed spacing data (**Figure 2.4 (a)**) we observed a remarkable growth rate difference for different dot diameters. The center height of the 40 μm diameter (referenced thereafter as μmD) dot was found to be 4 times taller than that of the 400 μmD at 20 μm spacing (referenced thereof as μmS). Edge effects are defined as growth processes that lead to strong growth rate and morphological anomalies compared to that of thin film. For example, concave-shaped surface morphology becomes prominent at larger dot diameters and larger spacings as discussed later. From **Figure 2.4 (a)**, the edge height for the 400 μmD is twice as high as its center. For sufficiently small diameters (<80 μm), the concave-shaped surface morphologies are generally minimal and become visible for larger spacing as can be observed in **Figure 2.3 (a)**. For dot diameters larger than 60 μm, concave-shaped surface morphology was observed as shown for the 150 μmD in **Figure 2.3 (b)**. The flatness of the surface was improved for larger diameter dots as shown in **Figure 2.3 (c)** and **Figure 2.3 (d)**.

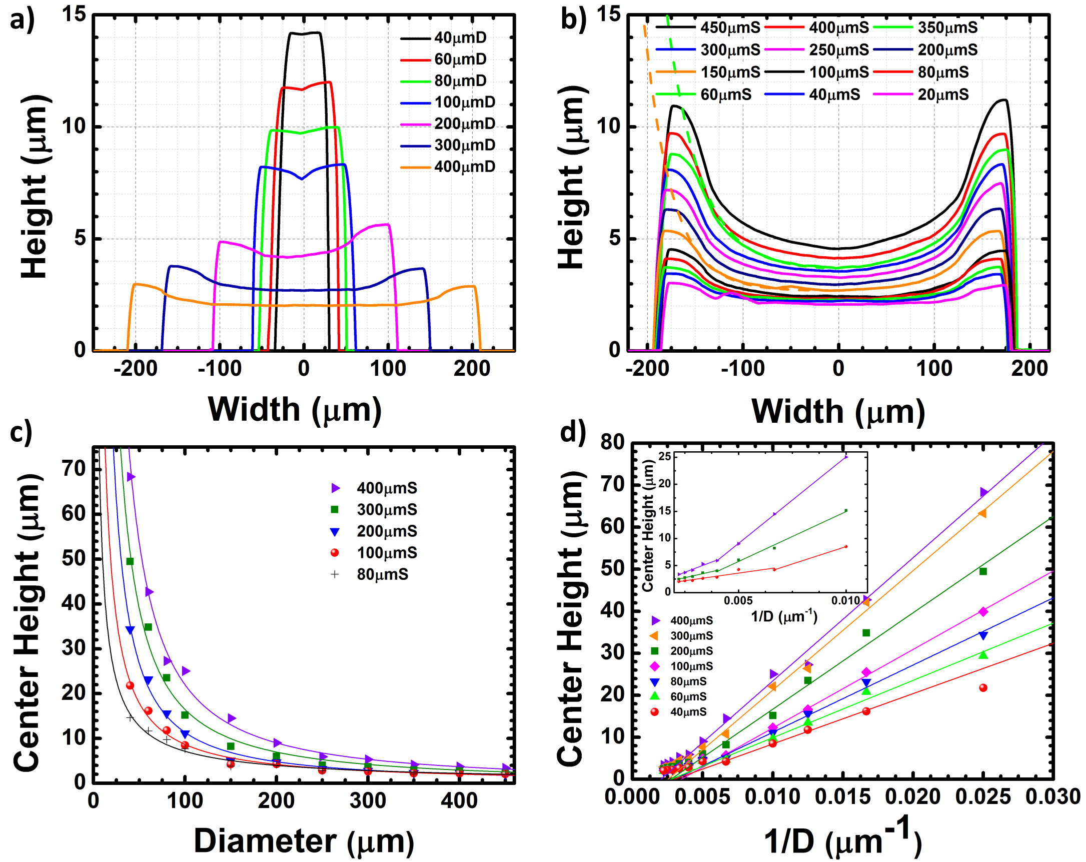

Figure 2.4 Surface profilometry on the grown structure with (a) fixed spacing at 20 μm and (b) fixed diameter at 350 μm. The solid lines represent the measured thickness profile and dashed lines are fitted lines for 350 μmS and 150 μmS dots to extract the Ga adatom diffusion length. (c) The heights of the grown structures as a function of the mask diameters and (d) the inverse of the mask diameters; the inset highlights the large diameter region of the plots.

2.3.1 Gallium Adatom Diffusion Length on GaN Surface

The above observations can be explained by the relative scales of pattern radii and the Ga adatom surface diffusion length on the c-plane GaN dot surface. If the Ga diffusion length is larger than the dot radius, the Ga adatom adsorbing/arriving at the edge of the dot can reach the center of the dot leading to a nearly flat dot surface. In contrast, if the Ga diffusion length is smaller than the radius of the dot, Ga adatoms impinged at the dot edge cannot make it to the dot center, resulting in nonuniformity of the dot height across its diameter. If the dot radius is much larger than the Ga adatom diffusion length, the height gradient will be limited to the edges of the dot that extend over a distance that is comparable to the Ga adatom diffusion length on the c-plane GaN surface, and the center region will be nearly flat. To extract the Ga adatom surface diffusion length, we utilize the formulation developed by Rozhavskaya et al. who considered the edge effects on the growth rate of GaN stripes and extracted Ga adatom diffusion length to be in the range of 5 µm to 24 µm.[33] In the 1D approximation along the diameter of a GaN dot, the solutions for the diffusion equation accounting for impinging flux and desorption of Ga adatoms from the GaN surface together with the two boundary conditions of a constant Ga adatom density at the dot center and zero density at the dot edge yield:[33]

$$\frac{H(x)}{H_{max}} = \frac{sinh(R/\lambda) + (\lambda_0/\lambda)\, cos[(R\text{-}x)/\lambda]}{sinh(R/\lambda) + (\lambda_0/\lambda)\, cos[R/\lambda]} \tag{2-1}$$

Here, R is the original mask dot radius, $\lambda = \sqrt{D\tau}$ is the incorporation-limited diffusion length of Ga adatoms on the GaN surface and λ_0 is the diffusion length on the dot side facets. For simplicity in the extraction of the diffusion lengths, we assume that the usually different diffusion length on different planes to be identical on our GaN dot top surface and sidewalls ($\lambda = \lambda_0$). The measured plots with fitting curves using equation (2-1) are shown in **Figure 2.4 (b)** with corresponding extracted values listed in **Table 2.1** to be 29 µm - 35 µm. The extracted diffusion

length has implications on the synergetic effects during the GaN SAG. For the same spacings and different diameters, the smaller diameter dot has a higher diffusion length. For the same diameters, the diffusion length increases with spacing. In our experiment, the growth conditions are the same such that the input molar fraction of precursors is identical. Thus, the difference in the diffusion length results from the mask geometry itself rather than the growth conditions as observed by Rozhavskaya et al. .[33] By changing the mask geometry, the local V/III ratio at the mask edge can change. For larger spacings, the larger collection area of Ga adatoms on the SiO_2 mask leads to more Ga diffusion to the growth interface and the effective V/III ratio at the mask edge decreases. Similarly, for smaller diameters, the relative ratio of the dot area to the collection area on SiO_2 is smaller resulting in enhanced Ga concentration at the edge and lower effective V/III ratio. Naturally, it is more likely for Ga adatoms to react with NH_3 when the V/III ratio is higher, which decreases the Ga adatom diffusion length. These trends agree well with those previously observed in the SAG of InGaAs.[34]

Table 2.1 Diffusion lengths for selected different mask geometries

Mask geometry	Extracted diffusion length (µm)
350 µmD 150 µmS	29
350 µmD 350 µmS	33
80 µmD 350 µmS	35

The surface nonuniformity became significant when the diameter of the openings were equivalent to or larger than the diffusion length of Ga on GaN surface. Therefore, this edge enhanced growth effect is specific to SAG in wide patterns. The thickness variation throughout the structure will affect the material thickness in critical regions of devices, such as in quantum wells, which can be detrimental to their performance and should be suppressed. Based on these observations, wider mask openings and tight edge-to-edge spacings would be the best-suited SAG geometries that can be utilized for attaining uniform device morphologies.

2.3.2 Diameter Dependent Vertical Growth Rate

To quantitatively analyze the size-dependent vertical growth rates in SAG GaN on sapphire, we need to fully account for reactant direct impingement as well as their mass transport on both the SiO_2 and the GaN surfaces to the growth interface. This is customary for whisker[35] and nanowire[36,37] growth and has been employed recently in the GaN SAG.[38] The reactant impingements on the top surface of the opened GaN surface, J_{top}, surface diffusion length of the reactants on SiO_2, λ_{sub}, surface diffusion of the reactants on GaN sidewall, λ_{sw}, and gas phase diffusion flux from the substrate and impingement on the sidewall surface, J_{sw}, all contribute to SAG GaN growth rate.[38] It is also important to note that the SAG occurs simultaneously normal to and parallel to the substrate surface, typically referred to as vertical growth and lateral overgrowth, respectively. For same diameter areas, the increase of lateral overgrowth is relatively small and can therefore be ignored. The lateral overgrowth rate as a function of diameter and spacing is discussed in section 2.3.4. With these considerations, the growth rate in SAG can be written as:[38]

$$\frac{dV}{dt} = \frac{\pi}{4} D^2 \frac{dH}{dt} = \gamma_{top} D^2 + \gamma_{sw}(t) D + \gamma_{sub}(t) \qquad (2\text{-}2)$$

Where V is the volume of the GaN dot, H is the height, D is the diameter, γ_{top} is a time independent constant related to top surface impingement, and γ_{sw} and γ_{sub} are time dependent impingement and adsorption parameters and are constant in our case due to the fixed growth time of 1 hour. γ_{sw} in our experiment is however dependent on facet development which varies with size and spacing as deduced from **Figure 2.2** and **Figure 2.3**. Therefore, the vertical growth rate dependency should be characterized with the following equation:

$$\frac{dH}{dt} \propto \gamma_{top} + \frac{\gamma_{sw}(t)}{D} + \frac{\gamma_{sub}(t)}{D^2} \qquad (2\text{-}3)$$

In **Figure 2.4 (c)** and **Figure 2.4 (d)**, we plotted the SAG GaN dot center height as a function of mask opening diameter and inverse diameter, respectively. The fitted lines in **Figure 2.4 (c)** are proportional to $1/D^{\beta}$ where $1 \leq \beta \leq 2$. **Figure 2.4 (d)** shows further details of the diameter dependence and its inset highlights the large diameter region where we see a transition from $\beta = 1$ for small diameters to $\beta = 2$ for large diameters. From equation (2-3), we can deduce that the sidewall diffusion coefficient γ_{sw} dependence dominates the SAG dot growth height. The larger spacing dots had heights with larger slopes ($\beta = 1$) as a function of inverse diameter because the diffusion of Ga is more favorable as shown in **Table 2.1**. The systematic SEM images in **Figure 2.2** and **Figure 2.3** demonstrated that the growth facets for larger dot diameters were not well developed whereas the growth facets for smaller dot diameters were well developed for all spacings. The non-flat and not well-developed facets impede Ga adatom diffusion on the sidewall and slow down the increase in the vertical height with inverse diameter whereas well-developed facets led to an increased slope of the height with inverse diameter.

2.3.3 Spacing Dependent Vertical Growth Rate

In addition to the strong size effects, the array edge-to-edge spacing was found to have significant influence on the vertical growth rate of SAG GaN as illustrated in **Figure 2.5 (a)**. The smaller diameter dots exhibited two different slopes with spacing whereas the height for the larger diameter dots showed weaker yet a fixed linear increase with spacing. This can also be explained by the relative difference between the Ga diffusion length which we extracted to be ~30 µm on the GaN surface and the GaN dot height. When the thickness is less than 30 µm, the collection area of SAG GaN structure increased with spacings because most of the impinging Ga adatoms on the GaN dot sidewall can diffuse on the sidewall and reach the growth interface at the top GaN surface. However, when the thickness becomes larger than 30 µm, the collection area of SAG GaN structure remains fixed within 30 µm from the top surface. The fixed collection area leads to an overall reduction of the rate of increase of the height with spacing than for thinner dots. This also corroborates with our earlier discussions that for smaller dot diameters, the Ga adatom surface diffusion lengths are high due to a lower effective V/III ratio at the dot edges. This size enhanced growth rate for smaller diameters diminishes when the collection area becomes constant (**Figure 2.5 (d)**) leading to a transition from sharp increase of growth height with spacing to slower increase at larger spacings when the dot height exceeded 25-30 µm.

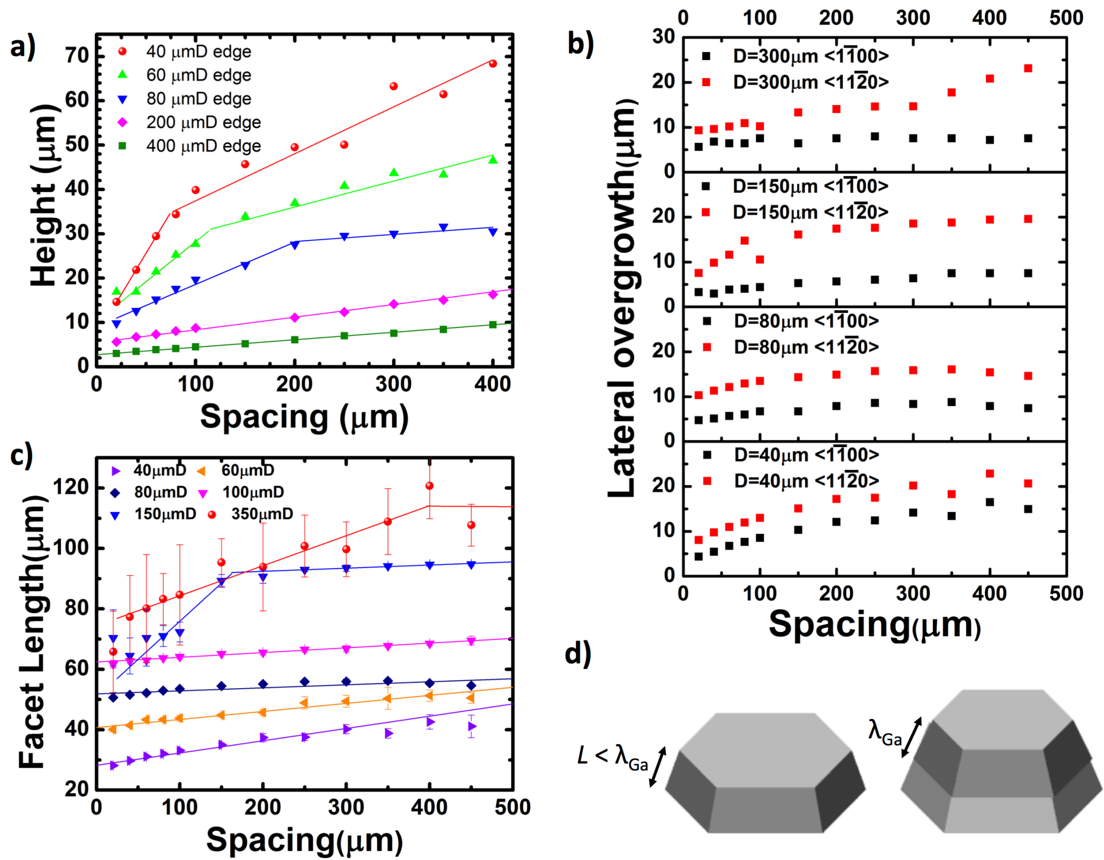

Figure 2.5 (a) Edge heights for the grown structures. (b) The lateral overgrowth lengths and (c) the facet lengths as a function of the mask spacings. The facet lengths are defined as the average length of the six sides of the grown hexagon base. (d) Schematic illustration of the collection area contributing to the vertical growth when the sidewall length is less than or equivalent to Ga diffusion length on GaN (left) and when it is larger than the diffusion length (right).

2.3.4 Spacing Dependent Lateral Growth Rate, Facet Length and Facet Evolution

Not only the vertical growth rate but also lateral overgrowth rate depends on the spacing. **Figure 2.5 (b)** shows the lateral overgrowth length as a function of the mask spacing. The lateral overgrowth length was determined by subtracting the original circular opening from the total length for each of $<1\bar{1}00>$ and $<11\bar{2}0>$ directions of the SAG GaN. As can be seen in **Figure 2.5 (b)**, the lateral overgrowth length depends on the growth direction. The growth in $<1\bar{1}00>$ direction usually has less lateral length than that in the $<11\bar{2}0>$ direction. The $\{1\bar{1}01\}$ facets have low surface energies[39,40] and the GaN circular dot transforms its shape to a hexagonal dot to reduce the total surface energy by developing these $\{1\bar{1}01\}$ facets that exhibit lower growth rate. Therefore, in order to understand the lateral overgrowth rate, we need to take into consideration the facet formation. **Figure 2.5 (c)** shows a plot of the facet length as a function of the mask spacing. We define the "facet length" as the average length of the six sides of the grown hexagon that were measured by SEM. For smaller diameters, the change of the facet length with spacing is weak and can be fitted with a single line. In contrast, for larger diameters, the facet length increases sharply with spacing and then plateaus for larger spacings. The slopes in the plateau region for larger diameter and larger spacing are similar to those for the smaller diameter. This can be explained with the facet development as a function of diameter and spacing that was characterized with top-view SEM (**Figure 2.2**) and plotted in **Figure 2.6**. The facet was defined as "developed" for structures that had no rough surface and with six complete and sharp facets. From **Figure 2.6**, we can find that there are well-defined transition points from well-developed to non-developed facets which corroborate with the transition points from non-saturated facet growth to saturated facet growth in **Figure 2.5 (b)** and **Figure 2.5 (c)**. For instance, the facet of the dots with a 150 µmD developed for spacings larger than 150 µm from **Figure 2.6** and in **Figure 2.2 (b)**, and the slope

of <11$\bar{2}$0> lateral overgrowth changed at the spacing 150 μm in **Figure 2.5 (b)**. Additionally, smaller diameter dots which already had developed complete facets for all spacing as listed in **Figure 2.6** exhibited a fixed and small slope for the facet length as a function of spacing in **Figure 2.5 (c)**. From these observations, we can conclude that the growth rate of the facet in the <1$\bar{1}$00> orientation decreased after the formation of a well-developed {1$\bar{1}$01} facets and increased rapidly prior to the formation of well-developed facets.

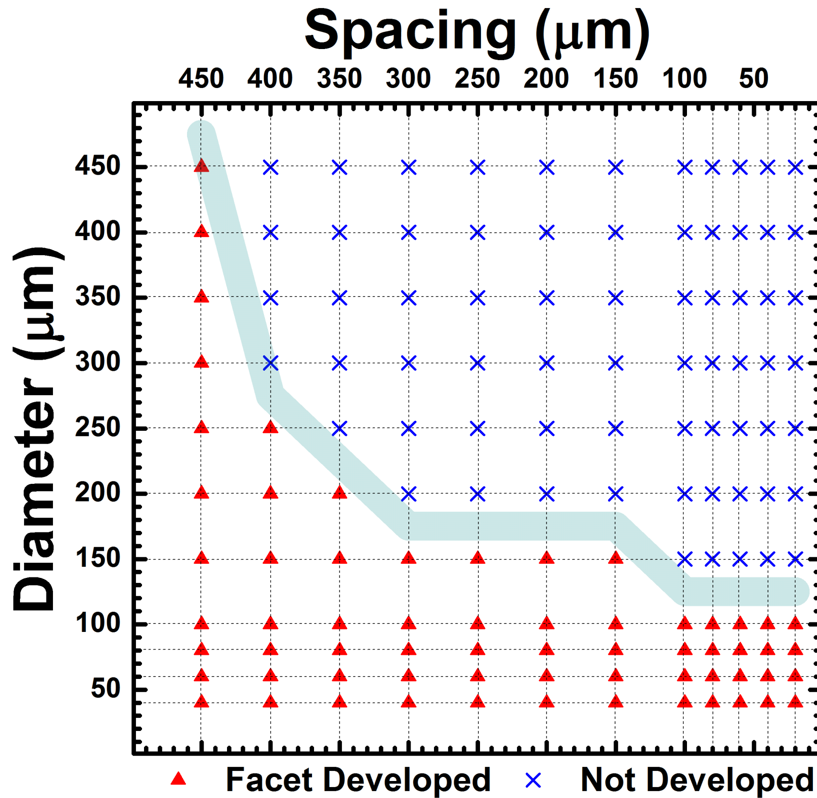

Figure 2.6 Facet evolution with the mask geometry as was observed by SEM. The triangles represent the grown structure with six complete well-developed facets and the crosses represent the grown structure with at least one rough sidewall.

2.3.5 Time Dependent Facet Evolution

The time evolution for facet formation is shown in **Figure 2.7** where three different samples were grown for 2 min, 4 min and 6 min. As in prior studies, we focused on only the center dot of the array, here for 80 µmD and 150 µmS sample. For the 2 min growth time, the facets didn't develop and the shape of the SAG GaN was circular similar to the starting original mask shape. For the 4 min growth time, the facets started to develop by growing faster in the $<11\bar{2}0>$ direction but the sidewall surface of the facets was still rough. For 6 min growth time, the facet was completely developed by forming smooth $\{1\bar{1}01\}$ facets for this mask geometry. After the facet development, all the six facets had the same length. This indicated that the facet evolution can be tuned by controlling the growth time as well as the mask geometry.

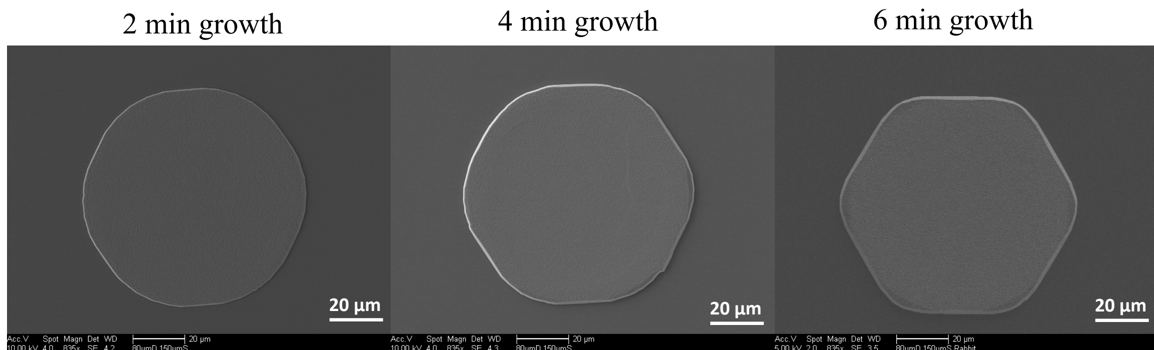

Figure 2.7 Top-view SEM image of the samples with 80 µmD and 150 µmS with different growth time.

2.4 Enhancement of LED Light Extraction by Tailoring Array Pattern Structure

From these growth studies, we developed the knowledge to tailor the SAG morphology by changing either mask opening size, spacing or growth time. These morphological changes are expected to influence the performance of devices made from these structures. To this end, we fabricated InGaN/GaN multiple quantum well (MQW) LED structures with/without well-developed facets as shown in **Figure 2.8 (a)** and **Figure 2.8 (b)**. To develop the well-faceted and non-faceted structures and yet maintain the same MQW layer thicknesses, we controlled the growth time for a pre-MQW n+ SAG GaN layer for 45 min (non-faceted) and 2.5 hours (well-faceted) as shown in the optical microscope images of **Figure 2.8 (c)** and **Figure 2.8 (d)**. A semi-transparent contact of Ni 5nm/Au 5nm was deposited atop of the dot followed by annealing in 100 sccm oxygen flow at 550 °C for 10 min which result in ohmic-like characteristics.[41–44] Ti 30nm/Al 70nm/Ti 10nm/Au 50nm ohmic contact was deposited on the n+ GaN bottom layer after etching of SiO_2. Their current voltage characteristics are shown in **Figure 2.9**. Electroluminescence characterization was performed on both well-faceted and non-faceted LED structures.

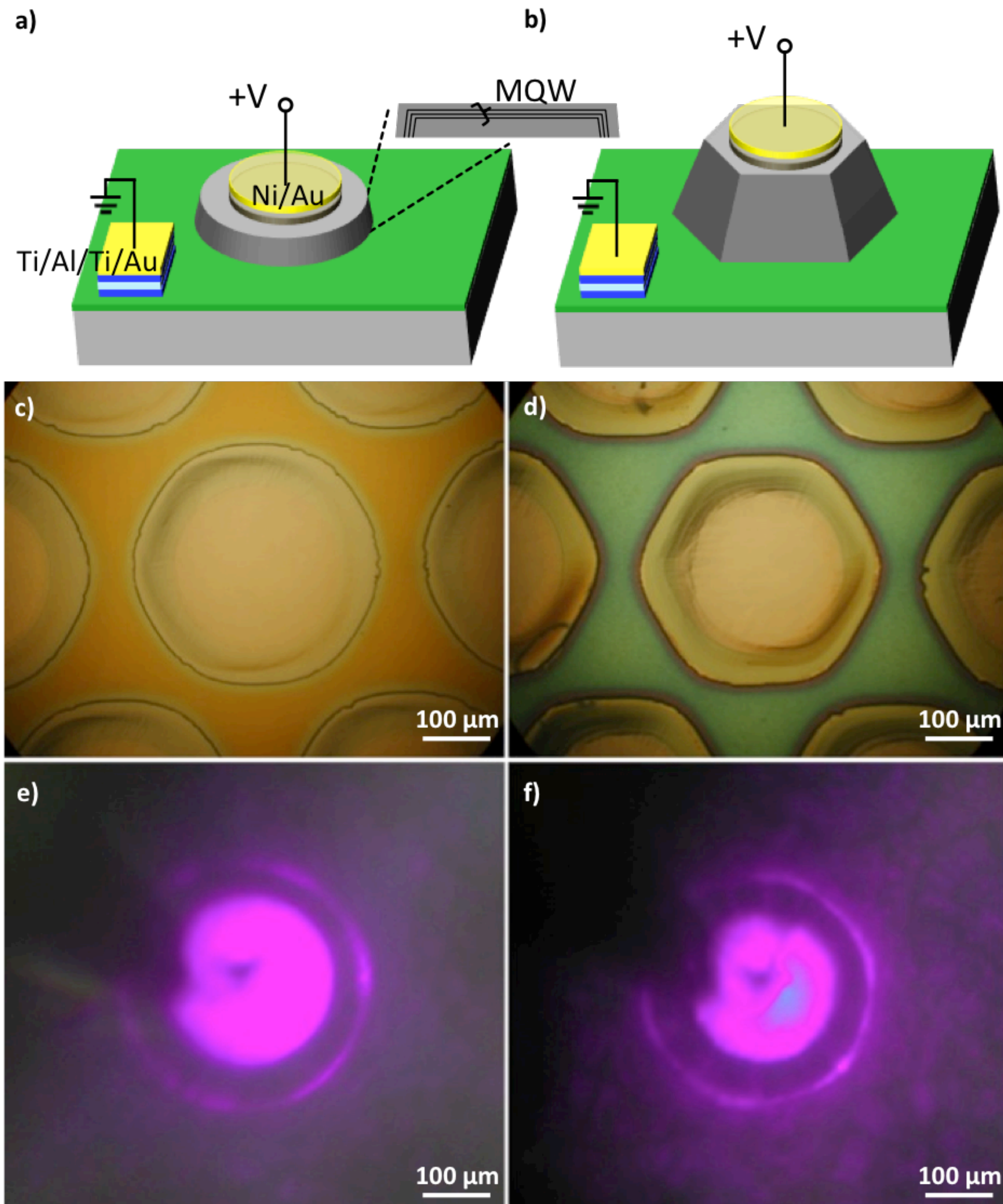

Figure 2.8 Schematic illustration of the device structure for (a) non-faceted SAG LED and (b) well-faceted SAG LED. Optical microscope images of (c) non-faceted and (d) well-faceted and their emitting images in (e) and (f) respectively. The mask geometries are the same, 350 µmD and 80 µmS for each structure.

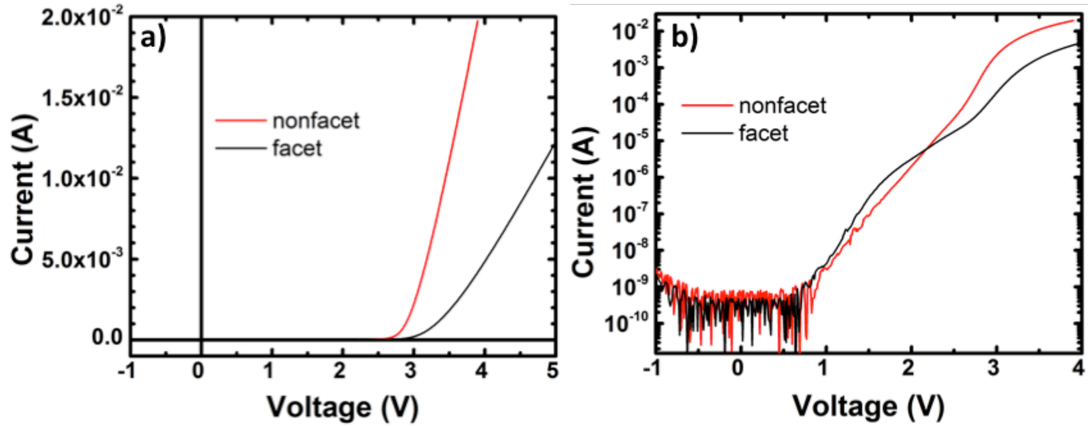

Figure 2.9 Current-voltage characteristics of (red line) non-faceted LED and (black line) well-faceted LED with (a) linear scale and (b) log scale.

The optical microscope images of the well-faceted and non-faceted LED samples at the drive current of 10 mA are shown in **Figure 2.8 (e)** and **Figure 2.8 (f)**, respectively. We observed strong emission through the thin metal contacts and some light reflection on the sidewalls. From the emitting images in **Figure 2.8 (e)** and **Figure 2.8 (f)**, relatively broadened light reflection and more light transmission parallel to the substrate surface were observed for the non-faceted samples while the reflected light of the well-faceted sample was sharper, less transmissive and more intense.

The electroluminescence (EL) data is shown in **Figure 2.10** for quantitative comparison of the light intensities. A well resolved InGaN/GaN MQW emission peak was observed for both of the well-faceted and non-faceted LED devices and the full width at half maximum of the spectra were found to be ~20 nm for both devices. It is well known that GaN LEDs grown on semipolar substrates or surfaces exhibit stronger light emission due to polarization field reduction and consequent stronger spatial overlap in the electron and hole wavefunctions.[45–48] In this work, we deposited metals on the c-plane top-surface such that the current spreading layer and consequently light emission is mainly from the polar surface. Despite this, **Figure 2.10 (a)** shows that the well-faceted LED had ~2.5 times higher EL peak intensity compared to the non-faceted LED. In

addition, the EL peak of the well-faceted LED was centered at 421 nm which is ~ 9 nm blue-shift compared to that of the non-faceted LED. The EL peak wavelength can depend on MQW thickness, strain, drive current, temperature, and In concentration.[49–52] To identify the origin of the observed blue-shift, we investigated the MQW structures by high resolution transmission electron microscopy (HRTEM).

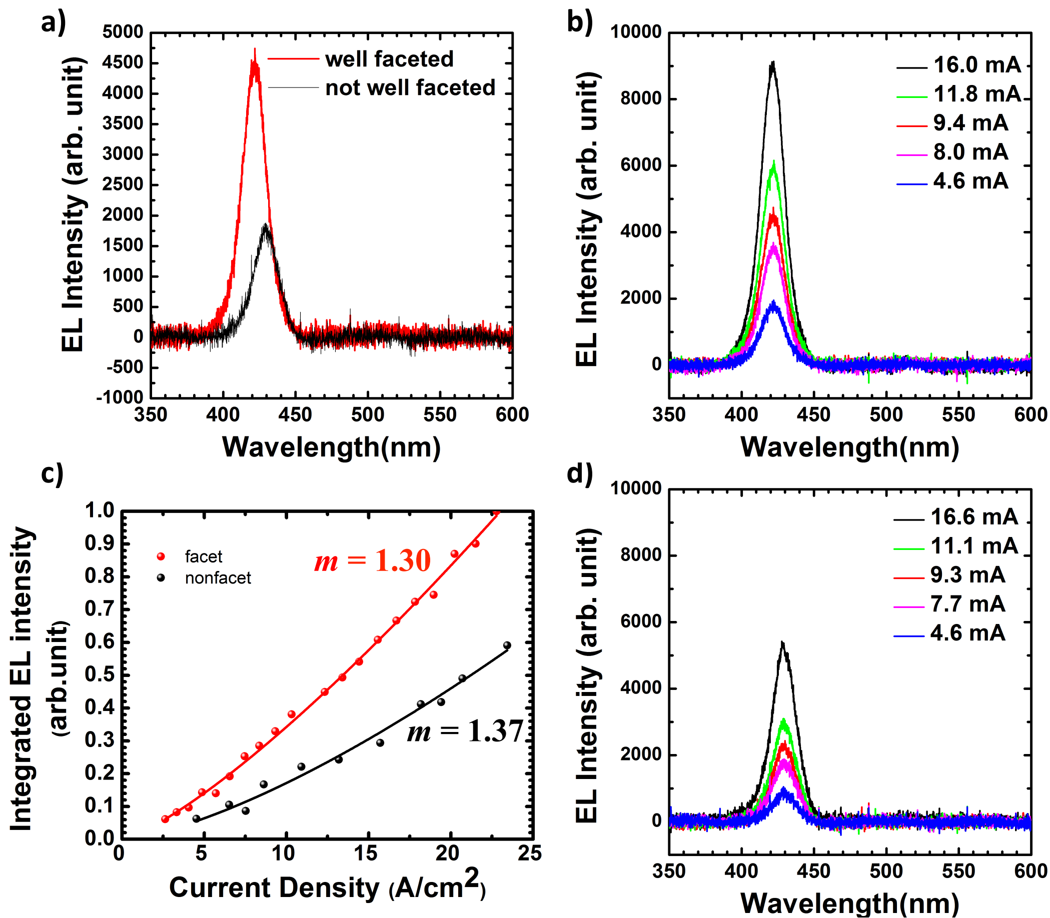

Figure 2.10 (a) Electroluminescence of the SAG LED samples with/without well-developed facets at 10 mA injection current. Electroluminescence of (b) well-faceted LED and (d) non-faceted LED with different currents. (c) Integrated EL intensities of well-faceted/non-facet LED with different current densities.

Figure 2.11 and **Figure 2.12** present the TEM characterization of the well-faceted and non-faceted structures and their locations of TEM samples. TEM images were taken both at the center of the dots and the sidewalls. As discussed in section 2.3, the MQW growth rate was also very different between the center and sidewall of the dots. The difference in their thicknesses are summarized in **Table 2.2**. The semitransparent contacts were deposited only on c-plane surface near the center of the structure and we found that the MQWs of both structures have similar QW thicknesses of 2.1 nm and QB thicknesses of 8.6 nm under the contacts (**Figure 2.12**). Therefore, we can conclude that the peak shift can be caused by the In concentration difference between the well-faceted and non-faceted samples. It is known that In incorporation efficiencies on different GaN surface planes are different.[45,53–56] T. Wunder et al. reported a 50 % higher indium incorporation for $\{1\bar{1}01\}$ semipolar facets in comparison to c-plane growth.[45] In our structures, Indium(In) adatoms diffusing from the mask were trapped more on the semipolar facets on than the c-plane top surface. Furthermore, as previously discussed for Ga adatom diffusion effects on the SAG growth rate, less In adatoms can reach the top of the SAG structure for the dots having thicker sidewalls than the In diffusion length. From the peak shift, we estimate around 14% lower In composition in the faceted LED when compared to the non-faceted LED. **Figure 2.10 (b)** and **Figure 2.10 (d)** show EL spectra of the well-faceted and non-faceted LEDs for different injection currents. The dispersion of the EL intensities with different currents was larger for the faceted LED. This implies that the sharp facets act as mirrors with strong index difference that reflect light to be emitted normal to the LED instead of diffracting it randomly in the lateral direction at the rough LED surface for the non-faceted LEDs.

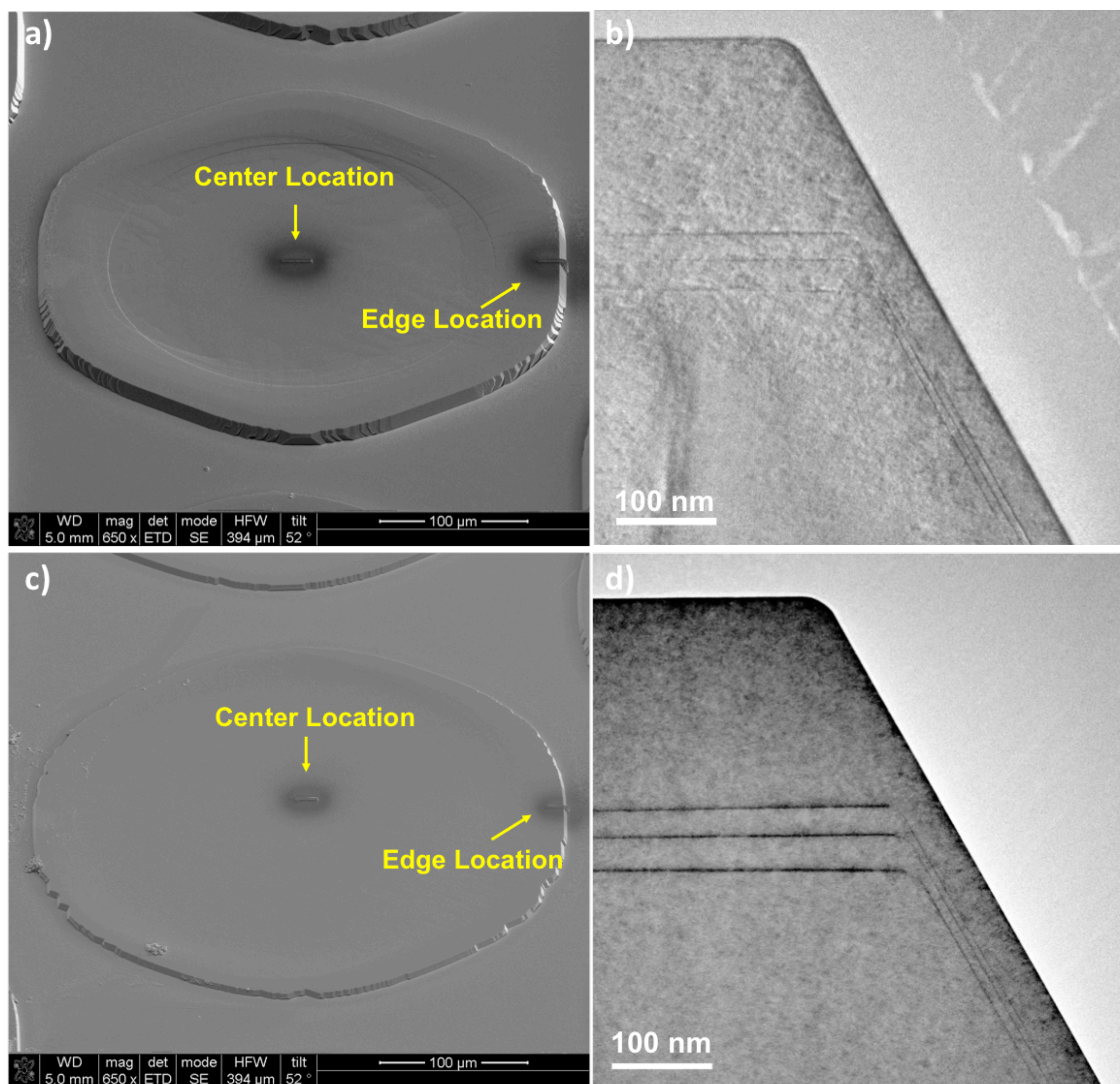

Figure 2.11 Angled view SEM images of (a) well-faceted and (c) non-faceted samples and their cross-sectional cut areas. The cross-sectional HRTEM images at the edge locations of (b) well-faceted and (d) non-faceted samples.

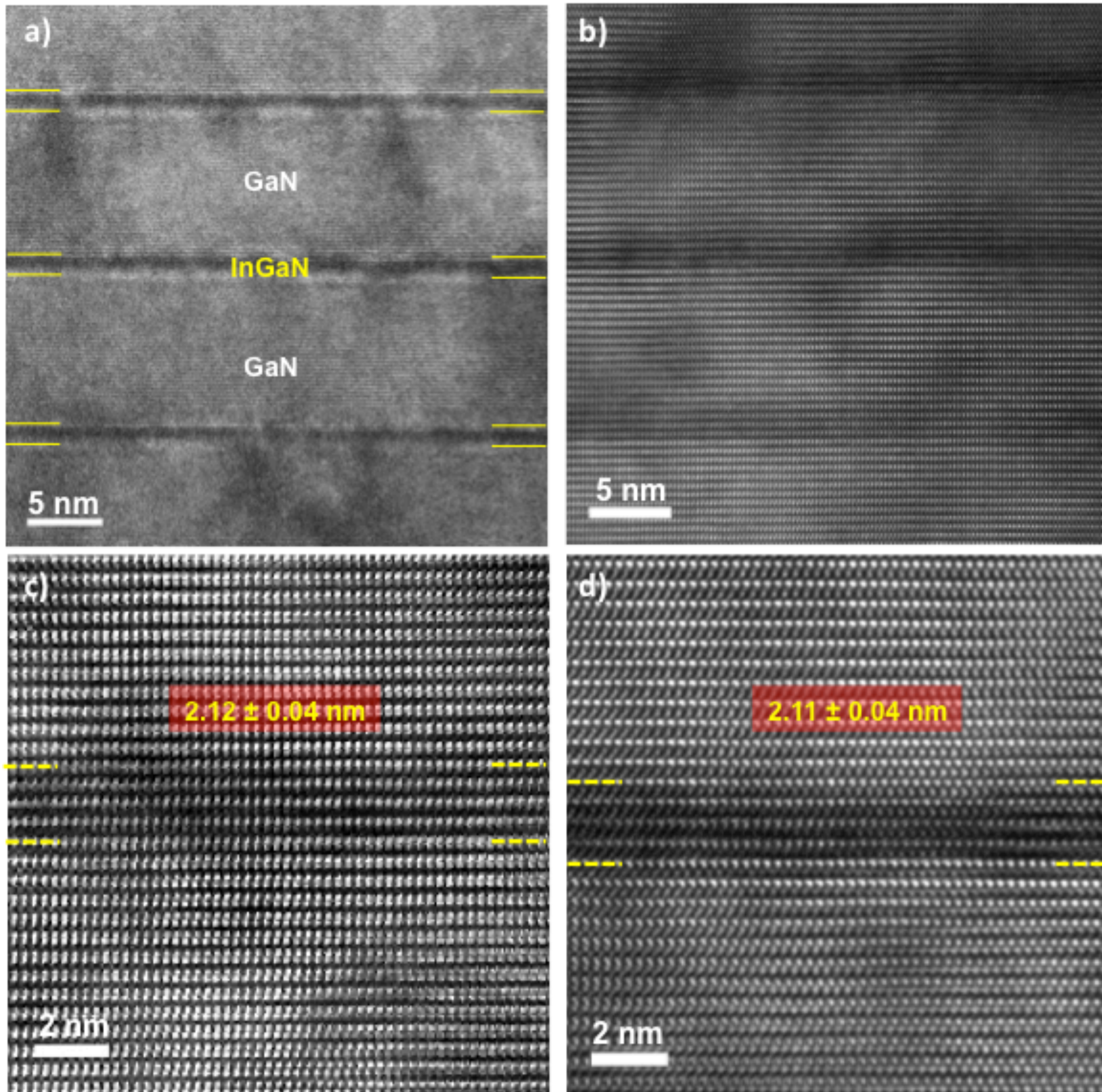

Figure 2.12 Cross-sectional TEM images of (a),(c) well-faceted and (b), (d) non-faceted MQW structures near the center of the structures. (a) and (b) show the uniform growth of three cycles of InGaN MQWs. (c) and (d) are zoomed-in images of (a) and (b), respectively.

Table 2.2 MQW thicknesses of the well-faceted and non-faceted LED at different points of the structures; center, edge and sidewall of the structure. These thicknesses were measured from TEM images and averaged over 10 lines for each point.

Sample location		QB thickness (nm)	QW thickness (nm)
Non-Faceted	Center	8.56 ± 0.21	2.11 ± 0.04
	Edge	27.78 ± 2.98	3.01 ± 0.41
	Sidewall	6.76 ± 2.01	1.42 ± 0.36
Well-Faceted	Center	8.58 ± 0.27	2.12 ± 0.04
	Edge	14.95 ± 0.81	2.07 ± 0.25
	Sidewall	7.35 ± 0.48	1.24 ± 0.01

To infer the dominant recombination mechanism, we plot **Figure 2.10 (b)** the *L-J* curves which are characterized by

$$L = P * J^{m} \tag{2-4}$$

where L is the integrated EL intensity, J is the current density (A/cm^2), P is a constant and m is an exponent parameter.[57,58] The exponent m can be used to characterize the emission mechanism of the SAG LED.[58] In our case of *L-J* dependence, both of the devices showed a super linear dependence ($m \sim 1.3$), which implies that most injected carriers recombine radiatively. With higher injection currents, Auger processes would become dominant with lower m values, a regime we didn't access in our experiments because of current limitation of our measurement setup. This result indicates that the well-developed semipolar facets are not only enhancing light emission by reducing polarization electric field but also assist in better light extraction in the c-axis direction.

2.5 Conclusion

To summarize, we showed in this study strong mask opening size and spacing effects in the GaN SAG on sapphire and demonstrated that such effects have implications on LED performance. By tailoring the SAG mask opening diameter, we observed as much as 4 times increase in the vertical height for 20 μm spacings. By changing the SAG spacing, we observed as much as 3 times increase in the vertical height at a dot diameter of 350 μm. We extracted the Ga adatom diffusion lengths to be ~29 – 35μm by fitting the surface profile plots, and attributed this difference to the effective V/III ratio or different mask geometries which also controlled the SAG surface morphology. The quantitative analysis of the mask opening size and spacing dependence on the vertical and lateral growth rate indicates that facet evolution of the SAG structure is a significant factor to determine the growth rate. With such understanding of and control over the growth morphology, we demonstrated that well-faceted structures exhibited stronger electroluminescence than non-faceted structures at the same current density. The strong morphology-performance effects in the LED structures developed in this work pave the way for higher efficiency LEDs.

2.6 Acknowledgements

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Jungjohann. Prof. Dayeh and I analyzed the data wrote the manuscript and obtained feedback from all authors.

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Chapter 3

Si Complies with GaN to Overcome Thermal Mismatches for the Heteroepitaxy of Thick GaN on Si

3.1 Introduction

Heteroepitaxial growth of lattice mismatched materials has advanced through the epitaxy of thin coherently strained layers, the strain sharing in virtual and nanoscale substrates, and the growth of thick films with intermediate strain relaxed buffer layers. However, the thermal mismatch has not been completely resolved in highly mismatched systems such as in GaN-on-Si. Here, we exploit geometrical effects and surface faceting to dilate thermal stresses at the surface of selectively grown epitaxial GaN layers on Si. We demonstrate the growth of thick (19 μm) crack-free and pure GaN layers on Si with the lowest threading dislocation density of 1.1×10^7 cm^{-2} achieved to date in GaN-on-Si. With these advances, we demonstrate the first vertical GaN metal-insulator-semiconductor field-effect-transistors (MISFETs) on Si substrates with low leakage currents and high on/off ratios paving the way for a cost-effective high power device paradigm on a Si CMOS platform.

For nearly five decades,[1] the large mismatch in the thermal expansion coefficients between GaN and Si (+116% with respect to Si) has limited the thickness of crack-free GaN film growth

on Si to less than 5 μm. In planar layers, severe substrate bowing and GaN layer cracking appears at thicknesses exceeding 1 μm.[2] The selective area growth (SAG) emerged as an effective approach to minimize the detrimental wafer bowing effects by confining the area of grown GaN and enabled the successful increase for this thickness limitation to ~ 1.5 μm.[3] But thicker layers are critical for electronic and optoelectronic devices where the density of dislocations and effects of Ga/Si inter-diffusion near the grown interface are thickness-dependent.[4,5] Additionally, thicker GaN layers improve the current spreading, minimize heating effects and reduce the efficiency droop in GaN light emitting diodes (LEDs). To the best of our knowledge, the thickest GaN layer achievable on Si was limited to 4.5 μm grown atop a low temperature AlN interlayer sequence with a total thickness of 14.6 μm.[6] The AlN layers block vertical current flow, thus limiting the effective useful GaN layers for certain types of LEDs and power devices that require >10 μm thicknesses.

3.2 Optimization of SAG Mask Design for Thick GaN Growth

To enable the growth of thick and crack-free GaN layers on Si, the interfacial stresses at any point of the GaN/Si interface need to be reduced to avoid crack nucleation. Stresses within the layers themselves need also to be directed away from the crack planes. But prior SAG growths have extensively used rectangular or square growth patterns where the stresses peak at the pattern corners and it is at these corners where the crack in the GaN layers nucleate.[3,7–9] Therefore, we first embarked on reducing the interfacial stresses along the circumference of SAG patterns in 10 μm thick GaN layers grown on Si.

The thermal stress simulations in this study were performed using Comsol Multiphysics. For the simulations in **Figure 3.1 (a)**, we assumed that the top 10 μm GaN was fully relaxed at the

growth temperature and stressed only by thermal expansion difference from 1 mm thick Si substrate. For fair comparison, the interface areas of the different structures were set to be the same as 350 μm diameter circle. The thermal stresses were calculated by Structural Mechanics Module combined with Heat Transfer interface to couple the temperature field to structural expansion. The built-in material parameters in Comsol were used for all simulations. Our thermal stress simulations showed that upon cooling from the 1050 °C growth temperature to room temperature, the corner stress is significantly reduced when more corners were added to the pattern and is lowest - and evenly distributed - for a circular interface (**Figure 3.1 (a)**). Our experiments of SAG GaN over the same SAG mask shape in **Figure 3.1 (b)** corroborated with the simulation results. For the 10 μm thick SAG GaN-on-Si, the triangular and square GaN patterns were severely cracked while those with hexagonal and circular masks were not. We limited our growth time to 3 hours for which we could grow by SAG 18 μm thick GaN-on-Si at the center of circular patterns with 350 μm diameter and the GaN thickness was over 35 μm at the disk edges. As discussed below, once the hexagonal facets are completely developed, thick and crack-free GaN layers exceeding 18 μm will be possible.

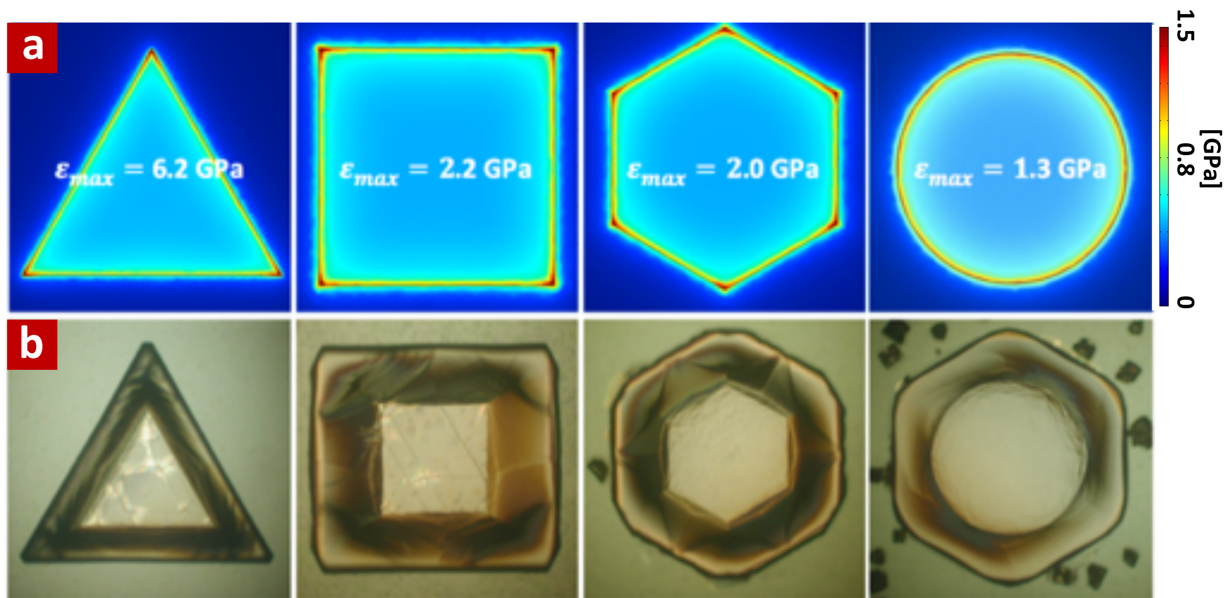

Figure 3.1 (a) Thermal stress distribution at the GaN/Si interfaces with different mask designs showing the lowest stress maxima for the circular mask. **(b)** Top view optical microscope images of the SAG GaN grown to have 10 µm at the center of the structure. The GaN with triangular and squared patterns severely cracked as predicted in Fig. 3.1 (a).

3.3 Cracking Mechanism of SAG GaN-on-Si

3.3.1 Time Dependent Growth of SAG GaN on Si

With the circular SAG mask patterns, we successfully achieved crack-free GaN layer on Si with thickness exceeding 10 μm. In order to understand the cracking mechanism further, we have grown SAG GaN with different times with the circular mask openings. **Figure 3.2** shows the top-view optical microscope images of SAG GaN on Si with different thicknesses. As shown in **Figure 3.2**, severe cracks appeared when the GaN thickness is less than 7 μm. In contrast, the GaN with thickness exceeding 10 μm did not show any crack in GaN. The mismatch stresses in lattice mismatched system usually increases with the heteroepitaxial thickness because it has larger volume to be stressed. However, what we observed in SAG GaN is the opposite to the result which was observed in typical heteroepitaxy. The notable difference between thick and thin SAG GaN is that the thicker SAG GaN has enough time to develop the hexagonal growth facets compared to the thin SAG GaN as discussed in chapter 2. Therefore, we hypothesized that the mechanism for GaN-on-Si stresses and crack elimination is directly related to the formation of the GaN facets.

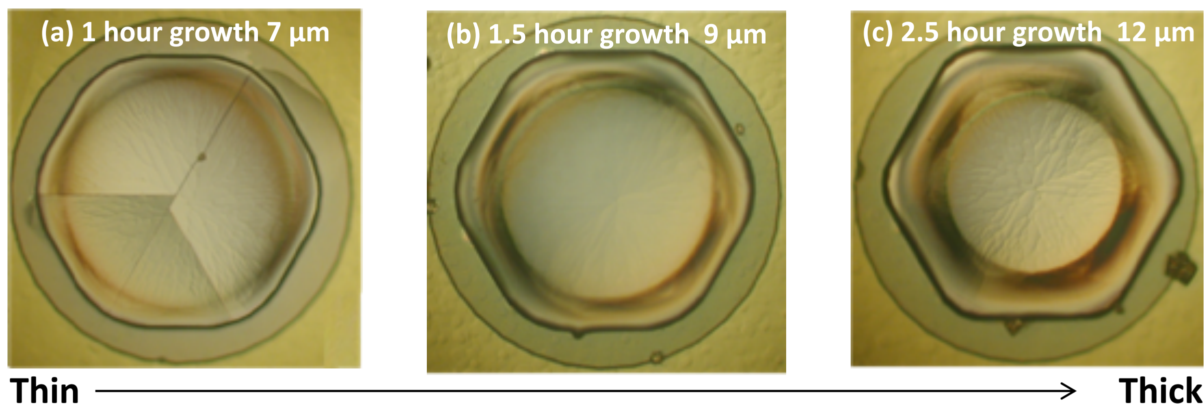

Figure 3.2 Top-view optical microscope images of SAG GaN with different growth time. The thicker GaN shows well-developed hexagonal facets and no crack whereas the thin GaN shows severe cracks and facets have not developed yet.

3.3.2 Stress Relaxation by Facet Evolution

In all our growth studies, we observed the cracks in GaN always occur on the $\{01\bar{1}0\}$ family planes and propagate in $\langle\bar{2}110\rangle$ type directions (Inset of **Figure 3.3 (a)** and **Figure 3.4**). From the cross sectional TEM images of the faceted GaN disk in **Figure 3.3 (a)** and its fast Fourier Transform (FFT), we deduced that the thick GaN disk developed $\{01\bar{1}0\}$ facets on the sidewall. Cross-sectional TEM analysis also validated that the cracks occur on the $\{01\bar{1}0\}$ planes (**Figure 3.5** and **3.6**) when the crystal was oriented in a $\langle\bar{2}110\rangle$ beam axis, i.e. along the line of propagation of the crack. The $\langle\bar{2}110\rangle$ crack propagation directions are common dislocation directions (Burgers vector $\vec{b}$) in hexagonal crystals and an avalanche of these dislocations under tensile stress will lead to cracking on the $\{01\bar{1}0\}$ planes. $\vec{b}$ is the line of intersection between the $\{01\bar{1}0\}$ and the $\{01\bar{1}1\}$ facet planes as illustrated in **Figure 3.3 (b)**. Therefore, if the stresses accumulated on the $\{01\bar{1}0\}$ planes in the $\vec{b} = \langle\bar{2}110\rangle$ are shared with the surface $\{01\bar{1}0\}$ facets, stress accumulation on the $\{01\bar{1}0\}$ planes inside the GaN disk does not reach a threshold for an avalanche of dislocations in the $\langle\bar{2}110\rangle$ direction. As a result, crack formation on the $\{01\bar{1}0\}$ planes in thick and well faceted SAG GaN-on-Si disks was eradicated.

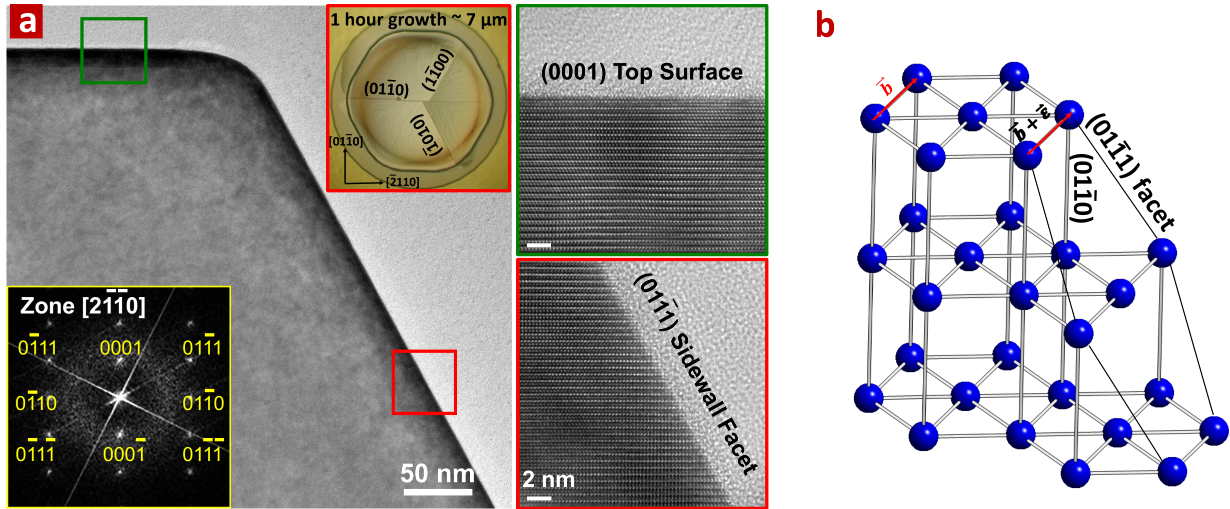

Figure 3.3 **(a)** Cross-sectional HR-TEM images at the edge of hexagonal facets. The sidewall facet and top surface planes are identified by FFT patterns in the bottom-left inset. The top-right inset shows top view microscope image of cracked GaN disk with the crack planes identified. **(b)** Illustration of hexagonal crystal structure (not showing inter-lattice atoms) showing that the (01$\bar{1}$0) crack plane and the (01$\bar{1}$1)growth facet share the Burgers vector $\vec{b}$ and allow the stress in GaN disk to dilate.

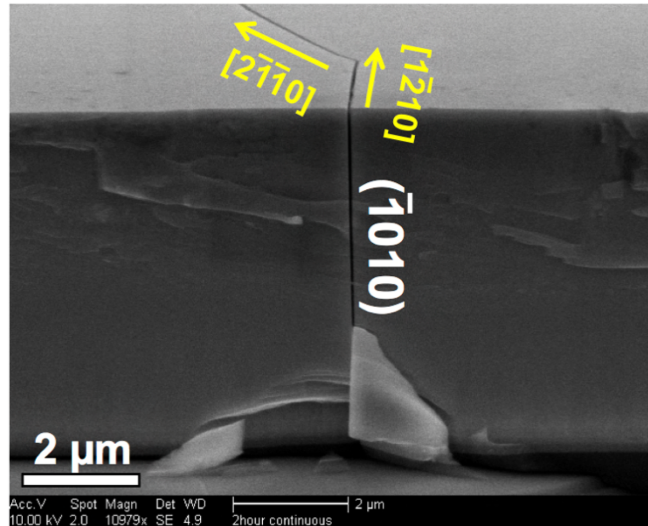

Figure 3.4 Major crack plane determination by SEM. Angled view SEM image of diced GaN disk in <10$\bar{1}$0> direction. The crack propagates straight down to the substrate and ~60° intersections, indicating the crack plane is in (10$\bar{1}$0) and propagate in the <$\bar{2}$110> directions.

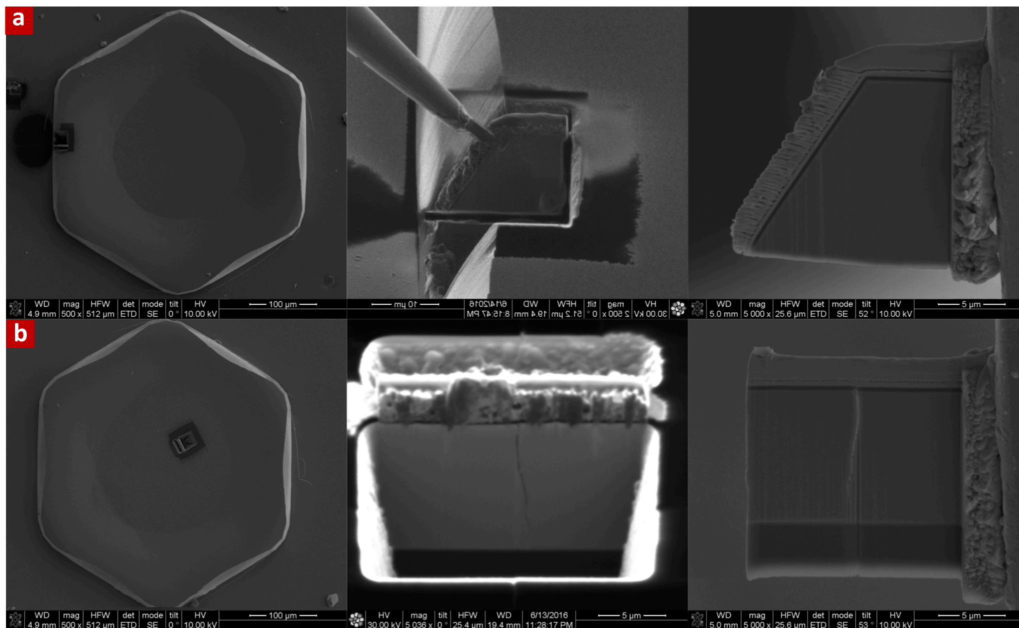

Figure 3.5 TEM sample preparation. SEM images of FIB cut and lifting of TEM slab by omniprobe. FIB cuts were perpendicular to the hexagonal facets $\{01\bar{1}1\}$ in (**a**) and to the major crack $\{01\bar{1}0\}$ planes in (**b**) to reveal the relationship between crack directions and facets.

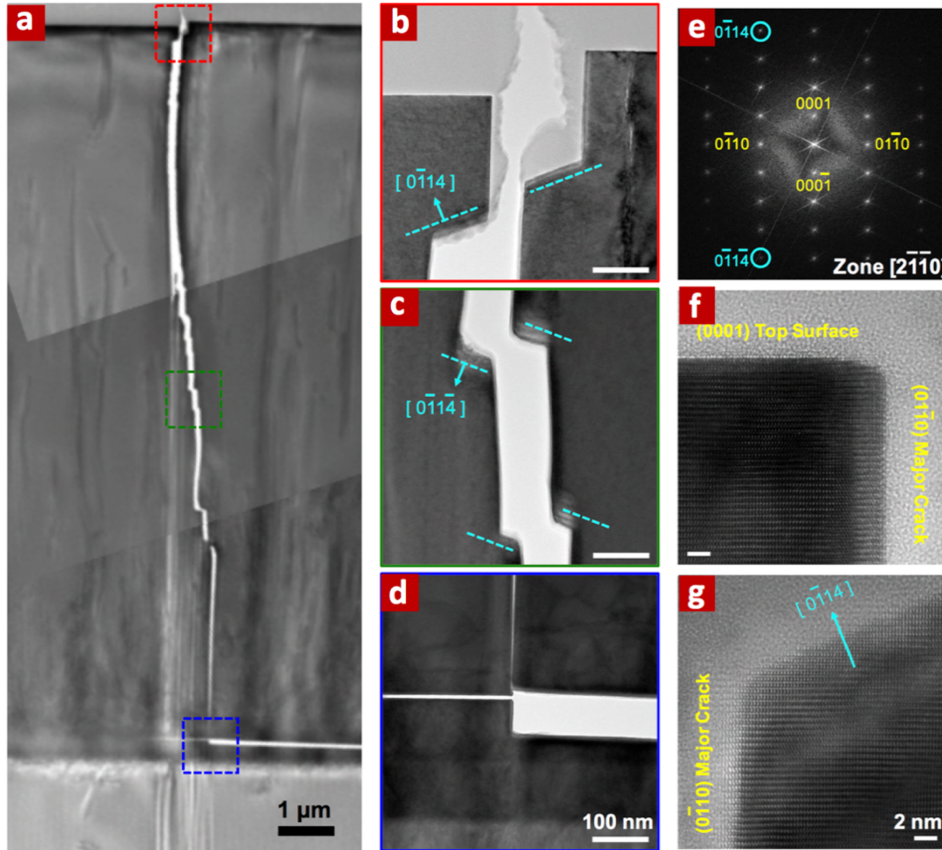

Figure 3.6 Crack plane determination by TEM. (a-d) Cross-sectional TEM image showing cracking from the Si interface propagated to the top surface with cracks gliding on $\{01\bar{1}4\}$ planes and maintaining a dominant $\{01\bar{1}0\}$ crack plane. **(e)** FFT pattern used to determine the minor cracking planes and **(f-g)** magnified HR-TEM image near the top surface of a small crack on the $\{01\bar{1}4\}$ plane.

3.3.3 Stress Measurement by Micro Raman Spectroscopy

In order to validate our hypothesis about the stress relaxation by the growth facet, we prepared 30 min and 3 hours growth SAG GaN samples. For a 30 minute SAG growth time, a 5 μm thick undoped GaN layer is grown without facets (**Figure 3.7 (a)**) whereas a 3 hour growth run resulted in 18 μm thick undoped GaN layers with $\{1\bar{1}01\}$ hexagonal facets (**Figure 3.7 (b)**). Although both images in **Figure 3.7 (a) and (b)** show un-cracked GaN disks, the yield of un-cracked disks for the thinner sample was only 4% (1 out of 25 disks) whereas, counterintuitively, the yield for the thicker and faceted hexagonal disks was 100 % (25 out of 25 disks). To evaluate the difference in residual stress in GaN for the two different growths, we used areal Raman spectroscopy to estimate stress from the Raman peak shift $\Delta\omega$. **Figure 3.7 (c) and 3.7 (d)** show the as-measured Raman peak (GaN E_2^H) as a function of X, distance from center of the disk. For the thin GaN disk, the GaN E_2^H is significantly lower than the unstressed reference sample GaN E_2^H peak. For all X, the Raman shift frequency remained relatively unchanged. In contrast, the peak shift with X for the thick GaN from the unstressed GaN E_2^H is largest near the center, and decreases toward that of the unstressed state near the disk edges (facets). This implies that the evolution of the hexagonal facets significantly reduced the stress in the GaN disk. For a σ_{xx} biaxial stress, the Raman shift $\Delta\omega = K\sigma_{xx}$ of GaN E_2^H peak with respect to stress-free GaN E_2^H peak, 568 cm^{-1}, was calculated using K = 4.2 cm^{-1}/GPa.[13] **Figure 3.8 a-f** show the 2- and 3-dimensional mapping of the stress in GaN disks with different thicknesses. These stress measurements identified that the thick GaN encompassed a maximal stress that is nearly half of that for the thin GaN layers. Significantly, the stress reduction is mostly effective near the edge of the thick GaN disks. Therefore, the stress reduction is directly related to the formation of complete facets for the hexagonal disks.

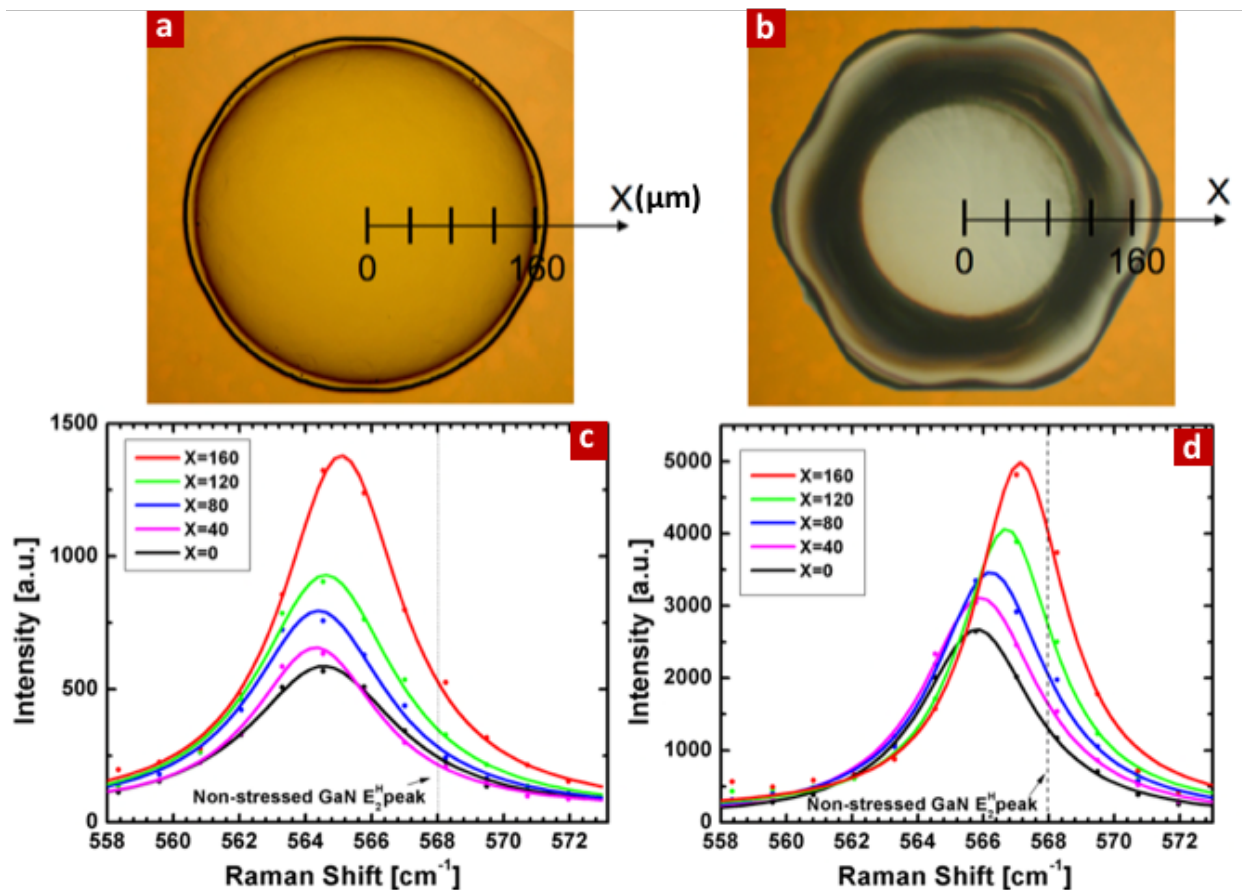

Figure 3.7 Stress relaxation due to hexagonal facets. Top view microscope images and Raman Shift of **(a, c)** thin GaN disk and **(b, d)** thick GaN disk as a function of X, distance from the disk center. The dashed line indicates the reference peak for non-stressed GaN E_2^H(568 cm^{-1}).

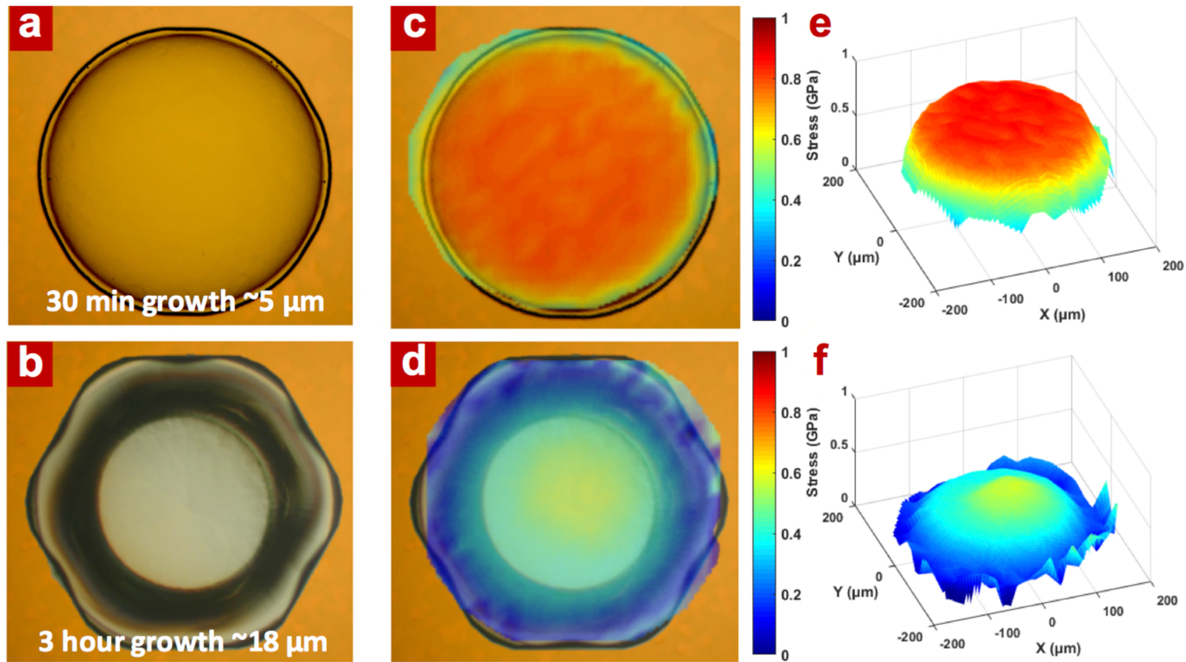

Figure 3.8 Stress relaxation mechanism in crack-free GaN-on-Si by facet formation. (a,b) Top view microscope images of 30 min GaN with no facets and 3 hour growth GaN with sharp hexagonal facets. **(c.d)** 2-dimensional stress mapping measured by Raman spectroscopy on the two different GaN disks overlayed over the images of (**a**) and (**b**). **(e.f)** 3-dimensional stress maps for disks in (**a**) and (**b**). The overall stress values in the thick GaN are almost half of that in the thin GaN due to effective stress reduction near the edge of the GaN disks, indicating stress relaxation by facet formation.

3.4 Tangential Stress in GaN/Si Interface and Cracking in Si substrate

3.4.1 Observation of Cracking in Si substrate

The use of circular mask and hexagonal growth facets successfully eliminated cracking in SAG GaN with the thickness of 18 µm. The facet development during SAG in circular structures is dictated by the differences in growth rates in the <$11\bar{2}0$> (fast) and <$1\bar{1}00$> (slow) directions leading to the evolution of $\{1\bar{1}01\}$ facets in the slowest growing interface and hexagonal vertices in the <$11\bar{2}0$> direction at the facet intercepts. However, the development of the hexagonal facets also accumulate stresses in the planar Si substrate. With the same growth disk morphology that was obtained during the growth, we repeated the thermal stress simulations of cooling from 1050 °C to 100 °C (**Figure 3.9 (a)**) The simulation results indicated that the stress peaks at the hexagonal vertices (**Figure 3.1 (a)**, **Figure 3.9**) lead to disk rotation by ~ 4-5°.

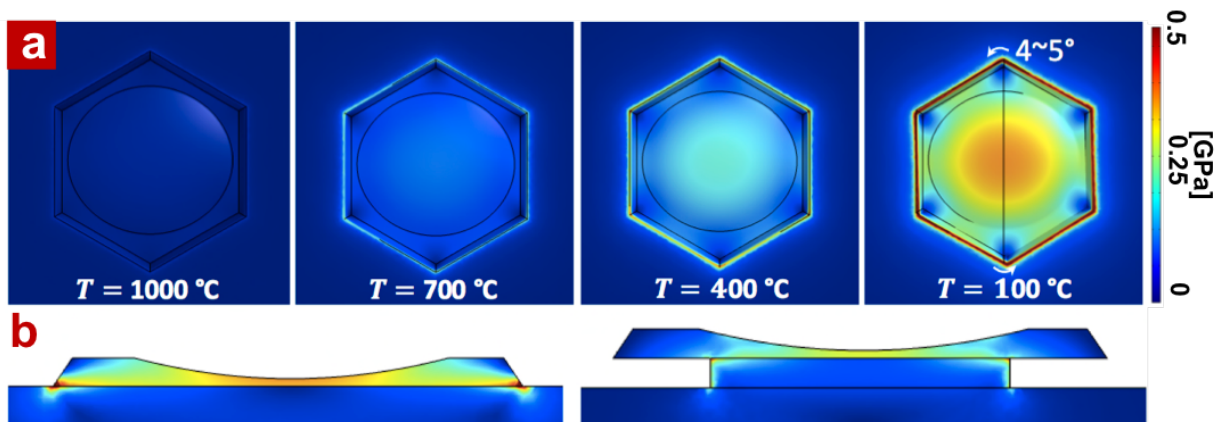

Figure 3.9 (a) Evolution of thermal stress during cooling down from 1050 to 100 °C. The solid black lines are the original GaN disk location at the growth temperature. As the GaN disk is stressed during cooling down, it starts to rotate, and results in ≈4–5° rotation with respect to the Si substrate. **(b)** Cross-sectional view of thermal stress simulation of SAG GaN with/without Si base etched. The stress peaks at the interface of hexagonal vertices were eliminated by removing Si under the SAG GaN.

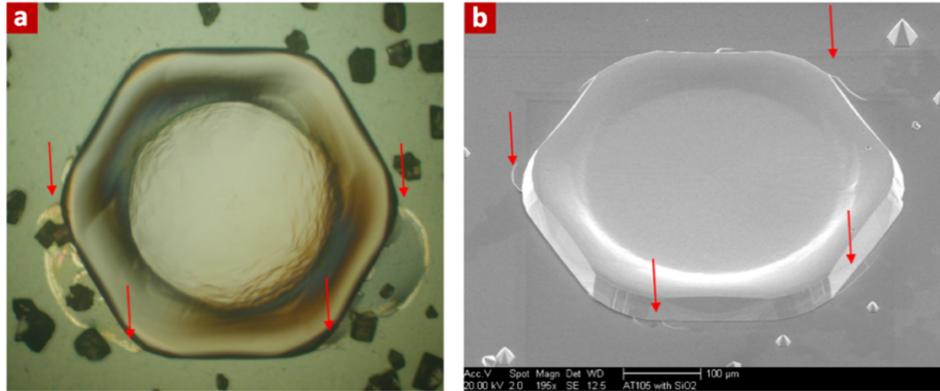

Figure 3.10 Elimination of tangential cracking in Si. **(a,b)** Optical/SEM images of thick SAG GaN on Si with no Si etch. Cracking can be clearly observed in the base Si in a tangential fashion. **(c,d)** Optical/SEM images of Si-etched thick SAG GaN on Si with no cracking in either GaN or Si.

Figure 3.10 (a) and (b) show severely cracked Si substrate. Different from cracking in GaN which always followed specific crystal directions, the cracks in Si nucleated below the vertices of the GaN dot and propagated in a tangential fashion due to tangential strain/stress accumulation under the GaN disk that is caused by the rotation due to shear stresses at each of the GaN hexagonal vertices. In the cross-section of the GaN/Si interface, we observed that the crack in the Si extended further to the center of the disk and its depth in Si t_{Si} was slightly thicker than the GaN top layer, t_{GaN}. ($t_{Si} \propto c_{11,GaN}/c_{11,Si} \cdot t_{GaN} > t_{GaN}$, where c_{11} is an in-plane elastic constant, **Figure 3.11 (a)**). Elevated levels of stress in the Si substrate that arise from high areal density GaN structures can lead to the eventual peel-off from the Si substrate as shown in **Figure 3.11 (b)** and **(c).**

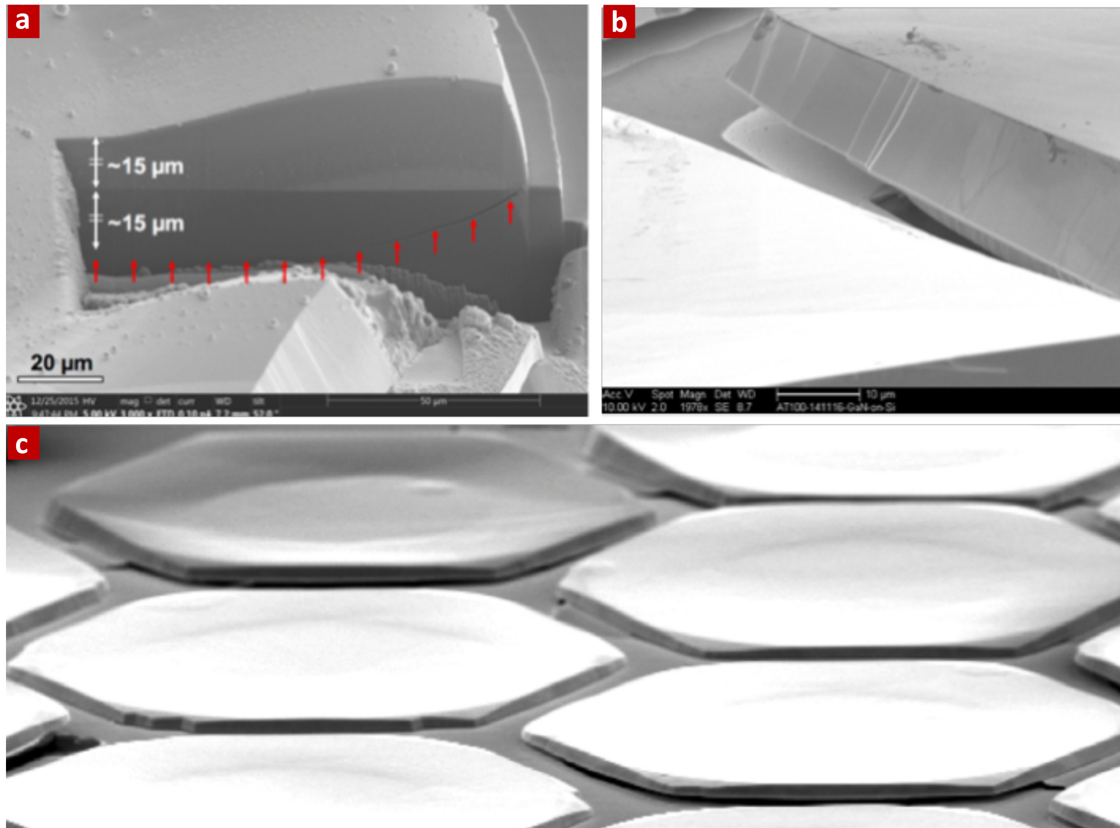

Figure 3.11 SEM images of cracking in Si. **(a)** Angled view SEM images of FIB cut GaN disk without isotropic etch. The cracking in Si nucleated at the corner of SAG GaN disk and propagated as deep as GaN total thickness. This highlights the need for etching Si base as deep as GaN thickness to relax the rotational stress. **(b,c)** Peeling issue in dense SAG GaN on Si array. Angled view SEM images of highly packed SAG GaN disk arrays (dot-to-dot spacing 20 μm). The high packing density led to severe cracking and eventual peel off for the GaN disk from substrate.

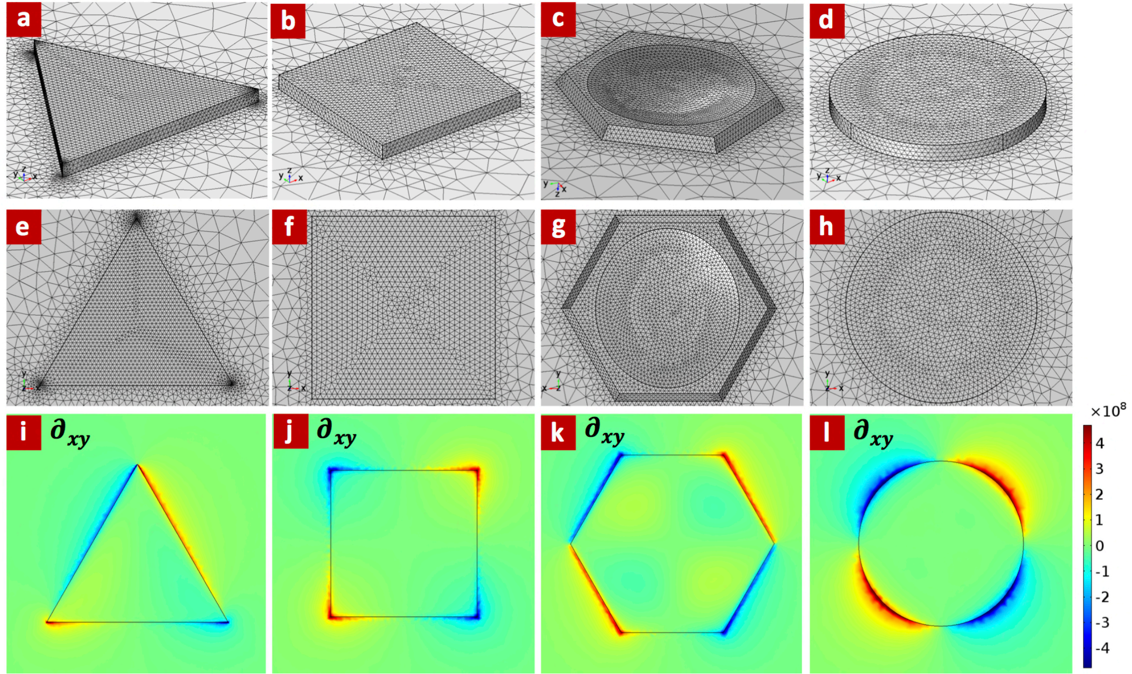

Figure 3.12 Mapping of rotational stress components, ∂_{xy}**.** Top view **(a-d)** and angled view **(e-h)** of mesh pattern for different geometries used in all simulations. **(i-l)** Mapping of stress tensors at the interface of GaN/Si with anisotropic elastic matricies. The non-uniform stress distribution along the side of the GaN hexagonal disk together with existing non-uniformites in the grown GaN island lead to rotational stresses in the xy plane at the interface.

To clarify the rotational stress in XY plane, we resolved the stress tensor to ∂_{xx} and ∂_{xy} for load stress and ∂_{xy} for shear stress components. **Figure 3.12 (a-d)** show tetrahedral mesh patterns built for this simulation. In the simulation, we assumed both iso- and anisotropic linear elastic materials. For Si, we defined its elasticity matrix as follow[10]:

$$\boldsymbol{D}=\begin{pmatrix} 1.66 & 0.64 & 0.64 & 0 & 0 & 0 \\ 0.64 & 1.66 & 0.64 & 0 & 0 & 0 \\ 0.64 & 0.64 & 1.66 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.80 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.80 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0.80 \end{pmatrix} \times 10^{11}\ \mathrm{Pa} \qquad (3\text{-}1)$$

For wurzite GaN[11], we used:

$$D = \begin{pmatrix} 3.90 & 1.45 & 1.06 & 0 & 0 & 0 \\ 1.45 & 3.90 & 1.06 & 0 & 0 & 0 \\ 1.06 & 1.06 & 3.98 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1.05 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1.05 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1.23 \end{pmatrix} \times 10^{11}\, Pa \qquad (3\text{-}2)$$

Figure 3.12 (i-l) show mapping of stress tensor, ∂_{xy}, at the interface of GaN/Si. The non-uniform shear stress components indicated the rotational stresses in GaN and Si exist at their interface.

3.4.2 Substrate Engineering to Accommodate the Tangential Stress

In order to eliminate the stress in Si, equal amount of Si under the SAG GaN needs to be removed. Therefore, we etched ~30 µm Si under GaN disk to eliminate cracking in both GaN and Si (**Figure 3.13 (a-c)**). We hypothesized that a free Si surface will also dilate the stresses in Si upon cooling down from the GaN growth temperature as supported by thermal stress simulations in **Figure 3.9 (b)**. Therefore, we estimated the lateral overgrowth based on our earlier SAG studies[12] and fabricated structures for which the exposed 500 nm thick GaN seed layer is surrounded by an SiO_2 growth mask on top of an isotropically etched Si structure (**Figure 3.13 (a)**). This free surface structure resulted in crack-free GaN layers and Si substrate because the free surface of the Si substrate can accommodate the stress by rotation(**Figure 3.13 (b,c)**). In this context, Si deformation that is caused by thermal stresses in GaN resembles the lead (GaN) and the follower (Si) in a Tango setting.

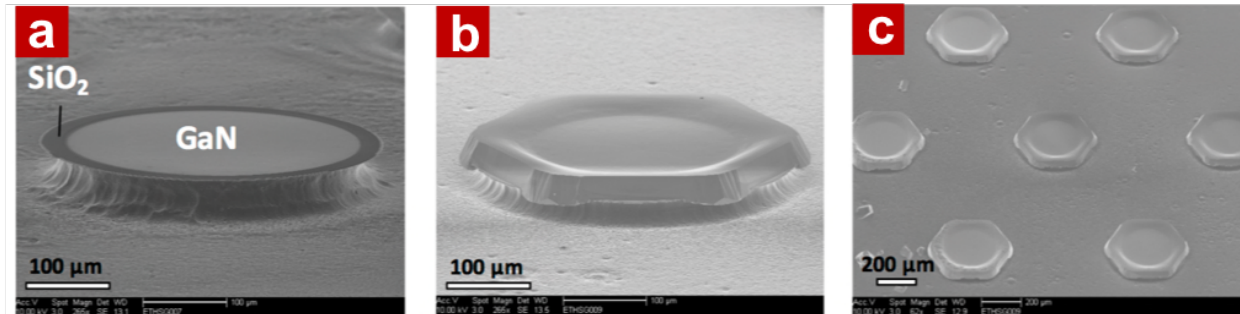

Figure 3.13 Angled-view SEM images of Si etched SAG GaN disk before **(a)** and after **(b,c)** growth.

A larger field of view angled SEM image of the grown array is shown in **Figure 3.13 (c)** and top-view optical and SEM images in **Figure 3.14 (a), (b)** showing no tangential cracking in Si. The cross-sectional SEM image through the edge-to-center in the SAG GaN-on-Si disk shown in **Figure 3.14 (c)** further validates that all cracks in both GaN and Si were exterminated. With this technique, we showed genuine crack-free GaN grown on Si with a thickness of 18 μm for the first time. This is advantageous because the enhanced growth rate by SAG epitaxy allows achieving high quality GaN layers by MOCVD in short growth times and is extendable to mm-scale growth GaN islands (**Figure 3.15**). Additionally moving the voltage blocking layers to the vertical direction can increase the device density per unit area compared to the conventially fabricated lateral devices on the substrate surface. Overall, these capabilities may contribute to a cost effective high power GaN device paradigm on Si.

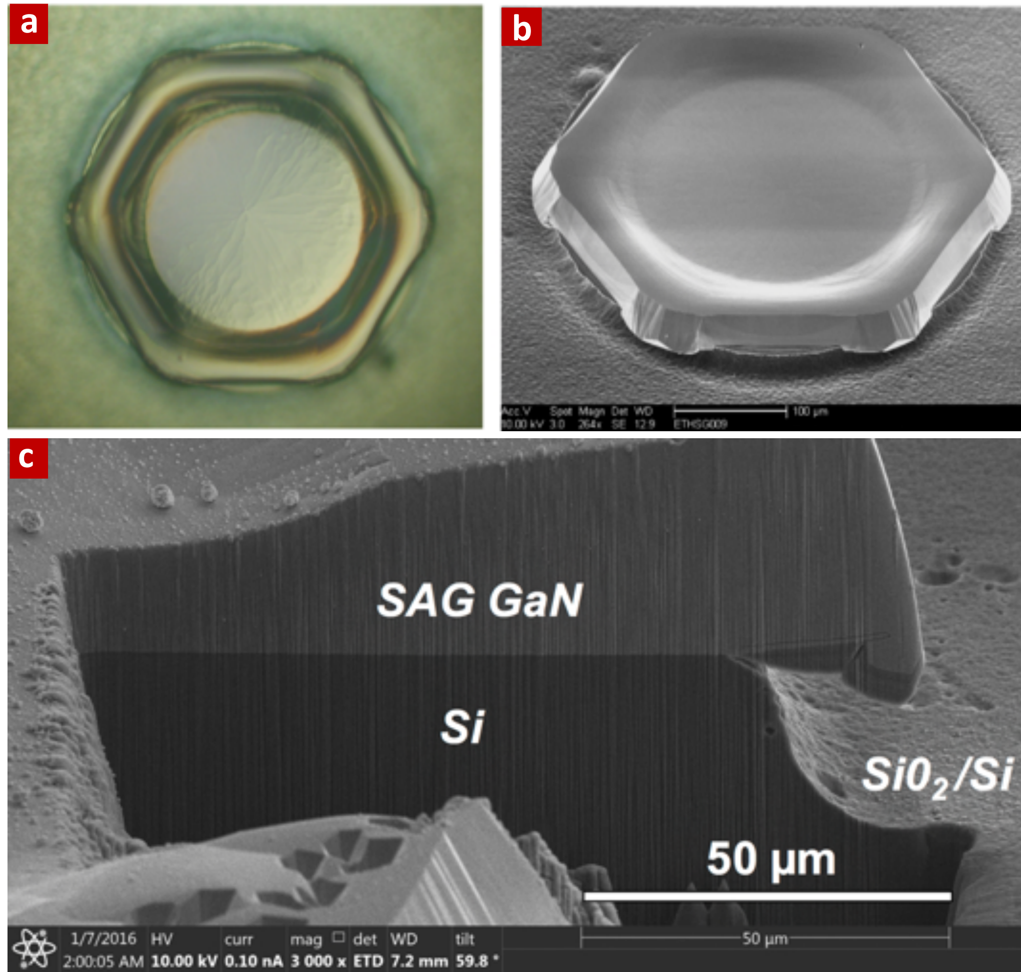

Figure 3.14 Substrate engineering for crack elimination in Si. (a) Top view microscope image and **(b)** angled view SEM image showing no cracking from both images. **(c)** Angled view SEM image of FIB cut GaN disk with proper base Si etching. The etching depth was nearly equivalent to the GaN thickness to accommodate all stress at the Si surface. There is no cracking found in GaN and Si.

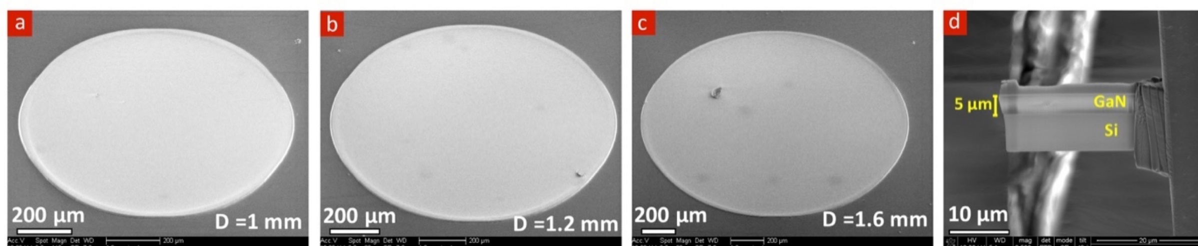

Figure 3.15 Millimeter scale SAG GaN growth on Si. (a,b,c) Angled view SEM images of 1mm, 1.2mm, and 1.6mm diameter GaN disks showing no cracking in GaN-on-Si post 3 hours of GaN growth. **(d)** Cross-sectionl SEM images from 1.4mm diameter GaN on Si showing a thickness of 5 μm.

3.5 Material Quality Improvement by Thick GaN Growth

The understanding of the cracking mechanism and geometrical effects on stress dilation enabled the growth of 18 µm thick crack free GaN-on-Si with 350 µm diameter in circular SiO_2 mask patterns. For device applications, the threading dislocation density (TDD) is one of the critical parameters which significantly degrade device characteristics and reliability.[14] Dislocations of various types are generated at the GaN/Si interfaces because of lattice and thermal mismatches with dislocation densities approaching 10^9-10^{11} cm^{-2}. It is known that the growth of thick layers in lattice mismatched materials[5,15] can lead to annihilation and reduction of the dislocation densities but in the context of GaN-on-Si, this approach has never been applied before because thicker GaN layers on Si were not possible before our work. With our thick crack-free GaN-on-Si, the dislocations at the interface of GaN/Si annihilated as the material grew thicker, and the TDD reduced from ~ 8.0×10^7 cm^{-2} for 10 µm thick GaN-on-Si to 1.1×10^7 cm^{-2} for 18 µm GaN-on Si as observed with the cross-sectional HR-TEM images in **Figure 3.16**. This TDD was also validated by dislocation enhanced wet etching and surface imaging. The grown GaN-on-Si was immersed in H_2SO_4:H_3PO_4 (3:1) solution at 270 °C to selectively etch the the mixed and screw dislocations in GaN disk. The **Figure 3.17** shows the top view microscope images showing a number of dark pits at the center. The dislocation density from the pit counting is 1.2×10^7 cm^{-2} (12 pits in 10µm^2) which agrees well with that deduced from the TEM analysis.

To the best of our knowledge, this is about 10 times lower than the state-of-the-art TDD of $9.7\text{x}10^7$ cm^{-2} reported for GaN-on-Si.[16]

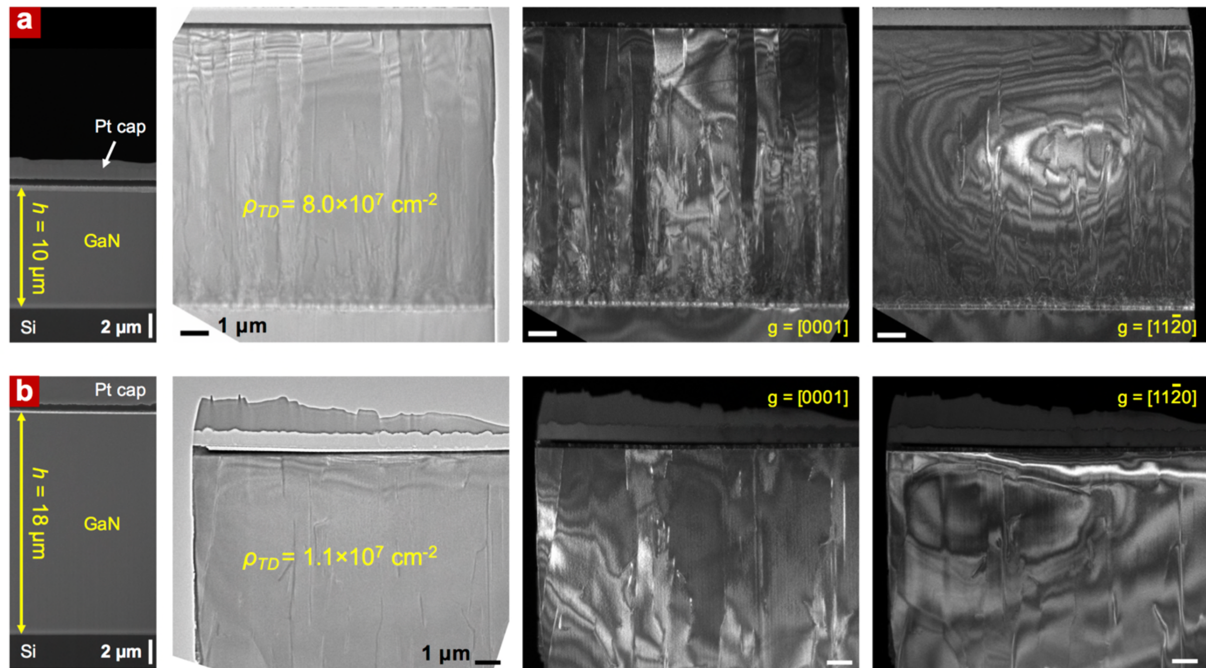

Figure 3.16 Threading dislocation density reduction in thick GaN disk. (a,b) L-R Cross-sectional images of GaN-on-Si by SEM, bright field TEM, dark field TEM at two-beam condition with g=[0001] and dark field TEM with g=[11$\bar{2}$0] for 10 μm thick (**a**) and 18 μm thick (**b**) GaN layers. The high density dislocations at the interface with Si in both samples is reduced as the thickness of the GaN layer increased, reaching 1.1×10^{7} cm^{-2} for 18μm thick GaN layer.

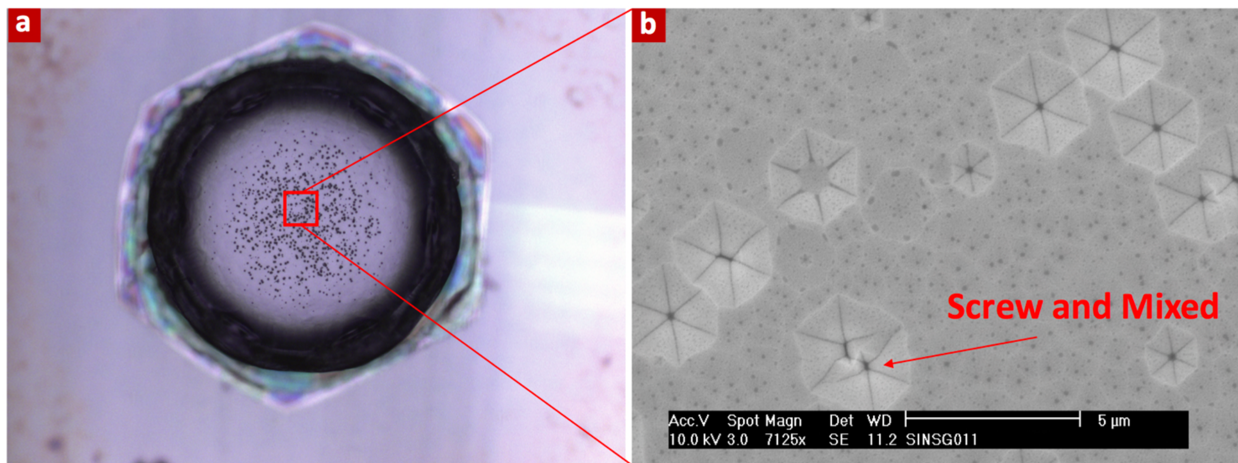

Figure 3.17 Dislocation selective etching. (a) Top view microscope image after etching **(b)** Top view SEM image near the center of the disk where most dislocations were found.

3.6 Demonstration of Vertical GaN MISFET on Si

To highlight the potential of the thick and crack-free GaN-on-Si with low TDD, we fabricated vertical trench-gate normally-off metal-insulator-semiconductor field-effect transistors (MISFETs) employing 19 μm thick drift layers.

For vertical trench-gate GaN MISFETs, after the SAG growth of $n^-/p^+/n^+$GaN (19/0.45/0.2 μm) epitaxial layers, we completely removed the SAG mask layer (SiO_2 and SiN_x) by 10 % diluted HF solution. We re-deposited a 600 nm SiO_2 isolation layer by PECVD, and then performed a mesa isolation etching with the PECVD-SiO_2 layer as a hard mask for a BCl_3/Cl_2-based RIE low damage etching with a RF power of 50 W. After removing the SiO_2 hard mask, we deposited another SiO_2 layer as a gate recess etching hard mask as well as a passivation layer for the devices. We etched 600 nm SiO_2 layer by RIE with a CHF_3/Ar gas mixture to obtain a vertical etching profile of the gate trench, and then etched the gate recess of 1.15 μm with RIE using the mesa isolation conditions. The etched GaN surface was cleaned by 5% tetramethylammonium hydroxide (TMAH) at 80 °C for 10 min and 29 % NH_4OH solution for 10 min with sonication at room temperature, and the sample was immediately loaded to a Beneq TFS200 Atomic Layer Deposition (ALD) system. ALD process was initiated by 20 cycles of TMA pre-pulses and followed by a 50 nm thick Al_2O_3 layer deposition as a gate insulator with a chuck temperature of 200 °C. No post-deposition annealing for the gate insulator was performed. A dry etching by RIE was performed for contact window opening, followed by an electron beam evaporation of a 30nm/70nm Ti/Al metal stack as Ohmic contacts on top of the n^+GaN layer. Finally, a 60nm/120nm Ti/Au was sputtered and dry etched by RIE for the gate metal and pads, in order to achieve a conformal profile at the gate trench sidewall.

Figure 3.18 (a) shows a schematic cross-sectional view of the MISFET structure and **Figure 3.18 (b)** shows a cross-sectional SEM image of the fabricated device. The vertical MISFET consisted of a 450 nm thick intermediate p^+-GaN current blocking layer, and a 200 nm thick n^+-GaN top current source layer, as labeled in **Figure 3.18 (b)**. The gate recess utilized a sequential dry and wet etching in order to result in smooth and ~80° slanted sidewalls and round corners at the bottom of the trench as shown in **Figure 3.18 (b)**. The device transfer curves shown in linear and semi-log plots are shown in **Figure 3.18 (c)** and exhibit a device threshold voltage of ~8 V and an I_{on}/I_{off} ratio of 10^7 approaching that of recently developed GaN-on-GaN trench-gate MISFETs.[17–23] The device output curves are shown in **Figure 3.18 (d)** exhibiting good saturation characteristics.

The MISFET device R_{on} is calculated by considering the device active area. The device trench width is 4 µm and gate width is 50 µm. The pitch of the device was calculated by adding the drift layer thickness 19 µm to the trench width in order to account for the current spreading in the drift region. Therefore, the active area of the device, A_{act}, is 23 µm (pitch) × 69 µm (50 µm gate width + 19 µm drift region thickness) and it is 1.59×10^{-5}cm². R_{on} is calculated

$$R_{on}=\left[\frac{1V\ (V_{DS}=1V)}{5.03\times10^{-4}A(I_{DS}\ at\ V_{DS}=1V\ and\ V_{GS}=20V)}\right]\cdot A_{act}=31m\Omega\ cm \qquad (3\text{-}3)$$

The modest hysteresis observed in the transfer curves (**Figure 3.19**) and the relatively high R_{on} observed for these first vertical GaN-on-Si trench MOSFETs can be further optimized with gate surface treatements[24] and regrowth[22,23], and with engineering the doping profile in the drift layers[25]. Additional work is also required for device edge termination in order to achieve high breakdown voltages in these devices. None the less, we demonstrate here that very low leakage currents and the successful formation of vertical p-n junctions is indeed feasible and led to the demonstration of the first vertical GaN-on-Si trench-gate MISFETs.

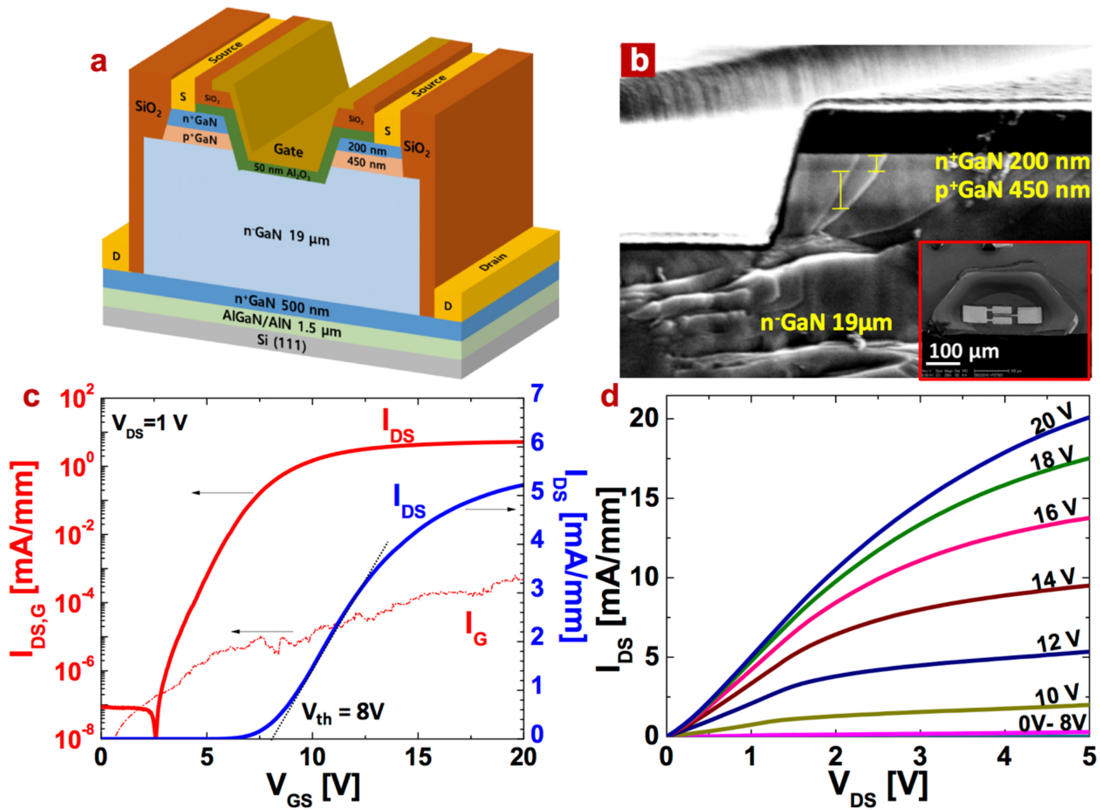

Figure 3.18 First demonstration of normally-off trench-gate GaN vertical MISFET on Si. **(a)** Schematic structure of GaN-on-Si vertical MISFET on 19 μm SAG GaN layer. **(b)** Cross-sectional SEM image of the trench-gate region. Clear p-GaN and nGaN contrast were observed and thicknesses were determined. The inset SEM image shows angled view device image. **(c)** Linear (blue) and log (red) scale transfer I-V characteristics (I_{DS}-V_{GS}) and gate leakage (I_G-V_{GS}) at V_{DS} = 1V **(d)** Output I-V characteristics (I_{DS}-V_{DS}) at different gate voltages in steps of 2V.

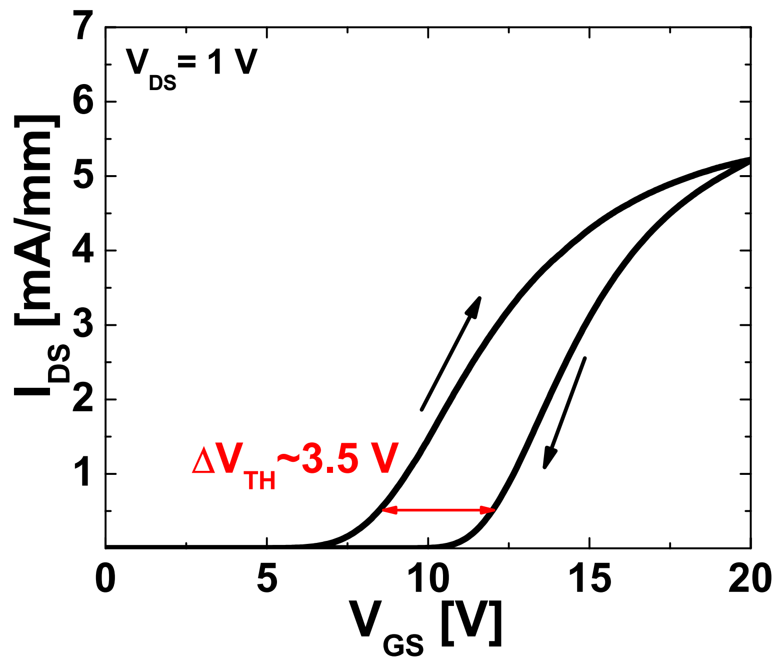

Figure 3.19 Threshold voltage shift. Linear transfer characteristics (I_{DS}-V_{GS}) at V_{DS} = 1V with different voltage sweep direction.

3.5 Conclusion

We demonstrated a new regime of epitaxy in thermal mismatched materials where the thick and crack-free GaN-on-Si is possible. With a systematic approach to understand the cracking behavior and lateral overgrowth to form faceted hexagonal disks on exposed underlying Si surfaces, we were able to grow over 18 μm thick GaN on Si and lower the TDD density to 10^7 cm^{-2}. These results allowed us to demonstrate functional vertical trench-gate GaN MISFETs on Si and pave the way for integrated vertical GaN power and optoelectronic devices on a Si CMOS platform.

3.6 Acknowledgements

The chapter 3, in full, is a reprint of the material as it appears in *Advanced Materials* in 2017 co-authored with Atsunori Tanaka, Woojin Choi, Renjie Chen, and Shadi A. Dayeh. Professor Shadi .A Dayeh conceived and supervised the study and I carried out SAG GaN growth and characterization by SEM and Raman Spectroscopy. Dr. Renjie Chen performed transmission electron microscopy. Woojin Choi optimized the GaN vertical MISFET on Si process and measured electrical characteristics. Prof. Dayeh and I analyzed the data wrote the manuscript and obtained feedback from all authors.

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Chapter 4

Structural and electrical characterization of thick GaN layers on Si, GaN, and engineered substrates

4.1 Introduction

A major challenge in GaN vertical power devices and other large bandgap materials is the high defect density that compromises the performance, reliability and yield. Defects are typically nucleated at the heterointerface and arise from both lattice and thermal mismatches. Here, we report the selective area growth (SAG) of thick GaN on Si and on newly available Qromis Substrate Technology™, QST substrates, that lead to significant reduction of the defect densities to a level that is nearly comparable to that on native substrates by defect annihilation. We performed a parametric study of the electrical properties of the SAG GaN layers by fabricating and characterizing Schottky barrier diodes for SAG GaN layer thicknesses of 5, 10, 15, and 20 μm for GaN-on-Si, GaN-on-QST, and GaN-on-GaN diodes. While thicker layers led to a significant reduction in defect densities and improvement in the diode forward current characteristics, the GaN-on-QST diodes exhibited nearly similar characteristics to the GaN-on-GaN diodes. Further improvement in the device structure and/or SAG growth for GaN-on-Si is needed to achieve

comparable performance as the defect densities in the GaN-on-Si is comparable to that of GaN-on-QST substrates.

The success of single phase growth of gallium nitride (GaN) and indium gallium nitride (InGaN)[1] has fueled the rapid commercialization of GaN devices such as blue light emitting diodes (LEDs) and generated strong interest in GaN as the basis material for next generation high power electronic devices. The recent progress on bulk GaN crystal growth techniques such as Na-flux, Hydride Vapor Phase Epitaxy (HVPE) and ammonothermal methods have made it possible to make vertical GaN devices with low threading dislocation densities (TDDs).[2–4] However, cost, scalability, growth uniformity and device reliability over large areas remain challenges to market adoption of technologies based on these substrates. The heteroepitaxy of GaN on cheap and technologically well-developed substrates such as Si would give an advantage to scalable and cost-effective production and further the monolithic integration to Si CMOS technology. But heteroepitaxial GaN usually suffers from a large TDD which has been a critical barrier for its utility in power electronics since leakage currents and breakdown voltages are strongly correlated to the TDDs and impurities.[5–8] Earlier pioneering work on the heteroepitaxial growth of thick GaN on sapphire substrates has successfully reduced the number of dislocations and showed improved device performances.[9] However, epitaxy techniques developed on sapphire cannot be simply adopted for the growth of GaN-on-Si due to both the large in-plane thermal expansion coefficient (CTE) (5.59×10^{-6} K^{-1} for GaN and 2.6×10^{-6} K^{-1} for Si) and to the 17 % of lattice mismatch which combine to generate tensile stress and cracking in the GaN films that are as thin as 4 µm. Our work demonstrated that we can safely deflect these mismatch stresses by SAG to grow structures that can be as thick as 20 µm for GaN-on-Si without cracking[10]. Here, we utilize these growth techniques to carry out parametric studies on the influence of the thickness (5 µm - 20 µm) of GaN

drift layers on the performance metrics of GaN-on-Si Schottky barrier diodes (SBDs), GaN on newly commercialized Qromis® substrate technology (QST) based on polycrystalline AlN[11] with matched CTE (GaN-on-QST), and benchmark the results relevant to GaN-on-GaN devices. We have succeeded in decreasing dislocation densities in hetero epitaxial GaN by growing thick SAG GaN, as demonstrated using etch pit density measurement and transmission electron microscopy (TEM), and improved SBD characteristics proven by current-voltage (I-V) and capacitance-voltage (C-V) measurements.

4.2 Experimental Detail

The SAG of GaN was performed on three difference substrates; GaN-on-Si, free-standing GaN (SCIOCS) and CTE matched QST substrate (Qromis®) by a 3 × 2” Thomas Swan/Aixtron close-coupled showerhead metal-organic chemical-vapor-phase deposition (MOCVD) system as discussed in Chapter 2 and Chapter 3. The starting GaN-on-Si substrate consists of a 500 nm n-type GaN layer on AlGaN/AlN buffer layers on Si(111) provided by Powdec Inc. The 400 µm thick n-type GaN substrate (SCIOCS) was grown by HVPE and the starting QST substrate (Qromis®) had ~8µm unintentionally doped GaN. The coefficient of thermal expansion (CTE) for the QST substrate is carefully matched with the CTE of GaN resulting in negligible thermal mismatch stresses in the GaN film. We grew a 1 µm n-type GaN layer doped with Si on top of the GaN-on-QST substrate for current spreading underneath the vertical drift layer of the SBDs, a layer that is adopted for all other substrates. The sheet resistances and doping concentrations of n-GaN buffer layer for each substrate were determined by Hall effect measurements and are listed in **Table 4.1**.

Table 4.1. Substrate and buffer layer details and properties.

	GaN-on-GaN	GaN-on-QST	GaN-on-Si
Substrate Growth	HVPE	NA	NA
As received GaN thickness	400 μm	8 μm	1.1 μm
Additional planar buffer layer growth	none	1μm	none
Planar surface layer sheet resistance	0.12 Ω/□	42.3 Ω/□	210 Ω/□
Surface layer doping density	5.5×10^{18} cm^{-3}	7.8×10^{18} cm^{-3}	4.1×10^{18} cm^{-3}
SAG GaN in 350μm diameter dot	5 - 20 μm	5 - 20 μm	5 - 20 μm

For all types of starting substrates, the area of each sample was 5×5 mm^2, and strong edge effects and non-uniformities in the growth were expected: the area is chosen to be small due to the high cost of the substrates. 200 nm SiO_2 layers were deposited over these substrates by plasma enhanced chemical vapor deposition (PECVD) and 4×5 arrays of circular openings were patterned and dry-etched by photolithography and reactive ion etching (RIE). The design of the selective growth masks was specifically optimized for the growth of thick GaN-on-Si which is described in detail in our earlier work.[10,12] Different thicknesses of SAG and unintentionally doped (UID) GaN were grown on each substrate and calibrated to result in thicknesses of 5 μm to 20 μm, at a relatively constant growth rate of 5 μm/hr for all samples, despite differences in the substrate thermal conductivities. These grown structures permitted us to perform parametric studies on the thickness dependence and the effect of substrate composition on the grown material quality and device characteristics. SBDs were fabricated by the electron beam evaporation of 200 nm Ni Schottky contacts on top of the SAG UID GaN dots that is followed by photolithography patterning and etching. The ohmic contacts on the n+GaN planar layer were defined around the UID GaN dot

by photolithography and lift-off process and were composed of a Ti(30 nm)/ Al(70 nm)/Ti(10 nm)/Au(50 nm) non-annealed ohmic contact deposited by electron beam evaporation. For GaN-on-GaN SBDs, the same ohmic contact was evaporated on the back of the substrate. The surrounding peripheries of the metal Schottky contacts were dry etched by BCl_3/Cl_2 RIE to a 1 µm depth to reduce the edge effects and surface leakage currents of the SBDs.

The SBD characteristics were evaluated by performing I-V and C-V measurements using Keysight B1500A semiconductor analyzer. After all electrical measurements, the Schottky metal contacts were completely etched by Ni wet etchant and then the samples were immersed in H_3PO_4:H_2SO_4 solution (HH solution) at 270 °C to selectively etch the threading dislocations under the Schottky contact.[13] The number of etch pits at the surface under the contact were counted under an FEI Apreo scanning electron microscopy (SEM). Cross-sectional TEM images using an FEI Tecnai G(2) F30 S-Twin were also taken to evaluate TDD.

4.3 Evaluation of Defect Densities as a Function of Thickness for Each Substrates

The defect preferential etching under the Ni Schottky contacts was performed on all 12 samples. **Figure 4.1** shows the top-view SEM images of the SAG GaN dot surfaces with an area of 25 μm^2 after defect selective etching. The HH solution reveals mixed and screw dislocations as large hexagonal pits and edge dislocations as small pits.[13,14] The dislocation densities of each sample can be estimated by direct counting of these etched pits and dividing the counted pit number by the 25 μm^2 area. The dislocation densities of the starting substrates are estimated to be ~10^9 cm^{-2} for the GaN-on Si, ~10^8 cm^{-2} for the GaN-on-QST substrate and ~10^6 cm^{-2} for the GaN

substrate. The top view SEM images were chosen at random from 20 SAG GaN dots in the same sample and the etch pit densities are averaged from all of the 20 dots for comparison. As shown in **Figure 4.1**, the GaN-on-Si samples showed a clear linear reduction of the pit density from 1.9×10^{7} cm^{-2} to 3.4×10^{6} cm^{-2} with an increase in the GaN thickness. The same trend of dislocation density reduction was observed in GaN-on-QST samples from 3.5×10^{6} cm^{-2} to 9.0×10^{5} cm^{-2} where the overall etch pit densities were about one order of magnitude smaller than GaN-on-Si. No pits were observed from GaN-on-GaN samples within the area of 25 μm^{2} which indicates that the defect densities of the GaN-on-GaN are less than 1.6×10^{5} cm^{-2} at the surface of the SAG GaN dots.

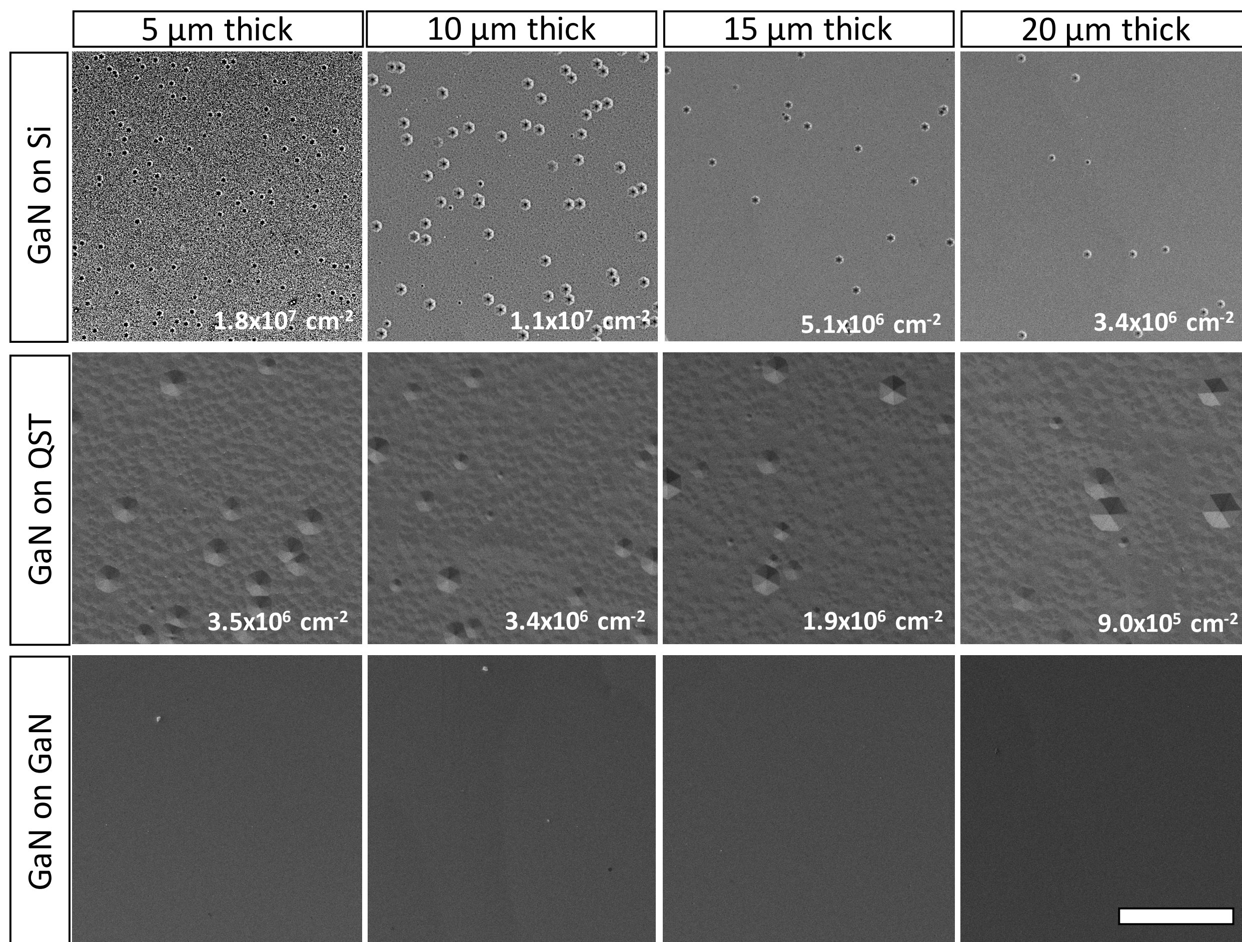

Figure 4.1 Top view SEM images of GaN surface after defect selective etching. Linear reduction of defect densities was observed in GaN-on-Si and GaN-on-QST with increasing the thicknesses. The GaN-on-GaN samples did not show any surface pits after the etching. The scale marker is 10 µm.

The number of dislocations measured by the etch pits densities is usually underestimated because two or more adjacent dislocations may be combined into one large etch pit. Therefore, dislocation density was also estimated from cross-sectional TEM slices made at the center dot for all 12 samples as shown in **Figure 4.2**. It is important to note that the numbers quoted below are deduced from one TEM slice/lamella to support the trends observed with the etch-pit density experiments; an accurate estimate of the TDDs from TEM characterization must be obtained from a large number of TEM slices/lamellas. One can observe that for the 5 μm thick GaN-on-Si, many dislocations nucleated at the interface with the Si substrate and prevailed up to 4 μm from the GaN/Si interface. However, only less than 10 % of dislocations made it to the surface of the 5 μm thick GaN-on-Si dot that was grown for 1 hour, due to the tendency of the dislocations bend and annihilate. As the thickness increased, the probability of annihilation became larger, which resulted in a lower dislocation density for thicker GaN films. Numerous earlier studies have reported the dislocation bending in SAG by epitaxial lateral overgrowth.[15,16] We believe that the dislocation bending in our samples was not caused by either facet termination or dielectric layer masking, but by stress generation and resultant atom/vacancy diffusion from/to the dislocation cores.[17–19]

Interestingly, the bending of dislocation was not only observed in highly stressed GaN-on-Si samples but also in GaN-on-QST samples where there is minimal thermal stress between the GaN and the substrate material. The dislocation density of 20 μm thick GaN-on-Si is almost the same value as 5 μm GaN-on-QST. The reduction of dislocation density in GaN-on-QST could be related to compressive stress generated at the SAG mask / regrowth interface since this reduction of was much faster than in planar regions. Additionally, by the nature of the enhanced reactant collection and growth rates at dot edges, stresses due to thickness non-uniformities (thicker at dot peripheries compared to dot center) are likely to contribute to dislocation bending and annihilation.

In the cross-sectional TEM images of the GaN-on-GaN SAG, there is no evidence of threading dislocations within the TEM lamella width of 10 μm which indicates that the dislocation density for the GaN-on-GaN samples is below 1×10^{6} cm^{-2}.

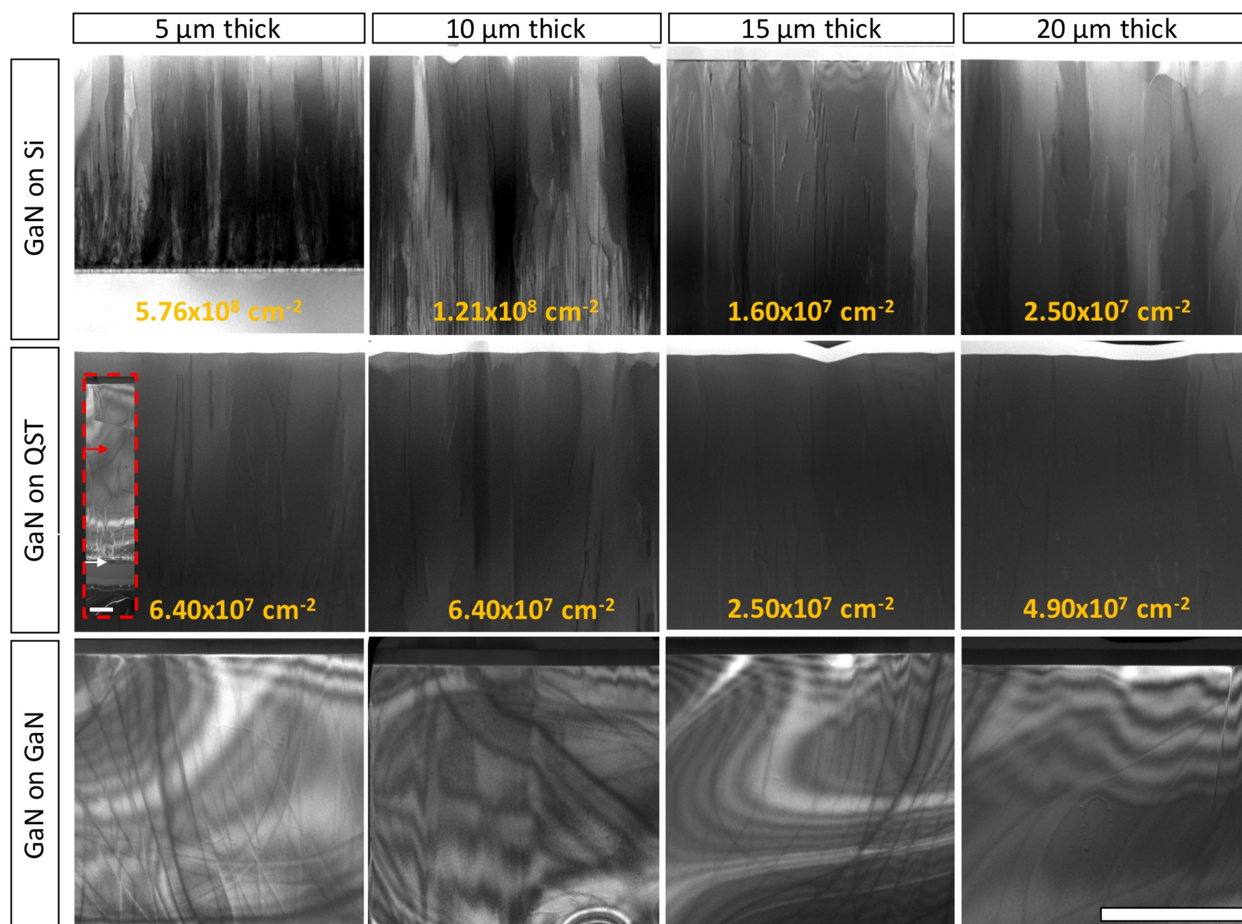

Figure 4.2 Cross sectional TEM images under the Schottky contact (g = [0001]). The width of the imaged sections is 10 μm and the scale bar is 5 μm. The inset for the 5 μm thick GaN-on-QST is a larger field of view TEM image that shows the interface with the Si layer (white arrow) and the location of the pre-grown planar GaN layer (red arrow) prior to SAG. The inset scale marker is 2 μm.

4.4 Evaluation of SAG Electronic Properties by Schottky Barrier Diode Characterization

4.4.1 Current, Capacitance -Voltage Characteristics of SBDs on Each Substrates

The fabricated SBDs were characterized by I-V and C-V measurement. Since no doping impurities were intentionally added during the growth, and at moderate unintentionally doped layers, the SBD current is dominated by thermionic emission (TE). Under forward bias with $V_D > 3kT/q$, the SBD current can be expressed by the fundamental TE diode current equation,

$$I = I_s[\exp(qV_D/nkT)] \tag{4-1}$$

where q is the fundamental electron charge constant, V_D is the voltage applied across the diode, k is the Boltzmann constant, and T is the absolute temperature. I_s can be expressed by[20]

$$I_s = A_{eff}A^{**}T^2 \exp(-q\phi_{B(IV)}/kT) \tag{4-2}$$

where A_{eff} is the effective area of the SBD contact and A^{**} is the Richardson constant. The diode ideality factor, n, and the Schottky barrier height, $\phi_{B(IV)}$, are extracted by fitting the semi-log I-V characteristics for each diode. The diode turn-on voltage is defined as the inflection voltage that is determined by extrapolating a fitted line to the linear region of the forward I-V characteristics.

For a standard reverse biased SBD, the carrier concentration can be extracted from changes in the capacitance by depletion width modulation with applied bias according to,[20]

$$N_d = \frac{2}{q\varepsilon_0\varepsilon_s}\left[-\frac{1}{d(1/C_d^2)/dV}\right] \tag{4-3}$$

where ε_0 is the permittivity of free space, ε_s is the dielectric constant of the semiconductor material and C_d is the depletion layer capacitance. The carrier concentration, N_d, is estimated from

the slope of $1/C_d^2$ as a function of voltage. The intercept of this $1/C_d^2$ with the voltage axis gave the built-in potential which was used to estimate the barrier height according to,

$$\phi_{B(CV)} = V_{bi} + \varphi_n \tag{4-4}$$

Here, $\varphi_n = kT/q \ln(N_c/N_d)$ is the doping potential that is determined for the doping concentration determined from eq. (4-3). The effective density of states in the conduction band edge is given by $N_c = 2(2\pi m^* kT/h^2)^{\frac{3}{2}}$, where the effective electron mass of GaN is $m^* = 0.22m_0$.[21]

Figure 4.3 shows the linear and semi-log scale I-V characteristics for GaN-on-Si SBDs with different thicknesses. For the 5 μm thick GaN-on-Si sample, the incomplete formation of hexagonal facets for such thin layers does not relieve thermal stresses as previously described,[10] and as a result, there were only three uncracked GaN dots out of 20 dots in this sample. The number of uncracked dots increased with GaN film thickness by deflecting the stresses to the surface hexagonal facets that were complete and flat. The reverse leakage current in the SBD decreased linearly with increasing GaN thicknesses, in accord with the linear reduction of dislocation densities. One of the major conduction paths for current in metal-contacted GaN is known to be through screw dislocations whereas edge type dislocations retain the Schottky contact characteristics with metals[22]. The reduction of the screw dislocations verified by **Figure 4.1** and **Figure 4.2** contributed significantly to the reduction of leakage currents from 10^{-1} A/cm^2 to 10^{-3} A/cm^2. In addition, the slope of the linear I-V plots should ideally decrease with thickness since the diode resistance, $R_{diode} = tA_{eff}/q\mu n$ should linearly increase with thickness, where t is the thickness of the drift layer, q is the electron charge, n is the free electron concentration in the drift layer and μ is the electron mobility in the drift layer.[5] However, the slope of the linear I-V plots shown in **Figure 4.3** increased with thickness, which suggests an increase of the electron mobility

assuming that the unintentional n-type doping in the drift layer does not change for 5-20 μm thick drift layers. Earlier studies have shown that changes in the background (O and Si) doping concentration in the growth direction (c-axis) during SAG GaN growth were confined to the first 5 μm.[23–25] By considering the potential for Coulombic interaction between electrons and charged dislocation lines, the large reduction of TDDs significantly improved the electron mobility in the drift layer for thicker GaN,[26] which we estimated to be, on average, about three times higher for the 20 μm thick layers than the 5 μm layer. The absolute numbers for the mobility are not reported because of the lack of a specific method to accurately measure the contact and series resistances in our structures. It is important to note that changes in the background doping concentration due to TDD annihilation and dominance of surface leakage current or confinement of current transport to the outermost layers of the drift region may also contribute to the lower R_{on} of the thicker GaN drift layers. As shown in the **Table 4.2**, the Schottky ideality factor, barrier height and turn-on voltage were also improved with increasing the GaN thicknesses. These improved characteristics are attributed to the improved Schottky contact interface quality with fewer surface defects for thicker GaN films.

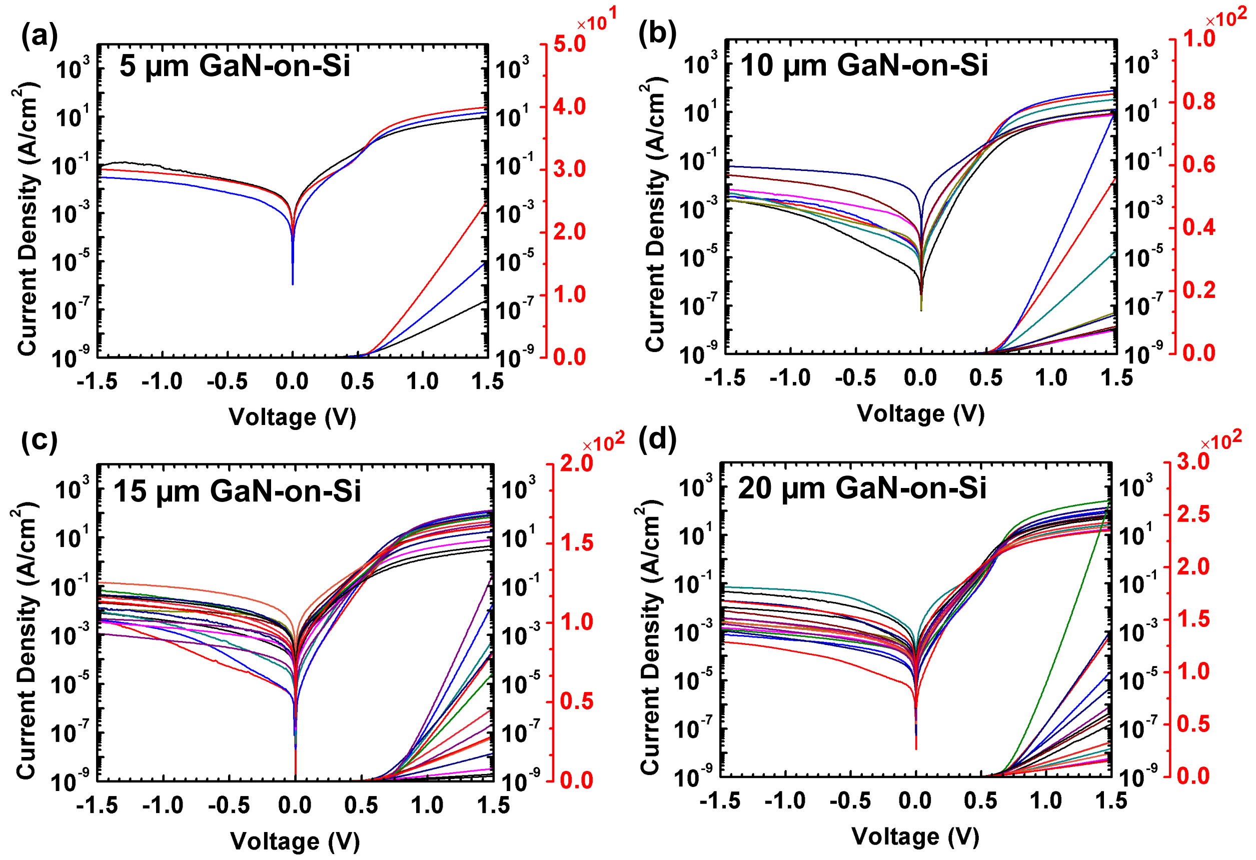

Figure 4.3 Linear and semi-log scale I-V characteristics of GaN-on-Si SBDs with different thicknesses of (a) 5 µm, (b) 10 µm, (c) 15 µm, and (d) 20 µm. The red axis shown in the right side is the linear scale axis.

Table 4.2 GaN-on-Si SBD characteristics.

	5 µm thick (GaN-on-Si)		**10 µm thick (GaN-on-Si)**		**15 µm thick (GaN-on-Si)**		**20 µm thick (GaN-on-Si)**	
	Best	Avg±stdev	Best	Avg±stdev	Best	Avg±stdev	Best	Avg±stdev
Ideality Factor	2.65	3.81±1.45	2.05	3.01±0.90	2.40	3.32±0.60	**1.13**	2.36±0.60
V_{on} (V)	0.64	0.62±0.03	0.66	0.61±0.03	**0.79**	0.70±0.06	0.76	0.67±0.05
$\phi_{B(IV)}$ (eV)	0.60	0.55±0.06	0.63	0.57±0.05	0.64	0.56±0.04	**0.73**	0.62±0.06
$\phi_{B(CV)}$ (eV)	1.21	1.13±0.06	1.16	1.11±0.03	**1.30**	1.19±0.05	1.13	1.11±0.02

* The values in bold font show the best values among all measured devices.

Figure 4.4 and **Figure 4.5** show the linear and semi-log scale I-V characteristics for GaN-on-QST and GaN-on-GaN SBDs with different thicknesses. The leakage currents and forward SBD characteristics are better than those obtained on GaN-on-Si SBDs as further discussed below. In contrast to the GaN-on-Si SBDs, there is no clear correlation between SBD characteristics and GaN thicknesses. We attribute this to the lower number of screw dislocations that results in negligible degradation of the leakage current. However, we observed some inhomogeneity in the SBD characteristics for GaN-on-QST and GaN-on-GaN that are due to the interface roughness of the non-optimized Schottky contacts.[27] With SEM, we observed that the long-range (several microns) surface roughness for GaN-on-QST substrates increased with thickness and believe that this increase in surface roughness led to an increase in the leakage current with film thickness as observed in **Figure 4.6 (b)**. In addition, morphological changes within a given array contribute to the spread of the characteristics as further discussed for **Figure 4.7- Figure 4.9**. Table III and IV show that the lowest ideality factors in GaN-on-QST and GaN-on-GaN are quite similar; however, the uniformity and standard deviations of GaN-on-GaN are superior to those of GaN-on-QST. The ideality factors, barrier heights, and turn-on voltages for GaN-on-QST and for GaN-on-GaN were superior to those of GaN-on-Si. It is also important to note that the R_{on} and the currents obtained on the GaN-on-GaN SBDs did not scale with the different drift layer thickness further suggesting that series resistances (spreading resistance under the SBD dot) or contact resistances dominate the overall impedance of the SBD.

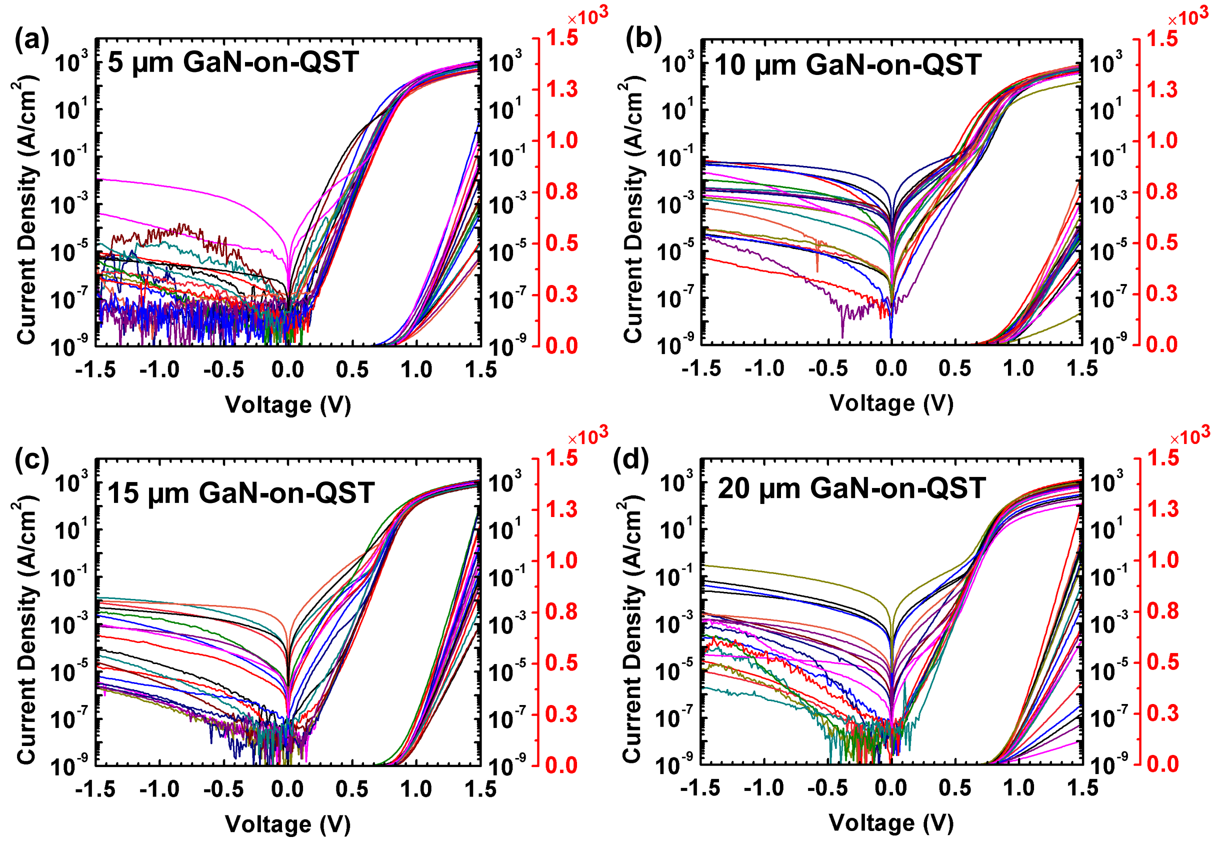

Figure 4.4 Linear and semi-log scale I-V characteristics of GaN-on-QST SBDs with different thicknesses of (a) 5 µm, (b) 10 µm, (c) 15 µm, and (d) 20 µm. The red axis shown in the right side is the linear scale axis.

Table 4.3 GaN-on-QST SBD characteristics.

	5 µm thick (GaN-on-QST)		**10 µm thick (GaN-on-QST)**		**15 µm thick (GaN-on-QST)**		**20 µm thick (GaN-on-QST)**	
	Best	Avg±stdev	Best	Avg±stdev	Best	Avg±stdev	Best	Avg±stdev
Ideality Factor	**1.11**	1.31±0.31	1.47	1.74±0.78	1.58	1.98±0.24	1.18	1.51±0.30
V_{on} (V)	0.98	0.95±0.03	**1.01**	0.95±0.05	0.93	0.89±0.02	0.94	0.91±0.01
$\phi_{B(IV)}$ (eV)	**0.96**	0.89±0.07	0.89	0.78±0.06	0.81	0.70±0.05	**0.96**	0.84±0.08
$\phi_{B(CV)}$ (eV)	1.37	1.34±0.03	**1.39**	1.35±0.02	1.32	1.30±0.02	1.33	1.29±0.02

* The values with bold font show the best values among all measured devices.

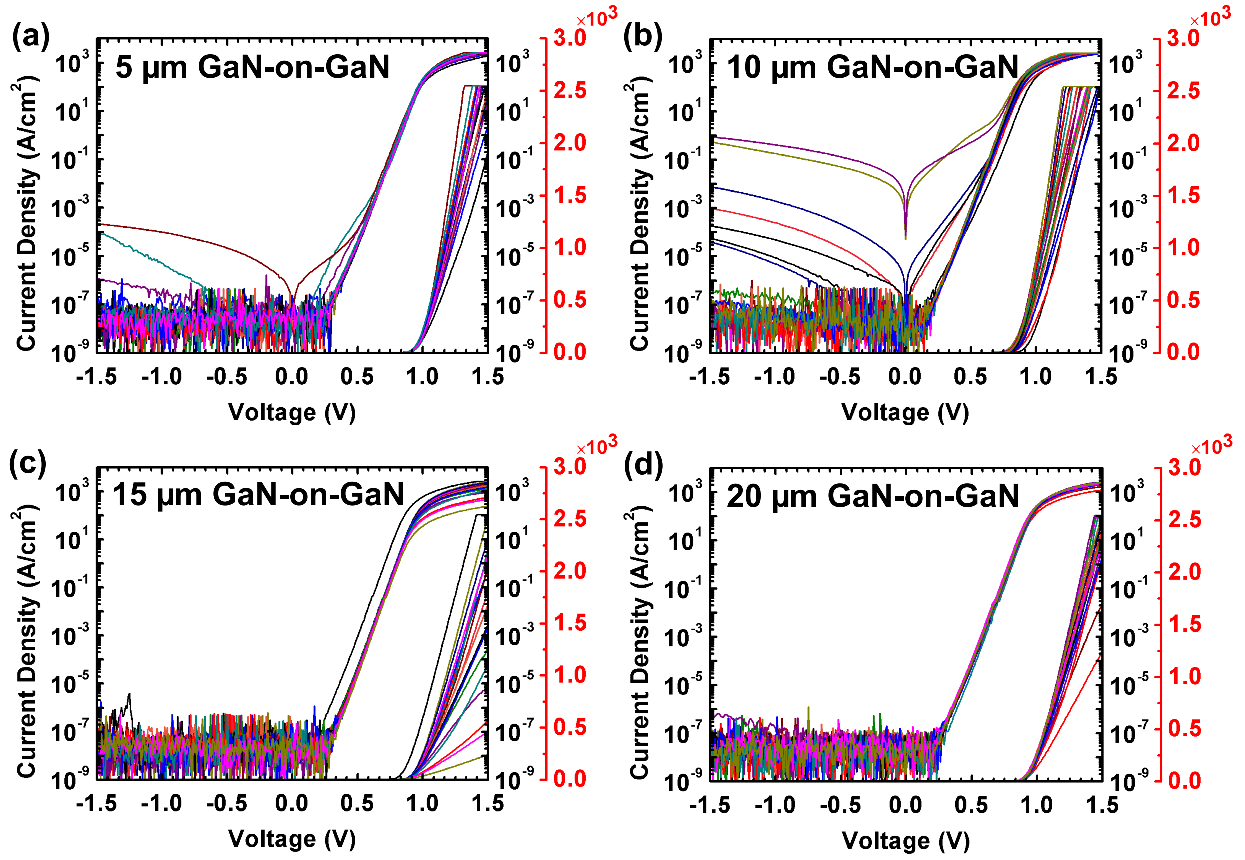

Figure 4.5 Linear and semi-log scale I-V characteristics of GaN-on-GaN SBDs with different thicknesses of (a) 5 µm, (b) 10 µm, (c) 15 µm, and (d) 20 µm. The red axis shown in the right side is the linear scale axis.

Table 4.4 GaN-on-GaN SBD characteristics

	5 µm thick (GaN-on-GaN)		10 µm thick (GaN-on-GaN)		15 µm thick (GaN-on-GaN)		20 µm thick (GaN-on-GaN)	
	Best	Avg±stdev	Best	Avg±stdev	Best	Avg±stdev	Best	Avg±stdev
Ideality Factor	1.13	1.16±0.03	1.16	1.23±0.13	**1.11**	1.12±0.01	1.12	1.14±0.02
V_{on} (V)	**0.98**	0.96±0.01	0.94	0.89±0.02	0.96	0.93±0.02	0.95	0.94±0.01
$\phi_{B(IV)}$ (eV)	**1.09**	1.07±0.02	1.00	0.95±0.07	**1.09**	1.08±0.01	**1.09**	1.06±0.02
$\phi_{B(CV)}$ (eV)	1.35	1.22±0.07	**1.37**	1.22±0.06	1.31	1.20±0.08	1.29	1.06±0.02

* The values in bold font show the best values among the all measured devices.

Figure 4.6 summarizes the I-V characteristics for the best devices for any given SAG thickness among the different studied substrates. For the thickest and best performance devices, the leakage current for the GaN-on-Si SBDs were still about 4 orders of magnitude higher than those of the other two substrates. Given that all structures are grown similarly and are expected to have similar surface leakage currents, the large leakage current in GaN-on-Si SBDs cannot be attributed to surface current leakage. We believe that the significant increase in the leakage current may come from the buffer leakage current at the lower and defective GaN/AlGaN layers near the interface with Si. The GaN-on-Si substrate contains only 500 nm n+GaN grown on top of 1.1 μm undoped buffer and transition layer that is highly defective and that is used for current spreading under the SBDs such that the high density of defects prior to annihilation penetrated deeper into the GaN drift layer. In contrast, the 8 μm planar undoped buffer layer on the QST substrate readily contains the highly defective regions. Since we grew a 1 μm thick n+GaN layer (**Table 4.1**) on top of this buffer layer, current spreading under the SAG pattern has to be solely contained in the 1μm n+GaN layer. This shields the SBDs on QST substrates from current passage in the defective regions (contained in the 8 μm buffer layer) at the substrate interface and therefore explains their much lower leakage currents. Engineering the current spreading layer doping concentration and thickness has been shown to be highly influential on the breakdown voltages of vertical devices.[28] Further improvement of the SAG layer growth and structure as well as the device structure for GaN-on-Si is required in order to achieve comparable levels of leakage current and overall SBD performance. For all devices, the Schottky barrier height measured by I-V are smaller than those obtained from C-V measurements. The differences in these values might come from the presence of an insulating layer or charges existing at the Schottky interface, deep impurity levels, image force barrier lowering, and edge leakage currents.[21,29,30] Consistently through both types of

Schottky barrier height measurements, the barrier heights for GaN-on-Si SBDs were significantly lower compared to those made on other substrates which is most likely due to the higher leakage currents for SBDs made on Si.

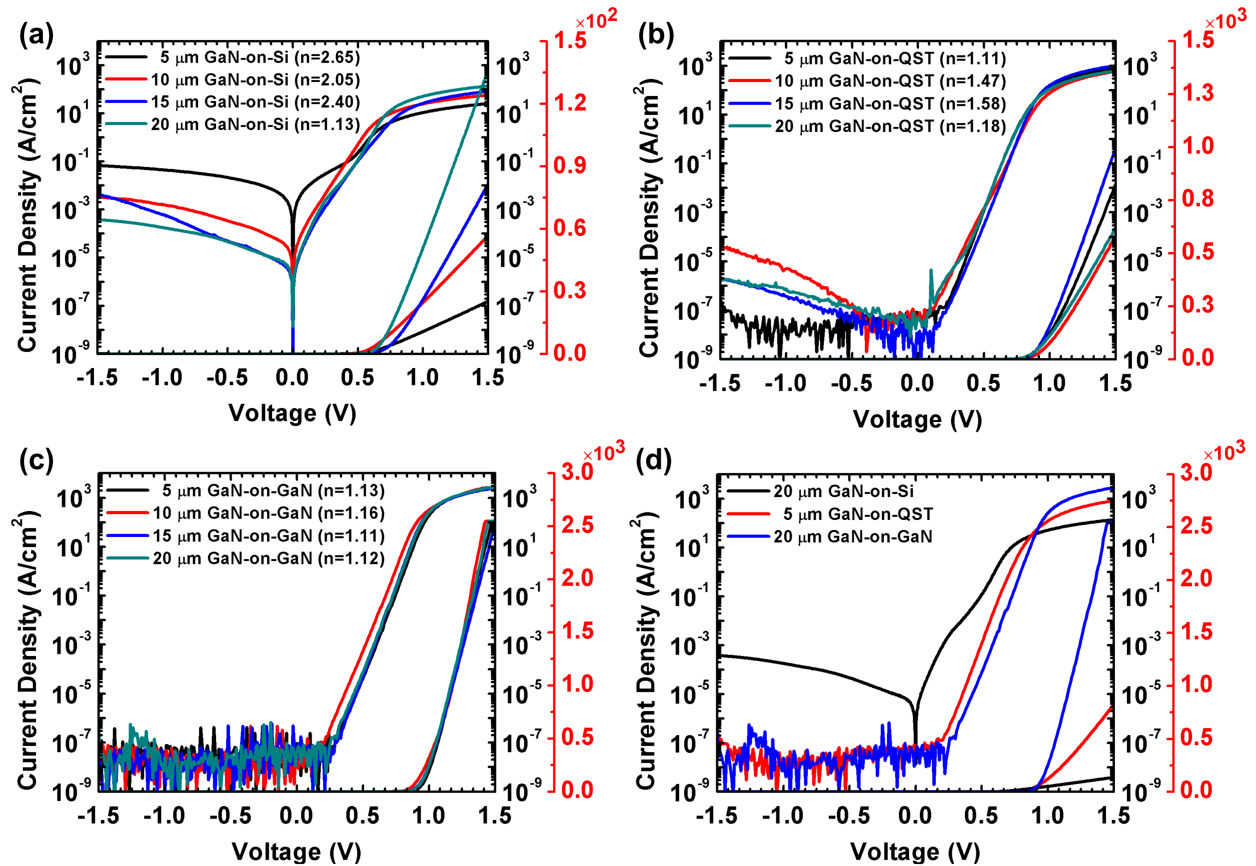

Figure 4.6 Linear and semi-log scale I-V characteristics of the best SBDs for any given SAG thickness and on all studied substrates for (a) GaN-on-Si, (b) GaN-on-QST, (c) GaN-on-GaN. (d) Comparison of the best performance devices from all three types of substrates.

4.4.2 Geometrical Effect of Dislocation Densities and Ideality Factors

The SAG GaN SBDs do not only depend on the growth thickness and substrate type but also on the location of the GaN dots within a given array. As noted above, there are 20 SAG GaN dots on the same substrate and the results were averaged over these 20 dots. **Figure 4.7** shows the mapping of the defect densities over all dots in the array per substrate. As noted earlier in **Figure 4.1** and **Figure 4.2**, the defect densities in GaN-on-Si and GaN-on-QST decreased linearly with increasing the thickness. However, the outer most GaN dots tend to show relatively lower defect densities than the dots near the center region, due to their larger height compared to the central ones. This higher growth rate originates from the enhanced Ga adatom collection at the outer most GaN dots since the effective dielectric mask spacing is large as discussed in Chapter 2.[12] The ideality factor color map is shown in **Figure 4.8**. As previously discussed, the ideality factor for GaN-on-Si samples decreased linearly with the thickness whereas the GaN-on-QST and GaN-on-GaN were readily better and did not show a notable further improvement. As shown in **Figure 4.8**, there is a trend that the outer most samples showed higher relative ideality factor than those of the center dots. This discrepancy comes from the surface roughness due to the fast growth rate for the outer most dots that result in non-ideal Schottky contact interfaces. Even in the GaN-on-Si samples, a similar trend can be observed from **Figure 4.8**, but the reduction of defect densities at the edges was much more significant than the influence of surface roughness on the ideality factor. Therefore, the average ideality factors reduced linearly by increasing the thicknesses.

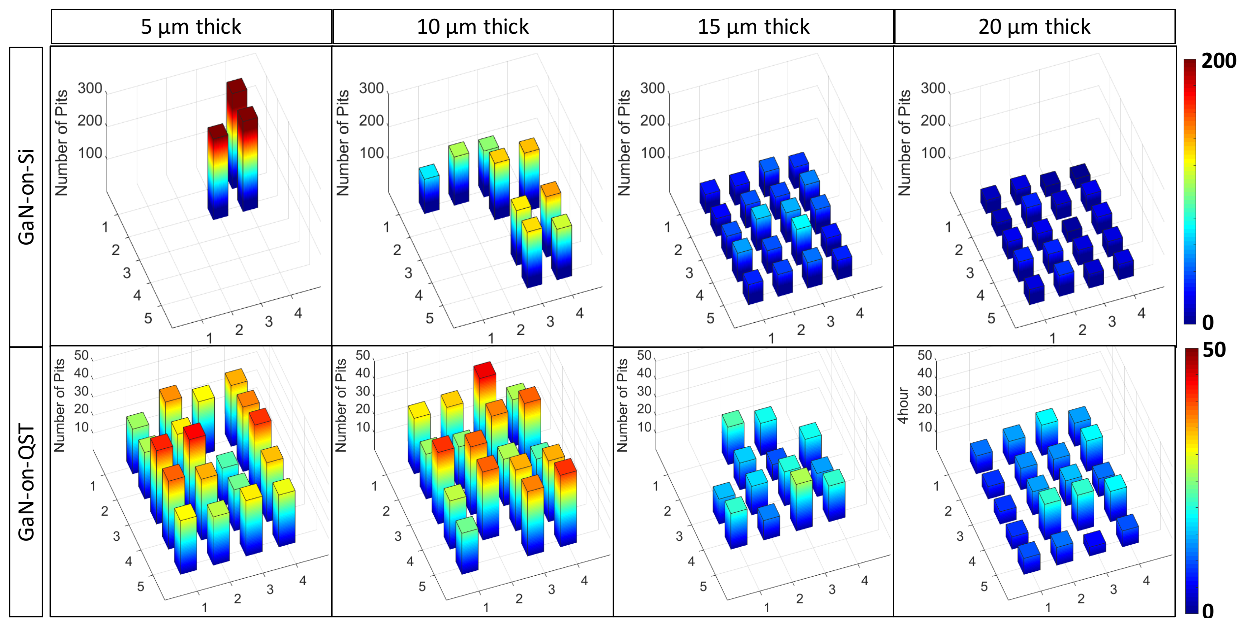

Figure 4.7 3D color map of etch pit counts for each dot in the SAG arrays on the GaN-on-Si and GaN-on-QST.

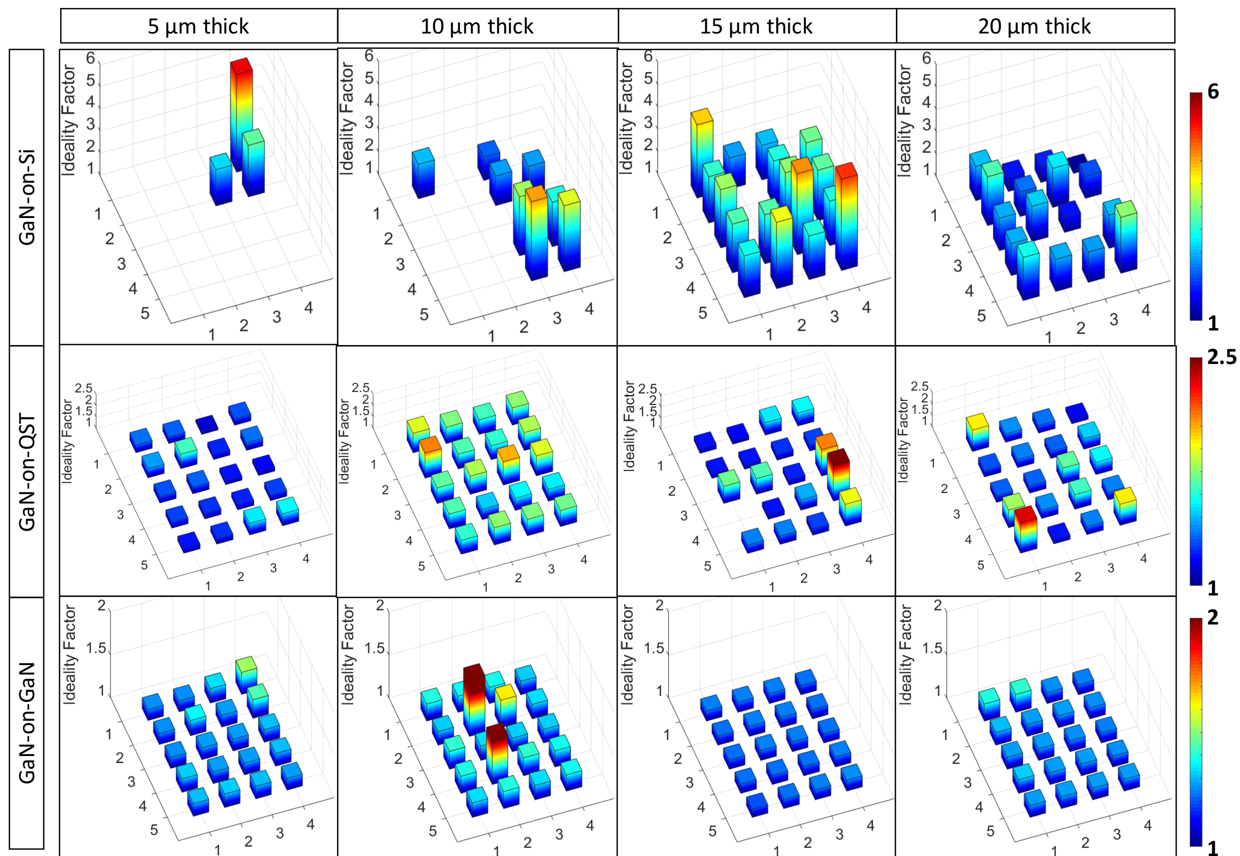

Figure 4.8 3D color map of ideality factors of each dot in the SAG arrays for the GaN-on-Si, GaN-on-QST and GaN-on-GaN.

4.4.3 Effect of Geometrical FCarrier Concentration and Sample Holder on the Carrier Concentrations

The grown SAG GaN is highly conductive even without any dopant flow during the MOCVD growth. It is very well known that nitrogen vacancies in GaN act as donner impurities and increase the carrier concentration. However, the level of the carrier concentration in SAG undoped GaN is far beyond the value that can be explained by nitrogen vacancies. There are several reports about unintentional doping from dielectric mask or SiO_2 residues at the regrowth interface.[31–33] Since both of Si and O atoms can act as donor-type impurities in GaN, the impurity diffusion from the SAG mask can result in high doping in SAG GaN but those impurity diffusion should only affect carrier concentration of SAG GaN near the interface of SiO_2. In terms of carrier concentration map in **Figure 4.9**, there was no clear dependence of the thicknesses and substrates for the samples fabricated in this work and also for all the conditions, the lowest carrier concentration was consistently obtained from the dots fabricated at the four corners of the array. These results contradict impurity diffusion either from dielectric mask or from substrate because the dots at the four corners of the array are closer to large SiO_2 mask region and edge of the substrate and we must have seen thickness dependence of the carrier concentration if it is from GaN/Si interfaces. Therefore, the lower carrier concentration at the four corner can be explained by (i) reduced impurity incorporation by the fast growth, (ii) increased carbon concentration by the lower local V/III ratio due to the higher collection of Ga adatoms, (iii) slightly lower growth temperature near the edge of the substrate, etc.

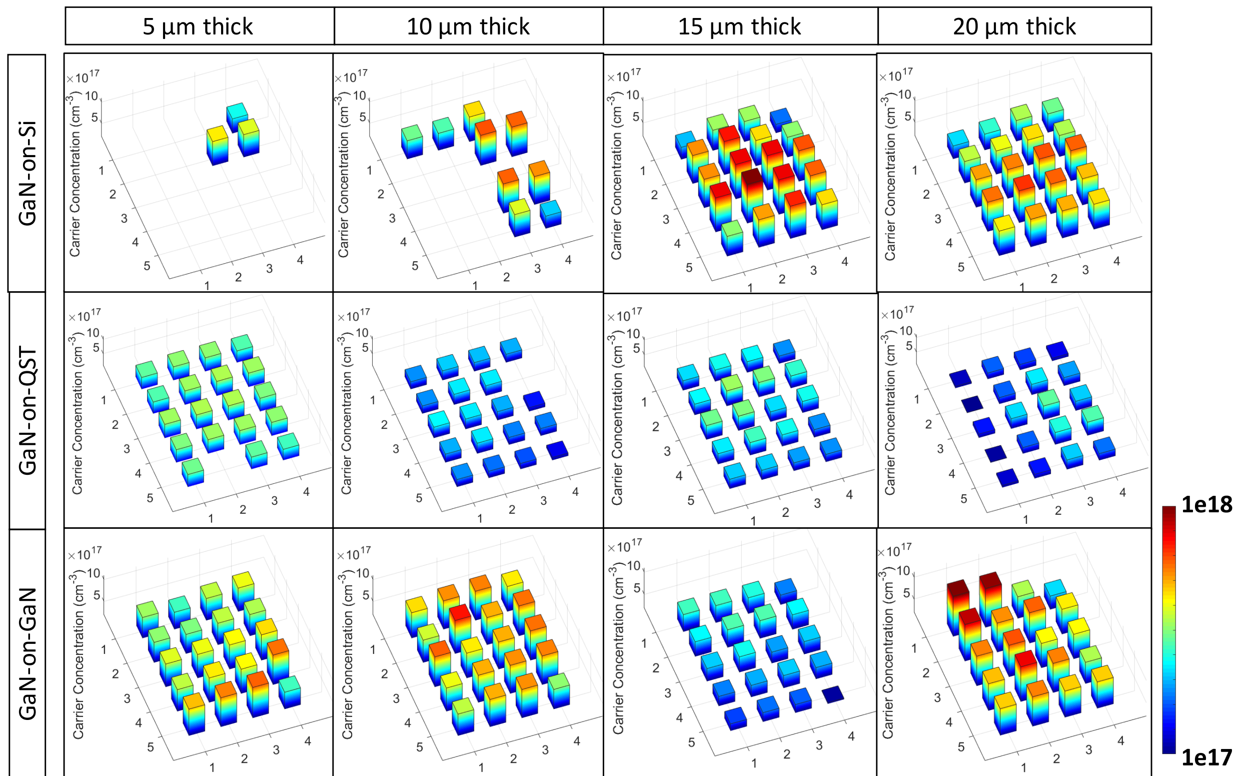

Figure 4.9 3D color map of carreir concentration of each dot in the SAG arrays for the GaN-on-Si, GaN-on-QST and GaN-on-GaN.

For all SAG GaN discussed thus far, we have used a sample holder composed of a sapphire wafer with machined holes near the center and tha can fit $5mm^2$ samples in order to prevent deposition of materials on the susceptors when we were using $5mm^2$ piece substrates. During GaN growth, it is possible for any contaminant at the surface of the sample holder to decompose/diffuse to SAG GaN substrate. Therefore, we carried out a growth run without the sapphire holder risking growth on the susceptor surface. **Figure 4.10** shows the sapphire holder and impurity concentration measured by C-V characteristics. As shown in **Figure 4.10 (b)** and **(c)**, the removal of the sapphire holder successfully reduced the overall carrier concentration on average from 3.7×10^{17} cm^{-3} to 5.2×10^{16} cm^{-3}. While the overall carrier concentration was reduced about one order of magnitude, the trend of geometrical effect was preserved. The source of unintentional doping in SAG GaN is still under investigation and even without the sapphire holder, carrier concentration of SAG GaN-on-Si was still slightly higher than GaN on QST. This suggests further optimization of the growth condition for each substrates. Further analysis by secondary ion mass spectrometry may be required to understand the origin of the unintentional doping impurity and the source of the low carrier concentration at the edge of the array.

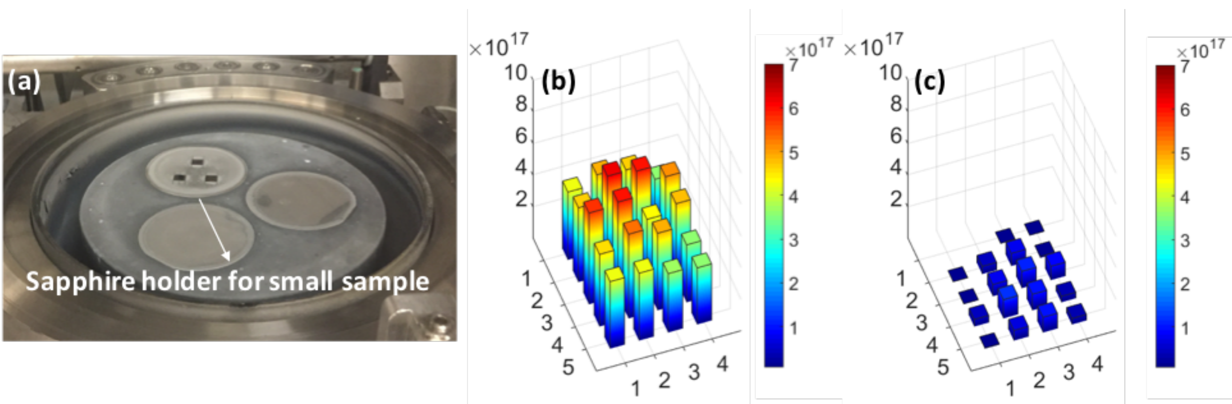

Figure 4.10 **(a)** A picture showing MOCVD growth chamber. The sapphire holder is to prevent deposition of materials on the susceptor surface. Carrier concentration mapping of SAG GaN on QST **(b)**before and **(c)**after the removal of the sapphire holder.

4.4.3 Breakdown Characteristics of GaN SBDs on QST substrate

Through a careful optimization of the growth conditions, we were able to achieve low carrier concentration in the drift layers of GaN-on-QST SBDs. The device breakdown characteristics for 4 SBDs are shown in **Figure 4.11** (SBD 1 - SBD 4 respectively). The carrier concentrations for these SBDs were determined by C-V measurement technique and are listed in **Table 4.5**. The breakdown voltages (V_{BR}) increased with decreasing the carrier concentration as shown in the **Table 4.5**. These breakdown voltages agree with simple one-dimensional calculations of the maximum electric field at the Schottky contact ($E_{max} = qN_d W_{dep}/\varepsilon_0\varepsilon_s$, where W_{dep} is the depletion width at V_{BR}). The breakdown electric field was estimated to be 0.91-2.47 MV/cm which is still lower than the theoretical value of 3.75 MV/cm especially for higher biased device (SBD 4).[34,35] This is mainly attributed to non-optimized device structure, especially lack of an edge-termination process and the presence of large fields at the edge of the contact with high applied voltage.

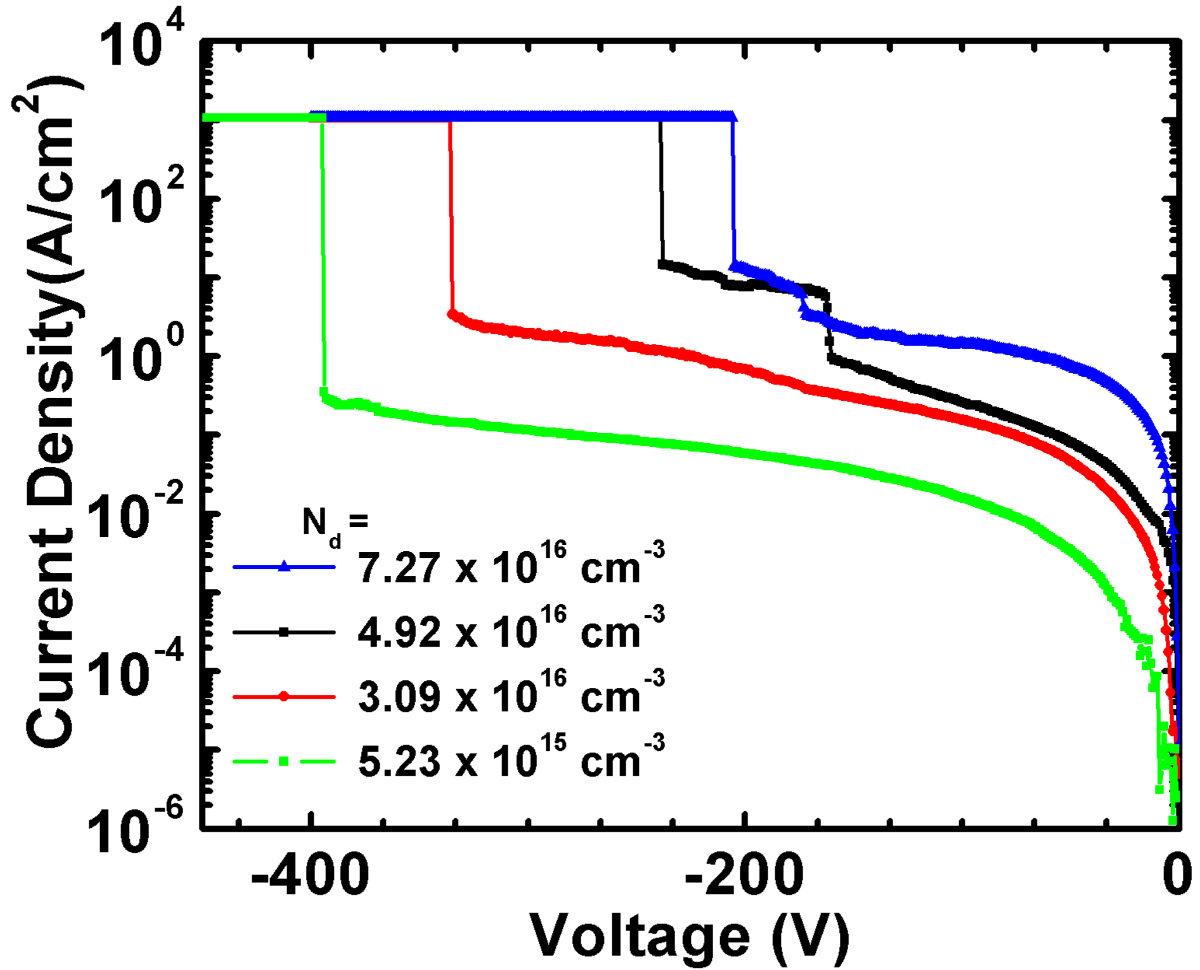

Figure 4.11 Breakdown characteristics of GaN-on-QST SBDs fabricated on 20 μm thick drift layers with different carreir concentrations. All the SBDs have no edge termination.

Table 4.5 SBD breakdown characteristics for GaN-on-QST substrates with different carrier concentrations.

	SBD 1	SBD 2	SBD 3	SBD 4
N_d	7.27×10^{16} cm^{-3}	4.92×10^{16} cm^{-3}	3.09×10^{16} cm^{-3}	5.23×10^{15} cm^{-3}
V_{BR}	-205	-239	-336	-395
W_{dep} at 0 V	116 nm	141 nm	178 nm	434 nm
W_{dep} at V_{BR}	1.67 μm	2.19 μm	3.28 μm	8.63 μm
E_{max}	2.47 MV/cm	2.19 MV/cm	2.06 MV/cm	0.92 MV/cm

4.5 Conclusion

In summary, we compared the thickness and substrate effects on the material and device characteristics for SAG GaN-on-Si, GaN-on-QST, and GaN-on-GaN. The selective area growth of heteroepitaxial GaN on foreign substrates successfully reduced the significant number of dislocations by annihilating TDDs with thick GaN layer growth. The leakage current in GaN-on-Si decreased linearly with increasing thickness due to the reduction of screw dislocations. Thermally matched QST substrates showed promising device characteristics that were comparable to the devices fabricated on bulk GaN substrates. Even though the GaN-on-Si samples showed comparable number of dislocation densities to the QST substrates, the leakage currents were still higher than those of the QST substrate and GaN substrate. This may originate from the leakage in the thin buffer layers for the GaN-on-Si substrates. Further improvement of epitaxial structure may further enhance the performance of the GaN-on-Si samples to be comparable to those on QST and GaN substrates.

4.6 Acknowledgements

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supported the use of Nitride MOCVD system. Prof. Dayeh and I analyzed the data wrote the manuscript and obtained feedback from all authors.

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