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Molecular Beam Epitaxy of Low Dimensional Electron Systems for Topological Quantum Computation

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Molecular Beam Epitaxy
of Low Dimensional Electron Systems
for Topological Quantum Computation

A dissertation submitted in partial satisfaction

of the requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

Mihir Pendharkar

Committee in charge:

Professor Christopher J. Palmstrøm, Chair

Professor Arthur C. Gossard

Professor Umesh K. Mishra

Professor Stephen D. Wilson

December 2019

The dissertation of Mihir Pendharkar is approved.

Professor Arthur C. Gossard

Professor Umesh K. Mishra

Professor Stephen D. Wilson

Professor Christopher J. Palmstrøm, Committee Chair

November 2019

Molecular Beam Epitaxy
of Low Dimensional Electron Systems
for Topological Quantum Computation

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by

Mihir Pendharkar

*Dedicated to Aai and Baba,
you have made all the difference.*

Acknowledgements

गुरु गोबिन्द दोउ खडे काके लागूँ पाँय |
बलिहारी गुरु आपने गोबिन्द दियो बताय ||

First and foremost, I must begin by thanking my research advisor, Prof. Chris Palmstrøm. I didn't know anything about vacuum when I joined his group and the 300 pages ahead in this dissertation are a sheer feat of vacuum science. While in 2011-12, I didn't know vacuum, I often doubt whether I even knew anything beyond vacuum. I must thank Prof. Palmstrøm for believing in me and creating an environment so conducive to learning and research that the last seven years of my MS and my PhD at UCSB have been a breeze. I learnt the basics, the advanced and even the most obscure and surprisingly useful tricks of the trade from him. He has always led by example and I am delighted to say that on the systems I worked with, he was often the first one to pick up a wrench at the sign of trouble. It mustn't come as a surprise that his lab is world renowned for its unique MBE hardware, and while we may lack a dedicated technician to keep the mammoth machinery running, we are trained to make up for it in dedication!

Next, I must thank my PhD committee. I didn't know that my PhD would take me towards the path of hunting for non-abelian particles in pristine materials grown by MBE, a hunt started by Prof. Art Gossard. He has also led by example and I thank him for being a great resource. Having lunch with him on occasion and discussing the scientific advances in the field, while also talking about everything else, was an unparalleled opportunity I had as a PhD student in the MBE club. I also want to thank Prof. Umesh Mishra, who taught me how to think about electrons and band diagrams in a way that has made my life much easier as an electrical engineer. His ECE 221 series courses are the classics for an aspiring electrical engineer. In fact, I remember students bringing folding chairs with them to his classes as it wasn't guaranteed that one would find a vacant seat in the classroom. Though this dissertation mentions magnetism and spins as the premise to most conversations, my only formal training of magnetism comes from Prof. Steve Wilson. I want to thank him for the candid discussions and the insight he has provided on my research progress.

This PhD wouldn't have happened had it not been for the members of the Palmstrøm group. Brian Schultz and Sukgeun Choi anchored the boat when it came to managing the lab behind the scenes and making sure the balance between equipment maintenance and research progress was always maintained. We got extremely valuable insight from them on the history of the machines we were working on, saving valuable time. Jason Kawasaki, Borzoyeh Shojaei and Sahil Patel were very patient and understanding mentors I was fortunate to have. They taught me the basics of tightening bolts on UHV systems and removing water lines – both made easier if you know the right technique. Javad Shabani, Joon Sue Lee and Shouvik Chatterjee were the postdocs whose experience of MBE labs at other universities, enriched my own experience without ever having to travel. Rachel Koltun, Tony McFadden, Nate Wilson, Anthony Rice, Sean Harrington, Jay Logan, Ryan Need, Dan Pennachio, Tobias Brown-Heft,

Aranya Goswami, Alex Chang, Hadass Inbar, Elliot Young, Connor Dempsey, Michael Seas, Rony Ballouz, Jason Dong, Aaron Engel, Luca Alt and Michelle Labrecque were essential members of the team and great colleagues to have (4pm) breaks, lunches and surprisingly often, dinners, with. Had it not been for their jovial spirit I'm not sure if I would've felt like coming into the lab on days I wasn't required to.

The UCSB MBE lab (*Le Club Epitaxie*) is the wealth of knowledge that every MBE PhD student would like to have. As I couldn't have worked on any more materials than I already did work on, the MBE lab and MBE meetings provided me the knowhow about where the world was going. In fact, if we had an issue with our machines or with our material systems, a brief conversation with the PhD students, postdocs and most importantly John English and Kurt Olsson was a quick way to find out if someone had already figured out a workaround for it. John English is the glue that holds the MBE lab together and his candid humor is why the stresses of MBE don't often take a toll on us. I also want to thank John personally for giving me insight on so many questions I've asked him and very often providing me in response, a completely new perspective on the same. We drilled a hole in the back of an ion pump as that was an idea John suggested, to add a cryo pump. To our surprise, the chamber grew world record mobility quantum wells within a few months after coming back up, something we hadn't dreamt of.

I want to thank the administrative staff that made my life much easier as an international student. Trea DePrima, Amanda Girdler, Audra Pearce, Val De Veyra, Shannon Gann, Lynne Leininger and the staff at ECE and CNSI student offices and at the Office of International Students, that helped me on a daily basis, to navigate through the bureaucracy at UCSB. I want to thank the bravery of Gabrielle Hovendon for giving me valuable comments on this dissertation. I also want to thank the Physics and Chemistry machine shops for making everything we dreamt of or could poorly draw, on tight time scales, so that we could get the MBEs back on bake. Doug Rehn, Jeff Dutter, Andy Segale, Guy Patterson really were the people we could rely upon when we made modifications to our machines. I also want to thank the ECE shop crew Paul Gritt, Avery Juan, Bear Ramirez for helping us with day to day items like key access and shipping and receiving.

The work that I have done has only been made better by the many collaborations we've had. Prof. Paul Crowell and Prof. Vlad Pribiag's groups at Univ. of Minnesota and Prof. Sergey Frolov's group at Univ. of Pittsburgh, really made sure we got quick feedback on our samples and learnt how to make them better. Prof. Erik Bakkers's group at TU Eindhoven was also an excellent crew to work with and we really learnt a lot about III-V material systems, on our weekly Skype calls, with their expertise in MOVPE, nanowire growth and nano-scale wafer fabrication. I want to thank the measurement teams of Prof. Leo Kouwenhoven at TU Delft and Prof. Charlie Marcus at Niels Bohr Institute, Copenhagen, for providing us the data on various exciting and truly cutting-edge platforms for MZM devices. Microsoft Station Q at Santa Barbara has been the global epicenter of research in topological quantum computing. I want to thank Mike Freedman, Roman Lutchyn, Chetan Nayak and Mason Thomas at Station Q for the many insightful discussions and meetings where we could freely bounce ideas about

devices that some may have construed as too outlandish. Their feedback also made sure we remained focused in our efforts. Microsoft Station Q has been kind enough to invite the world's best researchers every six months to Santa Barbara, for the Q meeting, in-turn making sure that I didn't have to travel to remain in touch with the latest happenings around the world in the field of topological quantum computation.

I want to thank the various funding agencies that have supported my research in part at UCSB. I also want to thank the ECE department, Bob Hill and the students I had the privilege of being a TA for. Their support and feedback made me a better teacher and helped me learn more. The many outstanding TA awards and the excellent TA award I received were the most generous of their acknowledgements. I also want to thank the many students I've had the opportunity to mentor over the years.

As I neared the end of my PhD, it became clear to me (yes, it took me that long), that I only made it here because someone believed in me long before I thought I could do it. I want to thank my school teachers at Choithram School, Indore, St. George's School, Alaknanda and Birla Vidya Niketan, New Delhi, for always answering even the most silliest of questions I had (we didn't have Wikipedia back then). I also want to thank the excellent professors I had in my Bachelors that made sure that I was primed to attend a graduate school like UCSB. I want to especially thank Prof. Pawan Ajmera and Prof. Aniket Khandekar for their conviction in making sure we only left the classroom or the lab after having learnt something concrete. Most importantly, my scientific career wouldn't have started had it not been for Prof. Chandrashekhar Mahajan at VIT, Pune. He took me into his research group, my first task being cleaning up the workspace so that the experiments could begin. This was a great opportunity as I could then ask him questions as I came across new things and he gave me the most in-depth and thoughtful perspectives. He has remained a mentor to me over the last decade and I shall always be in his debt.

Life of a PhD student can sometimes be tough (pun intended). Friends within the lab and outside of lab really helped me through my years at UCSB. I want to thank Yuvraj Khadke, Mihir Chinchalkar and Harshwardhan Vaze for being my roommates and close friends. There was never a dull moment with this crowd. Talking about lack of dull moments, I want to thank Arturo Deza, Garo Sarajian, Christian Bueno and Massy Khoshbin for the new 1229 that provided me the peace of mind at home for years. Yes, it was epic. I want to thank Prasad Iyer, Paolo Pintus, Sarah Grunden and all my friends outside of lab who've kept me sane. I also want to give a shoutout again to the VG crew, most importantly Sean Harrington, Joon Sue Lee, Hadass Inbar and Connor Dempsey for being there when I needed their help to remain productive. Dismantling and rebuilding a III-V MBE sample manipulator or a full III-V MBE for a broken weld, simply cannot be done by one person (both physically and mentally) and they always had my back. Thank you!

At last, I feel bitter-sweet writing this. I have just landed at New Delhi airport, from Tokyo and am now waiting to board my flight to Indore, my hometown, having told my mom that I will be done writing by the time I arrive. Mom, Dad, sorry for the years of delay in writing, I should've listened to you! Mom, Dad, Swati, Aji, and all my family back home,

especially my aunts, uncles and cousins who made sure I had a good laugh every time I felt down; I wouldn't have been able to do this without your constant support. Words aren't enough to thank you all.

गुरुर्ब्रह्मा गुरुर्विष्णु गुरुर्देवो महेश्वरः ।
गुरु साक्षात् परब्रह्मा तस्मै श्रीगुरवे नमः ॥

Curriculum Vitae

Mihir Pendharkar

December 2019

EDUCATION:

Ph.D. in Electrical and Computer Engineering **2013-2019**
University of California, Santa Barbara, CA, USA

M.S. in Electrical & Computer Engineering **2011-2013**
University of California, Santa Barbara, CA, USA
Specialization in Electronics and Photonics

B.E. in Instrumentation & Control Engineering **2007-2011**
Vishwakarma Institute of Technology, University of Pune, Maharashtra, India
Specialization in Embedded Control Systems

Exchange Student **2010**
Ecole Nationale Supérieure des Techniques Industrielles et des Mines d'Albi-Carmaux, Albi,
France

AWARDS:

- University Award of Distinction, UCSB **2018**
- Ovshinsky Student Award,
American Physical Society's Division of Materials Physics **2018**
- Young Scientist Award,
Conference on Physics & Chemistry of Surfaces & Interfaces **2018**
- Graduate Student Travel Award,
American Physical Society's Division of Condensed Matter Physics **2017**
- Outstanding TA Award, Electrical & Computer Engineering, UCSB **2017**
- Outstanding TA Award, Electrical & Computer Engineering, UCSB **2016**
- Outstanding TA Award, Electrical & Computer Engineering, UCSB **2015**
- Best Presenter Award,
November Mini-Workshop, Center for Spintronics (CSPIN) **2014**
- Excellent TA Award, Electrical & Computer Engineering, UCSB **2013**

TEACHING EXPERIENCE:

Teaching Assistant, Semiconductor Device Processing, ECE & Materials, UCSB **2012-2017**

- Guided graduate students with processing Si NMOS transistors in the cleanroom
- Guided graduate students with processing GaAs High Electron Mobility Transistors
- **ECE Dept. Excellent TA Award (2013),**
- **ECE Dept. Outstanding TA Award (2015, 2016, 2017)**

SERVICE EXPERIENCE:

Referee , APS Physical Review journals	2019-Present
Volunteer , Community science education events organized by CNSI, UCSB	2013-Present
Board Member , Laboratory Safety Committee, UCSB	2012-2017
Instructor , School for Scientific Thought, CNSI, UCSB	2014-2015
Vice-President , Graduate Students Apartments Community Council, UCSB	2011-2012

MENTORING EXPERIENCE:

• Yuanning Chen, Undergraduate student, UCSB	09/2019 – Present
• Simona Pukiene, Visiting PhD student, FTMC, Vilnius, Lithuania	09/2019 – 10/2019
• Taozhi Guo, Undergraduate student, UCSB	06/2018 – 06/2019
• Michelle Labrecque, Masters student in ECE, UCSB	01/2016 – 04/2017
• Charlotte Franc, Undergraduate student, UCSB	04/2017 – 06/2017
• Chuyao Tong, Undergraduate student, Cambridge University, UK	07/2016 – 09/2016
• Veronika Werner, Undergraduate student, Purdue University, IN	06/2015 – 09/2015
• Chanud Yasanayake, Undergraduate student, Pomona College, CA	06/2014 – 09/2014
• John Hitchcock, High school teacher, Camarillo, CA	06/2013 – 09/2013

POPULAR MEDIA:

- [Product brochure](#), Quantum Design, USA (2019)
 - Helped design operational workflow and specifications for the van der Pauw – Hall Transport measurement option for Quantum Design’s Physical Property Measurement System (PPMS)
- Interview, “[The Hunt For the Elusive Majorana Qubit](#)” by Sophia Chen, *APS News*, Volume 27, Issue 4, April 2018
- Selected news articles on H. Zhang, *et. al*, *Nature* **556**, 74–79 (2018), DOI:[10.1038/nature26142](#)
 - *BBC News*, “[Microsoft gambles on a quantum leap in computing](#)” by Rory Cellan-Jones
 - *Gizmodo.com*, “[Microsoft Creates Wild Half-Electron Quasiparticle for Its Future Quantum Computer](#)” by Ryan F. Mandelbaum
 - *Science Daily*, “[Latest nanowire experiment boosts confidence in Majorana sighting: New test matches theory and offers the best evidence yet for the oddball particles](#)”
- Selected news articles on P.P. Iyer, *et al.*, *Nat. Comm.* **8**, 472 (2017), DOI:[10.1038/s41467-017-00615-3](#)
 - *UCSB Current* mention, “[Pointing Light](#)” by James Badham
- Selected news articles on S. Gazibegovic, *et al.*, *Nature* **548**, 434–438 (2017), DOI:[10.1038/nature23468](#)
 - *UCSB Current* interview, “[Finding Majoranas](#)” by Sonia Fernandez

Member of the American Physical Society and Materials Research Society.

PUBLICATIONS:

2019

- 1. Parity preserving and magnetic field resilient superconductivity in indium antimonide nanowires with tin shells**
M. Pendharkar, B. Zhang, H. Wu, A. Zarassi, P. Zhang, C.P. Dempsey, J.S. Lee, S.D. Harrington, G.H.A. Badawy, S. Gazibegovic, J. Jung, A.-H. Chen, M.A. Verheijen, M. Hocevar, E.P.A.M. Bakkers, C.J. Palmstrøm, S.M. Frolov
Preprint: [arXiv:1912.06071](https://arxiv.org/abs/1912.06071), *Under review*
- 2. In-plane Selective Area InSb-Al Nanowire Quantum Networks**
R.L.M. Op het Veld, D. Xu, M.A. Verheijen, S.M.E. Peters, C. Tong, V. Schaller, M.W.A. de Moor, Q. Wang, B. Hesselmann, K. Vermeulen, J. Bommer, J.S. Lee, A. Sarikov, M. Pendharkar, S. Koelling, L.P. Kouwenhoven, L. Miglio, C.J. Palmstrøm, H. Zhang, E.P.A.M. Bakkers
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- 3. Surface Reconstructions of Heusler Compounds in the Ni-Ti-Sn (001) System**
A.D. Rice, A. Sharan, N.S. Wilson, S.D. Harrington, M. Pendharkar, A. Janotti, C.J. Palmstrøm
Preprint: [arXiv:1909.12487](https://arxiv.org/abs/1909.12487), *under review*
- 4. Mechanism for In-plane Self Assembled Nanowire Formation**
N.S. Wilson, S. Kraemer, D.J. Pennachio, P.G. Callahan, M. Pendharkar, C.J. Palmstrøm
Preprint: [arXiv:1909.08690](https://arxiv.org/abs/1909.08690), *under review*
- 5. Transport Studies in a Gate-Tunable Three-Terminal Josephson Junction**
G.V. Graziano, J.S. Lee, M. Pendharkar, C.J. Palmstrøm, V.S. Pribiag
Preprint: [arXiv:1905.11730](https://arxiv.org/abs/1905.11730), *under review*
- 6. Conductance-matrix symmetries of a three-terminal hybrid device**
G. C. Ménard, G. L. R. Anselmetti, E. A. Martinez, D. Puglia, F. K. Malinowski, J. S. Lee, S. Choi, M. Pendharkar, C. J. Palmstrøm, K. Flensberg, C. M. Marcus, L. Casparis, A. P. Higginbotham
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J.S. Lee, B. Shojaei, **M. Pendharkar**, A.P. McFadden, Y. Kim, H.J. Suominen, M. Kjaergaard, F. Nichele, H. Zhang, C.M. Marcus, C.J. Palmstrøm
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13. Electric field tunable superconductor-semiconductor coupling in Majorana nanowires

M.W.A. de Moor, J.D.S. Bommer, D. Xu, G.W. Winkler, A.E. Antipov, A. Bargerbos, G. Wang, N. van Loo, R.L.M. Op het Veld, S. Gazibegovic, D. Car, J.A. Logan, **M. Pendharkar**, J.S. Lee, E.P.A.M. Bakkers, C.J. Palmstrøm, R.M. Lutchyn, L.P. Kouwenhoven, H. Zhang
New J. Phys. **20**, 103049 (2018), DOI: [10.1088/1367-2630/aae61d](https://doi.org/10.1088/1367-2630/aae61d)

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H. Zhang, C. X. Liu, S. Gazibegovic, D. Xu, J.A. Logan, G. Wang, N. van Loo, J.D.S. Bommer, M.W.A. de Moor, D. Car, R.L.M. Op het Veld, P.J. van Veldhoven, S. Koelling, M.A. Verheijen, **M. Pendharkar**, D.J. Pennachio, B. Shojaei, J.S. Lee, C. J. Palmstrøm, E.P.A.M. Bakkers, S. Das Sarma, L.P. Kouwenhoven
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16. Materials considerations for forming the topological insulator phase in InAs/GaSb heterostructures

B. Shojaei, A.P. McFadden, **M. Pendharkar**, J.S. Lee, M.E. Flatté, C.J. Palmstrøm
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17. Growth, electrical, structural, and magnetic properties of half-Heusler CoTi_{1-x}Fe_xSb

S.D. Harrington, A.D. Rice, T. Brown-Heft, B. Bonef, A. Sharan, A.P. McFadden, J.A. Logan, **M. Pendharkar**, M.M. Feldman, O. Mercan, A.G. Petukhov, A. Janotti, L. Çolakerol Arslan, C.J. Palmstrøm
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18. Ultrawide thermal free-carrier tuning of dielectric antennas coupled to epsilon-near-zero substrates

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19. Interface formation of epitaxial MgO/Co₂MnSi (001) structures: Elemental segregation and oxygen migration

A.P. McFadden, N.S. Wilson, T. Brown-Heft, D.J. Pennachio, M. Pendharkar, J.A. Logan, C.J. Palmstrøm
J. of Mag. & Mag. Mat. **444**, 383–389 (2017), DOI: [10.1016/j.jmmm.2017.08.027](https://doi.org/10.1016/j.jmmm.2017.08.027)

20. Valence-band offsets of CoTiSb/In_{0.53}Ga_{0.47}As and CoTiSb/In_{0.52}Al_{0.48}As heterojunctions

S.D. Harrington, A. Sharan, A.D. Rice, J.A. Logan, A.P. McFadden, M. Pendharkar, D.J. Pennachio, N.S. Wilson, Z. Gui, A. Janotti, C.J. Palmstrøm
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21. Growth, structural, and magnetic properties of single-crystal full-Heusler Co₂TiGe thin films

J.A. Logan, T. Brown-Heft, S.D. Harrington, N.S. Wilson, A.P. McFadden, A.D. Rice, M. Pendharkar, C.J. Palmstrøm
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B. Shojaei, A.C.C. Drachmann, M. Pendharkar, D.J. Pennachio, M.P. Echlin, P.G. Callahan, S. Kraemer, T.M. Pollock, C.M. Marcus, C.J. Palmstrøm
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23. Electrically reconfigurable metasurfaces using heterojunction resonators

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Adv. Opt. Mat. **4**, 1582–1588 (2016), DOI: [10.1002/adom.201600297](https://doi.org/10.1002/adom.201600297)

24. Spray Deposited Nanocrystalline ZnO Transparent Electrodes: Role of Precursor Solvent

C.M. Mahajan, M. Pendharkar, Y.A. Chaudhari, S.S. Sawant, B. Ankamwar, M.G. Takwale
J. Nano- Electron. Phys. **8**(2), 02026 (2016), DOI: [10.21272/jnep.8\(2\).02026](https://doi.org/10.21272/jnep.8(2).02026)

IN PREPARATION:

25. MBE growth of InAs_{0.5}Sb_{0.5} nanowires with epitaxial-Aluminum islands: Platform for topological superconductivity

M. Pendharkar, S. Gazibegovic, J.A. Logan, R.L.M. Op het Veld, H. Zhang, M. Verheijen, D. Car, E. Fadaly, D. Xu, M. de Moor, N. van Loo, D.J. Pennachio, J.S. Lee, B. Shojaei, L.P. Kouwenhoven, E.P.A.M. Bakkers, C.J. Palmstrøm

26. Observation of quantized conductance in quantum point contacts on near surface InAsSb quantum wells

M. Pendharkar, J.S. Lee, M.A. Seas, A.P. McFadden, T. Guo, C.P. Dempsey, S.D. Harrington, D.J. Pennachio, T.L. Brown-Heft, H. Inbar, C.J. Palmstrøm

27. InSb Quantum Wells on GaSb and InSb (001)

M. Pendharkar, J.S. Lee, B. Shojaei, A.P. McFadden, S.D. Harrington, D.J. Pennachio, C.J. Palmstrøm

28. High-Q Optical Antennas through Zero-Index Material Dispersion Engineering

P.P. Iyer, **M. Pendharkar**, A. Agrawal, M. Iza, S. Keller, U.K. Mishra, S. Nakamura, S. DenBaars, C.J. Palmstrøm, J.A. Schuller

29. In-situ Study of Magnetic Anisotropy in Fe/MgO (001) Ultra-Thin Films

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InAsSb quantum wells

Mihir Pendharkar, Joon Sue Lee, Michael A. Seas, Anthony P. McFadden, Taozhi Guo, Connor P. Dempsey, Sean D. Harrington, Daniel J. Pennachio, Tobias L. Brown-Heft, Hadass Inbar, Chris Palmstrøm

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2. InAsSb Quantum Wells for Topological Quantum Computation

Mihir Pendharkar, Joon Sue Lee, Chris Palmstrøm

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4. InAsSb Nanowires with Epitaxial Aluminum as a Platform for Topological Quantum Computation

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5. Near Surface In(As,Sb) 2DEGs for Topological Quantum Computation

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Electronic Properties of 2 Dimensional Systems (EP2DS), Penn State University, PA, USA, 31 July – 4 August 2017

6. A Materials Perspective on 1D and 2D Electron Systems for Topological Quantum Computation

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Capri Spring School on Transport in Nanostructures 2017, Anacapri, Italy, 23-29 April 2017

7. **Demonstration of InSb quantum wells on InSb substrates**
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American Physical Society March Meeting 2017 (APS), New Orleans, LA, USA, 13-17 March 2017
8. **Preparation of InSb Surfaces for Molecular Beam Epitaxy Growth and Re-growth**
Mihir Pendharkar, Joon Sue Lee, Prasad P. Iyer, Borzoyeh Shojaei, Anthony P. McFadden, Jon A. Schuller, Chris J. Palmstrøm
Physics and Chemistry of Surfaces and Interfaces 2017 (PCSI), Santa Fe, NM, USA, 15-19 January 2017
9. **Improvement in Quantum Mobility in InSb Quantum Well Structures by Reduction of Extended Defects**
Mihir Pendharkar, Borzoyeh Shojaei, Anthony P. McFadden, Joon Sue Lee, Chris J. Palmstrøm
North American Molecular Beam Epitaxy Conference (NAMBE) 2016, Saratoga Springs, NY, USA, 18-21 September 2016
10. **Gate Tunable InSb Quantum Well Structures grown on GaSb (001)**
Mihir Pendharkar, Anthony P. McFadden, Borzoyeh Shojaei, Joon Sue Lee, Chris Palmstrøm
American Physical Society March Meeting 2016 (APS), Baltimore, MD, USA, 14-18 March 2016
11. **Growth of Ultra High Mobility Inverted GaAs/AlGaAs Quantum Well Structures for Lateral Spin Transport**
Mihir Pendharkar, Timothy A. Peterson, Anthony P. McFadden, Sahil J. Patel, Paul A. Crowell, Chris J. Palmstrøm
North American Molecular Beam Epitaxy Conference (NAMBE) 2015, Riviera Maya, Cancun, Mexico, 4-7 October 2015
12. **Molecular Beam Epitaxy Growth of Ferromagnetic Heusler Alloy Co₂MnSi/GaAs Heterostructures**
Mihir Pendharkar, Sahil Patel, Anthony McFadden, Changjiang Liu, Timothy Peterson, Gordon Stecklein, Ashutosh Rath, Chockalingam Sivakumar, William Butler, Paul Voyles, Paul Crowell, Chris Palmstrøm
International Conference on Compound Semiconductors (ISCS) and Compound Semiconductor Week (CSW) 2015, Santa Barbara, CA, USA, 28 June – 2 July 2015
13. **Towards Spin Injection in GaAs Quantum Wells Using Ferromagnetic Contacts**
Mihir Pendharkar, Anthony P. McFadden, Sahil J. Patel, Timothy A. Peterson, Gordon Stecklein, Kevin Christie, Chad Geppert, Paul A. Crowell, Chris J. Palmstrøm
Center for Spintronics (CSPIN) November 2014 Mini-Workshop, 10-11 November 2014
14. **Magnetoresistance and k-Space Filtering: Engineering Materials to Devices, Invited Tutorial**
Mihir Pendharkar, Anthony P. McFadden, Sahil J. Patel, Chris J. Palmstrøm
Center for Spintronics (CSPIN) 2014 Annual Review, Minneapolis, MN, 25-26 September 2014

15. Study of growth of InSb on GaSb (001) with varying interlayers

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16. MBE Growth of Lateral Spin Transport Structures, Channel Materials and Ferromagnets

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Center for Spintronics (CSPIN) 2013 Annual Review, Minneapolis, MN, 26-27 September 2013

“The effort to understand the universe is one of the very few things that lifts human life a little above the level of farce and gives it some of the grace of tragedy.”

- *Steven Weinberg*

Abstract

Molecular Beam Epitaxy of Low Dimensional Electron Systems
for Topological Quantum Computation

by

Mihir Pendharkar

Theoretically proposed by Ettore Majorana in 1937, Majorana fermions are a unique class of particles which are their own anti-particles. This concept is realized in Majorana Zero Modes (MZMs), which are quasi-particles bound to zero energy, with no measurable charge and mass. Arising out of topological states of matter, signatures of MZMs were first experimentally observed in 2012.

These quasi-particles are predicted to exhibit non-abelian braiding statistics, allowing them to “remember” whether they were moved clockwise or counterclockwise around each other, forming a braid in time and position. Being their own anti-particles, fusion or annihilation of a pair of MZMs is expected to lead to a different outcome based on how they were braided, making a pair of MZMs the simplest quantum bit or ‘qubit’, forming the basis of Topological Quantum Computation.

As MZMs are indistinguishable from each other and quantum information is encoded in the exchange of MZMs, it is protected from environmental perturbations (noise), referred to as topological protection. Computation based on these qubits is predicted to be fault tolerant and scalable.

This work focusses on the device heterostructure design, Molecular Beam Epitaxy (MBE) growth and low temperature electrical characterization of superconductor-semiconductor hybrid systems hosting MZMs. Low dimensional electron systems (2D quantum wells, 1D nanowires) in semiconductors with strong spin-orbit interaction (e.g. InAs, $\text{InAs}_x\text{Sb}_{1-x}$ and InSb), transparently coupled to a superconductor (e.g. Aluminum), have been investigated.

With an emphasis on improving electron mobility, the first demonstration of an InSb quantum well on InSb substrate, as part of this work, showed a record quantum mobility of $50,000 \text{ cm}^2/\text{Vs}$. Top and bottom gate control of InSb quantum wells on GaSb substrates has also been demonstrated. MBE of InAs and InAsSb nanowires has also been studied, with demonstration of induced superconductivity in InAsSb nanowires. Recent work focused on MBE of near surface InAsSb quantum wells showing gate-controlled depletion and observation of quantized conductance through a Quantum Point Contact.

Lastly, *in-vacuo* growth of Aluminum partial shells on InSb nanowires, led to the first observation of quantized Majorana conductance, consistent with predictions. While further proof is necessary, these 1D and 2D hybrid systems, coupled with *in-situ* selective area evaporation of dielectrics, pave the way for realization of complex topological networks and subsequent demonstration of a fault tolerant topological qubit.

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1. Chapter 1 – Introduction

1.1. What is Quantum Computing?

Quantum computing promises a paradigm shift in the way information is processed, resulting in vast capabilities which can be harnessed to address outstanding challenges for mankind [1]–[4]. A “true” quantum computer, with about a thousand quantum bits, is expected to be helpful in simulating quantum mechanical properties of materials – for example in aiding the discovery of room temperature superconductors – and in simulating quantum chemistry, to name just a few [5]–[8].

Currently, ‘conventional’ or ‘traditional’ transistor-based computing is the mainstay of computing, and it is primarily dominated by Silicon CMOS (Complementary Metal Oxide Semiconductor) technology. Though this technology does not offer the same exciting possibilities of quantum computing, it is still expected to aid in the operation of a quantum computer [9].

A traditional computer, processes information sequentially. By increasing the number of processing units and memory assigned to a task, a simulated parallelism can be introduced to solve the problem at hand, faster. A solution to mathematical problems like factoring large numbers can hence be performed faster on a multi-processor supercomputer, as compared to a single processor personal computer. Even though supercomputers based on the Silicon CMOS transistor technology do have the power to simulate small-scale quantum computers, they are not a replacement for quantum computing.

The key difference between quantum and classical computing can best be distinguished by the inherent ability to parallel process or lack thereof. In both the single processor personal computer and a multi-processor supercomputer, each physical bit is deterministically assigned “0” or “1” [10]–[15]. A quantum computer is expected to approach such a problem very differently, as each quantum bit can correlate to an infinite number of possibilities between “0” and “1”, by the quantum superposition of 0 and 1. The possibilities can be represented on the surface of a sphere, as shown in Figure 1.1.

To solve 2^n possibilities, a traditional computer requires 2^n bits, while a quantum computer would theoretically only require n quantum bits (also known as *qubits*, pronounced “Q-bits”) to simulate the 2^n possibilities. The true potential of a quantum computer is hence in the linear scaling of these qubits with increasing complexity as opposed to the exponential scaling required for traditional bits to solve the same problem. It is believed that the fastest supercomputer of today, can only solve problems that a ~50-qubit quantum computer can handle [16]. So, while supercomputers will keep on improving, the speedup provided by true quantum hardware by scaling upwards of 50 qubits will remain exponential and will very

quickly outperform any traditional approach. This milestone is referred to as “quantum supremacy” [16], and the increased speed it offers has widespread ramifications.

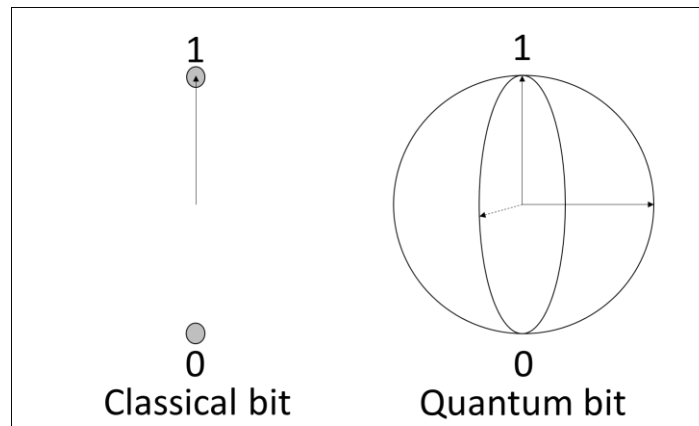


Figure 1.1 Representation of a classical and a quantum bit. A classical bit can only take two discrete values: 0 and 1, while a quantum bit can take a continuum of values between 0 and 1 as projected on the surface of a sphere.

There are a few different approaches to building a qubit. Each approach has its advantages and disadvantages, which can be broadly classified based on the fidelity of the qubits. A qubit’s fidelity broadly refers to the probability of error in the outcome. A higher fidelity would correspond to a lower error rate. This dissertation focuses on the materials aspects of realizing one such flavor of qubits, the *topological qubits*.

While many research groups and institutions around the world are experimenting with building qubits, industry funding has helped increase the speed of research of a few of these approaches. For example, superconducting qubits are being pursued by Google, IBM, and Rigetti [17]–[19]. Silicon impurity qubits are being pursued by Intel Corporation, ion-trap based qubits are being pursued by IonQ, and topological qubits are being pursued by Microsoft Corporation [20]–[22]. This is by no means an exhaustive list. To date, working qubits have been demonstrated by all except the topological approach [23]. Topological quantum computing based on topological qubits promises to reduce the error rate by orders of magnitude as compared to other quantum computing techniques, which makes building a topological qubit

the most viable approach for future scalable designs – contingent upon the demonstration of such a qubit, of course [24]–[27].

As of 2018-19, IBM has put up a small quantum computer, offering 20 qubits on-line for clients and a 14-qubit computer for free public use. Similarly, Intel has just launched a 49-qubit processor [28], [29]. Google has been testing a prototype 72-qubit processor since March 2018 [17]. Microsoft is offering a 30-qubit simulated quantum computer to developers via Visual Studio on any personal computer platform as well as a more powerful 40-qubit simulator via the Microsoft Azure cloud service [30]. These small quantum computers and quantum computer simulators are believed to be an enabling technology for further innovation, allowing scientists to experiment with potential applications that a “true” quantum computer may address. This first-generation quantum hardware is also the testbed for quantum software and software development environments, with various software development kits and languages already available [31]–[33]. In the future, the challenge will be to scale up these various rudimentary systems to a thousand *reliable* qubits, or technically a thousand *error-corrected* qubits.

To return to the issue of building a topological qubit, it is first necessary to give a brief overview of some fundamental physical principles of quantum mechanics. These fundamental principles underlie all quantum computing, regardless of the approach used.

Quantum superposition: This principle states that any two or more quantum states can be added together (“superimposed”) and the result will be another valid quantum state. Conversely, every quantum state can be represented as a sum of two or more other distinct

states [34]. This concept of superposition aligns with the wave nature of particles and the description of a physical system by its wavefunction in the Schrödinger's wave equation [35].

Quantum entanglement: It refers to a state when two or more particles are linked or correlated such that to give a true description of their state, a description of the system as a whole is necessary. Entangled entities can be separated by very large distances (in principle, a whole universe away), and yet remain quantum mechanically entangled. The first true demonstration of this entanglement was recently reported [36].

Wave-particle duality: This principle states that any fundamental particle can be described both as a particle and as a wave interchangeably and simultaneously [37]. The wavelength of any such particle-wave would then be described by the de Broglie equation where λ_B is the de Broglie wavelength, \hbar is Planck's constant, and ν is the frequency of the wave.

$$\lambda_B = \frac{\hbar}{\nu}$$

All of these concepts come together in quantum computing. In a quantum computer, the outcome or the result of the computer is probabilistic (e.g. 70% "0" and 30% "1") rather than deterministic (e.g. an unequivocal "0" or "1") and comes from the continuum of states any qubit can define [35]. The superposition principle is what leads to this multiplicity. The concept of entanglement allows for the interactions between the qubits and between the fundamental particles themselves (e.g. electrons) to be correlated, so that a change in the state of one has an immediate and simultaneous impact on the state of all, and that change is then reflected in the statistics of the entire system. Thus, the extremely fast information processing capability of a

quantum computer, or quantum supremacy, can be attributed to the combined concepts of superposition and entanglement.

The above concepts also introduce the major drawbacks of a quantum computer. While the future speedup because of a quantum computer will be exponential, the probability of an accurate or “correct” solution will eventually determine the usefulness of such a system [35]. Also, in most solid-state implementations of quantum computing, the energies between different quantum states is only a small fraction of thermal energy at room temperature. For this reason, the systems are prone to external environmental perturbations or “noise” and need to be operated at the lowest possible temperatures and shielded from unwanted electric and magnetic fields [38].

To reduce error due to various environmental perturbations, error correction in both hardware and algorithms is necessary [12], [39]. Error correction in hardware may involve multiple physical qubits operating in conjunction to execute an error-correcting algorithm [40], [41]. A combination of multiple such physical qubits could in principle represent an error-corrected logical qubit. The extent of error correction required, essentially depends on the specific approach used to build a qubit. Based on error rates reported as of this writing, superconducting qubit-based quantum computing is expected to require more than a thousand physical qubits to make a “reliable” logical qubit [42]. A thousand-qubit logical quantum computer based on this approach would hence require more than a million physical qubits entangled with each other. Luckily, with advancement in error correction algorithms and the all-round improvement of fundamental quantum hardware, error rates are decreasing rapidly [17].

However, there is also another option. To ease in the scaling up of the qubit technology to a thousand error-corrected logical qubits, qubits featuring intrinsic protection from external environmental perturbations are greatly desirable [25]–[27], [35]. Such “intrinsically protected” physical qubits would hence require much less error correction, which in turn reduces the number of physical qubits required to make a “reliable” logical qubit. Some estimates put this number between approximately ten and one hundred physical qubits for one logical qubit [43], [44]. This sharp reduction in the hardware required for reliable quantum computing is expected make such an approach a commercially viable alternative to building a “true” quantum computer. Topological quantum computation is one such approach and is described in the following section.

1.2. What is *Topological* Quantum Computing?

To understand topological quantum computation, some history is first necessary. The derivation of the wave equation by Erwin Schrödinger in 1926 and its expression in relativistic terms by Paul Dirac in 1928 opened new productive forms of atomic theory, for which they were jointly awarded the Nobel Prize in Physics in 1933 [45]–[50]. It was the Dirac equation that revealed particle spins, introduced the concept of anti-matter or anti-particles and predicted the presence of a positively charged electron [51]. The first confirmation of this concept of anti-particles was seen in experiments by Carl D. Anderson in 1932, demonstrating the existence of a “positive electron” – later referred to as a positron [52]. The positron had identical physical properties to an electron except for its charge which was opposite to that of an electron [52]. By Dirac’s theoretical prediction, combining the electron and positron (the

particle and the anti-particle) would annihilate them both and release a photon¹ with a known energy, which was also confirmed in the same work [52].

A solution of the Dirac equation by Ettore Majorana in 1937 predicted the existence of a special class of fermions that were their own anti-particles [53]. These were later referred to as Majorana fermions (as opposed to the Dirac fermions, which are not their own anti-particles).

Taking from the concept of Majorana fermions – Majorana Zero Modes (MZMs) – are quasi-particles which are their own anti-particles. MZMs are bound to zero energy² and are predicted to exist in condensed matter [54]. MZMs are expected to have zero charge, zero mass and zero energy! First observation of zero-bias peak, claimed to be signatures of MZMs was reported by V. Mourik, et al., in 2012 [55].

MZMs are not Majorana fermions but rather something called “Ising anyons”, a type of non-abelian anyons. Majorana fermions, as theorized, obey Fermi-Dirac statistics, and thus “Majorana fermion” is actually a misnomer for MZMs [54]. MZMs are named as such because they are the first particles (or quasi-particles) demonstrating the properties predicted by Ettore Majorana [56].

In principle, when a pair of MZMs is physically moved around each other clockwise, it is expected to give a different outcome of fusion as compared to the same pair being moved counterclockwise. This act of interaction or weaving of MZMs around each other in position

¹ A photon is a packet of energy with finite momentum but with no mass and is the wave-particle of light.

² The concept of “zero-energy” can be defined in superconductors where all states at energy different from the mid-gap are considered excited states [107], [108]. MZMs are energy states bound to the mid-gap of the superconductor’s density of states.

and time, is referred to as “braiding”. This “remembering”, or the property of the outcome being sensitive to the history of how the particle interacted is unique to a class of particles that follow non-abelian statistics. Experimental demonstration of braiding of MZMs remains elusive as of this writing. A schematic representation of braiding is shown in Figure 1.2. [27]

MZMs are indistinguishable quasi-particles. By braiding MZMs, information is stored in the exchange of MZMs and can only be accessed by fusing MZMs. This information is thus expected to be “hidden” or “protected” from the environment.

The outcome of a braiding operation is probabilistic: The outcome of fusion of a pair of MZMs from a clockwise rotation can be labelled as “0” or “low” while the outcome from a counterclockwise rotation can be labelled as “1” or “high”. In essence, a pair of MZMs forms the simplest qubit, and many pairs of MZMs lay the foundation for a quantum computer [57]. The idea for such a basis for quantum computing was first put forth by A.Y. Kitaev [24], [25]

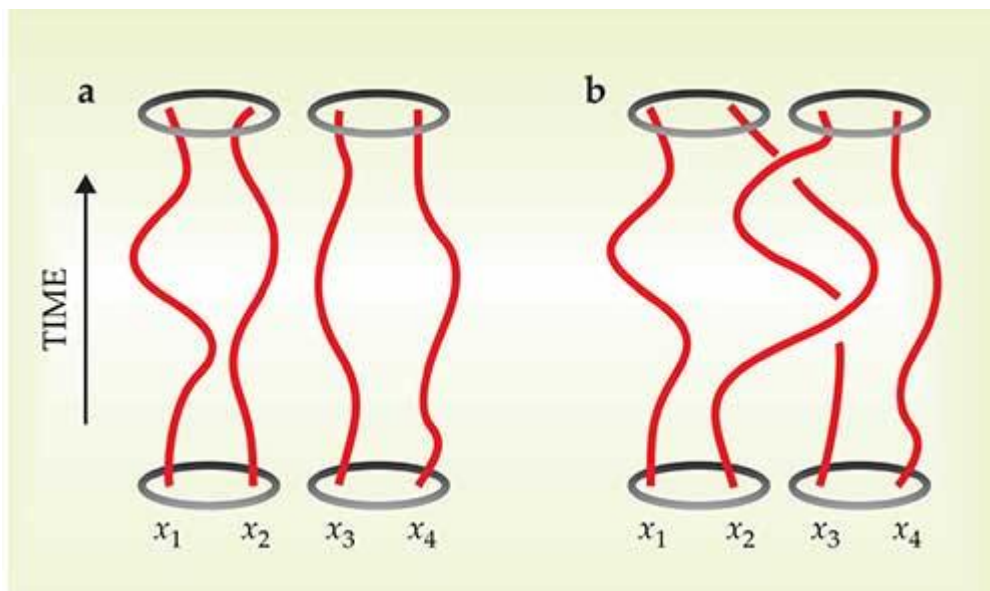


Figure 1.2 By imagining x_{1-4} as non-abelian anyons, a braid in time and position can be made by entangling x_2 and x_3 . Image Source – Ref. [27]. Reproduced from Physics Today **59**, 7, 32 (2006), with the permission of the American Institute of Physics.

and by M.H. Freedman [26]. Topologically protected qubits were theorized based on these fundamental ideas [27].

Thus, we arrive at MZM-based “topological” quantum computing. While it may seem unnecessarily complex at first, topological quantum computing offers great robustness or inherent protection from local or small-scale perturbations. This robustness in turn offers an innate ability for quantum error correction and makes topological quantum computing a viable candidate for commercial realization [26].

The robustness or the inherent protection from local or small-scale perturbations in the energy landscape, makes the MZMs a far more promising system, when the number of qubits is scaled up. While other approaches to quantum computing may require up to a million qubits to make only one “logical qubit” and up to a thousand such logical qubits to make a quantum computer, similar estimates for MZM-based quantum computing require only about one hundred physical qubits per logical qubit (though these numbers may vary by few orders of magnitude based on designs and confirmation of the same can only be obtained once an operational qubit has been demonstrated).

The reason that MZM-based quantum computing offers inherent protection from environmental perturbations lies in topology, the mathematical study of geometric properties and spatial relations unaffected by the continuous change of shape or size of figures [58]. The idea that a donut and a coffee mug are mathematically the same is a classic example of a topological classification of objects with one hole [59]. In general, the ability of a topological system to retain its classification comes from its disregard to local perturbations; in the donut model, for example, the donut remains an object with one hole even when a small bite is taken

out of the object. If a violent action like cutting the donut in half or breaking the handle off the coffee mug is taken, however, then the topological classification of the system would change. The ability of a system to still convey or hold the necessary distinguishing information (e.g. “object with one hole”) in spite of local perturbations is referred to as “topological protection”. An example of this property is shown in Figure 1.3 [60].

Similarly, if a pair of MZMs is to be exposed to local environmental noise, like impurities in the material hosting the MZMs, the MZMs are inherently protected by such perturbations until a certain extent, referred to as the topological energy gap³ (originating from the energy gap of the host superconductor) [61]. Generally speaking, the larger the topological gap, the larger the protection from environmental perturbations [61].

A topologically protected, fault tolerant quantum computer, starts with a topologically protected qubit. Such a computer can in principle be realized by braiding MZMs and other predicted non-abelian states [27]. One important attempt to build such a topological qubit was made in the 2000s based on the $5/2$ Fractional Quantum Hall State (FQHS). This enigmatic $5/2$ FQHS was originally observed in high mobility GaAs 2DEGs by R. Willet, et al., in 1987



Figure 1.3 A continuous deformation from the shape of a coffee mug to the shape of a donut leads still leaves the topological classification unchanged. Image Source – Ref. [60].

³ The theoretical discovery of topological phases of matter by D.J. Thouless, F.D.M. Haldane, and M.J. Kosterlitz was awarded the 2016 Nobel Prize in Physics [59].

[27], [62]. The challenges associated with making the $5/2$ FQHS interfere or braid with itself and the lack of conclusive results on the same, shifted the attention to MZM based topological quantum computation [56]. Apart from the MZM and the $5/2$ FQHS, predicted exotic non-abelian states also include parafermions and Fibonacci anyons, experimental demonstration of which remains a focus of future work [63]–[66].

Topological quantum computing is a very promising approach to quantum computing because of its intrinsic immunity to error. With the indications of possible successful realization of MZMs in condensed matter, the key challenge that still looms for research in topological quantum computing is how to achieve braiding of MZMs and consequently the demonstration of a topological qubit. This dissertation seeks to address the materials aspects of this challenge.

1.3. Majorana Zero Modes

1.3.1. Theoretical proposals for realization of MZMs

Since the prediction of Majorana fermions in 1937, there has been an extended hunt for Majoranas in high energy physics and neutrinos [67]. The specific theoretical framework required to guide the discovery of MZMs in condensed matter physics was put forth only in 2010 by J.D. Sau, et al., [68], R.M. Lutchyn, et al., [69] and Y. Oreg, et al., [70]. These researchers identified two key materials systems to host MZMs: firstly, a 1D chain of electrons, in a material with strong spin-orbit coupling, coupled to an s-wave superconductor, with a magnetic field applied along the length of the 1D chain of electrons; and secondly, the surface or edge of a topological insulator coupled to an s-wave superconductor. These proposals concluded that MZMs were a collective ground state of the system and not naturally occurring,

at least with reference to the proposed realizations. That research also put forward “recipes” to realize MZMs: analogous to how a fruit salad (the MZM) does not naturally occur in nature but can be synthesized by combining various fruits (the natural ingredients: semiconductors, superconductors, etc.).

One way to realize a material system that can host MZMs is by coupling a superconductor (like NbTiN or Al) with a semiconductor nanowire (like InAs or InSb), as shown in Figure 1.4. Once superconductivity from the superconductor can be induced in the semiconductor, or once the semiconductor is proximitized, the first key requirement for an MZM-hosting system is met. It must be noted that such a system, without an applied magnetic field (internal or external), is topologically trivial. A quantum phase transition is believed to occur on application of an in-plane magnetic field along the length of the nanowire (perpendicular to the direction of spin-orbit field) and the induced superconducting gap is expected to reduce. Beyond a certain critical field, the system is expected to undergo a quantum phase transition and become topologically non-trivial (see Figure 1.5). In this topologically non-trivial phase, a state at zero energy, i.e. in the middle of the superconducting gap, is expected to appear. This topologically non-trivial phase is predicted to be a p-wave topological superconductor [71]–[73] and the said zero bias peak in conductance spectroscopy is

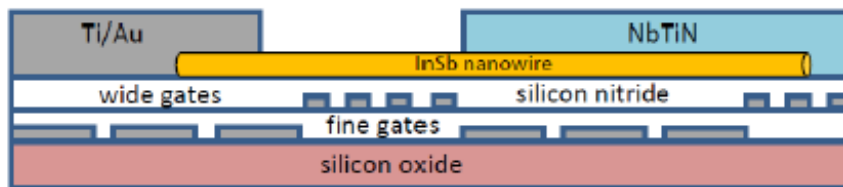


Figure 1.4 Schematic cross section of “Delft geometry” Majorana Zero Mode device showing an InSb nanowire covered with NbTiN for section, as the s-wave superconductor and Ti/Au contacts on the opposite end as the ohmic contacts. The silicon nitride dielectric layer under the nanowire, allows for bottom gating through gates embedded below the wire. These gates allow for tuning the chemical potential and controlling charge transport in and out of the wire. Image source – Ref. [55]. From V. Mourik, et al., Science 336, 6084 pp. 1003-1007(2012). Reprinted with permission from AAAS.

considered to be a signature of the MZM. Inferring Majorana’s prediction, such a zero bias peak should signify the presence of MZMs on the ends of the 1D chain of electrons.

Theoretical work proposing the use of high spin-orbit coupling semiconductors with transparent coupling to an s-wave superconductor also laid the guidelines for how the induced topological gap in the superconductor semiconductor hybrid system would scale. Increase in spin-orbit coupling strength is expected to aid in increasing topological gap, leading to enhanced topological protection [61].

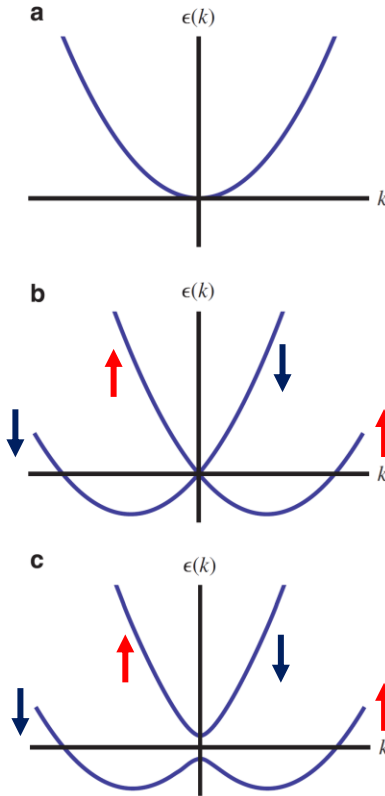


Figure 1.5 shows the evolution of the conduction band in energy-momentum space, starting with (a) absence of spin-orbit coupling or Zeeman splitting induced effects (b) presence of spin-orbit coupling but absence of Zeeman splitting (c) presence of both spin-orbit coupling and Zeeman splitting, leading to opening up of a gap. When the Fermi-level (chemical potential) is moved into the gap, the conduction is spin-momentum locked, leading to helical edge transport. This gap is referred to as the helical gap. Adapted from – Ref. [54].

With MZMs being insensitive to external electric or magnetic fields, small variations in electric field along the wire, as well as a further increase in the magnetic field applied along the length of the nanowire, is expected to not perturb the MZM and the MZM is expected to

remain bound to zero energy (this does not hold true when the necessary conditions are deviated from, though).

As the band structure of the system evolves and signatures of MZMs emerge, the conductance of the zero bias peak is predicted to be quantized to $2e^2/h$, as shown Figure 1.6. This conductance quantization is a result of the specific band structure of the system, with only one conduction path for each spin of electrons at the Fermi level leading to the prefix “2”. It must be noted that the fundamental quantum of conductance is e^2/h . With the system tuned to observe the zero-bias peak and the Fermi level tuned to $2e^2/h$ quantization, the Fermi level is considered to be in a “helical gap”. This helical gap persists while the conductance remains $2e^2/h$ and is called thus, due to the physical realization of such an energy system where the opposite spins form a parallel non-intersecting helix, in momentum and time.

Alternatively, in the approach proposed to realize MZMs, where s-wave superconductivity is induced in a topological insulator, or where an s-wave superconductor is placed on the surface of a 3D topological insulator – the precondition to enter a topological phase is already satisfied (with the host being a topological insulator). This alternative approach can hence in principle host MZMs with no externally applied magnetic fields [75].

To better understand how MZMs are realized, in this alternative approach, some clarification of the properties of topological insulators or “TIs” is necessary. Moreover, this understanding may help explain how the two seemingly independent approaches, first based on semiconductor-superconductors, and second based on topological insulator-superconductors, are inherently linked.

A TI here refers to a material system with trivial energy gap in the bulk and conducting surface states [76]. The surface conduction electrons of a TI also show spin dependent momentum locked transport and are in principle protected from backscattering without a spin flip, due to a lack of states with the same spin but opposing momentum [76]. Moreover, the properties of TIs are dependent inherently on their dimensionality, i.e. an n -dimension TI is expected to have an $n-1$ dimensional topologically non-trivial surface. In other words, a 3D TI has 2D conducting surfaces (e.g. surface of Bi_2Se_3 or PtLuSb), a 2D TI has 1D conducting edges (e.g. interface of an InAs/GaSb bi-layer or a strained HgTe/CdTe quantum well), and a 1D TI has 0D conducting points or ends (e.g. extremities of a 1D nanowire hosting MZMs). Thus, to summarize, a 1D semiconductor nanowire coupled to a superconductor, when tuned to host MZMs, represents a 1D topological insulator with two allowed “point-like” conducting energy states (in an otherwise forbidden gap) at the two opposite ends of the nanowire [77].

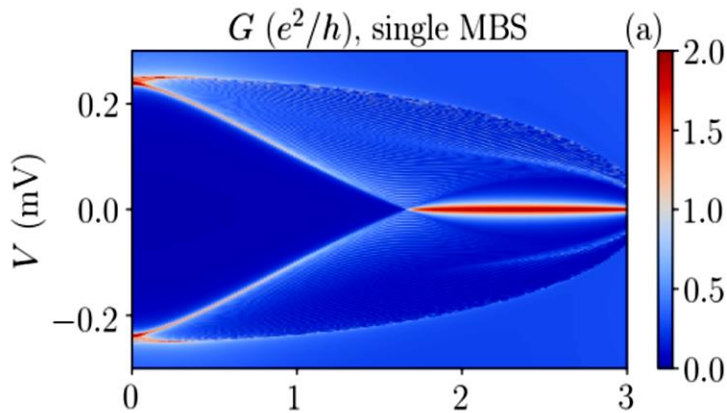


Figure 1.6 Shows a simulated image of a quantized Majorana Zero Mode (red line at 0 mV), where x-axis is the Zeeman energy splitting (in meV) induced by application of an external in-plane magnetic field and in experimental results is replaced by the magnetic field. y-axis shows the deviation from zero-energy of the center of the superconducting gap. As the Zeeman energy is increased, trivial superconducting gap closes and a zero-bias peak which quickly rises to the quantized value of $2e^2/h$, stays. At very high Zeeman energies, the superconductivity in the host s-wave superconductor vanishes, denoted by the outer quadratic response, and so does the zero-bias peak (not shown). Image source – Ref. [74]. Reprinted figure with permission from C-X. Liu, et al., Phys. Rev. B, 97, 21 p.214502 (2018). Copyright (2018) by the American Physical Society.

In the absence of experimental results to prove the non-abelian statistics of the MZMs with braiding, alternative explanations for the presence of zero bias peaks with non-Majorana origins have been proposed. Such explanations attribute the origin of a zero bias peak or zero bias anomaly to other phenomenon such as the Kondo effect, Andreev bound state or an anomaly in the density of states at the Fermi-level [74].

The original theoretical proposals predicting the presence of MZMs in condensed matter systems were a thrust to further our understanding of topological states of matter, exotic forms of superconductivity and implications of quantum mechanics in general. Most recently, this theoretical work has opened the possibility of linking interacting Majorana fermions to emergent quantum gravity [78]. This idea, however, remains beyond the scope of this work.

1.3.2. Experimental realization of MZMs

As mentioned above, topological quantum computing depends on the physical realization of MZMs. However, demonstration of MZMs is by no means easy; its eluded experimentalists for about 75 years. To finally achieve an experimental demonstration of MZMs required a fine control over all aspects of the physical system. Towards the same, the work of V. Mourik, et al., [55] was a groundbreaking feat that 1) demonstrated the ability to tune the chemical potential into the helical gap, 2) coupled superconductivity to a semiconductor, and 3) created a tunnel junction for bias dependent conductance spectroscopy at the edge of the superconductor (see Figure 1.7). In order to demonstrate MZMs in future, it is extremely important to address each of these steps with a materials perspective. While the following steps are necessary, the indications observed may not be conclusive and may require further theoretical and experimental exploration.

1) *Tuning of the chemical potential into the helical gap*: First, to realize the required 1D chain of electrons in a material with strong spin-orbit coupling, quantum wires or nanowires of semiconductor materials InAs and InSb, were chosen. Another advantage of working with semiconductor systems was the ability to tune the Fermi-level (or chemical potential) by applying external electric fields (i.e. gate voltages). Using such a “control knob” is essential in engineering the required 1D chain of electrons regardless of nanowire to nanowire differences in diameter and electron population. This control knob is not readily available in chains of metallic 1D atoms, even though those metallic chains (and the ensemble thereof) may satisfy all the other required criteria.

2) *Coupling superconductivity to a semiconductor*: Next, to meet the requirement of a large in-plane critical field of the superconductor, V. Mourik, et al., chose NbTiN. NbTiN is known to have critical field in excess of 10 Tesla and coupled to an InSb nanowire, was used to observe the first signatures of Majorana Zero Modes [55]. Later demonstrations incorporated thin films of aluminum on InAs [79], [80]. Coupling superconductivity with Al-InAs and Al-InSb systems with improved control over the interface is a prime focus of this dissertation. Improving the of experimental apparatus required for the same is described in Appendix B. . A partial coverage of the nanowire with a superconductor, rather than a full shell of a superconductor, is also essential so as not to screen the externally applied electric fields.

Aided by the work mentioned as part of this dissertation, the first demonstration of induced superconductivity in an Al-InSb nanowire system was performed by S. Gazibegovic, et al., [81]. The system showed an induced “hard gap”, which refers to a superconducting gap devoid of discrete sub-gap states. This hard-gap alleviated a common problem of a “soft-gap” from previous experiments on the InSb material system when working with NbTiN

superconductor [55], [82]. Similar work on the Al-InAs system by P. Krogstrup, et al., also showed an atomically sharp superconductor-semiconductor interface and induced hard gap [83], [84]. Recently, induced hard-gap was also eventually observed in InSb-NbTiN [85] which led to the observation of ballistic Majorana devices [86].

The first experimental demonstration of induced superconductivity in the Al-InAs 2D electron system by J. Shabani, et al. in 2015 was another necessary milestone for realization of wafer-scale Majorana device platforms [87]. See Figure 1.8.

3) *Tunnel junction for bias dependent conductance spectroscopy*: Lastly, tunnel junctions to probe the edge states in the nanowire system were constructed. While initial experiments used lithographically defined (etched) regions devoid of superconducting shell, the etched tunnel junctions damaged the exposed semiconductor.

After V. Mourik, et al., there have been numerous reports of observation of zero-bias peaks reminiscent of Majoranas [79], [80], [88], [89]. However, alternative explanations for the observation of such states have also been put forth, as were alluded to previously. To lay

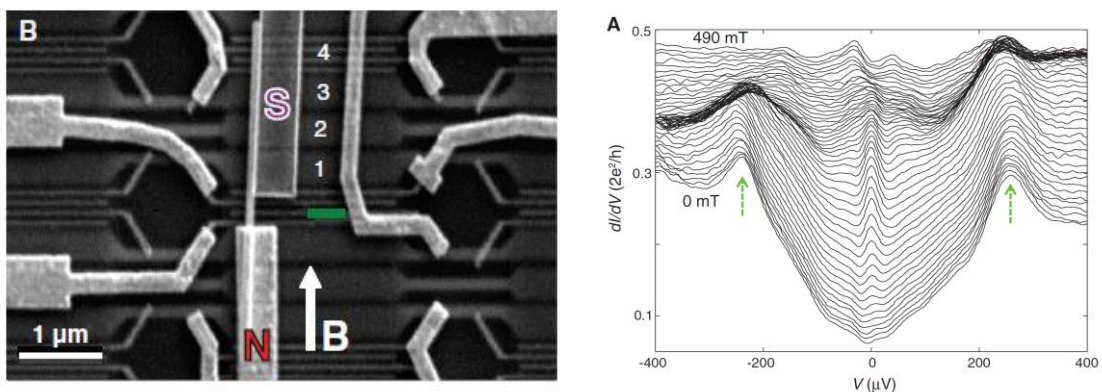


Figure 1.7 The left panel shows an SEM image of the device that lead to the first observation of signatures of MZMs in InSb/NbTiN. N is the normal Ti/Au metal conductor while S is the superconductor and B represents the direction of applied magnetic field along the length of the nanowire. The right panel shows the conductance spectroscopy data showing a zero-bias peak in units of quantized conductance. Note the zero-bias peak stays at zero-bias with varying magnetic field but its value is not quantized. Image source – Ref. [55]. From V. Mourik, et al., Science 336, 6084 pp. 1003-1007(2012). Reprinted with permission from AAAS.

to rest all speculation and for confirmation of these zero-bias peaks being the MZM requires observation of the predicted non-abelian statistics. As braiding remains an outstanding challenge, as of this writing, any argument in favor of observation of MZMs remains unverified.

All in all, these findings open the door to search for MZMs in many more superconductor-semiconductor hybrid systems. For example, a group of researchers led by H. Souminen, et al., expanded upon the work of Shabani, et al., and demonstrated scalable designs for observation of MZMs in 2D electron systems in the Al-InAs material system [87], [90]. And the possibilities hardly stop there. Preparation of materials ingredients for experimental realization of MZMs in a broad variety of superconductor-semiconductor hybrid systems is the primary focus of this dissertation.

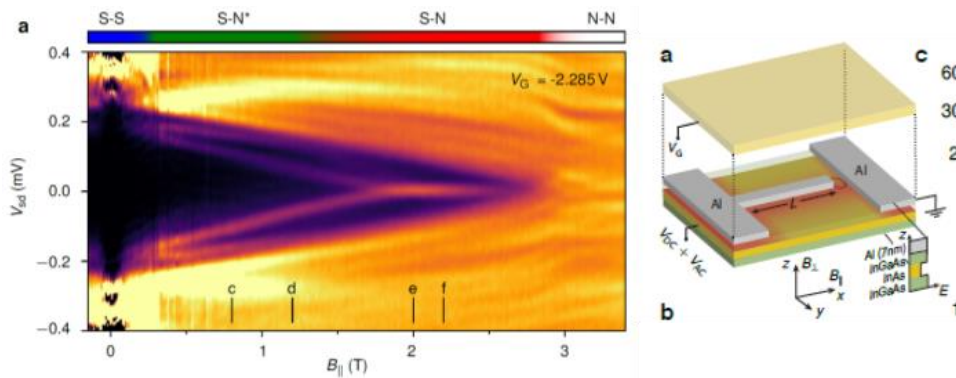


Figure 1.8 The left panel shows the first observation of a zero-bias peak, in an InAs quantum well on application of an in-plane magnetic field, in a near surface InAs quantum well coupled to a layer of superconducting Aluminum, from the surface. The device geometry is shown on the right and involves using the aluminum not only for proximitize the InAs quantum well underneath but also for use as the source drain ohmic contact. A top gate is placed globally on the device to deplete the exposed InAs (yellow) leaving a nanowire like region underneath the thin long strip of Aluminum. This top gate also allows for tuning the tunnel coupling between source and drain to perform conductance spectroscopy of the nanowire. Image source – Ref. [90]. Reprinted with permission from H.J. Souminen, et al., Phys. Rev. Lett., 119, 17 p.176805 (2017). Copyright 2017 by the American Physical Society.

1.3.3. Towards Majorana qubits⁴

MZM-based qubits will form the fundamental building blocks of any MZM-based topological quantum computer. To recap, a pair of MZMs can form a simple qubit. The theoretical framework for potential braiding schemes for non-abelian states, and more specifically for MZMs, preceded experimental realization of MZMs. Experimental demonstration of Majorana braiding and fusion are still elusive, as of this writing. The theoretical proposals, relevant to this dissertation, would be elaborated below. Some experimental advances towards demonstrating MZM qubits will also be discussed.

Various potential schemes have been proposed to facilitate demonstration of an MZM-based qubit. Based on the concept of a “knot” or a braid, where a pair of MZMs is moved around each other clockwise or counterclockwise, J. Alicea, et al., proposed a physical nanowire realization with a “T” shaped nanowire network. This T-shaped network is the simplest device to physically braid MZMs. From a materials perspective, demonstration of complex nanowire junctions like “T” or nanowire cross and “#” shaped devices followed [91], [92]. The prime requirement for any such nanowire network being the ballistic or scattering-free transport of electrons along the length of the nanowire and any nanowire junctions.

P. Bonderson, et al., proposed a “measurement-only” scheme [93], [94], while S. Plugge, K. Flensberg, et al., proposed a parallel nanowire device geometry [95] with a superconducting island linking the two nanowires. These designs alleviate the need to physically “move” the MZMs. The theoretical proposal of parallel nanowires also satisfied the condition of having an

⁴ See also: “[The Hunt for the Elusive Majorana Qubit](#)” by Sophia Chen, APS News, Volume 27, Issue 4, April 2018.

in-plane magnetic field along the length of the two nanowires, as now the same magnetic field could be used to tune the nanowires into the helical gap.

By monitoring the parity of electrons (odd or even) on the superconducting island, a change in parity could be measured once an electron was added or subtracted. This is significant because the addition or subtraction of an electron, is expected as an outcome of the fusion of MZMs (if such an operation were to be performed in the system). Such an observation would be definite proof of non-abelian statistics.

Previous work by S. Albrecht, et al., on the Al-InAs system [96] and recent work by J. Shen, et al., on the Al-InSb as a part of this dissertation [97], has successfully demonstrated the ability to determine electron parity on a superconducting Aluminum island.

By alleviating the need to move MZMs, the measurement operation is also expected to be faster [93]. T. Karzig, et al., (in collaboration with S. Plugge, et al.) proposed a comprehensive and robust nanowire network architecture based on the concepts put forth originally by S. Plugge, et al., defining in detail the exact physical realization of a topological qubit [44]. This dissertation seeks to realize nanowire architectures proposed in that work. Theoretical proposals for the realization of MZM-based qubits and the experimental construction of qubits are discussed in greater detail later.

1.4. Challenges for MZM devices and overview

The primary challenge for MZM based devices, when work commenced on this dissertation, was the absence of a quantized Majorana conductance peak. Superconductor-semiconductor interface was suspected to be one of the causes for this absence and steps to

improve this interface have been addressed in the Chapters 4 and 5. Technical aspects of the same have been elucidated in Chapter 3 and Appendix B.

A secondary challenge for MZM devices is the relatively high magnetic field required for observation of a zero-bias peak. Increasing the g-factor of the host semiconductor material, as well as control over the superconductor-semiconductor coupling was predicted to be the key to reducing the required field. A new material system for MZM devices has been explored and initial results have been presented in Chapter 6.

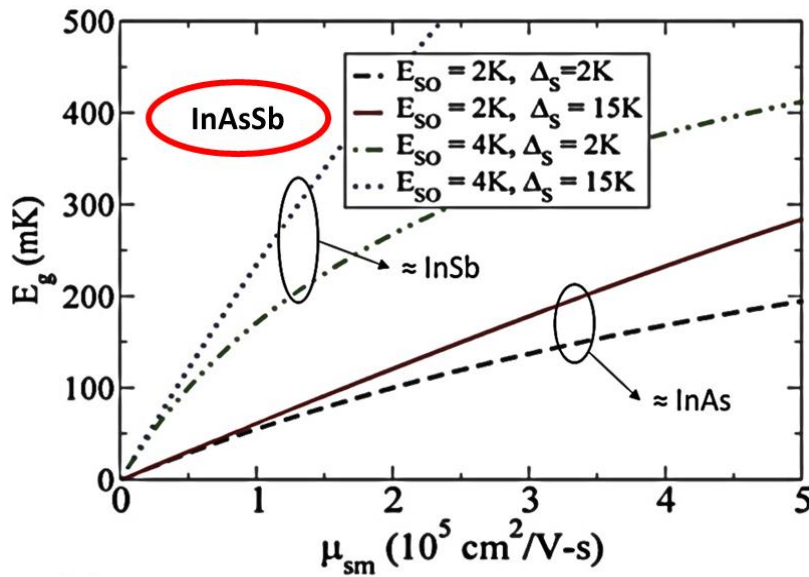


Figure 1.9 shows the theoretically calculated topological induced gap for InAs and InSb in contact with superconductors of gap 2K (e.g. Aluminum) and 15K (e.g. NbTiN), as the 2D electron mobility in the semiconductor is increased. An increase in spin-orbit coupling leads to an increase in the induced topological gap, for the same electron mobility. Similarly, an s-wave superconductor with larger superconducting gap, leads to a larger induced topological gap. Adapted from Ref. [61]. Reprinted figure with permission from J.D. Sau, et al., Phys. Rev. B, 85, 6 p.064512 (2012). Copyright 2012 by the American Physical Society.

Increasing the g-factor of the host semiconductor, along with improving material quality, has been predicted to increase the induced topological gap in the system. This increase in topological gap is expected to increase the robustness of the MZM from external environmental perturbations. A comparison increasing topological gap and material quality (represented by carrier mobility) for InSb, InAs, and InAsSb has been shown in Figure 1.9.

Lastly, fabrication of next generation superconductor-semiconductor heterostructures for realization of topological qubits, remains an outstanding challenge. Efforts to make MZM based topological qubits have been described in Chapter 7.

To summarize, this work provides a materials perspective on topological quantum computation and details the state-of-the-art in the realization of Majorana Zero Modes (see Table 1.1).

Table 1.1 Overview of materials platforms studied

	2D (quantum wells)	1D (VLS nanowires)	1D (SAG nanowires)	Induced superconductivity
InAs	Section 4.2	Section 4.3	Section 4.4	Section 4.4
InSb	Section 5.4	Section 5.5	Section 5.6	Section 5.5, 5.6
InAs _{0.2} Sb _{0.8}	Section 6.2	-	-	-
InAs _{0.5} Sb _{0.5}	-	Section 6.3	-	Section 6.3

2. Chapter 2 – Components of MZM Systems

2.1. Low Dimensional Electron Systems

To realize the required 1D chain of electrons in a physical system, semiconductors are the material of choice. Semiconductors like InAs and InSb have a strong spin orbit coupling (stronger than GaAs) and were proposed to be suitable candidates for such a realization. Undoped semiconductors, disregarding any surface effects, are by definition, insulators at 0 Kelvin.

Semiconductors with a very small band gap (like InSb and InAsSb) are electrically conducting at room temperature, primarily due to thermal excitation of carriers from valence band to conduction band. Control over the doping, during crystal growth, allows for fine tuning the free carrier density in the material system. Also, extrinsic control knobs like gate voltages can be utilized to further fine tune the electron density actively during operation. These attributes, combined with the pre-existing knowledge of the growth of nanowires (or quantum

wires) in the InAs and InSb material system, makes these semiconductors the materials of choice for exploring MZMs. The observation of MZMs in atomic chains of ferromagnetic materials has also been claimed but will remain beyond the focus of this work [98], [99].

While all physical objects are inherently three dimensional, there are various ways to quantum mechanically create low-dimensional electron systems. The systems can be created with physical constraints (e.g. using sheets of a material for a 2D system or nanowires for a 1D system) or with extrinsic electric fields (gate voltage). In 3D host semiconductor systems, 1D and 2D electron systems can form due to quantum confinement which leads to anisotropic energy level separation between allowed states. At low temperatures, with low electron carrier density, only the lowest energy level is occupied, leading to an effective reduction in dimensionality. Quantum confinement also leads to a quantization in the density of states as shown in Figure 2.1.

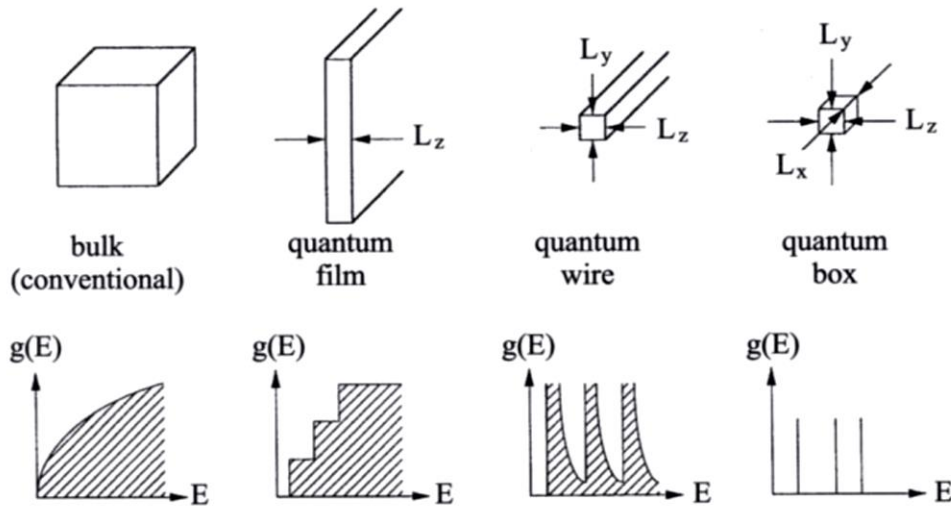


Figure 2.1 The upper half shows a 3D schematic representation of low-dimensional electron systems and the lower half shows their corresponding density of states with respect to energy. On shrinking dimensions from 3D (bulk), showing a continuous rise in the density of states, a 2D systems shows a quantization in the density of states, in one dimension. A nanowire further quantizes the density of states while a quantum dot has discrete energy levels only, regardless of dimension. Image source – Ref. [100]. Reprinted by permission from Springer, Epitaxy by M.A. Herman, W. Richter, H. Sitter (2004).

While the use of GaAs is not directly relevant, as of now, to experiments in the realization of MZMs, it has had a profound impact on developing the understanding of low dimensional semiconductors⁵. A typical technique used to grow heterostructures (different materials layered on top of each other) of GaAs (and Al,Ga,In-As,Sb), is called Molecular Beam Epitaxy, and is discussed in detail below.

An important concept in understanding the properties of semiconductors and their interaction with other materials is the chemical potential or Fermi level. It is defined as the highest occupied energy level in the material, at zero kelvin. For undoped semiconductors and insulators with an equal number of electron and hole populations, the Fermi level is expected to be in the middle of the band gap, in the bulk of the material.

Regardless of doping, in most III-V semiconductors, the Fermi-level at the surface has been observed to be ‘pinned’ or fixed to a certain energy, especially when put in contact with a metal (e.g. Au) [101], [102]. The metal-semiconductor interface forms a Schottky barrier

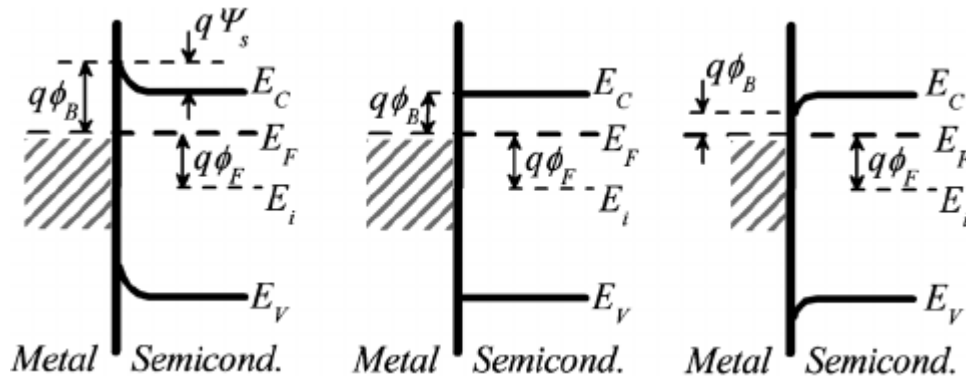


Figure 2.2 Bands in the semiconductor can bend at the metal semiconductor interface forming a depletion region (left panel), a flat band condition (center panel) or an electron accumulation region (right panel). The Schottky barrier height is denoted by $q\phi_B$. InSb and GaAs forms a depletion region at the surface, similar to the left panel while InAs forms an accumulation layer at the surface. Image Source – Ref. [103]. Reprinted from A. Ruzin, J. Appl. Phys. 109, 1 (2011), with permission of AIP Publishing.

⁵ Theoretical proposals for creation of heterostructures, leading to low-dimensional electron systems, were first put forth by Z. Alferov and H. Kroemer, for which they were awarded the Nobel Prize in Physics in 2000 [213].

(leading to electron depletion in the semiconductor) or an electron accumulation layer. The doping in the semiconductor can change the depletion region width, but not the height of the barrier and it is considered to be “pinned”. Figure 2.2 shows potential band alignments at a metal semiconductor interface.

InAs is known to have an electron accumulation layer at the interface, making ohmic metal contacts easier, while the Fermi-level of GaAs is known to be pinned mid-gap, resulting in rectifying contacts. Making low resistance ohmic contacts to GaAs has hence been a topic of interest for researchers. InSb also forms a Schottky barrier for metal contacts, but the barrier height is small enough for Thermionic-Field Emission at room temperature⁶.

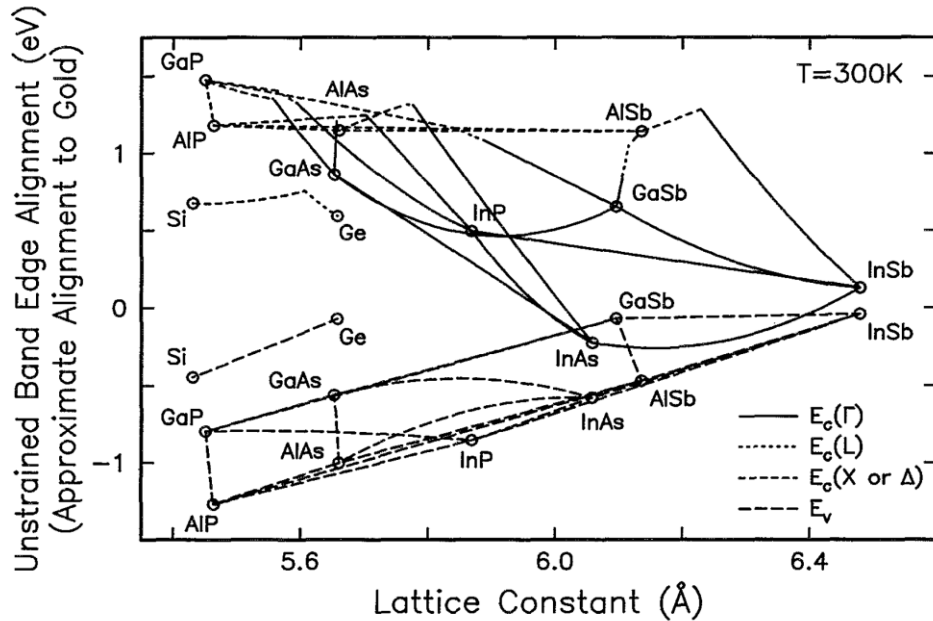


Figure 2.3 Semiconductor Band Alignment – The band alignment of typical III-V and IV semiconductors with respect to gold has been plotted against their lattice constant. Continuous lines indicate direct band gap. Image source – Ref. [101]. Reprinted from S. Tiwari and D.J. Frank, *Apply. Phys. Lett.*, 60, 5, pp.630-632 (1992), with the permission of AIP Publishing.

⁶ As part of this work, it was observed that ohmic contacts formed to InSb at 300K and operational at 2K, often formed Schottky diodes at 20mK. Due to the challenges involved in device fabrication (with antimonide semiconductors in general) and the lack of facilities to characterize samples at 20 mK, to get feedback on ohmic contact formation, a comprehensive study of the same remains a focus of future work.

As materials with different band gaps are layered on top of each other, sharp discontinuities between their conduction band and valence band may arise to maintain a continuous vacuum level. Figure 2.3 shows the band alignment with respect to gold for some common III-V semiconductors [101]. This plot is expected to change with varying temperatures, varying crystal orientations and the introduction of strain.

The band discontinuities could be used to engineer device heterostructures for specific applications, like hetero-junction bipolar transistors (HBTs), high electron mobility transistors (HEMTs) and lasers. Modulation doping originally proposed by H. Störmer and demonstrated by R. Dingle, H. Störmer, A.C. Gossard and W. Wiegmann at Bell Labs uses conduction band discontinuity to separate dopants from charge carriers to significantly enhance carrier mobility [104]. This concept is central to the realization of a high mobility 2D electron gas (2DEG) in

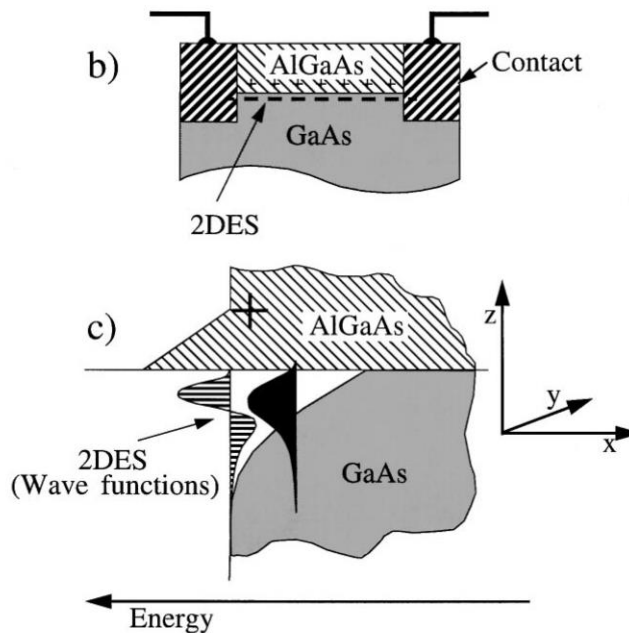


Figure 2.4 Modulation doping in GaAs//AlGaAs – The upper half of the figure shows a schematic diagram for modulation doping. The dopants (Si atoms) are inserted in the AlGaAs layer cladding the quantum well, such that the 2DEG formed in GaAs is not immediately impacted by scattering from dopants. The lower half shows the energy vs depth diagram, where the bands in GaAs bend, forming the 2DEG and its quantized energy levels, away from the dopants in AlGaAs. Image source – Ref. [105]. Reprinted figure with permission from H.L. Stormer, Rev. Mod. Phys., 71, 4, pp.875-889 (1999). Copyright (1999) by the American Physical Society.

any semiconductor material system as dopants lead to ionized impurity scattering reducing the peak mobility of carriers. By separating the scattering centers from the “active channel” of a narrower band gap material, and by using a band discontinuity, semiconductors can be “remotely” doped for low temperature operation. Furthermore, by controlling the doping, electron density in the 2DEG channel could be very precisely controlled. This concept is best observed in GaAs/AlGaAs material system, as shown in Figure 2.4 [105].

While there are techniques to grow small droplets of semiconductors, leading to a physical 3D confinement creating a quantum dot (0D electron system), some quantum dots need to be created artificially in other low dimensional electron systems like quantum wells or nanowires so that they can be incorporated into an active device. One proposed approach to braid MZMs by measurement, involves, linking two MZM states originating from separate nanowires, to a shared quantum dot [44], [95]. Such a structure can be created in a nanowire by applying gate voltages in a small region of the nanowire, not covered by a superconductor and has been discussed later. A schematic of one such potential qubit structure is shown in Figure 2.5.

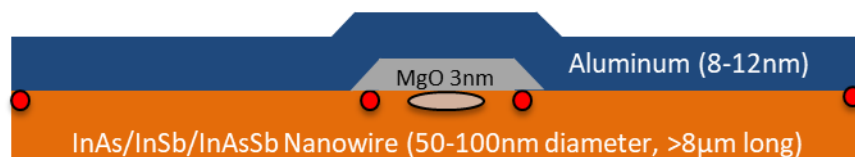


Figure 2.5 Qubit cross section – A VLS nanowire-based qubit, with red circles showing the presumed localized MZMs. A section of the wire is coated with MgO, such that it is not proximitized by the Aluminum. This break in Aluminum creates two sections of topological superconductors in nanowire. The superconducting Aluminum forms a link between these two otherwise independent topological sections. The trivial semiconductor under the MgO layer, now confined on all three dimensions is to be used to form a quantum dot, with gates lithographically defined, externally. This quantum dot and the superconducting link combined are necessary for readout of the MZM braiding operation.

2.2. Superconductivity

As realization of MZMs requires coupling superconductivity to a semiconductor or topological insulator, an introduction to superconductivity is necessary.

Trivial superconductors (otherwise simply referred to as superconductors) are broadly classified as Type I and Type II superconductors, while more complex states, referred to as multicomponent superconductors require more thorough classification [106].

In Type I superconductors, a sharp transition exists between the superconducting state (with electrons in cooper pairs) and the normal state (with unpaired electrons), as magnetic field strength is increased. In the superconducting state, magnetic flux quanta are all repelled due to the Meissner effect; in the normal state, magnetic flux can permeate through [107], [108] (see Figure 2.6). The transition from a Meissner superconducting state to normal conducting state often occurs at a sharp critical field H_c and a critical temperature T_c [107], [108].

In Type II superconductors, the Meissner states gives way to a vortex state, which eventually transitions to a normal conductor. A vortex in a superconductor is a local departure from superconductivity, leaving behind a circular edge on a 2D surface, or a

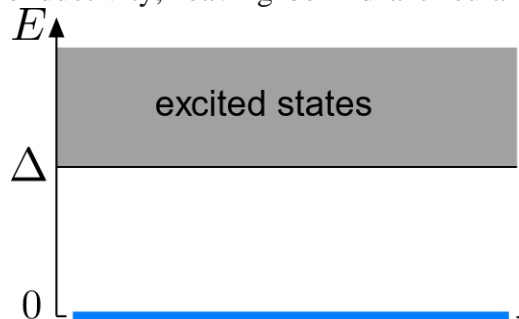


Figure 2.6 Shows the energy states in a superconductor such that states from 0 to Δ are purely for cooper pairs (bosons) and are considered within the superconducting gap with a total energy of 2Δ . States above the absolute energy of Δ are excited states and exist as individual fermions (electrons or holes). Transport in or out of the superconductor within the superconducting gap is a 2-particle process and always requires cooper pairs of electrons. Image source – Ref. [109].

cylindrical core in a 3D superconductor. Within the vortex is a normal conductor that allows magnetic flux to permeate through and outside the vortex is a Meissner superconductor that repels all magnetic flux.

For thin films of superconductors, H_c is anisotropic and is often suffixed with $H_{c\perp}$ for out-of-plane and $H_{c\parallel}$ for in-plane critical fields, respectively. An enhancement in the in-plane critical field of aluminum, when the magnetic field is in the plane of the film, is well known [110] (see Figure 2.7). As will be discussed later, observation of MZMs requires application of a “large” magnetic field. This enhancement allows for the use of Type I superconductors (like aluminum) with MZM devices, as the required magnetic field is along the axis of the 1D chain of electrons, in the plane of the superconductor.

s, p, d and f-wave classification of superconductors refers to the electron pairing symmetry based on their spin, singlet (for Cooper pairs of opposite spin $S=0$) or triplet (for Cooper pairs of the same spin $S=1$) and angular momentum ($l=0$ (s-wave), $l=1$ (p-wave), $l=2$ (d-wave), $l=3$ (f-wave)). This leads to a variation in the spatial and temporal (phase) dependence of the Cooper pair cloud, amongst the different types of classifications. To summarize the above, s-wave: $S=0$, $l=0$ (electrons with opposite spin, trivial superconductor), e.g. Al, V, Nb, etc.; p-wave: $S=1$, $l=1$ (electrons with same spin, topological superconductor), e.g. predicted in InSb-Al nanowire hosting MZMs and Sr_2RuO_4 ; d-wave: $S=0$, $l=2$ (electrons with opposite spin, trivial superconductor), e.g. $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$, GdOFeAs , etc.; f-wave: $S=1$, $l=3$ (electrons with same spin, topological superconductor), e.g. predicted in d-wave semiconductors on 2DEGs hosting MZMs and UPt_3 . Mathematically rigorous description of the above classification can be found elsewhere [111]–[113].

MZMs can also be theoretically be founds in other systems, which is worth mentioning. As has been previously mentioned, a 1D electron system hosting MZMs is predicted to be a p-wave topological superconductor. While smoking gun signatures of p-wave superconductivity in nanowires hosting MZMs are still elusive, MZMs are also expected to appear at the edge of the vortex core of a p_x+ip_y topological superconductor⁷. Sr_2RuO_4 is a candidate material system to host such superconductivity [113]–[115].

As wafer-scale quantum well heterostructures hosting 2D electron gases are well known, a 2D electron system in a strong spin-orbit coupling semiconductor when lithographically etched to a 1D wire and coupled to an s-wave superconductor, is still expected to show MZMs. This expands the concept of MZM-based qubits to a wafer-scale technology. This concept is expected to be an essential building block towards the realization of scalable superconductor-semiconductor networks, which in turn is necessary to demonstrate an operational topological quantum computer.

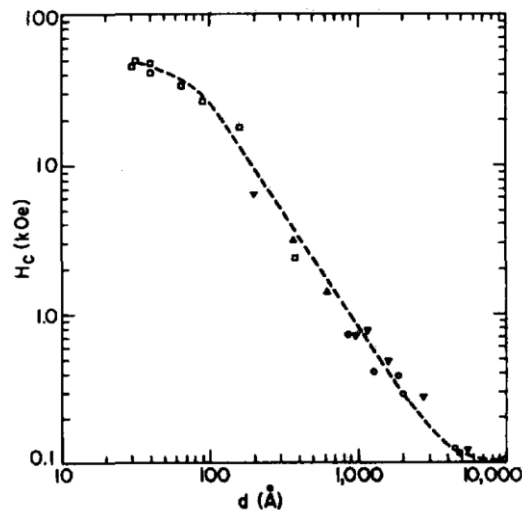


Figure 2.7 shows the increase in the in-plane critical field of Aluminum on reducing its thickness. Dashed line is a guide to the eye. Image source – Ref.[110]. Reprinted from R. Merservey and P.M. Tedrow, J. Appl. Phys. 42, 1, pp.51-53 (1971), with the permission of AIP Publishing.

⁷ p_x+ip_y refers to p-wave superconductivity in 2D, as against to *p-wave* in 1D and has a different spatial dependence of Cooper pairs [71].

On coupling a 2D electron system to a d-wave superconductor, Majorana localization and oscillations in emergent novel f-wave superconductivity have been predicted [116]. Experimental signatures of f-wave superconductivity in any system remain to be seen.

3. Chapter 3 – Experimental Techniques

3.1. Epitaxial materials growth

The desired heterostructures for low dimensional electron systems in semiconductors can be realized by various crystal growth techniques, each with their own advantage. For controlled growth of heterostructures, leading to electron confinement, techniques utilizing vacuum are the most favorable. Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) also known as Metal-Organic Vapor Phase Epitaxy (MOVPE) are the two most prominent vacuum techniques. Both of these techniques will be discussed in detail below.

Molecular Beam Epitaxy: MBE uses vapors of solid sources by heating pure elements (almost always elemental solid sources, though compound sources can also be used) individually in an Ultra High Vacuum (UHV) ambient for crystal growth (often called solid-source MBE). The vacuum apparatus (chamber and peripherals) idle at pressures of the order

of 10^{-11} Torr or less, while the operating pressures (not standby/idle) can be as high as 1×10^{-6} Torr. Due to UHV, the mean free path of vapors is much larger than the source to sample distance, making the vapors atomic or molecular beams. By identifying the conditions for crystal growth, and by starting off with a crystalline surface, it is possible to *epitaxially* layer materials using the above mentioned atomic or molecular beams.

By precisely controlling temperatures of the individual source furnaces or “effusion” cells, a control over the *flux* can be obtained, which translates to an exponential precision in control over the thickness of the layered element or compound. Operation under conditions where the mean free path remains larger than the source to sample distance also sets an upper limit on the flux of a given species and sets an overarching limit on the growth rate by MBE. For example, mean free path is estimated to be ~ 100 km (10^5 meters) at $\sim 10^{-10}$ Torr, reducing exponentially to ~ 100 mm (10^{-1} meters) at $\sim 10^{-4}$ Torr. In comparison, the typical source to sample distance is typically 100-300 mm, while peak flux of III-V elemental species can be as high as $\sim 10^{-5}$ Torr. Choosing the sequence of exposure of different elemental furnaces to the

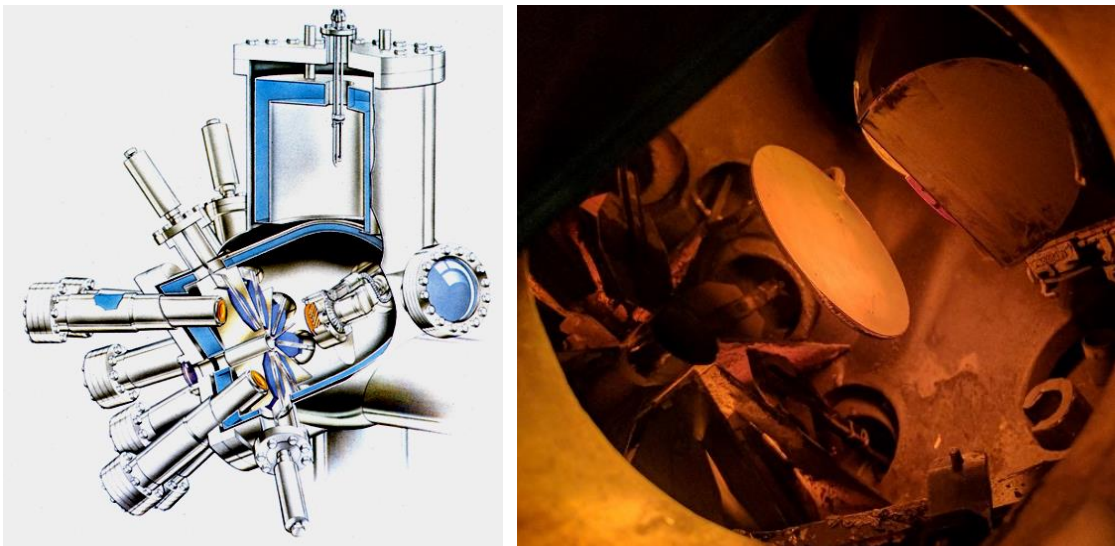


Figure 3.1 On the left is the schematic and on the right the image of the VG V80H III-V MBE in the Palmstrom Lab at UCSB. Schematic image source – Ref. [117]. Reprinted by permission from Springer, Molecular Beam Epitaxy by M.A. Herman and H. Sitter (1989).

substrate surface in effect allows hetero epitaxy of different materials. A cross-sectional schematic and a corresponding image of a III-V VG V80H MBE in operation at UCSB is shown in Figure 3.1.

Because MBE systems are baked to about 200C for at least a few weeks to attain UHV, all items within the UHV system are carefully chosen to reduce outgassing at bake temperatures and during normal operation. To maintain structural stability and to reduce outgassing, refractory materials are typically chosen for parts that will be exposed to elevated temperatures (commonly over 250°C and always above 450°C) as opposed to the stainless-steel body of the rest of the system. The long baking time and the use of refractory materials makes MBE a slow and costly technique.

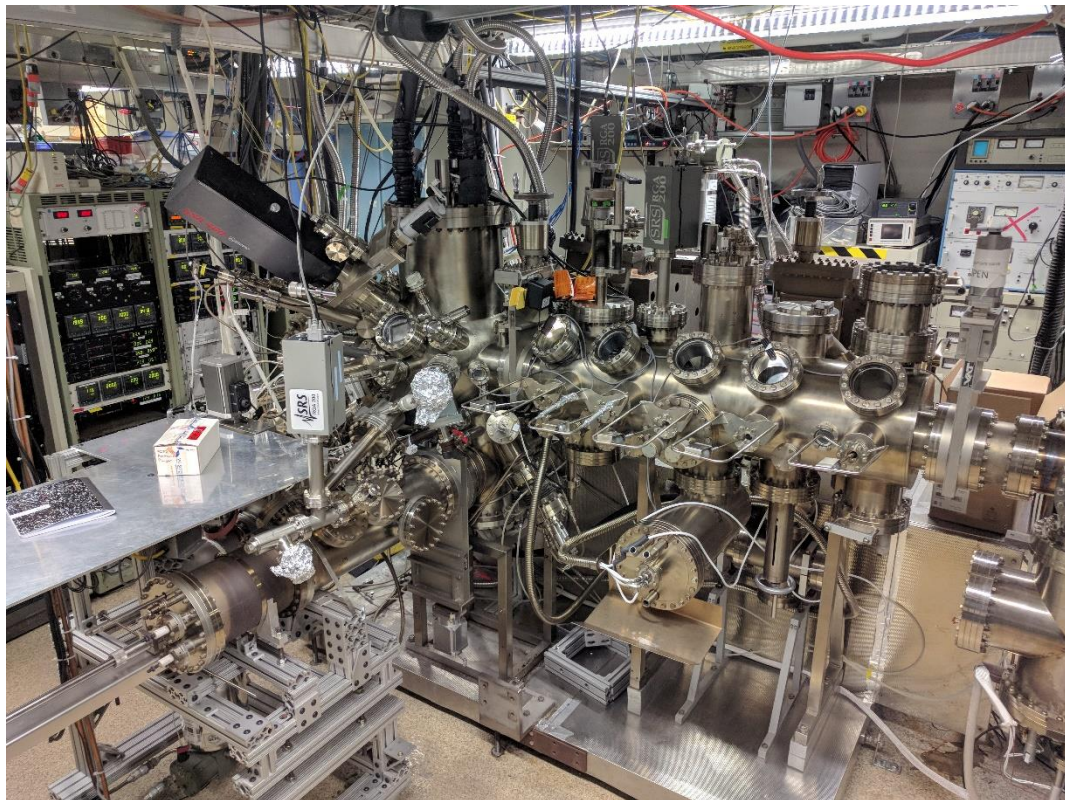


Figure 3.2 VG V80H III-V MBE in the Palmstrøm Lab at UCSB.

The extremely clean ambient of UHV significantly reduces the unintentional dopant concentration and has made MBE the technique of choice for growing ultra-high mobility electron and hole systems. The UHV ambient is also used to study the growth of crystals *in-situ* by electron diffraction and absorption-based techniques like Auger Electron Spectroscopy [118] and Reflection High Energy Electron Diffraction (RHEED). These techniques allow for the monitoring of growth rate and surface stability. The knowledge of surface reconstructions, as observed in RHEED, can aid in the determination of sample temperature and elemental fluxes (or flux ratios).

Improvements made to the MBE at UC Santa Barbara, as part of this work, are the focus of Appendix B. A historical perspective on the development of MBE leading to its current state is available elsewhere [119]. A picture of the MBE growth and sample preparation chamber, primarily used for this work, is shown in Figure 3.2.

Metal-Organic Chemical Vapor Deposition: MOCVD is an alternative approach to crystal growth that starts with metal-organic precursors. By controlling the individual metal-organic gas pressure, using a combination of capacitance manometers and needle valves or mass flow controllers, a control over the crystal growth rate can be obtained. The base pressure of an MOCVD system is much higher than an MBE system (typically 10^{-3} Torr), and the metal organic molecules are expected to crack at the surface of the growing sample, to further growth.

In terms of efficiency, the refilling or replacement of source material (gases, stored in individual gas bottles) in MOCVD is comparatively less obstructive to the operation of the rest of the chamber than in MBE and is also much faster. However, the price of high-purity metal-

organic precursors is a major component of the operating cost, as is the cost to purify hydrogen carrier gas that transports precursor from their individual bottles (or bubblers) to the reactor.

Typical MOCVD operating pressures can vary between 10^{-2} Torr and 10^2 Torr, a major jump as compared to MBE. Due to the higher operating pressures and the use of metal-organic precursors, the background impurity incorporation is much higher in MOCVD. Dominant impurities are often carbon and hydrogen. *In-situ* growth monitoring techniques based on electron diffraction or absorption also cannot be used in MOCVD due to the significantly short electron mean free path at the high operating pressures.

There are some cases where MOCVD is unequivocally the best technique. In applications where intentional doping exceeds the background doping (e.g. in opto-electronic structures like lasers or LEDs and in ohmic contacts to transistors) or in material systems where the effect of these impurities can be mitigated by post-growth processes (e.g. annealing Nitride semiconductors post-growth to release trapped hydrogen and activate p-type dopants), MOCVD provides a fast and commercially viable approach to crystal growth.

A hybrid of MBE and MOCVD techniques is Chemical Beam Epitaxy (CBE), also called Metal-Organic Molecular Beam Epitaxy (MOMBE). Bluntly put, CBE uses metal-organic precursors to grow crystals in a UHV chamber. The base pressure of CBE systems can be 10^{-11} Torr (similar to MBE), while typical operating pressures can vary from 10^{-9} Torr to 10^{-4} Torr depending on application (in between MBE and MOCVD). The intricacies of coupling two techniques (i.e. high-pressure source gases as used in MOCVD and ultra-high vacuum equipment from MBE) make CBE a complex and challenging tool. Higher growth rates than in MBE can be harnessed by using the metal-organic precursors, while certain *in-situ*

monitoring techniques like RHEED can still be used. However, CBE is also plagued with higher background impurity incorporation and hence reduced peak carrier mobility. Advantages of MOCVD like Selective Area Growth (SAG) are best harnessed in the CBE configurations for applications relevant to this work and will be explained in detail later. While MBE is the primary technique used in this work, 1D nanowires of InSb were grown by MOCVD.

Nanowires of interest for this work are typically 25-100 nm in diameter and greater than $2\mu\text{m}$ in length. MBE, CBE and MOCVD can all be used to grow VLS nanowires, while each technique has its own minor differences. The encompassing growth mode utilized to grow nanowires is referred to as Vapor-Liquid-Solid (VLS) growth mode.

To grow nanowires using the VLS technique, Au droplets of desired nanowire diameter and typically 3-8 nm thick are evaporated onto the starting substrate (typically a single crystal wafer of III-V compounds like InP, InAs, InSb). At growth temperatures (typically 400 to 600C depending on material) III-V vapors interact with the Au particle, and dissolve in the gold [120]. They then crystallize and precipitate under the gold, droplet at the substrate droplet interface. The process thus goes from a vapor to a liquid to a solid phase, giving it its name. VLS growth by MBE will be discussed in detail this work.

3.2. Electrical device measurements

To improve material quality, routine electrical characterization of all 2D structures is essential. The key figures of merit for evaluating material quality and heterostructure performance are carrier mobility, sheet carrier density and sheet resistivity. For applications related to topological quantum computing and for the observation of novel physical

phenomenon in materials, low temperature measurements (2K or lower) under applied magnetic fields are essential. For structures with aluminum as the superconductor in contact with the semiconductor, temperatures less than 1K are required to observe superconductivity; to observe exotic states like the MZMs further cooling to less than 50mK electron temperature is essential.

Under the application of a perpendicular magnetic field, electrons traversing perpendicular to the applied magnetic field, experience Lorentz force. This leads to a buildup of potential across the sample perpendicular to the magnetic field and perpendicular to the flow of the electrons (the direction of applied external potential). This potential is directly proportional to the mobile carrier concentration in the material and is referred to as the “Hall voltage”. The resistance of the sample measured perpendicular to the flow of current is called “Hall resistance” or “ R_{xy} ” and the resistance measured along the flow of current is called “ R_{xx} ” or “longitudinal resistance”.

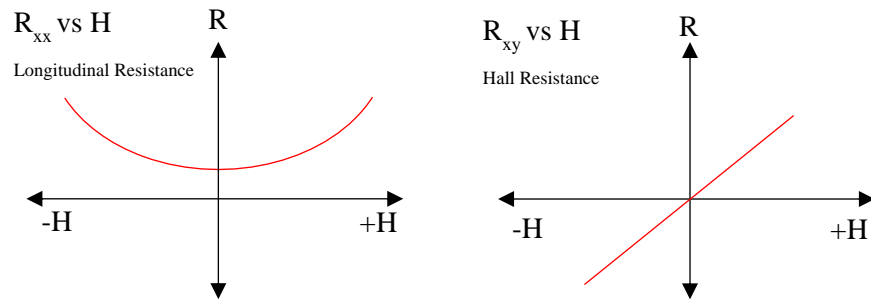


Figure 3.3 The left panel shows the expected classical magneto-transport response of longitudinal resistance vs applied perpendicular magnetic field, regardless of measurement geometry. The right panel shows the classical magneto-transport behavior of Hall resistance vs applied perpendicular magnetic field, regardless of measurement geometry. These classical responses are evident in 3D transport through trivial metal and semiconductor materials at all temperatures. 2D and 1D electron systems also show the same response under conditions where classical phenomenon are more apparent than quantum mechanical (high temperature and low magnetic field).

Typically, in a block of metal (3D), the longitudinal resistance, increases quadratically with increasing magnetic field, leading to a parabolic curve in R_{xx} vs H (the applied magnetic field). R_{xy} , on the other hand, typically shows a linear rise vs applied field, as shown in Figure 3.3. One of the physical devices used in this measurement is referred to as a Hall bar (see Figure 3.4), while measurements can be performed in other geometries as well, including the Van der Pauw geometry.

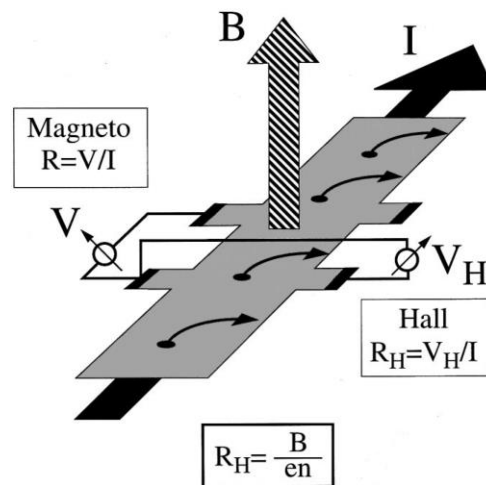


Figure 3.4 The schematic of electron transport through a hall bar under an applied perpendicular magnetic field. Hall voltage is measured perpendicular to the direction of current flow and perpendicular to the direction of applied magnetic field. Longitudinal resistance is measured along the direction of electron transport (or opposite to it). Electrons experience a Lorentz force under an applied magnetic field bending their trajectories to the outer edge of the Hall bar. Image source – Ref. [105]. Reprinted figure with permission from H.L. Stormer, Rev. Mod. Phys., 71, 4, pp.875-889 (1999). Copyright (1999) by the American Physical Society.

Sheet Resistivity: Depending on sample geometry, R_{xx} at zero field is used to calculate sheet resistivity or sheet resistance, while the slope of R_{xy} is used to calculate the sheet carrier concentration [121]. Comparing measurements of R_{xx} vs temperature, at zero field, can be used to understand the nature of the 2DEG and to infer the quality of the sample. This is because 2DEGs, being metallic in nature (Fermi level is above the first quantized sub-band), are expected to have a continuous reduction in resistance as temperature is reduced. The ratio of room temperature resistance to the final resistance at 2K or lower is called the Residual

Resistance Ratio (RRR). This ratio is a very good qualitative metric of sample quality and may be used quantitatively if identical sample geometries and layer structures are used for comparison.

In 2DEGs where the R_{sheet} increases with decreasing temperature, the 2DEG could be assumed to be vanishing with reducing temperature. This effect is primarily due to the reduced ionization efficiency of dopants. In GaAs, D_x - centers (silicon dopants in AlGaAs, negatively charged during cool down) can also lead to a sudden drop in mobility if structures with doping in AlGaAs are used. In all InSb 2DEGs, R_{sheet} increases with decreasing temperature initially, regardless of the presence or absence of an electron gas below the Fermi level at 2K. This is primarily due to an increase in band gap of InSb/AlInSb and a reduction (and eventual absence when at 2K) of intrinsic ionization. Intrinsic ionization dominates all InSb/AlInSb electrical characteristics at room temperature.

In some samples exhibiting a freeze-out of carriers at low temperatures, an LED can be used during the cool down, and turned off once the sample reaches about 4K. GaAs 2DEGs have extensively been studied with photo-excited carriers while the first evidence of photo-excited carriers in InSb 2DEGs was observed as part of this work and is described in detail later.

While Hall measurements of materials have been studied since the technique was developed by Edwin Hall in 1879, a significant advancement related to low dimensional electron systems, was made in 1980 with the discovery of the Integer Quantum Hall Effect (IQHE) in Si/SiO₂ Metal-Oxide Field Effect Transistor (MOSFET) by Klaus von Klitzing [122]. At the Si/SiO₂ interface, in a MOSFET operating in the inversion regime, a 2DEG forms

(in an otherwise p-channel). When cooled to $<10\text{K}$, this 2DEG can still be modulated in density by the transistor gate. It was discovered that modulating the 2DEG density at a constant non-zero perpendicular magnetic field led to the quantization of Hall resistance in quanta of h/e^2 . Correspondingly, the R_{xx} deviated from a parabola and R_{xx} minima touched zero resistance for every quantization in R_{xy} . The most significant consequence of this discovery was that the values of quantization in R_{xy} were independent of the host material system or geometry of measurement and were purely a function of Planck's constant and electronic charge [122]. Hence, quantum of resistance of $25,819.2\ \Omega$ was defined with extreme precision and became the international standard for resistance in 1990 [123]–[125] and in 2018, in conjunction with the Josephson coupling constant led to redefinition of Planck's constant and the SI unit of mass – kilogram [126].

This observation of quantized values in R_{xy} was attributed to the formation of Landau levels in the host material on application of a perpendicular magnetic field [127]. The Landau level separation (in energy) depends on the applied magnetic field. Landau level broadening or smearing can occur due to increased disorder or an increase in temperature (above 0K)⁸. When gate voltage is varied at a constant magnetic field, the Fermi level traverses various Landau levels individually, leading to the Integer Quantum Hall Effect⁹ (IQHE) [128]. The improvement in mobility of GaAs 2DEGs with a modulation doped heterostructure, led to the discovery of Fractional Quantum Hall Effect in GaAs by D. Tsui, H. Stromer and A. C.

⁸ In material systems where a sufficiently large Landau level separation could be engineered, or under extreme magnetic fields, the effect could be seen even at room temperature and was first observed in mono-layer graphene [128]. Recent work by J. Jang, et al., demonstrated a direct visualization of Landau levels under an applied magnetic field [129], [130].

⁹ After the initial discovery in 1980 of the Integer Quantum Hall Effect in a Silicon MOSFET by K. von Klitzing, resistance quantization in R_{xy} was soon confirmed by D.C. Tsui and A.C. Gossard, et al. in 1981, in the GaAs 2DEG system [214]. The significance of this observation, followed by its confirmation, led to the 1985 Nobel Prize in Physics being awarded to K. von Klitzing.

Gossard in 1981 [129], [130]. A detailed review of the Fractional Quantum Hall Effect (FQHE) and its applications in topological quantum computing, can be found elsewhere [35], [105].

While GaAs QWs have been the focus of intense study since 1980, discovery of FQHE in InAs QWs remained elusive for decades. InAs QWs grown on GaSb substrates with record electron mobility of $2.4 \times 10^6 \text{ cm}^2/\text{Vs}$ were demonstrated at ETH Zurich by T. Tshirky, et al., in 2017 [131]. Shortly thereafter, M. Ma, et al., reported the discovery of the $4/3$ Fractional Quantum Hall State in samples grown by T. Tshirky [132]. This discovery is of great interest in the search of non-abelian states in InAs QWs and has spurred renewed interest in the field. FQHE states in InSb QWs still remain elusive.

As was previously mentioned, increasing the perpendicular magnetic field leads to the Fermi level traversing the Landau levels. At low magnetic fields, oscillations in the longitudinal resistivity can occur when the separation between Landau levels is not large enough. This outcome is a manifestation of the Quantum Hall Effect. In the low magnetic field limit, R_{xx} minima may still not touch zero, but the R_{xy} remains quantized for every minimum in R_{xx} . These oscillations at a frequency inversely proportional to the magnetic field are referred to as “Shubnikov-de Haas oscillations” (SdH) [133]–[136]. Similar oscillations are seen in all other quantities that depend on the density of states, due to the creation of Landau levels.

The onset of SdH oscillations in the corresponding magnetic field is an important means of quantifying scattering in a 2DEG. A lower onset field indicates reduced scattering. This figure of merit, notated as $[\text{Tesla}^{-1}]$, can also be translated to a mobility – quantum mobility –

and is known to sensitive to all scattering. In comparison, Hall mobility is only sensitive to large angle scattering and hence is always larger than quantum mobility.

Measurement setup: Variable temperature measurements from 1.8K to 300K were performed in a Quantum Design Physical Property Measurement Systems (PPMSs), equipped with a 14 Tesla (Palmstrom group) or 9 Tesla (PPMS DynaCool, UCSB MRL TEMPO facility) superconducting magnet. Measurements down to 100mK were performed in an HPD Adiabatic Demagnetization Refrigeration equipped with a 5 Tesla superconducting magnet. Some measurements were also performed at the National High Magnetic Field Lab in Tallahassee on an 18 Tesla, Kelvinox 400 system with a base temperature of 20mK (SCM-1).

A standard lock-in technique was typically used for measurements of the QHE. Stanford Research SR830 lock-in amplifiers were used to measure V_{xx} and V_{xy} (later converted to R_{xx}



Figure 3.5 The left panels shows a PPMS puck used to measure Hall bars fabricated of quantum well structures. Hall bars on the semiconductor are connected with In:Sn solder, via gold wires, to another blob of In:Sn solder on the PPMS puck. In samples requiring external illumination, a generic red colored LED is installed on two pins of the puck. The LED was operated at 10mA constant current, and limited the base temperature of the PPMS to 4-10K. Once the LED was turned off a base temperature of <2K could be achieved. On the right is a typical measurement setup showing the Quantum Design DynaCool cryogen free PPMS. The puck shown on the left is inserted in the PPMS and cooled to ~1.8K and measured at fields up to 9 Tesla using AC lock-in technique. Lock-in amplifiers and a GPIB ground isolator are pictured in the instrument cart on the right.

and R_{xy}) while a Keithley 6221 AC current source was used to source AC current (50nA-100 μ A; 3-180Hz), though lower currents may be desirable for future work on the search for FQHE. Upon using a lock-in as a pseudo current source, and by connecting a 100k Ω to 100M Ω resistor in series, it was also observed that artifacts were induced in the measured QHE. These artifacts were due to a “current regulation” on (a decrease in current due to a corresponding increase in load resistance) that occurred upon changing the magnetic field and resistivity of the sample. Measuring the sourced current actively and correcting it based on the measured current and voltage helped remove the artifacts, at the expense of another lock-in amplifier. An example of the PPMS DynaCool setup, and a Hall bar device with an LED on a PPMS puck are shown in Figure 3.5.

3.3. Device fabrication

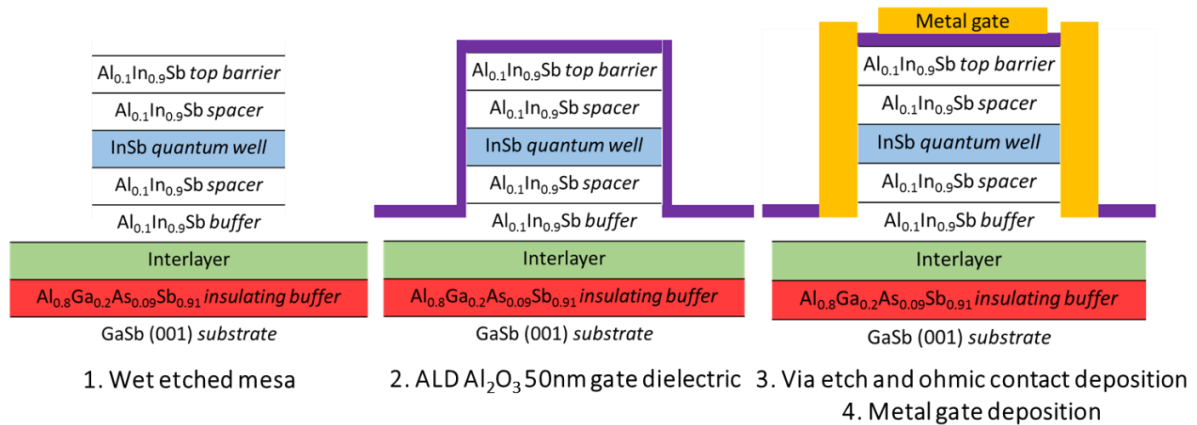


Figure 3.6 Process steps to make a top gated hall bar

A common fabrication recipe was employed for fabrication of Hall bar mesas and top gated hall bar devices for InAs, InSb and InAsSb quantum wells (with minor variations). This fabrication recipe was originally developed by Anthony P. McFadden, Borzoyeh Shojaei, Javad Shabani and Joon Sue Lee in the Palmstrom group at UCSB and has been described in greater detail elsewhere [137].

The process begins with defining a Hall bar mesa with AZ5214 positive resist and developed by AZ300MIF developer. The exposure and development parameters were specially tuned for processing in the UCSB nanofabrication facility. It was also observed that the developer visually changed the top surface of the exposed antimonide semiconductor. While most likely this is believed to be either a slight etch (due to the basic nature of the developer) or a change in the hygroscopic nature of the developed material (from hydrophilic to hydrophobic or vice versa). If a developed pattern was removed with solvent cleaning, remnants of this developer-semiconductor reaction were often visible. For future processing, it is hence advisable to minimize re-runs and use the least development time as may be necessary.

Post development, to remove unwanted photo-resist residue, an oxygen plasma cleaning was performed for 12 seconds at 100mTorr and 25 Watts. These parameters were found to be the minimum pressure and RF power to strike a plasma in the system available at UCSB. No Faraday cage was used for the cleaning but is advisable to reduce the risk of damage to the semiconductor.

A combination of $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{C}_6\text{H}_8\text{O}_7:\text{H}_2\text{O}$ (phosphoric acid, hydrogen peroxide, citric acid (buffer) diluted in water) in a 3:5:55:220 ratio was used for anisotropic etching of all antimonide and arsenide semiconductor layers. If needed selective etching of aluminum containing antimonides to stop at InAs or InSb QW layers was performed using buffered HF. The typical etch rate was found to be in the 30nm per minute range which was optimal for controlled etching of the semiconductor surfaces. The etchant was also found to be stable over time in its etch rate over a course of a month, with etch rate increasing with increasing time.

Over a course of six months, the etch rate was found to increase dramatically, typically exposing the (111) crystal planes.

Atomic Layer Deposition (ALD) was used to evaporate a 20-50nm Al_2O_3 amorphous dielectric layer for top gated devices, using an Oxford FlexALD system at 200 °C at a rate of $\sim 1 \text{ \AA/cycle/second}$. The precursors used for the evaporation were Tri-Methyl-Aluminum and water, with no oxygen plasma. Finally, a metal evaporation was performed in an electron beam evaporator, typically consisting of Ti/Au layers. If needed In or In:Sn metal was also evaporated in a thermal evaporator or the contacts were soldered/pressed on. A schematic of this process flow is shown in Figure 3.6.

4. Chapter 4 – InAs Quantum Wells (2D) and Wires (1D)

4.1. Introduction

This chapter will focus on realization of MZMs for topological quantum computation on an InAs semiconductor platform. Focusing on InAs 2DEGs, the chapter will explain why GaSb substrates are a superior choice for growing InAs quantum wells (QWs), and it will discuss what conditions were used to achieve the record-breaking electron mobility observed in a near-surface InAs QW grown in the Palmstrøm Lab's MBE.

The chapter will then go on to examine the growth of InAs nanowires for which will form the basis of making *in-vacuo* qubits detailed in Chapter 7. It will also discuss the results obtained from coupling superconducting aluminum to in-plane nanowires of InAs grown by Selective Area Epitaxy/Growth (SAG).

InAs QWs and nanowires are of interest in the field of topological quantum computation due to their increased spin-orbit interaction as compared to GaAs. With a lattice constant of 6.06 Å InAs is nearly lattice matched to GaSb (6.09 Å) and AlSb (6.12 Å). This matching allows for a wide variety of heterostructures to be synthesized for electronic and photonic applications [138].

The surface of InAs is known to be pinned in the conduction band [101] and hence undoped InAs forms an electron accumulation layer at the InAs-air (or vacuum) or InAs-metal interface (see Figure 4.1). This property can be exploited to inject supercurrent by proximitizing a near-surface (about 10nm or less deep) InAs quantum well with a layer of superconductor like aluminum [87]. Being an arsenide, the presence of an established *ex-situ* etch recipe to selectively remove aluminum from the surface of InAs, GaAs and InGaAs also aids tremendously in opening up a wide variety of superconductor-semiconductor device

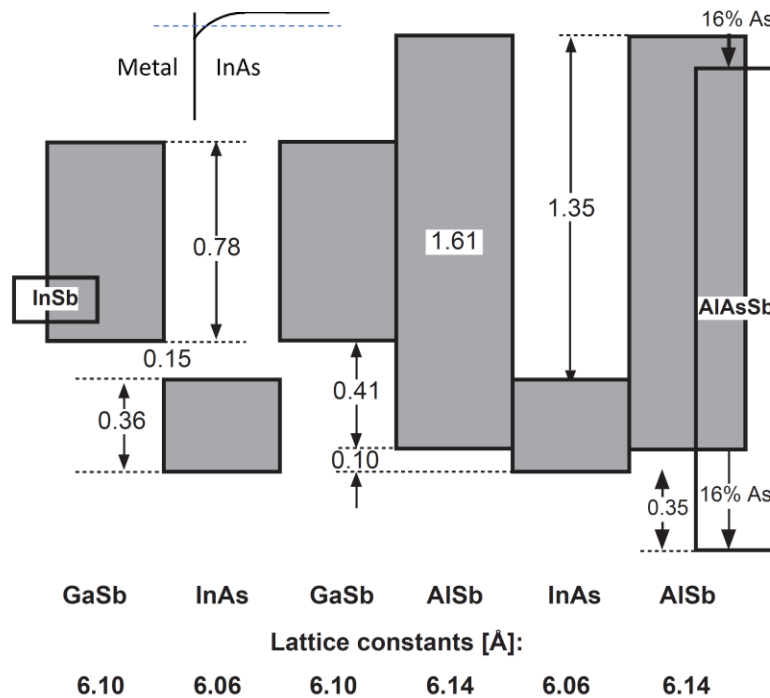


Figure 4.1 The figure shows the band alignments in eV of the 6.1Å family materials with a few others. Image source – Ref. [138]. Reprinted from Physica E: Low-Dimensional Systems and Nanostructures, 20, 3-4, pp.196-203, Copyright (2004), with permission from Elsevier.

geometries [139] and in exploring phenomena at the superconductor-insulator phase transition [140]. Selective etching recipes for removal of antimonide barrier layers to access a buried InAs quantum well are also available. This selective etch, aids in the deposition of ohmic contacts directly on the QW layer, significantly reducing contact resistance and contact formation uncertainty.

1D nanowires of InAs when coupled to aluminum were shown to host MZMs [79], [80]. Recently, these nanowires were used to confirm the presence of topological induced gap, which appeared on the closing of a trivial superconducting gap [72]. InAs nanowires benefit from the established MBE growth techniques and subsequent evaporation of aluminum *in-situ*, allowing for an atomically abrupt (sharp) and oxide-free (clean) superconductor-semiconductor hetero-interface necessary for induced superconductivity in such systems.

InAs quantum wells have also been demonstrated on InP substrates, especially if lattice mismatch is reduced by growth of InGaAs, InAlAs and/or InAsP buffer layers. InAs quantum wells on InP substrates have shown high electron mobility while also allowing for the use of the established nanofabrication processes for III-As [141]. This ability to fabricate nanoscale devices on InP/InAs hetero-structures has been utilized for selective area growth (SAG) of InAs on patterned InP substrates by Chemical Beam Epitaxy [142]. Coupled with *in-situ* evaporated aluminum, these in-plane nanowire networks have shown signatures of MZMs and are discussed in Section 4.4.

The InAs-GaSb bi-layer system exhibits a broken gap heterostructure at the interface of the two materials, with the conduction band minima of InAs being lower than the valence band maxima of GaSb (see Figure 4.1). This anomaly is predicted to host a 2D topological insulator

(2D TI) phase in thin layers, when the Fermi level is tuned appropriately. This 2D TI is also referred to as a Quantum Spin Hall Insulator (QSHI) for its ability to separate incoming electron current such that electrons of opposite spins travel with opposite momentum (i.e. on opposite edges, in opposite directions). On coupling superconductivity to such a system, MZMs are predicted to arise. A detailed analysis of the same, focusing on the materials considerations for forming the predicted topological insulator phase, is discussed in B. Shojaei, et al., [143].

4.2. InAs Quantum Wells

4.2.1. Prior work

There are several properties that make InAs quantum wells a promising candidate for exploration MZMs. Firstly, the surface of InAs is pinned in the conduction band at about 0.2 eV above the conduction band minima, which leads to a significant electron population on the surface [101]. This surface accumulation can be used for coupling superconductivity to the 2DEG.

Secondly, coupled with the low effective mass of InAs, the surface 2DEG of InAs can exhibit mobility in excess of 40,000 cm²/Vs at room temperature [144]. Buried quantum wells of InAs grown with InAlAs/InGaAs or AlGaSb/AlGaAsSb barrier layers above and below the quantum well (for electron confinement), show significant enhancement in electron mobility as compared to the intrinsic 2DEG at the surface (see Figure 4.2) [131]. Peak mobility of 2.4x10⁶ cm²/Vs has been reported in 25 nm deep InAs QWs on nearly lattice matched GaSb substrate [131]. As the QW is brought closer to the surface, peak reported mobility drops

rapidly (see Figure 4.2). Yet, the reasonable mobility of near surface quantum wells makes the mean free path long enough for quantum transport measurements.

Before quantum wells of InAs grown on nearly lattice matched GaSb substrates were proven to be best, a significant amount of work on InAs QWs was previously performed on lattice mismatched GaAs and InP substrates [137]. The lattice mismatch between GaAs and InAs is about 7% whereas the lattice mismatch between InP and InAs is about 3% [145]. Historically, the growth of InAs QWs on GaAs has been replete with dislocations; it required the growth of a multi-layered buffer structure with nucleation of high density of misfit dislocations at the heterointerface when switching from the 5.65Å lattice constant of GaAs to

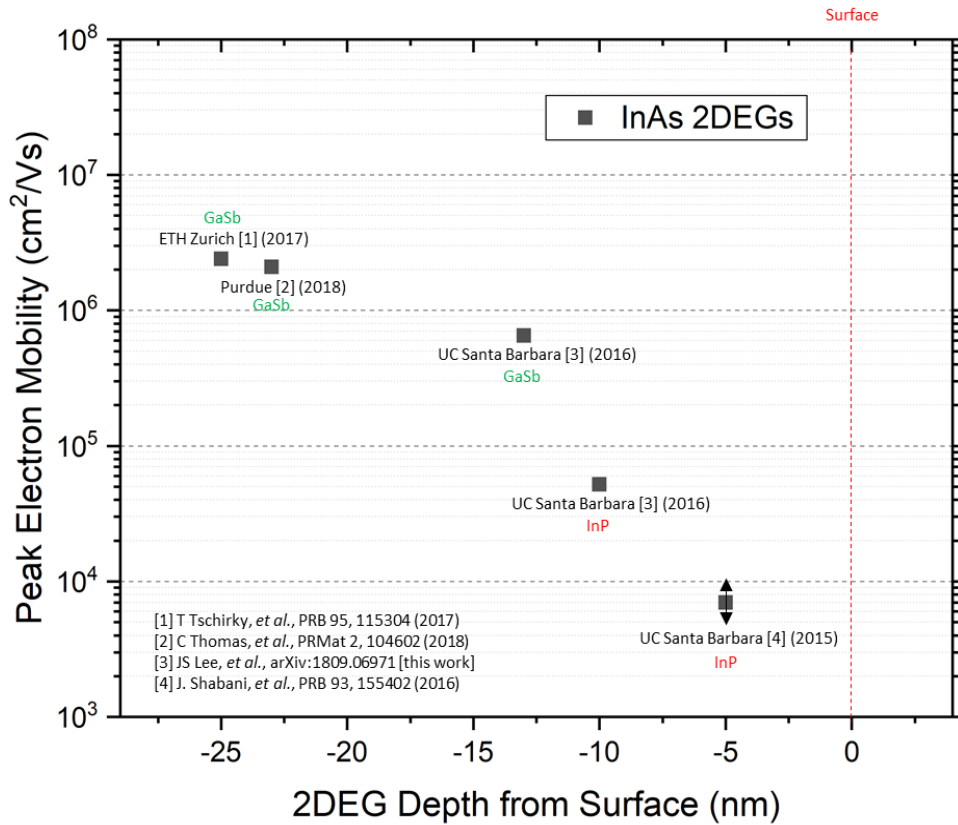


Figure 4.2 The figure above plots the peak reported electron mobilities in InAs quantum wells vs. their depth from the surface. It can be concluded that as the depth from the surface is reduced electron mobility tanks dramatically regardless of substrate and these results have been validated by a few different sources.

the 6.1Å family of InAs, GaSb and AlSb. While remedial measures like the growth of a GaSb/AlSb superlattice helped annihilate a fraction of the threading components of the screw dislocations generated by the misfit dislocations, the surface roughness was significantly impacted by the dislocations [146]. Moreover, recent work by B. Shojaei, et al., also reported a stunted quantum lifetime due to the high density of extended defects in quantum wells grown on GaAs as compared to quantum wells grown on GaSb substrates [146].

Until recently, GaAs substrates were still the substrates of choice due to the ready availability and low cost of semi-insulating GaAs and the relative ease of fabricating on an arsenide platform as compared to an antimonide platform. However, the high dislocation density and low Hall mobility in InAs QWs grown on GaAs necessitated exploration of other growth substrates.

Luckily, some substrates offer a compelling alternative to GaAs substrates. InP substrates, for example, have a reduced mismatch with InAs as compared to GaAs substrates. InP substrates also allow for the possibility of growth of graded buffers to effectively address the still-significant lattice mismatch between InAs and InP/InGaAs/InAlAs. While the antimonide barriers appear nearly lattice matched to InAs, another option is the use of arsenide barrier layers of InGaAs and InAlAs for growth of InAs QWs. This approach allows for arsenide only layer structures and the use of established III-Arsenide processing techniques for the fabrication of gate controlled mesoscopic devices.

On InAs QWs grown on InP substrates, J. Shabani, et al., with device fabrication and measurement by A. P. McFadden, reported the first demonstration of complete pinch off in an InAs 2DEG [147] and the demonstration of a Quantum Point Contact (QPC) in an InAs 2DEG

on InP [148]. A. Hatke, et al., recently reported a mobility of 1.1×10^6 cm²/Vs in 120nm deep InAs QWs on InP substrates [141]. While the deep quantum wells in all cases cannot be used directly for quantum computation due to the inability to couple superconductivity (from a superconductor 120nm from the QW), the record mobility on an InP substrate indicated the potential for further improvement by growth on a further reduced lattice mismatched substrate (like GaSb).

With a view towards realization of MZMs in InAs 2DEGs, J. Shabani, et al., evaporated superconducting Aluminum on near surface (~10nm deep) InAs QWs, without exposure to air, and thereby showed induced superconductivity in InAs 2DEGs on InP substrate [87]. While the electron mobility of these first-generation near-surface quantum well systems was limited to less than 20,000 cm²/Vs, H. Souminen, J. Shabani, et al., used these QWs as the basis for the design of scalable device geometries for realization of MZM devices in a 2DEG based Al-InAs system [90]. This was the first experimental observation of zero-bias peaks on a wafer-scale platform.

However, while InP substrates do have reduced mismatch as compared to GaAs substrates, they still do not offer the greatest electron mobility. To address the less-than optimal mobility that arose from growth on lattice-mismatched InP, B. Shojaei reported on the growth of InAs QWs on GaSb substrates and demonstrated a gate tuned mobility of ~800,000 cm²/Vs at a density of 1×10^{12} /cm² at 2K [149]. The QW structure employed a 15nm InAs layer that was 50nm from the surface and was grown on a bottom gateable GaSb:Te substrate. The sample was grown in the Palmstrom Lab's III-V VG V80H MBE prior to the modifications from 2016 mentioned in Appendix B.

To achieve this then-record electron mobility, certain notable departures from the established approach were made. Firstly, B. Shojaei developed an insulating buffer layer of $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}_{0.09}\text{Sb}_{0.91}$ that was lattice matched to the GaSb substrate. This allowed for the use of conducting GaSb substrates¹⁰ as bottom gate electrodes to an InAs QW. Secondly, barrier layers above and below the InAs QW were purely antimonide-like, allowing for a significantly reduced lattice mismatch between the substrate, barrier layers and the quantum well, such that the complete structure remained strained. Thirdly, GaSb and GaSb:Te substrates were atomic hydrogen cleaned immediately prior to MBE growth. The most drastic implication of this was the absence of square mounds on the surface when imaged by an atomic force microscope, indicating a dramatic reduction in density of threading components of screw dislocations propagating through the quantum well. Lastly, an improved MBE shutter sequence at hetero-interfaces to transition from antimonide-like barriers to arsenide quantum well was reported leading to the absence of any parallel conduction layer during pinch off and consequently full depletion of the quantum well layer on application of gate voltage. These improvements, originally developed by B. Shojaei, have been incorporated in all InAs quantum wells demonstrated in this work. A detailed discussion on the same can be found elsewhere [137].

¹⁰ While prior to 2014 undoped substrates of GaSb may have been partially conducting even at low temperatures (<10K), undoped wafers acquired from various vendors as part of this dissertation, were measured and showed semi-insulating response below 50K. Starting 2014, while undoped GaSb substrates could be used without concern for parallel conduction paths during measurements on the 2DEG, the development of AlGaAsSb lattice matched barrier was still necessary. Apart from acting as a low temperature gate dielectric, AlGaAsSb allows for growth of a thicker buffer layer separating the active QW region from the substrate-epi-layer interface without risk of relaxation.

It must also be noted that growth of InAs QWs on conducting Te doped GaSb substrates is still preferred over growth on undoped GaSb substrates due to the inherently lower etch pit dislocation density seen in Te doped GaSb wafers (<1000 /cm² as compared to ~2000 /cm² in undoped GaSb). The cause of this reduction in dislocation density of the native substrate, on addition of a doping concentration of Te (~10¹⁷ /cm³) is not well understood and is beyond the scope of this dissertation.

Inferences from the same have also been incorporated in the growth of InAsSb quantum wells in this work and are detailed in Chapter 6.

B. Shojaei, et al., reported QWs up to 15nm wide and observed a reduction in peak electron mobility, due to an increase in interface roughness scattering, for QWs less than 15nm wide. T. Tshirky, et al., report similar mobility to results previously reported for similar structures [131], [149]. T. Tschirky, et al., also observe that upon increasing the width from 15nm to 24nm in increments of 3nm, electron mobility can be drastically enhanced up to a peak mobility of $2.4 \times 10^6 \text{ cm}^2/\text{Vs}$ (the highest value reported to date, in any InAs QW, as of this writing). Beyond 24nm, the InAs lattice is expected to relax onto the barrier layers, leading to a sudden drop in peak mobility. The record mobility samples, demonstrated by T. Tschirky, et al., were 25nm from the surface and were gate tuned to the maxima of electron population (electron density) in the first sub-band, to measure this high mobility¹¹. For comparison, previous work by B. Shojaei, et al., reporting peak mobility of $800,000 \text{ cm}^2/\text{Vs}$ and report by A. Hatke et al., of a peak mobility of $1.1 \times 10^6 \text{ cm}^2/\text{Vs}$ were also gate tuned to the peak of first sub-band occupation [141], [149].

The record high mobility values reported by T. Tschirky, et al., opened avenues for search of Fractional Quantum Hall Effect in InAs 2DEGs; a phenomenon that had still remained elusive in the InAs system. Without any top gate, the highest mobility InAs QW reported by T. Tschirky, et al., had an electron density of $7.8 \times 10^{11} /\text{cm}^2$, at 24nm wide and

¹¹ While mobility increases with increase in electron density as the first quantized sub-band is populating, on reaching the peak of first sub-band occupation, inter-sub-band scattering starts dominating and leads to a sharp reduction in mobility as the second sub-band is filled. The mobility then increases again, as the electron density is increased until the peak of second sub-band occupation. The increase in mobility with increase in density is attributed to an increased screening of electrons, due to their increased population, from intrinsic and extrinsic scattering centers.

25nm deep from the sample surface. The mobility was 1.8×10^6 cm²/Vs and the quantum mobility measured by the onset of SdH oscillations was 20,000 cm²/Vs. Since the quantum mobility is sensitive to all forms of scattering (similar to the fragile fractional quantum hall states), it is believed that a further improvement in quantum mobility would lead to observation of a variety of fractionally charged excitations. In part, this was confirmed. On measuring this particular record mobility InAs QW at 25mK in a 45 Tesla magnetic field, M. Ma, et al., discovered the first evidence of the fractional quantum Hall state of 4/3, a composite boson [131], [132]. This was confirmed by temperature dependent analysis of the FQHE state. No other FQHE state was observed and development of higher mobility electron systems is again expected to aid in their discovery.

4.2.2. MBE growth and magneto-transport measurements

As part of this work, a further enhancement in mobility as compared to previous structures was seen. Emphasis was put on near surface quantum wells for applications in topological quantum computation and results mentioned here are from epitaxial structures grown immediately after the MBE modifications of 2016. In comparison to previous growths on the same MBE chamber (prior to the modifications), the Hall mobility on 13nm deep InAs quantum wells was measured to be as high as 650,000 cm²/Vs at 2K with a sheet carrier density of 3.8×10^{11} /cm², without a gate, in a Van der Pauw geometry (see Figure 4.3) [150].

While quantum wells of higher electron mobility have been reported, all higher mobilities have been achieved with an increase in depth from the surface, which due to the inability to couple superconductivity from surface, makes the system less useful for topological

quantum computation. Hence, the peak mobility of $650,000 \text{ cm}^2/\text{Vs}$ is a record for near-surface quantum wells.

B. Shojaei, et al., had already concluded that the scattering mechanism that limits electron mobility in InAs quantum well systems on GaSb substrates was remote ionized impurities primarily from the surface [149]. To further study this limiting mechanism, J.S. Lee, et al., varied the top barrier layer above the InAs QW [150]. The depth of the QW was kept constant at 13nm from the surface and all other elements of the hetero structure were also kept the same. $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ and $\text{Al}_{0.9}\text{Ga}_{0.1}\text{Sb}$ were chosen as two top barrier materials. To avoid exposing AlSb like material to surface a cap layer of 3nm GaSb or 3nm $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ was put on 10nm AlGaSb. A third comparison sample was chosen to have a top layer of 13nm InGaAs.

AlGaSb has a larger band gap than InGaAs; AlGaSb also has a significant part of the band gap difference skewed to provide a significant conduction band mismatch. The change in the tunneling from the surface to proximity couple superconductivity from an Aluminum layer with AlGaSb barrier layer has not been studied. InGaAs is also significantly tensile strained on the GaSb host layer while AlGaSb is slightly compressively strained. The effective band gap in both the layers is expected to further change due to the strain. The QW width was kept constant at 7nm wide and all three samples were measured in a Van der Pauw geometry at 500mK in an Adiabatic Demagnetization Refrigerator.

After experimenting with the above variables, it was observed that the sample with the GaSb cap had the highest electron carrier concentration (not electron mobility) in the quantum well with a density of $13.3 \times 10^{11} / \text{cm}^2$. While it did not have the highest electron mobility, it showed signs of second sub-band occupation as evidenced by the additional states in the Integer Quantum Hall Effect. The Hall electron mobility of this sample was measured to be $287 \times 10^3 \text{ cm}^2/\text{Vs}$.

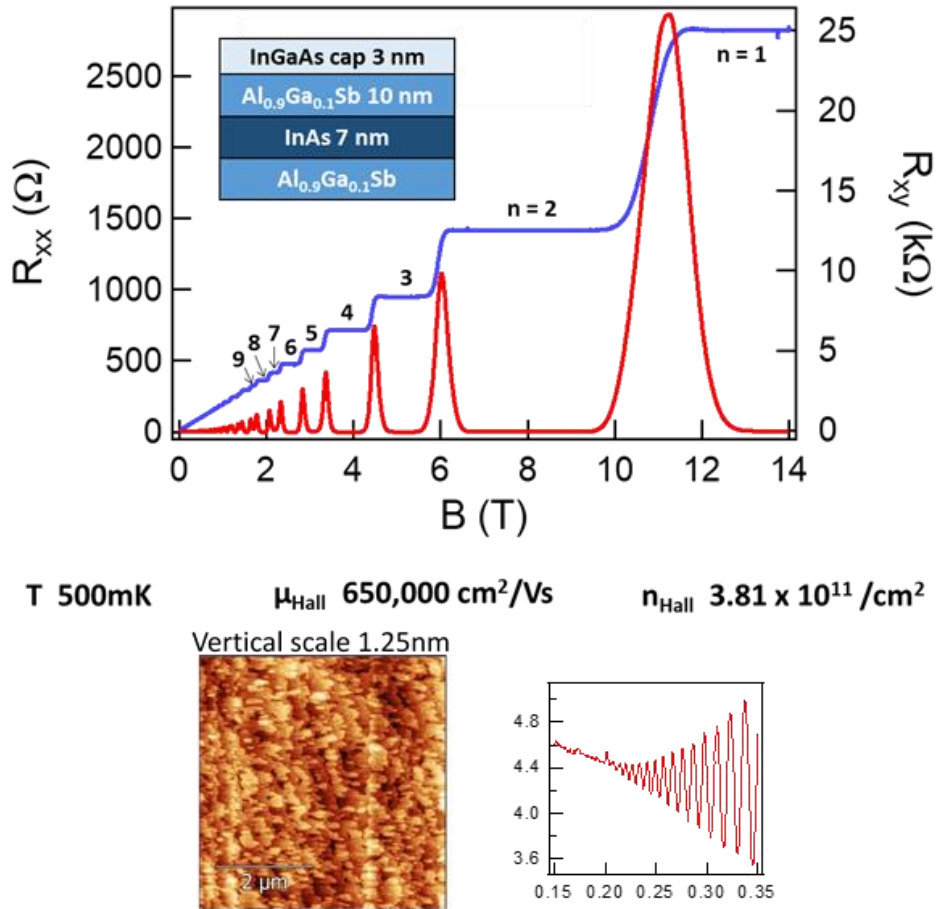


Figure 4.3 the top figure shows the integer quantum hall effect observed in an InAs quantum well that is 13nm from the surface, with the inset showing the layer structure for the quantum well. The Hall mobility was measured to be $650,000 \text{ cm}^2/\text{Vs}$ at an electron density of $3.81 \times 10^{11} / \text{cm}^2$ at 500mK. The onset of Shubnikov-de Haas oscillations was observed at 0.2 Tesla corresponding to a quantum mobility of $50,000 \text{ cm}^2/\text{Vs}$, which is the highest reported quantum mobility in InAs to date. The left bottom shows image shows the surface topography with a peak to peak roughness of two unit cells $\sim 12.5 \text{ \AA}$, over a $5 \times 5 \mu\text{m}^2$ area. Image courtesy – J.S. Lee, UCSB.

The sample with the 13nm InGaAs cap offered dramatically different results; it was observed to have an electron density of $8.1 \times 10^{11} / \text{cm}^2$ and a Hall mobility of $25.5 \times 10^3 \text{ cm}^2/\text{Vs}$. This significant reduction in mobility could be attributed to a partial relaxation of the top barrier layer, which would have led to the creation of additional new dislocations at the top barrier interface.

Lastly, the combination barrier with 10nm AlGaSb and 3nm InGaAs cap showed a record mobility of $650,000 \text{ cm}^2/\text{Vs}$ and simultaneously the lowest electron density of all three samples at $3.8 \times 10^{11} \text{ cm}^2/\text{Vs}$. The onset of Shubnikov-de Haas oscillations in this high mobility sample was observed to be at 0.2 Tesla, corresponding to a quantum mobility of $50,000 \text{ cm}^2/\text{Vs}$ at 500mK. This quantum mobility is the highest quantum mobility in an InAs quantum well system reported to date, regardless of all other factors (Hall mobility, depth from surface, substrate). In comparison, InAs quantum wells grown at ETH Zurich, by T. Tshirky, et al., and showing the fractional quantum hall state of $4/3$ and record Hall mobility in the $\sim 10^6 \text{ cm}^2/\text{Vs}$ range, also had a quantum mobility of only $20,000 \text{ cm}^2/\text{Vs}$ [131], [132]. Hence, with respect to other reported record mobility samples, then, these samples grown at UCSB offer a dramatic improvement in the material quality of InAs quantum wells.

It must be noted that, prior to the 2016 MBE modifications in the Palmstrøm Lab reported in Appendix B, the same VG V80H MBE was used to grow the then-record $800,000 \text{ cm}^2/\text{Vs}$ Hall mobility InAs quantum wells, which were significantly deeper (50nm from surface) and which had to be gate tuned to reach peak mobility at about $1 \times 10^{12} / \text{cm}^2$ at the peak of the first sub-band occupation. The significant improvements made to the MBE, along with improvements in operating procedures and a better understanding of the growth of InAs quantum wells, all led to this record demonstration.

4.2.3. Future directions for MBE growth

The improved electron mobility that these InAs quantum wells offer will have many useful applications. The search for fractional quantum Hall states in InAs quantum wells grown in the Palmstrom Lab at UCSB is in progress as of this writing. Also, in progress is the MBE growth of next-generation structures and the fabrication of devices for the gate control of electron density to the peak of the first sub-band occupation. Further details of this work have been reported elsewhere [150]. In the future, deeper quantum wells, primarily 25nm and 50nm-deep structures, need to be grown to directly compare the improvements made. Additionally, at a density of $3.8 \times 10^{11} / \text{cm}^2$, gate tuning to increase electron concentration to the peak of first sub-band occupation should lead to a further enhancement in mobility, which remains an outstanding challenge.

Another important question for further research remains: If scattering from the surface is the key limiting factor, how can electron mobility in InAs quantum wells be further improved? A deeper quantum well, though not immediately relevant for applications in topological quantum computing, may allow for a significant enhancement in electron mobility as compared to near-surface quantum wells¹². Deep quantum wells of InAs can be used to further explore and understand the occurrence of fractional quantum Hall states, especially, in the search for predicted non-abelian states.

If a deeper quantum well of InAs is to be employed to further increase peak mobility the choices of top barrier layer, gate dielectric, and gate control, are also critical. When exposed to air, the surface of a III-V semiconductor forms oxides that may lead to charged surface

¹² In comparison, highest mobility GaAs quantum wells reported to date with Hall electron mobility of the order of $3.7 \times 10^7 \text{ cm}^2/\text{Vs}$ [174], [175] were 180nm from the surface or more.

scattering centers, which are also potentially donor states leading to the intrinsic carrier concentration in the quantum well. Ex-situ growth of an Atomic Layer Deposited (ALD) AlO_x and HfO_x dielectric has also been studied with both showing intrinsic carriers in the quantum well at zero gate voltage [149], [151], [152]. ALD dielectrics have been proven to operate on III-Antimonides [149], [153], and, while being amorphous in nature, their contribution to further deterioration of electron mobility in the InAs quantum well has not been studied due to a lack of crystalline materials for comparison.

Taking all of the above in account, this work proposes a buried quantum well of InAs, with an $\text{Al}_x\text{Ga}_{1-x}\text{As}_y\text{Sb}_{1-y}$ barrier layer lattice matched to the GaSb substrate. This top barrier layer is known to be electrically insulating [151] and can act as a single crystal, epitaxial, lattice matched, top gate dielectric. Integration of the top barrier with the gate dielectric, to form one single crystal, insulating dielectric layer has shown to enhance transport in other material systems¹³.

Additionally, while metallic gate electrodes are also standard, the metal-semiconductor interface may lead to additional charge states, due to dangling bonds at the interface, that would potentially image onto the quantum well, leading to formation of new scattering centers. To alleviate this source of scattering centers, a single crystal, epitaxial, lattice matched, metal or metal-like gate is preferable. Being a metal, such a gate layer could then be exposed to air and any oxide-formation related scattering centers would then be screened by it. Luckily, in the

¹³ A shift to a single crystal dielectric (hBN) and a metal-like gate layer (multi-layer graphene) has led to significant strides in the discovery of new fractional quantum Hall states and has improved the tunability of fractional states in graphene [150]. These dramatic improvements have partly been attributed to the removal of a questionable scattering layer at the conventional metal-dielectric (e.g. Ti/Au-hBN) interface. By employing graphene/graphite as a metal gate, a nominally dangling bond-free interface is formed leading to significant enhancement in the quality of the observable fragile fractional quantum Hall states and enabling the predicted discovery of novel non-abelian fractional quantum Hall states.

6.1Å family of InAs-GaSb-AlSb, InAs offers the potential to be such a metal-like semiconductor gate layer. InAs forms an intrinsic surface charge layer, with its Fermi-level pinned in the conduction band, at the surface. Hence, a few-nanometer thick InAs may form an ideal single crystal, epitaxial, lattice matched top gate.

Intentional doping of the InAs may help better screen the surface charges that may form on oxidation of the InAs layer on exposure to air. Also, the thickness of this n-InAs layer must be limited to ~10nm so as to avoid lattice relaxation on the host layers of AlGaAsSb (lattice matched to GaSb). Further study of this proposed buried quantum well heterostructure, as shown in Table 4.1, with a single crystal semiconductor dielectric and semiconductor gate is in progress, as of this writing.

Table 4.1 Proposed generic layer structure of an all semiconductor top and bottom gate-tunable InAs quantum well eliminating metal-semiconductor and semiconductor-amorphous dielectric scattering layers. If layer thicknesses are chosen appropriately, all layers can be lattice matched or strained to the GaSb substrate, eliminating the formation of additional dislocations and new scattering centers for electrons in the quantum well.

n-InAs	Top Gate
$\text{Al}_x\text{Ga}_{1-x}\text{As}_y\text{Sb}_{1-y}$	Top barrier and Gate Dielectric
InAs QW	Quantum Well 2DEG Channel
$\text{Al}_x\text{Ga}_{1-x}\text{As}_y\text{Sb}_{1-y}$	Bottom Barrier and Gate Dielectric
n-GaSb	Bottom Gate and substrate

4.3. InAs VLS nanowires

While 2D electrons in a quantum well promise exciting results and a potential for scalable platform for realization of MZMs, realization of simple, proof-of-concept devices in the nascent field of topological quantum computing, requires etching down the 2D sheet of electrons leaving behind 1D nanowires. Growth of 1D nanowires, using Vapor-Liquid-Solid

(VLS) technique is a compelling alternative to grow bottom-up 1D nanowire structures for proof of concept devices.

The use of InAs nanowires for the observation of zero-bias peaks, considered to be signatures of MZMs, is not new; the first observation of zero-bias peaks in an InAs material system was reported by A. Das, et al., [79] shortly followed by A.D.K. Finck, et al., [80] followed by other detailed studies of various MZM characteristics by NBI QDev [84], [96]. Because of the great potential of nanowires to help realize MZMs, this section will discuss growth of InAs nanowires by VLS technique in the Palmstrom Lab's III-V MBE system. The section will also discuss *in-situ* evaporation of a partial shell of superconducting aluminum on said nanowires. (See Chapter 7 for a discussion of long InAs nanowires to make two superconducting islands joined by a superconducting bridge and separated by a gate defined quantum dot, thereby leading to the construction of a Majorana loop qubit.)

For the purposes of this work, InAs nanowires offer two main advantages that make them worthy of detailed consideration for MZM realization. Firstly, independent of the search for MZMs, the growth of InAs nanowires by Vapor-Liquid-Solid (VLS) technique in an MBE is well established [120]. Secondly, InAs nanowires offer a well-defined path to the selective removal of superconducting aluminum partial shell with regards to the nanowire surface by wet chemical etching (specifically, by using aluminum etchant Transene-D). This etching process makes lithographically defined superconductor-semiconductor structures significantly easier to create as compared to other antimonide-based materials systems (e.g. InSb). The combination of these two advantages makes *rapid prototyping* of superconductor-semiconductor hybrid devices based on InAs-Al a reality. This rapid prototyping is essential

in the current stage of topological quantum computing where realization of MZMs and their subsequent braiding are still a matter of active interest and research.

The potential drawbacks of the InAs material system are the low g-factor as compared to InSb and the potential electron accumulation at the sidewall-facets of the nanowire ($\{110\}$ type sidewalls). Because of a lack of clear understanding of required superconductor-semiconductor coupling strength and g-factor for suitable demonstration of topologically protected MZMs, researchers are unable to make a definitive statement on whether low g-factor and surface electron accumulation on the nanowire facets, are factors limiting the applications of InAs (as opposed to InSb, which has a comparatively higher g-factor) in topological quantum computing. However, the potential advantages of InAs nanowires still outweigh these drawbacks. The rest of this section will discuss in greater detail the growth of InAs nanowires by the VLS technique in the Palmstrom Lab's III-V MBE system.

First, some basic definitions and descriptions. Nanowires are typically between 10nm to 1 μ m in diameter. The diameters that are of interest for the purposes of topological quantum computation are in the 50 to 100nm range. The length is much easier to tune as compared to the diameter and is typically of the order of 2-10 μ m. Newer applications require greater separation between MZMs on either ends of the nanowire or nanowires; for shadow qubits (discussed in Chapter 7) the typical lengths are greater than 20 μ m. With the diameter of the wire being so small, VLS nanowires for a quasi 1D chain of electrons as required for realization of MZMs. Furthermore, while a 1D nanowire is in principal a 1D electron chain, the Fermi level (chemical potential) and the intrinsic ionization of charge carriers truly determine the available number of 1D channels. Application of a gate voltage uniformly along the length of

the nanowire to deplete the electron density in the nanowire, may allow for tuning the Fermi level to the necessary helical gap regime (as discussed in Section 1.3) for realization of MZMs.

With those definitional terms clarified, our discussion can turn to the specific techniques for growing InAs nanowires. MBE growth of InAs nanowires by VLS technique typically begins with blanket evaporation of 0.5-3nm of Au on a substrate of GaAs, InP or InAs (While blanket evaporation of Au on the surface of an epi-ready III-V substrate can be used to demonstrate growth of wires, it leads to uncontrolled growth of nanowires with randomly varying diameters and lengths. If reproducible carrier concentration and electrical properties are required from device to device, this method is discouraged.). VLS growth leads to the wires propagating along the [111]B axis. The exposed III-V substrate surface between the nanowires, also leads to further epitaxial 2D growth, which competes in part with VLS growth.

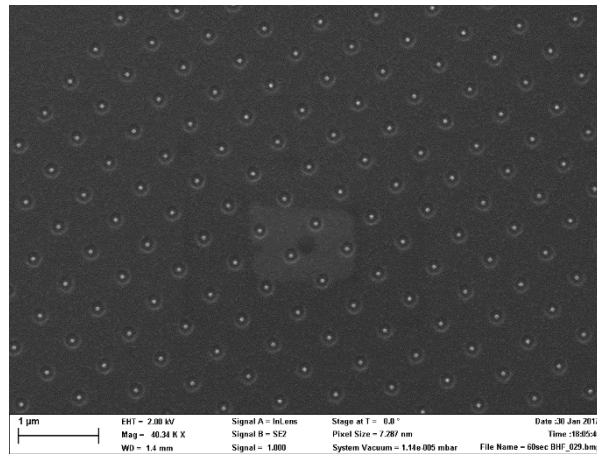


Figure 4.4 SEM image of a (111)B InP substrate with Au droplets deposited in electron beam lithography patterned vias on a dielectric. Image courtesy - S. Gazibegovic, TU Eindhoven.

For control over nanowire dimensions, the III-V substrate is lithographically patterned with a dielectric layer (e.g. SiO_x or SiN_x, ~20nm thick) and vias are opened in the dielectric corresponding to the diameter of the wire to be grown. A 3nm blanket-evaporated Au layer is then lifted off, leaving Au in “hockey puck” shaped discs on the III-V substrate in the vias (see Figure 4.4). Upon heating in an MOCVD or MBE reactor the puck-shaped Au liquifies by

forming a eutectic with In or Ga (from the InP/InAs/GaAs substrate) and VLS growth begins under an impingent III-V flux.

In comparison to VLS growth on bare epi-ready III-V substrates, VLS growth on patterned III-V substrates has significant differences, leading to a complete redefinition of the nanowire growth window. The differences in these two types of VLS growths can best be understood through a brief discussion of the sources of III-V ad-atoms forming the nanowire, in the following paragraph.

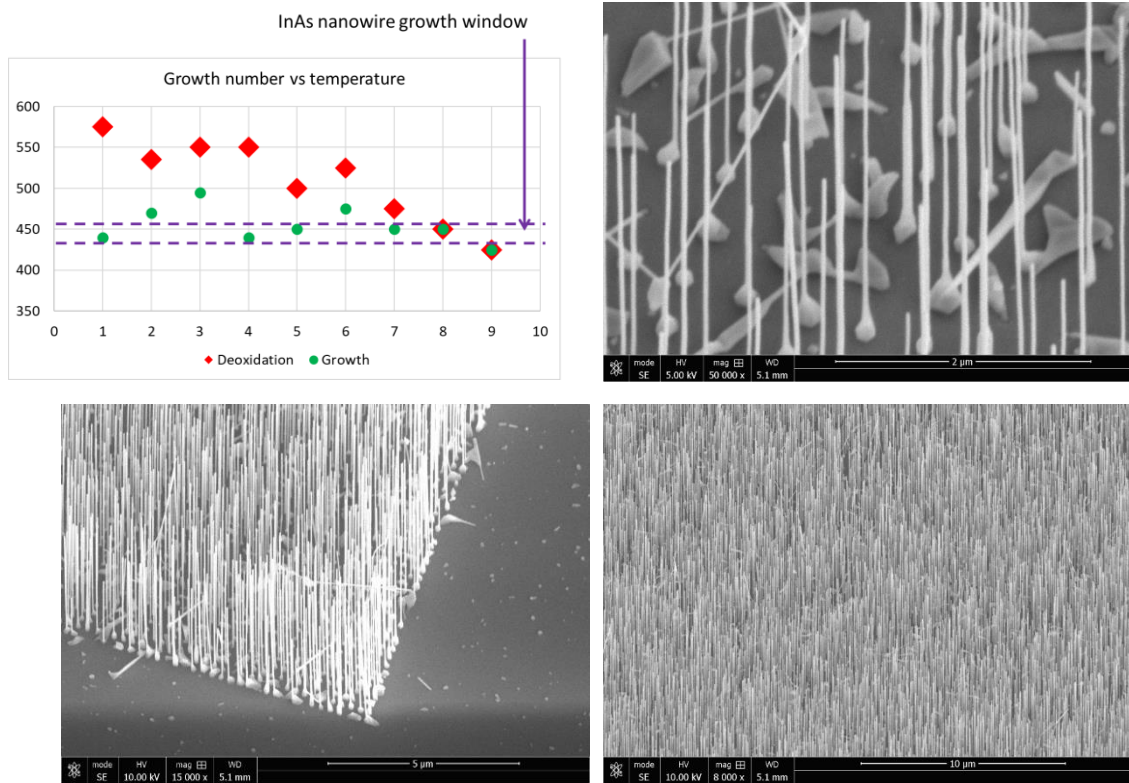


Figure 4.5 Clockwise from top-left: Temperature vs. sample growth number used to determine the growth window. Samples exposed to high temperatures showed melted nanowires and cracks in dielectric. Within the growth window the yield was >95% along with almost no growth on the dielectric mask. Top-right: Close up images of InAs nanowires on InP (111)B. Bottom-right: A zoomed out image showing the high yield of nanowires, forming a nanowire ‘forest’. Bottom-left: Highly selective growth of semiconductor nanowires with little to no growth on the dielectric surrounding the nanowires.

The basic mechanism of VLS growth is the same for both patterned and un-patterned substrates: Impingent III-V vapors dissolve in the liquid Au droplet, going through a vapor to liquid transition. The Au droplet, saturated with the impingent III-V atoms, then ejects a

crystalline III-V compound underneath it, leading to the liquid to solid transition and forming the nanowire. This mechanism is the same for growth on both patterned and un-patterned substrates. The departures between the two substrates now become significant. While the Au droplets only cover a very small percentage of the surface area of the wafer, the III-V flux, which is impingent upon the rest of the substrate, makes a major difference in how nanowire growth proceeds. On bare substrates, the excess III-V leads to 2D growth and competes with nanowire formation. On patterned substrates, on the other hand, the ad-atoms diffuse on the dielectric surface upon sufficient heating and eventually glide along the nanowire edges.

While excessive substrate heating can make the Au droplets diffuse away from the III-V inhibiting nanowire growth, very cold substrate temperatures lead to significantly reduced diffusion lengths, which in turn leads to tapered wires with thick stems (VLS and ad-atom diffusion) and thin ends (VLS growth only). Parasitic growth on the mask increases dramatically if growth temperature is reduced below optimum. A compromise between the two competing regimes is required: an approach that provides for enough diffusion so as to lead to growth of taper-free parallel/straight walled wires yet not so much as to lead to diffusion of the Au droplet away from III-V. This compromise leads to a significantly narrow growth window for VLS growth on patterned substrates, as compared to VLS growth on bare substrates. By a combination of pyrometry and band edge spectrometry, the growth window for successful growth of InAs VLS nanowires on patterned substrates was determined to be between 425°C to 445°C (see Figure 4.5). Adding antimony to grow InAsSb nanowires, as discussed in Chapter 6, further narrows this window to 435°C±5°C.

While this narrow growth window can be determined by experimenting with temperature, reproduction of the desired surface temperature with finite error within an MBE

reactor is non-trivial. In modern MBE reactors, thermocouple-based temperature measurement is found to be widely insensitive to surface temperature due to the relative placement of the thermocouple (i.e. close to the heater, behind the sample, not in contact with the sample block). The thermocouple reading hence changes from sample to sample, often strongly depending on reflectivity of the surfaces facing the heater, for the same semiconductor surface temperature. These challenges make it difficult to attain a target temperature, within the growth window, precisely and reproducibly.

An alternate means of measurement is to use known RHEED reconstruction phase transitions to estimate temperature. While RHEED reconstructions could be used to determine nanowire growth by VLS technique on bare substrates, it was observed that the 15kV electron beam, led to unwanted dielectric breakdown and preferential growth of polycrystalline III-V material on patterned substrates. This sticking of III-V ad-atoms to the dielectric surface, similar to the “cracking” of metal-organic precursors in CBE or MOCVD, leads to a preferential, uncontrolled reduction in effective flux that arriving on the nanowire stem. Moreover, nanowires within the RHEED beam path grow at a different rate as compared to nanowires out of the RHEED beam path. A visual change in the sample surface exposed to the RHEED beam was also observed. In short, RHEED is not a viable alternative for determination of temperature and achieving the narrow window of VLS growth.

To avoid using RHEED and thermocouple to measure sample temperature, non-contact thermometry based on band-edge spectrometry and pyrometry was finally utilized to determine temperature. Due to the arbitrarily small dimensions of the patterned substrate (3x3mm and up) and a required band-edge spectrometry spot size of 8mm (diameter), an InP calibration wafer was mounted on every sample block, which allowed for estimation of sample

temperature. The determination of the temperature for MBE growth of InAs nanowires on a patterned substrate, was performed by band-edge spectrometry (see Figure 4.5). By comparing to 2D growths, the sample to sample variation was determined to be less than 10°C when using band-edge spectrometry.

In an attempt to find an even more precise means of temperature measurement, a pyrometer with a spot size of 3.3mm (in diameter) was procured. It was observed that, by aiming directly on the nanowire wire growth sample, pyrometry provided an improved accuracy and significantly improved reproducibility between samples. Pyrometry was also found to be significantly more robust to surface quality (hazy, metal-rich surfaces) as compared to band-edge spectrometry. With temperature readings available from a pyrometer for the full duration of the growth run, it was also possible to feedback control the sample heater with the pyrometer temperature. Thus, pyrometry is an approach that allows for growth of hetero-epitaxial materials containing antimonides on patterned substrates (see Chapter 6 for more details).

When comparing the nanowire growth rate for bare versus patterned substrates, there are obvious differences. Due to the significant diffusion across the substrate surface, the required III-V flux (atoms/cm².s) for growth of VLS nanowires on patterned substrates was found to be about 10 times less than the flux for growth on a bare substrate. 100 nm/hour of planar InAs growth rate led to an effective growth of 2µm long nanowires with a diameter of about 50nm, every hour, scaling linearly, within the growth window. In comparison, on bare substrates, in the same MBE reactor, similar nanowire growth rates were achieved with 1µm/hour InAs planar growth rate. Increasing wire diameter reduced the vertical nanowire growth rate and scales accordingly.

While the growth of InAs nanowires by VLS has been well studied, the growth on patterned substrates, along with the specific determination of the growth window for materials in the UCSB MBEs, form the basis of Selective Area Epitaxy/Growth (See Section 4.4). As SAE/SAG requires growth purely on the semiconductor leaving clean dielectric surfaces behind, Figure 4.5 shows the growth of uniform nanowire forests and relatively clean dielectric surface close to a nanowire forest, in an early VLS growth of InAs on patterned InP substrates.

To make MZM devices, InAs nanowires grown on patterned substrates by MBE were also covered with a partial shell of aluminum by cooling down the substrate overnight (without any power to the heater), such that the substrate temperature is expected to have dropped to about -40°C (determined at a later date, after the modification of the sample manipulator and the installation of a Type-K thermocouple, see Appendix B for more details).

Upon evaporation of 10nm of Al on InAs, the nanowires appear to bow such that the facet covered with aluminum bows inward (see Figure 4.6). This effect is due to aluminum having a lower lattice constant than InAs or could also arise due to a mismatch of the thermal

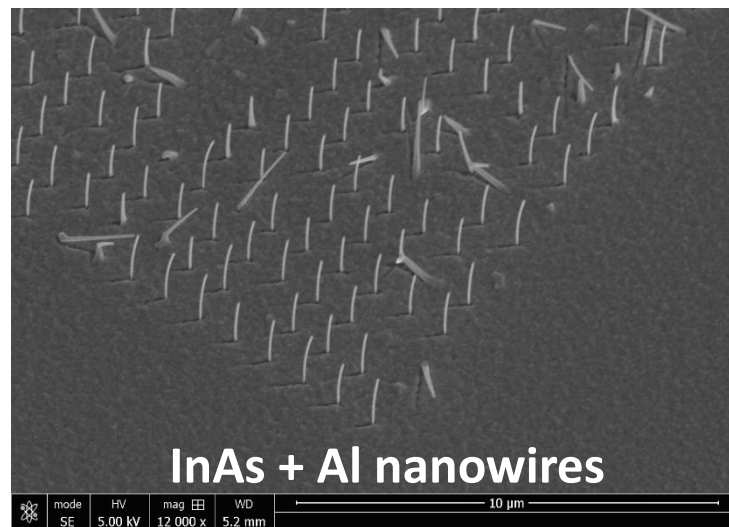


Figure 4.6 InAs nanowires on InP (111)B with a thin shell of aluminum, evaporated after growth in the MBE chamber on two facets of the nanowire. Thin aluminum is strained on the InAs such that it makes the nanowires bow.

expansion coefficient. It has been shown elsewhere [83] that the lattice of aluminum tilts by 3° to reveal a coincident lattice with InAs and that, upon growth at sufficiently low temperature (sub-zero Celsius), the interfacial reaction between Al-InAs can be substantially suppressed. Superconductivity induced from such an atomically clean and sharp interface induces a hard gap in the semiconductor (absence of sub gap states) though a definitive and systematic study of the same is lacking.

4.4. InAs Selective Area Growth (SAG) nanowires

This section will explore Selective Area Growth (SAG) of in-plane InAs nanowires followed by demonstration of InAs-Al devices on wafer scale SAG.

To begin, Selective Area Epitaxy/Growth offers some unique advantages over both top-down lithographically patterned nanowires grown from 2D quantum wells and bottom-up networks grown using vertical nanowires. The etch-defined nanowires suffer from significant scattering from rough edges defined by dry or wet etching. While the original mobility of the 2D electron gas may be very high, reduced dimensionality with rough sidewalls, makes the electron channel prone to significant scattering, dramatically reducing mobility. Furthermore, the significant etch depth between features, required for the electrical isolation of devices, makes the evaporation of other device elements like aluminum, complex. On the other hand, though bottom-up devices like nanowire networks have been demonstrated [81], they are not scalable. Again, the significant height variations involved in laying down a nanowire network on a dielectric substrate make the evaporation of superconductors and other dielectrics complicated.

Unlike both the top-down and bottom-up techniques, SAG offers the unique advantage that large, complex networks can be lithographically defined on the substrate, in a dielectric mask, prior to growth. Firstly, the III-V sidewalls formed by SAG are not exposed to etchants so that pristine structures can be fabricated, which in principle reduces scattering. Secondly, the dielectric layer between semiconductor surfaces opens up the possibility for the evaporation of superconductors to be used as bridges between different sections of the semiconductor. Such superconductor junctions are necessary for the implementation of Majorana qubits, specifically enabling readout via a parity transition in the superconducting island based on the outcome of the fusion of MZMs. It should also be mentioned that, compared to that of VLS nanowire-based networks, the demonstration of a working qubit on a SAG platform is significantly easier to scale up to a larger number of qubits in a relatively short time. This is because the key ingredients for growth and fabrication to get one working device remain the same when scaling up. Research focusing on SAG is hence a high reward investment.

In this work, InP substrates have been chosen for use in SAG because of their relative ease of nanofabrication as compared to the still-novel GaSb substrate. Due to the relatively narrow dimensions of the in-plane nanowires patterned (~50nm width), exceeding the critical thickness of InAs on InP leads to morphological changes apparent in scanning electron imagery. High-Angle Annular Dark Field – Scanning Transmission Electron Microscopy (HAADF-STEM) enables a detailed analysis of the substrate epi-layer interface and optimization of the same. In the first-generation structures, graded buffer layers of InAsP, on InP substrates, have been employed to reduce the immediate impact of lattice relaxation on active InAs channel hosting MZMs.

However, while ease of nanofabrication is a necessary requirement for a first demonstration, issues arising from the significant lattice mismatch between InP and InAs lead to a significant reduction in peak mobility that could be remedied with nearly lattice matched GaSb substrates. While the availability of insulating GaSb substrates would seem to encourage the further exploration of GaSb substrates for use in SAG, the existing dry- and wet-etch recipes have been found to be completely incompatible with antimonide surfaces, leading to excessive roughening of the GaSb surface post-nanofabrication. This makes the GaSb substrate very challenging to work with for epitaxial growth of a relatively smooth InAs channel hosting MZMs.

Attempts have also been made to use an AlGaAsSb lattice matched barrier layer on conducting Te doped GaSb substrates so that the in-plane nanowires could be bottom gated. These attempts use a thin InGaAs layer as a termination layer, allowing for a reduction in the damage caused by nanofabrication, by effectively encapsulating the antimonide surface. Utilization of GaSb substrates for InAs SAG remains an outstanding challenge and is expected to significantly enhance the mobility in the InAs channel. It is also expected to potentially enable global back gate control (by using a conducting substrate separated by an insulating barrier) and/or individual nanowire gates (by growth of an n-InAs gate metal-like layer below the InAs channel, separated by an insulating AlGaAsSb dielectric).

However, as mentioned above, the use of GaSb substrates for SAG will not be pursued in the scope of this work. The next several paragraphs will discuss the materials aspects of using these InP substrates to grow in-plane InAs nanowires for the realization of MZMs.

In a wafer fabrication process developed by J.S. Lee at UCSB, patterning of the InP substrates begins with a 3-5nm thick AlO_x ALD process at 200°C in an Oxford FlexALD system. Tri-Methyl-Aluminum along with water is used to grow AlO_x without the use of any oxygen plasma [142]. This lack of plasma is expected to lead a relatively weaker dielectric, but it also avoids any potential plasma damage to the III-V surface, preserving it for epi-growth. The growth rate has been adjusted to be about 1Å per second. Optionally, the system can be preconditioned with a thin coating of AlO_x at the same parameters, before inserting the sample for ALD. This is expected to eliminate most of the irregularities associated with evaporation of other dielectrics (like SiO_x) in a shared-use tool.

After the AlO_x layer is grown, a plasma enhanced chemical vapor deposition (PECVD) process is employed to deposit about 25nm of SiO_x on the substrate. The thickness of both the AlO_x and the SiO_x layer is measured individually in an ellipsometer. An electron-beam resist

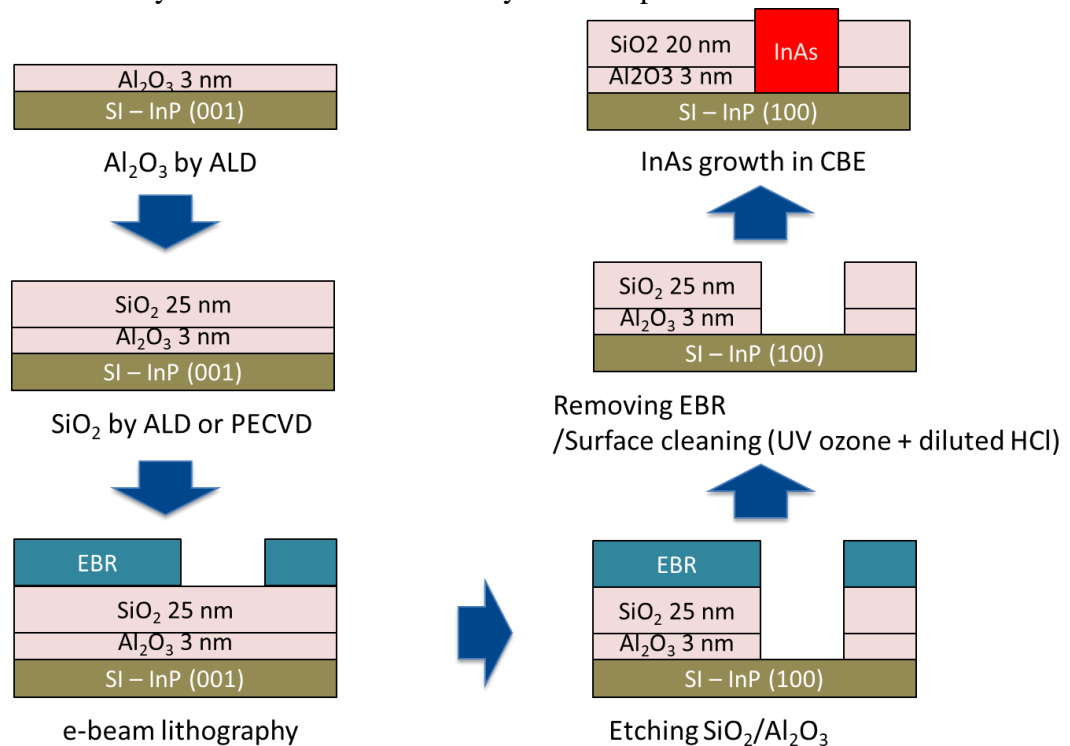


Figure 4.7 The process of patterning an InP substrate in preparation for selective area growth. Image courtesy – J.S. Lee, UCSB

(EBR) is then spun on, and necessary patterns are lithographically defined by electron-beam lithography. The typical widths of nanowires grown by this method vary from 30nm to 70nm, while typical lengths vary from 5 μ m to 20 μ m. After development of the exposed pattern, vias are etched in the SiO_x and AlO_x dielectric layers exposing the underlying semiconductor. The EBR is then removed and is followed by UV ozone treatment to ensure complete removal. The above process was developed by J.S. Lee with critical input from B. Markman and has also been described in detail elsewhere [142]. A process flow diagram for the same is shown in Figure 4.7.

Next, the patterned substrate is then prepared for growth. It is mounted on molybdenum block with indium along with a bare (unpatterned) InP substrate as a reference sample, for MBE and CBE growth. The reference sample is used to determine sample temperature, oxide desorption and growth conditions (group III-rich or V-rich) by band-edge spectrometry (in MBE) and pyrometry (in both MBE and CBE). In the CBE where phosphene PH₃ is cracked to give P₂ and H₂, thermal oxide is desorbed by observing the In rich reconstruction onset in RHEED. In the MBE where only an arsenic overpressure is available, thermal oxide is desorbed under an arsenic overpressure and again determined by RHEED. The thermal oxide desorption temperature in both cases is arbitrarily considered to be 525 °C.

It was observed that post thermal oxide desorption at ~525°C on InP, InAs growth with highest selectivity (i.e. growth occurring only in the trenches designated for semiconductor growth and not on the nearby dielectric) happened by maintaining the same growth temperature (525°C \pm 5°C) for growth of the InAs channel. The elevated temperature leads to an Indium rich surface on the reference sample, but near ideal growth on the SAG samples. The effective V/III ratio available for InAs growth in trenches on a SAG sample is estimated to be different from

the V/III ratio available for 2D growth on the reference substrate. This is due to the high diffusion length of III-V molecules and complete absence of growth on the dielectric. A typical InAs channel thickness of 30-70nm is targeted at a planar growth rate of about 100 nm/hr. An example showing high selectivity growth is shown in Figure 4.8.

Various considerations that may aid in determining the temperature growth window for other materials are listed below:

Firstly, any indium impinging on the sample during MBE growth is expected to have a sticking coefficient close to unity. This means that elevated temperatures are required to increase the diffusion length across vast lengths of the dielectric. While this immediate concern can be alleviated in MOCVD and CBE by the use of metal-organic indium as an indium source

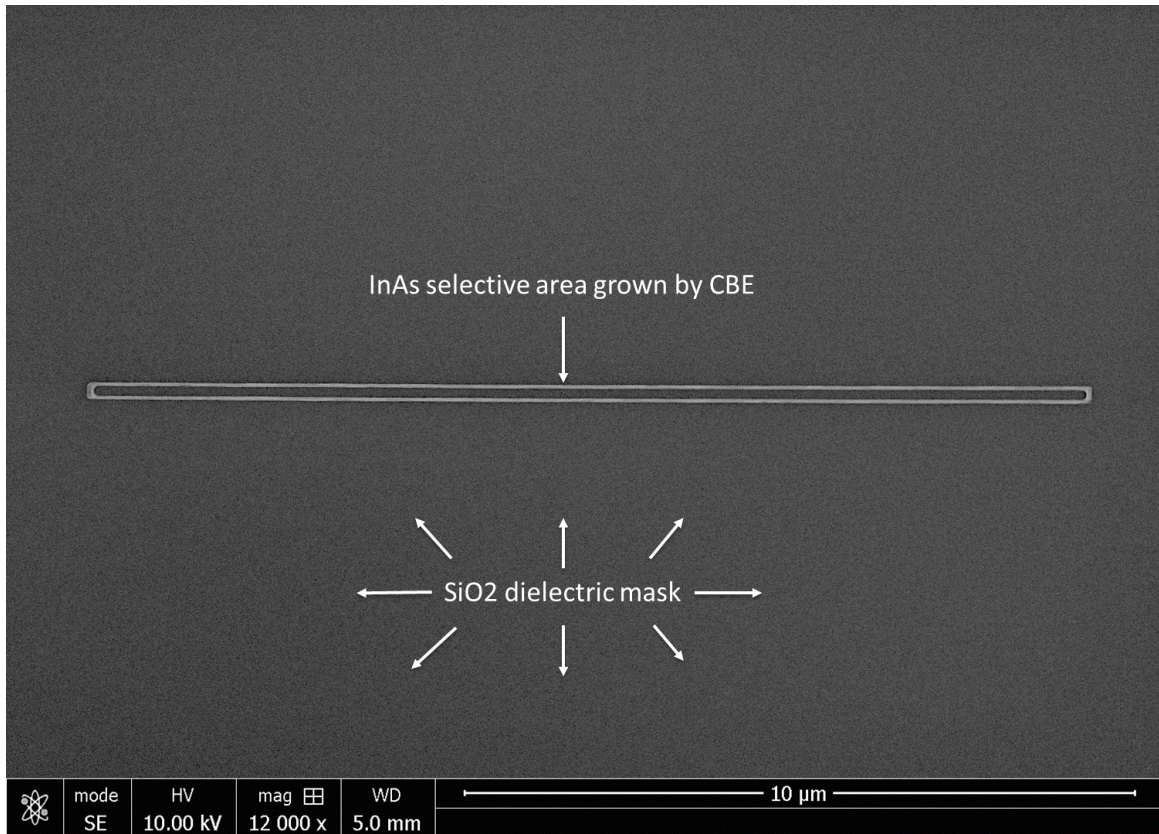


Figure 4.8 SEM image of selective area grown InAs on InP (001) by CBE, showing no growth on the dielectric (near ideal selectivity) and growth of long in-plane nanowires of InAs.

(e.g. Tri-Methyl-Indium), using metal-organic indium then requires an elevated temperature for another reason: to ensure sufficient cracking of the precursor on the sample, as cracking the precursor is a prerequisite to film growth.

Secondly, the use of As_4 should be beneficial as compared to As_2 due to the reduced sticking coefficient of As_4 as compared to As_2 . While As_4 is readily available by changing the cracker temperature in an MBE, the cracking of AsH_3 typically requires temperatures in excess of $800^\circ C$ (often around $1000-1200^\circ C$, high temperatures initially correspond to increased cracking efficiency from AsH_3 to As_2 and H_2 ; further heating leads to conversion of As_2 to As_1) leading to an inherently As_2 source in CBE and MOCVD growth.

The drawbacks having dimeric or monomeric group V sources is more apparent during VLS nanowire and SAG nanowire growth of antimonides, especially InSb, due to Sb having a lower vapor pressure. Challenges for antimonide selective area growth are further compounded by the temperature growth window for InSb growth, which happens to be narrower than that of InAs. Some of these challenges of growth of antimonides have been encountered in VLS growth of InAsSb nanowires and have been discussed in detail in Chapter 6.

Lastly, it was determined that complete oxide desorption is essential for uniform 2D nucleation of epi-layer within the trench. A partial island-like nucleation leads to multiple grains overgrowing on a layer of surface oxide, merging after sufficient overgrowth, and leaving behind grain boundaries, which are expected to be significant scattering centers for electron transport in the channel. *In-situ* atomic hydrogen flux for initial oxide desorption is expected to be helpful for uniformed, conformal nucleation of epilayers.

Additionally, it has been reported that atomic hydrogen exposure during selective area growth aides drastically enhancing selectivity in an MBE by increasing the adatom diffusivity on the dielectric surface [154].

Other considerations for determining the best out-of-plane ((001), (111)B, (110)) axis for crystal growth and the corresponding optimum in-plane growth directions (depending on n -fold surface symmetry) have been studied by J.S. Lee, et al., and have been detailed elsewhere [142]. Necessary lithographically defined patterns (e.g. the “sunshine” pattern shown in Figure 4.9) allow for the determination of optimum growth orientation of probing by microscopy in combination with electrical measurements.

For growth of superconductor-semiconductor networks with SAG, post III-V growth, the SAG sample is typically allowed to cool to room temperature overnight, prior to aluminum evaporation at about 80K (setup used for Aluminum evaporation has been described in detail

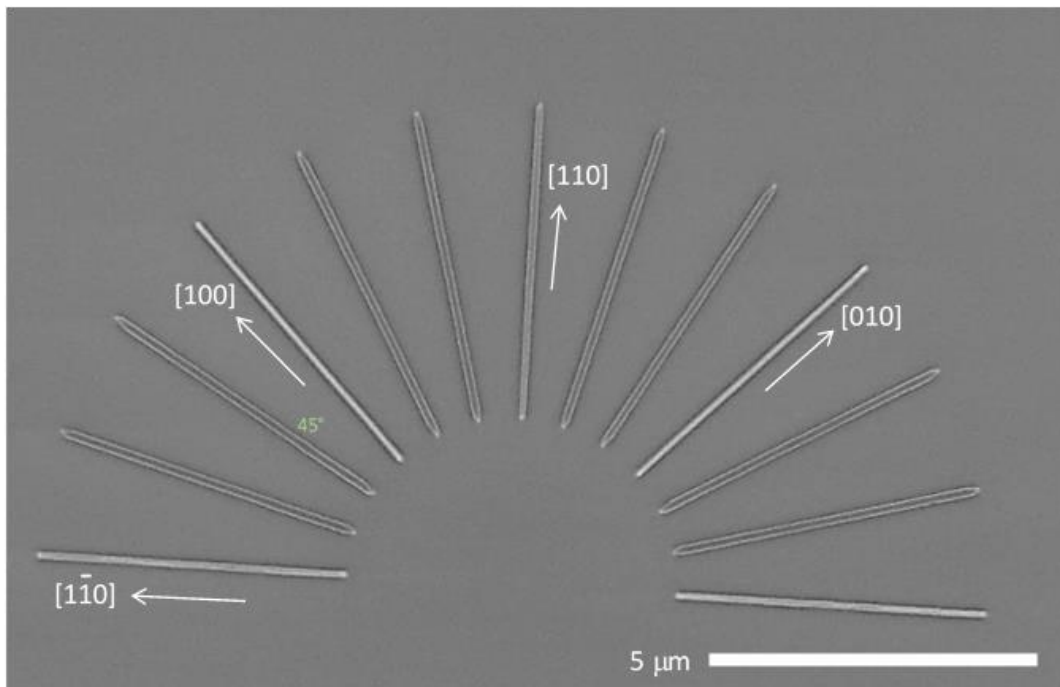


Figure 4.9 SEM image of a ‘sunshine’ pattern of nanowires of InAs grown on InP (001) with key in-plane directions marked. Best growth was observed along the [100] and [010] axis.

in Appendix B). The angle evaporation of aluminum typically leads to a self-shadowing on SAG structures, allowing for gate electrodes that are not screened by the aluminum layer to be placed on surface of the dielectric. Selective etching of the aluminum layer during device fabrication to make superconductor-semiconductor-superconductor and similar junctions is possible with Transene D etchant. Since the growth of in-plane nanowires by SAG and evaporation of superconductor are both wafer scale, etching of unwanted superconductor and patterning of gates is also wafer scale. This makes SAG a scalable technology with potential for immense progress and utility in eventual product technology when constructing a topological quantum computer.

Sacrificial features (e.g. ~200-2000nm high mounds/walls made of the dielectric material) in proximity with the active III-V channel allow for intentional shadowing of portions of the III-V channel, such that aluminum coverage on the III-V channel is not continuous. This intentional break in the aluminum leads to the formation of islands *in-situ*, obviating the need for etch defined superconductor-semiconductor junctions. These sacrificial structures have been termed as “shadow walls” or “smart walls”.

Having a lithography-free superconductor edge may in-turn lead to reduced sub-gap states in the superconductor. Since MZMs are expected to arise at/between the two ends of the superconducting island, the lithography-free superconductor edge could therefore improve the effective topological protection by reducing pathways for dissipation. The shadow wall structures are also proving to essential in immediate evaluation of various superconductors for improved superconductor-semiconductor characteristics, since selective etching of superconductor from semiconductor is not required.

InAs-Al SAG structures have been extensively characterized electrically and structurally. HAADF-STEM imaging of the cross section of the SAG nanowire shows an abrupt superconductor-semiconductor interface as well as preferential exposure of the {110} type facets on an otherwise (001) plane substrate. The exposure of the {110} facets is estimated to lead to a reduction in the surface energy, which is why a triangular cross-section is favored over a rectangular cross-section.

In-situ Energy-Dispersive X-Ray Spectroscopy (EDX/EDS) coupled with HAADF-STEM allows for imaging of the relative atomic species contributing to the image. Figure 4.10 shows one such EDX map. HAADF-STEM along the length of the wire, shows the stacking

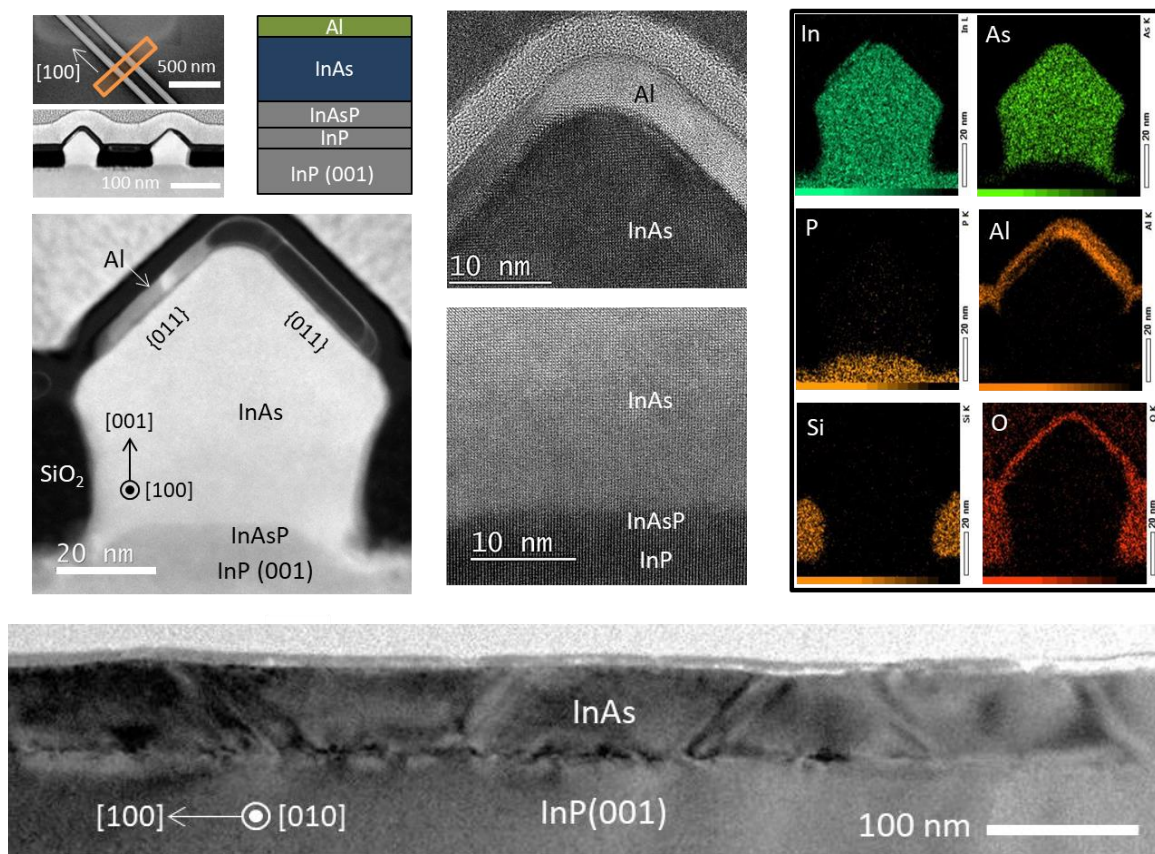


Figure 4.10 Image shows EDX and HAADF STEM of on InAs SAG nanowire grown on InP (001). The thin Aluminum layer is clearly visible on InAs with an almost atomically abrupt Al-InAs interface. The cross-sectional STEM image along the length of the nanowires shows stacking faults propogatting along the (111) slip planes of InAs. HAADF-STEM courtesy M. Verheijen, TU Eindhoven. Image courtesy J.S. Lee, UCSB.

faults arising from the lattice relaxation of InAs on InAsP/InP. Each stacking fault propagating through the channel is expected to lead to a significant reduction in the system's peak mobility.

Preliminary electrical measurements of Hall mobility and density were performed at 2K at UCSB. These were followed by gate-controlled measurements in a dilution refrigerator at Neils Bohr Institute, Denmark, and Technical University, Delft, Netherlands. Four-point IV measurements of individual nanowires (see Figure 4.11) showed full depletion of the channel. The measurements also showed a mobility of 1000-4000 cm²/Vs, which was extracted from the pinch-off curve of the nanowire under an applied gate bias.

Closed loops/rings of InAs (or any other conducting channel) at low temperatures, as shown in Figure 4.12, are expected to show quantum mechanical behavior of electrons – primarily wave-particle duality, as the electron wave, upon injection from one end of the loop acquires a phase dependent on the magnetic flux permeating through the loop. Electrons traversing the loop in the opposite sense (opposite direction), interfere with the opposite chirality of electrons, leading to an oscillation in the resistance measured across the loop as the magnetic flux through the loop is varied [155]. The amplitude of oscillations increases as the

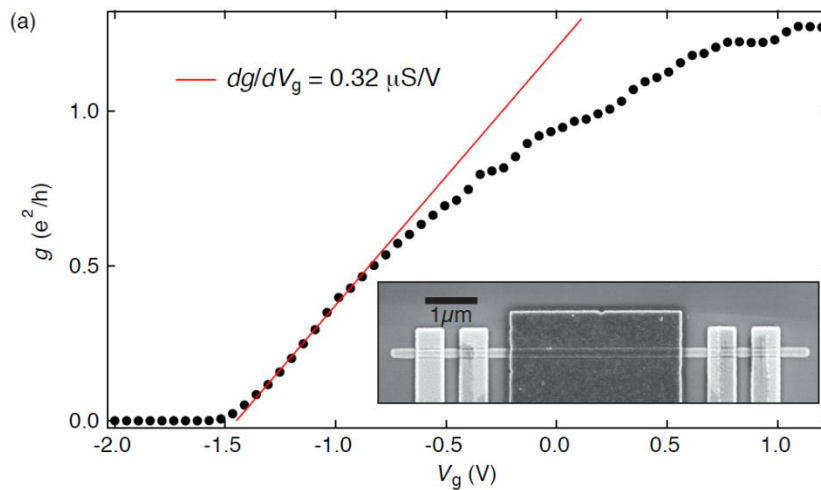
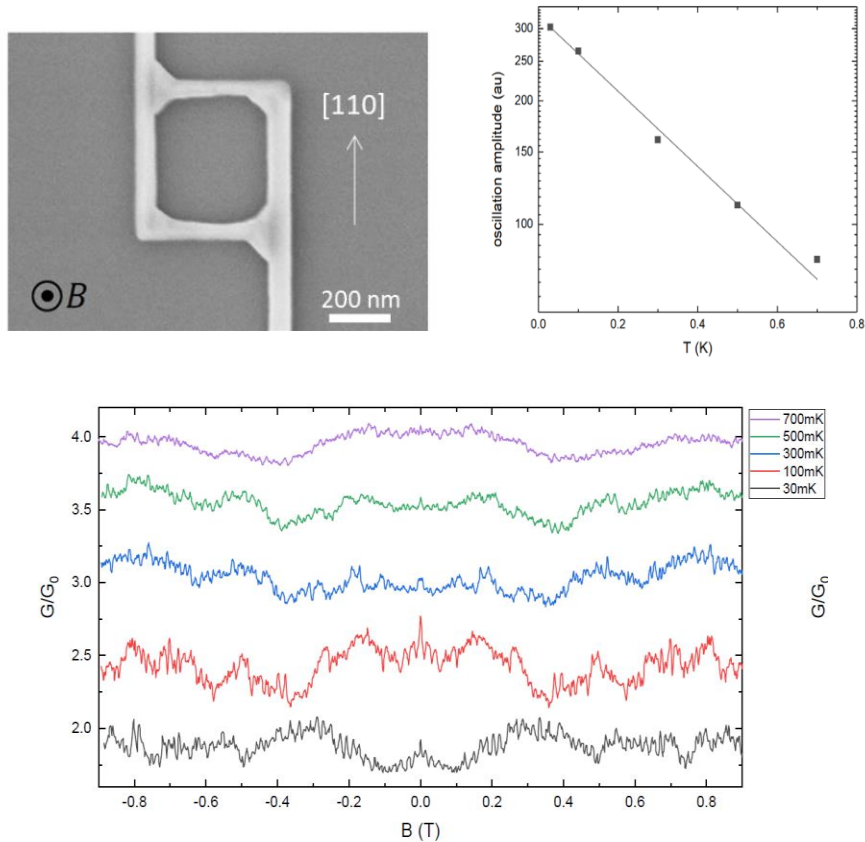


Figure 4.11 A four point measurement with a gate voltage, with the conductance change plotted vs. change in gate voltage. The plot shows complete pinchoff of the device as conductance goes to zero on increasing the gate voltage. Image courtesy – J.S. Lee, UCSB

temperature is lowered and this amplitude can be used to estimate the area of the loop and is correlated to the area as known from SEM imaging. The temperature dependence of oscillation amplitude can also be used to extract a phase coherence length of electrons at specific temperatures. These oscillations are absent of the electron channel has a short mean free path, comparable to the device length.



Expected AB period:

$$\Delta B = \frac{\Phi_0}{S} \approx 17 \text{ mT}$$

$$S \approx (0.48 \mu\text{m})^2$$

$$\text{fit : } a \exp(-b T)$$

$$\text{amplitude} \sim \exp(-l/l_{\varphi}(T)) \quad l_{\varphi} \sim T^{-1}$$

$$1 \text{ K : } l_{\varphi} = 500 \text{ nm}$$

$$50 \text{ mK : } l_{\varphi} = 10 \mu\text{m}$$

Figure 4.12 Starting from top-left, an Aharonov-Bohm loop with two ends used as source and drain contacts. Top-right, a plot of oscillation amplitude of the AB oscillations increasing with decreasing temperature, with a fit to extract the coherence length of electrons in the loop and gauge material quality. The bottom figure shows the AB oscillations in conductance at various temperatures vs. out-of-plane magnetic field. Image courtesy – J.S. Lee, UCSB

The measured data on InAs SAG channels indicates a loop area of $0.48 \mu\text{m}^2$ and a phase coherence length of $0.5 \mu\text{m}$ at 1 K and $10 \mu\text{m}$ at 50 mK has been extracted. The $10 \mu\text{m}$ coherence length indicates that the material quality is sufficient to see quantum transport phenomenon over large distances, which is especially relevant for MZMs separated by the length of the nanowire.

By probing the electrical density of states by tunneling electrons into the Al-InAs super-semi system, the presence or absence of zero-bias states can be detected. This technique, referred to as conductance spectroscopy or tunneling spectroscopy, maps the resistance/conductance of the device, with varying bias across the device. Conductance spectroscopy is a powerful tool to explore the local band structure of the device under test. A device structure to modulate the tunneling gate, effectively pinching off the semiconductor and setting up a potential barrier between the potentially topological nanowire and the ohmic contacts on either side is shown in Figure 4.13.

Additional gates (plunger) allow for tuning the electron density/Fermi level in the nanowire, independent of the tunnel gate. A map of conductance (dI/dV) in units of conductance quantum (e^2/h) is also shown below. The temperature is maintained constant at the base temperature of the dilution refrigerator at $\sim 50\text{mK}$. The conductance across the source drain contacts is plotted against changing Fermi level (V_B), using the plunger gate and source drain DC bias (V_{sd}) at zero magnetic field. The dark region showing zero conductance is symbolic of an induced superconducting gap in the semiconductor, indicating that unpaired electrons cannot tunnel into the superconductor. Twice the width of the dark region from zero energy, beyond which conductance suddenly jumps up to a finite value, is referred to as the

superconducting gap (2Δ). Being a particle-hole symmetric system, the superconducting gap is symmetric around zero energy – in essence enabling the definition of zero energy.

If one ramps up an in-plane magnetic field along the length of the nanowire such that the applied field 1) opens a Zeeman gap, 2) is perpendicular to the spin-orbit field, and 3) does not

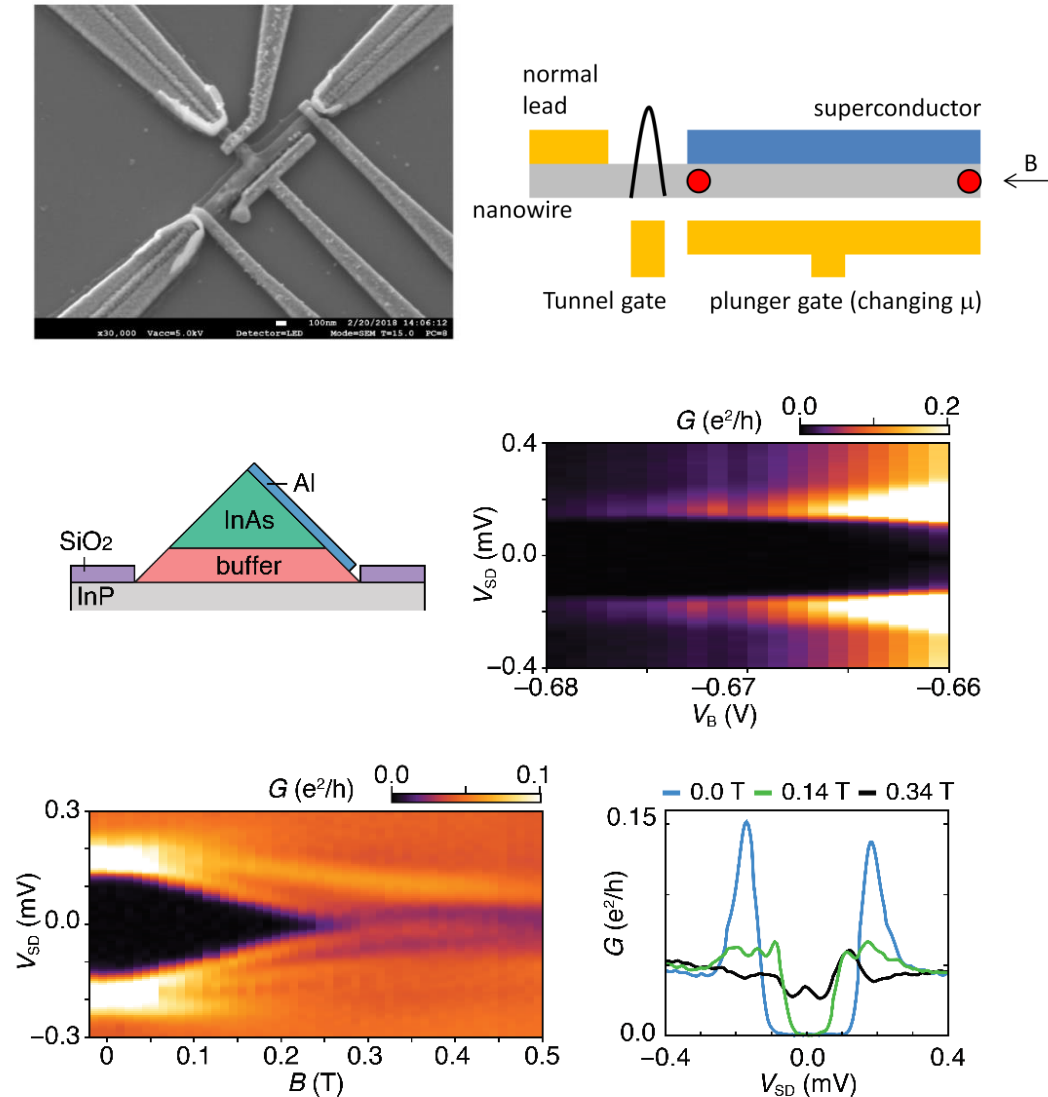


Figure 4.13 Clockwise from top-left: SEM image of a device with source drain contacts and multiple gates with an InAs-Al SAG nanowire. Top-right: Schematic of the device being probed. Center-right: Induced superconductivity in InAs nanowires, as function of variation in gate voltage. Bottom-right: Observation of a zero-bias peak in InAs with increase in in-plane magnetic field. Bottom-left: Conductance spectroscopy of the device showing ABS coalescing. Center-left: Cross section layer structure of the device being probed.

Image courtesy – J.S. Lee, UCSB

destroy superconductivity in the parent s-wave superconductor (aluminum), a closing of the induced superconducting gap will be observed.

Prior to complete closing of the induced gap, two sub-gap conductance states appear to coalesce. These states, referred to as Andreev Bound States (ABS) are bound to the edge of the superconducting gap at zero magnetic field and coalesce as in-plane magnetic field is increased. If the states coalesce and a quantized zero bias peak is observed, it would be a direct indication of a topological MZM, at zero energy of the induced gap. As the states do not coalesce ‘fully’ and do not stay together, but instead diverge, simulations [74] indicate these are trivial ABS (topologically trivial) and not Majorana Bound States (MBS) (topologically non-trivial). Yet, the observation of coalescing states is a key step for the realization of MBSs.

As of this writing, it is not clear what leads to MBS vs. ABS forming in various devices spread across various materials systems. While a preliminary theoretical understanding on differentiation between ABS and MBS does currently exist, an experimental litmus test akin to braiding the non-abelian MBS does not exist as of this writing, further complicating the subject.

4.5. Conclusion

Due to their ease of growth and fabrication, InAs quantum wells and nanowires are essential for the demonstration of topological phenomena like MZMs. Both have been explored thoroughly in this work. Firstly, near surface quantum wells of InAs with record high mobility have been demonstrated. Secondly, an understanding has been developed for the growth of InAs nanowires on patterned substrates with high selectivity. Using this understanding and taking advantage of the benefits of Chemical Beam Epitaxy (CBE), InAs nanowires coated

with aluminum have been selective area grown. These SAG devices are scalable and offer a great potential for wafer scale growth, fabrication and measurement. InAs-Al SAG nanowires measured also show a zero-bias peak while further work to establish presence of MZMs in InAs remains in progress.

5. Chapter 5 – InSb Quantum Wells (2D) and Wires (1D)

5.1. Introduction

InSb is the material of choice with the highest reported electron g-factor (-55 unstrained) in the binary III-V compound semiconductor family and a narrow band gap (0.24 eV at < 2K) [145]. This enhanced g-factor is significant for MZM systems due to potential for greatly enhanced induced topological gap as compared to InAs, for the same carrier mobility. Combined with a low electron effective mass ($\sim 0.013m_e$) [145] and thus inherently a high electron mobility ($\sim 700,000 \text{ cm}^2/\text{Vs}$ at 56K in 800 μm thick un-intentionally doped InSb substrate), InSb is a viable candidate for scalable platforms for next generation information processing.

InSb is promising in all platforms – 2DEGs, 1D VLS nanowires and 1D SAG in-plane nanowires. While bottom-up InSb VLS nanowire networks have recently been demonstrated

[81], lithographically defined wafer scale architectures based on quantum wells and selective area epitaxy will be necessary for the development of spintronics and quantum computing.

Because of its great potential for topological quantum computing, InSb will be the central focus of this chapter. While the growth of InSb (001) quantum wells has been extensively reported on GaAs substrates, the use of InSb substrates for a drastic reduction in lattice mismatch with the AlInSb buffer/barrier layers had not been reported, prior to this work and will be a part of the focus of this chapter. Perhaps most importantly, this work offers the first and only reported growth of InSb quantum wells on InSb substrates. This is a significant advancement in the field due to the observed improvement in electron quantum mobility in InSb quantum wells grown on InSb substrates.

Section 5.2 begins with a discussion of atomic hydrogen cleaning on InSb (001) surfaces. A fundamental impediment to the use of InSb substrates in the past has been the successful desorption of the native oxide on the surface of the substrate prior to commencement of epitaxial growth. Atomic hydrogen cleaning has been shown to aid in removal this oxide layer. Section 5.2 will also detail the first demonstration of regrowth of InSb on InSb, allowing for a plethora of opto-electronic devices.

Section 5.3 begins with an overview of the previously existing understanding of the MBE growth window of InSb (001), which was in part aided by RHEED reconstruction transitions on the surface of InSb [156]. It then discusses a common challenge in epitaxial growth of InSb and related compounds – the low decomposition temperature of InSb (often incorrectly referred to as low melting point). Section 5.3 addresses these challenges head-on, presenting a more refined perspective on the InSb growth window and indicating specific temperature

regions that lead to optimum growth, decomposition, and RHEED reconstruction transitions for InSb quantum wells. Lastly, Section 5.3 will discuss how the understanding thus developed can be ported to other MBE reactors by use of common pyrometry calibration techniques, during growth of InSb.

Section 5.4 focuses on the growth of InSb (001) quantum wells on GaSb and InSb substrates and reports low temperature magneto-transport data on the same. The section also discusses top and bottom gate control of electron density in InSb quantum wells and describes the first demonstration of bottom gate control in the InSb quantum well system, which was achieved as part of this work.

Section 5.5 focuses on InSb VLS nanowires for use in topological quantum computation, specifically emphasizing the growth of an epitaxial superconducting aluminum shell on nanowires grown by MOCVD (wires grown along the [111]B orientation). Results on induced superconductivity and observation of $2e$ charge periodicity in the superconductor, setting the stage for an eventual qubit readout, have been reported here. Lastly, the first ever observation of quantized Majorana conductance in InSb-Al nanowire systems has been described in detail. This quantized conductance at a value of $2e^2/\hbar$ is a direct manifestation of the Majorana property of the particle being its own anti-particle.

Section 5.6 focuses on in-plane InSb nanowires for topological quantum computation and describes state-of-the-art practices in InSb SAG on InP (111)B substrates. The section also provides a demonstration of induced superconductivity with an epitaxial aluminum shell.

Lastly, Section 5.7 focuses on a serendipitous discovery of transport phenomena suggestive of engineered superconductivity in an InSb/AlInSb heterostructure, at low

temperature, by rare earth doping. The absence of any previously known superconductor in this heterostructure, makes this result surprising.

5.2. Atomic hydrogen cleaning of InSb surfaces

5.2.1. Preparation of InSb substrates for MBE

While InSb substrates would be the default substrates for growth of InSb quantum wells, due to the nearly lattice matched growth of AlInSb buffer layers, InSb substrate also creates specific obstacles for the researcher. These obstacles have been extensive enough that the demonstration of InSb quantum wells on InSb substrates had remained elusive prior to this work. Specifically, thermal desorption of InSb substrates has been a challenge.

The incongruent sublimation of Sb and decomposition of InSb at temperatures in excess of $455\pm 5^\circ\text{C}$, under an antimony flux effectively leaving behind Indium droplets [157], which is a problem because it brings about an immediate and sudden end to further epitaxial growth. Furthermore, the melting point of InSb is known to be 527°C , but since InSb decomposes prior to that temperature in an MBE reactor, as mentioned above, the inability to thermally desorb the surface oxide is incorrectly attributed to this low melting point (to an untrained eye or an uncalibrated pyrometer, the decomposed InSb substrate with In droplets left behind, looks the same as a molten substrate).

Atomic hydrogen cleaning of InSb substrates has been explored by researchers in the past. Previous work has shown that in-situ atomic hydrogen cleaning could be used for low temperature desorption of the native oxide on III-V surfaces and could similarly be used for InSb substrates [158], [159]. Since the native oxide on the surface of InSb consists of

amorphous and separate oxides of In (In-O, In₂O₃) and Sb (Sb-O, Sb₂O₃, Sb₂O₅), atomic hydrogen can react directly with the oxides to release elemental Indium, Antimony and water vapor.

The following paragraph will detail the atomic hydrogen cleaning of InSb substrates. First, epi-ready double-side-polished 625 μm (2”) or 800 μm (3”) InSb substrates from Wafer Technology Ltd., with an unintentional n-type doping $<1 \times 10^{14}/\text{cm}^3$ and an etch pit density $< 20/\text{cm}^2$, were In bonded to Mo sample blocks prior to MBE growth¹⁴. Atomic hydrogen cleaning was performed in a sample preparation chamber with a base pressure of $<1 \times 10^{-10}$ Torr, which was interconnected via UHV transfer chamber to the MBE growth chamber. A 6N pure (Research Grade purity) hydrogen gas source was further purified with a getter (purchased from SAES Getters Inc.) to reduce O₂, H₂O, CO₂, CO, and other reactive gas contaminants and was injected through a leak valve into an MBE Komponenten manufactured Hydrogen Atomic Beam Source (HABS) operating at 1700°C and, pointing directly at the sample. During the hour-long atomic hydrogen cleaning, the chamber was held at a pressure of 5×10^{-6} Torr while the sample was continuously rotated at a thermocouple temperature of 380°C¹⁵. Post-cleaning, the sample was cooled and the remnant hydrogen gas from the chamber was pumped out ($<1 \times 10^{-8}$ Torr) before the sample was transferred to the MBE chamber.

¹⁴ InSb substrates should only be In bonded to Mo or W, if being heated above ~350°C. If Ga bonding is used, Ga reacts with the InSb substrate forming a strong bond making removal of an intact wafer from the growth block, post growth, near impossible.

As a rule of thumb, InAs, InP, InSb should be bonded with In on Mo or W blocks. GaAs, GaSb should be bonded with Ga on Ta or W sample blocks. W is the refractory material of choice for sample mounting as it doesn't react up to 1000°C with either In or Ga [212].

¹⁵ While temperature measurement in vacuum is known to be non-trivial, the error between thermocouple temperature and temperature of the sample surface, in this system, has been estimated to be about 150°C±50°C, deviating further (non-linearly) on increasing the substrate temperature.

Hydrogen cleaning at elevated temperatures allows for easier desorption of the water vapor formed on the sample surface, but it also increases the vapor pressure of otherwise non-volatile oxides of indium and antimony. Ideally, exposure to a group V (Sb) source, during hydrogen cleaning should allow for an increased temperature window for cleaning, while also leaving a smoother surface post cleaning. In the setup used, the combination of elevated temperature and the absence of a group V source preferentially lead to an Antimony poor and Indium rich surface. This indium rich surface was confirmed by Reflection High Energy

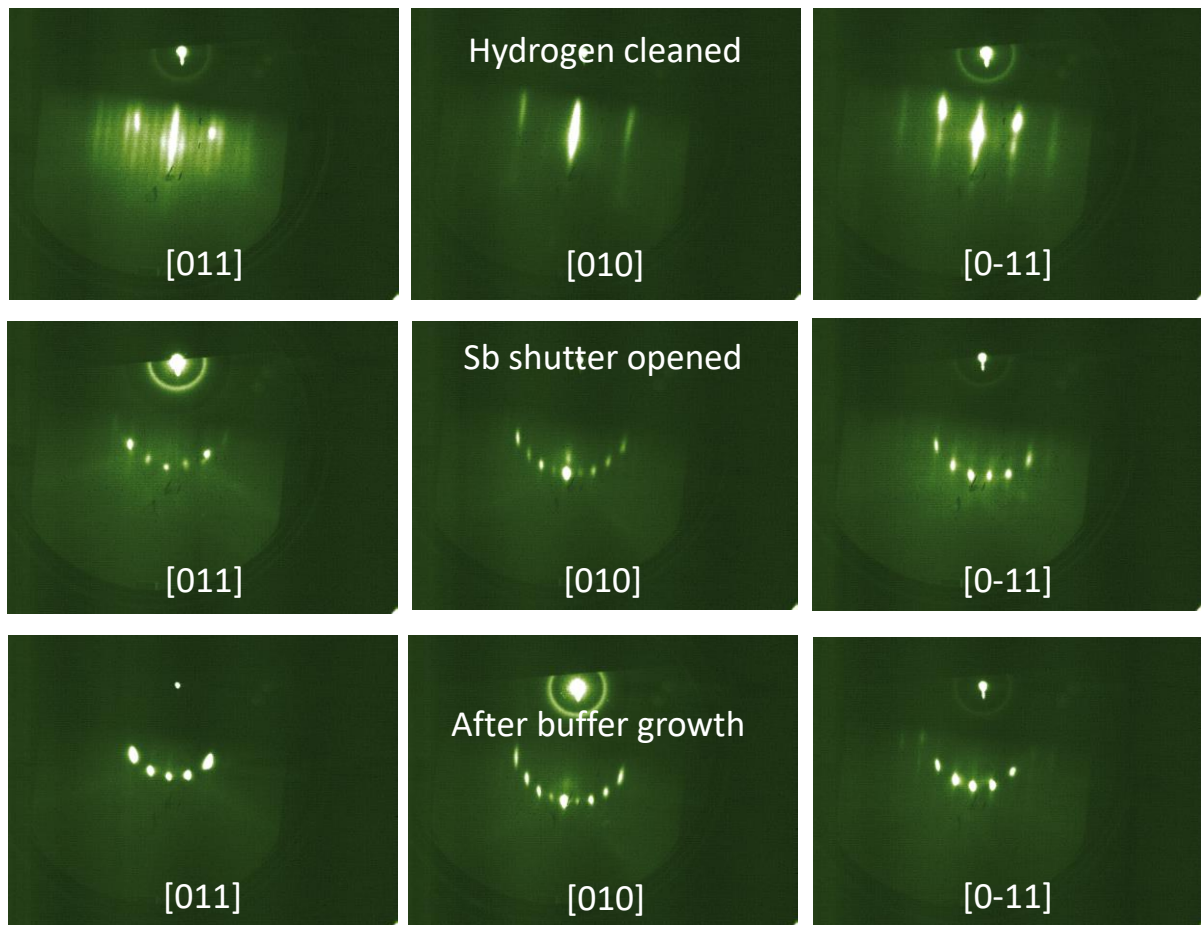


Figure 5.1 The top row shows the RHEED reconstruction observed immediately after hydrogen cleaning of an InSb substrate. It indicates a (4x2) Indium rich reconstruction. The center row shows the evolution of the reconstruction when the sample is exposed to an Sb flux at $\sim 300^\circ\text{C}$. A well known c(4x4) reconstruction of InSb is observed. The arc formed by Ewald's sphere cross-sectioning the fourier space, indicates a very smooth surface of InSb prior to any buffer growth. Such a surface is not evident in RHEED in materials where the oxide is desorbed thermally. The bottom row shows the evolution of the reconstruction after the growth of a buffer layer. The c(4x4) reconstruction has been sharper indicating improvement in surface morphology as compared to the RHEED prior to buffer growth.

Electron Diffraction in the MBE chamber when the sample surface showed a $(4 \times 2)/c(8 \times 2)$ indium rich reconstruction (see Figure 5.1) and also by in-situ scanning tunneling microscopy (STM).

There are a few caveats to the atomic hydrogen cleaning process. Firstly, because exceeding the temperature window could lead to indium droplet formation on the *already* indium-rich surface, accurate determination of the sample temperature, which is specific to each individual setup, is greatly beneficial. Secondly, continuous rotation of the sample during cleaning is also necessary for successful atomic hydrogen cleaning, as it ensures direct exposure of the complete sample surface to the atomic hydrogen beam. It also facilitates a uniform temperature across the sample surface, which is necessitated by the tight desorption-limited temperature window and by the extreme radiative heating from the high temperature filament of the hydrogen atomic source in proximity with the substrate.

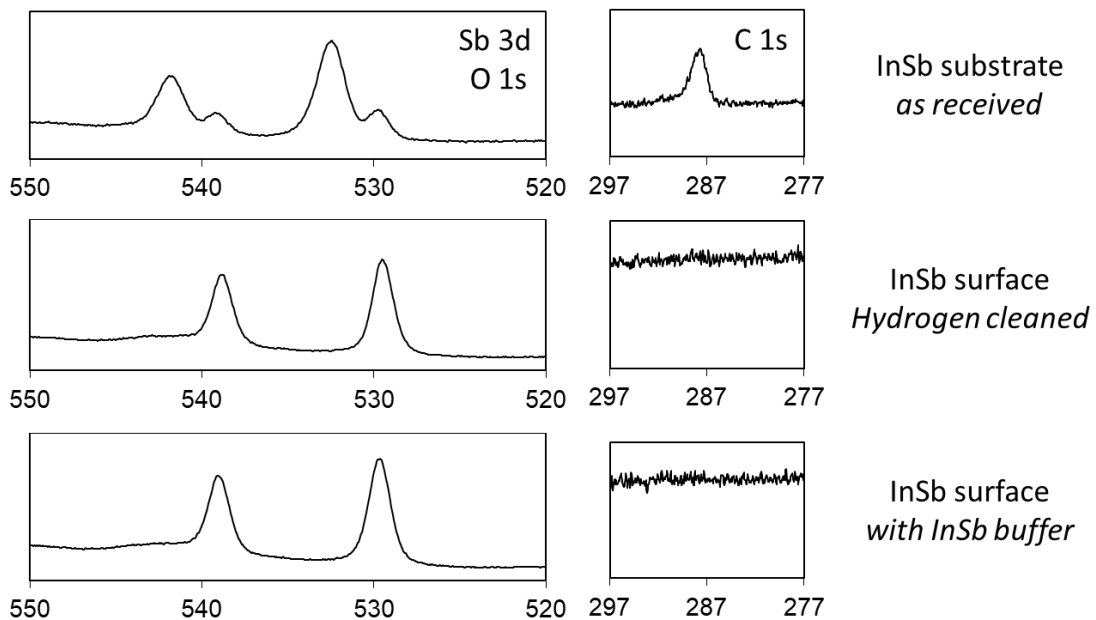


Figure 5.2 XPS scans showing the Sb 3d, O 1s and C 1s peaks on as received InSb substrates, on hydrogen cleaned InSb substrates and after growth of InSb buffer on an InSb substrate after hydrogen cleaning. Carbon and oxygen reduce to below the detection limit on hydrogen cleaning and the XPS spectra look identical to the XPS spectra from after growth of an InSb buffer indicate successful atomic hydrogen cleaning of the the sample surface.

Also, while the sample temperature is estimated to be $150^{\circ}\text{C}\pm 50^{\circ}\text{C}$ less than the measured temperature of 380°C , a more precise determination using a pyrometer, taking into account radiative heating from the atomic hydrogen source operating at 1700°C , would be necessary to define accurate bounds of the temperature window for successful atomic hydrogen cleaning. Experimentally, it was observed that the temperature window for atomic hydrogen cleaning of InSb substrates less than 40°C , as samples outside of the $380^{\circ}\text{C}\pm 20^{\circ}\text{C}$ seldom looked acceptable in RHEED. The time window for H cleaning at 380°C was varied from 20 minutes for VLS InSb nanowires to 1 hour and 20 minutes for (001) InSb substrates, with best results in the 30 minutes to 1 hour range (30 minutes for nanowires, 45 minutes for selective area grown films, 1 hour for (001) wafers).

After atomic hydrogen cleaning was performed, the sample surface was analyzed by *in-vacuo* (UHV inter-connected) X-Ray Photoelectron Spectroscopy (XPS) with an aluminum K-alpha anode and a Surface Science Labs hemispherical analyzer to confirm complete desorption of the surface oxides. Evidence of the success of the oxide removal from the surface of InSb was clear: an as received InSb substrate showed a strong presence of carbon (C 1s) and antimony oxides and oxygen (Sb 3d, O1s). Post-hydrogen cleaning, on the other hand, the carbon and oxygen were undetectable and below the noise threshold, and the Sb 3d peaks showed no indication of partial oxidation. The spectra were also compared with a 500nm thick InSb buffer grown on an InSb substrate, which was expected to have buried any desorption related oxides and which was found to look identical to the post-hydrogen cleaned surface. This indicated a successful atomic hydrogen cleaning.

5.2.2. Regrowth of InSb on InSb

In combination with atomic hydrogen cleaning and development of a novel wet-etch recipe for restoration of surface quality post nanofabrication, regrowth of InSb on InSb has been demonstrated.

To realize complex opto-electronic structures for demonstration of new phenomena, parts of the hetero-structure may require conformal growth post nanofabrication. This has been shown to be a handy tool in the development of regrown source-drain contacts in InAs/InP-based high speed transistors [160]. The demonstration of regrowth on InSb was lacking prior to this work due to the challenges involved in restoration of the sample surface post-fabrication, and the consequent requirement for successful atomic hydrogen cleaning, prior to regrowth.

In this section an epilayer of undoped or intrinsic InSb (i-InSb) is first growth on n-InSb. The goal is to make in-plane nanowires of i-InSb which as encapsulated by n-InSb in all three dimensions.

After the nanofabrication of required structures (see Figure 5.3) by Reactive Ion Etching (RIE), a significant amount of amorphous debris is observed in Scanning Electron Microscopy (SEM). Epitaxial growth on amorphous or a very rough surface is not feasible. Additionally, electrical and optical properties of the device are significantly hampered by electrical shunt paths from sidewalls and by absorption losses from such surfaces.

To restore the surface roughness and uncover the underlying crystalline layers, ex-situ wet etch consisting of alternating etches in 1:10 HF:H₂O and 1:10 HNO₃:H₂O was performed. While a combination of HF:HNO₃ is known to etch almost all metals and semiconductors [161], it is also a preferred etch for etch pit dislocation density tests and chemical mechanical polishing of InSb surfaces [162]. The HF in this wet-etch process can also be replaced with HCl to get the same results, as HF and HCl both act as acids that specifically remove oxidized layers. Once the top few layers of the material which were oxidized by either air or the oxidizer (e.g. HNO₃ or H₂O₂) the etch rate through un-oxidized layers is many orders of magnitude slower, making an exposure to just the dilute acid a relatively self-limiting etchant of just the native oxide or otherwise intentionally oxidized layers. Often, a quick dip in a dilute acid is the suggested step prior to various metal evaporations in III-V semiconductor processing, as the dilute acid is expected to remove the native oxide layer formed [163].

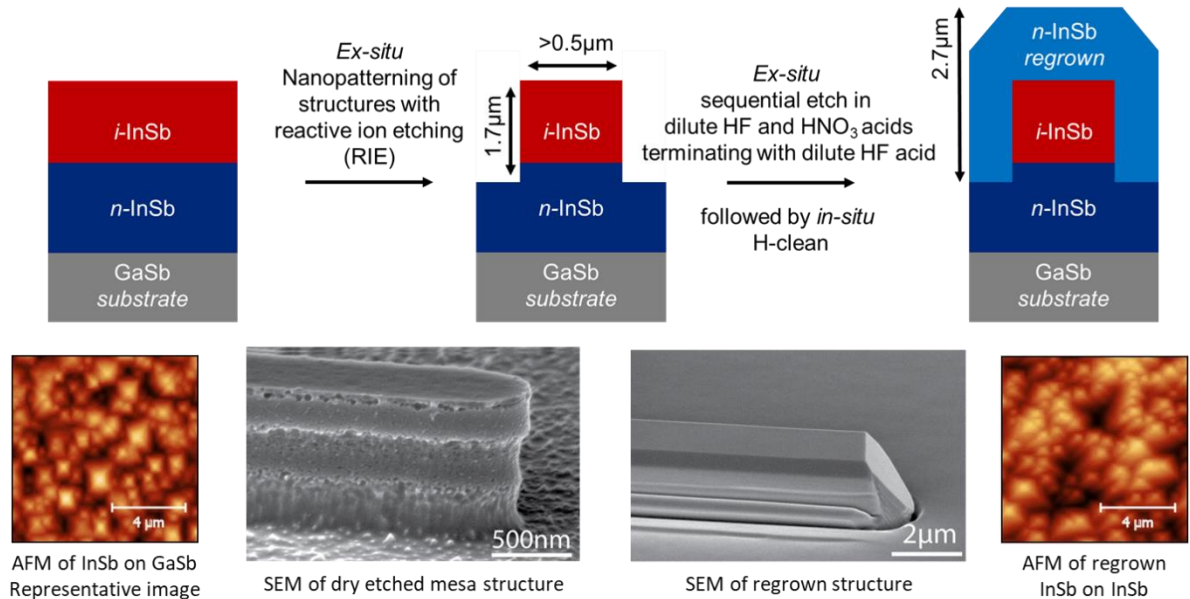


Figure 5.3 Start from left, the layer structure of the sample as grown in the first MBE run with a representative AFM image of the surface. After ex-situ patterning, the SEM of the dry-etched mesa structure shows extremely rough surfaces. Structures as high as few microns were etched leaving behind an amorphous debris. After cleaning with HF and HNO₃ in alternating steps, followed by hydrogen cleaning, the sample is loaded back in the MBE for regrowth. The regrown surface looks smooth and regrowth is evident on all facets. The AFM image of the surface resembles the AFM of a generic InSb film on GaSb, indicating first demonstrated successful regrowth of InSb on InSb, post device fabrication. SEM image courtesy – P.P. Iyer, UCSB.

HNO_3 (nitric acid) on the other hand is primarily a strong oxidizer. While working with a HNO_3 rapid oxidation is expected, non-porous surfaces of metals and semiconductors often exhibit self-limiting oxidation. In this case, working with dilute HNO_3 further reduces the oxidation rate and depth. Now, in preparation for regrowth, the top few layers of the semiconductor (post-fabrication) are peeled off by sequential exposure to a dilute acid followed by a dilute oxidizer. By separating the acid and oxidizer combination, into two separate self-limiting processes of oxidation and oxide removal, a layer by layer etch has been created. This novel etch developed as part of this work, significantly aids in removal of amorphous debris and restoration of underlying step terraces. Applications of this etch technique on other semiconductors remain to be explored.

After ten cycles of alternately dipping in HF and HNO_3 , the sample was rinsed in water, dried, and immediately mounted for MBE growth, to avoid the formation of a thick native oxide. The sample was then introduced in the MBE preparation chamber for atomic hydrogen cleaning of the surface. By design, in this test sample, all exposed surfaces are InSb (see Figure 5.3). It must be noted that atomic hydrogen cleaning is not expected to work with exposed surfaces containing aluminum, though arsenides, antimonides, phosphides of indium and gallium are expected to be compatible with this process due to the relatively higher vapor pressure of their constituent oxides.

Lastly, atomic hydrogen cleaning was performed as has been described in Section 5.2, and the sample was moved into the MBE chamber via interconnected UHV transfer chambers. Using pyrometer emissivity calibrations from other InSb samples, an unintentionally doped InSb layer was grown on the sample. RHEED imaging was severely hindered by the $>1\mu\text{m}$ -thick ridges etched onto the sample surface. Post-growth AFM and SEM analysis conformed

epitaxial growth and complete restoration of the sample surface, similar to the original sample surface, indicating successful regrowth.

5.3. InSb Surface Stability and Reconstruction Phase

Diagram

As was mentioned in Section 5.2, on atomic hydrogen cleaned InSb (001) substrates, an indium-rich $(4 \times 2)/c(8 \times 2)$ reconstruction was observed in RHEED. Once the sample was heated to above 300°C in the MBE chamber (as measured by a pyrometer), it was exposed to a dominantly Sb_2 flux, which led to an instant transition to a $c(4 \times 4)$ Sb-rich reconstruction of InSb. The sample was then further heated under an Sb_2 overpressure, and the transition from $c(4 \times 4)$ to $a(1 \times 3)$ (asymmetric (1×3) or pseudo (1×3) reconstruction) was used to calibrate the pyrometer to 387°C ¹⁶ [156]. It was determined that, based on the available Sb_2 flux, the upper limit of the MBE growth window of InSb was limited to $455 \pm 5^\circ\text{C}$, for a Sb stabilized surface, during growth. This upper-limit temperature can be referred to as the decomposition temperature. Upon exceeding this upper limit temperature of $455 \pm 5^\circ\text{C}$, the sample showed irreversible indium droplet formation in RHEED and a visually hazy surface.

The lower limit of the growth window was established to be $300 \pm 10^\circ\text{C}$ for the same Sb_2 flux. Upon growing samples at substrate temperatures lower than $300 \pm 10^\circ\text{C}$, a rough (1×1)

¹⁶ Since the calibration at 387°C is based on a RHEED reconstruction transition, it is sensitive to temperature and Sb flux uniformity across the sample and is also extremely sensitive to the rate of change of sample temperature and hence for calibration purposes a rate of change of $2\text{-}5^\circ\text{C}/\text{min}$ was found to be most reproducible. Faster rate of temperature change lead to an increased error in calibration and reduced the reproducibility which was judged by repeating the calibration. The error in calibration, under reasonable conditions, is estimated to be about $\pm 5^\circ\text{C}$ or less.

3D RHEED reconstruction was observed, with increasing intensity of 3D spots on continued growth. This roughness was irreversible in cases of prolonged or lower temperature growth.

While this growth window of $300\pm 10^\circ\text{C}$ to $455\pm 5^\circ\text{C}$ was strictly for the Sb_2 flux available in the Palmstrom Lab's III-V MBE system, it is expected to shift to lower temperatures with the use of Sb_4 or reduced Sb_2 flux and to higher temperatures with the use of an increased Sb_2 flux. The original temperature calibration at $387\pm 5^\circ\text{C}$ was still found to be relevant and accurate but with a relative absolute error.

Upon probing the temperature stability of the $c(4\times 4)$ to $a(1\times 3)$ transition as Sb_2 flux was reduced from $\sim 5\times 10^{-6}$ Torr to $\sim 5\times 10^{-8}$ Torr, a sharp drop in the transition temperature from the previously calibrated value of $387\pm 5^\circ\text{C}$ was observed. This drop was apparent only when the flux was lowered by more than an order of magnitude (i.e. below $\sim 5\times 10^{-7}$ Torr). After reducing the flux to $\sim 5\times 10^{-8}$ Torr, deviation from the previously calibrated value of $387\pm 5^\circ\text{C}$ further increased to $\sim 30\pm 5^\circ\text{C}$. Thus, while the $387\pm 5^\circ\text{C}$ calibration is not independent of Group V flux, it is robustly reproducible for day-to-day processes of MBE growth of InSb as the Group V flux from a valve cracker cell is relatively constant for majority of the growth campaign until just before the effusion cell runs dry.

RHEED intensity oscillations were observed between $300\text{-}350^\circ\text{C}$. The oscillation amplitude was dependent on growth rate and temperature, as has been reported previously [164], with the optimum temperature being $\sim 325^\circ\text{C}$ and extremely high growth rates of up to $2\mu\text{m}$ per hour of InSb. No oscillations were observed ever above $\sim 390^\circ\text{C}$ indicating a transition from layer-by-layer growth mode to step flow growth mode at that temperature.

Step-flow growth mode is of special interest for growth of quantum wells, while layer-by-layer growth mode was used for growing very highly doped structures for photonic metamaterials.

A summary of all the above observations was used to construct the InSb surface stability and reconstruction phase diagram as shown in Figure 5.4.

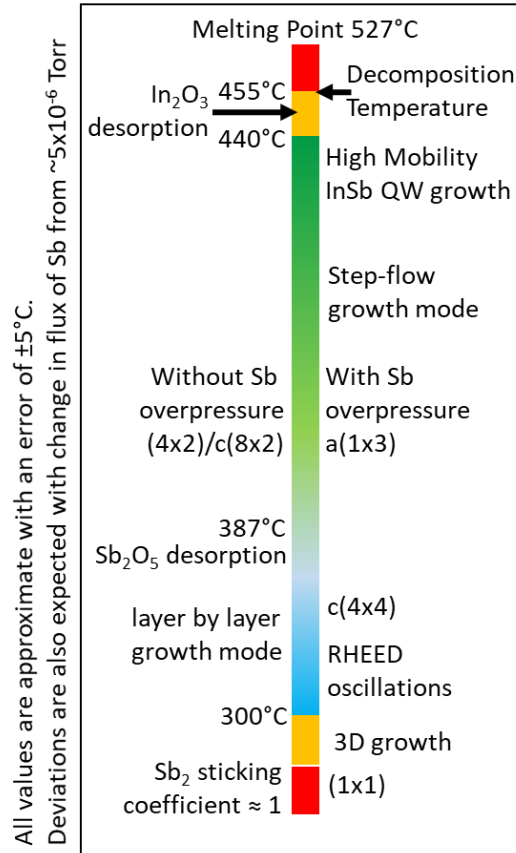


Figure 5.4 Surface stability and reconstruction phase diagram of InSb (001) with various reconstruction and growth windows identified.

Because growth of high mobility quantum wells – one of the primary goals of Section 5.4 – requires the smoothest possible surface, the step-flow growth mode is necessary, with sample surface temperatures as close to decomposition as possible. Indeed previous record mobility InSb quantum wells have reported growth solely in the $450 \pm 5^\circ\text{C}$ range [165]–[167]. Aiding in growth of high mobility, low impurity films of InSb, the added benefits of elevated temperature are: a) Reduced sticking coefficient of impurities inherent to the MBE chamber,

as has been demonstrated by the growth of GaAs ultra high mobility quantum wells [168], ii) Reduced incorporation of Sb leads to a stoichiometric growth of InSb as the vapor pressure of Sb is much higher at 450°C than at temperatures below 400°C.

5.4. InSb Quantum Wells

5.4.1. Heterostructure design

Having established all the conditions necessary for growth of InSb in Section 5.3, the discussion will now move on to the growth of InSb quantum wells on GaSb (001) and InSb (001) substrates.

Electron Hall mobility in InSb quantum wells has been shown to be limited by a high density of threading dislocations and by micro-twins [169], [170], and it has remained saturated at $4 \times 10^5 \text{ cm}^2/\text{Vs}$ [165]–[167]. Recent work by C.J. McIndo, et al., has incorporated optically determined surface roughness into an improved model for determining the factors limiting electron mobility at low temperatures [171], [172]. According to this work, an improvement in electron mobility can be achieved in the InSb 2DEGs by a reduction in extended defects underlying the quantum wells, i.e. by focusing on layers below the quantum well rather than the quantum well itself or the layers above it.

In this work, InSb quantum wells with $\text{Al}_x\text{In}_{1-x}\text{Sb}$ barriers have been grown by molecular beam epitaxy on GaSb (001) and InSb (001) substrates. While growth on GaSb substrates had not been reported until recently [167], this work remains the first and only reported growth of InSb quantum wells on InSb substrates. While previous reports have heavily focused on GaAs (001) substrates [153], [165], the impact of reduced lattice mismatch offered by GaSb and InSb

substrates, on electron mobility and gate tunability, remained to be explored. While GaSb substrates offer a reduced lattice mismatch in comparison to GaAs and open the possibility for a step graded buffer scheme to reduce the effective dislocation density that influences the active quantum well region, InSb substrates offer a paradigm shift by enabling the possibility of growth of low dislocation density pseudomorphic $\text{Al}_x\text{In}_{1-x}\text{Sb}$ buffer layers.

For quantum well heterostructure growth, samples were loaded into a modified VG V80H III-V MBE equipped with an Applied EPI Arsenic valved cracker and a Veeco Mark IV antimony valved cracker. A cold lipped Veeco SUMO effusion cell with a pBN crucible was used for aluminum evaporation while hot lip e-Science TITAN effusion cells with graphite crucibles were used for gallium and indium evaporation. RHEED images were taken at a potential of 15kV with a STAIB electron gun. Silicon dopant source was evaporated from a high purity silicon wafer from a pBN crucible while tellurium was evaporated as an outcome of preferential incongruent sublimation of gallium telluride (GaTe). The system was equipped with a LumaSense IMPAC IGA 6/23 Advanced pyrometer sensitive to 2.0 to 2.6 μm wavelength range as has been described in Appendix B. GaSb substrates were gallium bonded to tantalum or tungsten sample blocks, while InSb substrates were indium bonded to molybdenum blocks.

On undoped GaSb substrates, the etch pit dislocation density was $<2000/\text{cm}^2$, while the p-type background dopant concentration was $<5 \times 10^{16}/\text{cm}^3$ at 300K. Upon cooling below 50K, the measured resistivity increased to above 1×10^{10} ohm.cm which provided an insulating platform for the measurement of pure 2D transport through the epi-layers. Electrically conducting tellurium-doped GaSb substrates (GaSb:Te), were metallic at all temperatures and had an intentional n-type carrier concentration of $1-9 \times 10^{17}/\text{cm}^3$ and a comparatively low etch

pit dislocation density of $<1000 /\text{cm}^2$. The native oxide on the surface of GaSb substrates was thermally desorbed under an antimony (Sb_2) overpressure in the MBE chamber, and the pyrometer was calibrated to 540°C at oxide desorption, based on transition from a diffused glow (amorphous oxide) to a sharp 3D RHEED pattern (single crystal diffraction). The sample was then cooled to 480°C under Sb_2 overpressure before a ~ 100 nm thick GaSb buffer layer was grown. Post-buffer growth RHEED patterns showed a smooth surface with a characteristic $(1 \times 3)/c(2 \times 6)$ reconstruction of GaSb as has been previously reported [149], [173].

On conducting GaSb:Te substrates, a layer of $\text{Al}_{1-x}\text{Ga}_x\text{As}_{1-y}\text{Sb}_y$ lattice matched to GaSb substrate layer was grown, as reported by B. Shojaei, et al., [149] for electrical isolation of electrical transport in epi-layers from the conducting substrate. This layer also served additionally as a gate dielectric for bottom gating of the electron density in the InSb QW using the conducting substrate as a global back gate. A thin layer of GaSb, or in some cases a thin AlSb/GaSb superlattice, was grown before the abrupt transition from the 6.1 \AA family of GaSb/AlSb to the 6.4 \AA lattice constant of AlInSb/GaInSb.

While electron mobility in GaAs and InAs 2DEGs has improved with a better understanding of limiting scattering mechanisms [131], [149], [174], [175] electron mobility in InSb 2DES has been limited to $400,000 \text{ cm}^2/\text{Vs}$. A study of dominant scattering mechanisms limiting the mobility in InSb 2DES has confirmed that lattice mismatched growth of AlInSb/InSb layers and issues arising thereof are the primary limiters. Lattice mismatched growth, upon relaxation, leads to dislocations. These dislocations act as charge background impurities in the quantum well channel, lead to increased surface and interfacial roughness and act as remote ionized impurities, imaging charges onto the quantum well. As such, it is clear

that the potential choice of materials sandwiching the InSb 2DEG layer limits in many ways the electrical properties of InSb quantum well material system.

While still requiring extensive study, InSb channel thicknesses of 15nm or more are desirable to avoid significant penetration of the probability distribution of the electron wavefunction into the adjacent barrier layers. Peak reported mobility in the InSb 2DES has been reported for quantum well thicknesses of 25 to 30 nm [165], [166], [153], and hence 25 to 40 nm thicknesses were chosen for this study.

Regardless of the substrate used, a large conduction band discontinuity is desirable between the quantum well channel and the electrically insulating barrier layers sandwiching it. $\text{Al}_x\text{In}_{1-x}\text{Sb}$ is one of the few and best studied material for these purposes. Limiting the thickness of the InSb layer to 40nm or less determines the maximum allowed aluminum composition (primarily in the buffer layer) so that the critical thickness of InSb quantum well layer is not exceeded during quantum well growth. Additionally, care must be taken not to exceed the critical thicknesses so as not to nucleate new dislocations at the InSb/AlInSb upper and lower interfaces of the quantum well. The above puts the maximum allowed Al composition in AlInSb. Using Matthews-Blakeslee's critical thickness approximation [176], [177], for a 15nm thick InSb QW to remain strained on the AlInSb barrier, the aluminum composition in AlInSb must not exceed 39%, with the estimated conduction band mismatch being 0.46eV at 300K and increasing further at measurement temperatures of $<2\text{K}$ [101]. Upon increasing the quantum well thickness to 25, 30, and 40nm, the aluminum composition rapidly drops to 24%, 20%, and 15%, respectively, with corresponding conduction band discontinuities also dropping to 0.273eV, 0.225eV, 0.167eV, respectively, at 300K [101]. $\text{Al}_{0.24}\text{InSb}$ is hence a

widely used compromise, as it allows for pseudomorphic growth of the quantum well yet but also provides the highest allowable conduction band mismatch for thin quantum wells.

To circumvent the above requirement of low aluminum content layers a heterostructure consisting of higher aluminum content layers immediately abutting the quantum well could be grown while keeping the aluminum composition very low in majority of the layer structure. Such a structure would be greatly beneficial for growth on the InSb substrate. A common impediment in the growth of such a structure by MBE is the requirement for sudden change in aluminum flux. This sudden change in flux can be achieved by either employing a second effusion cell of aluminum in the MBE chamber or by digital-alloying [178].

However, while an increased aluminum composition does have its benefits, it was observed in GaAs quantum wells that increasing aluminum composition in the vicinity of the quantum well increases surface roughness, leading to rougher interfaces and consequently lower mobility. For GaAs, the crossover from improved characteristics to lower mobility occurred at a composition of roughly 30% aluminum, depending on the heterostructure, and was primarily determined by the limiting growth temperature of 630-650°C, which is not sufficiently hot for the growth of smooth high aluminum content layers. In the highest mobility GaAs structures, significantly reducing the aluminum composition to range of 17% to 24% in layers immediately abutting the GaAs quantum wells has proven to be most successful [174]. For InSb, there is no existing estimation of when the crossover from improved characteristics to poorer mobility would be. However, the crossover point is expected to be strongly dependent on 1) 455°C growth temperature of InSb quantum wells and 2) the conduction band discontinuity that leads to the most optimum penetration of probability distribution of the electron wavefunction in the AlInSb cladding layers.

Impact of lattice strain must also be considered when growing InSb quantum wells as a key phenomenon that is intrinsic to the lattice mismatched growth of InSb on AlInSb is the compressive strain (all compositions of AlInSb have a smaller lattice constant than InSb and hence all InSb quantum wells with AlInSb barriers are inherently compressively strained).

Compressive strain is expected to increase the effective in-plane mass of the channel, reduce its in-plane g-factor (make it isotropic due to induced tetragonal distortion), and essentially compromise the key features that were originally the highlight of the material system. Tensile strain, on the other hand, is expected to reverse the above effects and make such an (001) oriented zinc-blende crystal more favorable for in-plane electron transport, specifically for applications relating to low effective mass and high g-factor [179]. It must also be noted that AlGaAs tensile strains the GaAs quantum well, and so does growth of InAs on GaSb or AlSb. InAs quantum wells grown on InP substrates with InGaAs/InAlAs cladding layers are the exception and are negatively impacted similar to the InSb/AlInSb/GaInSb system.

To avail the benefits of tensile strain, a novel and highly complex but rewarding approach would be to replace the InSb quantum well with an InAsSb quantum well on an AlInSb buffer (studied in detail in Chapter 6). The As/Sb ratio chosen for such an InAsSb quantum well should allow for tensile straining of the InAsSb layer, allowing for enhancement of the intrinsic properties, i.e. further reduction in effective mass and enhancement of in-plane g-factor.

With the impact of strain still in mind, the above discussion on the choice of optimum aluminum composition in the buffer and cladding layers for InSb quantum wells must now be revisited. The inference is that a higher aluminum composition leads to increased compressive

strain and is extremely detrimental to the intrinsic properties of the quantum well (i.e. detrimental to the properties that made InSb interesting, to begin with) therefore the desirable composition should consist of just enough aluminum to provide suitable electron confinement and allowing pure 2D transport (i.e. no parallel conduction path through the AlInSb layer). This conclusion is in contrast to the naïve conclusion drawn from the understanding of quantum well growth from the GaAs/AlGaAs and InAs/AlSb perspective and is one of the key challenges to growth of ultra high mobility InSb quantum wells.

Due to the underlying AlInSb barrier and buffer layers, all InSb/AlInSb quantum wells are hence compressively strained in-plane. Free-standing VLS InSb nanowires, however, do not suffer from this fundamental limitation, and the theoretically predicted electron g-factor of -55 has been observed in them [179], [180]. Meanwhile, the in-plane g-factor in InSb/AlInSb quantum wells was measured to be as low as -22 with a significant anisotropy in the in-plane and out-of-plane g-factor (-55) on a compressively strained InSb/AlInSb quantum well [181]. The g-factor enhancement is still appreciable in moving from InAs to InSb. However, for applications requiring the highest of g-factors InAsSb may be the more suitable choice (see Chapter 6 for more details).

5.4.2. MBE growth

Having discussed the composition of the AlInSb layers cladding the quantum well, we now move onto the MBE growth of the quantum well structure. In this work, when growing an InSb quantum well, thick buffer layers preceding the electrically active quantum well region nominally consisted of typically 1-4 μm AlInSb grown at about $445\pm 10^\circ\text{C}$. A superlattice of AlInSb/InSb or GaInSb/AlInSb was also incorporated in some structures. As a prelude to quantum well growth, typically a 50 to 150nm thick $\text{Al}_{0.1}\text{InSb}$ layer was typically grown, followed by the sample being briefly cooled to $350\pm 30^\circ\text{C}$ for the lower silicon/tellurium delta doping layer. The AlInSb spacer layers that sandwiched the InSb quantum well were again grown at $445\pm 10^\circ\text{C}$ as was the quantum well. In some quantum well growths, the sample was briefly cooled from $445\pm 10^\circ\text{C}$ to $350\pm 30^\circ\text{C}$ prior to the growth of the upper delta doping layer and the top barrier/cap layers were then grown at elevated temperatures. A typical layer structure for growth of InSb quantum wells on GaSb substrates is shown in Figure 5.5 with the desired temperature variations.

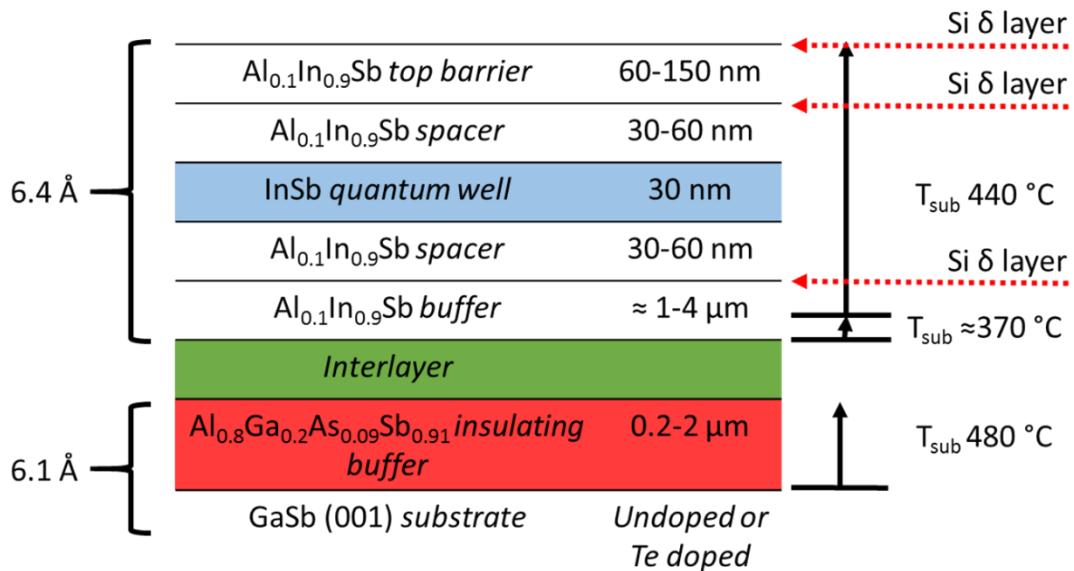


Figure 5.5 Layer structure and respective growth temperatures of layers during the growth of InSb QW on GaSb substrate

The concept of using low temperature for doping layers and high temperature for capping layers, adheres closely to the well-studied low temperature doping process used in high mobility GaAs quantum wells [174]. In contrast, some previous works reporting high mobility InSb quantum wells instead chose to grow the dopants and all layers above, including the quantum well at the cooler temperature used for doping to prohibit the dopants from the riding on the growth surface. This compromise may have negatively affected the peak mobility and electron scattering [166]. While this approach was successful, further improvements in the InSb quantum well layer quality could in principle be achieved by growing the quantum well at the elevated temperature, as discussed above, with dopant riding inhibited. On a separate note, background impurities incorporated in the quantum well due to vacuum quality in the MBE reactor were expected to be of very little consequence due to a chamber pressure of $<5 \times 10^{-11}$ Torr during quantum well layer growth.

5.4.3. Characterization of MBE grown films

We now move onto analyzing the quantum well growth. On GaSb substrates, the RHEED pattern changed from streaky to spotty for all abrupt transitions from $\sim 6.1 \text{ \AA}$ to $\sim 6.4 \text{ \AA}$. While growth temperature was optimized to minimize the 3D RHEED, it was inferred from the surface roughening, indicated by the spotty RHEED that the dislocations that

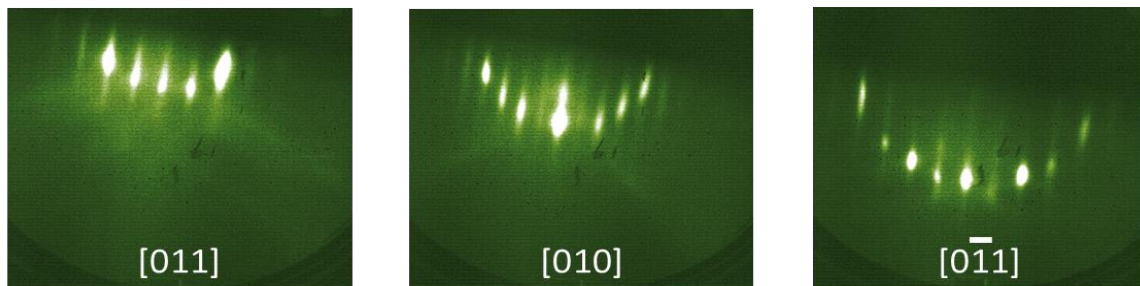


Figure 5.6 c(4x4) RHEED reconstruction of a thin layer of InSb terminating InSb QW grown on GaSb substrate.

predominantly impact and limit electron mobility in InSb quantum wells were nucleated at the transition from 6.1Å to 6.4Å lattice constant.

On InSb substrates, a similar issue was encountered on nucleating an AlInSb layer and transitioning from 6.479Å to 6.4Å (approximately, depending on composition of AlInSb), once the critical thickness of AlInSb on InSb was exceeded. It is safe to assume that the electrical properties of InSb 2DEGs are predominantly determined by this lattice mismatched interface and by the dislocations nucleated at this interface as they image charges leading to scattering in the well and also propagate up towards the well, leading to further scattering of electrons in the well. Regardless of the growth substrate, the InSb quantum well structure is often capped with a thin layer of InSb. This layer is terminated with a c(4x4) reconstruction at the end of the growth and is a RHEED image of the same is shown in Figure 5.6.

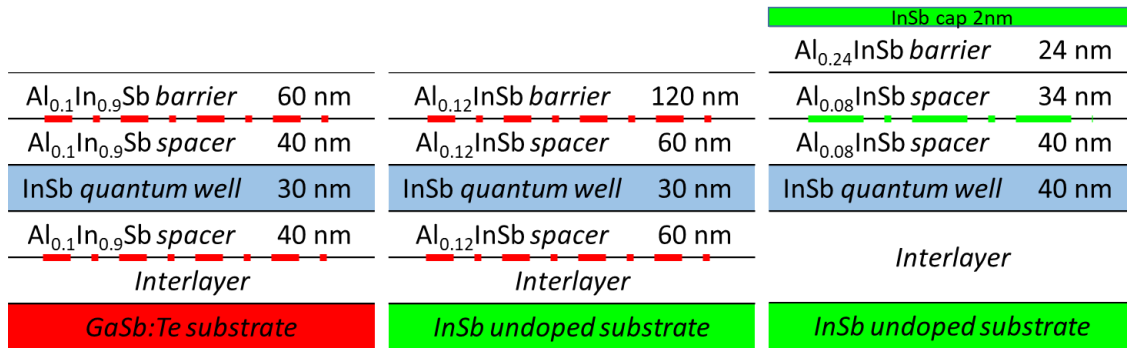


Figure 5.7 The layer structures of three InSb QWs which are compared further below. Left most of GaSb, center of InSb with a nominally 12% Al content buffer layer and the right of a nominally 8% Al content buffer layer. Red dashed lines correspond to Silicon delta doping layers. Green dashed line corresponds to Tellurium delta doping layer from a GaTe compound source.

An analysis of the typical dislocation densities and types of dislocations observed when growing InSb quantum wells on GaSb and InSb substrates is now discussed and compared to previously reported growth of InSb quantum wells on GaAs substrates. Atomic Force Microscope (AFM) topographic analysis of quantum well heterostructures on GaSb and InSb substrates shows a dramatic shift in the type of dislocations and their density. The layer structure of the heterostructures grown for this comparison are shown in Figure 5.7.

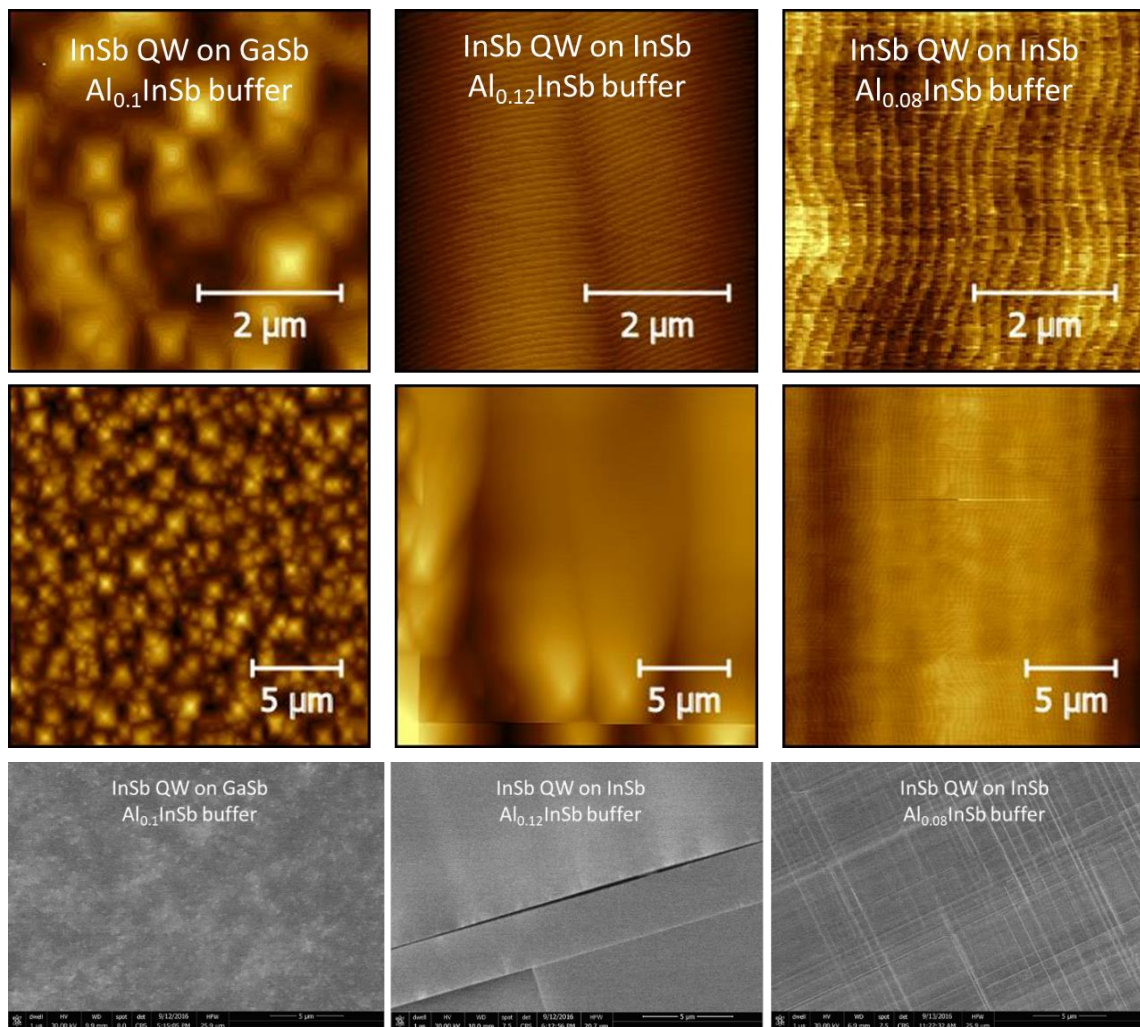


Figure 5.8 The top row shows AFM images with high density of screw dislocations in the left column due to the high mismatch of GaSb and InSb, with significantly smoother surfaces of InSb on InSb.

ECCI images confirm the high density of dislocation in the lower most row with a variation in prominent dislocation type as lattice mismatch is tuned. All ECCI images have a scale bar of 5 μm.

On GaSb substrates, a typical dislocation density of about 10^7 to 10^9 dislocations/cm² was observed, with step-flow growth around the threading components of screw dislocations, as evidenced from the square mounds. The peak to peak roughness was measured to be about 30nm over a 20 μ m square region, which was also the thickness of the quantum well. In comparison, previous work on GaAs substrates has reported peak to peak roughness of the order of 50-100nm [182]. Typical dislocation densities of 10^8 to 10^{10} /cm² have also been observed on the surface of InSb quantum well structures grown on GaAs substrates [169] and these results on GaSb are in line with those observations.

On structures grown on InSb substrates, dislocations were nucleated on the AlInSb/InSb substrate heterointerface as was observed by surface roughening on hetero-nucleation (or growth beyond the critical thickness). The separation on the surface between the threading components of the dislocations depended on the lattice mismatch (i.e. the aluminum content in AlInSb) and, in effect, on the mode and extent of lattice relaxation. In this work, it was seen that low aluminum content buffers grown on InSb had exceptionally low density of square mounds on the surface. The underlying misfit array led to wide area undulations and can be seen in AFM. With increasing aluminum content, the number of square mounds increased, as did the peak to peak roughness, measured over the same area.

Apart from AFM imaging, Electron Channeling Contrast Imaging (ECCI), was employed to further analyze the dislocations and get an accurate count of their density. ECCI is sensitive to sub-surface dislocations and correlated well with topographic images. It revealed that each square mound was a coagulation of about ten or more threading components of screw dislocations. The results from ECCI indicated that the dislocation counting by AFM is at most an optimistic approximation by about an order of magnitude, leading to the final dislocation

density of about 10^7 to 10^9 dislocations/cm². Figure 5.8 shows the comparative AFM and ECCI images for InSb quantum wells grown on GaSb and InSb substrates.

Figure 5.9 shows a HAADF-STEM cross section of an InSb quantum well grown on an InSb substrate, with nominally 12% aluminum content in the AlInSb buffer. The z-contrast from AlInSb/InSb superlattice is clearly visible and indicates the interfaces were abrupt. The z-contrast from the quantum well is also apparent, as it lacks aluminum. The image indicates the quantum well layer was also very well defined, and it correlates well with the AFM of the same shown in Figure 5.8 (center panel).

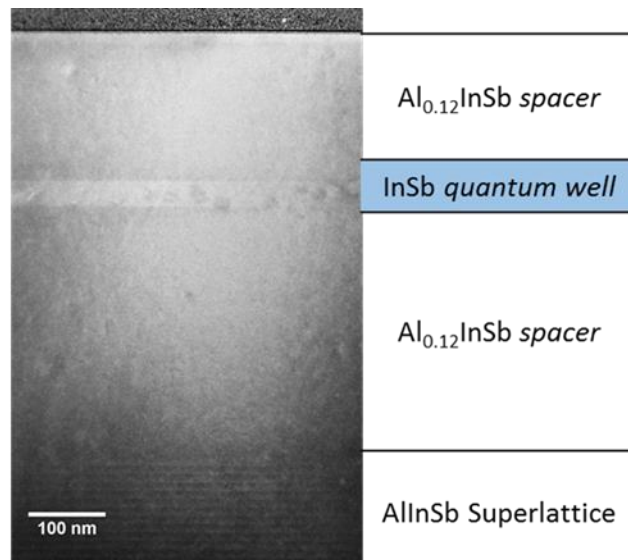


Figure 5.9 HAADF-STEM image of an InSb QW grown on InSb substrate with nominally 12% Al content buffer layer. AlInSb/InSb superlattice is visible in the lower part of the image with a well-defined layer of InSb QW. Image courtesy – D.J. Pennachio, UCSB.

5.4.4. Future directions for MBE growth

Having discussed the limitations and challenges of InSb growth and the growth of InSb quantum wells on GaSb and InSb substrates, a few inferences for future growth can already be drawn. In future InSb/AlInSb quantum well heterostructures, apart from incorporation of a superlattice of AlInSb/InSb or AlInSb/GaInSb, varying the substrate temperature (e.g. a

superlattice like cyclic variation from $445\pm 10^\circ\text{C}$ to $345\pm 10^\circ\text{C}$) during the 1-4 μm AlInSb buffer growth may further help in reducing the dislocation density and improving the surface roughness. With the newly incorporated pyrometric temperature feedback loop to automatically control substrate temperature based on a computerized program/routine (see Appendix B), such a “temperature superlattice” is much more feasible. Growth of buffer layers, prior to the quantum well, at sufficiently low temperature allows for reduced dislocation propagation but leaves a rough surface, as was seen in InAs quantum wells on InP [148]. Low-temperature growth also leads to excess group V incorporation which may increase remote ionized impurity scattering. To compensate for the shortfalls of low temperature growth, a high temperature buffer layer recovers surface roughness while also not significantly reducing the dislocation density – apart from the inherent reduction due to dislocation annihilation with increase in layer thickness. Therefore, a cyclic controlled repetition of low-high-low-high growth temperature, in the buffer layers preceding the quantum well, may lead to optimum results. Improvements in material quality with a low temperature hetero-nucleation followed by high temperature buffer growth have been reported widely elsewhere [148].

Careful observation of hetero-epitaxial nucleation in RHEED is also beneficial for growth of improved structures. When transitioning from the 6.1 \AA family of GaSb to the AlInSb lattice constant of $\sim 6.4 \text{ \AA}$, a nucleation temperature of $< 350^\circ\text{C}$ was found to be optimal [183] and was confirmed in this work. It was observed, in this work, that nucleating with a layer containing AlGaInSb led to a faster restoration of 2D RHEED after the significant mismatch upon transitioning from GaSb. Further improvements were also observed upon nucleating with a superlattice of InSb/AlInSb or AlInSb/GaInSb, as compared to solely nucleating with AlInSb, which is the most common approach.

There are other notable improvements that can be achieved through careful observation of RHEED reconstructions. Low temperature growth of 100-250nm immediately following the nucleation allows for a complete restoration of RHEED reconstruction intensity, while the 3D pattern (from relaxation of lattice mismatched materials) is either completely absent or disappears immediately post nucleation. A quick restoration of 2D RHEED is indicative of successful and relatively smooth hetero-interface nucleation.

Upon nucleating at higher temperatures, between 380-420°C the nucleation can fail (permanent presence of microscopic metal rich spots/haze), or restoration of RHEED can take significantly longer. Indeed, smooth 2D diffraction may never be observed if the nucleation is not perfected, as at elevated temperatures indium diffusivity increases rapidly [157]. This allows Indium to de-wet the surface of GaSb/AlSb and form quantum dots of InSb, which lead to a permanently 3D RHEED reconstruction and formation of grain boundaries on coalescing. In contrast, low temperature nucleation appears to promote 2D layer growth, by removing excess energy and hence is typically accompanied by an absence of 3D spots in RHEED but purely a dimming of diffraction intensity, until sufficient thickness of InSb is grown so as to lead to an InSb like $c(4 \times 4)$ diffraction pattern.

A key understanding that future work will need to develop concerns the doping efficiency of various dopants in InSb, AlInSb and GaInSb. As part of this work, preliminary efforts to grow heavily doped 1 μ m-thick layers of InSb showed that silicon had a doping efficiency of 25% when measured at cryogenic temperatures (<77K). On the other hand, tellurium from a GaTe compound source, had a doping efficiency of 50% at the same temperatures. Because, Si and Te are known to ride on the growth surface in the InSb material system [165], [166] at growth temperatures, reducing doping temperatures to less than 300°C

may aid future growths. Such a low temperature doping can be achieved by closing off the Sb flux when below $\sim 380^{\circ}\text{C}$ and followed by dopant evaporation and growth of a 1-3nm (possibly rough) InSb at $\sim 300^{\circ}\text{C}$ to effectively bury the dopants and minimize further riding. Following this process, the remainder of the structure could again be grown at the elevated temperature of $445\pm 10^{\circ}\text{C}$. This doping scheme would be similar to the routine used in growth of ultra high mobility GaAs quantum wells where silicon dopants are introduced at a substrate temperature of about $440\pm 40^{\circ}\text{C}$ while the rest of the quantum well structure (both above and below the delta doping layer) is grown at a temperature of $640\pm 10^{\circ}\text{C}$ [174].

Additionally, quick feedback on doping efficiency in the InSb material system is also a continuing challenge due to narrow band gap of InSb and related compounds, which makes intrinsic ionization much greater than commonly used doping concentrations, at 300K. Feedback could be obtained on cooling samples to cryogenic temperatures ($< 77\text{K}$), but obtaining that feedback would significantly limit the nature, scope and affordability of studies relating to doping efficiency, dopant ionization, and ohmic contact formation.

On InSb quantum wells grown on InSb substrates, Hall measurements on a series of samples showed that the doping efficiency at low temperatures was typically about 100% or greater. These observations indicate that electrons may be in the quantum well due to other unintentional donors imaging charges on the quantum well. It was also observed that for certain InSb quantum wells grown on GaSb substrate, cooling down under LED illumination led to silicon dopant ionization while the quantum well was “frozen out” (insulating) without an LED cooldown. By growing structures without any intentional doping, an attempt could be made to delink ionization under illumination from the formation of D_x - centers in AlInSb. While D_x - centers in AlInSb have never been reported, as have been extensively studied in GaAs [174],

almost any understanding on doping efficiency in InSb is lacking and the presence of D_x -centers in AlInSb is only one possibility. These future studies will improve the understanding of doping in InSb and also shine light on limiting scattering mechanisms for electrons in InSb quantum wells. Study of quantum well structures under illumination at cryogenic temperatures, in principle, also addresses the fundamental challenge of achieving reproducible growth of InSb QWs. This lack of reproducibility is believed to be one of the root causes of the lack of literature on InSb quantum wells.

Using the above studies as a guide, an ideal heterostructure promising ultra-high mobility InSb quantum wells could hence be inferred. This heterostructure would start with an InSb substrate and a thick buffer layer with a very low aluminum content AlInSb, separating the substrate from the quantum well channel. The structure can be grown without any intentional doping and, if necessary, with a small increase in aluminum content (of AlInSb) abutting the quantum well layer, to increase confinement. If the quantum well freezes out at low temperatures, then illumination could be used to attract carriers in the well prior to magneto-transport measurements. A top gate could also be used to do the same. Such a heterostructure, one with exceptionally low dislocation density and no intentional dopant-induced scattering centers, should be able to harness the full potential of InSb's intrinsic properties and may well be a necessary step towards the eventual discovery of fractional quantum Hall effect in InSb.

A lesser explored, high-risk, high-reward approach to making the growth of InSb quantum wells on InSb substrates more feasible is to grow AlInSb/InSb buffer layers with intentional mid-gap traps so that, at low temperatures, the buffer is insulating. This could alleviate the key challenge associated with the growth of InSb quantum wells on InSb substrates, i.e. parallel conduction from the substrate. An intentional p-type doping with very

low doping density of beryllium or carbon in the 10^{13} - 10^{15} /cm³ range to counteract the unintentional n-type doping from the substrate (typically n-type in the 1 - 3×10^{14} /cm³ range) could create a large depletion region, which in effect could serve as the intended “insulating layer”, between the conducting quantum well and the conducting InSb substrate. While this proposal restricts carriers within epilayers only, the intentional p-type doping could lead to a conducting layer close to the quantum well. For this reason, tight control of the p-type doping density would be essential.

Another option, for making the growth of InSb quantum wells on InSb substrates more feasible would be to introduce elemental metals like iron or chromium or rare earth elements like gadolinium, erbium, or lanthanum, in the AlInSb buffer layers grown on the InSb substrate, prior to the quantum well. The III-V VG V80H MBE used in this work does have elemental sources for some of the above elements (Cr, Gd, Er), out of which gadolinium and erbium were studied as potential mid-gap trap states. Semiconductor wafer manufacturers have used similar dopants in GaAs (CrO) and InP (Fe) to pin the Fermi level mid-gap in the substrate to make it insulating.

While doping with erbium and gadolinium was relatively successful, a significant parallel conduction path was still observed with both dopants. Due to the use of solder In:Sn contacts, which permeate uncontrollably through the epi-layers, a conclusion could not be drawn on whether the doping was successful in making insulating epi-layer buffers of AlInSb. An extensive study of intentional mid-gap traps, as dopants in buffer layer of AlInSb, is needed on insulating substrates like GaAs and GaSb, to draw reliable conclusions.

A final option for improving reproducibility and peak mobility of InSb quantum wells on InSb substrates is to study the cap layer. An insulating cap layer can also act as a gate dielectric layer. The addition of an *in-situ* gate dielectric layer, prior to exposure of the III-V to air. An example this option would be the low temperature deposition of a thin (~1-3nm) aluminum, on the InSb cap layer of the InSb quantum well heterostructure, which would then be intentionally oxidized, prior to exposure to air. The thickness of the aluminum layer would have to be precisely controlled so as to lead to complete oxidation (no parallel conduction path to metallic aluminum) and yet induce minimal oxidation of the InSb/AlInSb semiconductor layer below. Such an *in-situ* evaporated dielectric would prevent the formation of Sb-O bonds which are known to be conducting and would avoid the formation of uncontrolled surface scattering centers, thus in-principle enhancing peak mobility, while also improving gate-tunability. A thicker dielectric could then be deposited *ex-situ* (e.g. electron beam evaporated AlO_x or Atomic Layer Deposition (ALD) AlO_x).

5.4.5. Magneto-transport measurements

Hall measurements were performed on all InSb quantum wells grown. These measurements provided feedback on device hetero-structure design, material quality and provided an insight on fabrication more complex devices.

Most often, low temperature magneto-transport measurements were performed in a Quantum Design Physical Property Measurement System at 2 K as detailed in Section 3.3. Multiple sample geometries were studied, including: Van der Pauw (each side about 5mm) and, Hall bars (150 μm by 200 μm and 20 μm by 80 μm). In samples with a top gate, a water-based Al₂O₃ Atomic Layer Dielectric was evaporated post-mesa etching with the sample

temperature at 200°C and a thickness of about 25-50nm. The ohmic contacts and gate metal were electron beam evaporated Ti/Au. In Van der Pauw geometry samples, solder contacts were made with an alloy of In:Sn (52:48 by weight). If required, annealing was performed at 150-200°C on a hot plate in air. Details of the device fabrication are provided in Section 3.2.

Electrical transport characteristics measured by mobility, sheet resistance and presence of parallel conduction were found to be sensitive to the III-V cap layer on the sample. While an extensive study correlating the impact of capping layer, to magneto-transport in InSb quantum wells remains pending, an immediate difference was noted between samples capped with InSb (1-10nm) and samples capped with AlInSb (1-100nm, including the top barrier above the quantum well). It was observed that the samples with an AlInSb layer on the surface were susceptible to minor variations in annealing conditions (primarily time and temperature). No such immediate dependence was apparent in samples capped with a thin layer of InSb.

Based on Hall measurements performed, it was observed that samples capped with AlInSb showed an increase in carrier concentration and a decrease in mobility, upon increasing the annealing time. On the other hand, samples with an InSb cap layer were robust against annealing time and showed the most consistent results with annealing. Due to the significant diffusivity of In:Sn in the InSb/AlInSb heterostructure at the temperature of the soldering iron (~200°C), most samples did not require any further annealing. Care was taken to ensure the In:Sn did not diffuse through the insulating AlGaAsSb buffer when working with GaSb:Te substrates. Similarly, In:Sn diffusing into the conducting (undoped) InSb substrate was a persistent challenge due to a lack of AlGaAsSb like insulating barrier layer. Samples measured on InSb substrates hence showed signs of parallel conduction at low field. The foremost conclusion obtained from using solder contacts in Van der Pauw geometry samples was that

shallow, evaporated contacts, rather than soldered contacts, are required for next generation of experiments on InSb substrates [153].

In the course of this work, the first reported growth of an InSb quantum well on a GaSb substrate was achieved. A conducting GaSb:Te substrate was used for growth, and an $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}$ buffer layer was used to isolate the conducting substrate from the AlInSb/InSb layers of the 2DEG. A Van der Pauw geometry sample was measured and showed clear Integer Quantum Hall Effect (see Figure 5.10). The mobility was measured to be $101,000 \text{ cm}^2/\text{Vs}$ at 2K at an electron density of $3 \times 10^{11} / \text{cm}^2$. The onset of SdH oscillations was measured to be at

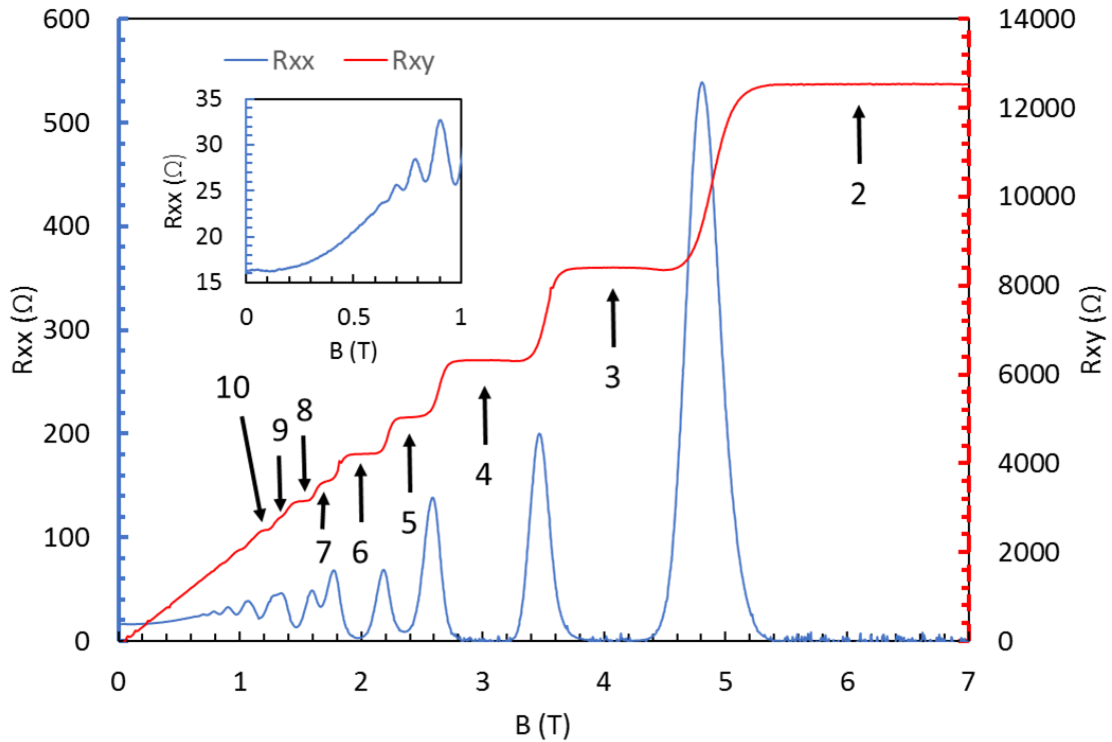
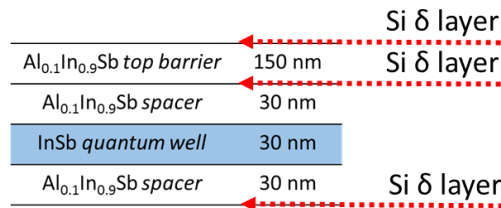


Figure 5.10 Integer Quantum Hall Effect observed in an InSb quantum well grown on GaSb:Te substrate. Inset shows the onset of SdH oscillations, with the layer structure shown above.

about ~ 0.6 Tesla, indicating a quantum mobility of about $\sim 17,000$ cm^2/Vs . The structure consists of a 180nm deep square symmetric 30nm wide quantum well, with silicon delta doping layers $3 \times 10^{11}/\text{cm}^2$ each, on either side of the quantum well, separated by 30nm AlInSb. The structure also consists of a $2 \times 10^{12}/\text{cm}^2$ uniformly doped 6nm capping layer of AlInSb with nominally 9% aluminum. This first demonstration thus indicates that quantum wells of InSb can be successfully grown on conducting GaSb substrates, without any parallel conduction.

As has been mentioned previously, Fractional Quantum Hall Effect (FQHE) has not been observed in InSb as of this writing. In the search for FQHE, after the demonstration of InSb QWs on GaSb, efforts were made to reduce electron density in the quantum well and to

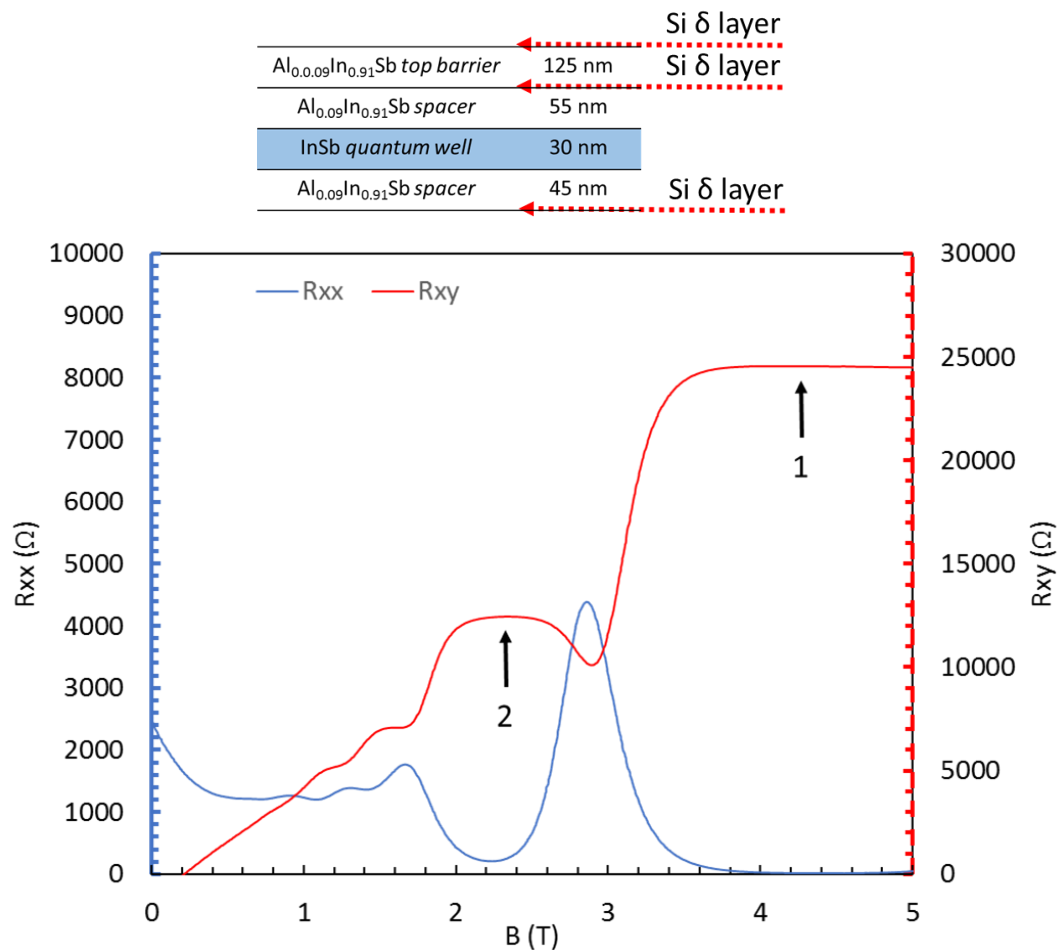


Figure 5.11 A low density InSb quantum well, as measured in VdP geometry with an electron density of $1 \times 10^{11}/\text{cm}^2$.

demonstrate quantum wells of electron density in the $\sim 10^{10}/\text{cm}^2$ range (as opposed to the typical $10^{11}/\text{cm}^2$ range). While a reduction in density is expected to lead to a reduced corresponding mobility, the observation of lower Landau levels at a lower magnetic field is also of great interest.

With the aim to observe the $1/3$ FQHE state at magnetic fields of ~ 15 Tesla (less than the 18 Tesla available at NHMFL, Tallahassee), InSb QWs with doping density about half of the previously reported $2\text{-}3 \times 10^{11}/\text{cm}^2$, were grown at 180nm from the surface. The results from this growth are summarized in Figure 5.11, which shows magneto-transport at 2K from a 180nm quantum well with an electron density of $1.2 \times 10^{11}/\text{cm}^2$, measured in the Van der Pauw geometry. $\nu=1$ is observed at 5 Tesla, which would put $\nu=1/3$ at ~ 15 Tesla. Upon measuring at 20mK at NHMFL, the contacts were found to have transformed from ohmic at 2K to Schottky (metal-semiconductor diode)-like at 20mK. Unfortunately, no hints of a fractional quantum Hall state were observed through the Schottky contacts.

A detailed study of ohmic contact formation in buried InSb quantum wells is required, as has been mentioned previously. Such a study would be necessary for applications of InSb in quantum computing where the operating temperature of 20mK is standard. Understanding of metallic contact response at elevated temperatures may not be directly relevant, however, due to the significantly narrow band gap of InSb and the impact thermal energy can have on electron transport through a Schottky barrier (thermionic emission vs field emission vs thermionic field emission).

To further improve upon the growth of InSb quantum wells, InSb quantum well structures on InSb substrates were grown. The substrates were cleaned with atomic hydrogen

detailed earlier in this chapter (see Section 5.2) and AlInSb was nucleated on a buffer of InSb. This abrupt nucleation of AlInSb on InSb is expected to lead to the AFM morphology evident in Figure 5.8 (center panel), although reducing the aluminum composition to 8%, significantly helped with improving the morphology at the cost of reduced resistance of the AlInSb buffer layers (see Figure 5.8, right panel). The nominal aluminum concentration was maintained at about 12% and a 180nm deep 30nm wide quantum well was then grown. Silicon delta doping layers were incorporated 60nm away from the well on either side with a doping density of $2 \times 10^{11}/\text{cm}^2$ each. The electron density estimated from the slope of Hall resistance is about $4.35 \times 10^{11}/\text{cm}^2$, indicating a doping efficiency in excess of 100% at 2K.

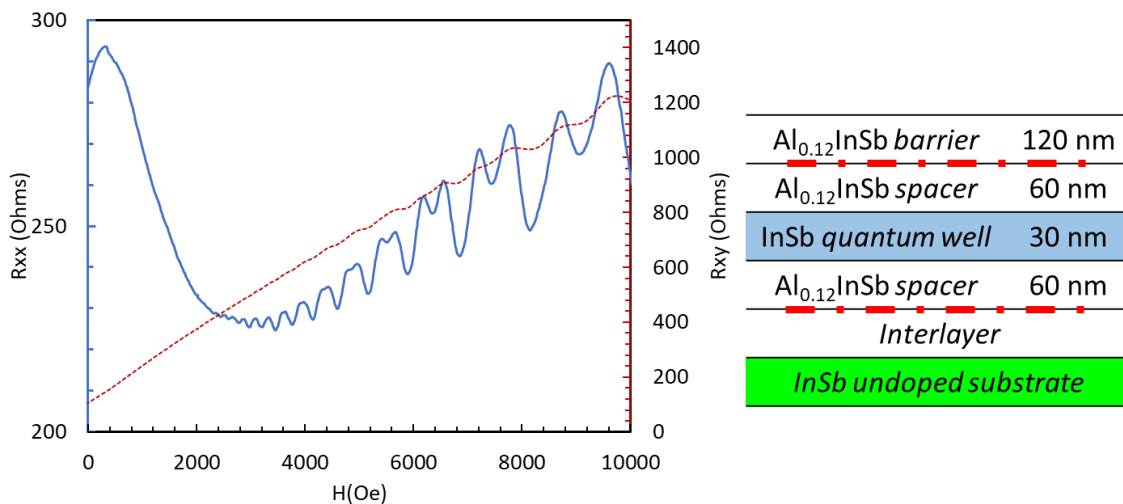


Figure 5.12 Onset of SdH oscillations at 0.2 Tesla at 2K in an InSb QW grown on InSb substrate showing the highest reported quantum mobility in an InSb QW system, to date.

In these InSb quantum well structures grown on InSb substrates, magneto-transport measurements at 2K showed significant R_{xx} and R_{xy} intermixing, making it very difficult to extract a Hall mobility. However, low field data did show an onset of SdH oscillations at a magnetic field of 2,000 Oe, indicating a quantum mobility of $50,000 \text{ cm}^2/\text{Vs}$. This quantum mobility is a record and is greater by ~ 2.5 times as compared to previously reported mobility on highest Hall mobility samples in InSb [165], [166].

Some other notable features were also observed. At 0.5 Tesla odd and even integer splitting is evident, as a result of the very high g-factor of InSb. Furthermore, at high magnetic fields, parallel conduction leads to R_{xx} values being negative. This parallel conduction is expected from the substrate as ohmic contacts were made by In:Sn solder to a Van der Pauw geometry sample. Thus, the results from the first generation of devices fabricated from the first InSb quantum well samples on InSb substrates were considered to be highly successful.

In the future, if evaporated ohmic contacts are successfully developed for InSb quantum wells, such that the contact does not permeate through to the conducting substrate, a Hall mobility could finally be measured. The Hall mobility measured on this sample or on other structures grown on InSb substrates is expected to far exceed the previously reported highest Hall mobility (this increase is expected because Hall mobility is sensitive primarily to large angle scattering while quantum mobility is sensitive to all scattering; therefore, an improvement in quantum mobility corresponds to a dramatic improvement in Hall mobility). Meanwhile, the paradigm shifting growth of InSb quantum wells on an InSb substrate, though still requiring further work to remove parallel conduction, can be considered a significant improvement on the more traditional approach of growing InSb quantum wells on GaSb and GaAs substrates.

5.4.6. Gate-tunable InSb quantum wells

To further study the quantum wells grown, gated Hall bar structures were fabricated on InSb quantum wells on GaSb substrates. A key goal of the gated structures was to see if the InSb quantum wells could be depleted of carriers completely (indicating, in part, a pure 2DEG devoid of parallel conduction or screening paths). A secondary goal was to study structures with bottom gate control. The final goal, which remains a focus of future work, is demonstrate InSb quantum wells with simultaneous top and bottom gate control – i.e. changing the Rashba spin orbit coupling (electric field on the 2DEG) while keeping the electron density constant.

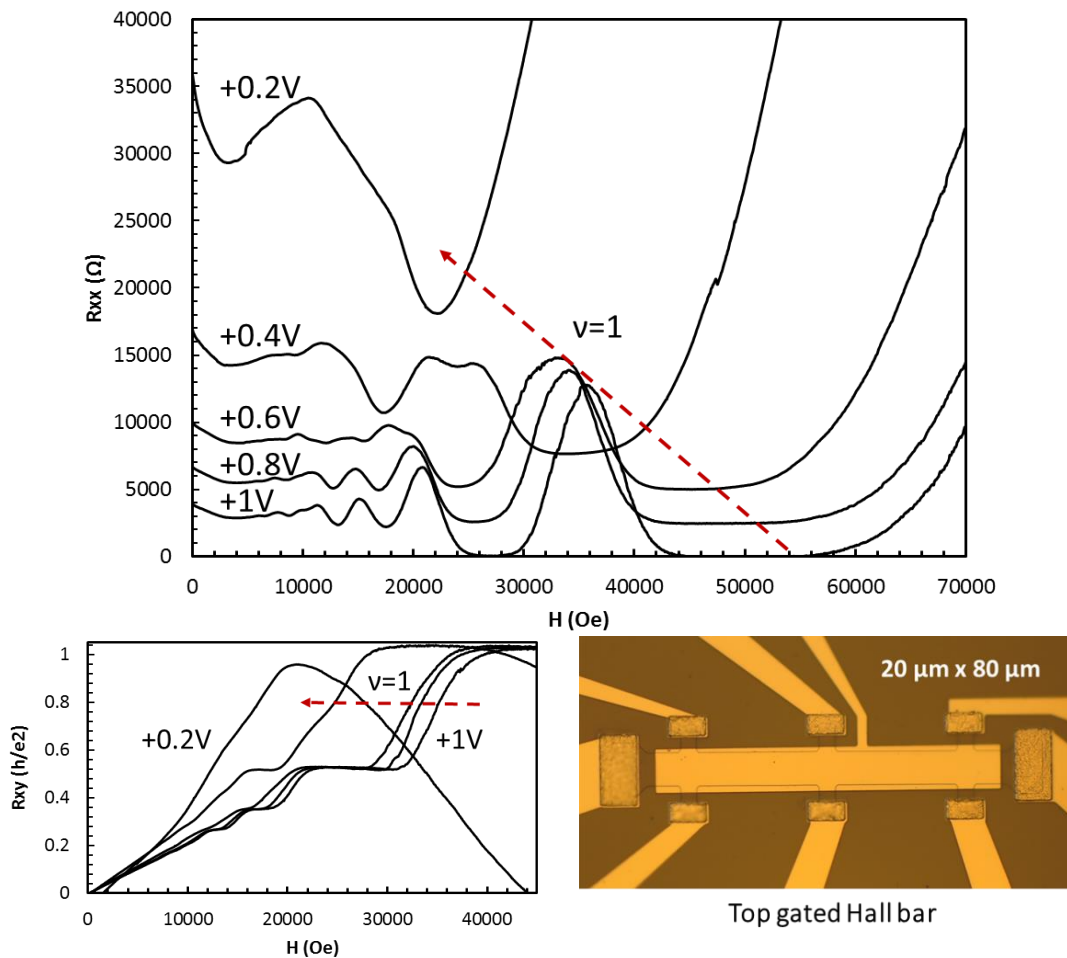


Figure 5.13 Top gate control of electron density in InSb quantum well, with full depletion at 0V.

A top gated Hall bar structure was fabricated on a 180nm deep InSb on an undoped GaSb substrate. VdP measurements of the same sample, without any gate, are shown in Figure 5.11. Upon cooling down the gated-Hall bar, it was observed that the sample was depleted at zero-gate voltage. While it is common for the ALD process to introduce charge trap states at the dielectric-semiconductor interface, the effects of dielectric deposition are often cushioned by a miniscule change in electron density. Dielectric deposition can add or subtract carriers from the system depending on the energy of trap states, which means that it introduces significant uncertainty in device performance post-fabrication. Potential workarounds to avoid this uncertainty have been suggested previously in Section 5.4.4.

In the current sample, the original electron density is very low to begin with, and hence the change in carrier concentration towards a lower number leads to depletion of the electron gas at 2K at zero gate voltage. Upon application of small positive gate voltage, though, electrons are restored in the quantum well. Figure 5.13 shows the changing IQHE in this low-density sample with a gated Hall bar at 2K, leading to full depletion. While this is the first demonstration of full depletion of an InSb quantum well on a GaSb substrate, it must also be noted that depletion of InSb QWs on GaAs substrates was first reported first by M.M. Uddin, et al., in 2013¹⁷ [153], [184].

¹⁷ W. Yi, et al., (2015) wrongfully claim first demonstration of full depletion as the premise of the publication [153], while also citing the actual first demonstration by M.M. Uddin, et al., (2013) [184].

Now that the demonstration of top-gate control and IQHE without parallel conduction on a conducting substrate has been achieved, it is natural to explore other ideas. For instance, it makes sense to study the use of conducting substrates, especially after the development of an insulating buffer on GaSb with demonstrated bottom gate control of InAs quantum wells [151]. As has been mentioned previously, top and bottom gate control simultaneously allows for maintaining electron density constant while changing the Rashba spin-orbit coupling, i.e. the structural inversion asymmetry and is an interesting challenge to pursue.

This work undertook just such a study, the results of which was the first demonstration of bottom gate control on an InSb quantum well, using a tellurium doped, conducting, GaSb substrate.

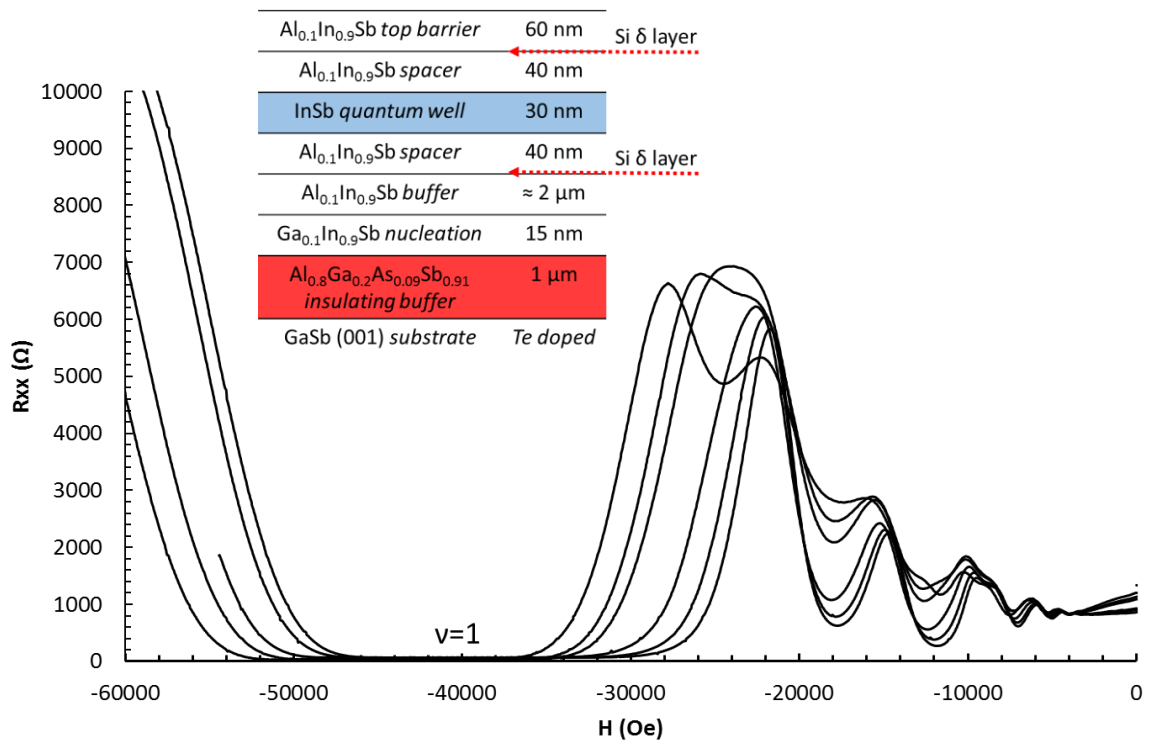


Figure 5.14 Bottom gate control with doped GaSb:Te substrate as a global bottom gate, showing modulation of electron density in an InSb quantum well. $\nu=1$ plateau moves further towards a higher magnetic field as bottom gate voltage is swept from zero (right most plot, lowest carrier density) to +6V (left most plot, highest carrier density).

The layer structure consists of a 100nm deep 30nm wide InSb quantum well, with an InGaSb type nucleation layer at the hetero-interface when the lattice constant of the epi-layers is changed. Figure 5.14 shows the results, with changing electron density leading to a shift in the Integer Quantum Hall Effect minima at $\nu=1$. Upon application of a positive gate voltage on the bottom gate, the electron mobility increased from 60,000 cm^2/Vs at a density of $6 \times 10^{10} / \text{cm}^2$ to a mobility of 90,000 cm^2/Vs at a density of $\sim 1 \times 10^{11} / \text{cm}^2$. The gate was found to be significantly “hysteretic”. Hysteresis can be attributed to significantly high density of electronic traps in the gate dielectric, i.e. in the semiconductor buffer layers below the quantum well. The electronic trap states could potentially be due to the high density of dislocations nucleated at the transition from the 6.1 Å family of GaSb/AlGaAsSb to the 6.4 Å family of InSb/InAlSb.

Despite the success of bottom gate control, the demonstration of top and bottom gate control simultaneously, remains an outstanding challenge for InSb quantum wells. Such a demonstration of tandem gate control would effectively demonstrate full depletion of the 2DEG and accumulation of electrons in second sub-band occupation – going through the complete filling of the first sub-band. Tandem gate control would also help with the determination of the peak electron mobility with a symmetric wave function at maximum occupation of the first sub-band in an InSb quantum well, which has never been reported.

5.5. InSb VLS nanowires

5.5.1. Prior work

As discussed in previous sections of this chapter, InSb quantum wells have shown great promise, and they have plenty of opportunity for further study. However, InSb VLS nanowires are without doubt the most attractive material system for realization of Majorana Zero Modes for topological quantum computation. Indeed, the first observation of zero-bias peaks in 2012 was in an InSb nanowire grown by MOCVD with a partial sputtered shell of NbTiN as the s-wave superconductor [55]. Signatures of zero-bias peak reminiscent of the predicted MZMs were first observed upon the application of an in-plane magnetic field along the length of the nanowire. In this section, the work described has cemented the place of InSb as the material of choice, and InSb nanowires as the geometry of choice, in the search for novel phenomena necessary for the realization of topological quantum computing.

After V. Mourik, et al., [55], a significant number of research groups reported the observation of zero-bias peaks in a few different flavors of materials, device geometries and measurement techniques [54]. The next several paragraphs will provide an overview of the materials aspects of these first wave of findings. After these pioneering efforts have been explained, this section will then show how work performed as part of this dissertation has added to the findings of predicted topological states in InSb nanowires.

Firstly, the two materials that were common among all the ‘first-wave’ of MZM findings (2012-13) were InSb and InAs. NbTiN and aluminum were the superconductors of choice, with NbTiN coupled to InSb and aluminum coupled to InAs for some [54].

In all cases, NbTiN was evaporated *ex-situ*, i.e., the sample was removed from the growth reactor (MBE or MOCVD), exposed to air, lithographically patterned, and (optionally) lightly cleaned prior to NbTiN sputtering. NbTiN was chosen for its extremely high H_c , as the theoretical proposals had recommended a superconductor that remains superconducting even after the application of a relatively strong in-plane field.

In stark contrast to the NbTiN deposition on InSb, aluminum on InAs was evaporated *in-situ* immediately post-growth in the MBE reactor. The interface thus formed between aluminum and InAs was devoid of oxide, (assuming a smooth and uniform coverage of aluminum). P. Krogstrup, et al., later claimed they had grown an abrupt Al-InAs epitaxial interface by evaporating aluminum in the MBE reactor; post-growth at a thermocouple temperature between 0°C and -40°C (273-233K) [83]. The most notable improvement in this low temperature aluminum-InAs process as compared to the previous deposition of any superconductor on semiconductor nanowire was the presence of an induced hard gap in the superconductor.

Such an induced hard-gap was not evidenced in the NbTiN-InSb system then, and instead the other systems could be considered to be plagued with a ‘soft-gap’ problem [82]. In terms of electrical band structure, a hard gap was a superconducting gap devoid of measurable sub-gap states, such that the properties of the superconductor matched theoretical predictions [84]. Theory required the sub-gap conductance to be significantly suppressed in a conductance spectroscopy measurement as presence of unpaired electrons was not permitted in a hard gap superconductor – or a region of semiconductor in close proximity with the superconductor, such that the semiconductor possessed an induced superconducting hard-gap. In experimental results demonstrated prior to the work by P. Krogstrup, et al., soft-gap, i.e. significant

conduction through the superconducting gap was immediately apparent, even though the zero-bias conductance peak was one such peak in conductance [55].

It was theoretically argued that the zero-bias peak was not of the required and expected quantized value due to the presence of a soft induced gap in the material system. Such a soft-induced gap would enable the Majorana state to be smeared out leading to the experimentally observed value of 1-20% of the expected peak height of $2e^2/h$ conductance (though it must be noted that, even though epitaxial Al-InAs interfaces with a hard-induced gap were developed, the peak height did not reach the quantized conductance value [96]).

In parallel with the work on InAs-Al, other efforts to improve the superconductor evaporation on InSb surfaces bore fruit, and ballistic Majorana transport was observed after a gentler cleaning of the InSb surface followed by ammonium-sulphide passivation to create an intentionally n-type interfacial layer (by surface doping with Sulphur) [85], [86], [185]. Sulphur passivation modified the surface of InSb by locally doping it heavily with Sulphur, making it reminiscent of the InAs surface. As a result, ohmic contacts were formed much easier and superconductivity was induced with relative ease. While transport did improve, however, an induced hard gap was not observed, and neither was quantized Majorana conductance.

While a variety of superconductors can be evaporated in MBE or an electron-beam evaporator or sputtered, NbTiN and aluminum emerged from all these first-wave studies as the “go-to” s-wave superconductors for the realization of MZM devices. NbTiN offers a large parent superconducting gap and a process that can be optimized in a nanofabrication facility. Aluminum, on the other hand, has a much lower superconducting gap, a lower critical temperature, and a lower critical field, and is readily available in all III-V MBE systems. Thin

films of aluminum also exhibit reasonably high in-plane critical field, though not as high as NbTiN. As MZM applications require application of a magnetic field perpendicular to the spin-orbit field, i.e., along the length of the electron chain/nanowire, aluminum became a viable option with its critical field in excess of 4 Tesla for low thicknesses [110].

Ideally, to replicate the progress made in InAs-Al platform on the InSb-Al material system, MBE growth of long ($>10\mu\text{m}$) InSb nanowires followed by low-temperature evaporation of aluminum on these nanowires was required.

5.5.2. InSb nanowire growth and cleaning

MBE growth of long InSb nanowires posed many challenges. As has been mentioned in Section 4.3, to achieve a uniform nanowire diameter and length, the semiconductor substrate was covered with a dielectric ($\text{SiN}_x/\text{SiO}_x$) such that III-V growth was inhibited on the dielectric and such that nanowire growth proceeded only in exposed vias which were also covered in a thin (3nm) film of Au. The determination of MBE growth parameters for the growth of long ($>10\mu\text{m}$), uniform VLS nanowires with a primarily Sb_2 flux remains an outstanding challenge. This challenge arises, in part, due to the competition between surface diffusion (In and Sb on the dielectric vs nanowire sidewalls), decomposition of InSb ($\sim 450^\circ\text{C}$ under the peak flux in the MBE reactor) due to desorption of antimony, and the sticking coefficient of indium (unity at all temperatures in consideration, on all surfaces on the sample).

In comparison to MBE growth, MOCVD growth of InSb nanowires is performed at significantly elevated temperatures of $\sim 490\text{-}510^\circ\text{C}$ under a Sb_2 flux that is many orders of magnitude greater ($\sim 100\text{ mTorr}$ to few Torr) than the peak Sb_2 flux available in an MBE ($\sim 10^{-5}$ Torr). Selectivity of growth only on the III-V and not on the dielectric is aided by the use of

metal-organic indium, which has a sticking coefficient less than unity on the dielectric [81], in comparison to the elemental indium available in an MBE, which has a sticking coefficient of unity (i.e. all indium impinging on the surface, remains on the surface and does not desorb). With the current understanding, MOCVD is able to better address the InSb growth window leading to the growth of long InSb nanowires, with minimal growth of the dielectric mask.

In effect, this meant that the aluminum evaporation now had to be perfected on nanowires that were grown by MOCVD at TU Eindhoven. These nanowire samples were loaded into vacuum after exposure to the atmosphere and surface oxide was removed by atomic hydrogen cleaning. This cleaning was an additional step that the InAs-Al process lacked. Efforts to evaporate aluminum on InSb nanowires (grown by MOCVD at TU Eindhoven) started as early as 2014 at UC Santa Barbara. However, significant challenges were encountered – primarily relating to 1) the presence of an interfacial layer (consisting of oxygen and/or carbon) between the aluminum and InSb, and 2) the evident “balling up” of aluminum on the InSb nanowire surface.

In comparison, a relatively smooth film of aluminum on InAs, devoid of any interfacial layer, was shown to be obtained by evaporating at substrate temperatures between 0°C and -40°C (273-233K) [83], [87]. For MBE-grown VLS InAs nanowires, power to the substrate heater was turned off such that the liquid nitrogen-cooled cryo-panel could radiatively cool the sample (with VLS nanowires) to the lowest possible temperature over a course of few hours. Aluminum from an effusion cell in the MBE chamber was then used to coat the VLS wires. Unfortunately, this process was not replicable for InSb. Repeating the same steps with MBE-grown InSb nanowires (or MOCVD nanowires that were loaded into MBE chamber), led to the surface of aluminum de-wetting the InSb surface. It could thus be concluded that -40°C

(233K) measured on the sample manipulator was still too “hot” for the evaporation of aluminum on InSb.

Now, some details of the cleaning process must be clarified. Specific parameters for the atomic hydrogen cleaning of InSb wafers were developed in 2015 as part of this work, and they have been described in detail in Section 5.2. The growth of InSb quantum wells on InSb substrates using those parameters was also demonstrated in 2015 and it has been described in Section 5.4.2. In 2016, these same parameters were implemented by J.A. Logan for the cleaning of InSb VLS nanowires. The exposure time of 20 minutes was chosen for the (011) facets of nanowires as compared to the 60 minutes used on the (001) InSb wafers.

In another cleaning-related issue, certain procedures had to be adapted to avoid unexpected and unintentional surface contamination, prior to aluminum evaporation. While it was common to image nanowires in an SEM in a nano-fabrication facility prior to loading into the UHV, it was observed by STEM-EDX analysis that the InSb-Al interface was covered in carbon and carbon compounds. The origin of this “carbon contamination” was estimated to be the poor vacuum in of $\sim 10^{-4}$ to 10^{-7} Torr in the SEM chamber. Starting in 2016, samples studied by S. Gazibegovic and J.A. Logan were not looked into under the SEM until after aluminum had been evaporated. This modified operating procedure successfully removed the carbon layer formed at the superconductor-semiconductor interface. As such, all data reported here is from samples that followed this new approach.

Next, confirmation of the success of cleaning procedures had to be adapted for nanowire growth. As has been reported in Section 5.2, the successful removal of thermal oxide from the surface of InSb wafers by atomic hydrogen cleaning was confirmed by RHEED, XPS and the

epitaxial growth of InSb by MBE. Unfortunately, these tools are not favorable for determining the removal of surface oxide on nanowires, especially when the 2D substrate is covered in a dielectric. While RHEED is surface sensitive when used with 2D wafers, the nanowires themselves are electron transparent, and RHEED indicates a 3D diffraction reminiscent of the bulk crystal. Furthermore, since the nanowire cross-section is relatively small as compared to large swath of SiO_x/SiN_x dielectric on the substrate, a large area sampling technique, like a conventional XPS with a spot size greater than 1 mm² was found to be insensitive to minor changes in the surface chemical composition of the nanowires. Without these quick and readily available *in-situ* feedback tools, SEM and STEM were heavily used to confirm whether cleaning processes worked, increasing the time between growth and feedback.

5.5.3. Aluminum evaporation on InSb nanowires

With the nanowire growth, handling and cleaning procedures now established, this discussion can move onto the growth of aluminum. Since it was observed that -40°C (233K) wasn't cold enough to form a smooth film of aluminum, a specialized sample manipulator was employed. This sample manipulator was designed for conductive cooling of the sample during MBE growth and its construction and operation has been described in detail in Appendix B.

In the first round of growths, using the cold manipulator, aluminum was evaporated at a substrate temperature of 140K (-133°C) using nitrogen gas as the coolant [81] (see Figure 5.15). In later work, aluminum growth was performed at temperatures as low as 80K (-193°C) using liquid nitrogen as the coolant. These low temperature growths showed a reasonably smooth surface of aluminum with large grains. A ~10nm film of aluminum with a growth rate of 12 (±2) nm/hour, was chosen for this particular study. This growth rate corresponded to an

aluminum effusion cell temperature between 1040 to 1080°C. The source to sample distance was approximately 200 mm and all samples were capped with approximately 5nm of AlO_x from an electron beam evaporator, within 10 minutes of the growth ending.

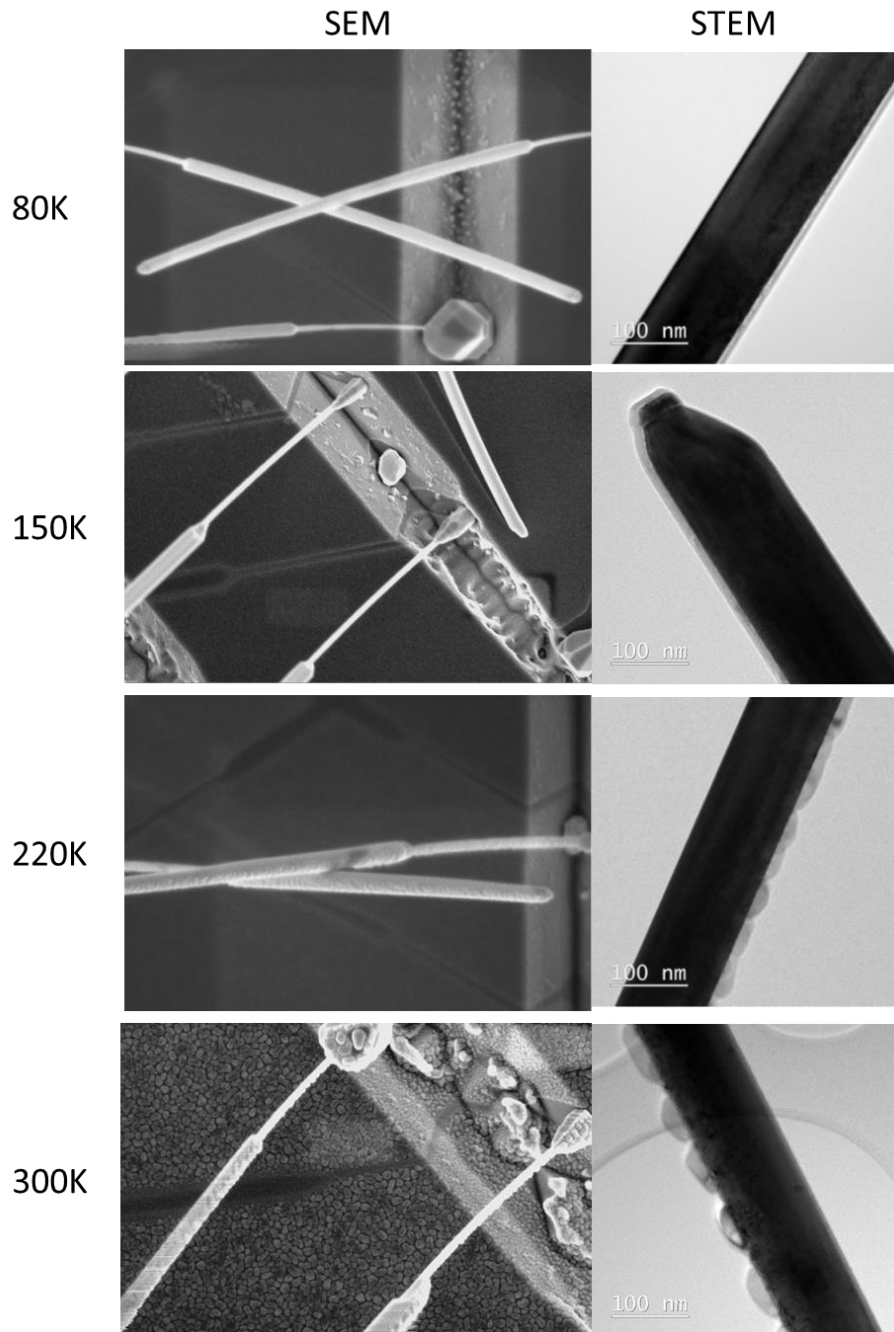


Figure 5.15 Scanning Electron Microscopy (SEM) and Scanning Transmission Electron Microscopy (STEM) of ~10nm aluminum on atomic hydrogen cleaned InSb VLS nanowires. Aluminum growth was studied at 80K, 150K, 220K and 300K. TEM images courtesy – M. Verheijen, TU Eindhoven

Growth of aluminum on the (011) type facets of InSb nanowires was studied at 80K, 150K, 220K and 300K and all samples were treated identically otherwise (see Figure 5.15). On samples grown at 300K, the 10nm film “balled up” and led to coagulation of impinging aluminum and formation of well separated aluminum islands. This behavior could be attributed to the “de-wetting” of aluminum, which was assisted by the energy provided by ambient at 300K. Evidence of an interfacial reaction between aluminum and InSb was also observed. This interfacial reaction could be due to the tendency of aluminum to form AlSb.

The growth of aluminum at 220K, shows a larger grain formation as compared to the growth at 300K in a HAADF-STEM, but is still not a smooth film with an abrupt interface between aluminum and InSb. Smooth films of aluminum on InSb were observed in HAADF-STEM for growths at 150K and 80K while there was no evidence for an interfacial reaction at both 150K and 80K. Even though the films appeared smooth in SEM and HAADF-STEM, careful examination revealed aluminum to be textured at both temperatures, i.e. it maintained epitaxy with the nanowire beneath, but had grains that were rotated w.r.t. each other.

In summary, 80K and 150K growth of aluminum on InSb VLS nanowires was found to be optimum for growth of thin continuous films with an abrupt interface. As the discussion now moves on to the electrical characteristics of Al-InSb devices, it must be noted that non-ideal response (sub-gap states in induced superconductivity) may originate from non-ideal superconductor growth, or non-idealities at the super-semi interface. A correlation between electrical characteristics of induced superconductivity in semiconductors from epitaxial, single crystal superconductors vis-à-vis textured or polycrystalline superconductors has not been studied and remains a focus of future work.

While the growth of aluminum on InSb was successfully observed after atomic hydrogen cleaning and aluminum evaporation at 150K and lower, it was observed that solely letting the sample warm up from 80K or 150K to room temperature (300K) after evaporation was not enough to ensure a smooth film (when observed in a SEM or STEM, hours or days later). Based on the SEM images, after warming up to 300K, or in the process of warming up, the pure elemental aluminum on the surface was expected to become mobile leading to formation of droplets, similar to the aluminum de-wetting the surface of InSb observed by growing at 300K (see Figure 5.15).

To prevent this issue, the layer of aluminum was intentionally oxidized by several processes: i) the evaporation of 2-5nm of AlO_x , by a UHV interconnected e- beam evaporator from an Al_2O_3 source, ii) exposure to pure O_2 in an interconnected UHV MBE with the oxygen pressure as high as $\sim 1 \times 10^{-3}$ Torr (base pressure $< 1 \times 10^{-10}$ Torr) for 15 minutes iii) exposure to nitrogen at atmospheric pressure in the load lock, for about one minute, where N_2 was expected to contain trace levels of O_2 , and lastly iv) exposure to ~ 100 Torr of pure O_2 in a load lock for 15 minutes. This was followed by letting the sample warmup close to room temperature, in vacuum, prior to unmounting of the nanowires from the growth block. This wait in vacuum (of about 1 to 12 hours) was introduced to prevent excessive condensation of moisture on the sample, while it was below 0°C (273K).

Formation of AlO_x on the surface of pure aluminum upon exposure to O_2 is nearly instantaneous due to the enthalpy of formation of primarily Al_2O_3 [184]. It is also known that aluminum reacts with O_2 and does not require an activated form of oxygen (which may be even more reactive than O_2). An exposure of one Langmuir of oxygen (1×10^{-6} Torr for 1 second) is expected from all four of the above three techniques used. Care was taken to move the sample from the cryogenic cold stage, used for aluminum evaporation at 77K, to the next process chamber (typically a load lock) for exposure to oxygen in as short a time period as possible (typically 4 to 7 minutes, always less than 10 minutes). The sample was not expected to warm up rapidly to room temperature during this transfer time. The samples were exposed to 100 Torr of oxygen for 15 minutes to ensure complete oxidation (see Figure 5.16).

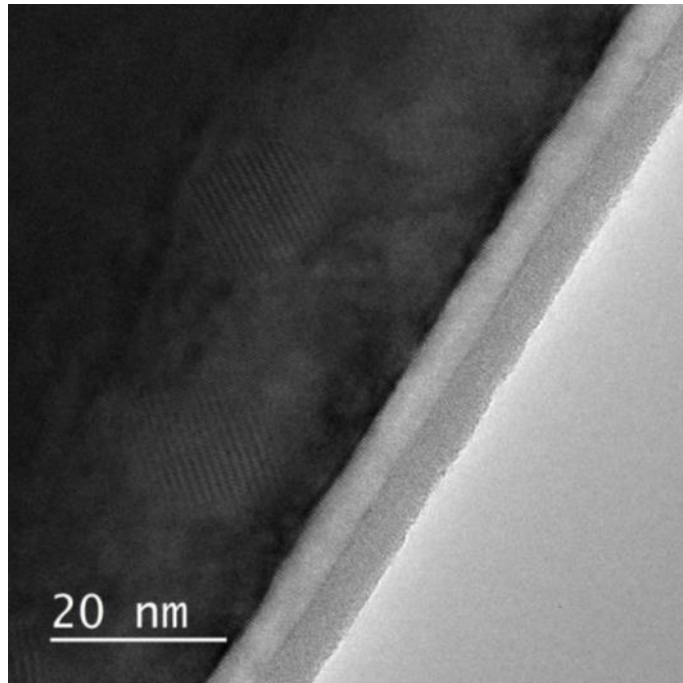


Figure 5.16 STEM image of 10nm aluminum on InSb, grown at 80K, which was oxidized by exposure to 100 Torr of pure oxygen in a load lock. The Al-InSb interface appears abrupt. Image courtesy – M. Verheijen, TU Eindhoven.

The results from all the four oxidation processes were similar, if the samples were measured immediately, post growth. Samples evaporated with 2-5nm e-beam AlO_x were

observed to be more robust to changes in electrical properties (like induced superconducting hard gap) over time, and interfacial atomic structure was preserved at least six months after sample growth. Samples exposed to 100 Torr of O₂ in a load lock were found to be comparable after a few months, though a detailed aging study is still pending.

Degraded samples, oxidized using the other two approaches, showed deterioration in electrical performance with regards to induced superconductivity. Upon STEM-EDX analysis, some degraded samples showed the formation of an AlSb-like interfacial layer¹⁸.

5.5.4. *In-situ* nanowire shadow junctions

Now, with the optimum growth recipe established, the discussion must move on to the fabrication of Al-InSb nanowire devices. While superconductor-semiconductor heterostructures are required for the stabilization of MZMs, ohmic contacts, with normal metals, within tunneling distance are required for the measurement and probing of these MZM states. Therefore, while majority of the nanowire is required to have a continuous layer of aluminum on InSb, a break in the aluminum shell is required to form a “tunneling” contact. External gates could be used to deplete the nanowire (without the aluminum layers), forming a potential barrier, i.e. a tunneling contact. This tunnel barrier is essential for conductance spectroscopy measurements to probe the electronic structure of the super-semi system. Beyond the tunnel barrier, a normal metal contact is required to the InSb nanowire which would require the removal of aluminum from that region as well (see Figure 1.4).

¹⁸ AlSb is well known to oxidize and peel off in epitaxial 2D thin films, and the incorporation of small amounts of gallium (10-20%) is one way to inhibit the continued oxidation from the sidewalls. This approach is used when growing InSb and InAs quantum wells and has been described in Section 4.2.

With regards to device fabrication, for selective removal of aluminum from the surface of InSb, it was observed that no known wet chemical etches yielded optimal results. So, while the growth of Al-InSb was now established, removal of aluminum from InSb required attention.

A work around for the selective evaporation of aluminum was developed by S. Gazibegovic, et al., and has been described in detail elsewhere [81]. Starting with the surface of an (001) InP wafer, opposing (111)B facets are exposed by wet/dry chemical etching and covered in dielectric, and vias are opened where Au is evaporated on opposing (111)B facets. By intentionally introducing an offset between Au droplets patterned on the substrate, nanowires that miss each other, but point towards each other, could be grown (see Figure 5.17). A directional flux of metal atoms (like aluminum) could hence be blocked by the front wire, leaving behind a shadow or a break in the aluminum shell of the wire behind. This break in the aluminum shell due to the shadowing of one nanowire over the other now obviates the need for *ex-situ* lithography of the nanowire tunnel junction where a selective removal of aluminum was previously required.

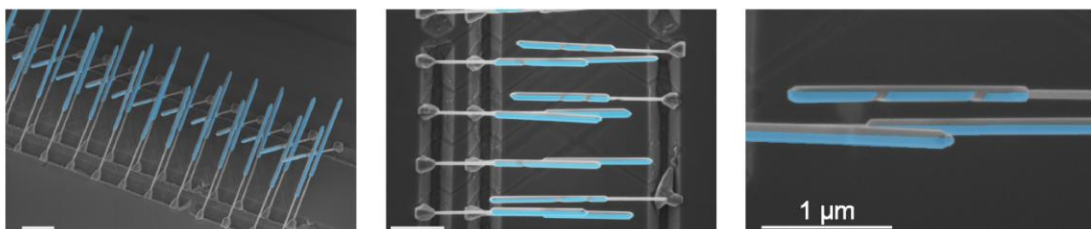


Figure 5.17 Left panel shows InSb nanowires on InP stems grown on opposing trenches. Blue is false colored Aluminum. Center panel shows how using two wires to shadow each wire, an Aluminum island could be made. A close of the same island on the third wire is shown on the right. Image courtesy – S. Gazibegovic, TU Eindhoven.

To summarize the growth and fabrication of Al-InSb heterostructures, the surface oxide formed on exposure to air was removed by atomic hydrogen cleaning, and the evaporation of aluminum outside of an MBE reactor in a dedicated cold stage allowed for the evaporation of

smooth thin films. Shadow evaporation of aluminum led to the formation of *in-situ* tunnel junctions for probing the superconductor-semiconductor system, an issue that could not be addressed by *ex-situ* lithography and processing. The above led to a smooth, atomically abrupt, epitaxial film of aluminum on InSb with large grain size and was confirmed by SEM and STEM.

5.5.5. Quantized Majorana Conductance

On aluminum on InSb nanowires, device fabrication and electrical measurements at 300mK and 20mK were performed at TU Delft, and superconductivity with an induced hard gap was observed for the first time in the InSb. Figure 5.18 shows the device geometry used for investigating induced superconductivity in the aluminum-InSb system. Suppression of sub-

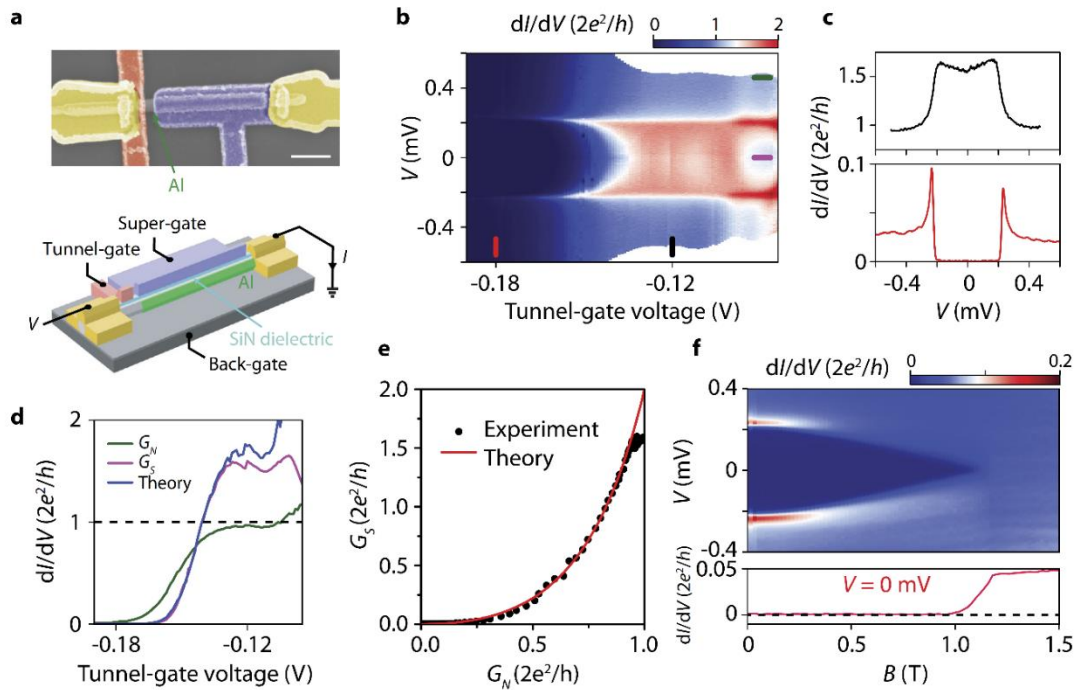


Figure 5.18 (a) False colored SEM image and device schematic of the device used to measure induced superconductivity in InSb with an Al partial shell. (b) Observation of a superconducting hard gap in tunneling conductance as tunnel-gate voltage is swept (c) cross section line cuts showing hard gap when in tunneling regime. (d) line cut along the gate sweep direction with conductance in the normal state above the gap and superconducting state below the gap, matching the predicted response (e) experimental and theoretical curves relating above gap and sub gap conductance in the induced superconducting gap regime (f) Evolution of the superconducting gap with in-plane magnetic field with vanishing superconductivity beyond ~ 1 Tesla.

Image source - Ref [185].

gap conductance was observed to be about three orders of magnitude, and 15nm-thick films with critical field of ~ 1.1 Tesla were measured in the first run. Upon reducing film thickness in later work, the critical field was increased. Initial results demonstrating induced superconductivity have been reported in [81], [186].

Armed with an induced superconducting “hard-gap” in InSb, a Majorana device was first fabricated from the Al-InSb nanowires by H. Zhang, et al. A zero bias peak indicative of Majorana Zero Modes was observed in the device, and to much surprise, was measured to be quantized to the value of $2e^2/h$ (see Figure 5.19). This observation by H. Zhang, et al., is considered to be the first observation of the predicted quantized Majorana conductance [186].

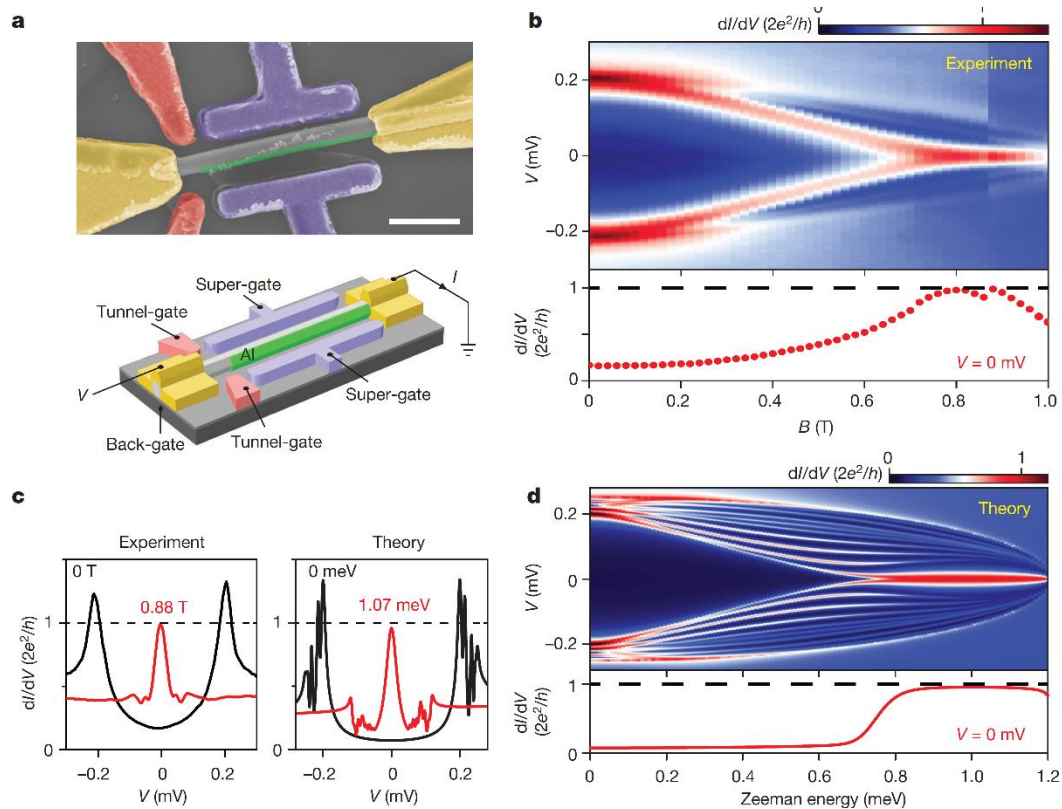


Figure 5.19 (a) Device geometry used to measure conductance spectroscopy response of Al-InSb nanowire under an in-plane magnetic field. (b) As the in-plane magnetic field is increased the Andreev Bound States at the edge of the gap merge to form a quantized zero bias peak that does not diverge. (c) line cuts at 0 Tesla and 0.88 Tesla showing quantized conductance peak which matched theoretical calculations and prior predictions. (d) simulated response of the conductance spectroscopy map showing comparable zero bias peak. Image source – Ref [185].

The predicted conductance value was observed in two independent devices. While the zero bias peak is believed to be of topological origin, non-topological sources, like Andreev bound states, cannot be completely ruled out [74]. Figure 5.19 shows the Majorana device geometry used to study the system, with line cuts of calculated and measured conductance data, at the quantized conductance value.

Upon changing the tunnel coupling into the nanowire, it was observed that the zero-bias peak reaches a quantized value of $2e^2/\hbar$, while the above gap conductance keeps on rising, indicating the increase in tunneling – i.e. increasing transmission through the tunnel barrier, while theory confirms the same. Figure 5.20 shows the results of experimental probes used study the predicted robustness to external perturbations of the zero-bias peak in this system. Based on the predictions, the zero-bias peak – being a charge-less, mass-less particle, energy-less, quasi-particle – should remain quantized and should not deviate from its quantized conductance value.

In order to measure and evaluate the outcome of braiding, one must look for the addition or removal of an electron – a fermion – formed by the fusion or annihilation of two MZMs [54]. Since the semiconductor is proximitized by the superconductor and has the superconductor-semiconductor hybrid system has a common superconducting gap, the electron thus formed or removed is expected to be ejected out of the system. Moreover, since all fermions within the superconducting gap have bosonized to form cooper pairs, the addition or removal of one electron is expected to change the parity of the superconductor.

Conductance spectroscopy of charge transport in/out of a superconducting island shows $2e$ periodicity (due to transport from cooper pairs) within the superconducting gap and $1e$ periodicity above the gap (due to transport from electrons, i.e. trivial fermions). Similar results were observed in the Al-InSb samples mentioned above, indicating the system is primed for the measurement of braiding outcomes (see Figure 5.21).

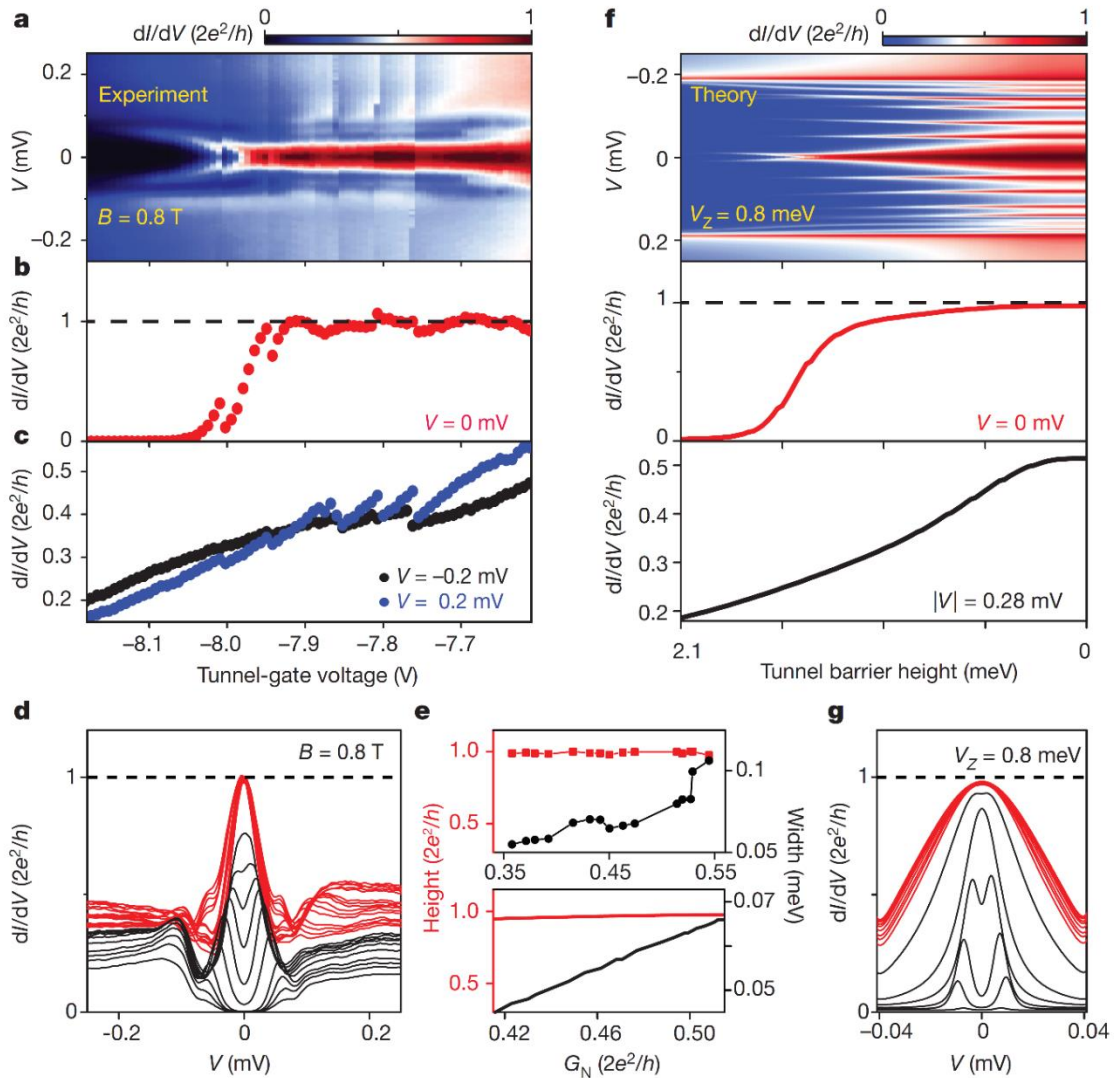


Figure 5.20 (a) Probing the zero bias peak by varying the tunnel gate voltage. The peak remains quantized even as above gap conductance keeps on increasing (b), (c) (d) line cuts showing the quantization with varying gate voltages at constant magnetic field (e) scaling of the width of the zero-bias peak while its height is quantized, matched with theory (f), (g) theoretical simulations of (a), (b), (c), (d).

Image source – Ref [185].

While it must be noted that parity transitions were first reported in the InAs-Al nanowire system by Albrecht, et al., and point to the effective “cleanliness” of the superconductor [96]. Zero-bias peaks with values close to the quantized value, have been claimed in Al-InAs 2DEGs by F. Nichele, et al., [187]. These complementary results on the Al-InAs system point to the importance of exploring multiple material systems in parallel.

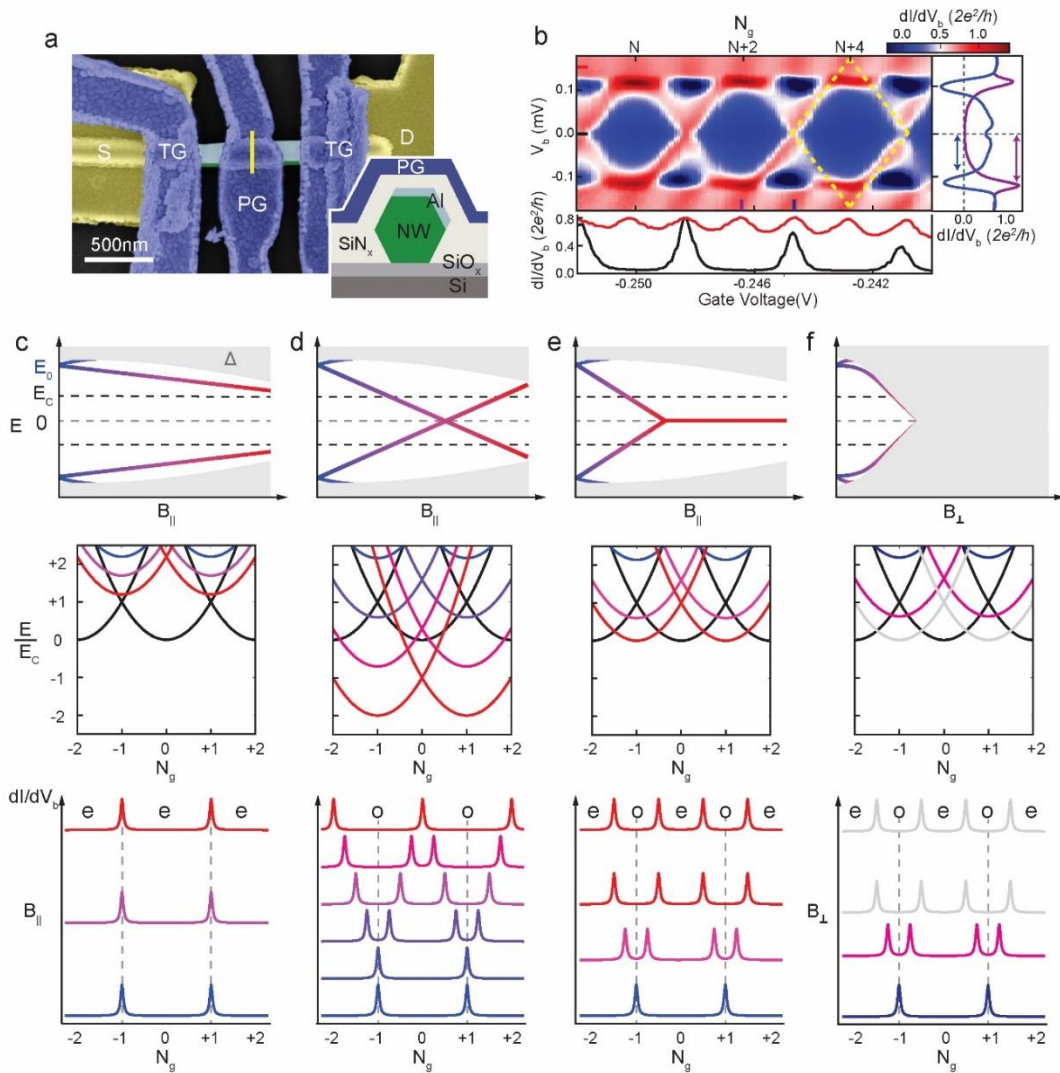


Figure 5.21 (a) device geometry used to measure the charge parity on the aluminum island. (b) the superconducting gap showing $2e$ periodicity with a $1e$ periodicity measured at the edges of the gap. Line cuts of the same are shown in the lower part (c)(d)(e)(f) evolution of bands, as measured by conductance spectroscopy and their influence on charge parity and periodicity. Image Source – Ref. [97].

With nanowires grown at TU Eindhoven, aluminum evaporated at UC Santa Barbara, and devices fabricated and measured at TU Delft, the Al-InSb VLS nanowire system remains the only nanowire system showing $2e^2/h$ quantized Majorana conductance as of this writing. Combined with the observation of parity transitions, Al-InSb nanowire system remains the platform of choice for the demonstration of braiding, Majorana fusion, non-abelian properties of MZMs – all necessary for making a topological qubit. Device geometries necessary for the demonstration of these characteristics have been reported in Chapter 7.

5.6. InSb SAG nanowires

Given the significant progress achieved with VLS InSb nanowires with epitaxial aluminum, attention can now turn to future work. One logical extension is advancing the system towards a scalable approach, like Selective Area Growth (SAG) to initially replicate the results seen on other materials platforms and then scale up those results towards realization of large area qubit arrays. Just such an endeavor to achieve Selective Area Growth of InSb on InP substrates was performed by MOCVD at TU Eindhoven by R.L.M. Op het Veld, followed by surface cleaning and aluminum evaporation at UC Santa Barbara. Device fabrication and measurements at low temperatures were performed in TU Delft. The results of this work are detailed in this section.

Since the SAG growth of InSb was performed on InP substrates, the significant lattice mismatch of about ~10% was expected to lead to an immediate relaxation of the InSb epi-layer

and to the formation of a very high density of dislocations¹⁹. Combined with the low effective mass of InSb, electron mobilities measured on InSb SAG grown on (111)B InP, were estimated to be of the order of $5\text{-}6 \times 10^3 \text{ cm}^2/\text{Vs}$. In comparison, typical mobility in the InAs/InP (001) SAG is between $1\text{-}3 \times 10^3 \text{ cm}^2/\text{Vs}$.

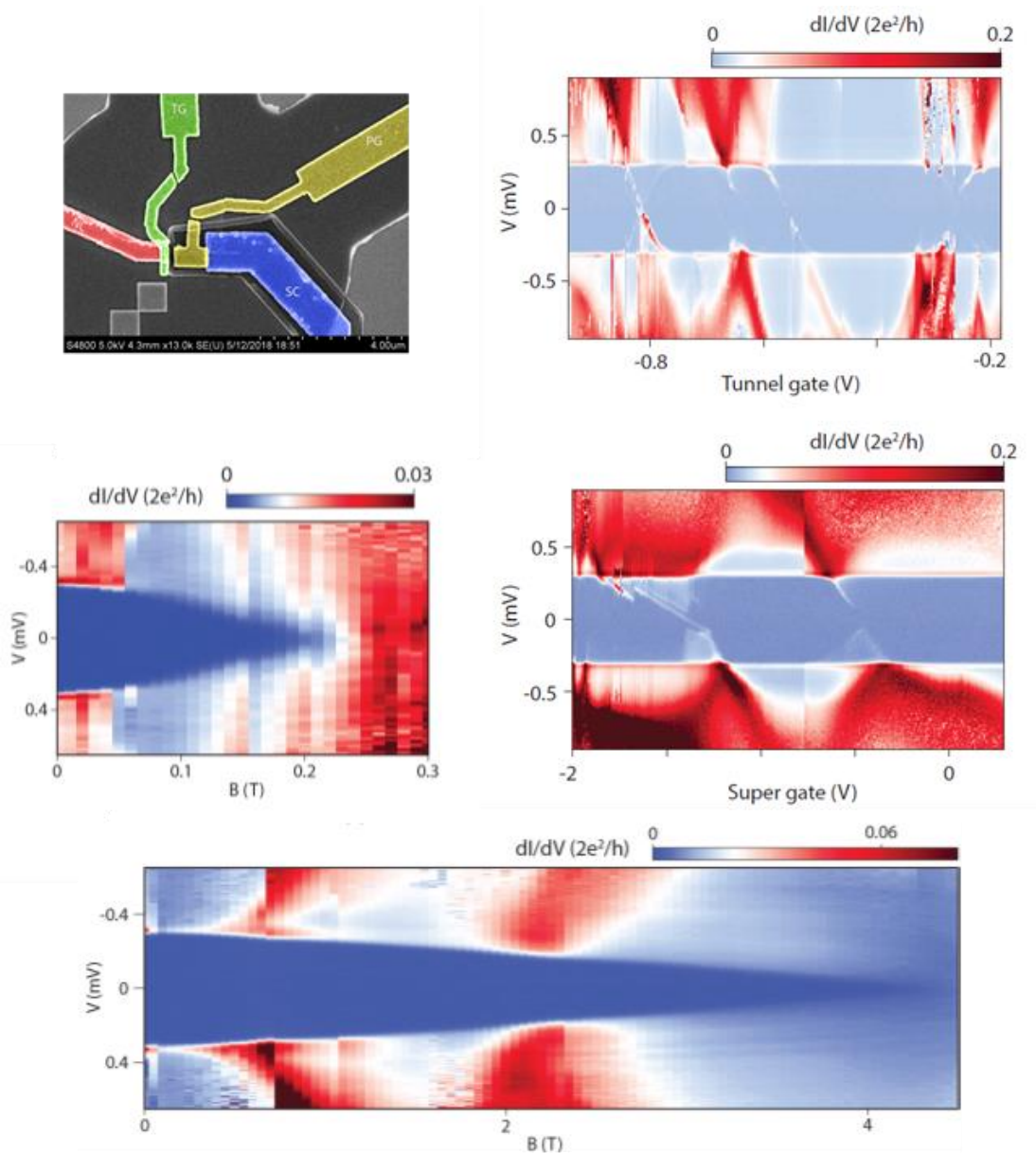


Figure 5.22 Clockwise from top-left: device geometry used to measure induced superconductivity in Selective Area Grown InSb with Aluminum evaporated on top. Top-right: Robust induced gap with variation in tunnel gate voltage. Center-right: Induced gap on variation on electron density in the SAG wire Bottom: Evolution of induced gap with in-plane magnetic field. Critical field above 4 Tesla is evident. Center-left: out-of-plane critical field of aluminum of about ~ 0.2 Tesla as expected. Image courtesy – H. Zhang, TU Delft.

Atomic hydrogen cleaning of the SAG InSb surface was performed with the same conditions as were used with 2D wafers and VLS nanowires. The only change in the process being the cleaning time. While VLS InSb samples were cleaned for 20 to 30 minutes, SAG samples were cleaned for 45 to 60 minutes.

Electrical measurements of induced superconductivity, showed an in-plane critical field of ~ 4.3 Tesla, corresponding to an aluminum film thickness of ~ 8 nm, which was the intended target (see Figure 5.22). The out-of-plane critical field is measured to be 0.2 Tesla. A device geometry similar to the VLS nanowires was chosen for the measurements with a tunnel gate controlling transmission through the tunnel barrier (fabricated by wet etching) and operating independently of a global (super) gate being used to tune the Fermi-level position in the wire. The induced superconductivity was observed to be robust to sweeping the transmission through the tunnel gate and on changing the super gate. With the demonstration of induced hard-gap superconductivity in InSb SAG, experiments in search for Majorana Zero Modes are under way as of this writing.

5.7. Conclusion

The development of atomic hydrogen cleaning of the InSb surface for growth at UCSB has helped tremendously in various aspects. This hydrogen cleaning was demonstrated to lead to a clean surface devoid of detectable oxygen and carbon. The process was utilized to clean

¹⁹ In the zinc-blende crystal structure, one of the slip planes for dislocations to glide is the (111) crystal plane [186]. If the substrate is chosen to be (111), then the dislocations formed along the [111] axis, and initially propagating along the [111] axis, along the surface normal, may under certain conditions, bend in-plane so as to glide in the (111) plane. Such a bend is energetically favorable since the slip-plane is (111). This work specifically reports on the growth of InSb on InP (111)B, and STEM images along the length of the nanowire confirm dislocations gliding in-plane beyond an initial thickness of a few nanometers. This bend and glide, allows for electron transport to occur in a thickness of the semiconductor largely free of dislocations, providing a significant relief from the heavily dislocated InSb-InP interface.

the surface of a device post nanofabrication to demonstrate the first regrowth of InSb on InSb. The growth of InSb quantum wells on InSb and GaSb substrates followed, accompanied by the observation of the highest reported quantum mobility to date an InSb quantum well. The top and bottom gate control of InSb quantum wells was also demonstrated.

Next, InSb VLS nanowires were hydrogen cleaned and epitaxial aluminum islands were evaporated to form pristine superconductor-semiconductor heterostructures, resulting in the long sought-after signatures of quantized Majorana conductance. Aluminum shells on InSb nanowires also showed $2e$ charge periodicity in the superconducting gap and $1e$ periodicity above the superconducting gap, indicating that the necessary building blocks for the realization of a topological qubit now exist. Lastly, InSb SAG structures with evaporated aluminum showed evidence of induced hard gap, while the observation of MZMs in SAG is still lacking.

6. Chapter 6 – InAsSb Quantum Wells (2D) and Wires (1D)

6.1. Introduction

As proposed by J. Sau, et al., [61], increasing spin orbit coupling in the host semiconductor nanowire is expected to lead to an increase in the induced topological energy gap (when a topological superconductor phase hosting MZMs is realized in the said nanowire). Certain compositions of $\text{InAs}_x\text{Sb}_{1-x}$ are predicted to have spin orbit coupling greater than the individual binary constituent compounds of InAs and InSb. The band gap of these compositions of InAsSb is correspondingly lower than the band gap of both InAs and InSb and can be attributed to band bowing (deviation from Vegard's law [102]). For $\text{InAs}_{0.35}\text{Sb}_{0.65}$, the band gap is predicted to be as low as 100 meV at 300K, in comparison to 172 meV for InSb and 354 meV for InAs (both at 300K) [145]. The bowing being very broadly spread over a

range of As/Sb ratios allows for compounds with As/Sb being 0.5/0.5 to 0.2/0.8 still being interesting (see Figure 6.1).

The g-factor of unstrained InAs is known to be about -15 while the g-factor of unstrained InSb is known to be about -55 [179]. The growth of InSb quantum wells on compressively strained AlInSb layers can unfavorably impact the g-factor as has been discussed in Chapter 5. On the other hand, the careful selection of AlInSb compositions to lattice match to InAsSb or to further tensile strain it, can on the other hand, further enhance the g-factor of InAsSb. Such potential for tunability is lacking in InSb due to the lack of III-Sb compounds to tensile strain the InSb quantum well layer. The effective mass of InAsSb is also, in principle, expected to be less than both the constituent compounds of InSb and InAs [179], while a direct measurement of both the g-factor and effective mass is lacking for specific compositions ($\text{InAs}_x\text{Sb}_{1-x}$; $0.5 > x > 0.2$).

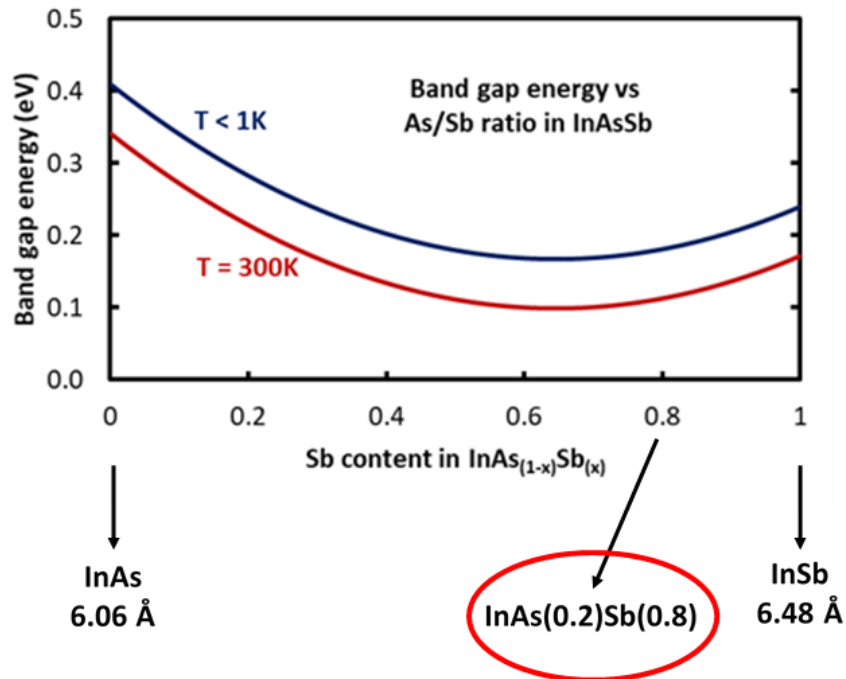


Figure 6.1 Band gap vs As/Sb ratio in InAsSb with band gaps at 300K and <1K. $\text{InAs}_{0.2}\text{Sb}_{0.8}$ system has been studied for quantum wells.

While the surface of InAs (001) is pinned in the conduction band (0.2 eV above the conduction band minima), and the surface of InSb (001) is expected to be pinned within the band gap [101], control over the As/Sb ratio in InAsSb, in-principle, allows for tuning of the Fermi level pinning position at the surface (see Figure 6.2). This key tuning parameter can be used to better understand superconductor-semiconductor coupling by controlling the electron transparency of the superconductor-semiconductor junction, making it more InAs-like or InSb-like.

This work demonstrates the MBE growth of InAs_{0.5}Sb_{0.5} nanowires with aluminum in Section 6.3 and InAs_{0.2}Sb_{0.8} quantum well structures in Section 6.2, for use as a platform for robust topological quantum computation.

Perhaps most importantly, InAsSb is predicted to form a 3D topological insulator (much like HgTe, sandwiched by CdTe) when sufficient in-plane bi-axial tensile strain is applied [188]. Coupling superconductivity to a 3D TI is predicted to give rise to MZMs providing an

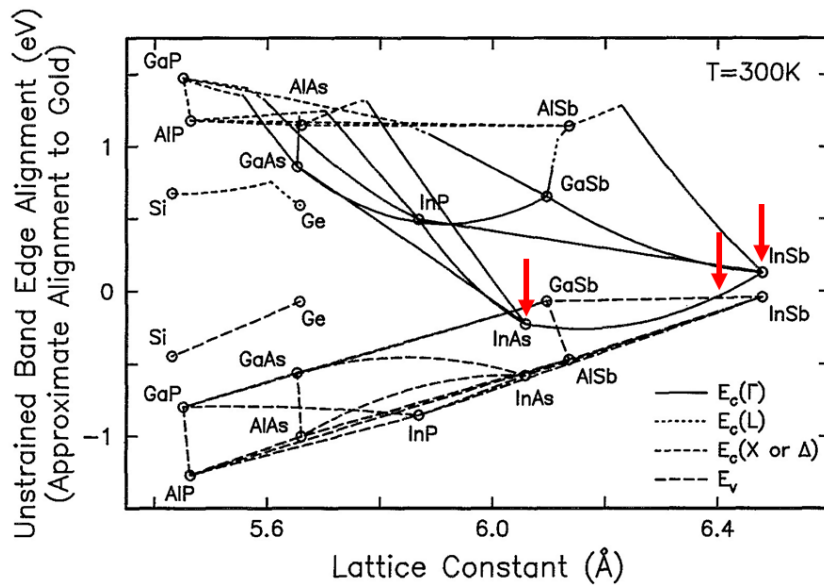


Figure 6.2 Band gap vs. lattice constant for III-V semiconductors with alignment to Au. 20% As in InAsSb is expected to make the fermi level be pinned very close to the conduction band edge. Image source – Ref [101]. Reprinted from S. Tiwari and D.J. Frank, *Apply. Phys. Lett.*, 60, 5, pp.630-632 (1992), with the permission of AIP Publishing.

alternate platform for topological quantum computation. Compressive and tensile strained layers of $\text{InAs}_{0.5}\text{Sb}_{0.5}$ have been grown and are awaiting angle resolved photo-emission spectroscopy (ARPES) analysis as of this writing.

6.2. InAsSb Quantum Wells

This section reports on the first reported demonstration of InAsSb quantum wells. MBE growth of InAsSb has been reported for use in mid-infrared photonics due to its lower band gap than InSb, which allows for accessing of significantly longer wavelengths than that of InSb [189]. In this work, InAsSb quantum well structures have been grown by MBE on GaSb and InSb (001) substrates. The depth of these quantum wells from the surface has been varied in order to study the influence of proximity from surface on electron transport.

As has been discussed previously, near surface quantum wells of materials with high spin orbit coupling are of special interest in quantum computing. This interest is because of the potential to couple superconductivity from a superconductor evaporated on the surface of the sample and thereby allow for the realization of MZMs in the superconductor-semiconductor hybrid system. An increase in spin-orbit coupling, compensates for reduction in mobility, with respect to the induced topological gap, as has been reported by J.D. Sau, et al [61]. Moreover, if electron mobility in highly spin-orbit coupled systems like InAsSb can be brought up to the level of InAs and InSb, the increase in spin-orbit coupling is expected to enhance the induced topological gap in InAsSb to a value much greater than possible in InAs and InSb [61]. Hence, InAsSb quantum wells, in theory offer robust topological protection and are a pathway towards realization of topological quantum computing.

6.2.1. Growth and characterization

In this work, $\text{InAs}_{0.2}\text{Sb}_{0.8}$ quantum wells have been grown on $\text{Al}_{0.3}\text{In}_{0.7}\text{Sb}$ buffer layers, where the composition of AlInSb was determined by individual group III fluxes calculated from RHEED oscillations prior to the growth, and the composition of InAsSb was determined post-growth by triple-axis X-Ray Diffraction (see Figure 6.3). The composition of the buffer layer was kept the same for all samples on both InSb and GaSb substrates. Additionally, structures with both step-graded and abrupt transitions in lattice constant to the buffer layer composition have been studied.

$\text{Al}_{0.3}\text{In}_{0.7}\text{Sb}$ is expected to compressively strain the $\text{InAs}_{0.2}\text{Sb}_{0.8}$ quantum well and unfavorably increase the in-plane electron effective mass, reduce the g-factor and increase the band gap. Further work to grow tensile strained films of InAsSb , with 35-50% arsenic, either on lattice matched or tensile strained AlInSb buffer layers, so that the maximum advantage of growth of InAsSb could be harnessed, is in progress as of this writing.

One potential drawback of InAsSb as compared to compounds like GaAs , InAs and InSb is ternary alloy scattering, with regards to electron transport in quantum well. While an ideal ternary compound is expected to have a uniform distribution of group V elements, fluctuations caused by MBE growth (non-uniform substrate temperature, non-uniform incident flux, absence of substrate rotation) could exasperate segregation and may lead to regions rich in InAs and InSb . In this work, no such non-uniformity was observed in TEM but compositional variations, measurable potentially by techniques like Atom Probe Tomography, cannot be ruled out. Quantum mechanically, a uniform periodic fluctuation is not expected to add to scattering, and this concept forms the basis for all of the following work on InAsSb .

The next several paragraphs will explain the conditions used for growing InAsSb structures. First, the thickness of InAsSb layers for all quantum wells was kept constant at 25nm. The growth temperature, as measured by a calibrated pyrometer, was maintained at 430°C during the growth of quantum wells and at 445°C during the growth of the buffer layers. Silicon doping layers below the quantum well were deposited at a temperature below 350°C,

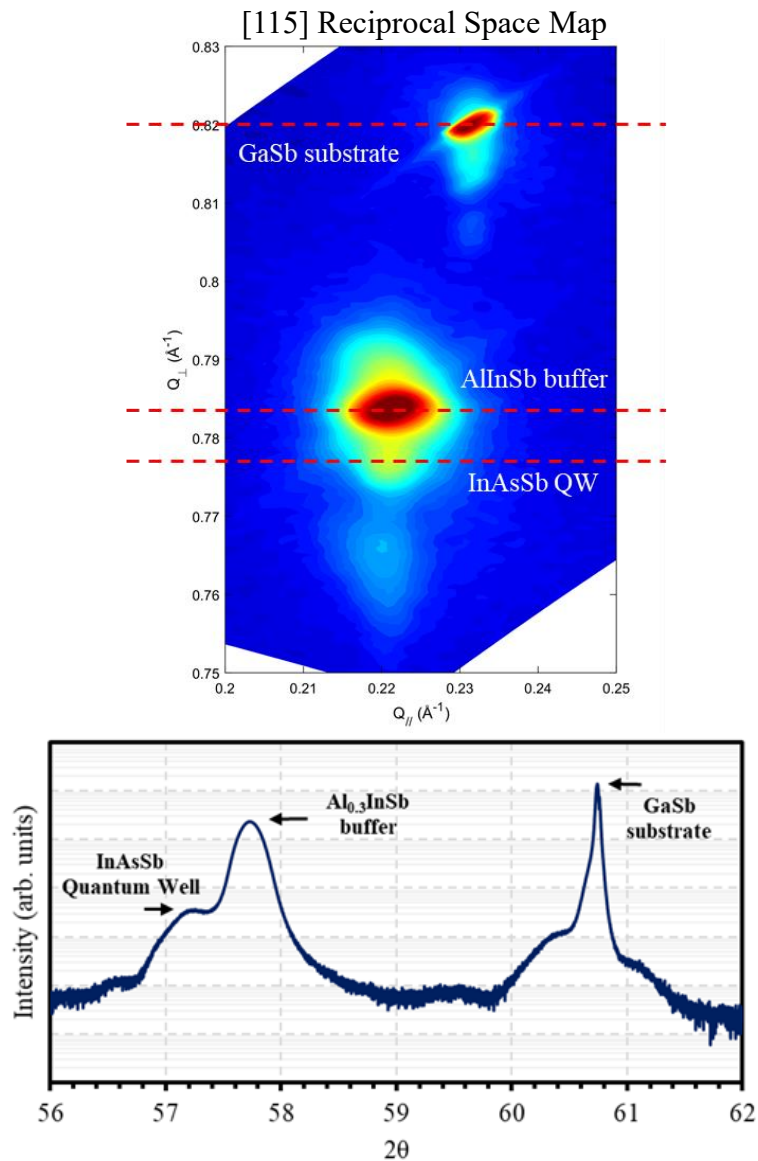


Figure 6.3 Top: Reciprocal space map of the [115] peak of the substrate and epi-layers in X-Ray Diffraction (XRD). Bottom: Triple axis XRD of the [004] peaks showing the InAsSb quantum well with respect to the AlInSb buffer and the GaSb substrate. The InAsSb quantum well layer is compressively strained by the buffer. Reciprocal Space Map (RSM) courtesy – H.S. Inbar, UCSB

under a Sb_2 over pressure, and a thin layer of AlInSb was grown at the low doping temperature to inhibit riding of the silicon up the growth front.

Prior to the growth of the quantum well layer, the growth of the complete structure is under a constant Sb_2 flux; however, an As_4 flux is used for the quantum well growth, with the As cracker at 500°C , along with an Sb_2 flux with the Sb cracker at 900°C .

Considering “incorporation ratio” adds another layer of complexity to the growth of compounds with high vapor pressure constituent elements. Incorporation ratio refers to the ratio of atoms of a particular species incorporated in the crystal as compared to the specific atomic flux. It could also be thought of as a perturbation of the sticking coefficient of the atomic species. When growing III-Vs, especially InAsSb, the sticking coefficient of As and Sb is not unity and the partial pressure of the individual species is not solely responsible for the final composition of the material grown. While indium has a sticking coefficient of unity, the flux of indium (i.e. the growth rate of the film), in part, determines the incorporation of arsenic and antimony. Substrate temperature also directly affects the sticking coefficients of arsenic of antimony, changing their incorporation ratios.

Changing various parameters will change the composition of the InAsSb layer, making the growth of uniform quantum wells a challenge. Among the more conventional means of changing composition are altering the incident flux of impinging species via either changing the arsenic or antimony valve positions or by changing the total flux (i.e. by changing the bulk evaporator temperature). An alternative approach is to change the “type” of impinging As and Sb species by changing the cracking zone temperature (i.e. selecting between As_4 , As_2 and As_1 ; and Sb_4 , Sb_2 and Sb_1).

To determine the optimum temperature for growth of InAsSb, it is assumed that InAsSb growth window will lie within the two extremes of InAs and InSb, with InSb defining the lower bounds for growth and decomposition temperature and InAs defining the upper bounds.

More details emerge as InAsSb quantum wells are examined closely. Figure 6.4 shows Transmission Electron Microscopy data of a 25nm InAsSb quantum well grown on a GaSb substrate, with inset showing a zoomed in view of the quantum well region. The dislocations are immediately apparent, the quantum well can still be observed to be uniform. 25nm below the quantum well where a doping layer should be, a brighter streak could be seen, which could be attributed to having a constant flux of antimony during the cool down to 350°C and growth of the doping layer. Indeed, since Sb has a very high sticking coefficient at 350°C, the presence of excess and unwanted antimony at that interface is expected. Corrections to the same need to be made in future structures.

For future growths of InAsSb quantum wells, it will be necessary to determine a capping layer that would lead to a stable surface that does not change the electron density or mobility over time (i.e. post-oxidation). As has been reported in Section 5.4, InSb quantum wells

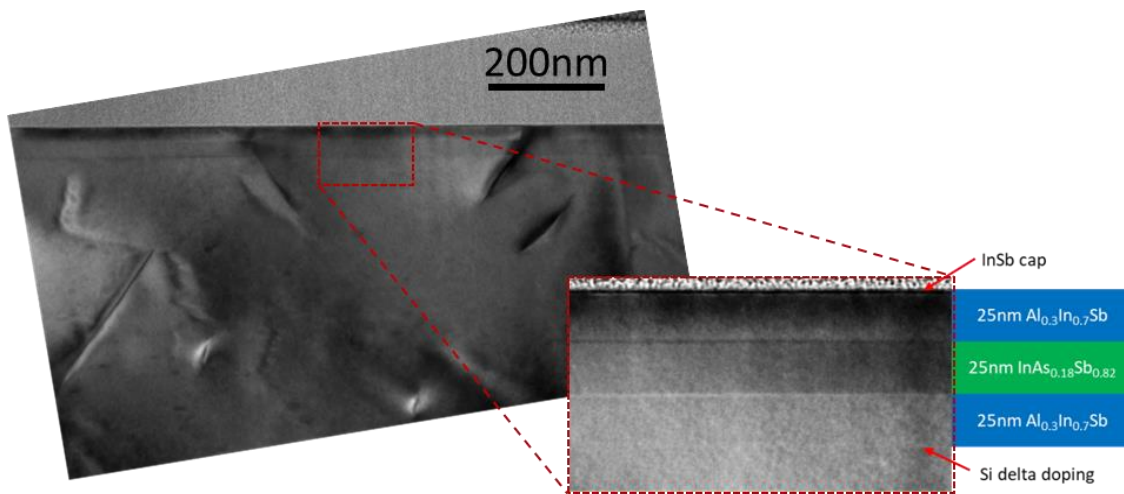


Figure 6.4 TEM image showing a 25nm deep InAsSb quantum well on a GaSb substrate with very high density of dislocations evident. Image courtesy – M. Seas, UCSB

showed reproducible results only with an InSb capping layer, and the incorporation of an aluminum-containing capping layer led to a significant susceptibility to post-growth annealing required for ohmic contact formation. Though structures with both GaAs and InSb capping layers were studied in this work, a larger sample space is necessary to draw reliable conclusions.

Meanwhile, the doping efficiency of Si donors was found to decrease upon reducing the depth from surface, with quantum wells that are closer to the surface having lower carrier concentration. This behavior could be attributed to the presence of a surface depletion layer for the chosen capping layer, or it could be attributed the As/Sb ratio in the InAsSb quantum wells (all of which had the same InAsSb composition) such that the conduction band minima in the InAsSb layer would be above the Fermi level if brought up to the surface. Figure 6.5 shows this relationship of depth of quantum well versus doping efficiency.

The 25nm-deep and 15nm-deep structures were used to fabricate gated hall bars with an ALD evaporated gate dielectric. With a GaAs cap, the 15nm-deep structure, showed an increase in electron density from about $1 \times 10^{11}/\text{cm}^2$ to about $5 \times 10^{11}/\text{cm}^2$ post-device fabrication. On the other hand, no change in electron density post-device fabrication was observed for the 25nm deep sample, which had an InSb cap. Whether this change in electron density was due to the increased susceptibility of a near surface well to dangling bonds at the interface, or lattice mismatch/dislocations, or the ALD dielectric or whether the GaAs cap layer lead to an increase in the electron density, needs to be studied further with more growths of near surface wells with an InSb cap layer.

The 15nm and 25nm deep structures were both “inverted” quantum wells with the silicon dopant levels incorporated below the 25nm-wide quantum well and separated by a 25nm spacer. While it needs further investigation, electron mobility in the inverted quantum wells may be limited by riding of silicon dopants up the growth front, even at the low doping temperature, leading to a significant reduction in mobility [190]. As the doping efficiency is less than 100%, a dopant-free structure would lead to a depleted quantum well, but it might allow for a definitive answer to the question of how dopants impact electron mobility.

Gate control of electron density in the quantum well (see Section 6.2.2) has demonstrated tuning of electron population in the well from full depletion to occupation of the first sub-band and it may be necessary to study undoped structures.

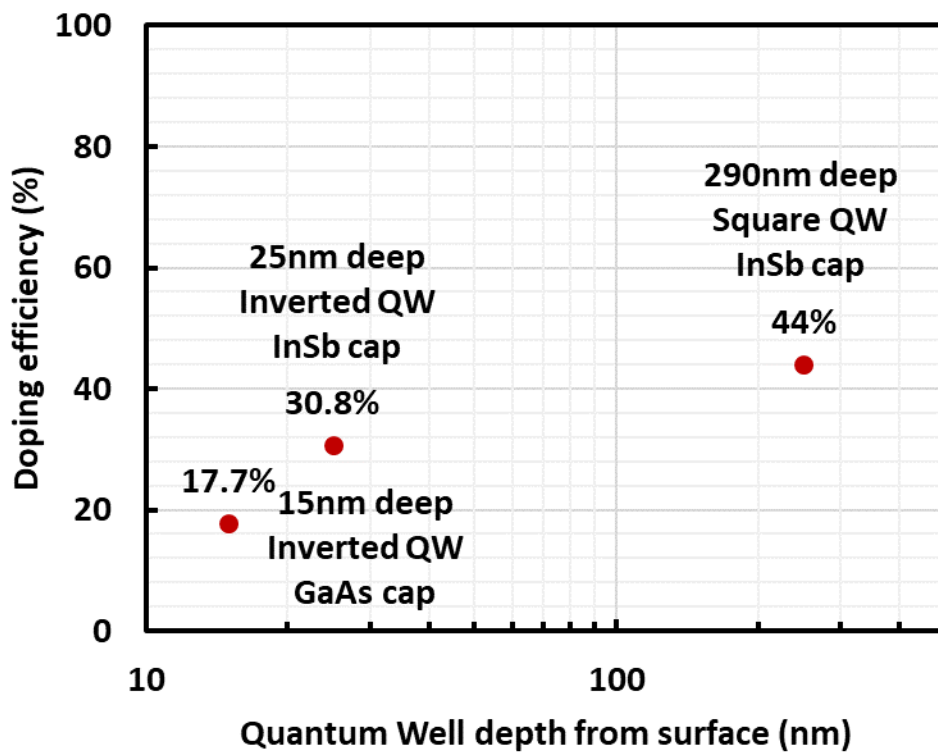


Figure 6.5 Doping efficiency of silicon dopants in InAsSb quantum wells, as the depth of the quantum wells is varied from the surface. A reduction in doping efficiency indicates the presence of a surface depletion layer.

Lastly, Atomic force microscopy of the same sample confirms the presence of a high density of mounds, and a rough surface with a peak-to-peak roughness of 12.5nm (see Figure 6.6). This topography is similar to the observed topography of InSb quantum wells on GaSb substrates and is expected for the significant lattice mismatch between the GaSb substrate and the $\text{Al}_{0.2}\text{InSb}$ buffer layer.

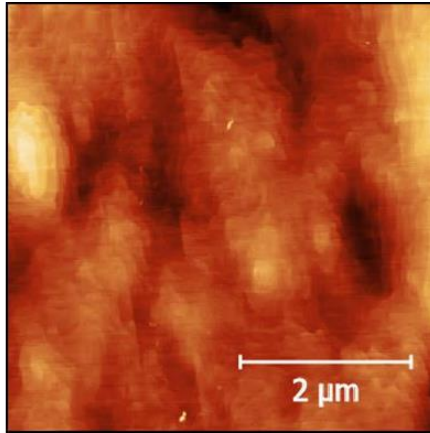


Figure 6.6 AFM image of an InAsSb QW with peak to peak roughness of 12.5 nm. The high roughness is expected due to the significant lattice mismatch as compared to the GaSb substrate

6.2.2. Low-temperature magneto-transport measurements

This section will discuss the magneto-transport results measured on InAsSb quantum wells. InAsSb quantum wells with varying depths from the surface were studied from 2K to 10K (see Figure 6.7). It was observed that all quantum wells grown on GaSb substrates showed Integer Quantum Hall Effect with pure 2D electron transport, which was indicated by R_{xx} minima attaining zero resistance and a single slope in R_{xy} . The electron density in the quantum wells was found to vary with depth as has been described in the previous section. The decay in amplitude of the SdH oscillations with increasing temperature can be used to estimate the

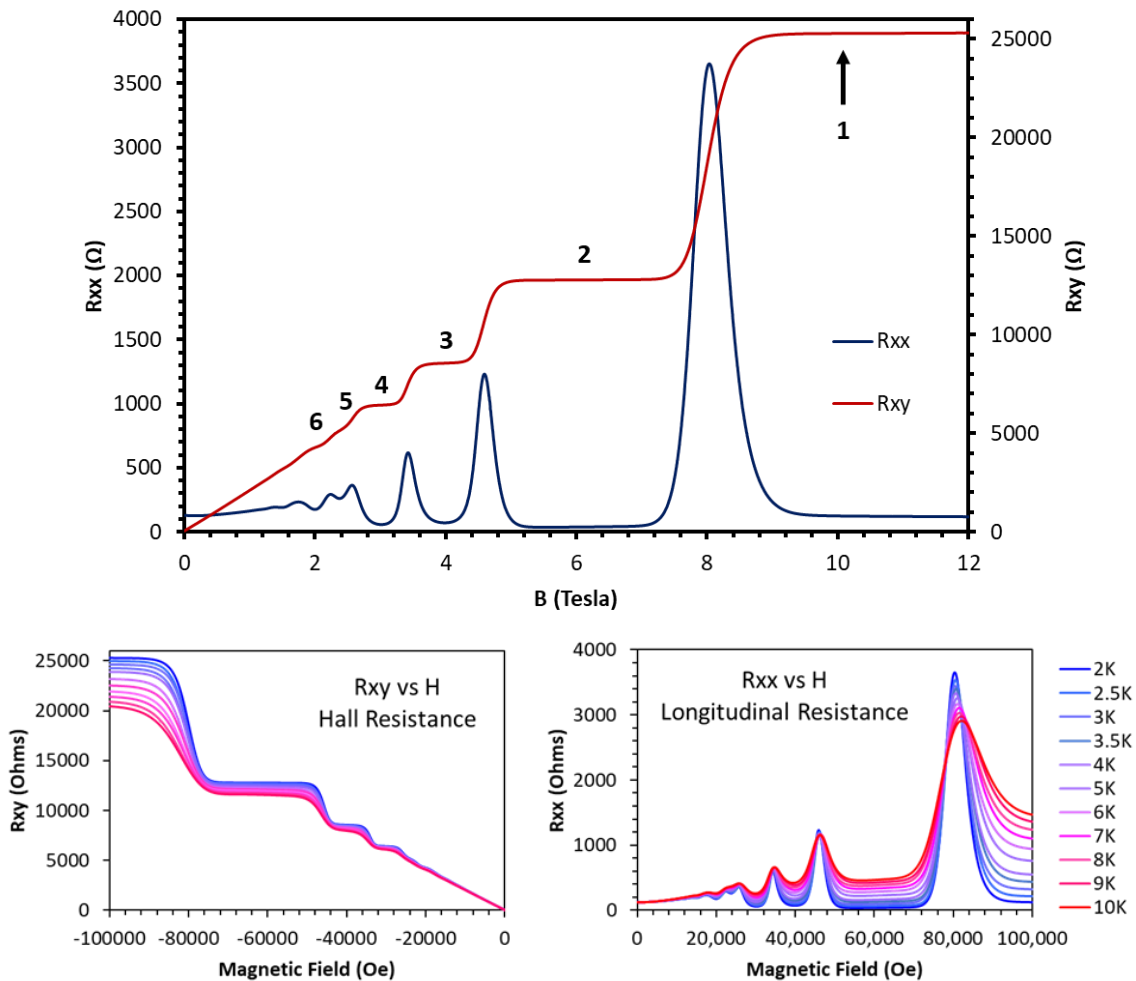


Figure 6.7 The top panel shows the Integer Quantum Hall Effect seen in a 25nm InAsSb QW at 2K. the bottom panel shows the variation of R_{xx} and R_{xy} as the temperature is varied from 2K to 10K.

effective mass of the electrons in the channel [191]. InAsSb quantum wells grown on an InSb substrate showed signatures of Integer Quantum Hall Effect at high magnetic field while the low field data was overwhelmed by parallel conduction through the buffer layers/substrate (see Figure 6.8).

Further work is required to make InAsSb quantum wells with higher electron mobility on both InSb and GaSb substrates. Efforts to remove parallel conduction are also required to be undertaken on InSb substrates.

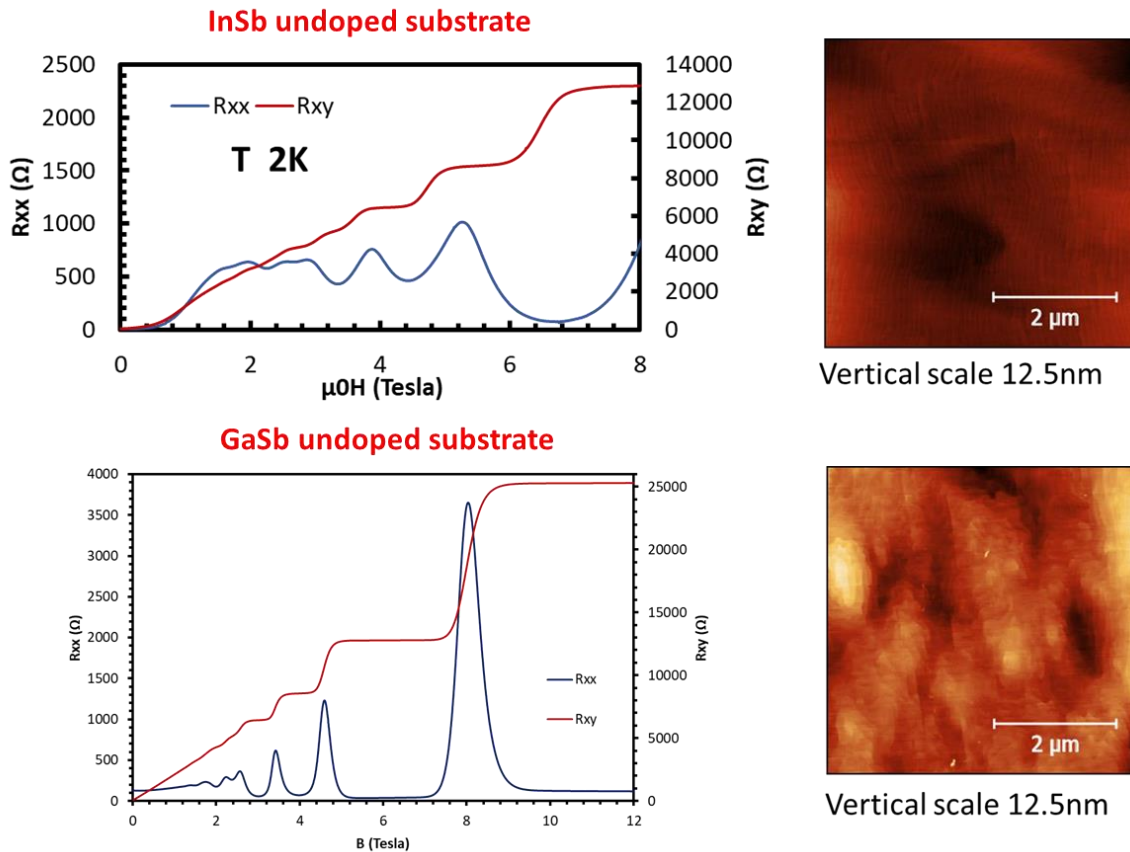


Figure 6.8 The top panel shows AFM and Quantum Hall results from an InAsSb QW grown on an InSb substrate. The low field data shows the presence of a parallel conduction path. The lower panel shows InAsSb QW on a GaSb substrate where no parallel conduction path is observed. QW on InSb is smoother as compared QW on GaSb.

6.2.3. Quantum Point Contact

In this section, we report the first demonstration of a quantum point contact on an InAsSb quantum well. This section will discuss the phenomena associated and analyze the results obtained.

A Quantum Point Contact (QPC) is formed by pinching off a 2D channel by using two sharp gates, such that conduction is restricted to a quasi-1D limit. QPCs allow for a direct probing of the electronic levels in a material system being probed [192]. When starting with a 2D electron gas, upon pinching the channel from 2D to 1D, using the side gates forming the QPC, steps in the source-drain resistance are expected to be observed. On subtracting a parasitic resistance, referred to as the channel resistance, which varies from device to device and also varies with applied magnetic field, the steps observed in resistance are expected to be multiples of the fundamental quantum of conductance $2e^2/h$ (G_0). In this work, both 15nm and 25nm-deep InAsSb quantum wells, showed expected quantized steps in conductance in a QPC device. The channel resistance subtracted in this study was a positive value and was attributed to a series resistance being added to the 1D channel on either side of the constriction though there remains a possibility that the channel resistance is negative²⁰.

As has been discussed in prior sections (see Section 1.3.1), a helical gap can be directly measured in a 1D limit of a 2DEG by using a QPC, when conductance through a point contact drops from the spin degenerate $4e^2/h$ ($2G_0$) to $2e^2/h$ (G_0) for the energy of the helical gap. The

²⁰ There have been reports of a negative channel resistance also being observed [215], which could be attributed to a system with an extremely long electron coherence length such that part of the electron wave injected from the source is reflected to it and only part of the wave is transmitted. This reflection would lead to a net negative channel resistance, which is in effect a resistance that gets added to the measured resistance between source and drain to “make” the conductance steps align with the quantized conductance values.

conductance is again expected to shoot up to $4e^2/h$ and continue increasing as more channels are added and transport becomes two-dimensional again. This helical gap is a pre-requisite for topologically protected Majorana Zero Modes, and the larger the helical gap, the stronger the topological protection, coupled with an s-wave superconductor under an applied magnetic field. Reports on observation of such a helical gap exist but are marred with noise [193].

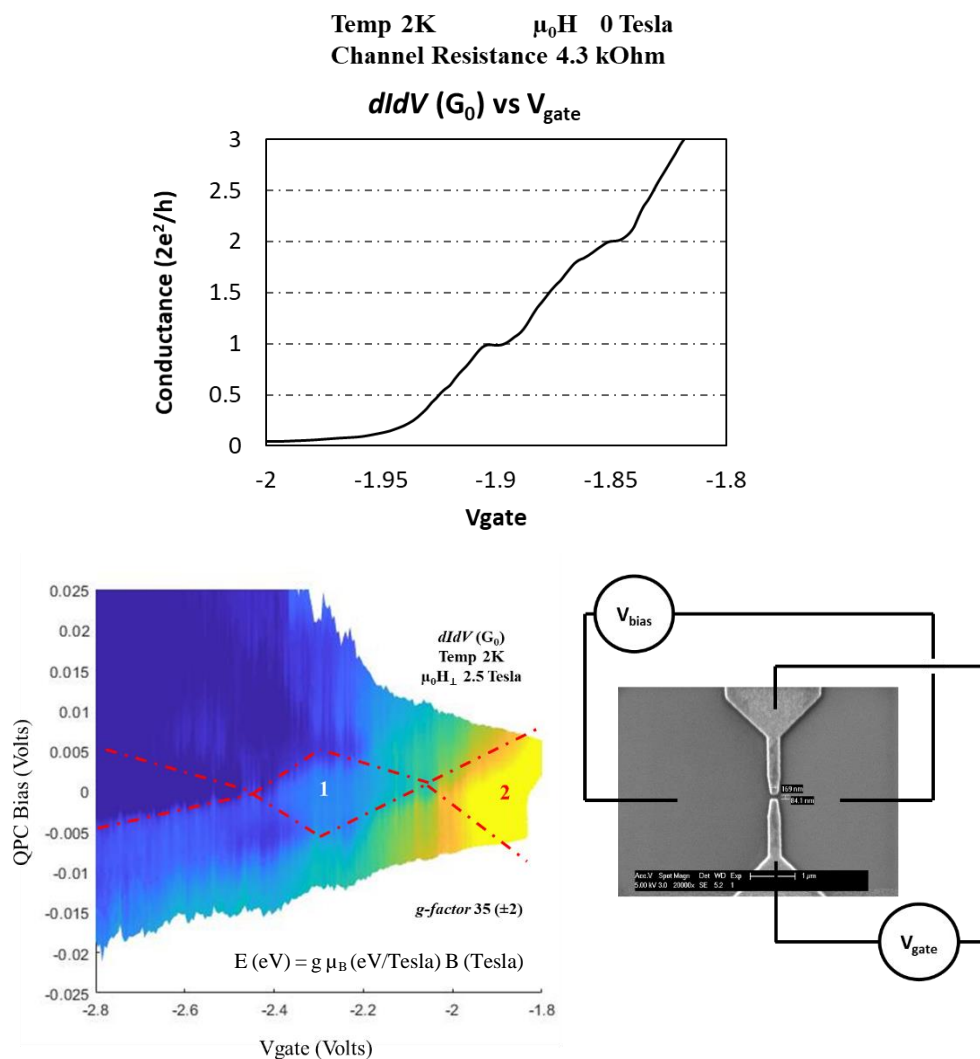


Figure 6.9 Top: Line cut of QPC at zero magnetic field in a 25nm deep InAsSb quantum well.. Bottom Left: Bias spectroscopy map of the same QPC at 2.5 Tesla field, showing the energy spread of the first conductance plateau. The extracted g-factor is 35. Bottom right: SEM of the device used for this QPC measurement with a contact separation of ~ 85 nm.

As spin-degeneracy is lifted, under an applied magnetic field, conductance quantization of e^2/h ($0.5G_0$) and multiples thereof appear due to spin-splitting. This spin-splitting is proportional to the applied magnetic field and the electron g -factor and can be observed by performing a conductance spectroscopy map by varying the source-drain bias (see Figure 6.9)²¹.

In this work, the channel width was kept at ~ 80 - 200 nm, depending on the device and was defined by Electron Beam Lithography (EBL)²². The plot of rate of change of conductance with respect to the QPC's gate voltage (dG/dV_{gate}), when plotted versus source drain bias (V_{bias}) and QPC gate voltage (V_{gate}) reveals diamond like features indicative of conductance transitions and in effect the energy separation (measured by V_{bias}) with respect to zero energy, for the G_0 plateau transitioning to a higher conductance plateau can be used to calculate the g -factor. The estimated g -factor from was measured to be 35 ± 2 (see Figure 6.9). This value is less than the expected value for unstrained $\text{InAs}_{0.2}\text{Sb}_{0.8}$ but can be attributed to the compressive strain due to growth on $\text{Al}_{0.3}\text{In}_{0.7}\text{Sb}$ buffer layer, leading to a reduction in g -factor. For confirmation, further measurements at lower temperature and with varying magnetic fields, along with a correlation from g -factor measured from tilted field measurements, are required.

6.3. InAsSb VLS nanowires

InAsSb quantum wells remain a viable option for the realization of MZMs and also for the exploration of electron phenomena in highly spin-orbit coupled 2D electron systems.

²¹ A key feature that yet has remained an enigma is the observation of conductance plateau at $0.7G_0$. As no sum of individual electron channels ($0.5G_0$ conductance) can lead to the sum of 0.7 , this feature is believed to arise from electron-electron interactions akin to the fractional quantum hall effect [216]. The 0.7 plateau has not been observed in the InSb quantum well and wire system but is routinely observed in GaAs QPCs and more recently in InAs QPCs [148].

²² Quantum Point Contact device fabricated by J.S. Lee, Palmstrøm Lab, UCSB.

However, the lack of a lattice matched substrate for the growth of InAsSb quantum wells, leads to implementations that would always remain sub-par. This section will discuss the advantages of the InAsSb VLS nanowires and discuss their growth in detail.

First, the one-dimensionality of the InAsSb nanowires gives it certain advantages over the InAsSb quantum well. In an ideal VLS nanowire growth, lattice relaxation is almost immediate due to small x-y dimensions along the cross-section of the nanowire and comparatively longer z-axis dimension by at least an order of magnitude (~100nm diameter as compared to >1 μ m length). Such an asymmetry in the in-plane and out-of-plane growth axis allows for many dislocations to reach the edge of the nanowire during the initial few hundred nanometers of growth. Thus, the remainder of the length of the nanowire can often be dislocation free. In comparison, the in-plane dimensions are much larger (>1mm in-plane as compared to >1 μ m growth in z-axis) for growth on 2D surfaces, and dislocations formed at the lattice mismatched interface, propagate through the active quantum well layer, impacting

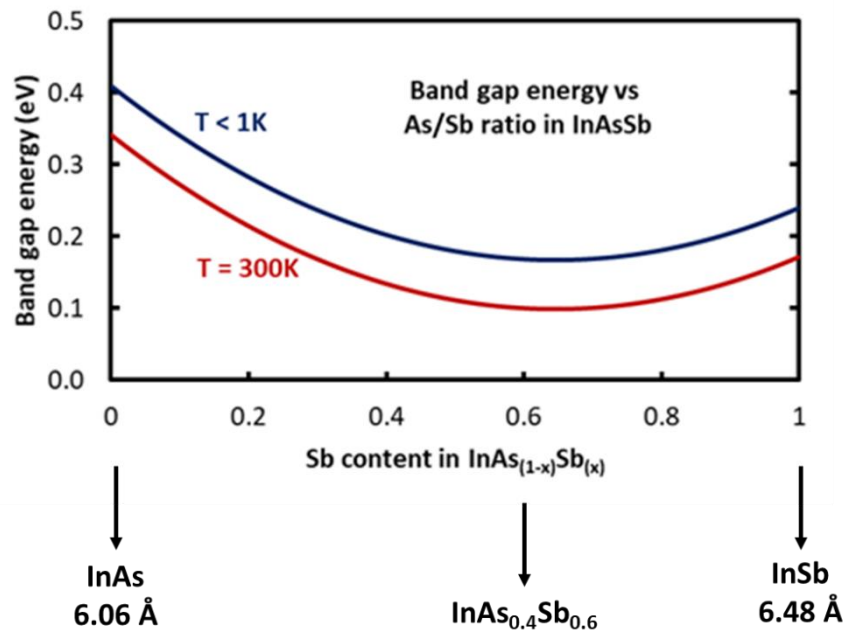


Figure 6.10 Band-gap vs Sb content in InAsSb, showing InAs_{0.4}Sb_{0.6}, the composition chosen for VLS nanowires

electron transport. Due to these properties and to their relatively pristine crystal quality, 1D VLS nanowires of InAsSb are hence a much more suitable platform for study of 1D electron transport than quantum wells.

While InSb and InAs nanowires have been studied in-depth for the demonstration of Majorana Zero Modes, observation of MZMs in InAsSb VLS nanowires remains an outstanding challenge. Growth of InAsSb nanowires has been previously reported [194]–[196] with a focus on applications in photonics and nanowire FETs. As has been described previously, advantages of InAsSb are its small band gap, increased spin-orbit coupling and potential for higher electron mobility due to reduced effective mass (see Figure 6.10). When combined, these two properties should lead to an increase in the induced topological gap in an InAsSb semiconductor host than in InAs or InSb. This increased induced topological gap should in turn lead to an enhanced topological protection in InAsSb as compared to InAs and InSb.

To use of InAsSb nanowires as a new platform for topological quantum computation, some key requirements first need to be demonstrated. Specifically, these requirements are 1) the growth of long nanowires with uniform ternary composition, 2) full depletion of the nanowire under an applied gate voltage, and 3) the demonstration of induced superconductivity.

Apart from the advantage of having a large induced topological gap, InAsSb nanowires also have a larger g -factor and therefore induced superconductivity in InAsSb nanowires is expected to transition from trivial to topological superconductivity (onset of MZM zero-bias peak) at a much lower in-plane magnetic field than InAs or InSb. A further advantage is that

the Fermi-level pinning on the surface of InAsSb is expected to vary from surface depletion (InSb like) to surface accumulation (InAs like) as the composition is varied. This ability to tune the pinning position, by tuning the composition allows us to determine the optimum Fermi-level position, for the most suitable superconductor-semiconductor coupling.

Lastly, the advantage of transparent coupling and complete wavefunction overlap in the InAsSb nanowire is a strong induced superconductivity. However, these properties are also known to reduce the effective g-factor of the hybridized system, as the g-factor of aluminum is +2, while the g-factor of InAs and InSb is -15 and -55, respectively. A poorer coupling, on the other hand, allows for an improved g-factor but leads to a reduced induced superconducting gap, effectually reducing the induced topological gap. This is also detrimental to the system. Recent work by M. de Moore, et al., on InSb-Al samples grown as part of this dissertation, demonstrates electric field tuning of superconductor-semiconductor coupling [197].

This section reports specifically on MBE growth of long InAsSb nanowires with uniform composition. In this paragraph, the properties of these nanowires will be elaborated upon. First, these nanowires demonstrate full depletion under an applied gate voltage. A break in the aluminum shell was introduced by using a nanowire to shadow another during aluminum evaporation. Induced superconductivity was observed in these long InAsSb nanowires with critical field in excess of 4 Tesla. Recent work by P. Krogstrup, et al., also demonstrates growth of InAsSb nanowires with induced superconductivity [198], though observation of MZMs remains elusive.

1D nanowires of InAs typically suffer from a high density of stacking faults, which due to very small energy difference between the stability of the two phases, leads to a change in crystal structure from zinc-blende to wurtzite and back to zinc-blende. InSb nanowires, on the other hand, are always phase pure, in the zinc-blende crystal structure. This phase purity, coupled with the lower effective mass of InSb and the presence of a surface depletion layer which may provide inherent dielectric screening, is a distinct advantage. Furthermore, InSb nanowires exhibit a significantly enhanced peak electron mobility of up to $\sim 4 \times 10^4 \text{ cm}^2/\text{Vs}$. InAsSb nanowires, on the other hand, transition from a phase unstable InAs-like crystal structure to a phase pure zinc-blende structure, like InSb, as the ratio of As to Sb is varied. Therefore, this work focuses not just on general MBE growth of long InAsSb nanowires, but specifically on the MBE of phase pure, zinc blende $\text{InAs}_{0.4}\text{Sb}_{0.6}$ VLS nanowires by MBE.

While observation of these stacking faults and changes in crystal structure from zinc-blende to wurtzite is apparent in HAADF-STEM, accurately determining the composition of the ternary compound is non-trivial. In this work, the composition of the nanowire is determined by estimating the intensity of As/Sb in *in-situ* EDX mapping in HAADF-STEM. The uncertainty in determining nanowire composition is estimated to be about $\sim 10\%$, and EDX

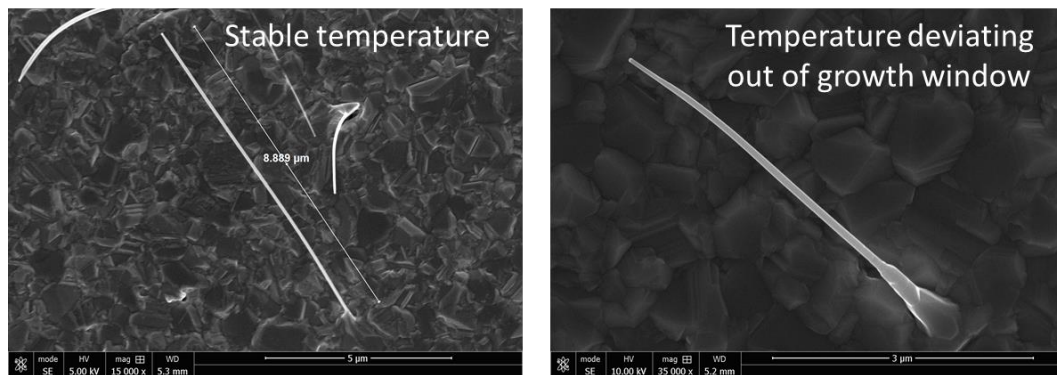


Figure 6.11 Left panel shows InAsSb nanowire grown with a constant temperature showing long straight nanowire. The right panel shows a nanowire when the temperature deviated out of the growth window near the end of the growth, leading to a bend in the nanowire.

spectra of known composition materials would be needed to further reduce the error. The composition of $\text{InAs}_{0.4}\text{Sb}_{0.6}$ was the target composition, as it is expected to have the highest g-factor and lowest band gap of III-As,Sb compounds.

The next several paragraphs will discuss the methods used to grow the InAsSb nanowires in this work. Starting with a (100) InP substrate and, with prepatterned Au droplets, a nucleation layer of $\sim 200\text{nm}$ long InAs VLS nanowires was nucleated at a temperature of $445\pm 10^\circ\text{C}$. The indium flux was chosen to be equivalent to a planar growth rate of 100 nm per hour which led to a nanowire growth rate of $\sim 2\mu\text{m per hour}$ for nanowires nominally $\sim 50\text{nm}$ in diameter. An As_4 flux was used throughout the growth. Upon growth of the $\sim 200\text{nm}$ stem of InAs on InP substrate, the substrate temperature was then lowered to $435\pm 10^\circ\text{C}$ and antimony was opened with a primarily Sb_2 flux. The growth of InAsSb by this method was

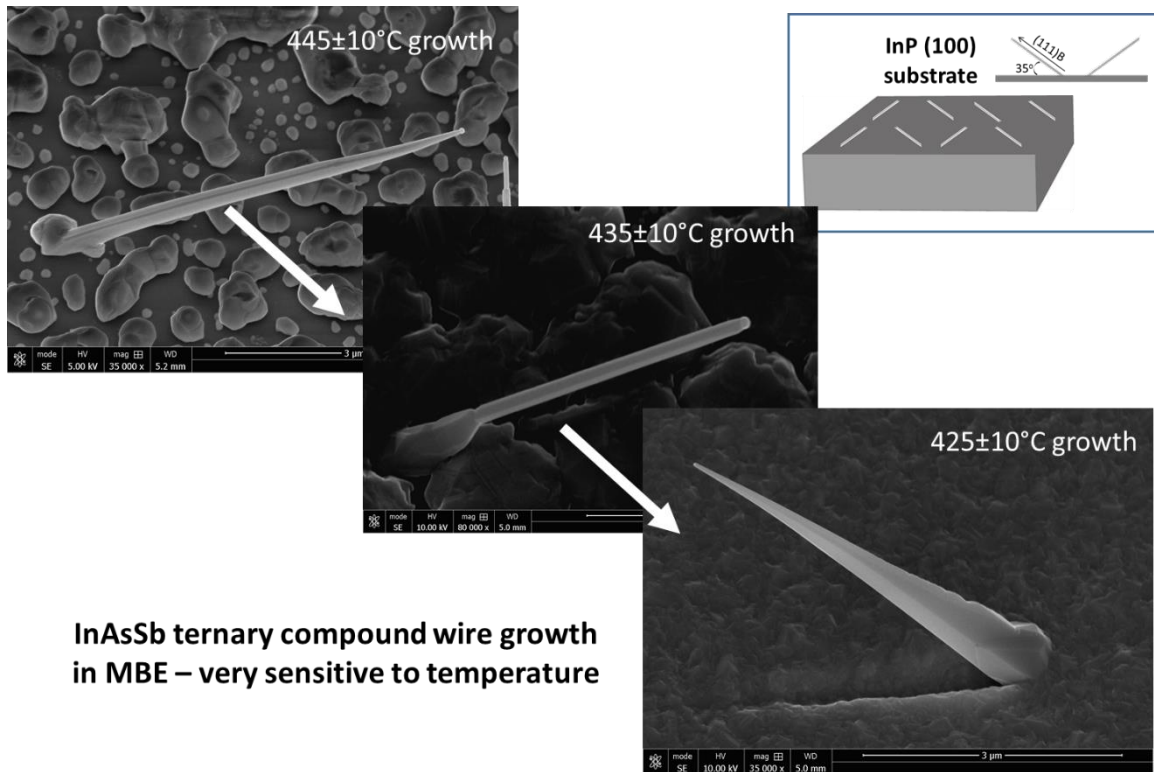


Figure 6.12 The very small growth window for achieving the right composition of growth is shown above. The top left image shows a nanowire at higher growth temperature while the bottom right is lower temperature than the ideal temperature. The center SEM image shows nanowire grown exactly at the temperature required for growth of this composition.

observed to be slightly faster than growth of InAs, which, given the unity sticking coefficient of indium, could be attributed to the larger lattice constant of InAsSb.

Maintaining a steady growth temperature was found to be essential to get straight InAsSb nanowires. Since the relative incorporation ratios of arsenic and antimony are exponentially dependent on temperature, a $>5^{\circ}\text{C}$ average deviation from the growth temperature led to tapered wires or if the change in temperature occurred during the growth itself, bent wires (see Figure 6.12). Shutter transients from opening/closing the shutter for antimony (with the cracker at $900\text{-}1000^{\circ}\text{C}$) were about $2\text{-}5^{\circ}\text{C}$ and reduced as the surface was covered in absorbing III-V. This gradual deviation in measured temperature added to the challenge of maintaining a $<5^{\circ}\text{C}$ deviation from the real sample temperature for long growths, as evidenced in Figure 6.12. $8\mu\text{m}$ nanowires required growths of four hours, not including warmup, nucleation of InAs and

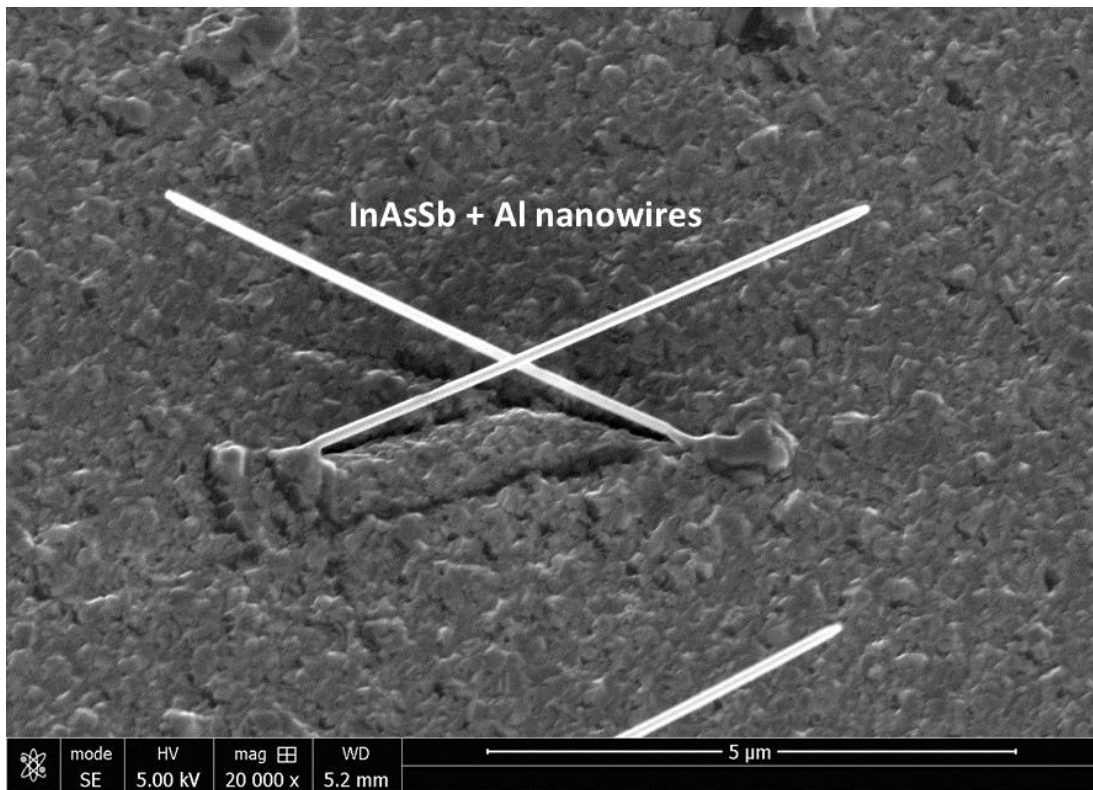
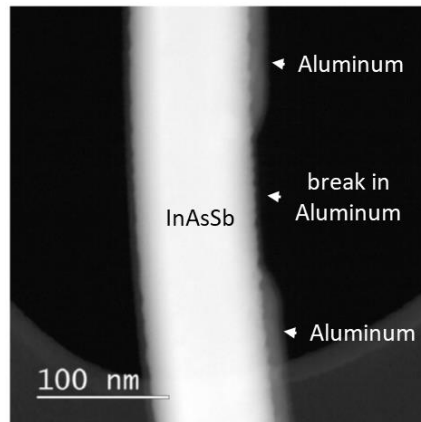


Figure 6.13 Two InAsSb nanowires growing opposite to each other on a (001) InP substrate, such that they miss each other intentionally. One nanowire has been used to shadow the another leaving behind an in-situ grown island of aluminum.

cooldown time. A long length of nanowires – covered by a continuous Aluminum segment, creating a long topologically superconducting section – is expected to be necessary for well separated MZMs. This separation is in turn necessary to prevent dephasing of Majorana qubits [199].



HAADF STEM of InAsSb nanowire with *in-situ* epi-Aluminum

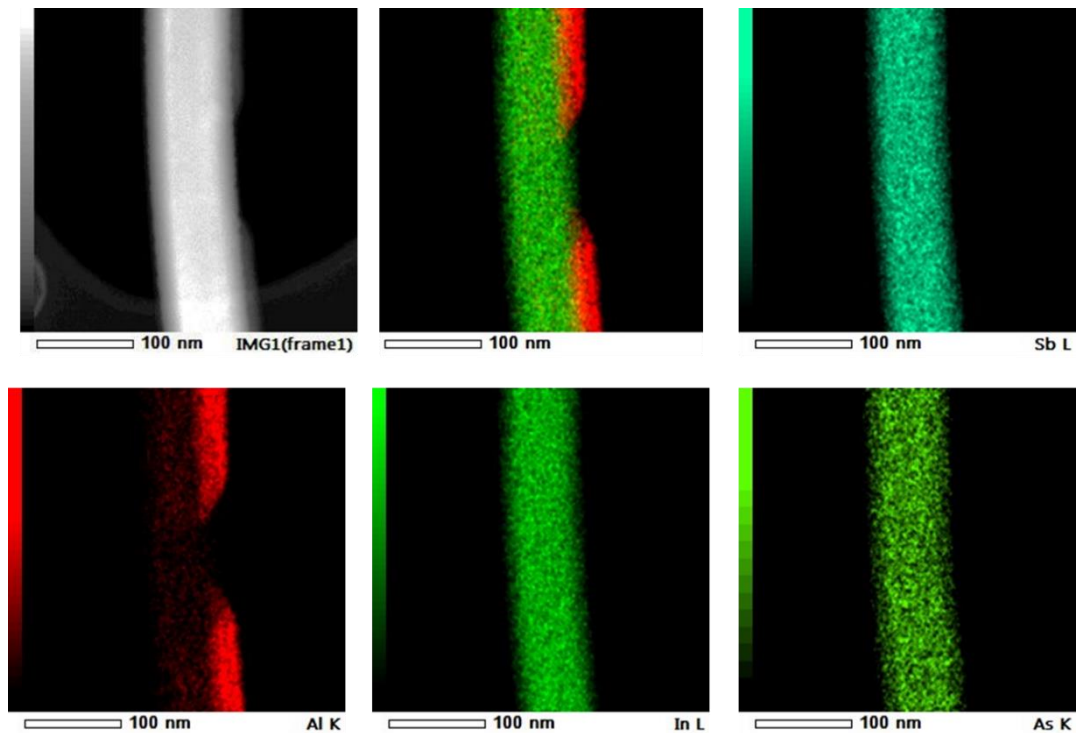


Figure 6.14 HAADF-STEM image showing the break in the aluminum shell from the wire pictured previously. EDX mapping of the wire also confirms a break in the aluminum shell along with a uniform composition of arsenic and antimony showing no segregation.

Image courtesy – M. Verheijen, TU Eindhoven

Figure 6.12 shows this sensitive growth window. The dielectric mask is a very good indicator of substrate temperature and is primarily where Sb_2 sticks to the dielectric surface. As_4 growths at the same temperature led to very good selectivity. It can be observed that the deposited III-V on the dielectric has coagulated at 445°C , with patches of the dielectric visible, while it is rough at 435°C and has a comparatively smoother uniform coverage at 425°C . The competition between 1) sticking (incorporation in the nanowire) and 2) surface diffusion on the dielectric and along the facets of the nanowires determines the growth window for any given As/Sb ratio. It was observed that arsenic incorporation increased disproportionately faster with respect to an increase in Arsenic flux, and hence the growth temperature and fluxes would require careful redetermination if the composition of the nanowire is to be changed.

On a (100) InP substrate, nanowires grew at a relative angle of 35 degrees from the substrate surface. By carefully positioning the gold droplets with electron beam lithography, wires that would barely miss each other could be grown. Though this positioning did not lead

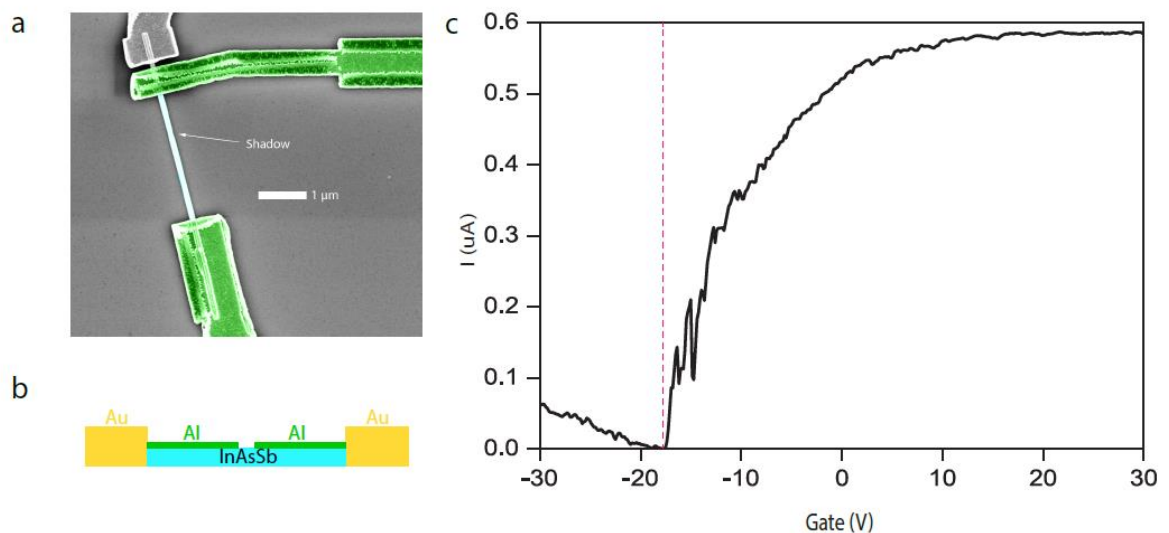


Figure 6.15 (a) InAsSb nanowire device with a gate on the tunnel junction, with the schematic shown in (b). (c) shows the nanowire pinching off on application of a negative gate voltage. Due to the narrow band gap, holes lead to conduction after the gate voltage is further reduced. Image courtesy – H. Zhang, TU Delft.

to as high a yield as growing nanowires on trenches, it still led to quick substrate fabrication and the growths of wires that could be used for shadow evaporation of aluminum to create *in-situ* epitaxial islands. As the wires grow axially along the (111)B axis, they have an equal probability on the (100) wafer of choosing two orientations projecting 180 degrees from each other. Yet the probability that few wires would lead to shadowing is high and an example of this shadowing is shown in Figure 6.13.

HAADF-STEM imaging of the nanowire confirms the break in aluminum shell as observed in SEM. EDX mapping shows uniform As and Sb distribution across the nanowire, indicating no clustering or phase segregation (see Figure 6.14). STEM imaging also confirms that the crystal structure is purely zinc-blende, devoid of any wurtzite segments. The slight

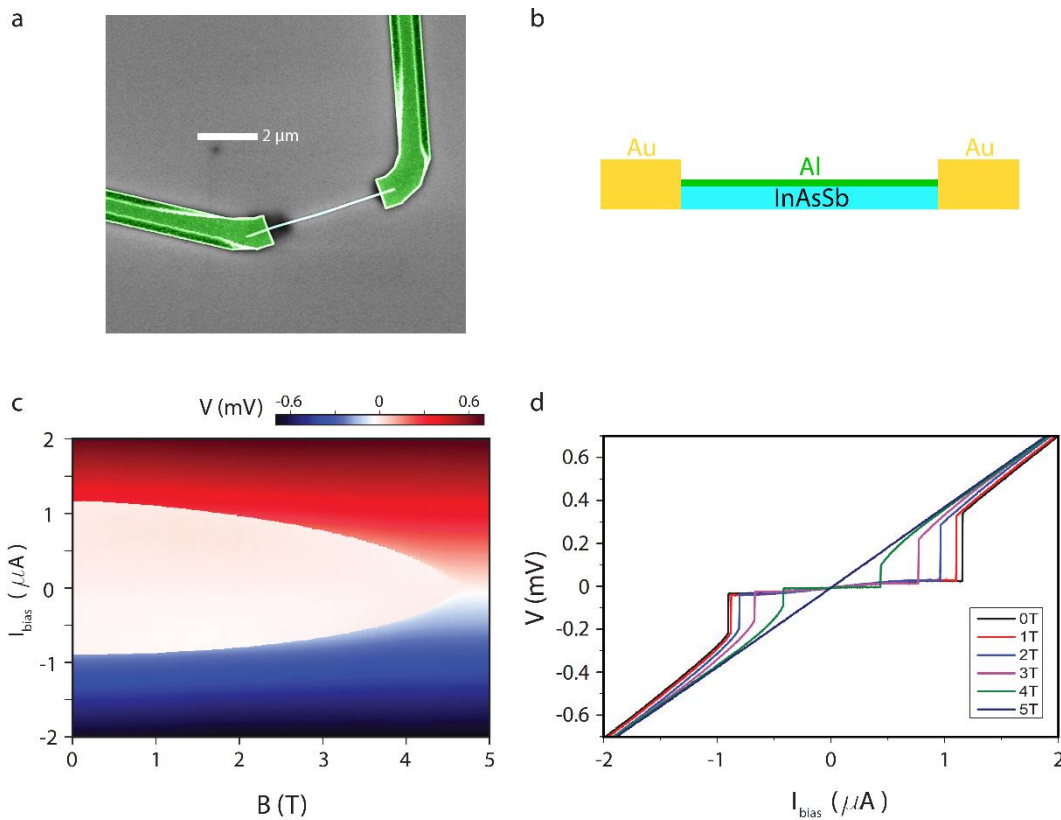


Figure 6.16 (a) device geometry used to study superconductivity of the aluminum shell with the schematic shown in (b). (c) shows the observed superconductivity with critical field of about ~4.5 Tesla. (d) shows line cuts of the superconductivity. Data taken at 300mK.

Image courtesy – H. Zhang, TU Delft.

bowing of the nanowire is believed to have been caused by the strain put on by ~10nm aluminum shell on two facets and is not seen in nanowires without an aluminum shell.

Upon application of a top gate voltage on the part of the nanowire uncovered by the aluminum shell, conduction could be pinched off completely, demonstrating full depletion (see Figure 6.15). Upon continued depletion, the junction was observed to conduct again. This region of conduction is expected to be caused by holes, as the band gap of InAsSb is expected to be of the order of 100 meV at 300K. These measurements were performed with the aluminum in the normal/metallic conduction regime, where it could be used as an epitaxial ohmic contact to the nanowire. This observation of full depletion is a necessary prerequisite

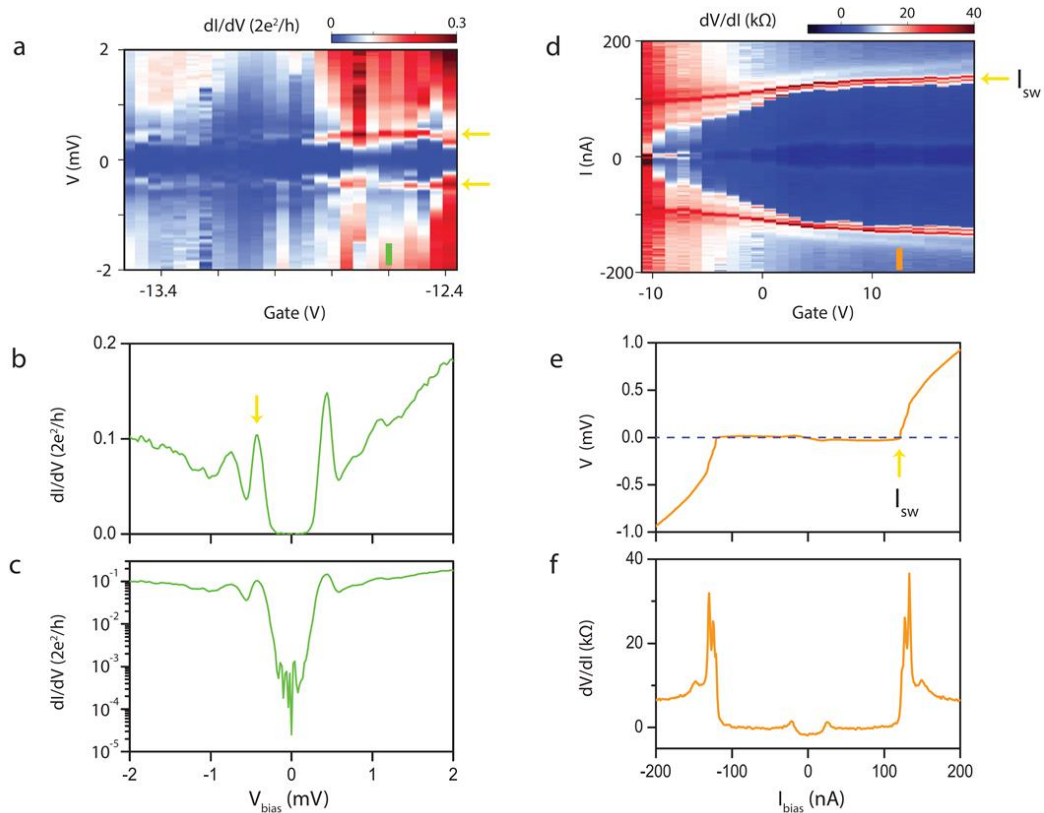


Figure 6.17 (a-c) show induced hard gap superconductivity in the InAsSb nanowire while (d-f) show supercurrent flowing through the nanowire and eventually pinching off as the tunnel barrier is pinched off. Image courtesy – H. Zhang, TU Delft.

for the use of InAsSb nanowires for observation of MZMs as the spectroscopy measurements required for search of MZMs are performed in the tunneling regime very close to full depletion.

Next, the superconductivity of the aluminum shell was probed to gauge its critical field. While HAADF-STEM indicated smooth and continuous coverage of about 8nm Aluminum and about 2nm AlO_x formation, further electrical measurements with in-plane magnetic field will be necessary to probe the quality of the superconducting film. At 300mK, a critical field in excess of 4.5 Tesla was measured (see Figure 6.16), which is close to the limit of in-plane critical field for thin films of aluminum [110]. The critical current at zero field was measured to be about 1μA.

After confirmation of both full depletion and the presence of a superconducting shell, the presence of induced superconductivity in the nanowire was confirmed by conductance spectroscopy (see Figure 6.17). An induced hard gap was observed with suppression of conductance within the superconducting gap by more than two orders of magnitude. Upon application of an in-plane magnetic field, features were observed (potentially Andreev bound states) that could not be directly associated with the presence of MZMs.

In future work, the growth of long sections of nanowires with a varying As/Sb ratio and without a superconducting aluminum shell will be necessary for basic characterization of the nanowire's material properties – properties like field effect mobility, quantized conductance through a quantum point contact, and g-factor as measured by bias spectroscopy of the quantum point contact. Such experiments could also observe directly the presence of a helical gap, which could then be quantitatively compared with claims of helical gaps observed in other III-V semiconductors. Finally, upon the expected eventual observation of MZMs, a

quantitative determination of the topological induced gap could be made. This gap could be compared directly with those of InSb and InAs, allowing researchers to state definitively which semiconductor host system is most suitable for topological quantum computing.

6.4. Conclusion

To summarize, this chapter offered the first demonstration of InAsSb quantum wells showing Integer Quantum Hall Effect with no parallel conduction. Full depletion on application of a top gate voltage was observed along with observation of quantized conductance through a quantum point contact. By demonstrating growth of InAsSb nanowires with *in-situ* evaporated epitaxial aluminum shells, a direct drop-in replacement for the existing semiconductor-superconductor systems of InAs-Al and InSb-Al could be created. InAsSb-Al could hence form the basis for demonstration of robust induced topological superconductivity, which will be necessary for the realization of a broadly useful, fault tolerant topological quantum computer.

7. Chapter 7 – Constructing a Topological Qubit

7.1. Introduction

The previous chapters have elaborated upon semiconductors and superconductors and the emergence of topological states at their interface. However, the primary means to build a topological quantum computer, i.e. putting together quantum bits or *qubits*, remains an outstanding challenge as of this writing. This chapter covers a few of the approaches to constructing a topological qubit that are currently being pursued both by other researchers and as part of this work. While detailing the individual components required to contrive such a physical qubit. The approaches covered vary from purely theoretical – which are the most advanced and perhaps most challenging to physically construct – to nanowire loop qubits, which were first constructed *in-vacuo*, in August 2017 as part of this work, but electrical measurements still remain due to the extreme level of complexity.

Before our discussion of the various approaches for constructing a topological qubit, a brief recap is necessary. Based on the common understanding developed in this writing, all topological qubits share a few basic requirements:

1. Well separated Majorana Zero Modes [199]
2. Braiding of MZMs, either by:
 - a. physical motion of MZMs under an applied electric field [200], or
 - b. measurement [44], [93], [95]
3. Readout of the outcome of braiding [96], [97]

The previous chapters of this dissertation addressed the creation of MZMs that are quantized, well separated, and topologically protected and that can be realized in various materials systems like InAs, InSb, and InAsSb. Section 7.2 focuses on the proposed concepts of either physically moving the MZMs to braid them around each other or of braiding them by measurement. Section 7.3 elaborates on the progress made as part of this work in realizing the proposed qubit geometries, and it also introduces the concept of readout via change in parity of a superconducting island.

7.2. Theoretical proposals

As has been described previously, MZMs are quasiparticles that are predicted to have a “memory” of how they were moved around each other or “braided”. If the positions of the MZMs on opposite ends of the nanowire were to be exchanged, the quasiparticles are expected to remember whether they were moved clockwise or anti-clockwise. The simplest network with which to physically perform this operation of moving MZMs around each other is a ‘T’-junction of nanowires [200] or a “hash” (#) shaped nanowire structure [81].

In 2011, J. Alicea, et al., [200] proposed constructing a ‘T’-junction such that MZMs would localize at the extremities of the ‘T’ (see Figure 7.1). Since MZMs localize at the edge of superconductor-semiconductor hybrid systems, this “edge” could be moved inward upon application of a gate voltage. Thus, by gate depletion of the semiconductor in the semiconductor-superconductor hybrid system, the MZM could effectively be moved. It must be noted that, since the MZM is charge-less, the externally applied electric or magnetic fields will not have any impact on the MZM itself but would rather impact its semiconductor or superconductor host system. Furthermore, a sequence of gate operations can be chosen such that the MZMs can be exchanged around each other forming a braid in time and position. Figure 7.1 shows the motion of MZMs with gates positioned like “piano keys” under the nanowire. However, while sound in principle, such a system could not be realized without further modifications. Most notably, a ‘T’-junction would mean that the in-plane magnetic

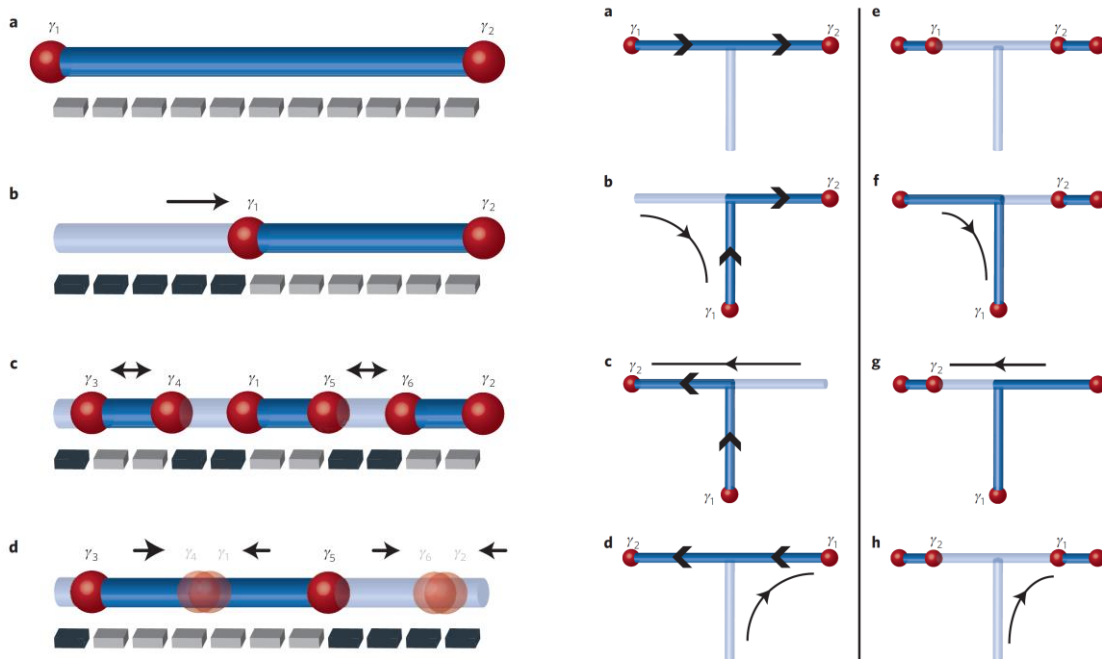


Figure 7.1 The left panel shows a MZM hosting nanowire with gates placed underneath like piano keys. On application of a gate voltage, the length of the wire could be reduced or it could be broken into multiple sections. The right panel shows how a T-junction of nanowires could in-principle be used to exchange the MZMs for braiding. Image source – Ref. [200]. Reprinted by permission from Nature Physics, J. Alicea, et al., Nat. Phys. 7, 5, pp.412-417 (2011).

field could not be applied along the length of both the orthogonal sections of the nanowire. For this reason, ‘T’-junction nanowires are not being pursued for current devices.

Bonderson, et al., [93] proposed braiding of anyons by measurement only, alleviating the need to move anyons physically in 2008. In 2016, Aasen, et al., proposed key milestones and device geometries required to realize topological qubits [201].

In 2017, with regards to the specific implementation of MZM-based qubit with parallel wires (i.e. the ‘#’ shaped network), Plugge, et al., proposed superconductor-semiconductor device geometry and operations to make a “Majorana Box Qubit” [95] (see Figure 7.2). In this proposal, the MZMs on one end of the two parallel wires were linked by a trivial semiconductor nanowire, while the topological sections of the wire were linked by a trivial superconducting bridge.

Based on this proposal by Plugge, et al., the research team led by Karzig, et al., proposed scalable designs for fault tolerant qubits, in 2017 [44]. These designs laid out a roadmap for the realization of topologically protected qubits and showed how those qubits could be scaled to realize a quantum computer (see Figure 7.3).

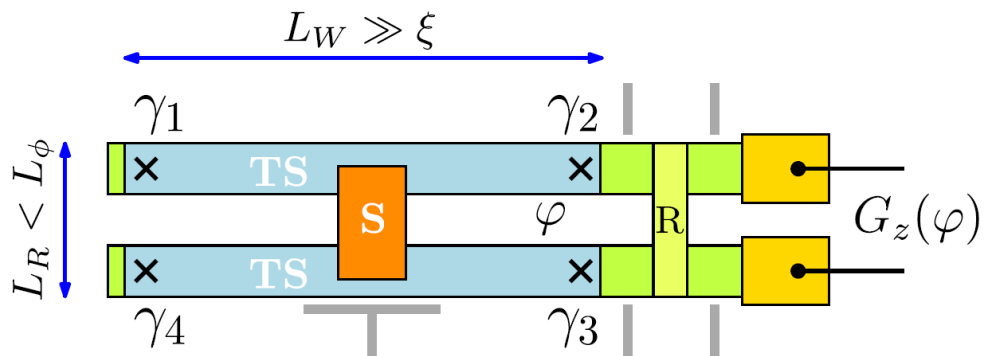


Figure 7.2 Majorana Box qubit proposed by S. Plugge, et al.
Image source – Ref. [95].

The key features of the proposed designs are a set of two semiconductor nanowire sections arranged in parallel and covered with superconductors, creating a topological superconductor with MZMs on either end of the section. A trivial superconducting island or bridge links the two topological sections and quantum dots in semiconductors to “read” the state of the MZMs.

In this setup, the s-wave superconductor that is in contact with the semiconductor and that forms the bridge between the two topological sections would have to be pristine enough to allow for the measurement of charge parity in the superconductor. The outcome of the measurement/fusion of MZMs after braiding – either the ejection of an electron from the topological section or the absorption of an electron into the topological section – would be

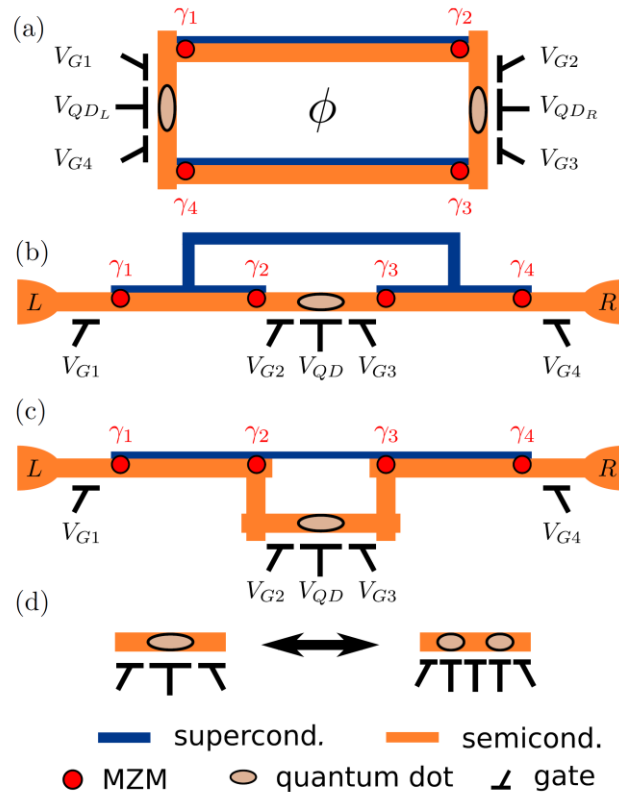


Figure 7.3 Nanowire based qubit designs with superconducting aluminum bridge between nanowires and a quantum dot linking the nanowires. Image source – Ref. [44]. Reprinted figure with permission from T. Karzig, et al., Pys. Rev. B, 95,23, p.235305 (2017). Copyright (2017) by the American Physical Society.

mediated by the superconductor. This addition or subtraction of an electron from the s-wave superconductor is expected to change its parity either by +1 or by -1, which would be the output of the topological qubit.

Given the above, the system would have to be sensitive to the change in state of just one electron by either addition or subtraction. Moreover, an ideal superconductor-semiconductor hybrid system operating at the lowest possible temperatures would be required as low operating temperatures would reduce unwanted thermal fluctuations.

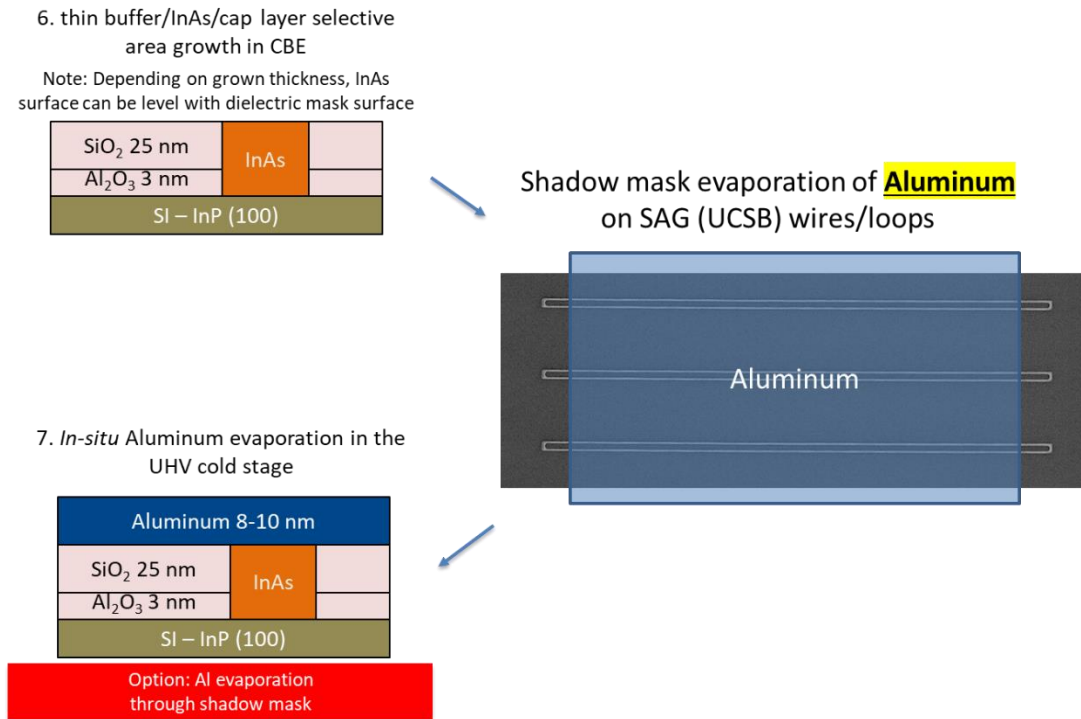


Figure 7.4 The SAG InAs process steps required for making a qubit *in-situ* have been slightly modified to involve evaporation of aluminum on InAs post-growth such that the end of the in-plane wires are not covered by the stripe of aluminum allowing for a gate defined quantum dot in the region uncovered by aluminum and two topological sections of the wire connected by a superconducting bridge. Image courtesy – J.S. Lee, UCSB

7.3. Experimental realization

As has been described previously, selective area growth (SAG) allows for the realization of complex topological networks in a scalable manner. By the evaporation of aluminum on in-

plane nanowires grown by SAG, a prototype device to demonstrate braiding could be realized. The steps to realize just such a device will be described in this section.

First, the evaporation of aluminum could be performed either by blanket evaporation or via a shadow mask such that the edges of the semiconducting wires are not covered in superconductors.

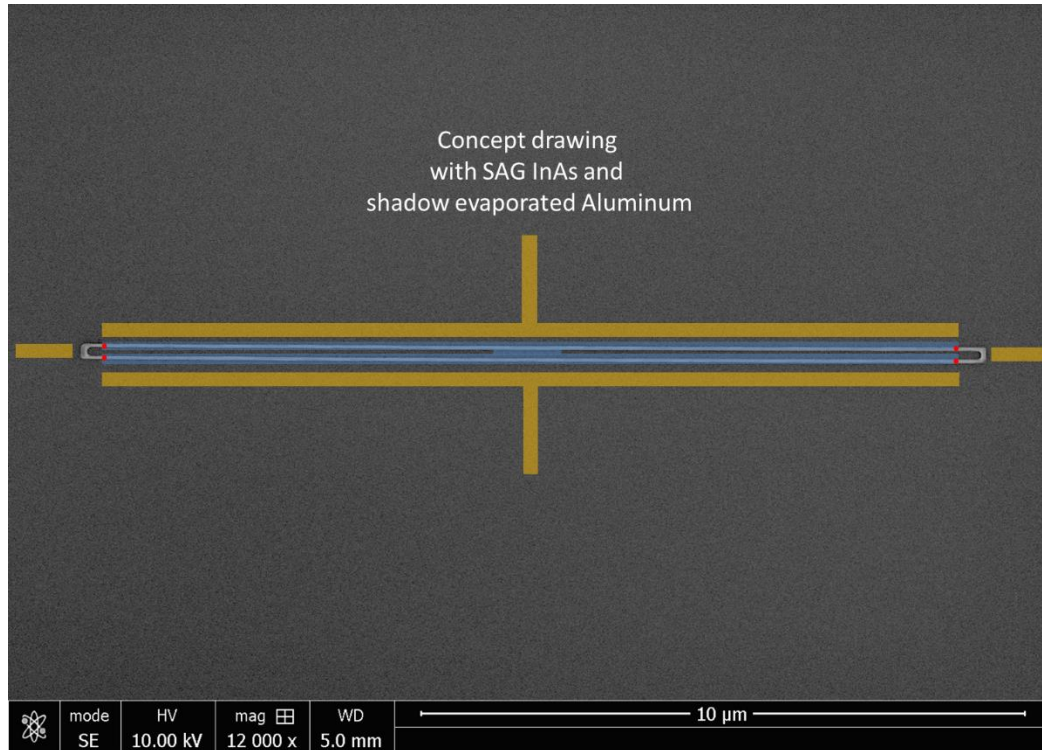


Figure 7.5 A concept drawing showing a qubit constructed from SAG InAs.

While aluminum can be selectively etched from InAs surface, no good chemical wet etch exists for removing aluminum from the surface of InSb. Therefore, shadow evaporation must be used. Shadow evaporation of an island or bridge would leave the ends of the nanowires uncovered, which is necessary for the desired device structure. These ends would define the edge of the topological sections hosting MZMs, while the perpendicular sections of the

semiconductor would be used to create quantum dots²³. Though more complex, it is possible to achieve such a geometry by using VLS nanowire ‘#’ networks [81].

Long VLS nanowires of InSb, InAsSb and InAs could be used to make loop-less “loop-qubits” (see Figure 7.6). For nanowires longer than $>8\mu\text{m}$, two separate sections of $\sim 3\mu\text{m}$ each, separated by a section of semiconductor that is not covered by a superconductor, which by external lithography of metal gates could be used to create a quantum dot. Figure 7.7 below reiterates the growth of long InSb, InAs, and InAsSb nanowires and shows what the cross section of such a nanowire-based loop qubit would look like.

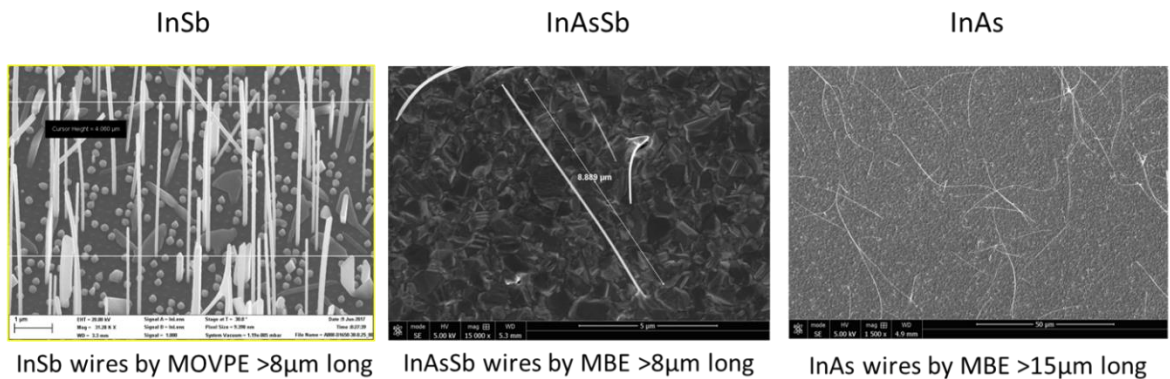


Figure 7.6 As required for constructing a loop qubit, long nanowires now practical for InAs, InSb and InAsSb. InSb nanowire SEM image courtesy – S. Gazibegovic, TU Eindhoven.

²³ Quantum dots should be thought of as regions of a semiconductor that are confined in all three dimensions. The confinement here is being executed through a combination of physical constraints in two dimensions (by virtue of the semiconductor being a nanowire) and through lithographically defined gates applying a repelling electric potential in the third dimension. These constraints would make for a 3D confinement, effectively realizing a 0D system. In such a 0D system, the energy levels are well separated and can be probed capacitively. The energy level separation is inversely proportional to the dimensions of the dot; thus, a smaller dot is expected to have a higher separation between energy levels, making individual probing/readout easier. The separation is required to be significantly greater than thermal energy so as not to smear the charge state.

The process of constructing nanowire-based loop qubits in this work begins with having a high density of nanowires rubbed/swiped onto the surface of a Si/SiO₂ wafer and loaded into the UHV. A shadow mask made of 90nm thick Si₃N₄ membrane on silicon, is also prepared and loaded into the UHV. The molybdenum wafer carrier block and the mask membrane carrier block are then mated such that the mask is nominally in physical contact with the nanowire. Because, this process can rupture the fragile mask membranes, the ~9x9mm² active region is divided into a 3x3 grid to allow for the mask to still be usable on future runs (see Figure 7.8).

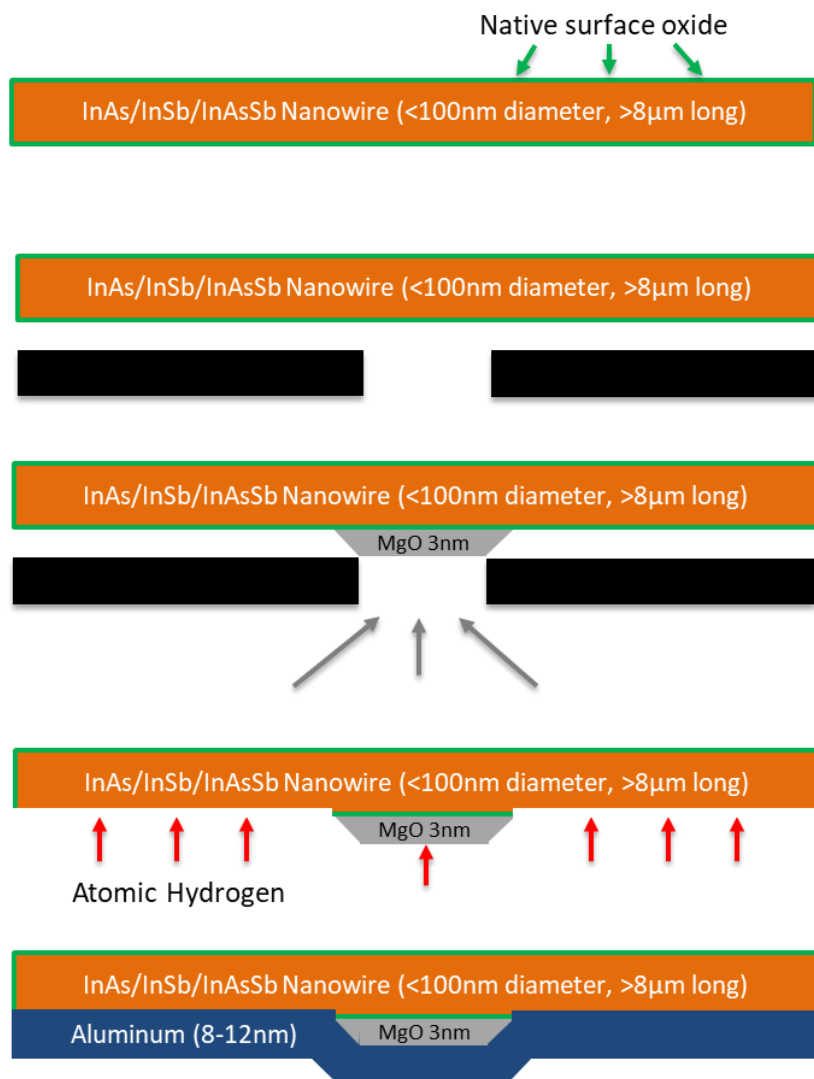
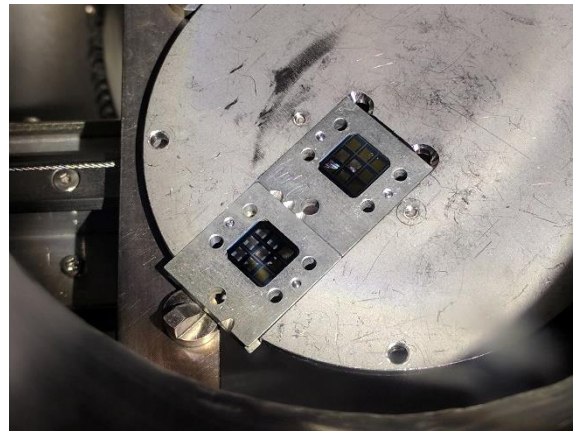
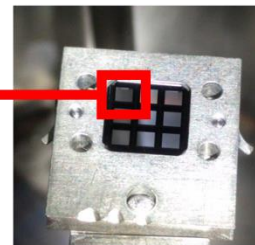
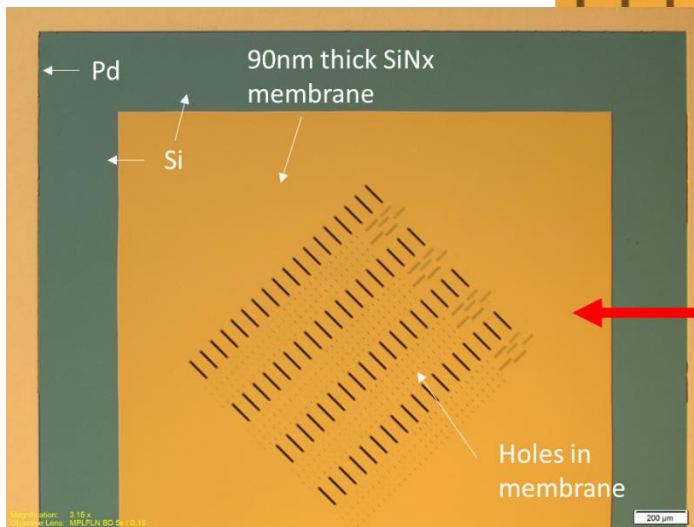
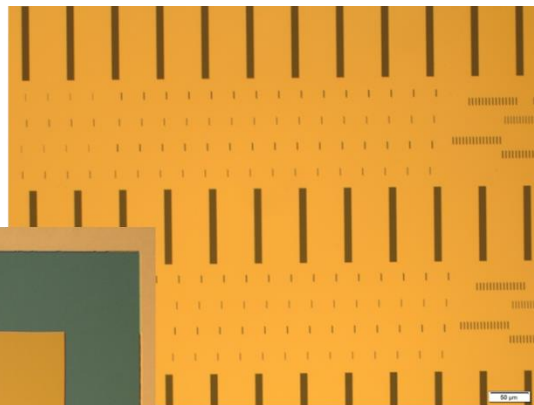


Figure 7.7 Steps required for construction of a nanowire based topological qubit *in-vacuo*. Starting using membrane mask for evaporation of MgO, followed by hydrogen cleaning and then evaporation of aluminum at cryogenic temperatures, followed by oxidation of the evaporated aluminum

The assumption shadow mask evaporation with nanowires is that windows in the mask would align with the center of the nanowires, in rare instances. After the samples are loaded in UHV, the next step is electron beam evaporation of MgO dielectric. The target thickness was chosen to be ~3nm and calibrated by ellipsometry immediately prior to e-beam evaporation, on a test wafer. MgO and AlO_x were the two available dielectrics in the Palmstrøm lab's



- Shadow masks prepared and ready for SAG InAs (CBE) samples
- Same patterns compatible with free standing nanowires (MOVPE/MBE) also (first run 18-Sept-2017)



Shadow masks prepared by Tony McFadden, Palmstrøm Group

Figure 7.8 The top panel shows the shadow masks in UHV on a sample block with the lower panel showing a microscope image of the openings in the membrane of the mask. A ~200nm thick Pd layer spaces the mask above the nanowires on the sample. Image courtesy – A.P. McFadden, UCSB.

interconnected MBE system, for electron-beam evaporation and because MgO is known to evaporate almost congruently (it is slightly oxygen deficient), a 3nm film was evaporated. It was observed that ~2nm of MgO is used as a reliable tunnel barrier for the fabrication of Magnetic Tunnel Junctions [202] and 3nm is insulating (which was required for current experiments).

The ~3nm of MgO hence is expected to be an insulator, though it requires confirmation via electrical measurements. The MgO layer is also expected to create only a small bump in the aluminum shell that will be evaporated next onto the nanowire. A bump in the shell, is expected to expose the two small sections of aluminum on either side of the bump to a small out-of-plane component of magnetic field, even though the applied magnetic field to realize MZMs is in-plane of the nanowire. Hence a taller bump would lead to a greater out-of-plane field applied to small aluminum sections, making them go normal. The purpose of the aluminum on top of the MgO is to create a superconductor-only bridge as required for readout. On the other hand, the semiconductor section, separated from the aluminum bridge by the thin MgO layer could be used to lithographically define gates and localize a quantum dot, coupling the two MZMs.

Next, the membrane mask for shadow evaporation is removed and the nanowires are cleaned with atomic hydrogen. These steps will be followed by a blanket evaporation of ~12-15nm aluminum at ~80K in the cryogenic cold stage. The sample containing the nanowires is then immediately oxidized by exposure to pure oxygen in a load lock. The result is expected to look like Figure 7.9.

Upon observation of one such sample under a microscope in Nomarski mode, the MgO regions were immediately apparent, and, upon further zooming in, specific “rare” instances of MgO patches overlapping with wires roughly near the center were observed (see Figure 7.10). These instances are loop qubit devices fabricated completely *in-vacuo*. Steps to increase yield and, reproducibility and to measure the electrical functionality of individual aspects of these devices are currently underway.

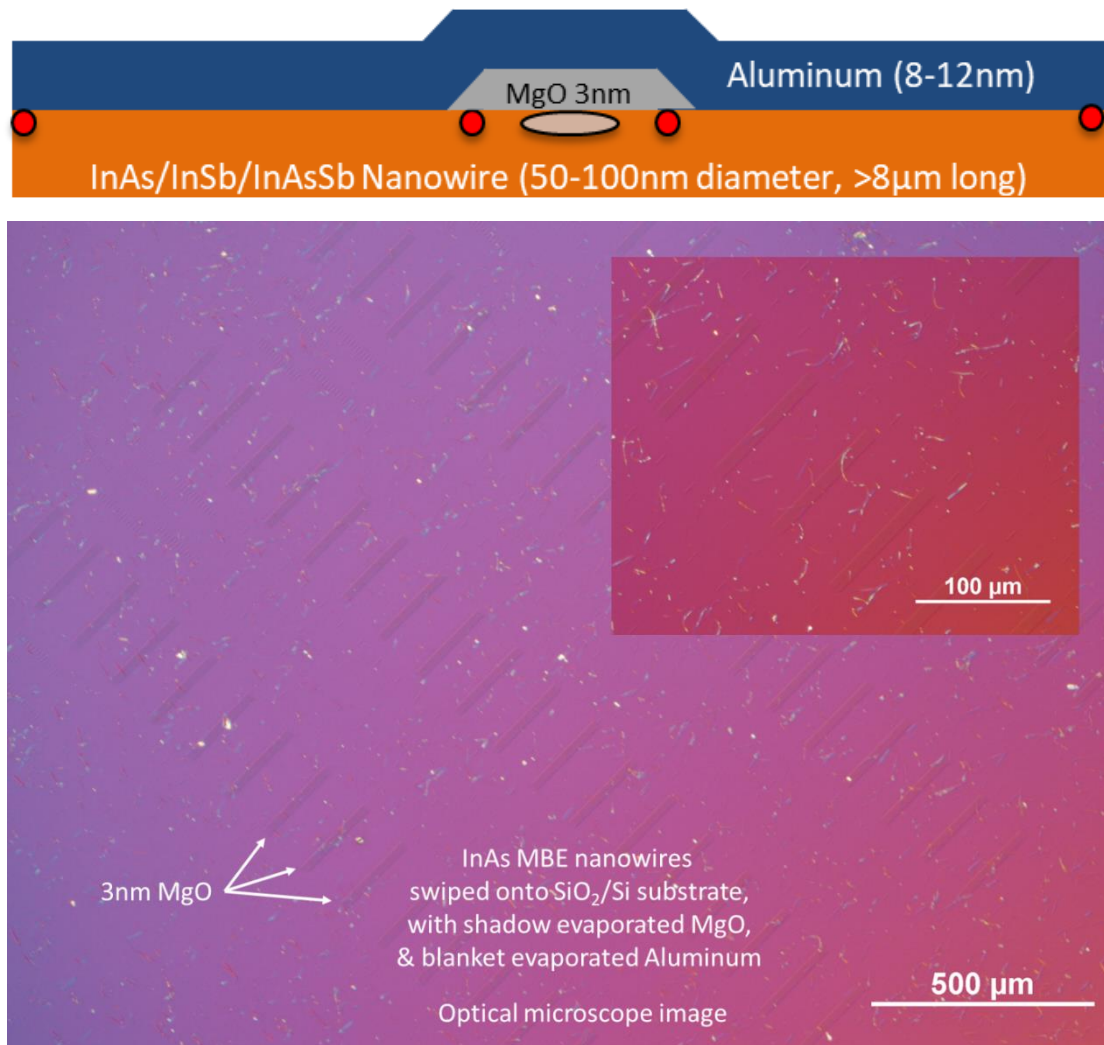


Figure 7.9 A schematic of the device made and a microscope image of MgO patches on a field of nanowires. Out of the thousands of interactions of nanowires with MgO, a few are expected to have the expected structure required for a qubit.

Finally, for readout, observation of a $2e$ periodic conductance on aluminum islands on InSb is required [97]. Similar $2e$ periodicity was previously observed on InAs-Al by Albrecht, et al., [96]. Upon measuring above the induced superconducting gap, the periodicity changes to $1e$ periodicity of a normal metal (aluminum). Coupled with the ability to fabricate loop qubit devices *in-vacuo*, this key observation of $2e$ periodicity on the InSb-Al platform is expected to be one of the last key aspects required to eventually measure a change in parity of the superconducting ground state after a braiding operation. The stage is now set for the demonstration of MZM braiding and for the observation of long-predicted non-abelian statistics.

7.4. Conclusion

The various approaches have been described in previous chapters to make superconductor-semiconductor heterostructures capable of hosting MZMs. These approaches have now been used, experimentally, to construct topological qubits, based on proposed theoretical geometries. SAG InAs and InSb structures are a natural choice for scalable qubit geometries. Since the demonstration of an operational topological qubit has not yet been

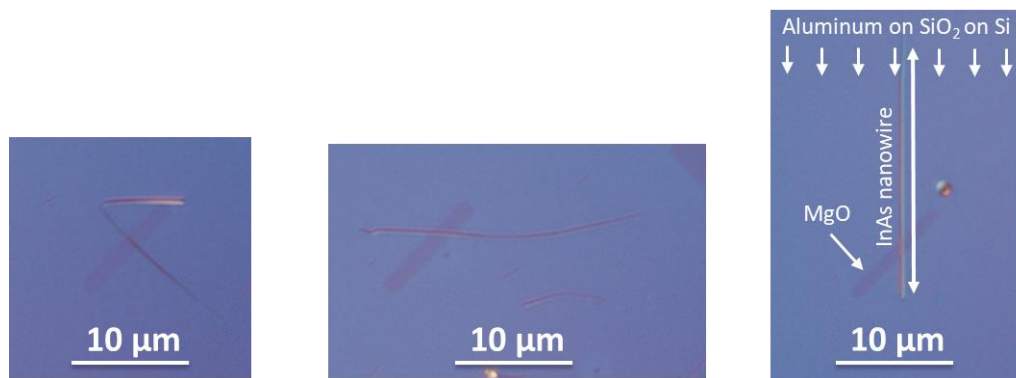


Figure 7.10 Three examples of a full structure of a topological qubit on an InAs nanowire with MgO and aluminum. Due to the very long InAs nanowires, a small section being intersected with MgO breaks the topological region in two parts, putting together the required constituents of a qubit.

achieved, a nanowire-based superconductor-dielectric-semiconductor hybrid approach has been demonstrated to make a topological qubit *in-vacuo* using the known processes. Electrical measurements are now required to establish if that process was successful.

8. Chapter 8 – Summary and Outlook

The discovery of topological states of matter along with the prediction and subsequent realization of Majorana Zero Modes has invigorated the field of materials physics and condensed matter physics in general. The materials challenges ahead in the design and realization of a topological quantum computer are expected to permeate to other fields.

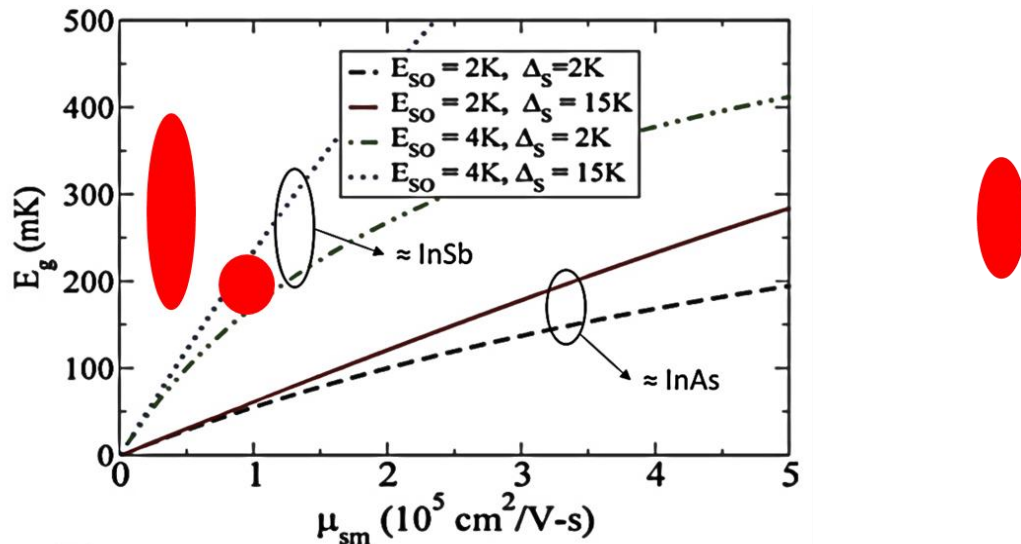


Figure 8.1 The three red marks indicate the current state of InAsSb (left), InSb (center) and InAs (right), as reported in this work, with the expected topological induced gap. A larger topological induced gap is expected to lead to increased topological protection and the realization of a practical topological quantum computer. Image adapted from – Ref. [61]. Reprinted figure with permission from J.D. Sau, et al., Phys. Rev. B, 85, 6 p.064512 (2012). Copyright 2012 by the American Physical Society.

Similarly, progress made towards addressing some of these materials challenges are expected to aid in better devices for opto-electronics (mid-IR and far-IR materials based on InAs, InSb, and InAsSb), high-speed traditional computing (superconductor-semiconductor hybrid networks), and many as-of-yet unforeseen applications.

With the advancements in high electron mobility systems in InAs and InSb 2DEGs, new frontiers in physics are expected to be explored in the areas of Fractional Quantum Hall Effect in low effective mass and in high spin-orbit coupling materials of InAs (and, in the future, InSb and InAsSb, too). Ideally, future work should specifically focus on the search for parafermions and Fibonacci anyons, which would allow for universal gate operations in a topological quantum computer [65] and would improve our understanding of non-abelian anyons in general.

This work reported an improvement in the mobility of near surface InAs 2DEGs and the first demonstration of signatures of zero bias peaks in in-plane nanowires of InAs grown by Selective Area Growth. These technologies offer distinct advantages towards the realization of wafer-scale device networks, necessary for practical demonstration of a topological quantum computer.

InSb 2DEGs grown on InSb substrates remain at the forefront of the most promising materials enhancements, as they enable a paradigm shift in the growth of low-dimensional electron systems. This shift is expected to lead to a dramatic reduction in extended defects. Future work is expected to focus on achieving pure 2D electron transport and on characterization of these high mobility electron systems at very low temperatures, in search of FQHE.

Meanwhile, the InSb-Al nanowire system has paved the way for the first observation of quantized Majorana conductance and remains a highly promising material system for the short-term realization of a topological qubit. The in-plane nanowire network of InSb coupled with superconducting aluminum has also demonstrated robust induced superconductivity. This progress in InSb is the most significant, as it is expected to lead directly to the realization of a topological quantum computer.

InAsSb nanowires and quantum wells remain of interest, too, due to their enhanced topological gap. This enhanced gap may prove essential in the realization of large-scale topological networks and in demonstrating the promise of topological protection.

While various approaches are being simultaneously pursued for the realization of topological qubits VLS nanowires coupled directly to a superconductor remain at the center of multiple experiments. SAG nanowires are also of great interest, as any demonstration using SAG can be quickly implemented to a larger scale qubit network.

Moreover, the improvements to vacuum technology (like cryogenic superconductor growth), initially made to achieve the aforementioned enhancements in materials physics, may benefit other fields as well. This same technique is now being explored for other elemental and compound semiconductors, like Tin (Sn), Lead (Pb), Niobium (Nb) and Tantalum (Ta).

For any new superconductor to replace aluminum (currently the de-facto superconductor for topological quantum computation), observation of two-electron charging in the superconducting regime, would be necessary. This search may benefit from the low temperature growth and shadow evaporation geometries developed in this work. Tin is now emerging as one potential candidate [203]. Future work on superconductors would need to

address the role of superconductor-semiconductor interface and dislocations and disorder in superconductor on the induced superconducting gap in the semiconductor.

However, these various advances also highlight new challenges. Firstly, a robust gate dielectric with the antimonide material system may be needed. Impact of such a dielectric on electron density and on the mobility of nanowires and of 2DEG should be studied. A single crystal lattice matched gate dielectric and metal-like gate may be the alternative.

Secondly, the reduction of ionized impurity scattering in InAs and InSb needs to be further studied. A reduction in scattering would be required to observe more FQHE states. As a non-traditional alternative, potential use of rare-earth arsenides and antimonides as screening layers above and below the quantum wells, for reduced scattering should also be investigated.

Lastly, in-situ electron microscopy-based nanomanipulators, electron beam lithography, and focused ion beam-based micro-machining may further enhance the gamut of devices that could be made based on advances in coupling superconductors and semiconductors materials growth, mentioned in this dissertation. The ability to construct a topological qubit *in-situ* should greatly benefit the realization of a topological quantum computer and also aid in the discovery of fragile interfacial phenomena, at the super-semi interface.

In addition to all these predictable challenges and advances, however, there is also the potential for achievements that researchers cannot yet imagine. A quantum computer once built, may very well benefit society in ways and to degrees yet unforeseen.

A. Appendix A – GaAs Quantum Wells (2D)

A.1 Introduction

GaAs quantum wells have been at the forefront of two-dimensional electron physics for the last four decades. Due to the well-developed understanding of materials growth, surface pinning, and device fabrication in GaAs/AlGaAs heterostructures, GaAs quantum wells have been studied for a wide variety of applications. This appendix focusses on the heterostructure design, growth and low temperature electrical characterization of GaAs quantum wells, with a special emphasis on inverted triangular GaAs quantum wells, for injection of spin polarized current into a two-dimensional electron gas.

A.2 Spintronics

Injection and detection of spin polarized current in III-V semiconductors provides a unique avenue for research in the field of spintronics by coupling the mature III-V technology with the nascent understanding of spin transport. Manipulation of spins in III-V semiconductors is predicted to require a spin polarized 2 Dimensional Electron Gas (2DEG),

coupled to ferromagnetic contacts [204]. Recent work by Oltscher, et al., [205] has demonstrated efficient spin injection at low temperatures in inverted GaAs/AlGaAs quantum wells, using (Ga,Mn)As contacts. This appendix aims to develop this technology for ferromagnetic contacts using Fe and Heusler compounds Co_2MnSi and Co_2FeSi as electrodes.

All electrical spin injection and detection in GaAs was first demonstrated by X. Lou, et al., [206] and previous work by Q. Hu, et al., [207], had determined the ideal n-type doping level at the semiconductor (GaAs) ferromagnet (Fe) interface to be $5 \times 10^{18} / \text{cm}^3$. This doping level, at the metal semiconductor interface, allowed for injection of spin polarized current from Fe into a 2.5 μm thick channel of GaAs that was lightly doped to $\sim 3 \times 10^{16} / \text{cm}^3$ (see Figure A.1). The lightly doped nGaAs channel was used to study spin transport in this system. Proposed devices for manipulation of spin polarization along the channel required electron transport through a ballistic 2DEG in material with strong spin-orbit interaction. While, in principle, GaAs lacks the required strong spin-orbit interaction for effective manipulation of spins over a short range, the well-developed understanding of GaAs 2DEGs make GaAs the material of choice for a first demonstration of the so-called spin-Field Effect Transistor (SpinFET).

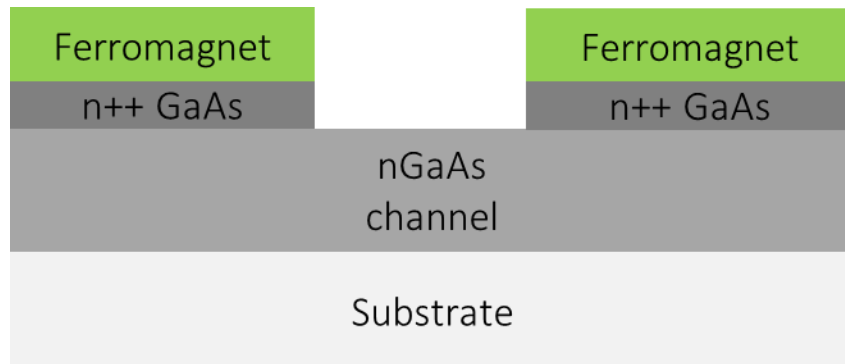


Figure A.1 Layer structure and device schematic used for injection of spin current in 2.5 μm thick GaAs channel.

An ideal 2D electron channel for spin transport, would have a ballistic path between the injector and the detector ferromagnetic contacts. Such a system requires high electron mobilities at the temperatures required for operation. Another key requirement is single sub-band occupation in the quantum confined 2DEG. Inter-sub-band scattering, apart from reducing electron mobility, may also lead to spin-flip scattering which is detrimental to spin transport. Lastly, the designed heterostructure should allow for gate control of electron density. Fine control over Rashba spin-orbit coupling, or structural inversion asymmetry, ideally requires top and bottom gates, so as to maintain the electron density constant while sweeping the electric field on the 2DEG. A square symmetric quantum well, is therefore an ideal heterostructure for all of the above requirements to be satisfied and a representative electronic band diagram for the same is provided in the Figure A.2.

Any semiconductor heterostructure for a symmetric square quantum well, requires aluminum containing layers both above and below the quantum well, typically composed of $\text{Al}_{0.24}$ to $\text{Al}_{0.33}\text{GaAs}$. As injection of spin current into the 2DEG channel requires a continuous

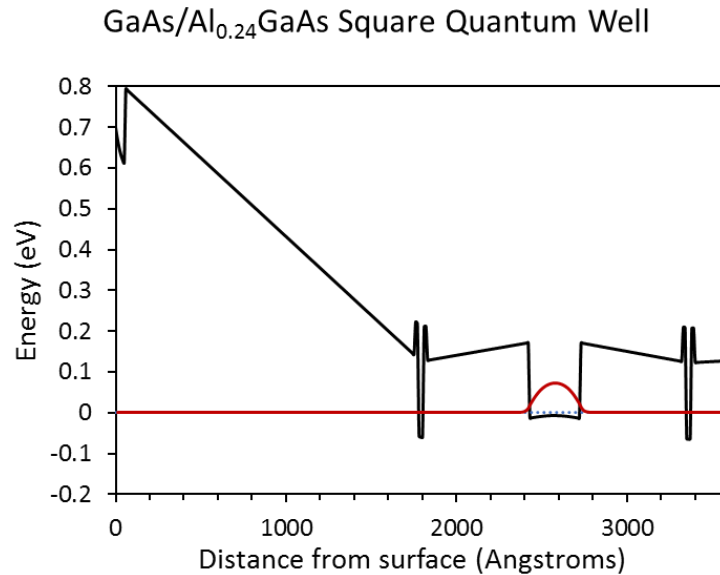


Figure A.2 Band-diagram of a square symmetric GaAs quantum well, 240nm deep with $\text{Al}_{0.3}\text{GaAs}$ barrier layers.

conducting path, at the operating temperature, from the *in-situ* grown ferromagnets to the 2DEG, AlGaAs layers are unfavorable. A SpinFET device based on square quantum wells, could hence be fabricated by *ex-situ* etching of contact regions designated for ferromagnetic contacts, followed by *in-vacuo* surface cleaning and selective area growth of n-type GaAs in the contact regions followed by *in-situ* growth of ferromagnetic contacts.

Another approach to building a proof-of-principle device, to study spin injection, detection and transport in a GaAs 2DEG is an inverted quantum well (see Figure A.3). This structure *inverts* the well-known triangular quantum well structure in GaAs by the growth of the large band gap AlGaAs layer below the GaAs channel containing 2DEG. In this work, for spin injection and detection, the layers above the GaAs 2DEG channel do not consist of any aluminum containing layers and the doping in the structure is varied so as to maintain an electrically conducting path between the ferromagnetic electrodes, and the 2DEG, at all temperatures.

While maintaining a conducting electron channel between the ferromagnetic electrode and the GaAs QW channel is necessary for spin injection if not removed by *ex-situ* etching,

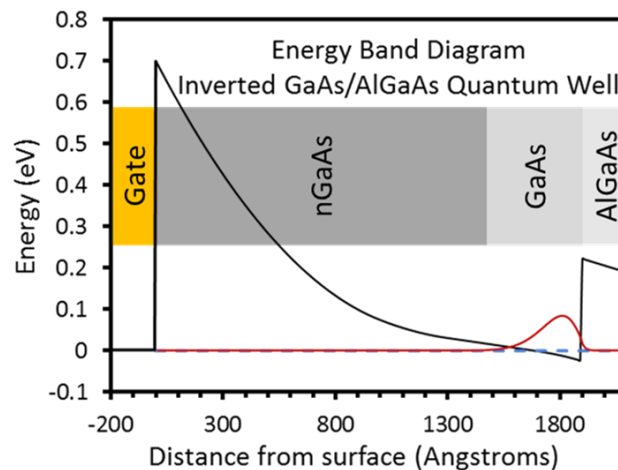


Figure A.3 The expected band-diagram of an inverted GaAs quantum well with conduction only in the 2DEG.

the heavily doped layer would lead to parallel conduction along with the 2DEG (see Figure A.4). As the surface of GaAs is known to be pinned mid-gap, by selectively etching the heavily doped nGaAs, to a selective depth, a depletion region could be created that extends to the quantum well, while preserving the 2DEG in the quantum well. This compromise, while at the risk of reducing electron mobility due to the strong proximity of ionized impurities (n-type dopants in nGaAs) to the 2DEG, allows for the realization of a proof-of-principle device.

The minimum electron density required to keep nGaAs electrically conducting at all temperatures was determined in previous experiments to be about $3 \times 10^{16} / \text{cm}^3$. N-type doping required to compensate the charges on the surface of etched GaAs, so as to create a depletion layer between the quantum well and the surface, was experimentally determined, in this work, to be $7 \times 10^{11} / \text{cm}^2$. By effectively distributing this doping over the lightly doped nGaAs layer,

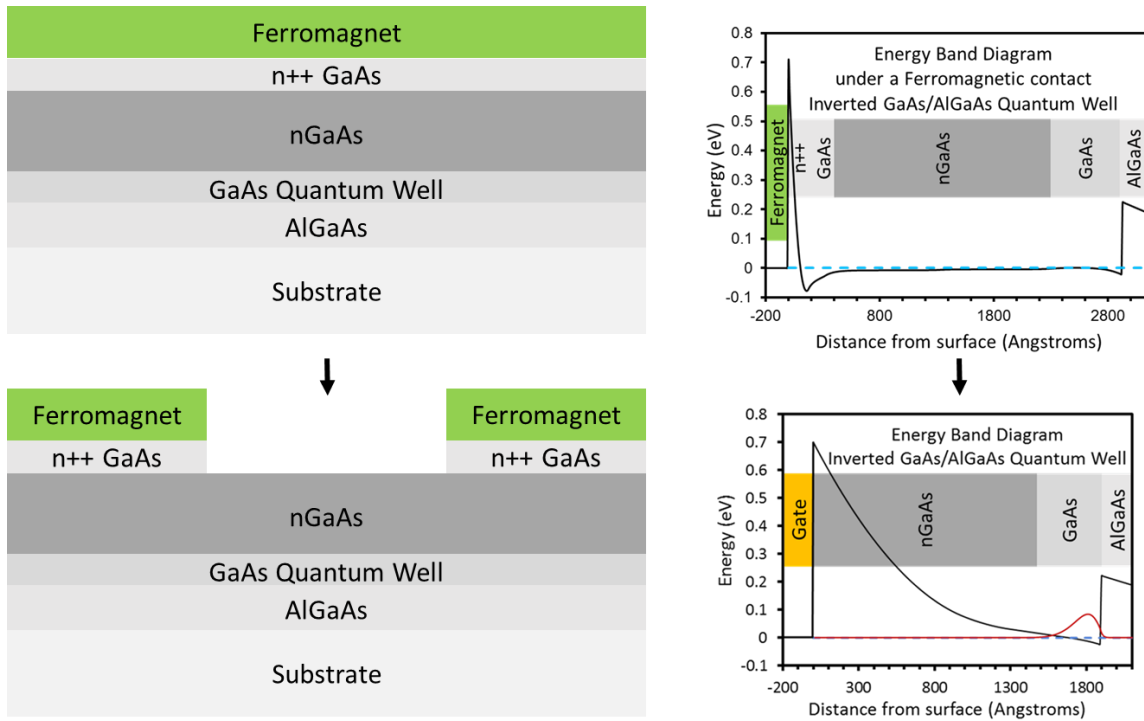


Figure A.4 Top: The expected band-diagram of the contact layers for spin injection and detection, incorporating the dopant layers at the metal-semiconductor interface, and the quantum well layer structure. Bottom: The expected device schematic, incorporating an inverted GaAs quantum well with conduction only in the 2DEG and spin injection and detection from ferromagnetic contacts on either side.

so as not to reduce the doping to below $3 \times 10^{16}/\text{cm}^3$, a pure 2DEG channel, coupled with ferromagnetic contacts, could be realized.

A.3 GaAs Inverted Quantum Wells

The first GaAs inverted quantum well heterostructure studied is shown in Figure A.5. The 30nm GaAs channel is grown on top of a 30nm $\text{Al}_{0.3}\text{GaAs}$ separating $2 \times 10^{12}/\text{cm}^2$ sheet dopants (Silicon) in AlGaAs. This doping configuration is expected to lead to formation of D_x -centers which lead to increased ionized impurity scattering. The electron mobility in the structure was measured to be $25,000 \text{ cm}^2/\text{Vs}$, with ferromagnetic contacts, at 2K with a sheet carrier density of $3.3 \times 10^{11} /\text{cm}^2$ and a corresponding mean free path of 160nm. The mean free path of 160nm was much smaller than the contact separation of 10 μm . As expected, no spin current was detected. Integer Quantum Hall effect was observed and confirmed a successful etching away of the parallel conduction channel, with R_{xx} minima touching zero. Only even integers were observed, which may either be due to reduced electron mobility or an effect of ferromagnetic contacts. It must be noted that using ferromagnetic contacts for measurement of IQHE and FQHE has not been studied and the impact of spin polarized current on IQHE and FQHE remains yet to be observed.

To increase the mean free path of electrons, the width of the QW was increased from 30nm to 50nm effectively separating the nGaAs layer further from the 2DEG. The separation between the dopants and the GaAs channel was also increased from 30nm to 50nm and Aluminum composition was increased from 30% to 35% in the spacer to increase the conduction band discontinuity. Measured using ohmic contacts, this structure showed a

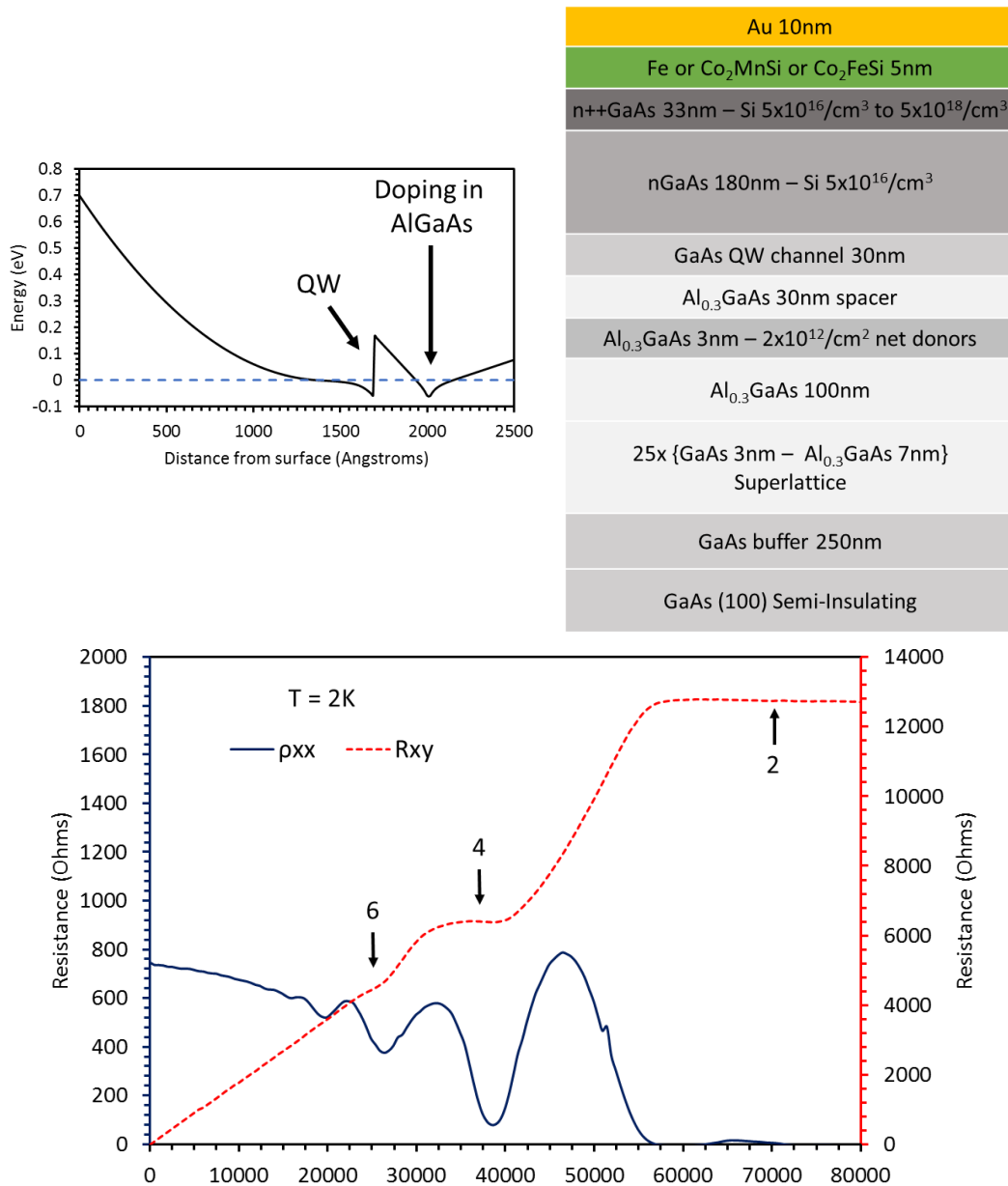


Figure A.5 The first generation of inverted quantum well heterostructure investigated with the band diagram in top-left, layer structure in top right and the observed IQHE with ferromagnetic contacts at the bottom.

significant enhancement in electron mobility to $381,000 \text{ cm}^2/\text{Vs}$ at a density of $2.5 \times 10^{11} / \text{cm}^2$ at 2K (see Figure A.6).

In this second generation of device heterostructure, the electron mean free path was estimated to be $2.2 \mu\text{m}$. Even though the mean free path has increased, it was still far shorter than the $5\text{-}10 \mu\text{m}$ separation between electrodes. Also, the silicon doping was performed at growth temperature, where Silicon is known to “ride” up to the GaAs/AlGaAs interface [190].

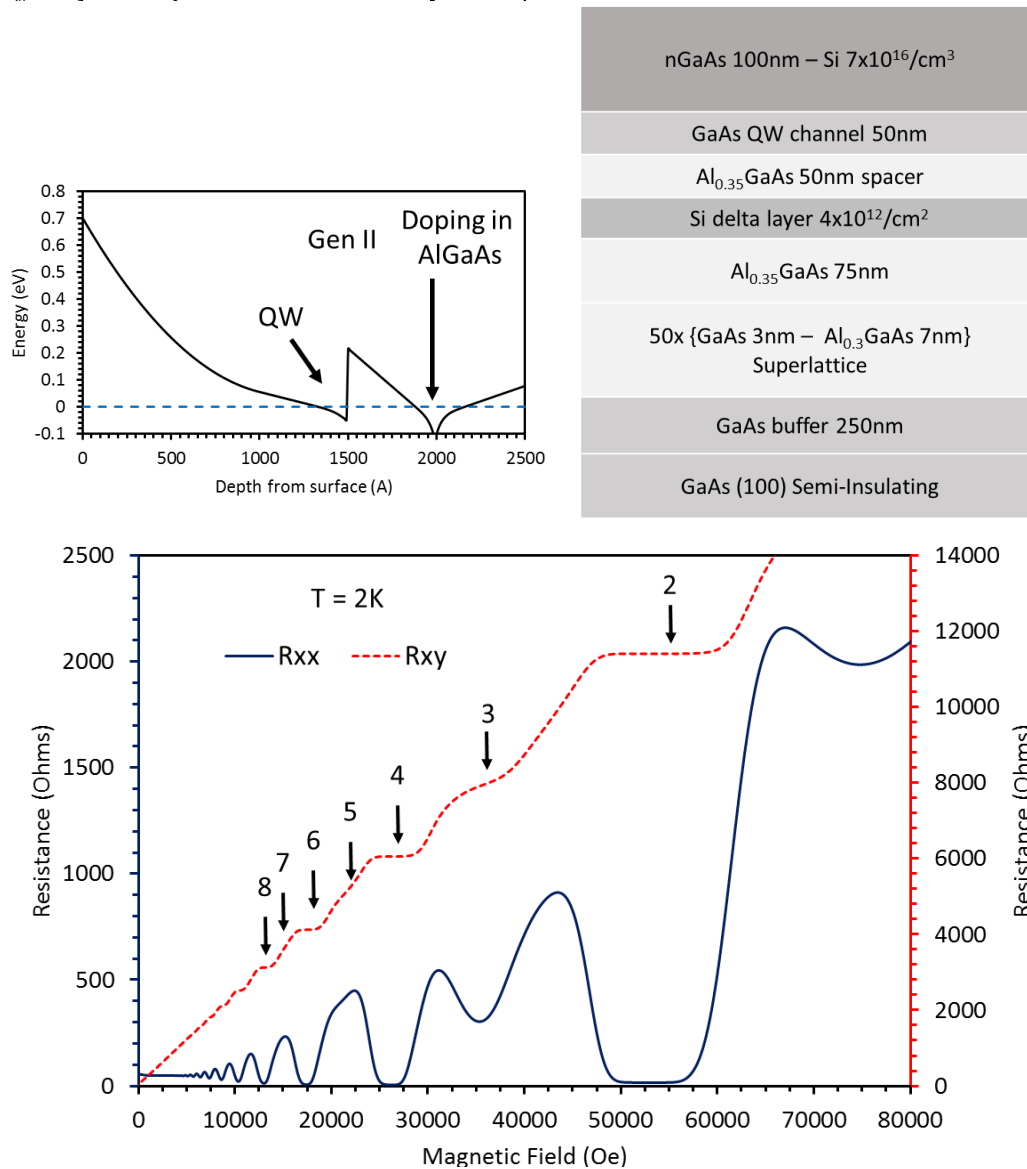


Figure A.6 Second generation of device heterostructure with the band diagram in top-left and the layer structure in top-right. The IQHE observed is shown at the bottom with a mobility of $381,000 \text{ cm}^2/\text{Vs}$.

To compensate for the increased setback between dopants and the GaAs channel, the doping density was also increased from 2×10^{12} to 4×10^{12} /cm², effectively increasing remote impurity scattering in the 2DEG. The increased Al composition of 35% was also expected to lead to rougher interface of GaAs/AlGaAs, host to the high mobility 2DEG. The improved mobility led a much-improved observation of the IQHE and odd integers (3, 5, 7) could be observed at 2K.

To further improve the mobility and reduce scattering due to the chosen silicon doping profile, a newer generation of heterostructure with an improved “short period super lattice” (SPSL) doping was investigated [174]. This concept requires a GaAs (~2.8nm) containing the silicon dopants to be grown at very low temperature (<480°C) and sandwiched between layers of AlAs (~2nm each) making a superlattice. In structures grown for this work, one or two repeats of such superlattice have been used for every doping layer and the sheet doping density of 2×10^{12} /cm² has been chosen at the upper limit, for 2.8nm thick GaAs layer. Increased doping is expected to lead to formation of Si-Si bonds and lead to a further reduction in effective ionization efficiency and carrier concentration of electrons in the well. It is proposed that by growth of such a superlattice, the quantized levels in GaAs are energetically unfavorable than the X valley in AlAs. Electrons ionized from the dopants in Si:GaAs hence populate the X valley in AlAs and act as a screening layer for the electrons in the quantum well.

Due to the absence of Aluminum in the pure GaAs layer host to the dopants, formation of D_x centers is also avoided, increasing ionization efficiency and reducing scattering. Structures with such a doping scheme have been responsible for the highest electron mobility system reported to date (found in GaAs) of 37×10^6 cm²/Vs in square symmetric quantum wells of GaAs [174], [175] and in the Pfeiffer group at Princeton University. The absence of D_x.

centers also alleviates any requirement of illumination to further enhance the ionization efficiency.

With regards to inverted QWs of GaAs, the GaAs undoped channel was increased from the previous 50nm to 60nm, to further reduce the scattering due to Si dopants in nGaAs, while

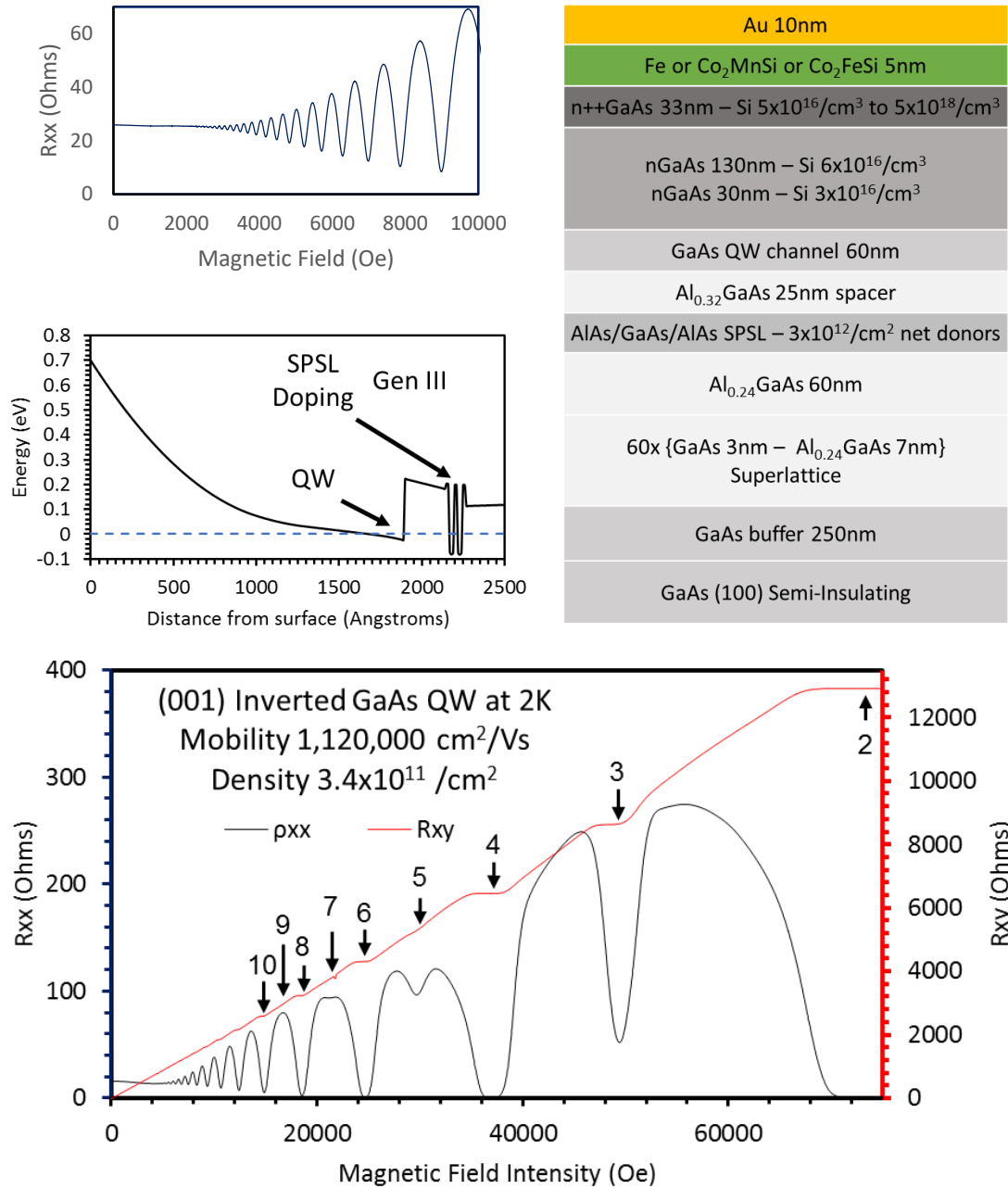


Figure A.7 The third generation of inverted GaAs quantum well heterostructure showing a peak mobility exceeding 1.1x10⁶ cm²/Vs.

the setback between the QW and SPSL doping layer was reduced from 50nm to 25nm primarily to increase the doping efficiency in the QW, requiring less dopants. The aluminum composition in the setback was also reduced from 35% to 32% to slightly reduce the interface roughness scattering at the GaAs/AlGaAs interface.

Upon cooling down to 2K, the electron mobility in the above inverted QW with SPSL doping was measured to be $1.12 \times 10^6 \text{ cm}^2/\text{Vs}$ in $200 \mu\text{m}$ long and $150 \mu\text{m}$ wide hall bar while a 50 by $100 \mu\text{m}$ hall bar of the same sample showed an electron mobility of $1.25 \times 10^6 \text{ cm}^2/\text{Vs}$ (see Figure A.7). The electron density for a doping of $3 \times 10^{12} /\text{cm}^2$ was measured to be $3.4 \times 10^{11} /\text{cm}^2$ (about 11% doping efficiency). The IQHE showed marked improvement due to the enhancement in electron mobility and the mean free path was estimated to be $7.6 \mu\text{m}$. Nearly the same electron mobility was obtained by replacing ohmic contacts with ferromagnetic Fe contacts.

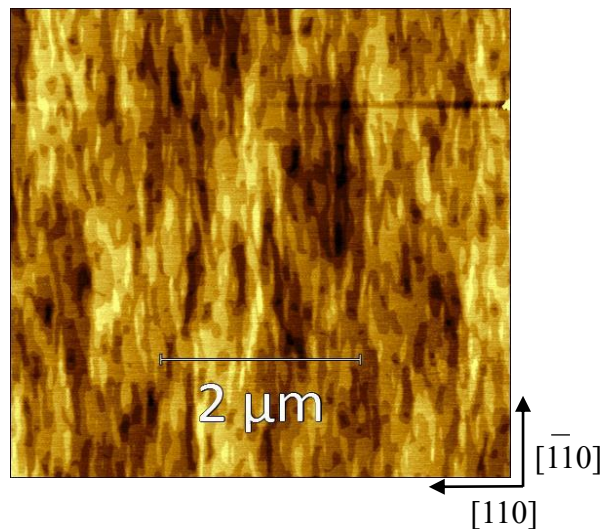


Figure A.8 AFM image with peak to peak height variation of 2nm

Atomic force microscopy imaging of the sample surface showed a peak to peak variation of a few monolayers over a $5 \mu\text{m}$ by $5 \mu\text{m}$ region (see Figure A.8). The electron mobility and density along with the variation in mean free path with temperature is shown in Figure A.9. At

300K the electron mobility is about 6,600 cm²/Vs at a density of 5.7x10¹¹ /cm², where the mobility is primarily limited by phonon scattering. The high-frequency Shubnikov-de Haas oscillations in this high mobility quantum well also indicate a quantum mobility in excess of 50,000 cm²/Vs at 2K.

Measurement of non-local spin valve devices in these structures showed signatures of injection of spin polarized current while further work is needed before spin injection can be confirmed.

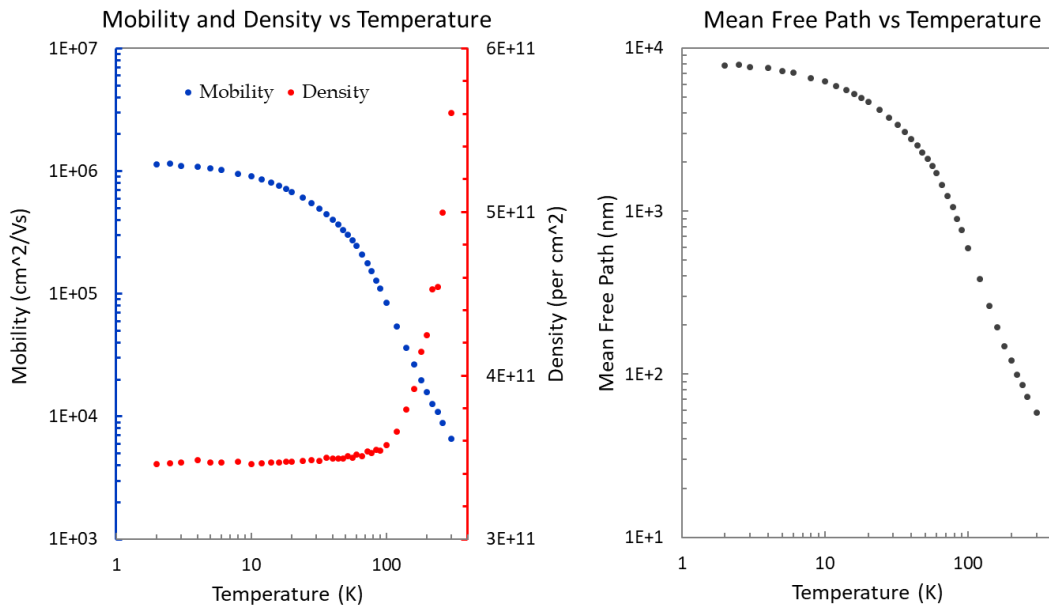


Figure A.9 Left: Mobility and density variation in the third-generation quantum well structure, as a function of temperature. Right: Estimated mean free path in the quantum well, as a function of temperature.

A.4 Conclusion

In this appendix, GaAs quantum well heterostructures, especially, inverted quantum wells have been studied for use as pure two-dimensional channels in spin transport. With improving device designs, mobility was seen to dramatically improve from 25,000 cm²/Vs to over

1,100,000 cm²/Vs. This work establishes the necessary design parameters for exploration of inverted quantum wells in GaAs. The design and growth of these inverted heterostructures was used as the basis for growth of InAs, InSb and InAsSb quantum wells (see Chapters 4, 5, 6) for injection of supercurrent, necessary for topological quantum computation.

B. Appendix B – Improvements to Molecular Beam Epitaxy

B.1 Introduction

The work reported in this dissertation was performed in the Palmstrom Lab's interconnected UHV growth and characterization system (see Figure B.1). While significant amount of previous work has already been performed on upgrading the III-V VG V80H MBE that remains the primary tool used in this work, some major upgrades and modifications were performed during the course of this dissertation to further improve the vacuum and reduce the unintentional dopant concentration in the materials grown. This appendix also focuses on the current optimum procedures for performing maintenance, bakes and operation of the III-V MBE, which may be applicable elsewhere as well. Additionally, key lessons from residual gas analysis for detection of small leaks, along with accurate and reliable determination of temperature based on pyrometry and band-edge spectroscopy (both added to the system as part of this work), have also been included. With regards to formation of epitaxial superconductor-

semiconductor interfaces on samples grown by MOCVD and then introduced into the UHV system at UCSB, improvements to and operation of the atomic Hydrogen cleaning setup, cryogenic sample stage for superconductor evaporation and load lock for high pressure oxidation of samples, have also been discussed. Lastly, implications of these lessons learnt on the design of an ideal MBE system have been elucidated.

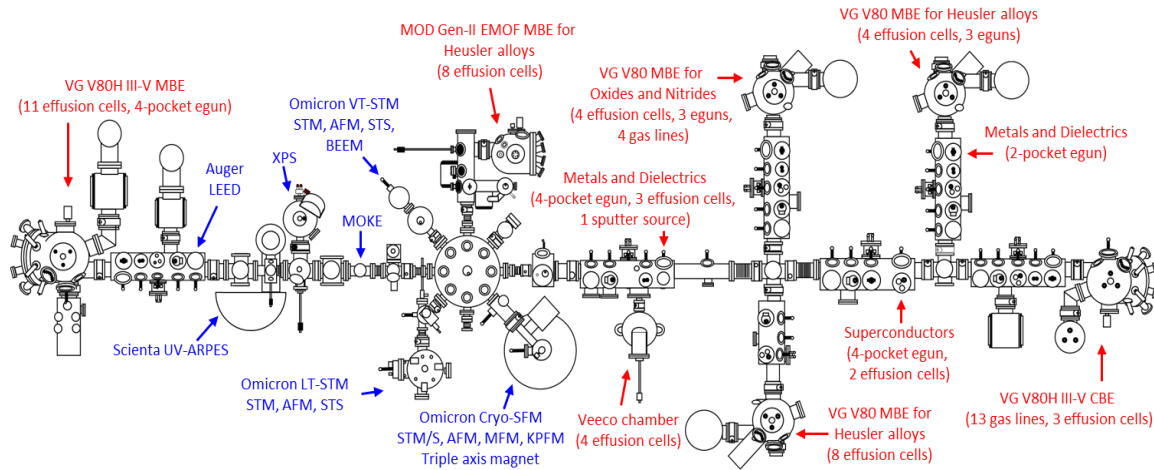


Figure B.1 Schematic diagram of the interconnected UHV MBE growth and characterization system at the Palmstrøm lab at UCSB (December 2019).

B.2 III-V VG V80H Molecular Beam Epitaxy

The III-V VG V80H MBE in the Palmstrom lab at UCSB is a 15-element system capable of growing Arsenides and Antimonides. It includes a 4-pocket electron beam evaporator equipped with elemental superconductors (Nb, Ta, V, Mo).

B.2.1 Antimony cracker cell

Prior to April 2013, the chamber was equipped with an SVT Associates Antimony valved cracker, which was replaced with a Veeco Mark IV Sb 200-V valved cracker. In subsequent growth campaigns, it was determined that the Veeco cracker could be refilled with a near full

charge of 700gm of 7N pure Antimony, for its installation angle, and could be completely used up in a typical run of 18 months. A key challenge during the initial operation of the cracker cell was the excessive deposition of Antimony on the shutter. At a critical weight, the chunk of Antimony would fall back onto the face of the cell, completely blocking any flux, leading to a chamber opening. A workaround to delay such a fallout was to use the automated valve positioner, provided with the cracker cell, and to keep the valve in near closed condition while ramping the cracker cell to growth temperature or back down to idle. When not in use, the valve was strictly kept closed. This increased the time interval between the catastrophic falling out of the deposited charge on the cell facing side of the shutter.

It was observed during subsequent chamber openings, after the initial installation of the cracker cell that the water-cooling shroud enclosing the cracking zone of the cell, acted as a

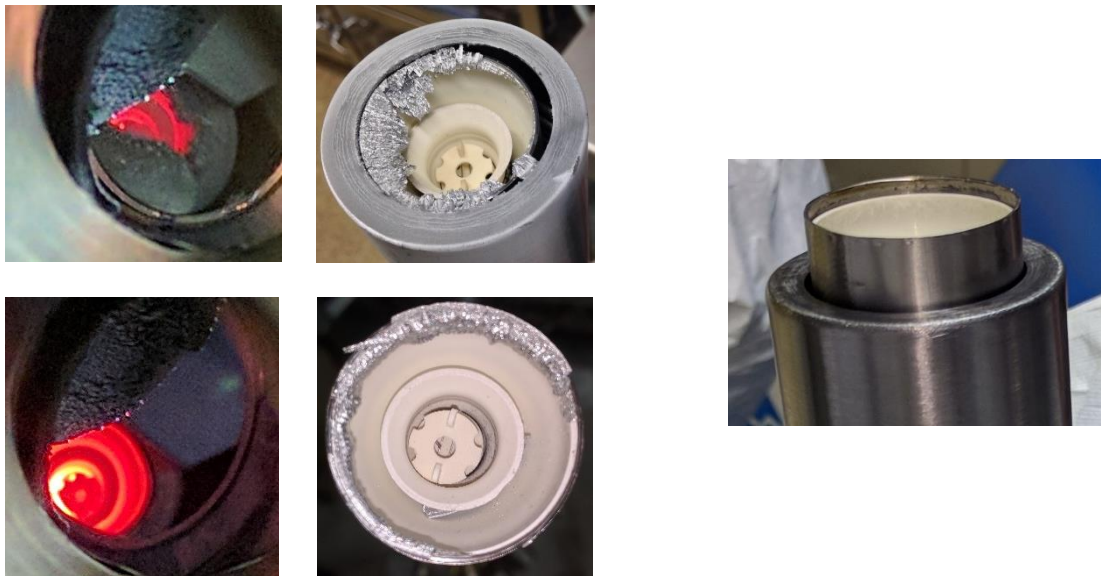


Figure B.2 Left panel clockwise from top-left, tip of the Antimony cracker cell covered with Antimony growing from the edges of the water cooling jacket. Growth/precipitation is exasperated by lower cracker temperatures necessary for growth using Sb4. Top-right: a close-up view of the Antimony deposition, after the cracker cell has been removed for maintenance, showing growth nucleates where the water cooling jacket cools the tip of the cell more. Bottom-right: close up of the tip of the cell with antimony desposited around the edges. Bottom-left: red glow from a clean tip of the antimony cell with no deposition. The right panel shows the modification made, where the water cooling jacket was modified to be 0.5" below the tip of the cell, so as not to cool the tip of the cell, fundamentally eliminating the formation of water-cooling related build-up.

cold zone for growth of Sb stalactites (see Figure B.2). These stalactites were responsible for partially blocking the flux and were also a risk for the Sb valve needle during valve operation. An example of the deposition on the face of the cell, nucleating on the water jacket, is shown below. The primary reason for such an occurrence was believed to be a lack of prior testing, as the original part, for Veeco MBEs does not require a water-cooling shroud for the cracking zone.

Controlling water flow in the shroud and running nitrogen gas through the shroud were also attempted but are not ideal due to the stainless-steel construction of the water cooling lines in proximity to a typically 1000C cracking zone. Heating the cracking zone to 1400C for several hours, under a nitrogen flow in the water cooling lines, lead to a reduction in the deposited Sb (see Figure B.2). In recent modifications, the water-cooling shroud was shortened from its base so that the hot face of the cracking zone could protrude 0.5” from the face of the shroud. This is expected to permanently alleviate the issue of stalactite formation.

B.2.2 Cryopumps

The Palmstrom Lab III-V VG V80H MBE’s growth chamber, due to its electron beam evaporator, is broadly split into two sections – the upper growth half and the lower e-beam evaporator – by a liquid nitrogen cooled cryo-panel with a few <1” diameter openings. While it aids in reducing outgassed impurities from an operating e-beam evaporator from reaching the sample surface, it also leads to a major constriction in vacuum pumping. This constriction of greater consequence as, prior to 2016, the upper half was equipped with only a 400 l/s Varian triode ion pump, while the lower evaporator section was equipped with a Perkin Elmer 120 l/s ion pump (leaking, removed in 2016) and CTI CT-8 cryo pump. Effectively, the sole cryo-

pump on the growth chamber was differentially pumping on the active part of the growth chamber equipped with effusion cells and the sample manipulator. During growth of Arsenides, a careful monitoring of vacuum pressures on either side of this cryo-panel constriction showed a differential pressure of two orders of magnitude (10^{-8} Torr in upper half, 10^{-10} Torr in lower half).

Apart from the limited pumping during normal operation, where majority of the active pumping was provided by the 77K cryo-panel, the most notable impact of the constriction was during chamber bakes. To avoid reducing the lifetime of the ion pump, the ion pump gate valve was closed to near shut position, which essentially left the growth chamber only differentially pumped. It was hence common for the bake to be pressure limited to $\sim 5 \times 10^{-6}$ Torr for a week, prior to attaining the max temperature of 180 ± 20 C. In comparison, the highest mobility chambers (e.g. Bell Labs high mobility III-V chamber) incorporated three each of CTI CT-10 cryo pumps on the growth chamber (one CT-10 is roughly twice the pumping speed of one CT-8). It was hence felt essential to increase the active pumping capacity to aid in the bake and to attain lower base and operating pressures post-bake, hopefully leading to improved electron mobility.

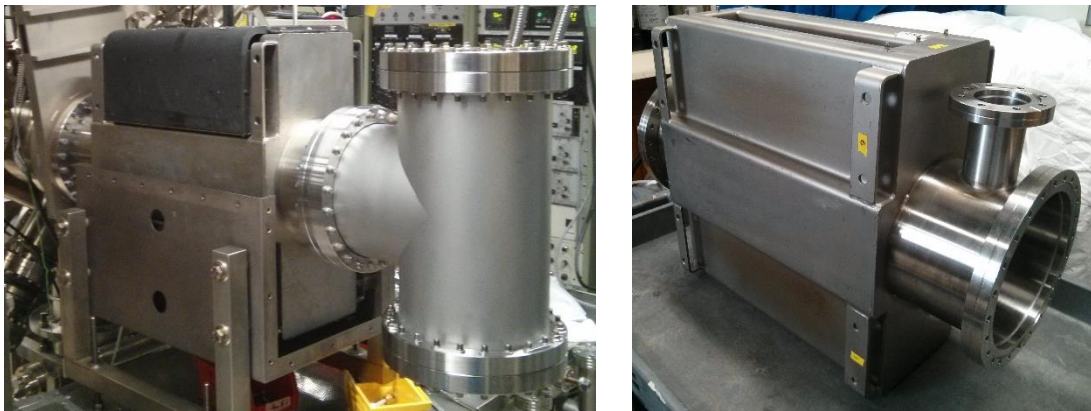


Figure B.3 Right panel shows the modified Varian style 400 l/s ion pump with 10" flanges welded on the front and the back. Left panel shows the modified ion pump's front 10" flange installed on the MBE on a 10" manual gate valve (previously 8" flange on an 8" gate valve) and the rear 10" flange (previously non-existent) with a 10" Tee.

Figure B.3 shows the modified ion pump and the modified ion pump, post installation with a 10” Tee. As cryo-pumps could not be placed inside the bake box, the primary 400 l/s Varian ion pump on the growth chamber was modified to have 10” flanges on the front and the back to act as a conduit for connecting a 10” Tee, capable of cryopump installation, outside of the box (see Figure B.4). New triode elements were installed, and the ion pump was freshly etched prior to installation. A 10” manual gate valve was also added between the growth chamber and the ion pump, replacing a smaller 8” gate valve. This concept of incorporating a cryopump on the back of an ion pump, was first mooted by J.H. English, and allowed for increased pumping, yet required minimal modification of the bake-out box.

In the bake immediately following the addition of the cryopump, ultimate bake pressure of 1×10^{-7} Torr, at bake temperature of $190 \pm 10^\circ\text{C}$ was achieved. Along with other improvements to the bake procedures described later, all interconnected UHV chambers included in the bake-box achieved a base pressure of 3×10^{-11} Torr or less (X Ray limit of the

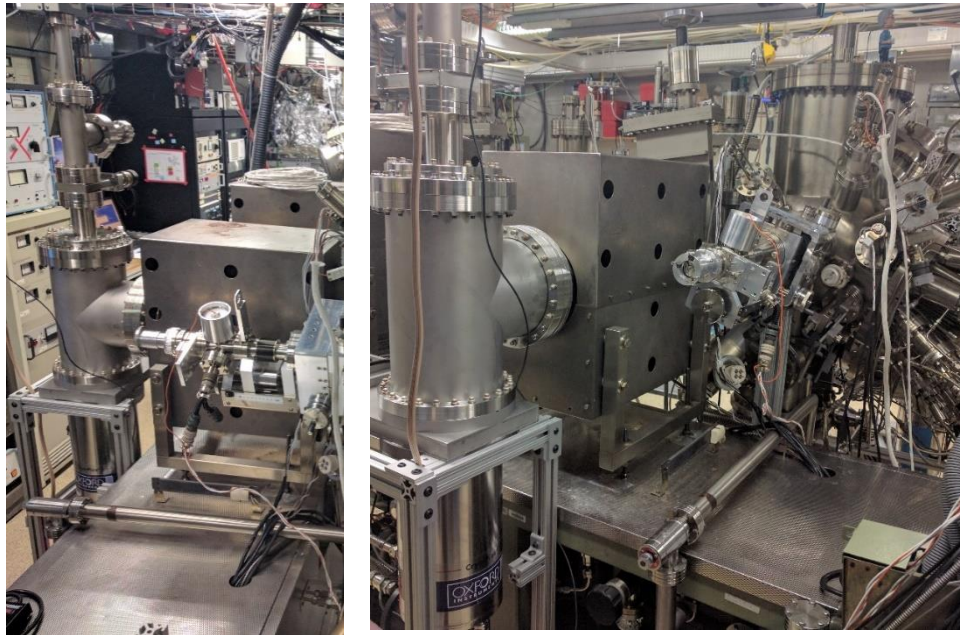


Figure B.4 Pictures above from April 2016 show the modified ion pump in operation with a new Oxford CP-8 cryo on one end of the Tee and an RGA on the other end of the Tee.

ion gauge), following the bake. Near surface InAs QWs with a then highest mobility of 650,000 cm^2/Vs were grown within two months of returning to normal operation. While the use of As_4 leads to an increase in the chamber pressure, the typically used Sb_2 during the growth of Antimonides, helps further getter gases and reduce chamber pressure. Again, within the first two months of returning to normal operation, in combination with the newly added cryo-pump, operating pressure of 5×10^{-11} Torr *during* the growth of an InSb QW ($T_{\text{substrate}} 450^\circ\text{C}$) was achieved with five effusion cells (Al, In, Ga, Sb, Si) at temperatures close 1000°C . Prior InSb QW growth pressures were 1.5×10^{-10} Torr or higher.

This unprecedented improvement in the operating chamber pressure, is expected to lead to improvements in material quality by reduction of unintentional background impurities. In a chamber maintenance cycle, two years later (April 2018), a second CTI CT-8 cryopump was added above the CT-8 cryopump from 2016 (see Figure B.5). The additional cryopump, though

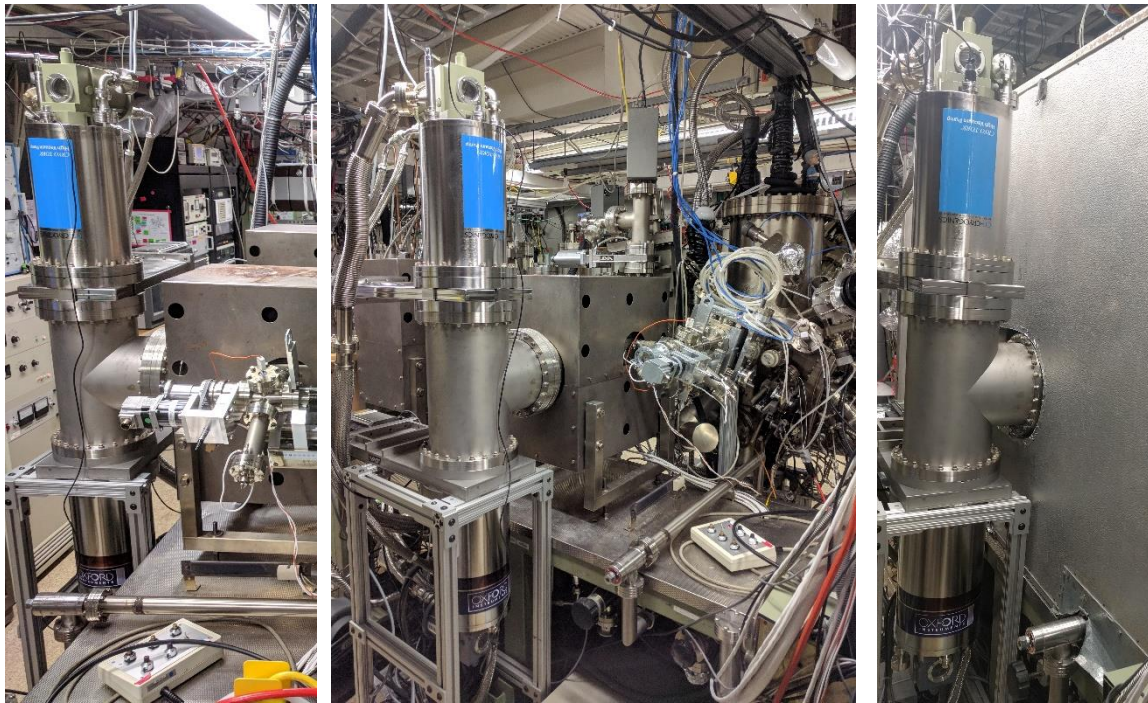


Figure B.5 Left and center panels show a second cryo pump installed in April 2018 above the previously installed CP-8, from April 2016. The new CTI CT-8 was installed to further improve the pumping speed and base pressure. Right panel shows both the cryopumps outside of the MBE bake box.

limited in conductance by the ion pump, lead to a further enhancement in ultimate bake pressure at a bake temperature of $190 \pm 10^\circ\text{C}$ and a pressure of $7-9 \times 10^{-8}$ Torr was observed. A pressure of $< 2 \times 10^{-7}$ Torr with nearly all effusion cells at 30°C within the bake was also observed. By Residual Gas Analysis, the dominant species in the chamber at this pressure and temperature was determined to be Arsenic.

With the addition of a second cryopump to the upper half of the growth chamber, a further improvement in peak mobility, and reduction in operating pressure during the growth of InAs and InSb QWs is expected.

B.2.3 Arsenic cracker cell

The Veeco Mark III Arsenic cracker cell installed on the system can hold 2.5kg of Arsenic in one fill and operate for about 6-8 years (including maintenance) on a full charge,



Figure B.6 The left-top picture shows the leaking thermocouple on the cracking zone of the Arsenic cell. The thermocouple was also not operational and was reading the temperature of the chamber wall, which could be attributed to the excessive amount of Arsenic shorting the two terminals. Right-top: Cracking zone with thermocouple removed. Right-bottom: Cracking zone with new thermocouple installed with ceramics (white) encasing the thermocouple lines. Left-bottom: Cracker thermocouple in operation reading 500°C .

depending on use. Due to the elevated temperatures during a bake and corrosiveness of accumulated Arsenic, the cracker cell has had to be removed on multiple occasions. It was found that the accumulated Arsenic, on heating up to 200°C during a bake, reacts with copper and silver-plated copper gaskets (lesser) closest to the cracker cell, leading to major leaks to air. This has led to the leak sealing of both cracker and power feedthroughs, while both are also connected to ground with $<1\Omega$ resistance. The heating elements in both zones are still operational as DC power supplies, isolated from ground, are being used. Replacement of gasket for the bulk power feedthrough requires a complete disassembly of the cell.

The thermocouple on the cracking zone was also not operation due to the accumulated Arsenic dust (see Figure B.6) and eventually developed a leak, that could not be leak sealed. Additional barrel connectors and sections of matching Type-C thermocouple wire were used to reconnect the cracker thermocouple, without rebuilding the cracking zone.²⁴

B.2.4 Substrate manipulator

A 2” substrate manipulator was newly installed in 2010, as an upgrade from a previous maximum sample size of 17x17mm. The new manipulator included a 1200°C sample heater with pBN encapsulated graphite heating element. The prime consideration for determining the most suitable manipulator for the MBE was the ability to rotate the sample in-plane and out of plane, while maintaining the same center of rotation, located on sample surface. This essential requirement was necessitated by the original design of the MBE chamber, including alignment of RHEED ports, for use in conjunction with an *in-situ* Rutherford Backscattering (RBS) beam.

²⁴ Due to ingenious ideas of J. H. English, J. S. Lee, S. D. Harrington and M. Pendharkar, the fix was implemented without having to send the cell for repair. The recommended way to repair requires disassembly of the cracking zone.

This put a stringent requirement on the design of the sample manipulator, when coupled with a less than 3” opening in the cryo-panel, for insertion of the old 17mm sample manipulator.

Some key issues that needed attention with the new 2” manipulator were:

1. Presence of a gold-plated glass tube (light pipe) for an *in-situ* back light illumination of the sample, along with an in-built bulb. Gold is a unwanted element in a III-V MBE due to its contribution of sub-gap states (typically mid-gap traps) to a GaAs or similar material system [101]. The light pipe emerged between the heater, right behind the sample (see Figure B.7).
2. A significant use of stainless-steel parts that had discolored upon the first heat cycle to 1200°C indicating temperatures in excess of 400°C on the stainless steel. Stainless steel under vacuum, upon heating, gives off vapors of H₂, Mn, Cr among other unwanted impurities.
3. Electrical lines connecting the sample heater and leading up to the bulb for backlight illumination were Kapton coated. The electrical lines in the hot-zone close to the sample heater were Tantalum but made extensive use of stainless-steel barrel connectors as unions or junctions. Also, due to the torque put on the union between sections of the wire, when rotating the manipulator out-of-plane (sample loading in and out), substrate heater wires would disengage bringing an immediate end to the growth campaign.
4. Water cooling lines were extremely thin (high impedance) and being made of stainless steel were bolted by stainless steel anchors to the hot zone of the manipulator, which was previously determined to have exceed 400°C during heat cycling. The thin lines were another design constraint imposed because of the necessity to rotate nearly 270 degrees out

of plane, and the risks associated with the less favorable alternative of hydroformed bellows.

5. Due to the stringent limitations put on the sample position with reference to axis of rotation, and the pre-installed RHEED ports, rotating the sample in-plane required a more complex

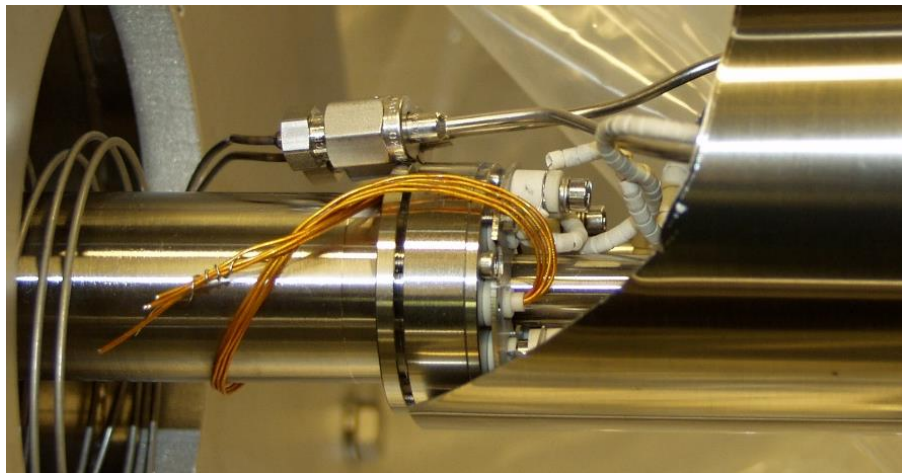


Figure B.7 The top panel shows the new manipulator from UHV-Design with a gold coated glass tube for back-side illumination of the sample. The center panel shows the Kapton lines on the manipulator. The bottom panel shows the old shield to protect manipulator parts from III-V flux.

design of parts. The incorporated design elements relied on elasticity of Molybdenum after multiple heat cycles, which did not work reliably. The system was hence operated without any sample rotation, leading a variation in alloy composition and uniformity across the 2” wafer.

6. Sample shield was too close to the surface of substrate during growth, potentially leading to outgassed vapors, from the elevated region reaching the sample surface, increasing cross contamination of grown materials, and reduced mobility. The design of the shield left the power lines and temperature sensor lines exposed to a constant flux of all elements, preferentially Arsenic and Antimony during growth. This increased the risk of electrical shorts between the thermocouple and the other elements.

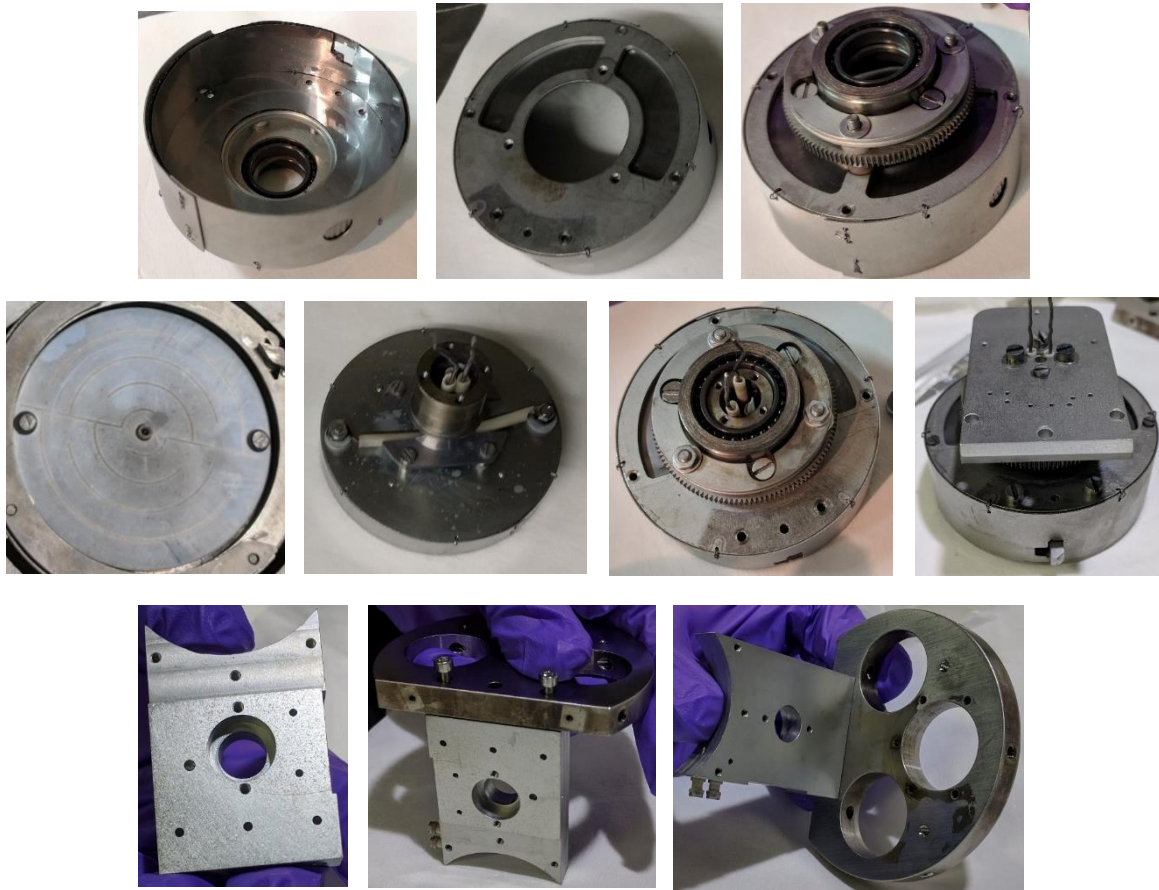


Figure B.8 The step-by-step construction of the modified manipulator head with new parts to prevent Arsenic exposure to bearings and replacement of previously stainless steel parts with Molybdenum among other improvements.

A combination of all the above led to a reduction in the peak mobility the MBE system could achieve and also led to repetitive failures of the electrical lines for the heater, forcing sudden chamber openings. A major thrust to re-design the parts, so that the problems above could be individually addressed with a view towards improving both carrier mobility and

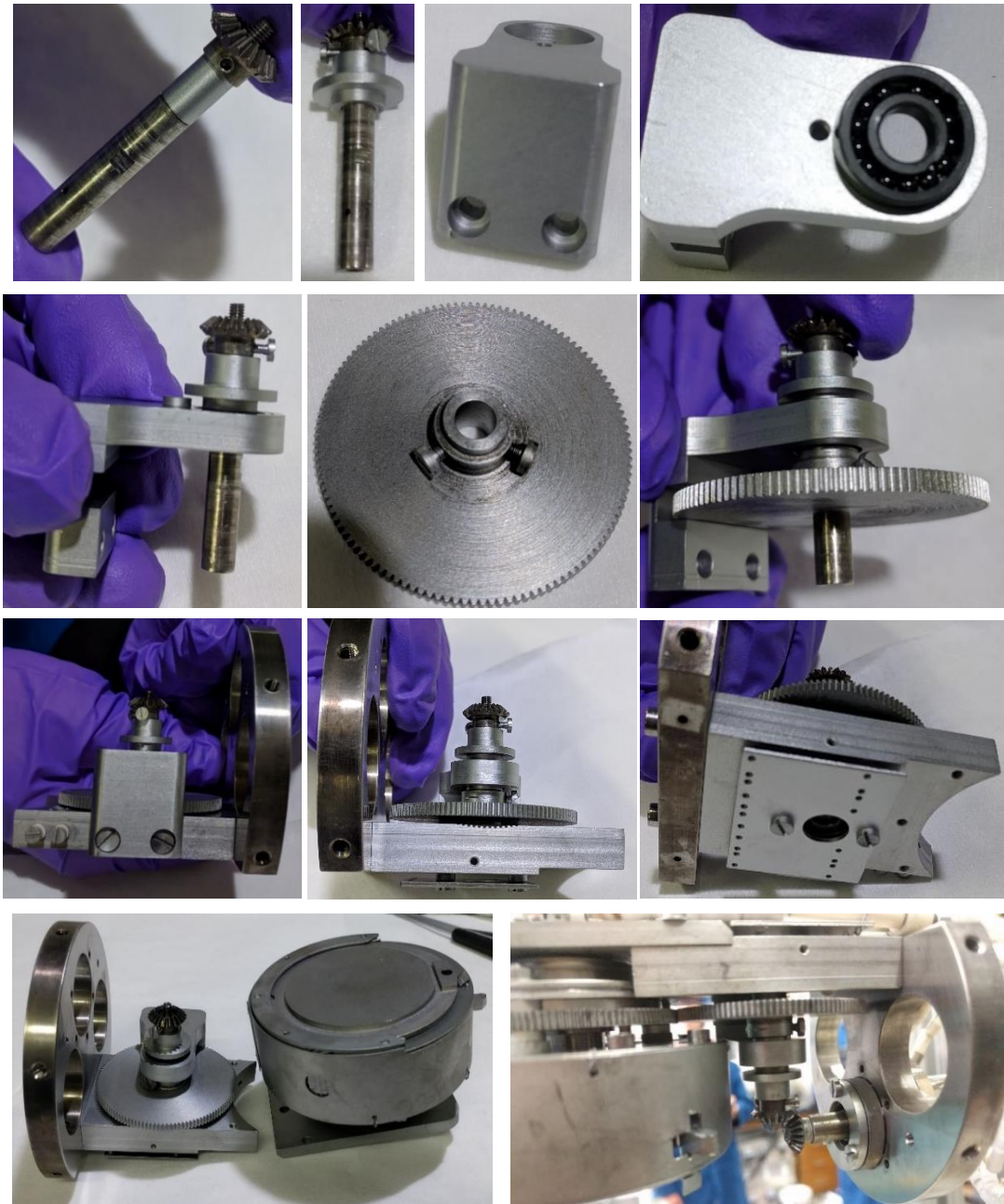


Figure B.9 The step-by-step construction of manipulator with modified parts is continued here showing the gears for in-plane rotation assembly.

operational reliability, was undertaken from Nov 2017 to April 2019. A summary of the improvements made, and their impact is mentioned below.

Multiple layers of tantalum heat shielding were added to reduce the power output required to attain growth temperature (see Figure B.8). Effectively, unnecessary heating of neighboring steel parts was also reduced. As part of the original design, except for the bearings, which were Si_3N_4 , all the parts on the heater assembly, directly below the heater were Mo or Ta. A newly added ‘door’ to allow for sample rotation was tested but eventually installation was postponed due to Mo-Mo cold welding.

Parts adjacent to the assembly holding the sample stage and the heater were all previously stainless. Except for bevel gears and the stem holding the bevel gears, used for in-plane sample rotation, all parts including a spur gear were converted to Mo (see Figure B.9). During the conversion, the designs were modified to allow for a more robust operation and increasing

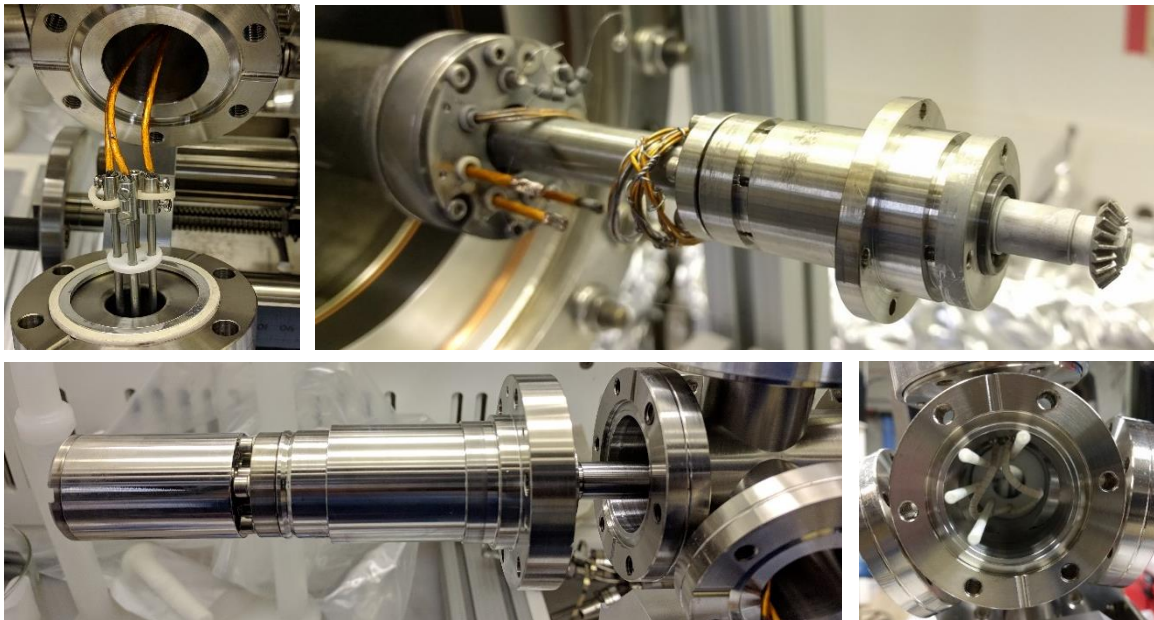


Figure B.10 Clockwise from left-top: Feedthrough showing Kapton power lines for the sample heater. Right-top: Kapton lines for the sample heater and back-side illumination bulb, near the manipulator head. Right-bottom: new alumina tubing installed as a conduit for new Molybdenum power lines for sample heater. Left-bottom: UHV design’s magnetically coupled-rotary, with a mini-flange employed for another magnetically coupled rotary, to provide both in-plane and out-of-plane rotation to the sample, without using bellows.

lifetime between maintenance operations. For example, to encapsulate bearings in place, rotating screws (which would come undone, over multiple rotations and continuous heat cycling) were replaced with screws holding the stationary race of the bearing, reducing moving parts (and rotating screws). All moving parts were lubricated with Inficon graphite lubricant with iso-propyl-alcohol as the lubricating agent. Upon heat cycling to 1200C and two weeks of baking at 200C, the parts were still found to be ‘sticky’ but operating under an Arsenic overpressure and constant use, led to smoother functioning within the first week of normal

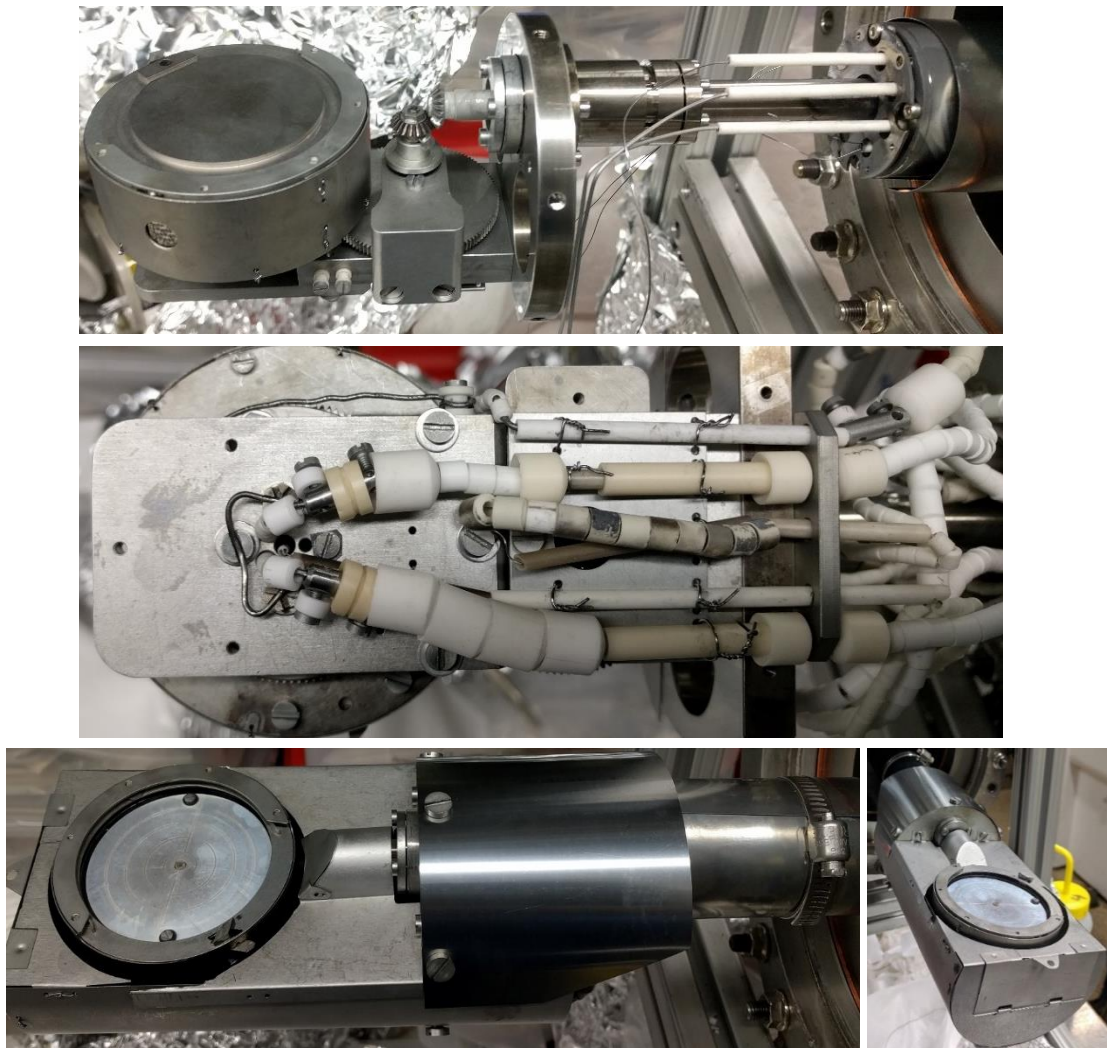


Figure B.11 The top panel shows the modified head assembled with Mo wires coming out of ceramic conduits. The center panel shows the Mo wires not connected to the sample heater behind the head, with ceramic beads insulating all the parts. The bottom panel shows the completed manipulator with 3 shields fully covering the wires regardless of out-of-plane rotation position.

operation under vacuum. It is believed that Arsenic dust acted at the final lubricant, while the initial graphite lubricant prevented cold welding during assembly, heat cycling and baking.

With the opportunity to re-design the substrate manipulator, it was decided to add a Type-K thermocouple (see Figure B.11) to monitor the temperature of the bottom plate of the assembly. The location of the Type-K thermocouple was chosen to be such that it would give a direct measure of a part that was previously stainless steel (prior to Nov 2017) and yet was part of the thermal sink of the sample holder assembly via the cryo-panel, in case the heater was powered off. The sample manipulator, during normal operation was used for both: growths up 650C for GaAs QWs and sub-zero Celsius growth of Aluminum superconducting layer and Arsenic cap layers. As Type-K thermocouples can be used to read temperatures from -200C to 1200C a location ideally not expected to cross few hundred Celsius during normal operation was chosen.

Table B.1 VG V80H MBE substrate manipulator Type-C vs. Type-K thermocouples

Current (A)	Voltage (V)	Power (W)	Thermocouple Type-C (C)	Thermocouple Type-K (C)
0	0	0	0	-40
1.0	7.5	7.5	190	54
2.0	12.5	25	425	109
3.0	17.8	53	605	140
4.0	23.1	92	786	253
5.0	29.1	146	929	382
6.0	34.9	209	1037	396
7.0	41.1	288	1154	473

Table B.1 shows how the Type-C substrate thermocouple, directly behind the sample holder and the Type-K thermocouple correlated during a 1200C heat cycle, with a blank Tungsten block rotated at 10 rpm. The test results showed the assembly was far warmer than originally believed and this heating was the primary reason for the discoloration of the previously stainless-steel parts.

The results from measuring the temperature of the newly installed Type K thermocouple, indicated that during the growth of a GaAs QW at surface temperature of $640\pm 10\text{C}$, at a heater power of about 175 Watts, the previously stainless-steel assembly was between 375-400C. The high flux of unintentional dopants like Manganese, Zinc among other constituents of steel, being outgassed at that temperature were detrimental to the material quality and electron mobility in an ultra-high mobility quantum well. For comparison, InAs QWs were grown at about 75 Watts and InSb QWs were grown at a further lower power.

The Kapton insulated wiring (see Figure B.10) was also removed and replaced with 0.040” Mo wire through alumina tubes. Crimp connectors were used to make a permanent union of heater wires and thermocouple wires where required, while all remaining unions were made out of Mo barrel connectors, rather than the previously used steel.

The singular large Mo heat shield surrounding the manipulator’s hot zone and shielding it from continuous exposure to all growth species in the MBE chamber was re-designed into multiple smaller pieces, to create a better containment. A key focus of the work was to significantly reduce the surface area of the shield capable of re-depositing onto the sample.

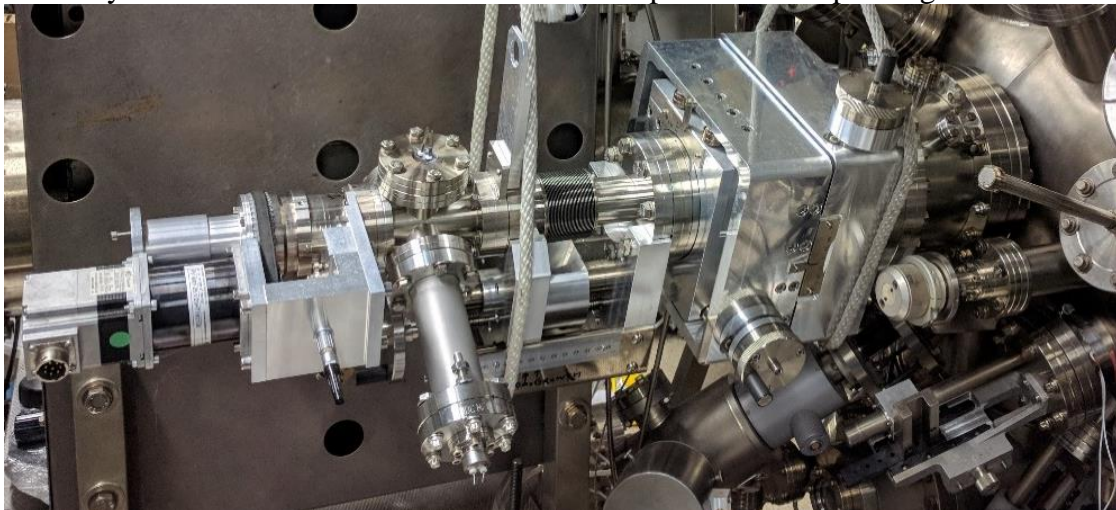


Figure B.12 shows the manipulator reinstalled on the chamber, after modifications lasting six months. Picture taken April 2018. The newly added Type-K thermocouple is evident in the fore-ground, with Type-C thermocouple poking up top.

This is now expected to lead to a major reduction in particulate density (especially during sample rotation and manipulation) and also in reducing cross contamination of primarily Arsenides and Antimonides by unintentional heating of the shield. A picture of the modified shield is shown in Figure B.11. The updated sample manipulator is shown in B.11 and B.12.

B.2.5 Pyrometry and band-edge spectrometry

Pyrometry allows for a non-contact measurement of the sample temperature based on the intensity of emitted black-body radiation and is known to be a reliable approach to temperature measurement in an MBE. In March 2017, the III-V MBE was equipped with a LumaSense IGA 6/23 Advanced pyrometer with a spot size of $\sim 3\text{mm}$ on the sample surface (see Figure B.13). Operating principle of a pyrometer can be found elsewhere [208]. This pyrometer has a center wavelength of $2.3\mu\text{m}$ and can detect an integrated intensity from 2.0 to

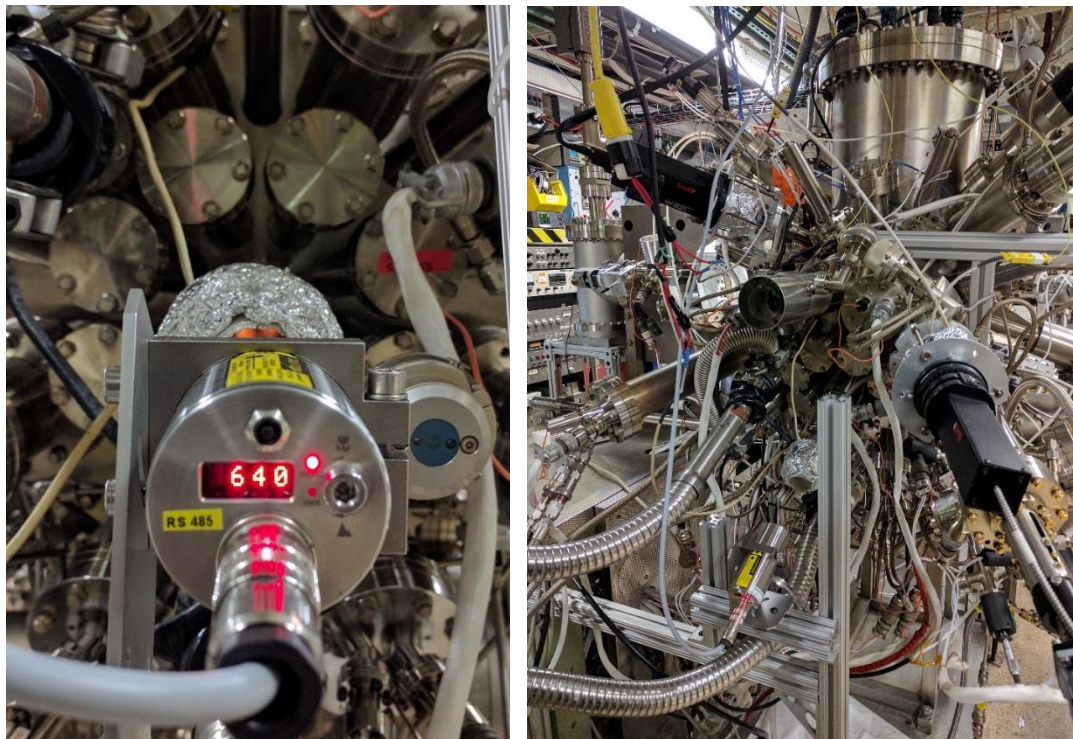


Figure B.13 Left panel shows the new Lumasense pyrometer in action, measuring the temperature of a GaAs quantum well in growth at 640°C . The right panel shows the two black boxes for Bandit – lamp and detector – used to measure temperature by band-edge spectrometry.

2.6 μm . Selection of a pyrometer capable of detection at this wavelength is of direct consequence to the growth of narrow band gap materials like InAs and InSb. Due to a strong absorption edge at the band gap of a semiconductor, the wavelength range that the absorption edge can shift in (with varying temperature) should be avoided in selecting a pyrometer for that material. A 2.3 μm pyrometer would primarily be sensitive to the temperature of epilayers of InAs, InSb and InAsSb. For GaAs, InP and GaSb, a 2.3 μm pyrometer is transparent to the absorption edge and is hence sensitive to the substrate-sample block interface (typically Gallium or Indium liquid metal). Using pyrometers specifically capable of ‘above gap’ sensing for the relatively larger band gap materials would aid in more accurate determination of surface temperature for such materials.

While a pyrometer can measure temperature for a wide variety of materials, it requires calibration for every specific growth. This work uses known RHEED reconstruction transitions or oxide desorption as a relative reference for calibration of the pyrometer temperature and allows for reproducible measurement of sample temperature. For materials smaller in band gap than the 2.3 μm wavelength (longer wavelength) of the pyrometer, it was observed that sample to sample pyrometer recalibration was not required and led to reproducible temperature-RHEED reconstruction transition correlations. For materials with a larger band gap than 2.3 μm (shorter wavelength), a minor recalibration was typically needed. Figure B.13 shows the new pyrometer at 640C during a GaAs QW growth. Pyrometer temperature, feedback controlling the substrate power is expected to reduce manual intervention, increase reproducibility between growths (and low temperature doping routines of QWs). It is also expected to lead to a strict composition control in sensitive ternary, quaternary and quinary compounds containing both Arsenic and Antimony (like InAsSb) as the incorporation ratio and sticking coefficient of

As and Sb are extremely sensitive to minor variations in temperature. Growth of both nanowires and quantum wells of InAsSb (see chapter 6) relies heavily on the pyrometer to maintain stoichiometry during growth.

Using the absorption edge of the semiconductor as another sensitive temperature probe, k-Space Associates BandiT²⁵ is a band edge spectrometry tool capable of accurately estimating temperatures. In this work, growth of GaAs compounds and materials on InP substrate (except InAs QWs) have benefitted from the use of band edge spectrometry. In absence of a pyrometer, the blackbody spectrum tool incorporated within the band edge spectrometry suit can be used

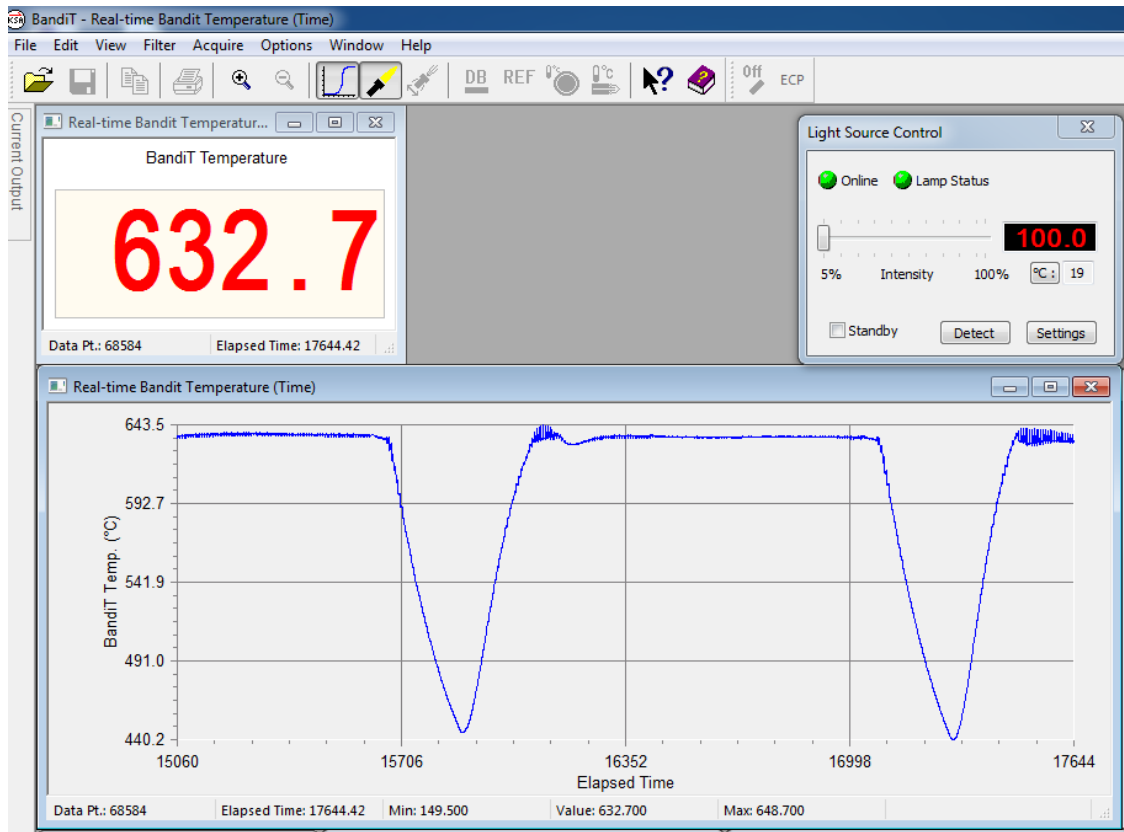


Figure B.14 A screenshot of Bandit software for band-edge spectrometry showing the temperature measured to be 632.7°C. The temperature vs. time plot shows the two short-period-superlattice (SPSL)

Silicon delta doping layers before and after the quantum well growth, where the temperature was lowered from the ~630°C growth temperature to <480°C. The minimum temperature during the thermal cycle ~440°C.

²⁵ 2.75" CF window mounts for Bandit lamp and detector were machined by Tobias Brown-Heft.

for estimation of GaSb, InAs and InSb materials. Accurate determination of temperature on a GaAs surface is of key importance when doping at low temperature (less than 480C, in a 640C QW structure growth, see Figure B.14) and when growing (110) GaAs based materials (390-440C) and ErAs on GaAs (300-350C). Some high temperature pyrometers are incapable of measuring temperatures in this range and band edge spectrometry is hence essential for such applications.

B.2.6 Residual Gas Analysis

Quadro pole mass analyzers are essential for the successful operation of any MBE. This work extensively makes use of Stanford Research RGA200 Residual Gas Analyzers, equipped with a Channel Electron Multiplier (CEM). Careful analysis of mass species, often in the 1-100amu range can lead to improved material quality and early detection of eventually catastrophic failures. While use of RGAs with He (4 amu) is the most common, detecting very small leaks by looking for an inversion in the peak heights of masses 14 and 15 amu is of the greatest consequence (mass 15 is about 3 times mass 14 under normal operation without a leak). It was observed that the pumping configuration (speed, type of pump) and placement of RGA play an important role in the ability to detect small leaks, allowing for achievement of chamber base pressure at the X-Ray limit of an ionization gauge ($\sim 3 \times 10^{-11}$ Torr).

While the detailed operation of an RGA is detailed elsewhere [209], some of the lessons learnt from operation of the SRS RGA in the III-V MBE have been mentioned below. Some details are also covered by B. Shojaei [137]. All SRS RGAs in the UHV system, when possible, were operated at a gain of 1×10^6 with a slow scan in the range 1-100amu. The filament current was maintained constant at 3.5 mA. It was observed that differential pumping in the MBE

growth chamber due to a small cryo-panel, lead to significant difficulties when detecting leaks. The He used for leak checking the lower half, was restricted in reaching the upper half and lead to leaks as large 1×10^{-9} Torr go untraceable. A dedicated RGA each for the upper half of the growth chamber, lower half of the growth chamber and the preparation chamber was installed in 2018 as shown.

It was also determined that reduced pumping speed, in general, lead to a better detectability of a leak especially with the ratio of masses 14 and 15. For leak detection, immediately post bake without liquid nitrogen, all cryopumps were closed prior to leak checking, and only one ion pump >90% closed was used to pump the continuous vacuum space exposed to the RGA. With the cells cold (room temperature typically, except for In, Ga) post bake the chamber idled at 1×10^{-10} or better pressure, under such a reduced pumping.

While cryopumps can pump Helium effectively if cooled below 10K, the increased pumping speed of nitrogen (leading to the larger 14 and 28 peaks), was found to have the potential to make the leak untraceable by reverting the 14/15 ratio to the normally expected value. Also, it was observed that cryopumps typically add to the helium partial pressure, increasing the baseline. This is believed due to the prior handling and packaging of the pumps. A new cryopump is sealed under high purity helium for shipment, filling the charcoal with Helium Thorough baking of the cryopump showed that this additional Helium source from the charcoal could be effectively removed. Sublimation ion pumps, especially triode ion pumps designed to pump noble gases more effectively than diode ion pumps, can increase the helium pumping speed and reduce chance of detection of a small or slow leak, in case where the RGA is placed behind the ion pump (III-V MBE from April 2016 to April 2018). It was determined that turning the ion pump off (gate valve full open) and using another pump for vacuum was

the best course of action. In certain large leaks and most small leaks, presence of a 32amu peak corresponding to oxygen was not observed and hence should not be used a metric for a leak free system.

On critical items containing bellows, quartz windows and items as large as the source flange gasket, effective leak detection required containment of the equipment in a bag. On UHV parts where a rotatable CF flange was connected to another rotatable CF flange, an exceptionally high occurrence of leaks of was encountered, especially if the specific installation geometry allowed for torque on the flange (e.g. valves, elbows).

For efficient detection of slow leaks, and establishment of a correlation between material quality and residual gas partial pressure (like oxygen, which is not traceable under normal operation) specialized high performance RGAs capable of detection down to 10^{-16} Torr partial pressure should be used [210], [211].

B.2.7 Other modifications

1. Relocating and replacing effusion cells and source materials –
 - a. A Cold-lip Veeco SUMO cell for Aluminum was installed and its operating procedures were developed and are noted.
 - b. With a view towards increasing uniformity over a 2” wafer, self-shuttered GaTe cell was relocated to different port, in place of Erbium.
 - c. A new 2.75” cell for Erbium, with an in-built shutter was installed, opening up the older cell port.
 - d. Indium and Aluminum effusion cells were swapped so that Indium and Gallium were the lowest two cells in the MBE reactor. It was discovered that, due to the

low melting point of Indium and the heating up of the cell separators (conduction cooled by LN₂), stray Indium from the shutter was cross contaminating Aluminum from a higher port. This swapping of cell ports, to move Indium lower than Aluminum, is expected to reduce cross contamination between source materials.

- e. Chromium was added as an element, replacing Fe, to study effect of Chromium gettering on material quality and to study the use of Chromium as an intentional mid-gap trap in Antimonides, among other potential applications.
 - f. Gd effusion cell was replaced with a smaller effusion cell capable of a *nearly* flat-walled Ta crucible. As Gd is operated while molten, a shallow angle installation of the effusion cell requires flat-walled crucibles to avoid the molten source material from dripping out of the walls of a conical crucible.
2. Due to the installation of new larger effusion cells like the e-Science TITAN (Ga, In) and Veeco SUMO (Al), effusion cell shutters for five out of the eight cells on the source flange were modified for a better coverage of the 2” wafer. The previous shutters were suitable for a 17x17mm sample but lead to constant growth on certain edges of a 2” wafer. To increase shutter operation reliability and reduce ‘splashing’ of source material, soft-action pneumatic shutters were used on critical Al, Ga, In, As, Sb cells, while solenoid shutters were used for the rest. During shutter modifications, shutter rods were metal polished and moving parts were lubricated with MOS₂ spray lubricant and baked in air before being outgassed under vacuum.
 3. To reduce the base pressure of the load-lock during normal operation (previously between 5x10⁻⁸ to 5x10⁻⁹ Torr, after overnight pump-down), the load lock was equipped

with a new Titanium Sublimation Pump (TSP). The active pumps were also upgraded to a 300 l/s turbo pump backed by a scroll pump, for the second stage of pumping. The first stage of pump down was kept the same to a molecular drag backed by diaphragm pump combination or a scroll pump. Installation of a load-lock heater to heat the sample cassette to $\sim 150\text{C}$, is currently in progress. The new load-lock pumping configuration allowed for a typical operating pressure of 1×10^{-8} Torr to 1×10^{-9} Torr after 30 minutes (and TSP operation) and led to a base pressure of $6 \pm 3 \times 10^{-10}$ Torr after an overnight pump-down. This improvement has led to an improvement in the base pressure of the UHV preparation chamber connected to the load lock ($< 5 \times 10^{-11}$ Torr as compared to 1×10^{-10} Torr, after months of load lock operation), along with a reduction of O_2 partial pressure introduced into UHV.

4. To be able to continuously measure temperature during growth, window heaters were added on three windows for pyrometer and BandiT. A thermocouple temperature of $475 \pm 25\text{C}$ was maintained and on certain windows²⁶, no deposition of As or Sb was observed after a continuous growth campaign of 18 months. The temperature of the glass surface, in front of the optical components is expected to be more than 200C . Careful placement of the heater to heat the glass rather than the glass to metal flange was found to be essential (see Figure B.15).

²⁶ Construction and installation of 24VAC power unit for window heaters, was performed by Tobias Brown-Heft.

5. Sample blocks used for growth of high mobility 2DEGs of GaAs and InAs were redesigned²⁷ to create an overhang of 1mm on the edge of the 2” wafer (50mm). This ‘pedestal’ is expected to reduce the propagation of dislocations from the edge of the wafer and reduce the effective ‘droop’ of liquid Gallium used to bond the wafer to the Mo/Ta/W block, allowing for a better temperature uniformity over longer growths. Tungsten (W) blocks were introduced into service and it was noted that Gallium bonded Tungsten blocks far outperformed Gallium bonded Tantalum blocks. The W blocks were also more affordable per unit as compared to Tantalum. The power output required to desorb the native oxide off the surface of GaSb and GaAs was observed to be similar while the Gallium on the surface of Tungsten block remained uniform, unreacted and liquid post growth. Gallium on the surface of Tantalum showed signs of reaction, and non-uniform coverage with dry patches which was later confirmed by other sources [212].

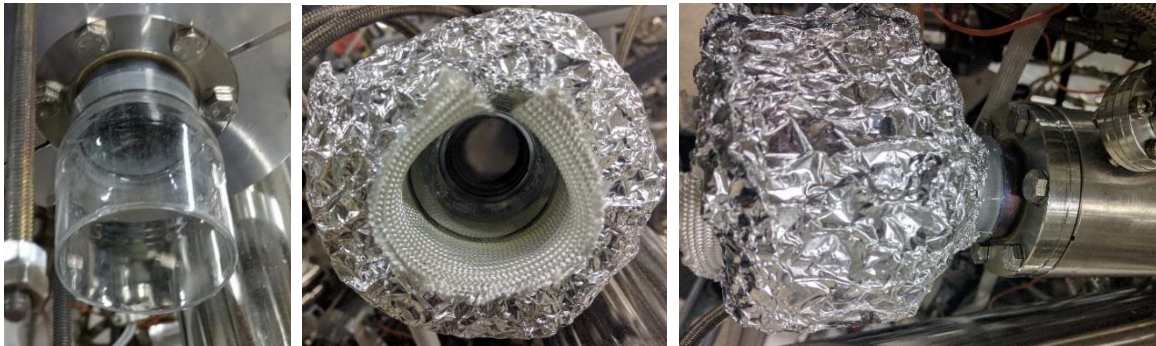


Figure B.15 The pictures above show a Bomco manufactured quartz window with a Molybdenum glass to metal seal capable of withstanding high temperatures. A 24VAC heater manufactured by MBE Control, Santa Barbara is installed on the window such that the center of the heater depth lies on the front edge of the glass window, creating a quasi-furnace to keep the front of the glass window hot. This prevents build-up of otherwise high vapor pressure volatile species like Arsenic and Antimony. The thermocouple embedded in the heater is operated at $\sim 475^{\circ}\text{C}$, and the glass temperature is expected to be in excess of $\sim 200^{\circ}\text{C}$ during growth. Over a course of 18 months, the windows were still found to be transparent for use in pyrometry and band-edge spectrometry.

²⁷ Redesigned by Dan Pennachio and MP and machined by Thermo-Shield US, Inc.

B.3 Atomic Hydrogen cleaning

Atomic Hydrogen cleaning has been reported to be essential for successful desorption of stubborn native oxides on the surface of certain III-V compounds like InSb [159]. Primarily oxides of Indium having lower vapor pressure require excessive heating in the MBE chamber ($>450^{\circ}\text{C}$) prior to which InSb decomposes. Atomic hydrogen reacts with the native oxides of Indium, Gallium, Arsenic and Antimony and leads to formation of pure III-V and water vapor. When the sample is maintained at an appropriately high temperature, water vapor from the sample surface can desorb along with more volatile oxides. This process, without any group V

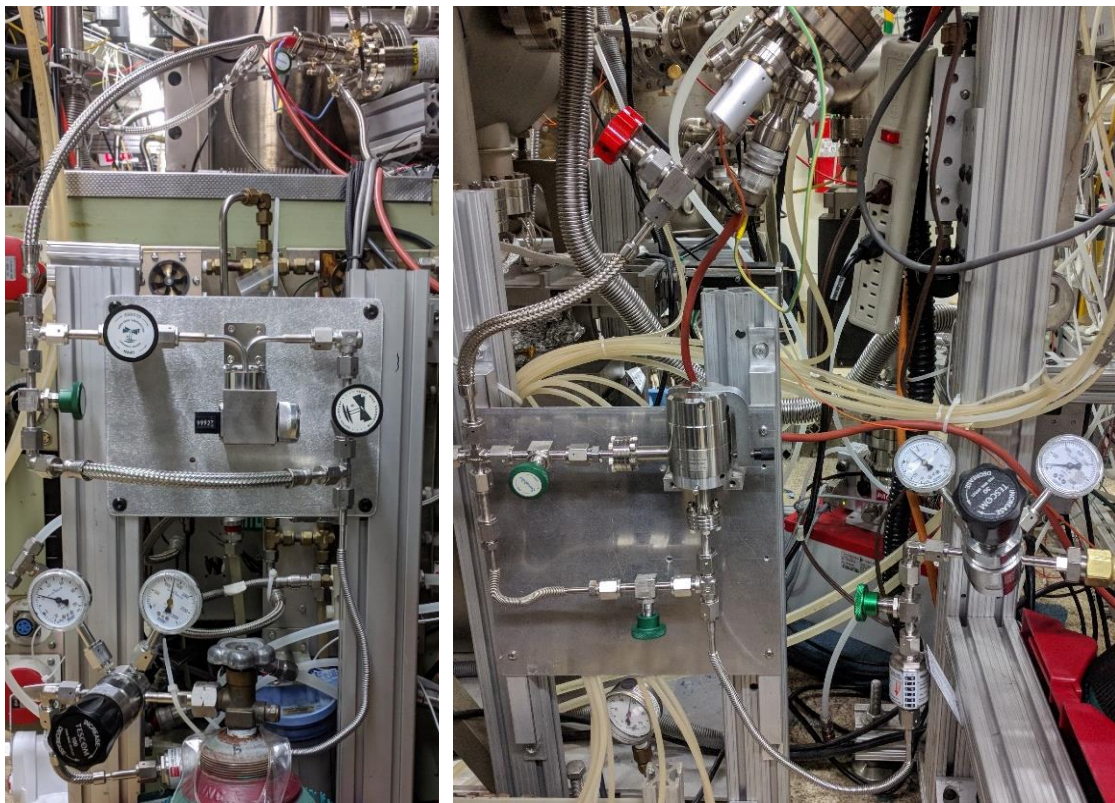


Figure B.16 The left panel shows the gas handling system for the atomic hydrogen source installed on the III-V Chemical Beam Epitaxy chamber, while the right panel shows a similar gas handling setup installed on the big-bi-directional transfer chamber. Both the setups have common parts and plumbing starting with the hydrogen gas cylinder (35 cu. ft.), a low-pressure VCR flanged regulator, followed by a SAES getters manufactured Hydrogen gas purifier and a UHV leak valve. The assembly has been baked and has metal sealed valves for safety cut-off and pump-out after maintenance.

overpressure, obviates the need for relatively higher temperatures which would otherwise require significant group V overpressure to prevent the III-V from decomposing.

As part of this work, atomic hydrogen cleaning has been used to prepare surfaces of InSb substrates for growth of InSb QWs and InSb nanowires for evaporation of epitaxial Aluminum. *In-vacuo* transfer of prepared samples to interconnected MBE chambers has been essential for utilizing the capabilities of atomic hydrogen cleaning with the interconnected UHV setup. Other uses of atomic hydrogen also include preparation of InAs and GaSb substrates prior to MBE growth and cleaning for various III-As,Sb nanowires for Scanning Tunneling Microscopy measurements.

The atomic hydrogen setup installed in the Palmstrom lab's big-bidirectional transfer chamber, prior to March 2018, was modified to improve base pressure of the host system post hydrogen cleaning. The 200°C bakeable apparatus relies on MBE Komponenten Hydrogen Atomic Beam Source (HABS). An addition of SAES Getters MC1-904F hydrogen purifier, has allowed for removal of H₂O, CO₂, O₂ and CO to < 100 ppt from a previously 5N pure source of hydrogen (see Figure B.16). Additionally, the turbo-molecular pump actively used during hydrogen cleaning has been upgraded to a HiPace 300H pump backed up a scroll pump. The new turbo pump is capable of pumping hydrogen and other lighter gases at a much faster speed, and also improved the compression ratio for light gases. The purification of source gas and improved pumping has allowed for a stable base pressure of 1×10^{-10} Torr after months of regular hydrogen cleaning, as compared to a previous base of $5-10 \times 10^{-10}$ Torr. It has also allowed for a faster pump-down post hydrogen cleaning.

In addition to the improvements made above, a nearly identical hydrogen cleaning apparatus was installed in the Chemical Beam Epitaxy growth reactor, for *in-situ* atomic hydrogen cleaning, based on an MBE Komponenten HABS (see Figure B.16). The CBE chamber is equipped with a diffusion pump for pumping metalorganics and hydrogen very effectively. Being a growth chamber, it also includes a RHEED and active sources of AsH₃, PH₃ and Sb. This allows for continuous monitoring of the sample surface for effective oxide removal and increases the available growth window for hydrogen cleaning with the possibility to expose sample surface to group Vs if needed. It has been reported that hydrogen cleaning under and impingent group V flux leads to the smoothest final surface [159].

B.4 Cryogenic sample stage



Figure B.17 The right panel shows the cryogenic sample stage manufactured by VG Semicon, without any plumbing attached to it. The left panel shows the new plumbing attached to the stage with thermal insulation (black). During operation ice builds up on joints not covered by insulation.

The cryogenic cold stage designed by VG Semicon and used as part of this work for evaporation of Aluminum and other superconductors (In, Nb, V, Ta, Pd) allows for the sample to be held close to 77K when used with liquid nitrogen. It also can be configured for use with liquid Helium, allowing for even lower temperatures (see Figure B.17). The stage is designed in three separate cooling zones (see Figure B.18). Zone 1 is in direct contact with the sample

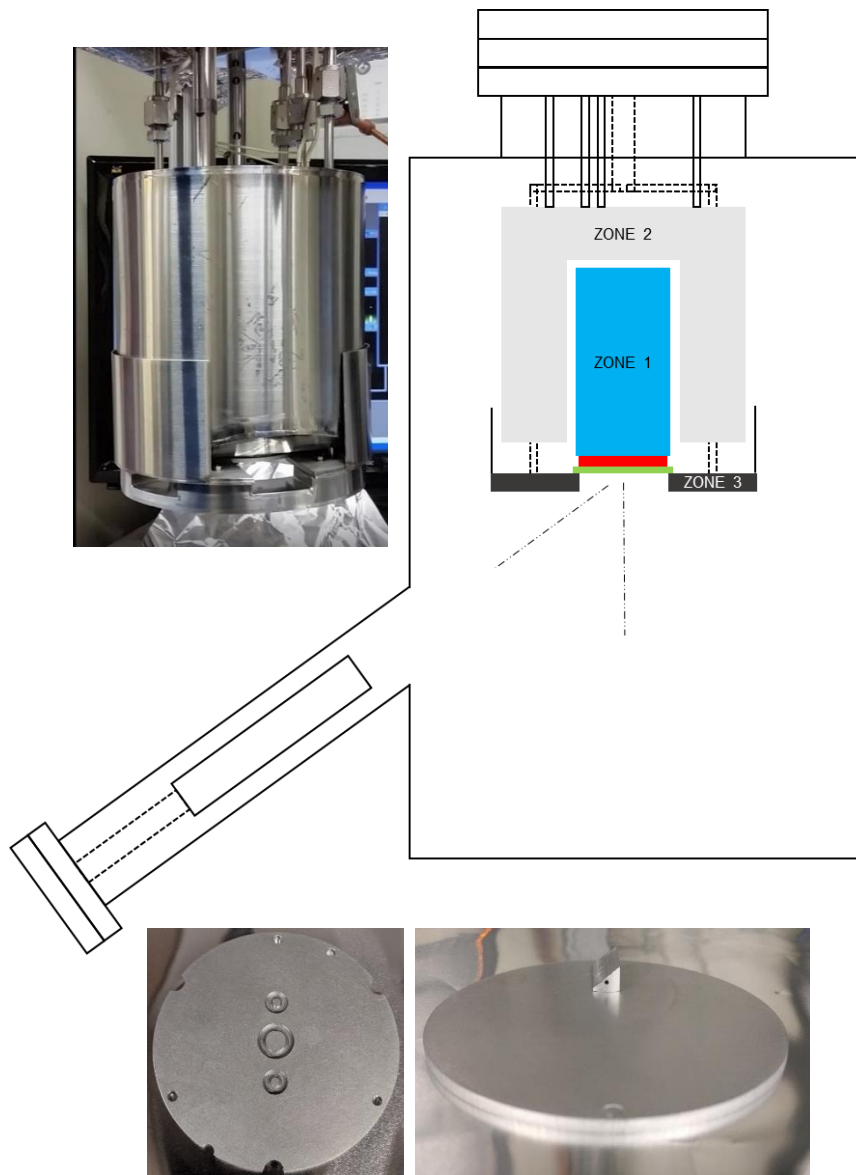


Figure B.18 Top-left: A picture of the cryogenic sample stage when it removed for modification and maintenance in June 2017. Top-right: Schematic of the cryogenic sample stage with 3 zones for storing liquid nitrogen. The heater is shown in red and the sample is shown in green. Effusion cell of aluminum evaporated aluminum at a 47° angle from the normal.

and can be cooled with liquid helium or liquid nitrogen. Zone 2 is the shroud and is designed for reducing radiative losses and increasing the 'hold time' of the stage at base temperature. Zone 3 holds the sample and can move vertically, allowing for to force the sample in direct contact with zone 1. This design relies on forced contact of the back of the growth block (typically Mo, Ta, W) and conductively cools the sample via the block. This conductive cooling provides enough cooling power to maintain sub 100 K temperatures, as measured by a thermocouple in close proximity to the sample, when evaporating with an effusion operating at ~1300 K. The cold stage, as part of this work, was also modified to increase reliability and reduce mean time before failure. Aluminum growth rate was calibrated with growth of thin aluminum films via a shadow mask and Atomic Force Microscopy was used to accurately measure the thickness. A Quartz Crystal Microbalance was also added for active monitoring of the growth, once calibrated. Typical growth rates of 10 nm/hr. were used for growth of Aluminum.

Angle of evaporation of aluminum was determined by shadows of nanowires growth on blocks with 'wedges' of known angles. These wedges also allow for evaporation of aluminum from non-standard angles (shallow angle evaporation or near normal incidence) and implications of the same are relevant to the making of a qubit (see Chapter 7). Additionally, sample blocks with wobble stick holes at exactly 120 degrees were made to allow for in-plane rotation.

B.5 Load-lock for sample oxidation

Immediately following evaporation of Aluminum, oxidation of the aluminum surface was found to be necessary to freeze the aluminum. This prevented ‘balling up’ of the aluminum on the surface of InSb and led to uniform conformal superconductor layers, essential for MZM devices. A load-lock for loading samples in and out of vacuum was specifically equipped with the required features so as to make the process of sample oxidation faster, reproducible and reliable (see Figure B.19). The typical transfer times from the cryogenic sample stage to the load lock were noted to be between 4 to 7 minutes. The load lock with equipped with an Alcatel 5011 molecular drag pump back by a Varian SH-100 scroll pump. It was also equipped with a Pfeiffer wide range gauge capable of reading continuously from 10^{-9} Torr to atmosphere. All-metal plumbing for 5N purity oxygen along with a Teflon sealed valve was also incorporated. Plumbing to use the load-lock under normal operation with a nitrogen purge was also

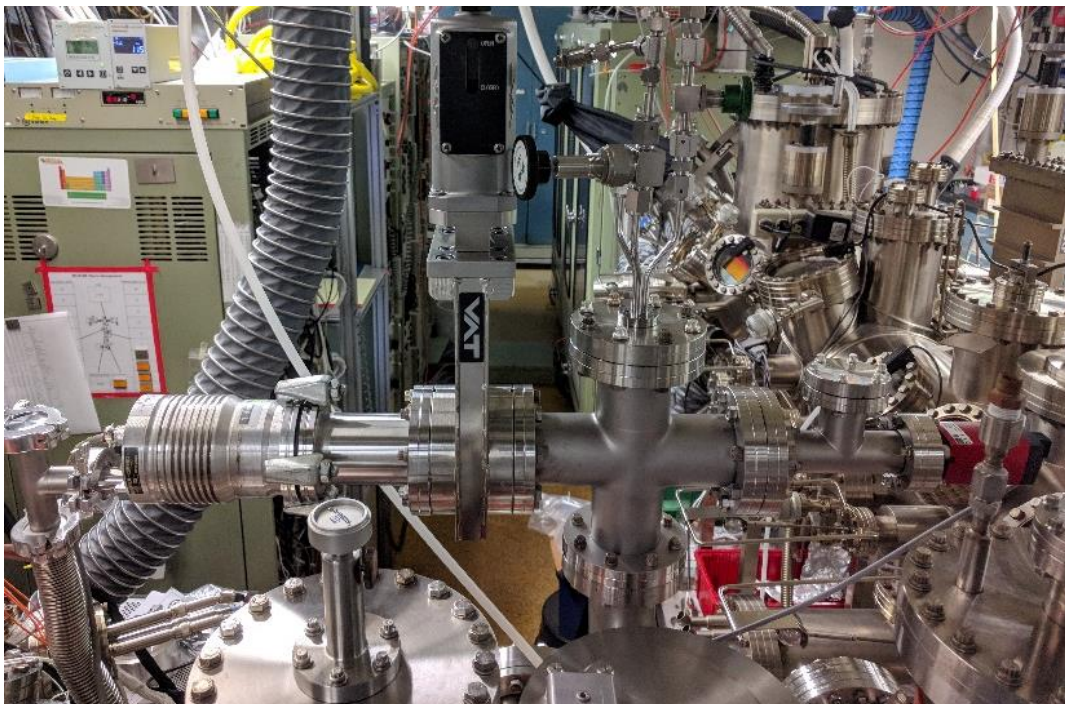


Figure B.19 Picture of load lock equipped with oxygen and nitrogen along with a wide-range gauge to read continuously from atmospheric pressure to high vacuum. This load lock is used to expose samples with aluminum evaporated at cryogenic temperatures to ~ 100 Torr of oxygen, within minutes of growth.

incorporated. The Teflon sealed valve allowed for an affordable alternative to a leak valve and was used to oxidize the samples at 100 Torr of oxygen for 15 minutes. The load lock was then purged with nitrogen and pumped back down, to allow for the sample to warm up to room temperature, prior to removal.

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Even though this work adds to the knowledge of superconductor-semiconductor systems and the more exotic topologically non-trivial Majorana Zero Modes, concrete evidence of exotic properties, like non-abelian braiding statistics, remains an enigma. In absence of direct measurable evidence, many have discounted the presence of Majorana Zero Modes or their usefulness. A consensus is only expected once the milestone of experimental topological quantum computation has been reached.

The improvement in understanding of superconductor-semiconductor and topological systems, in pursuit of Majorana Zero Modes, remains undeniable.

“The most savage controversies are about those matters as to which there is no good evidence either way.”

- *Bertrand Russell, ‘An Outline of Intellectual Rubbish’ (1943)*