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A Compact Model of Ferroelectric Field-effect Transistor

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Abstract- In this paper, we present a compact model of ferroelectric field-effect-transistor (FEFET). The model consists of a ferroelectric (FE) capacitor model and a Berkeley Short-channel IGFET Model (BSIM), a standard SPICE MOSFET model. The FE model, similar to the nucleation-limited-switching model, is based on the statistical multidomain dynamics of FE materials. The charge equality between FE and MOSFET is satisfied through the SPICE simulator. The model reproduces the steep switching in the reverse bias region observed in experimental FEFETs and the current drop at both major loop and minor loop switching. Α versatile inverted-memory-window (IMW) model can model the IMW behavior of FEFET that may be caused by charge trapping. We demonstrate that the reported model can accurately fit the published data of Fin-FEFET and FDSOI-FEFET under different bias conditions.

Index Terms—Compact model, ferroelectric, ferroelectric field-effect transistor (FEFET), hafnium zirconium oxide (HZO).

I. INTRODUCTION

erroelectric material has become one of the most promising candidates for future non-volatile memory (NVM) due to the discovery of ferroelectricity of thin-film HfO₂ in 2011 [1]. The compatibility with the standard CMOS technology of hafnium zirconium oxide (HZO) makes it suitable for integration with our current integrated circuits (ICs). By using HZO as the gate insulator of a MOSFET, FEFET gains the most interest as an FE-based NVM. It has been demonstrated on GlobalFoundries' 22nm and 12nm Fully-depleted-silicon-on-insulator (FDSOI) processes with memory windows up to 1.5V [2]. The endurance of FEFET has been shown to exceed 10^{10} cycles [3]. The polycrystalline nature of HZO also makes FEFET possibly used for multi-bit operations [4].

For circuit design with this up-and-coming FEFET-NVM technology, the designers require a SPICE-compatible compact model of FEFET, accurately capturing its electrical

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Fig. 1. (a) The equivalent circuit model of FEFET and (b) the charge equality between FE and MOSFET.

characteristics. Several FEFET models have been developed previously. One of the popular FEFET models is the Preisach-based compact model, which couples Preisach ferroelectric model with a BSIM model [5, 6]. Preisach model is a computationally efficient model that can capture the hysteresis loop of FE. However, it is purely empirical and cannot describe the multidomain polycrystalline physics of HZO. It acks scalability, variation, and stochasticity properties according to [7], which are important in FEFET simulations. Therefore, the nucleation-limited-switching (NLS) model is introduced, which can describe the statistical multidomain properties of HZO [8-10]. The FEFET models using the NLS framework are reported in several works [11, 12]. However, the steep-switching and inverted-memory-window cannot be described by the NLS model.

In several recent experimental reports, a steep subthreshold slope (<60mV/dec) has been seen in FEFET [13-15]. There are many explanations for this effect: negative capacitance (NC), channel percolation or domain propagation, and so on [12, 16-18]. Several works include the percolation or domain propagation effects into their model and reproduce the steep switching characteristics; however, these works only showed the experimental trends and not a model fit to the data [12, 16, 17]. In addition to the steep switching, charge trapping is another critical issue in FEFET that may cause the IMW [14, 15]. [12, 19] include the charge trapping effect into their FEFET models using an analytical charge trapping model containing the integration over both energies and distances. Such an approach is computationally expensive, and unsuitable for compact modeling for a large circuit design purpose.

In this work, we develop a computational efficient compact model for FEFET using the NLS-based FE compact model we previously developed [20]. The steep-slope phenomenon as well as the IMW are captured using empirical equations that

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provide good fitting flexibility and computational efficiency. We demonstrate that this model can fit the experimental FEFET data well.

II. COMPACT MODEL

A. Equivalent circuit & FE model

Fig. 1a shows the equivalent circuit of our FEFET compact model. A FE capacitor is connected to the MOSFET gate, modeled by the BSIM model [21, 22]. The total charge on the FE capacitor (Q_{FE}) has to equal the total charge on MOSFET (Q_{MOS}). Since the electric field on FE varies with the channel position, directly making FE and MOSFET in series is not entirely physical. However, we choose to build the compact model in this way to achieve a good computational speed. Then, the OMOS is computed by the BSIM model, and OFE is calculated by the FE compact model in [20], rewritten here in (1). This FE model considers the statistical multidomain dynamics of polycrystalline FE where $P_{\rm R}$ is remanent polarization, $E_{\rm a+,-}$ are the activation fields at $E_{\rm FE}$ >0 and $E_{\rm FE}$ <0 respectively, $E_{\rm FE}$ is the electric field, η is the random variable describing the activation field distribution on different grains, P_{η} is the polarization for each η group, τ_0 is the characteristic time for a very large $E_{\rm FE}$, α , β and γ are fitting parameters, t_i is the time when $E_{\rm FE}$ polarity changes. We make E_{a+1} to be V_{DS} dependent as (1c) to capture the variation in channel potential profile at different V_{DS} where E_{ah+a} are the activation fields at high V_{DS} and E_{a0+a} are the activation fields at 0 V_{DS} . The total polarization is the average of P_n using (1d), where Prob (η) is the probability of η and $f(\eta)$ is the probability density function. The total charge is $P_{\rm FE}\,$ plus the background dielectric charge ($\varepsilon_{\rm FE}V_{\rm FE}\,/\,t_{\rm FE}$) times the area ($A_{\rm FE}$) where $\varepsilon_{\rm FE}$ is the background dielectric constant and t_{FE} is the thickness of FE.

$$P_{\eta}(t) = P_{R} - \left(P_{R} - P_{\eta}(t_{i})\right) \exp\left(-\left(\int_{t_{i}}^{t} \frac{1}{\tau(t')} dt'\right)^{\beta}\right),$$

if $E_{FE}(t) \ge 0,$
$$= -P_{R} + \left(P_{R} + P_{\eta}(t_{i})\right) \exp\left(-\left(\int_{t_{i}}^{t} \frac{1}{\tau(t')} dt'\right)^{\beta}\right),$$
(1a)

if
$$E_{\text{FE}}(t) < 0$$
,
 $\tau(t) = \tau_0 \exp\left(\left(\frac{\eta E_{\text{a+},-}}{|E_{\text{FE}}(t)|}\right)^{\alpha}\right)$,

$$E_{a+,-} = \left(E_{a+,-} - E_{a0+,-}\right) V_{DS}^{\gamma} + E_{a0+,-}, \qquad (1c)$$

(1b)

$$P_{\rm FE}(t) = \sum P_{\eta}(t) \operatorname{Prob}(\eta) \cong \int_{0}^{\eta \max} P_{\eta}(t) f(\eta) d\eta, \qquad (1d)$$

$$Q_{\rm FE} = A_{\rm FE} \left(P_{\rm FE} + \varepsilon_{\rm FE} V_{\rm FE} / t_{\rm FE} \right), \tag{2}$$

Since both the FE and BSIM models can only give charge as a function of voltage and not the other way round, we need to ensure the charge equality numerically. We utilize the solver in the SPICE simulator by using two current sources whose value equals Q_{FE} and Q_{MOS} , respectively. As shown in Fig. 1a, these two current sources form a current loop, and SPICE will automatically make sure they cancel each other. Fig. 1b shows a simulated Q_{FE} and Q_{MOS} using this method, from which we can see that these two charges are equal.

B. Steep-switching (SS) model

The experimental I_D -V_G FEFET data from several research groups show a sub-60mV/dec slope in the reverse sweep [13-15]. This has been attributed to a transient NC (TNC) effect in [18], but it also appears under DC conditions [13], implying that it could be due to the intrinsic NC. The percolation theory has also been proposed to explain the steep switching in [12, 16], where they used an effective threshold voltage shift to produce the steep slope. Another theory is the low electric field domain propagation which says the switching rate is dominated by domain propagation at the low electric field which gives higher switching rate [12, 17]. They modified the NLS model to show the sub-60 mV/dec slope. Due to the multiple reasons for the steep switching, we propose a phenomenology model.

We mainly adopt the idea of percolation theory, but it does not have a simple physical model and requires Monte Carlo simulation which is too computationally expansive. Thus, our SS model uses the concept of threshold voltage shift to model the sudden current drop [12, 16]. As shown in (3a), the internal gate voltage used in calculations (V_{MOS}') is the node voltage (V_{MOS}) pulse a shift (ΔV). ΔV is a function composed of ΔV_1 and ΔV_2 as (3b) where they are the voltage shift functions for major loop forward and reverse sweepings, respectively. The variables, a, b, c1,2, d1,2, e1,2, and f1,2, in (3) are empirical parameters. From percolation theory, the threshold voltage shift happens when $P_{F\!E}$ is smaller than a certain value [12, 16]. Here, e1,2 determine where the voltage shift will happen, a and b control the smoothing between ΔV_1 and ΔV_2 , and c1,2, d1,2, and f1,2 control the amplitude and the slope of this voltage shift. However, we have also observed a different current drop in the minor loop of experimental data (such as shown in Fig. 3) which is much smoother and cannot be covered by (3). Thus, we introduce a current multiplication factor (4) with m_1 to m_5 as the fitting parameters, which can be used to model this current decay. m2 and m5 determine the place where this current decay appears on PV plane, and the other parameters control the amplitude and smoothness of this function.

$$V_{\text{MOS}}' = V_{\text{MOS}} + \Delta V, \qquad (3a)$$
$$\Delta V = 0.5 \Delta V_2 \left(\frac{\Delta V_1}{\Delta V_2} - 1\right) \tanh \left[a\left(V_{FE} - b\right)\right] + 0.5 \Delta V_2 \left(\frac{\Delta V_1}{\Delta V_2} + 1\right), \qquad (3b)$$

$$\Delta V_{1,2} = 0.5c_{1,2} \left\{ \tanh\left[d_{1,2} \left(P_{\rm FE} - e_{1,2} P_{\rm R}\right)\right] - 1 \right\} + f_{1,2}, \qquad (3c)$$

$$I_{\rm DS} = I_{\rm DS}' \times M, \qquad (4a)$$

$$M = 1 - 0.25 \left\{ \tanh\left[m_{1}\left(P_{FE} - m_{2}P_{R}\right)\right] - 1\right\} \times \left\{\left(1 - m_{3}\right) \tanh\left[m_{4}\left(V_{FE} - m_{5}\right)\right] + \left(m_{3} - 1\right)\right\},$$
(4b)

C. Inverted-memory-window (IMW) model

The IMW is caused by charge trapping (CT) [14, 15]. If we want to model CT, we need to consider the quantum mechanical tunneling and the integration over both energy and distance [12, 17, 19]. However, this is too time-consuming for a compact model. Therefore, we propose a phenomenological IMW model that is coupled with the FE model and does not require additional computational power for the model convergence. Based on observation, the IMW happens in reverse sweeping, and the FE charge is not large enough. Therefore, the model is given by (5) and is activated during the reverse sweep when $P_{\rm FE}$ is smaller than a threshold polarization P_t where t_i is the time when reverse sweeping happens. The time constant τ_{nw} is now determined by the corresponding electric field E_t at t_i and a new activation field $E_{\rm a,IW}$ to tune the switching rate. Fig. 3 shows that our model can reproduce the IMW effect in I_D-V_G curves and Q_{FE}-V_G loop. The biggest advantage of this model is that we don't need to worry about the interaction between FE and CT which will increase the difficulty of convergence for solving the charge equality and the fitting complexity that people need to iteratively tune both models to get the good fitting.

if
$$dV_{\text{GS}} < 0$$
 and $P_{\text{FE}} < P_{\text{t}}$,
 $P_{\eta}(t) = -P_{\text{R}} + (P_{\text{R}} + P_{\eta}(t_{\text{i}})) \exp\left(-\left(\int_{t_{\text{i}}}^{t} \frac{1}{\tau_{\text{nw}}(t')} dt'\right)^{\beta}\right),$ (5a)
 $\tau_{\text{nw}}(t) = \tau_{0} \exp\left(\left(\frac{E_{\text{a,IW}}}{|E_{\text{FE}}(t) - E_{\text{t}}|}\right)^{\alpha}\right),$ (5b)

III. RESULTS

We validate our model by fitting the published FEFET data. We model both Fin-FEFET and FDSOI-FEFET by coupling this FE model with BSIM-CMG [21] and BSIM-IMG [22]. respectively. Fig. 2 shows the fitting results of an FDSOI-FEFET [14] and a Fin-FEFET [23]. The model can be used for both SS and non-SS cases at different V_{DS} . The difference in the MW at different V_{DS} is captured by (1c). Fig. 3a shows the validation with the different minor loops of the FEFET for different maximum gate voltages (V_{MAX}) [14]. As we can see the SS is reproduced by adding a voltage shift when $P_{\rm FE}$ is smaller than a certain value. The charge shows a steep switching as well as the current at the corresponding P_{FE} . For $V_{MAX}=1.2V$, the smoother current drop different from the SS at $V_G=1V$ is captured by (4) which activates in minor loops. For IMW at $V_{MAX}=1.0V$, from Fig. 3b, we can see that the charge decreases when reverse sweeping happens and P_{FE} is smaller than Pt which produces the IMW effect.

IV. CONCLUSIONS

We have presented a compact model of FEFET. The FE switching is modeled by a statistical multidomain switching model, which is coupled with the BSIM SPICE model with a subcircuit to achieve charge equality. To model the SS and IMW phenomena, we apply empirical models which are flexible enough to accurately fit the IV characteristics from experimental devices. We show that this model can fit Fin-FEFET and FDSOI-FEFET well at different bias conditions.



Fig. 2. Fitted $I_D\text{-}V_G$ curves compared to the experimental data of (a) FDSOI-FEFET with W=170nm, L=24nm, $t_{F\!E}$ =10nm, T=300K, E_{a0+} =2.7MV/cm, E_{a0-} =3.7MV/cm, E_{ab+} =3.5MV/cm, E_{ab-} =3.8MV/cm, a=2, b=-0.1, $c_{1,2}$ =1.2, d_1 =20, d_2 =500, e_1 =-0.5, and e_2 =0.4 [14] (b) Fin-FEFET with H_{FIN} =30nm, W_{FIN} =50nm, L=70nm, $t_{F\!E}$ =10nm, $E_{a0+,-}$ =4MV/cm, $E_{ab+,-}$ =4.6MV/cm [23] where symbols are the measurement and lines are the simulation.



Fig. 3. (a) Fitted I_D -V_G curves for different minor loops of the FDSOI-FEFET [14] where symbols are the measurement and lines are the simulation with W=170nm, L=24nm, t_{FE}=10nm, T=300K, $E_{a,+}=3MV/cm$, $E_{a,-}=3.2MV/cm$, a=2, b=-0.2, c_{1,2}=1.2, d₁=20, d₂=500, e₁=-0.3, e₂=0.45, m₁=600, m₂=0.6, m₃=1e-4, m₄=1.5, m₅=0.33, and P₁=0.33. The maximum gate sweep voltages are 1.0V, 1.2V, 1.6V and 3.0V. (b) The QV loops correspond to the IV curves.

REFERENCES

- T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, no. 10, 2011, doi: 10.1063/1.3634052.
- [2] S. Dünkel et al., "A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond," in 2017 IEEE International Electron Devices Meeting (IEDM), 2-6 Dec. 2017 2017, pp. 19.7.1-19.7.4, doi: 10.1109/IEDM.2017.8268425.
- [3] A. J. Tan *et al.*, "Ferroelectric HfO2 Memory Transistors With High-κ Interfacial Layer and Write Endurance Exceeding 1010 Cycles," *IEEE Electron Device Letters*, vol. 42, no. 7, pp. 994-997, 2021, doi: 10.1109/led.2021.3083219.
- [4] H. Mulaosmanovic *et al.*, "Switching Kinetics in Nanoscale Hafnium Oxide Based Ferroelectric Field-Effect Transistors," ACS Appl Mater Interfaces, vol. 9, no. 4, pp. 3792-3798, Feb. 1 2017, doi: 10.1021/acsami.6b13866.
- [5] K. Ni, M. Jerry, J. A. Smith, and S. Datta, "A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs," presented at the 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, June, 2018.
- [6] A. K. Saha and S. K. Gupta, "Modeling and Comparative Analysis of Hysteretic Ferroelectric and Anti-ferroelectric FETs," presented

at the 2018 76th Device Research Conference (DRC), Santa Barbara, CA, USA, 2018.

- [7] S. Deng *et al.*, "A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors Scalability, Variation, Stochasticity, and Accumulation," presented at the 2020 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, June, 2020.
- [8] A. K. Tagantsev, I. Stolichnov, N. Setter, J. S. Cross, and M. Tsukada, "Non-Kolmogorov-Avrami switching kinetics in ferroelectric thin films," *Physical Review B*, vol. 66, no. 21, Dec. 2002, doi: 10.1103/PhysRevB.66.214109.
- [9] C. Alessandri, P. Pandey, A. Abusleme, and A. Seabaugh, "Switching Dynamics of Ferroelectric Zr-Doped HfO2," *IEEE Electron Device Letters*, vol. 39, no. 11, pp. 1780-1783, Nov. 2018, doi: 10.1109/led.2018.2872124.
- [10] C. Alessandri, P. Pandey, A. Abusleme, and A. Seabaugh, "Monte Carlo Simulation of Switching Dynamics in Polycrystalline Ferroelectric Capacitors," *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3527-3534, Aug. 2019, doi: 10.1109/ted.2019.2922268.
- [11] Z. Wang *et al.*, "Depolarization Field Induced Instability of Polarization States in HfO2 Based Ferroelectric FET," presented at the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020.
- [12] Y. Xiang et al., "Compact Modeling of Multidomain Ferroelectric FETs: Charge Trapping, Channel Percolation, and Nucleation-Growth Domain Dynamics," *IEEE Transactions on Electron Devices*, pp. 1-9, 2021, doi: 10.1109/ted.2021.3049761.
- [13] H. Mulaosmanovic *et al.*, "Impact of Read Operation on the Performance of HfO2-Based Ferroelectric FETs," *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1420-1423, 2020, doi: 10.1109/led.2020.3007220.
- [14] Z. Wang *et al.*, "Cryogenic characterization of a ferroelectric field-effect-transistor," *Applied Physics Letters*, vol. 116, no. 4, 2020, doi: 10.1063/1.5129692.
- [15] M. N. K. Alam *et al.*, "On the Characterization and Separation of Trapping and Ferroelectric Behavior in HfZrO FET," *IEEE Journal* of the Electron Devices Society, vol. 7, pp. 855-862, 2019, doi: 10.1109/jeds.2019.2902953.
- [16] Y. Xiang *et al.*, "Implication of Channel Percolation in Ferroelectric FETs for Threshold Voltage Shift Modeling," presented at the 2020 IEEE International Electron Devices Meeting (IEDM), 2020.
- [17] Y. Xiang *et al.*, "Physical Insights on Steep Slope FEFETs including Nucleation-Propagation and Charge Trapping," in 2019 IEEE International Electron Devices Meeting (IEDM), 7-11 Dec. 2019 2019, pp. 21.6.1-21.6.4, doi: 10.1109/IEDM19573.2019.8993492.
- [18] M. Kobayashi, C. Jin, and T. Hiramoto, "Comprehensive Understanding of Negative Capacitance FET From the Perspective of Transient Ferroelectric Model," in 2019 IEEE 13th International Conference on ASIC (ASICON), 29 Oct.-1 Nov. 2019 2019, pp. 1-4, doi: 10.1109/ASICON47005.2019.8983568.
- [19] S. Deng *et al.*, "Examination of the Interplay Between Polarization Switching and Charge Trapping in Ferroelectric FET," presented at the 2020 IEEE International Electron Devices Meeting (IEDM), 2020.
- [20] C. T. Tung, G. Pahwa, S. Salahuddin, and C. Hu, "A Compact Model of Polycrystalline Ferroelectric Capacitor," *IEEE Transactions on Electron Devices*, pp. 1-4, 2021, doi: 10.1109/TED.2021.3100814.
- [21] J. P. Duarte et al., "BSIM-CMG: Standard FinFET compact model for advanced circuit design," in ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC), 14-18 Sept. 2015 2015, pp. 196-201, doi: 10.1109/ESSCIRC.2015.7313862.
- [22] S. Khandelwal et al., "BSIM-IMG: A Compact Model for Ultrathin-Body SOI MOSFETs With Back-Gate Control," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2019-2026, 2012, doi: 10.1109/TED.2012.2198065.
- [23] D. D. Lu, S. De, M. A. Baig, B.-H. Qiu, and Y.-J. Lee, "Computationally efficient compact model for ferroelectric field-effect transistors to simulate the online training of neural networks," *Semiconductor Science and Technology*, vol. 35, no. 9, 2020, doi: 10.1088/1361-6641/ab9bed.