A 34 Gb/s Distributed 2:1 MUX and CMU Using 0.18 μm CMOS

Ullas Singh, *Member, IEEE*, Lijun Li, *Student Member, IEEE*, and Michael M. Green, *Member, IEEE*

***Abstract*—A 34 Gb/s 2:1 serializer consisting of a CMOS MUX and CMU using a 0.18 μm SiGe BiCMOS process is presented. The serializer is based on distributed amplifier topology realized using spiral inductors. The circuit also includes an on-chip 2-channel 2^7-1 PRBS generator. The 34 Gb/s serial output has single-ended voltage swing of 380 mV with rise/fall time of 13 ps, and measured ISI is less than 5 ps p-p.**

***Index Terms*—Broadband communication, clock multiplier unit, CMOS integrated circuits, distributed amplifiers, high-speed integrated circuits, multiplexer, serializer.**

I. Introduction

TO SATISFY the bandwidth demands of global digital communications traffic, speed requirements for optical telecommunication systems are continually increasing. Current state-of-the-art systems are running at about 10 Gb/s. The next generation systems will operate at 40 Gb/s and above. Such high bit rates pose particularly challenging technology and design issues. Recent implementations of a 40 Gb/s MUX/CMU have been realized mainly in high speed InP and SiGe technologies [1]–[3]. With aggressive scaling, modern CMOS technologies have the potential for use in serial communication systems operating at data rates well above 10 Gb/s. A 2:1 MUX has already been shown to achieve operating speeds of 40 Gb/s in 0.12 μm CMOS [4]. To achieve the desired speed, designers have been relying on CMOS feature sizes continually scaling down (e.g., 2:1 MUX [4] or frequency divider [5]). However, scaling of submicron CMOS technology, which is desirable to optimize the digital performance, does not always translate to improved performance and speed in the analog blocks due to various factors such as lower voltage headroom, short-channel effects, and device mismatch. In addition, for high-speed circuit design the chip area is usually limited by passive devices (i.e., resistors, inductors and capacitors), not by transistor sizes in contrast to low-frequency circuits design with no passives. In general, scaling down the gate length is not a panacea for improving analog/high-speed circuit performance. The need for circuit improvement is very important in relaxing the device requirements as much as possible. For example, a 40 Gb/s CDR using a multi-phase *LC* VCO and novel architecture has been demonstrated in 0.18 μm CMOS technology in [6].

In this paper, we present circuit techniques used to design a 2:1 MUX and CMU operating at 34 Gb/s using 0.18 μm CMOS technology. Section II describes the overall circuit design and Section III presents chip measurement results. Conclusions are given in Section IV.

II. Design Description

This chip was designed using the Jazz Semiconductor SiGe120 BiCMOS process, which provides n-p-n HBTs with f_T of 150 GHz combined with 0.18 μm CMOS transistors with f_T of 57 GHz. Since our goal is to demonstrate a CMOS 34 Gb/s system, all critical blocks operating at full rate were designed using only MOS transistors; only the supporting circuitry (e.g., PRBS generator) used bipolar transistors.[1]

The chip block diagram is shown in Fig. 1. It consists of a 2:1 select circuit which receives two parallel channels of data each running at 17 Gb/s and multiplexes them to a serial output running at 34 Gb/s. A clock multiplier unit (CMU) generates a low-jitter 17 GHz on-chip clock signal from an external reference clock of 1.0625 GHz. The output of the select circuit is designed to match to 50 Ω; thus it drives the external load directly. The circuit also contains an internal 2^7-1 pseudorandom bit sequence (PRBS) generator which provides two 17 Gb/s channels as input to the MUX. Low-jitter performance (in particular, low ISI) is the primary goal of this design.

The design of the important blocks of the chip is described in the following sections.

A. Multiplexer Circuit

The 2:1 multiplexer portion of the circuit (Fig. 1) consists of a 34 Gb/s 2:1 select circuit, 17 Gb/s input retimers, data drivers and 17 GHz clock drivers. There are significant challenges in the design of circuits operating at such high frequencies. For example, the bandwidth of an optimized CML buffer with fan-out of 2 is only 7.2 GHz in this process. Hence, the maximum data rate it can handle with reasonable inter-symbol interference (ISI) using conventional circuit topology is approximately 10 Gb/s. To enable 34 Gb/s operation various broadband techniques were used depending on the input signal and bandwidth requirement and are described as follows.

The most crucial and challenging portion of the circuit is the final 2:1 select circuit which operates at the full rate (34 Gb/s). The schematic of a typical conventional 2:1 select circuit, along with

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U. Singh was with the University of California, Irvine, CA 92697 USA. He is now with Broadcom Corporation, Irvine, CA 92618 USA.

L. Li and M. M. Green are with the Department of Electrical Engineering and Computer Science, University of California, Irvine, CA 92697-2625 USA (e-mail: mgreen@uci.edu).

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[1]The design goal was to operate at 40 Gb/s. All simulations are done for 40 Gb/s, but measured output data rate was 34 Gb/s due to variations in the VCO oscillation frequency (explained in the CMU design section, Section II-B). The measured VCO frequency is 17 GHz, instead of simulated frequency of 20 GHz.

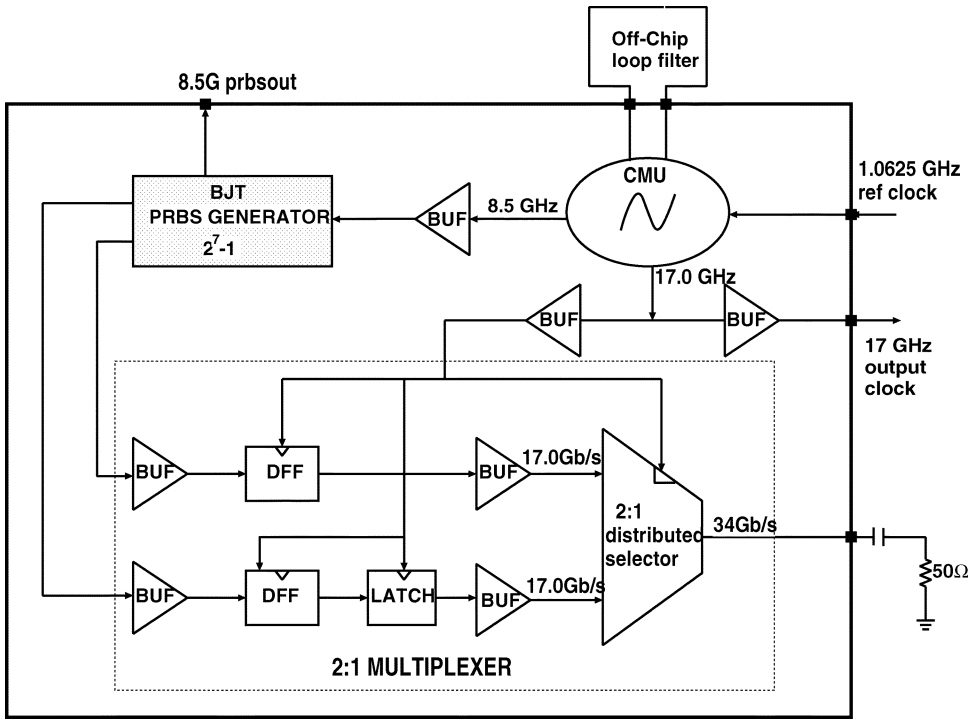

Fig. 1. 34 Gb/s multiplexer chip block diagram.

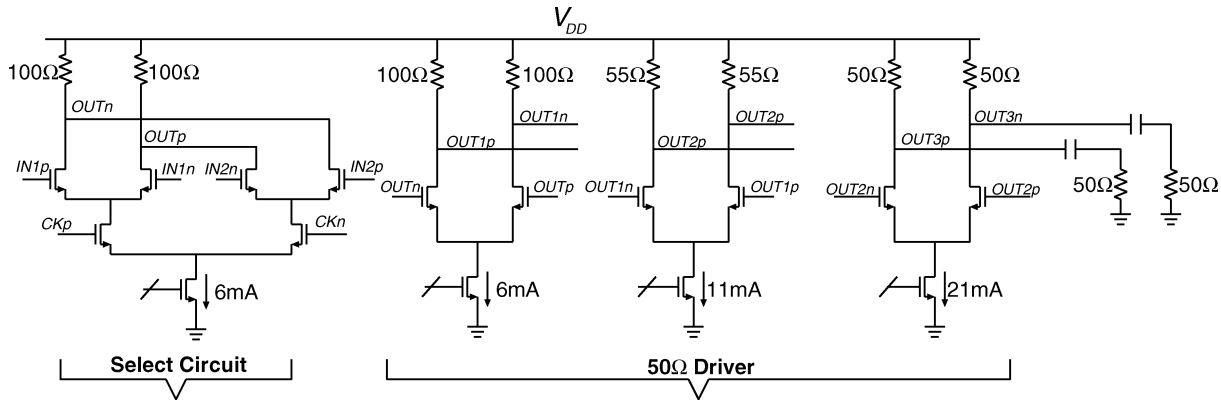

Fig. 2. Lumped select circuit with 50 Ω driver.

three stages of a conventional 50 Ω driver, is shown in Fig. 2. Using inductive peaking for all stages, the simulated eye diagrams for the 20 Gb/s input and 40 Gb/s output are shown in Fig. 3(a). The output eye is not sufficiently open, and the output ISI is 150 mUI. The main reason for this poor performance is the bandwidth limitation of the select circuit which needs to drive the large capacitive load of the output buffer. The output of the select circuit is degraded further as it goes through a chain of buffers, which also suffers from bandwidth limitation. To alleviate the bandwidth limitations one possible solution described in [1] is to combine the 50 Ω driver and the multiplexer. This does improve the performance, but both the input and output loading are increased significantly. To improve the bandwidth further, a different approach based on the well-known distributed amplifier structure can be used as demonstrated in [7], [8]. A proposed three-stage CMOS distributed select circuit is shown in Fig. 4. Each stage is just a standard series-gated CML select circuit. The input and output transmission lines are realized using spiral inductors combined with the inherent device capacitances. A wide bandwidth is achieved from this structure by ensuring that the cutoff frequencies of the transmission lines are sufficiently high. An added advantage is that if the characteristic impedance of the output transmission line is designed to be 50 Ω, then the output can be directly connected to an external 50 Ω load. The simulated input and output eye diagrams for this structure, shown in Fig. 3(b), show greatly improved performance with output ISI of only 60 mUI. An added advantage is that the performance improvement comes with reduced power consumption; the total power consumption for this circuit is the same as that of the last stage of a 50 Ω driver.

Although the Fig. 4 circuit is based on well-known distributed amplifier techniques, there are some important differences be-

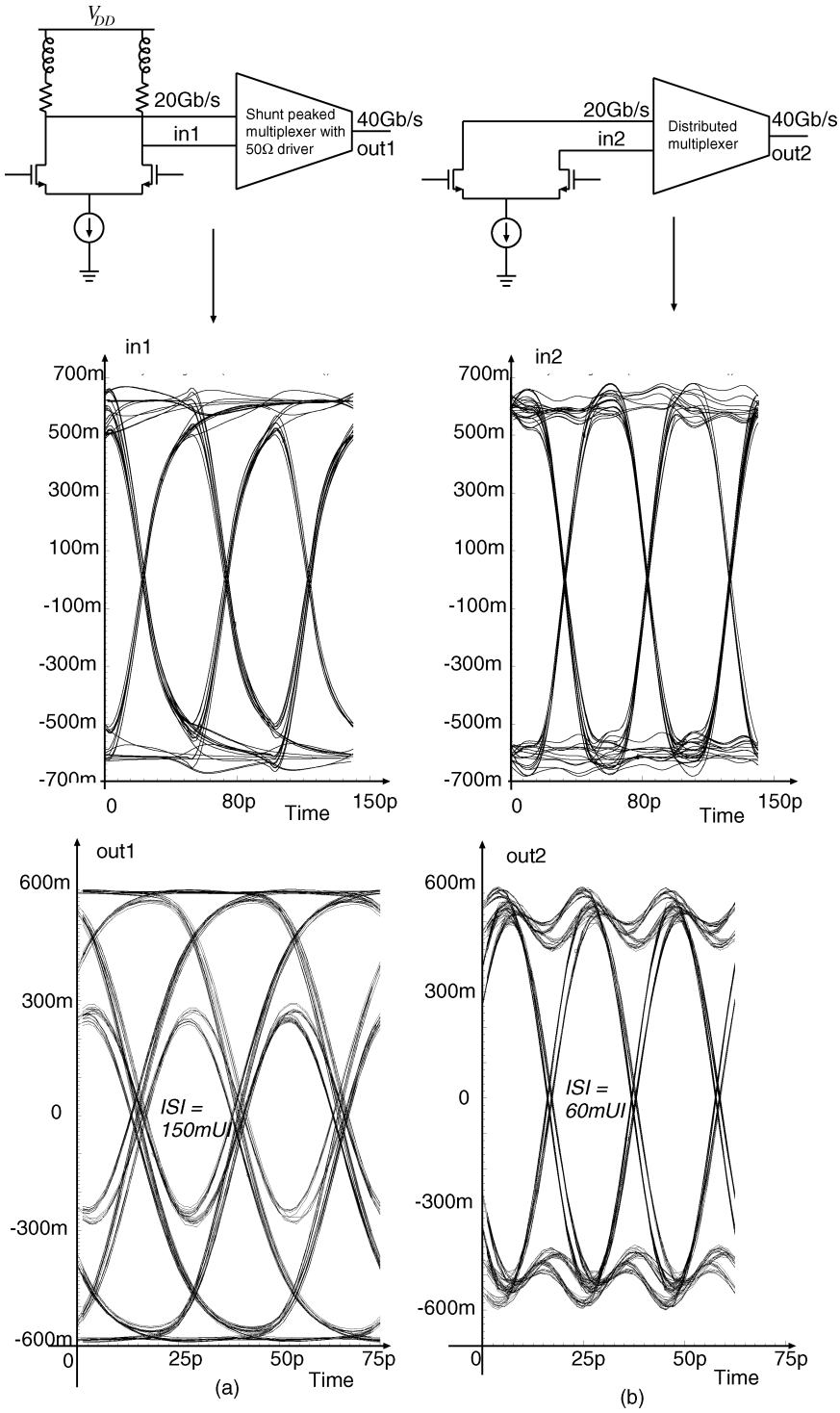

Fig. 3. Eye diagram for input and output of (a) conventional shunt peaked 2:1 select circuit; (b) proposed distributed 2:1 select circuit.

tween it and a conventional distributed amplifier. First, a distributed amplifier has a single input, while the Fig. 4 circuit has multiple inputs (clock and two data inputs). Second, a distributed amplifier is generally used as a small-signal amplifier, and thus a linear model suffices. On the other hand, the Fig. 4 circuit operates using large-signal voltage swings. As a result the device parameters (e.g., gate capacitances) are not constant over the entire voltage swing. These issues call for combined optimization of the small-signal (impedance matching) and large signal behavior (ISI) of the distributed select circuit. The total device size is usually determined by standard CML circuit design techniques described in [9] and is fixed to 120 μm/0.18 μm for this design. Thus, the goal of the optimization is to find the values of inductors L_g, L_c, and L_d, as well as the number of sections, which give the least output ISI when driving off-chip 50 Ω. A simple simulation-based approach was used. All the inductors were modeled using the scalable broadband inductor models described in [10]. This model accounts for the skin ef-

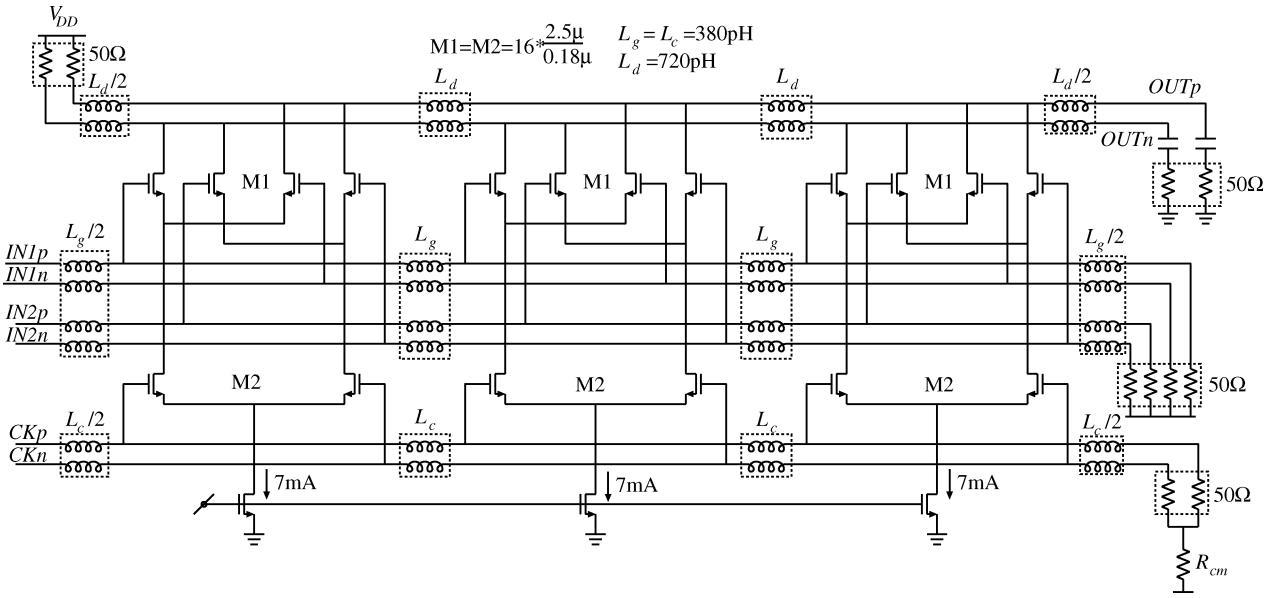

Fig. 4. Distributed select circuit schematic.

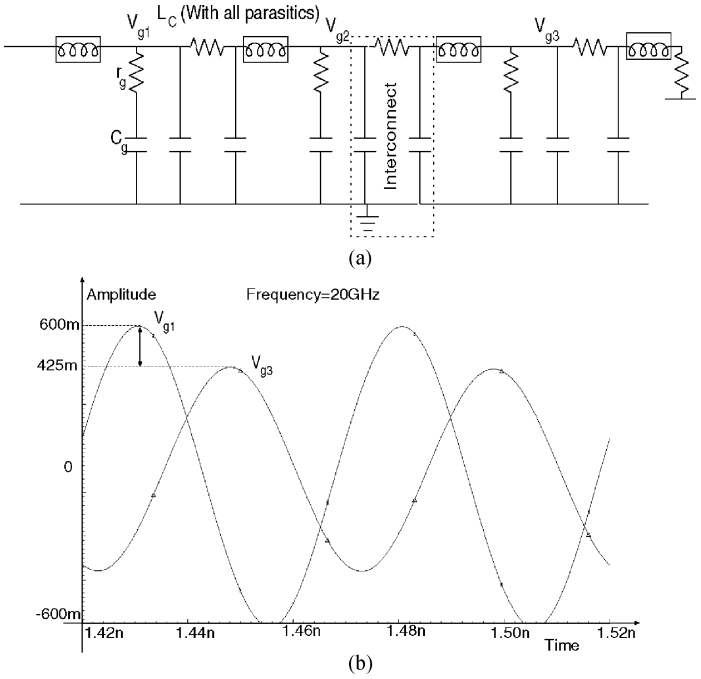

Fig. 5. (a) Equivalent gate line model. (b) Clock amplitude at the first and third stage of the clock line.

fect, substrate loss, proximity effect and other on-chip non-idealities and was included as part of the design kit provided by Jazz Semiconductor used for the chip. For physical implementation, the spiral inductor was realized using the aluminum top metal layer (2.8 μm thickness; 10.5 mΩ/square sheet resistance) directly over the substrate. The resistivity of the substrate was approximately 8 Ω-cm.

The design steps are described as follows.

1) If the transmission lines were lossless, the cutoff frequency of the distributed amplifier would increase without bound with the number of stages. However, when losses (due to series resistances in the inductors, transistor terminals, and interconnect) are considered, there is a maximum number of stages such that the loss of signal power does not dominate the performance. To find the optimum number of stages we first make a rough estimate of the transmission line inductances based on the desired characteristic impedance. Since the clock signal operates at the highest frequency, an equivalent model for the clock input line with all the parasitics was constructed as shown in Fig. 5(a). The waveforms at two points on the transmission line, V_{g1} and V_{g3}, are shown in Fig. 5(b). At the third stage the clock amplitude of V_{g3} has decreased by about 175 mV, which can barely switch the current fully in the following stage as required for correct CML operation. As a result increasing the number of stages further would not be beneficial, and thus three stages were used for this design. Further refinement of the inductor values is accomplished in the subsequent design steps.
2) We next find the values of L_g and L_c. A linear analysis suffices here. The criteria for finding these values is based on matching to the termination resistor of 50 Ω. Small-signal optimization is performed for these lines to find the inductor value which gives the best matching. The real and imaginary parts of the input impedance of the input data lines are plotted for different values of L_g in Fig. 6. From this simulation the values of these inductors were selected to be $L_g = L_c = 380$ pH. (The transistor sizing for both lines was identical.)
3) The last step is the determination of the output line inductance L_d. Since minimization of ISI is the most important specification for this circuit, transient analysis is used here. The value of L_d is chosen such that the output ISI is minimized when driving an external 50 Ω load for the values of L_g and L_c found in the previous step. The output ISI for five different values of L_d is shown in Fig. 7 where it can be observed that minimum ISI occurs for $L_d = 720$ pH. We can gain insight into why this gives the least ISI by

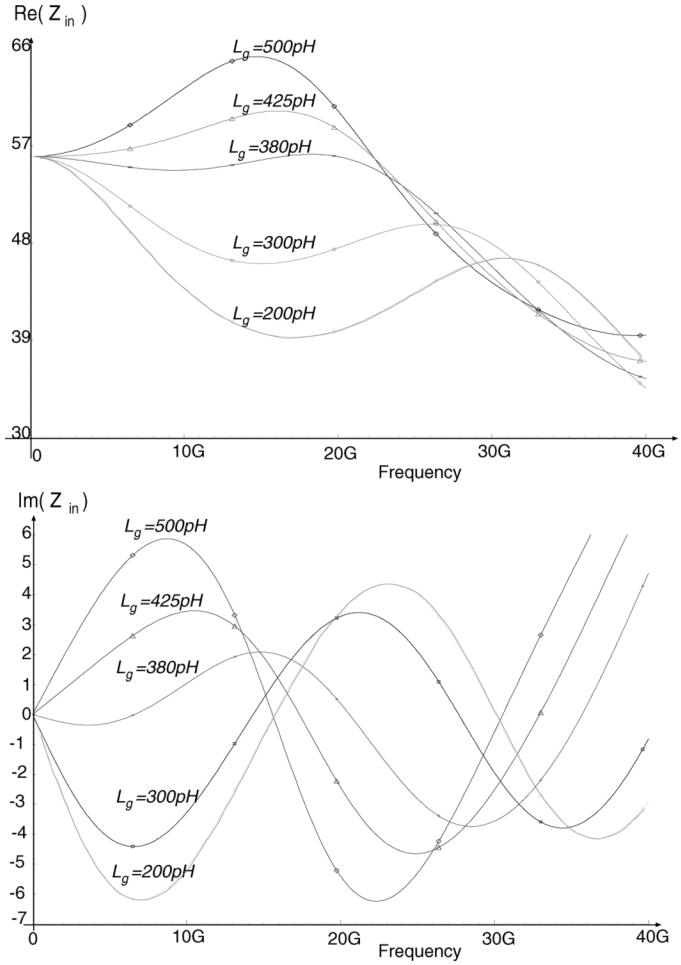

Fig. 6. Real and imaginary part of input impedance for different values of gate inductor.

considering the small-signal gain of an N-stage distributed amplifier, given by [15]:

$$A_v = \frac{g_m \left[\frac{L_d}{C_d}\frac{L_g}{C_g}\right]^{1/4} \sinh\left[\frac{N(\theta_d - \theta_g)}{2}\right]}{2\sqrt{\left(1 - \frac{\omega^2}{\omega_c^2}\right)} \sinh\left[\frac{(\theta_d - \theta_g)}{2}\right]} \cdot e^{-N(\theta_g + \theta_d)/2} \tag{1}$$

where g_m is the transconductance of each stage; ω_c is the cutoff frequency of the lines; θ_g (gate line propagation constant) $= \theta_{rg} + j\theta_{ig}$; θ_d (drain line propagation constant) $= \theta_{rd} + j\theta_{id}$. From (1), it can be seen that the gain exhibits a rapid increase as the cut-off frequency is approached, which is undesirable and leads to distortion of the pulse response. We can rewrite (1) assuming the losses are zero ($\theta_{rg} = 0$ and $\theta_{rd} = 0$):

$$A_v = \frac{g_m \left[\frac{L_d}{C_d}\frac{L_g}{C_g}\right]^{1/4} \sin\left[\frac{N(\theta_{id} - \theta_{ig})}{2}\right]}{2\sqrt{\left(1 - \frac{\omega^2}{\omega_c^2}\right)} \sin\left[\frac{(\theta_{id} - \theta_{ig})}{2}\right]} \cdot e^{-Nj(\theta_{ig} + \theta_{id})/2}. \tag{2}$$

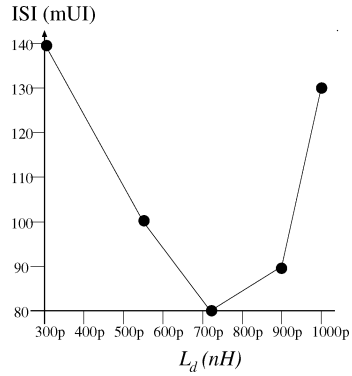

Fig. 7. Output ISI for 40 Gb/s 2^7–1 PRBS input data for different values of L_d.

In (2) if θ_{id} is made slightly higher than θ_{ig} such that the factor $\sin[N(\theta_{id} - \theta_{ig})/2]/\sin[(\theta_{id} - \theta_{ig})/2]$ becomes very small near ω_c, then the peaking in the gain can be reduced. Such a "staggered" distributed amplifier design with different propagation constants for the gate and drain line [14] provides a simple scheme to flatten the amplitude response. Hence, $L_g \neq L_d$ for this design.

A linear phase response is also desirable for maintaining low ISI since this impacts on the precise location of the zero crossings for varied data patterns. Although most of the effort in the design of the distributed multiplexer was focused on maximizing the gain-bandwidth product, a sufficiently linear phase was implied in simulations by minimizing the ISI as explained earlier. We can also give some insight into the phase linearity by considering the last term in (2), which gives the approximate phase shift of the distributed amplifier as $-N(\theta_{ig} + \theta_{id})/2$, which is simply the average of the phase shifts introduced by the gate line (θ_{ig}) and drain line (θ_{id}). In general for a transmission line, we would expect that the phase would deviate from linearity most severely near the cut-off frequency. As mentioned earlier, gate and drain propagation constants were made slightly different, implying that the cut-off frequencies of the gate and drain lines were also slightly different; thus we would expect that the phase characteristic of the gate line would be more linear than that of the drain line at the frequencies of interest. Hence, the average of the two phase characteristics would more linear than that of the drain line alone.

Another advantage of the staggered design comes from the fact that the data inputs to the distributed amplifier are not ideal—that is, these 17 Gb/s signals exhibit ISI because the driver circuits are overpeaked by about 16% to improve the amplitude of the isolated pulses, degraded significantly due to bandwidth limitations. The increased input ISI is compensated by the gate/drain line mismatch of the select circuit.

Lastly, an important design consideration is the instability due to the presence of gate-to-drain capacitance of transistors M_1 in the Fig. 4 circuit. The passive coupling between the gate and drain lines through the transistor C_{gd}'s and the active coupling through the transistor

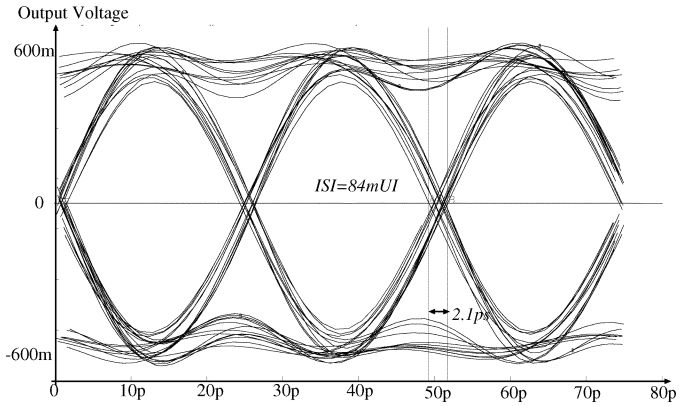

Fig. 8. 40 Gb/s serial output eye diagram.

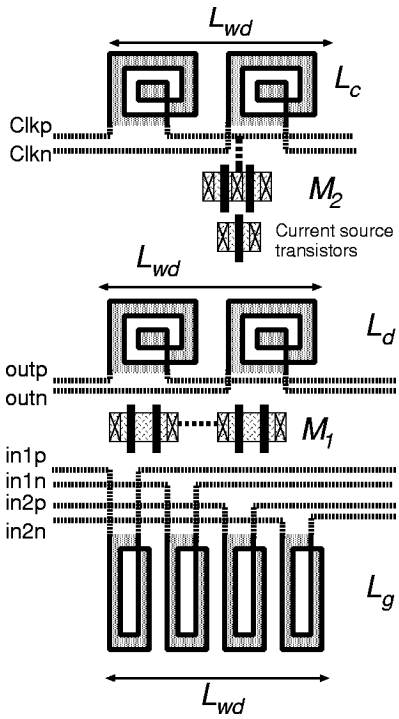

Fig. 9. Layout of a section of distributed select circuit.

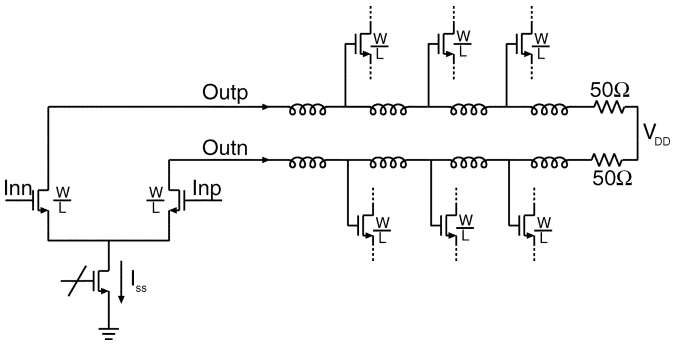

Fig. 10. Open-drain driver for distributed select circuit.

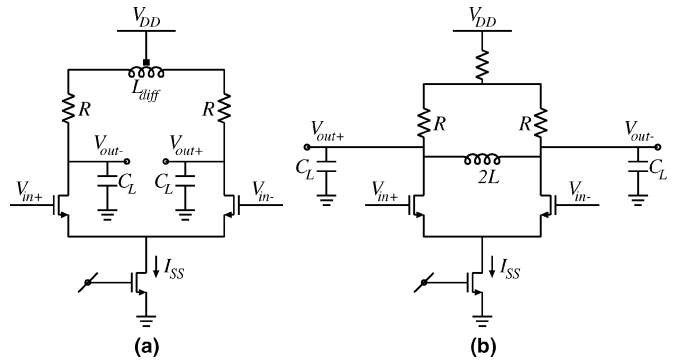

Fig. 11. (a) Shunt-peaked CML buffer circuit. (b) Resonant-peaked CML circuit.

transconductances lead to two different signals—one traveling faster than other—to propagate along the drain line [12]. For the slower propagating signal, the real part of θ_d may become negative at high frequencies depending on the values of C_{gd} and g_m, resulting in instability. The staggered design, as well as the presence of losses in the transmission lines, avoids this problem.

The optimized bandwidth of the select circuit was found to be 24 GHz with rise/fall times of 13 ps. The 40 Gb/s simulated output eye diagram (including post-layout R and C parasitics) is shown in Fig. 8.

4) There are two other major issues which must be considered for the distributed select circuit.
   a) *Layout:* The circuit performance is highly sensitive to the layout, particularly losses in the transmission lines. The floorplan for each section is shown in Fig. 9. To make a compact layout, rectangular inductors were used in the gate and drain lines in order to fit four gate line inductors in the same horizontal dimension as the two drain and clock line inductors. Also, the number of turns of each inductor was carefully selected for each case so that the two connecting terminals of each inductor were on the same side to ensure symmetrical interconnect length.
   b) *Driving the distributed select circuit:* An open-drain CML circuit as shown in Fig. 10 was used to drive the clock and data to the distributed select circuit. As compared to a conventional back-terminated driver, for the same voltage swing and device current density, this would require half the DC current and device sizes. This reduces the power consumption and improves the high-speed performance since the output loading conductance is halved. The only issue is the reflection from the source. This is not a problem for the data and clock input lines since the signals travel only in one direction—from the source to the load. The signal traveling to the right is absorbed by the matched on-chip termination. The situation is different for the output line, however. Since the input signals are applied at various locations along the output line, these signals will propagate in both directions. Thus, the output transmission line must be doubly terminated.

For circuits operating at 17 Gb/s (input retimer, drivers, etc.) shunt-peaking was used, as shown in Fig. 11(a). This improves the rise time of the circuit by 70% compared to

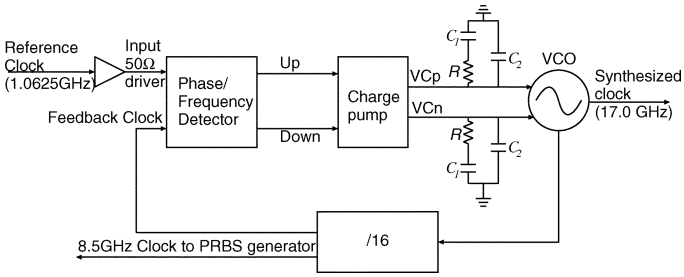

Fig. 12. CMU block diagram.

the unpeaked circuit and is described in [13]. An added benefit of shunt-peaking is that it is very robust in the presence of parasitic series resistance and shunt inductor capacitance; as a result inductors can be placed far away from the rest of the other CML circuit elements, which allows minimization of the parasitics on the signal lines. On the other hand, since the clock signal is made up of a single frequency, resonance can be used to increase gain with greatly reduced power dissipation as shown in Fig. 11(b). The reason for this is that the *LC* tank concentrates energy into a narrow range of frequency. An additional benefit of using tuned buffers is that the presence of the inductor provides a DC short between the two output nodes and thus reduces the DC offset at the output (which contributes to duty cycle distortion), thereby producing a clock with nearly 50% duty cycle. The buffers were designed to be low-Q in order to provide sufficient bandwidth to cover process variations. In this chip, four stages of cascaded tuned buffers were used to drive the 17 GHz clock to the select circuit and the input retimers.

B. Clock Multiplier Unit (CMU)

Fig. 12 shows the block diagram of the CMU. It uses a standard architecture consisting of a VCO, phase/frequency detector, charge pump, low-pass filter, and clock divider. The CMU generates an output clock at a frequency 16 times that of the low-frequency input reference clock. All the blocks of the CMU use differential signals to minimize the noise coupling from substrate or power supply.

As was mentioned before the measured VCO oscillation frequency was 17 GHz instead of the designed value of 20 GHz. An investigation into the reasons for this deviations revealed two inaccuracies: 1) varactor capacitances were 10% higher than predicted by the model, and 2) interconnect inductance between the tank inductor and the device, which was not accounted for in the simulations, added 12% to the effective inductor values. In spite of the lower frequency of oscillation, the basic principle of distributed circuit design for high bit-rate operation is still demonstrated.

A current-biased nMOS cross-coupled structure shown in Fig. 13(a) was used. Differential control was used to decrease the effect of common-mode noise (e.g., supply and substrate noise) coupled into the control voltage. The transistor sizes and bias current were selected by optimizing the phase noise and power consumption. The simulated VCO phase noise is -103 dBc/Hz at 1 MHz frequency offset and $K_{\mathrm{VCO}} = 1$ GHz/V. The 17 GHz VCO output is applied to a divider built by four stages of cascaded divide-by-two cells. The first two divider stages use the dynamic frequency divider shown in Fig. 13(b). This divider exhibits better high-frequency performance than the conventional D-flip-flop (DFF)-based frequency divider which was used in the other, lower frequency divider stages. Standard techniques were used in the loop filter design where the jitter bandwidth was set to 2.5 MHz.

III. PRBS Description

A $2^7 - 1$, two-channel 17 Gb/s PRBS generator was implemented for ease of testing and evaluation purposes. This circuit was implementd using high-speed n-p-n transistors. The block diagram of the two-channel 17 Gb/s PRBS generator is shown in Fig. 14(a). It consists of an 8.5 Gb/s core generator, a four-channel 8.5 Gb/s PRBS generator, a 4:2 multiplexer and an output mode selector. The core generates 8.5 Gb/s $2^7 - 1$ PRBS data. The generator polynomial employed is $x^7 + x + 1$ [16], and is realized as shown in Fig. 14(b). From this core PRBS, three additional channels are generated such that the delay between any two adjacent channels is 32 bits. These four signals are then applied to the 4:2 multiplexer. As discussed in [16], multiplexing these signals with appropriate delays creates two identical $2^7 - 1$ PRBS signals at 17 Gb/s. Two clock drivers are employed to drive the input 8.5 GHz clock to the PRBS core and 17 Gb/s multiplexer.

Following the 4:2 multiplexer, there is an output mode selector which enables four different output modes. The first mode is the normal mode which outputs two channels of shifted 17 Gb/s PRBS data ready for further multiplexing. The other three modes are used for the test purposes of the distributed multiplexer. In these three test modes, after the distributed multiplexing, the 34 Gb/s data would have a data pattern of "0101", "0011", or "1101".

IV. Measurement Results

To perform the measurements, the die was placed in a cavity on a custom-made PCB and bond wires were connected directly from the chip pads to the board as shown in Fig. 15. The cavity allows shorter bond wire lengths connecting from the chip pads to the board. SMP connectors served as ports for the high speed output data, CMU output clock and input reference clock. The measurement data presented here are taken in this configuration with a 1.0625 GHz reference clock. Fig. 16 shows the 34 Gb/s single-ended data eye diagram with $2^7 - 1$ PRBS data as measured with an Agilent 86100C digital communications analyzer (DCA) triggered by the CMU reference clock. The vertical eye opening is greater than 200 mV single-ended peak-to-peak. The ISI is measured to be less than 5 ps p-p and random jitter measured to be 940 fs; this is close to the analyzer's trigger jitter specified to be 800 fs. The measured ISI is more than twice the simulated value predicted by simulations. The reason for this discrepancy may be due to extra ISI caused by measurement set-up (bond-wires, cable, connectors, and probes) which was not taken into account during simulation. The measured VCO tuning range is 16.4GHz to 17.2GHz. The output spectrum of the 17 GHz clock when the VCO is locked to the input reference along with phase noise is shown in Fig. 17. The phase noise at 1

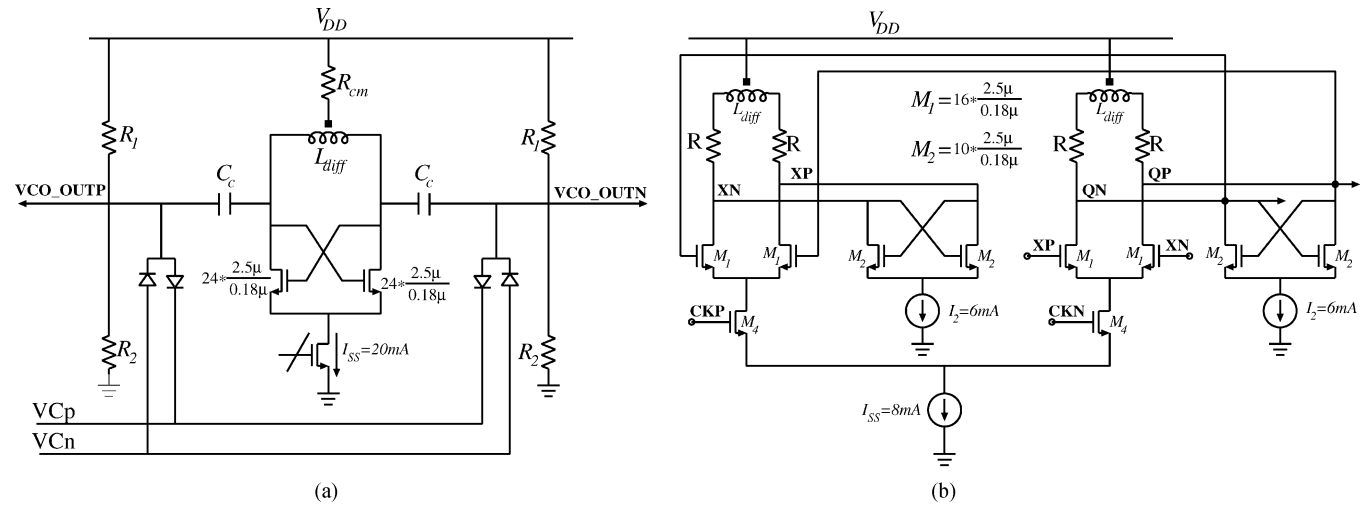

Fig. 13. (a) *LC* VCO schematic. (b) Dynamic frequency divider.

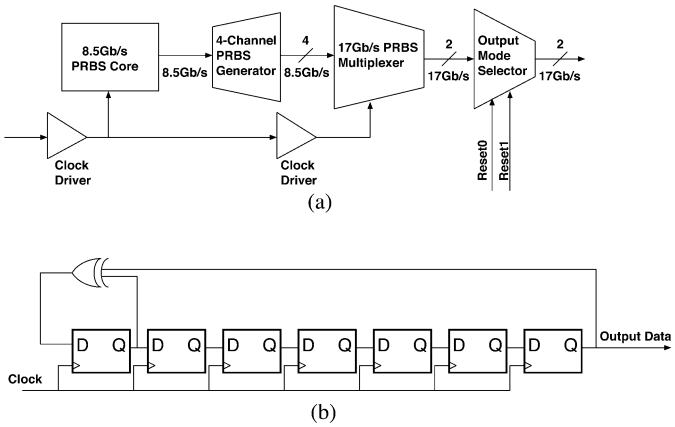

Fig. 14. (a) Block diagram of two-channel 17 Gb/s PRBS generator. (b) Schematic of core generator.

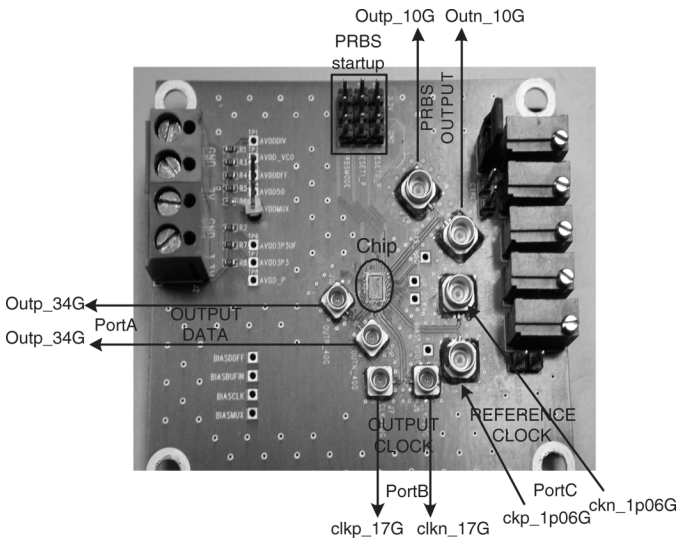

Fig. 15. Circuit board used for testing.

MHz offset is -97 dBc/Hz. The calculated rms clock jitter from 50 kHz to 80 MHz away from the fundamental of 17.0 GHz is about 7.9 mUI (230 fs). The jitter performance is summarized in Table I.

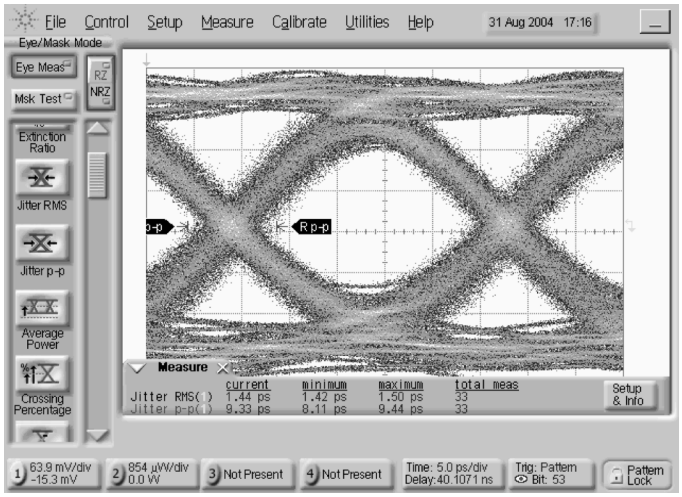

Fig. 16. Measured 34 Gb/s eye diagram.

An important performance measure for high-speed communication circuits is the determination of the bit-error rate (BER). Equipment which enables the measurement of BER for 40 Gb/s was not available for the reported measurements. As a result a direct BER measurement was not performed. However, correction functionality was verified by manually observing the entire PRBS pattern over a 381 bit cycle $(3 * (2^7 - 1))$ via the waveform capture feature of the DCA. This can be observed in Fig. 18 where the full PRBS pattern and transient waveform for a 34-bit window are shown. It can also be observed from Fig. 18 is that the pattern with consecutive output transitions (..1010..) gives rise to maximum ISI since they are not able to make the full logic transition in one unit interval. As a result this $2^7 - 1$ PRBS pattern is sufficient to capture the worst-case scenario and it can be conjectured that using a longer pattern (such as $(2^{31} - 1)$) would likely give similar results.

The total power dissipation of the chip is 1.3 W (of which 44 mW is due to the select circuit and 360 mW is due to the CMU) with a 2.0 V supply voltage for the CMOS circuitry (set higher than the nominal 1.8 V to account for IR drops in

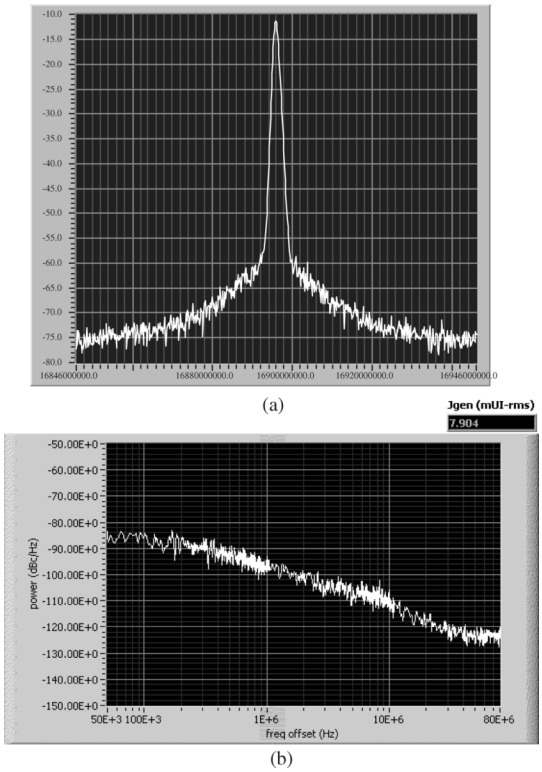

Fig. 17. (a) Output clock spectrum. (b) Phase noise plot.

TABLE I
MEASURED JITTER PERFORMANCE

ISI	5ps p-p
Duty Cycle Distortion	600fs p-p
Random jitter	940fs rms

TABLE II
MEASURED PERFORMANCE SUMMARY

Transmitted clock jitter	7.9mUI (80kHz – 50MHz)
Transmitted data swing	380mV single-ended p-p
Transmitted output clock swing	300mV single-ended p-p
Supply voltage	2.0V for MOS, 3.3 V for BJT
Power dissipation	PRBS (700mW), CMU (360mW), Input retimer and driver (200mW), 34Gb/s select circuit (44mW). Total=1.335W

the supply and ground connections) and 3.3 V for the BJT circuitry. The die photo is shown in Fig. 19. The total chip area is 1900 μm $\times$ 2800 μm; the final 2:1 select circuit occupies 25% of the die area. This is the penalty to pay for using distributed circuit techniques since it uses a large number of on-chip inductors to realize the artificial transmission lines.

V. CONCLUSION

A 34 Gb/s 2:1 MUX/CMU was successfully implemented in 0.18 μm CMOS. The measured performance results are summarized in Table II. Such high bit-rate operation was possible due to innovative distributed circuit design approach. To the authors' knowledge, this is the highest speed of a serializer reported to date in a similar technology.

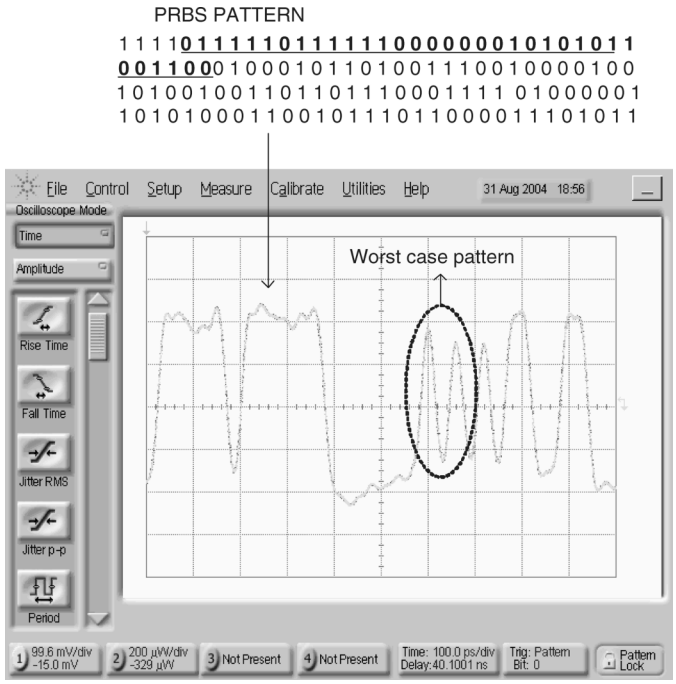

Fig. 18. Single-ended output transient response.

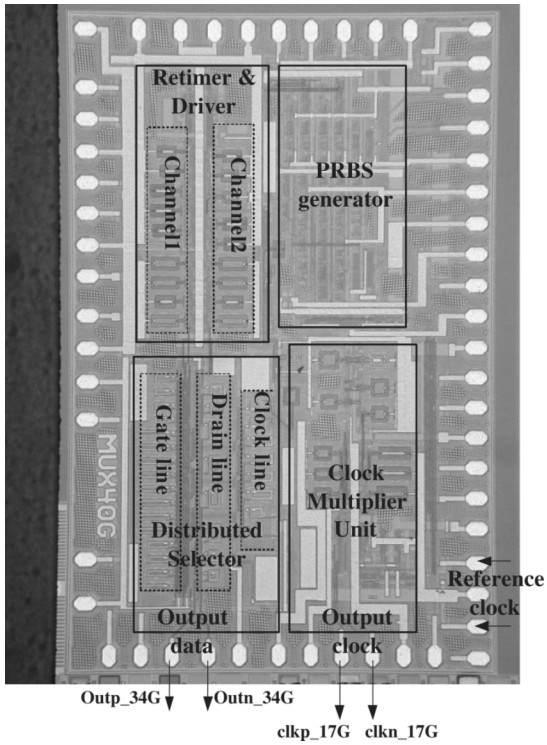

Fig. 19. Die photo.

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Ullas Singh received the B.E. degree in electronics and communication engineering from University of Roorkee, India, in 1996, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Irvine, in 2001 and 2005, respectively.

From 1996 to 1999, he worked for Temic Usha Ltd., India, and Motorola India Ltd., designing custom memories for micro-controllers. He is currently with Broadcom Corporation, Irvine, as a Staff Scientist designing high-speed data communication circuits.

Lijun Li received the B.S. degree in electronics engineering from Tsinghua University, Beijing, China, in 1998, and the M.S. degree in electrical engineering from Northeastern University, Boston, MA, in 2002. He is currently working toward the Ph.D. degree at the University of California, Irvine.

From 2000 to 2001, he was a Hardware Design Engineer at Lucent Technologies, Westford, MA, working on multi-service ATM WAN switch service cards. During the summer of 2004, he was an intern at Maxim Integrated Products, Inc., involved in the design of powerline transeivers. During the summer of 2005, he was an intern at Menara Networks, involved in the design of single-mode optical fiber transceivers.

Michael M. Green received the B.S. degree in electrical engineering from the University of California, Berkeley, in 1984, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, in 1988 and 1991, respectively.

Since 1997, he has been an Associate Professor in the Department of Electrical Engineering and Computer Science at the University of California, Irvine. From 1999 to 2001, he was an IC Designer with the Optical Transport Group at Broadcom Corporation (formerly Newport Communications). His current research interests include the design of analog mixed-signal integrated circuits for use in high-speed broadband communication networks and nonlinear circuit theory. He has published over 50 papers in technical journals and has three patents.

Dr. Green was the recipient of the Outstanding Master's Degree Candidate Award in 1989 and the Outstanding Ph.D. Degree Candidate Award in 1991, both from the UCLA School of Engineering and Applied Science. He is also the recipient of the Sigma Xi Prize for Outstanding Graduate Science Student at UCLA in 1991, the 1994 Guillemin–Cauer Award of the IEEE Circuits and Systems Society, the 1994 W. R. G. Baker Award of the IEEE, a 1994 National Young Investigator Award from the National Science Foundation, and the Award for New Technical Concepts in Electrical Engineering from IEEE Region 1. He has served as Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS, and IEEE TRANSACTIONS ON EDUCATION.