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Operational Energy Analysis of Plasmonic Imaging Lithography

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***Abstract*— Plasmonic imaging lithography (PIL) is a new direct-write lithograghy process based on disk drive technology. Using the benchmark of similarly scaled masked and maskless lithography processes, this paper evaluates the operational energy use of PIL, as a component of manufacturing and environmental impact analysis. This study serves two purposes: to inform the sustainable development of this emerging technology, and to identify PIL as most appropriate for prototyping or highly agile manufacturing of 11 or fewer wafers per design change.**

I. INTRODUCTION

Plasmonic imaging lithography (PIL) is a new photolithography exposure technique under development by the NSF Center for Scalable and Integrated Nano Manufacturing (SINAM). PIL allows researchers to surpass the diffraction limit of light using the special properties of surface waves or plasmons [1],[2]. The effervescent nature of plasmons requires the use of a near-field scanning system, in this case, one based on hard disk drive technology. PIL has the potential to pattern sub-wavelength features with the precision and throughput time suggested by established hard disk technology.

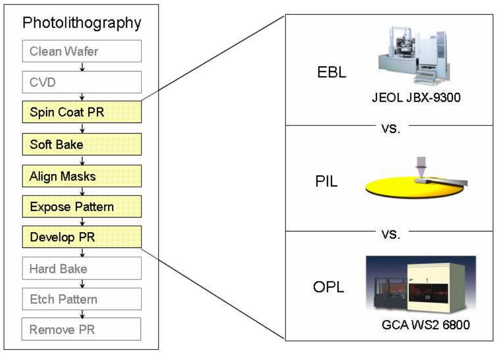

Fig. 1. Scope of analysis comparing electron beam lithography (EBL), plasmonic imaging lithography (PIL), and optical projection lithography (OPL). Generic lithography process flow based on [3].

As is characteristic of emerging technologies, there are many unanswered questions regarding the applicability, significance, and environmental impacts of PIL in a real world manufacturing setting. This paper aims to inform further development of PIL based on the manufacturing efficiency and environmental impact, as indicated in part by energy use, of PIL compared to that of two benchmark processes.

II. BENCHMARK PROCESSES

In this paper, we compare the direct electrical energy use of the PIL process flow to those of masked optical projection lithography (OPL) and maskless electron beam lithography (EBL). As shown in Figure 1, we evaluate process steps affected by PIL in addition to the exposure step itself. Spin coating is included, for example, because PIL uses a hard phase-change resist to facilitate reliable flight of the scanning head, and this resist must be sputtered, rather than spin-coated, onto the wafer.

PIL is still a developing process. Since comparison to production-scale processes would not yield useful information, similarly-scaled laboratory scale equipment is chosen as the benchmark for PIL. Specifically, we evaluate tools from the Microfabrication Laboratory at the University of California at Berkeley, as listed in Table 1. Reflecting the capabilities of PIL, we consider the exposure of one layer of a 4” wafer with 130nm linewidth, 30% density features for each of the lithography techniques.

Please note that while the scenarios are chosen to be similar, they are not equivalent processes. For example, processing times for EBL exposure vary with feature geometry and density. Meanwhile, the actual linewidth produced by PIL is higher than the 120nm spot size for all but a few feature orientations due to stitching.

III. METHODOLOGY

Rapidly emerging technologies present unique challenges for manufacturing and environmental analysis. In the case of PIL, design changes easily outpace assessment, and reliability and performance characteristics are indeterminate.

We address the developing nature of the PIL technology in three ways: *(A)* extrapolated performance characteristics based on practical milestones are assumed, *(B)* energy embodied in consumable materials and equipment is tentatively ignored, and *(C)* energy use is parameterized as a function of spot size and number of lenses used in parallel.

A. Extrapolated Performance Characteristics

Currently, PIL is capable of patterning portions of a wafer with 120nm lines and 200-300nm arbitrary features. In order for it to be applicable outside of basic research, it needs to be able to reliably pattern an entire wafer with high resolution arbitrary features. This analysis assumes these practical milestones are met.

B. Energy Use Modules

During the tenure of this analysis, the PIL resist material has changed numerous times. It is not possible to evaluate the embodied energy of each species in pace with these changes. Also, as with many developmental technologies, the quantities of materials used are not optimized as they would be in a production or established laboratory-scale environment.

Therefore, only operational energy use is evaluated in this paper, as it is static relative to the energy use associated with the quantity and species of materials consumed. As PIL development converges, it is our intention to add embodied energy modules for consumable materials and equipment use to the operational energy use module presented here.

C. Parameterized Energy Use

The energy use of PIL exposure is driven by track spacing. The narrower the track spacing, the more tracks on a wafer, and at a constant rotational velocity, the greater the processing time per wafer. Assuming constant power draw, the relationship between energy use of exposure and track spacing can be described logarithmically.

Each flying head or air bearing slider (ABS) is currently equipped with a single plasmonic lens, but subsequent milestones call for multiple lenses aligned across the width of the ABS. With a sophisticated system of optical modulators and lens, up to 100 lines of features could be patterned in parallel. To pattern continuous features, the lenses and tracks should be spaced to ensure an overlap of half a spot size.

The spot size currently produced by a plasmonic lens is 120nm, though the goal of SINAM is to reduce the spot size to under 10nm [1]. As spot size decreases, the number of tracks on a wafer increase accordingly. Thus, operational energy use is ultimately a function of spot size and number of lenses per air bearing slider.

Data Collection

Energy use data is collected from various sources. Electrical energy use is ideally measured directly [4] using power monitoring equipment with logging capabilities, such as those made by Summit Technology, Fluke, and Dent Instruments. However, it is often not possible to take functional equipment off-line for power measurement.

Instead, power supply requirements are collected from physical power supply inspection, and user and installation manuals. Power supply requirements are related to actual power use as follows:

$$P_{use} = S \times PF \times UF \times \sqrt{\phi} \tag{1}$$

where P_{use} is the actual power use in kilowatts (kW), S is the apparent power supply in kilovolt-amperes (kVa), PF is the power factor, UF is the ratio of power use to power supply, and ϕ is the phase of the power system (either single or 3-phase).

Power factor (PF) is the ratio of real power (P) to apparent power (S), where apparent power is the product of voltage and current [5]. Power factor is 0 for a purely reactive load and 1 for a purely resistive load. California utilities charge for power factors less than 0.85 [6], so we assume a power factor of 0.85. We also assume a usage factor (UF) of 0.67 [7] for all process tools.

Process time information is collected from expert machine operators, technicians and sales representatives based on average batch sizes and processing times. In the case of electron beam lithography exposure, expert operators reported an enormous range of processing times, ranging from 1 hr/cm^2 [8] to over 20,000 hr/cm^2 [9]. We instead calculated operational processing time as:

$$t = \frac{D \times A}{I} \tag{2}$$

where t is the time in seconds, D is the dose in μC/cm^2, A is the exposure area in cm^2, and I is the current in nA. As with all process tools, startup and idle times are included where appropriate.

More realistic models of energy use for production-scale products and processes can be found from [10], [11] and [12] However, their results are used for comparison only in order to preserve consistency in the scale and scope of this comparative analysis.

IV. RESULTS

Actual power use, processing time, and resulting energy use is shown in Table 1 for each process step of the three lithography techniques. For a static design, plasmonic imaging lithography consumes 56 kWh per wafer, compared to 0.95 kWh for optical projection lithography and 1.4 MWh for electron beam lithography, as shown in Figure 2.

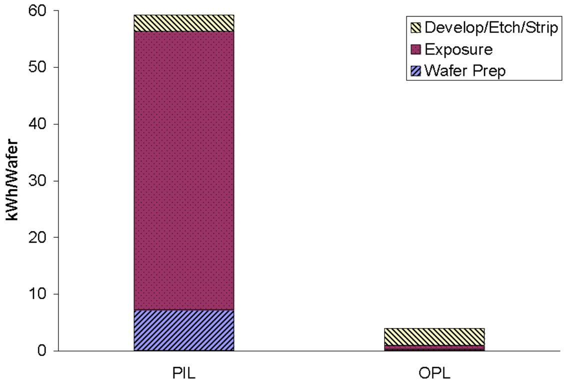

Fig. 2. Operational energy use per 4” wafer for a static design, for plasmonic imaging lithography (PIL) and optical projection lithography (OPL). Electron beam lithography (EBL) is left off to preserve resolution.

However, this calculation does not reflect processing energy used to fabricate the air bearing slider used in PIL and the reticle mask used in OPL. When we include 0.082 kWh for an ABS and 620 kWh for a mask, as we would for a one-off design, the operational energy use of the lithography techniques rank very differently, as shown in Figure 3.

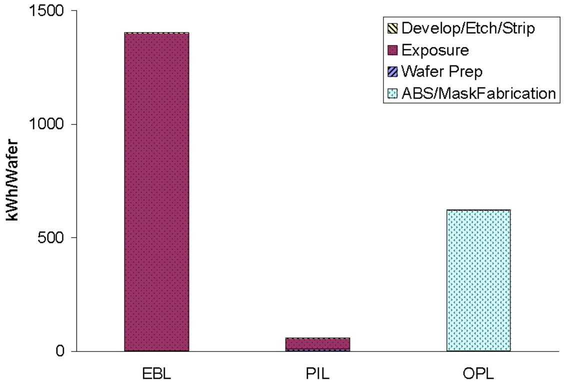

Fig. 3. Operational energy use per 4” wafer for a one-off design, including the processing energy of an air bearing slider (ABS) for plasmonic imaging lithography (PIL) or a mask for optical projection lithography (OPL).

A realistic manufacturing scenario lies somewhere between these bounding cases. While an ABS is assumed to have a functional life of one wafer pass, a photolithography mask can be used well past the desired life of a particular design. Figure 4 shows energy use as a function of design agility, which we associate with wafers per design change. The crossover point at which OPL becomes more energy efficient than PIL is 11, 39, and 85 wafers for 1, 10, and 100 plasmonic lenses per air bearing slider, respectively. This suggests that PIL is most appropriate for prototyping or highly flexible manufacturing.

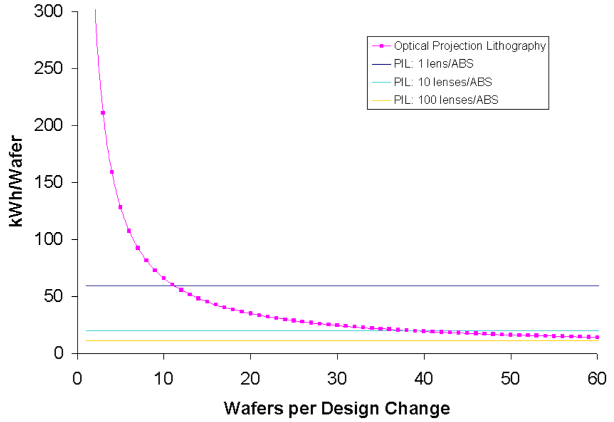

Fig. 4. Energy use as a function of design agility.

These results are also useful for informing the design of the PIL process for energy efficiency. Design for environment is especially valuable to consider at this early stage in the development process, as the design space is still relatively unconstrained.

The range in which PIL is the best option in terms of operational energy use can be expanded most significantly by addressing the biggest sources of energy use in the PIL process flow. The ion laser used in PIL wafer exposure is a good example, consuming 78% of energy used in wafer processing. It draws 10kW of electrical power, and though it is capable of much higher powered laser beams, it is only used to produce a 260mW laser beam, representing a loss of four orders of magnitude.

Another change that could expand the niche of PIL considerably would be to increase the number of lenses on each air bearing slider. Assuming the use of the same laser, the number of lenses on an ABS is inversely proportional to wafer exposure time and resulting energy use (Figure 4).

Outside of wafer exposure, the greatest contributor to operational energy use for PIL is sputtering of the resist. To protect the phase-change resist, a metal adhesion layer and a diamond-like coating are also applied to each wafer, requiring two separate sputtering processes. The analysis presented here adds to the practical argument for a liquid photoresist.

V. DISCUSSION

Energy use is ideally measured directly rather than calculated based on power supply. Using power supply to find energy use introduces uncertainty into these values of energy use. However, in this analysis, we are primarily interested in the relative energy use of the lithography techniques and the relative energy use of the components of PIL. If the methodology is applied consistently, power supply information can be useful for comparative energy analysis.

To arrive at the power use values shown in Table 1, we evaluated the power use of a number of comparable tools for the sputter, spin-coat, EBL exposure, OPL exposure, and develop/etch/strip processes. A wide spread of values were found for the sputter, spin-coat, and OPL exposure processes, while the power use of two EBL tools were relatively close: 7.1 kW for the JEOL JBX 9300 and 7.7 kW for the LEICA VB6-HR.

Yet, the uncertainty in power use values is small relative to the uncertainty in processing time values. Specifically, start up and idle times vary dramatically with any number of factors including initial state of the machine, age and reliability of the machine, operator experience, and quality or species of material inputs. As with power use, we collected a range of possible processing times to arrive at the results in table 1.

There are many discrepancies in power and throughput time between the results reported here and those reported by [10]. This can easily be attributed to differences in production scale, wafer size, and analysis scope. Yet, energy use per area per layer is within a 50% margin of error for the spin-coat and OPL exposure processes.

However, this was not the case for the sputter and develop/etch/strip processes. The energy use per area for these processes are more than twice that reported by [10]. This difference may be due to improved production-scale efficiencies or overly generous estimates of set up or processing times. Nevertheless, the impact of these discrepancies on the energy use rankings of the three lithography techniques is minor.

	Unit	Process (Tool)	kW	Hr/Unit	kWh/Unit	Note	Reference
EBL	Wafer	HMDS Priming (YES LP-III-M5)	1.4	0.0058	0.0083		[14]
		Spin Coat (SVG 8626 PC)	6.1	0.033	0.20		[14]
		EBL (JEOL JBX 9300)	7.1	200	1400		[15],[16]
		Develop, Etch, Strip (Chemcut 547)	120	0.025	3.0		[17],[18]
PIL	Wafer	Sputter (Edwards Auto 306)	12	0.58	7.1	a	[14],[18]
		Ion Laser (Spectra-Physics 2020-05RS)	10	4.5	46		[19]
		Optical Modulator (Conoptics 25D)	0.25	4.5	1.1	b	[20]
		Nanostage (Physik Instrumente P-611.3SF)	0.042	4.5	0.19	b	[21]
		Acoustic Emissions Sensor (SRS 560)	0.0060	4.5	0.027	b	[22]
		Spindle (Seagull Solutions 02424)	0.41	4.5	1.8		[23]
		Develop, Etch, Strip (Chemcut 547)	120	0.025	3.0		[17],[18]
	ABS	HMDS Priming (YES LP-III-M5)	1.4	0.000015	0.000021	a	[14]
		Spin Coat (SVG 8626 PC)	6.1	0.000083	0.00051	a	[14]
		Stepper (GCA WS2 6800)	18	0.00010	0.0018	a	[14],[18],[24]
		Reactive Ion Etching (LAM3 690B)	24	0.013	0.031	a	[14],[18]
		Sputter (Edwards Auto 306)	12	0.00083	0.010		[14],[18]
		Ion Beam Lithography (FEI Strata 400)	6.8	0.00058	0.0040		[18],[25],[26]
		Wafer Dicing (Disco)	7.1	0.0050	0.035		[14],[24]
OPL	Wafer	HMDS Priming (YES LP-III-M5)	1.4	0.0058	0.0083		[14]
		Spin Coat (SVG 8626 PC)	6.1	0.033	0.20		[14]
		Stepper (GCA WS2 6800)	18	0.040	0.73		[14],[18],[24]
		Develop, Etch, Strip (Chemcut 547)	120	0.025	3.0		[17],[18]
	Mask	Sputter (Edwards Auto 306)	12	1.2	14		[14],[18]
		HMDS Priming (YES LP-III-M5)	1.4	0.0058	0.0083		[14]
		Spin Coat (SVG 8626 PC)	6.1	0.066	0.41		[14]
		EBL (JEOL JBX 9300)	7.1	80	600		[15],[16]
		Develop, Etch, Strip (Chemcut 547)	120	0.050	6		[17],[18]

Note:
a = Process is performed twice
b = End use power, no usage or power factor considered

TABLE I

SPECIFIC PROCESS TOOL DATA

VI. CONTINUING WORK

Materials inventory is currently being compiled for relatively static inputs to PIL, such as the sapphire air bearing slider substrate. However, the inventory does not yet include the resist material, as it is an active point of research.

The materials inventory will be used to enrich the energy use analysis presented here, and to expand the environmental assessment of PIL. Embodied energy of materials, scarcity of raw materials, and toxicity of emissions will be important to consider, as exotic materials and nanoparticles are under exploration for use in PIL.

Another practical concern we are working to address is the precision of features produced with PIL. There is an inherent stitching problem in creating cartesian coordinate features in a polar coordinate system. On top of the gaussian line edge roughness (LER) due to processing error observed in all lithographic products, we expect to observe a systematic LER due to the nature of PIL stitching.

It is important to minimize both sources of LER, as it can cause current leakage and device failure [13]. While processing LER is outside the scope of our research, we are developing a Matlab tool to model systematic LER as a function of spot size, track spacing, and feature dimensions, orientation, and location along the radius of the wafer. These relationships, in turn, will characterize the effect of LER, or more generally, of precision, on energy use.

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