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Advanced Electrical Characterization of Semiconductor Nanowires

by

Devesh Raj Khanal

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Materials Science and Engineering

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Junqiao Wu, Chair
Professor Eugene Haller
Professor Sayeef Salahuddin

Fall 2010

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Devesh Raj Khanal

Abstract

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Doctor of Philosophy in Engineering - Materials Science and Engineering

University of California, Berkeley

Professor Junqiao Wu, Chair

Over the past decade, semiconductor nanowires have emerged as a potential candidate for the continued miniaturization of microelectronics. However, there exist major problems in characterizing their basic electronic properties, which result from the difficulty of using conventional semiconductor characterization techniques such as the Hall effect on individual nanowires due to their small size and aspect ratio. As a result, alternative methods of quantifying their basic semiconducting properties, including carrier concentration and mobility are required. To date, the most common alternative to the Hall effect experiment is the field-effect transistor (FET) measurement, where the nanowire is assembled into a field-effect device and gated current-voltage curves are recorded.

Extracting information about the carrier concentration and mobility from FET measurements, however, requires a precise knowledge of the electrostatics of the nanowire, which are usually neglected in favor of analytical approximations. In this work, a series of experiments and theoretical studies are presented, which are shown to both improve the accuracy of extracted values of carrier concentration and mobility as well as allow for the quantification of additional electronic properties such as the Fermi-level pinning position and the relative magnitudes of individual carrier scattering mechanisms.

In chapter 2, finite element modeling of the electrostatics of nanowire-gate devices is used to evaluate the validity of assumptions used in common analytical capacitance formulas. It is shown that assumptions about the nanowire-gate geometry, the semiconducting nature of the wire, and length of the nanowire device lead to significant misestimations of the nanowire-gate capacitance, which can result in equally significant misestimations of carrier mobility and concentration.

A method for quantitatively extracting Fermi level pinning information, using a combination of FET measurements and finite element electrostatics modeling, is presented in Chapter 3 using InN nanowires as an example. The results indicate that the Fermi-level at the non-polar sidewalls of the nanowires is pinned to between 0.6 - 0.8 eV below the conduction band minimum, in good agreement with InN thin films. In Chapter 4, universal mobility analysis is used to determine the relative magnitude of individual scattering mechanisms on carrier mobility using only FET measurements and thorough calculations of the

nanowire-gate electrostatics. The techniques of extracting Fermi level pinning position and free carrier scattering mechanisms in Chapter 3 and 4 can be applied to *single* nanowires, which has yet to be reported elsewhere in the literature. Finally, Chapter 5 includes a theoretical study of the doping limitations of ultra-small diameter nanowires where quantum confinement appreciably perturbs the density of states.

Professor Junqiao Wu
Dissertation Committee Chair

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This dissertation represents a short summary of the last five years of my work in graduate school. In that time, I have received the guidance and support of so many people. Listing their names here in a short few paragraph surely would not suffice as adequate thanks, however, I will do so anyways.

The research summarized herein was performed with the close guidance of Professor Junqiao Wu. We started years ago with no lab space, our own laptops, and some ideas. Looking back at my scientific understanding back then, I can now fully appreciate his instruction and guidance that helped lead me to this point. I am deeply grateful for all he has taught me. I am also thankful to several other professors and scientists for instruction, guidance, and support. I thank Professors Eugene Haller, Oscar Dubon, Tom Devine, Peidong Yang, Daryl Chrzan, and Sayeef Salahuddin for providing scientific guidance in various fashions throughout the years. Early on, Frank Ogletree and Ed Wong helped tremendously with experiments at the Molecular Foundry at Lawrence Berkeley National Laboratory. In addition, scientists and staff of the Materials Science Division at LBNL have been either close collaborators on several projects or provided invaluable assistance to experiments and interpretation, including Wladek Walukiewicz, Zuzanna Liliental-Weber, Jeff Beaman, and Lothar Reichertz. Finally, none of the InN experiments would have been possible without collaboration with Enrique Calleja's group at Cuidad Universitaria in Madrid.

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Lastly, family is, of course, so special that I have decided to allot them their own paragraph in the Acknowledgements section. My family, especially my parents, are responsible not just for love, support, and guidance during my stay at graduate school, but also the 22 years of arduous child-rearing required beforehand without which I would not have been fit to undertake such a journey.

Chapter 1

Introduction to Semiconductor Nanowires

1.1 Properties and Applications

Wagner and Ellis first reported on the synthesis of single crystal whiskers of Si via the vapor-liquid-solid (VLS) mechanism in 1964 [1]. For decades after, however, the electronics industry focused almost exclusively on bulk and thin film semiconductors, and useful device structures (most notably the field-effect transistor) were consistently scaled down to smaller and smaller sizes to fit more devices in a given chip area, leaving little incentive for further exploration of these micro and nanoscale whiskers. But in the past decade, this scaling trend, famously described by Moore's Law, has shown signs of slowing down, due in large part to limitations in the top-down fabrication of sub 50 nm features [2].

These limitations have fueled a renewed interest in bottom up grown nanostructures, most notably inorganic semiconductor nanowires, where the most critical dimension, nanowire diameter, can be controlled during growth with single nanometer precision [2, 3]. In addition, control of chemical composition and material structure during growth allows device structures such as p-n junctions and heterojunctions to be incorporated into the material without additional post-growth processing [2, 4], as Wagner and Ellis predicted would be possible in their original paper [1]. For example, axial [5] and radial [6] p-n junctions can be grown into nanowires (Fig. 1.1), allowing not only very precise control of the overall material dimensions (i.e., wire diameter) but also precise control of device dimensions. Over time, "nanowire" has come to mean any semiconductor crystal (usually single crystal) with a diameter generally smaller than 100 nm and length at least an order of magnitude greater. Although

diameter and radius are often used to describe their size, nanowires have been grown with many different faceting arrangements [7], via a variety of different growth techniques [8].

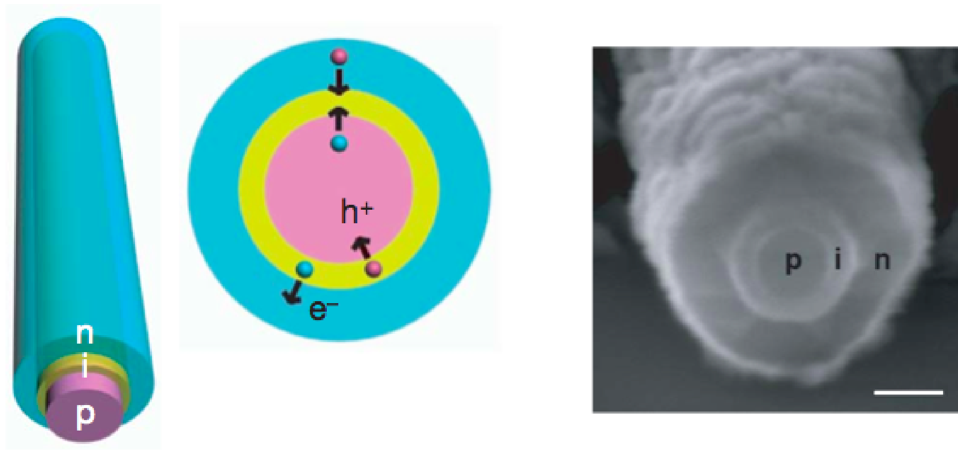

Figure 1.1. Schematic and scanning electron micrograph of a Si nanowire with a radial p-n junction from Tian *et al.* [6]. The scale bar is 100 nm.

The small size and high surface area to volume ratio of nanowires can be exploited for many applications. Semiconductor nanowire sensors, for example, have shown great sensitivity as chemical and biomolecular sensors, sensing everything from pH [9], to carbon monoxide gas [10], and even cancer markers using the appropriate surface receptors [11]. The size and shape of nanowires also gives them advantages in photovoltaic applications. Vertical arrays of Si nanowires at the surface of a solar cell have been shown to have superior light trapping capabilities compared to conventional techniques and can be fabricated with excellent periodicity on the wafer scale [12] (Fig. 1.2). In addition, if the p-n junction is radial, photo-generated minority carriers only have to diffuse a very small distance (a few nanometers) to get collected. This improves collection efficiency and can potentially enable the use of "dirty" semiconductor material (e.g. metallurgical grade Si), which could reduce solar cell cost [13]. Lastly, battery electrodes are a quintessential application where high-surface area materials are tremendously beneficial, and Si nanowire arrays have shown promising results for the improvement of Li-ion battery specific charge storage capacity [14].

What all of these applications have in common is that the nanowire must be a *semiconductor*. That is, the conductivity of the wire must be adjustable in some manner, whether by doping, exposure to light, adsorption of chemical species, or by application of an electric field. This property of semiconductors, adjustable or controllable conductivity, is essential for their use in electronic applications and nanowires are no exception. However, what makes semiconductor nanowires particularly unique are the new physical phenomena that are observable or dominant at nanometer length scales, including quantum confinement of free carriers [15], dielectric confinement [16], and short-length electrostatic effects [17]. These size-dependent properties can be exploited for new device applications, but they also create complexity in characterizing semiconductor nanowires. In addition, surface-based phenom-

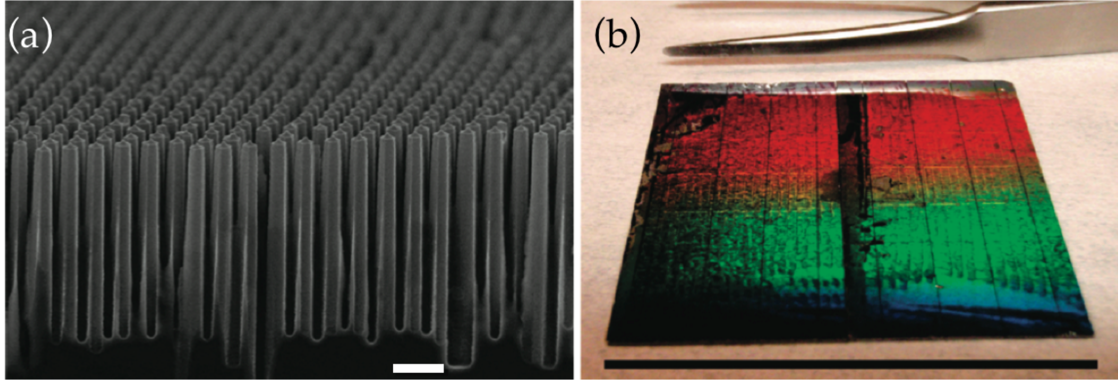

Figure 1.2. (a) SEM image of the surface of a silicon nanowire radial p-n junction array solar cell. Scale bar is 1 μm. (b) Tilted photograph of Si nanowire solar cell arrays with a color gradient that is indicative of excellent periodicity on the wafer scale. Both (a) and (b) from Garnett et al. (Ref. [12]).

ena (e.g., surface Fermi level pinning and surface scattering) have a much greater impact in nanoscale materials, where the surface area to volume ratio is much higher than bulk or thin film semiconductors. This makes careful evaluation of the quantitative impacts of surface effects imperative as well.

When designing and engineering new semiconductor materials, we must first be able to *characterize* their electrical behavior, for what use is trying to adjust or control charge carriers concentrations if we have no method of measuring them in the first place? With this in mind, when exploring any new semiconductor material such as nanowires, one must ask if existing characterization methods can still be used. If not, research must be done towards finding and verifying alternative methods of characterization. The size, shape and unique properties of nanowires discussed above do, in fact, make thorough characterization of their basic semiconducting properties non-trivial, and thus alternate and improved methods must be explored. That is the subject of this dissertation.

1.2 Conventional Characterization Techniques for Carrier Concentration and Mobility

Two of the most important material properties of semiconductors are the free carrier mobility and concentration, as they determine the conductivity in a semiconductor and can be engineered as discussed above. Because conductivity (σ) involves the product of carrier concentration (n)[1] and carrier mobility (μ), a second experiment, beyond a simple conductivity measurement, is needed to measure one of the two parameters independently.

[1] Though n-type semiconductors will be used as an example throughout this dissertation, p-type is analogous.

In bulk and thin-film semiconductors, this second measurement is the Hall effect. Making reliable electrical contact to measure a Hall voltage induced on the sidewalls of nanowires with diameters on the order of $10-60$ nm, however, is extremely difficult with current lithography technology and, at the time of this writing, has yet to be reported on bottom-up grown nanowires. Instead, in nanowires, n and μ are most often quantified via transconductance measurements, wherein a nanowire is placed in a field-effect transistor (FET) setup (Fig. 2.1), a gate voltage is used to modulate the current in the nanowire and μ is extracted in the following way.

Using the Drude model of conductivity, the current through a wire of area A and length L is:

$$I = \frac{AV_{sd}}{L} ne\mu \tag{1.1}$$

where e is the charge of an electron, and V_{sd} is the source-drain voltage. A gate voltage (V_G) is used to modulate n in the nanowire channel via the capacitance between the gate electrode and nanowire:

$$ne = \frac{C(V_G - V_t)}{AL} \tag{1.2}$$

where V_t is the threshold voltage, defined as the gate voltage that fully depletes the wire of free carriers ($n = 0$). After combining Eqs. 1.1 and 1.2, the mobility can be defined in one of two ways: the field-effect mobility μ_{FE} or the effective mobility μ_{eff}. The field-effect mobility is derived from the slope of the current versus gate voltage curve, called the transconductance ($g_m = \frac{\partial I}{\partial V_G}$):

$$\mu_{FE} = \frac{g_m L^2}{CV_{sd}} \tag{1.3}$$

The effective mobility is simply:

$$\mu_{eff} = \frac{IL^2}{C(V_G - V_t)V_{sd}} \tag{1.4}$$

The field-effect mobility is more commonly used for semiconductor nanowire studies as it does not require knowledge of V_t, which is often difficult to define and is a common source of error in μ_{eff} (Fig. 1.3). Figure 1.3 shows schematics of typical $I(V_G)$ behavior as well as the resultant μ_{FE} and μ_{eff} as functions of gate voltage. Since an experimental $I(V_G)$ curve is never linear for all V_G, μ_{FE} is most often reported using the peak transconductance (steepest slope). This is referred to as the peak field-effect mobility. In Fig. 1.3 (b), we see that except for at the peak transconductance, μ_{FE}, by definition, will always be lower than μ_{eff}, and when the transconductance approaches zero (or even becomes negative) at very large gate voltages, μ_{FE} will go to zero or become negative, which is obviously inconsistent with the fact that at such gate voltages a (positive) current is still flowing. Thus, μ_{FE} is not a good descriptor of mobility beyond the peak transconductance, and consequently μ_{eff} has been most commonly used over the years for device modeling of Si-based FETs to accurately predict current and switching speeds [18].

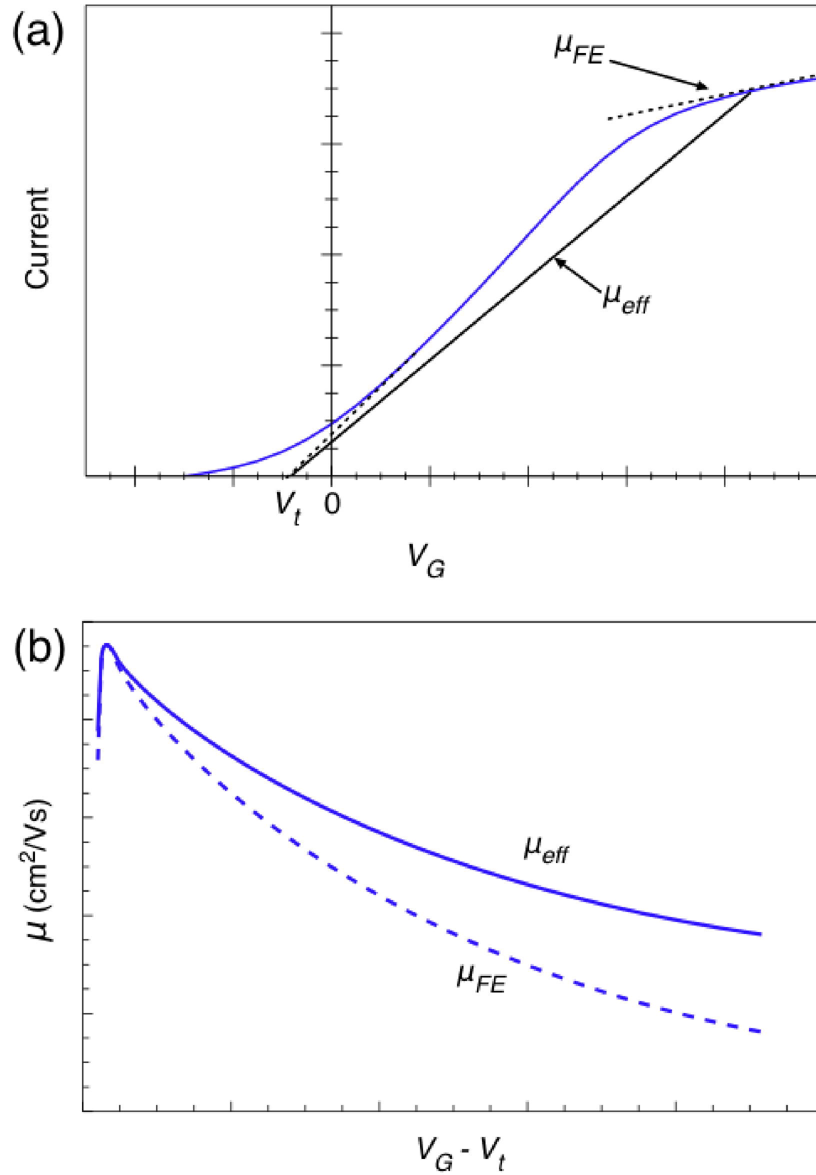

Figure 1.3. (a) Schematic of an $I(V_G)$ curve for an n-type nanowire showing μ_{FE}, μ_{eff}, and V_t. Note that the method of extrapolating the $I(V_G)$ data to the x-axis as shown is one approximate method of estimating V_t, but does not generally result in the precise V_t that yields $n = 0$ in Eq. 1.2. (b) Effective and field-effect mobilities as a function of $V_g - V_t$ that correspond to (a). Both (a) and (b) are adapted from Ref. [18].

1.3 Problems with the Conventional Technique

The above method for estimating carrier concentration and mobility in nanowires, though widely used, has limitations. First, it requires measurement or estimation of C, the gate-nanowire capacitance. The gate-nanowire capacitance of a single nanowire device, however, is usually on the order of femtofarads, which makes it difficult to distinguish from various sources of background capacitance, most notably, the electrical leads and the gate electrode. For this reason, there are very few reports of single nanowire capacitance measurements [19, 20] relative to the vast number of reports citing nanowire mobilities and carrier concentrations obtained via the transconductance technique. Consequently, C is most often estimated using an analytical formula for the capacitance of two metallic bodies in the relevant geometry (e.g. cylinder-on-plane capacitance for the backgate geometry or coaxial cylinders for surround-gate or top-gate geometries). However, as will be discussed in Chapter 2, finite-element-modeling of the electrostatics in nanowire field-effect transistors (NWFETs) has revealed that these analytical formulas can yield significant errors in estimates of C, which result in proportional errors in estimates of μ and n.

Second, the conventional transconductance method yields single values for n and μ in nanowires. That is, a given nanowire is ascribed *one* carrier concentration and *one* mobility. Physically, this corresponds to an average n and an average μ for the wire. Although this can be useful and sufficient in many situations, it prevents a thorough understanding of electronic transport in semiconductor nanowires because n is likely a function of radial position due to surface state induced band bending and μ is likely a function of the electron distribution due to differences between surface and core mobilities. Thus, both are functions of band bending in the wire.

Band bending occurs naturally in many semiconductors with a high density of surface states, which trap charge, pin the Fermi level at a specific energy with respect to the band edges and create a built-in electric field (and thus a non-uniform carrier distribution). This electric field penetrates a distance on the order of tens of nanometers, comparable to the diameter of nanowires. Hence, band bending can cause the free carrier distribution in a single nanowire to be non-uniform across its entire diameter. This can have an enormous effect on its transport characteristics.

As for mobility, the surfaces of semiconductors (including interfaces with their native oxides) will often scatter carriers and result in a difference between carrier mobility in the core and the near surface region of the semiconductor. Consequently, the average μ of the nanowire must be dependent on the distribution of carriers, and thus on the band bending as well. Furthermore, as mentioned earlier, band bending not only differs between different semiconductors, but can differ for a given semiconductor *during* device operation. For example, a nanowire sensor may have a radically different band bending situation before and after chemical species are adsorbed onto the surface. Thus, neglecting non-uniformities in n and μ and their interrelationship leaves us with an incomplete understanding of electrical conduction in semiconductor nanowires.

The limitations to the conventional transconductance technique for measuring n and μ beg for more rigorous methods for determining carrier concentration and mobility in semi-

conductor nanowires. The following chapters highlight different steps towards this goal. In chapter 2, work on modeling the electrostatics of semiconductor nanowires and nanowire FET devices is presented. Specifically, the problems with approximate analytical solutions to the Poisson equation and, inversely, the utility of three-dimensional numerical solutions to the Poisson equation using finite-element-modeling are discussed and quantified. Then, results involving numerical calculation of gate-nanowire capacitances in common NWFET geometries and comparison with analytical capacitance estimations are presented.

Chapter 3 discusses a method for extracting quantitative information about surface Fermi level pinning in a semiconductor nanowire based on a combination of FET measurements and numerical modeling. Results are presented using InN nanowires as an example material and contrasted with properties of InN thin films.

In chapter 4, the issue of quantifying the impact of different scattering mechanisms on carrier mobility is tackled. Using well-established universal mobility analysis, we present results on the relative impact of different scattering mechanisms on mobility as a function of band bending in a single nanowire.

Finally, after discussing methods for characterizing free carrier distributions and mobilities in preceding chapters, chapter 5 presents a theoretical study on limitations to doping semiconductor nanowires with radii small enough to show appreciable quantum confinement effects. Though the details of the effect of quantum confinement on the density of states are detailed in that chapter, it is worth outlining here the nanowire size regimes where quantum confinement does and does not significantly impact the classical density of states. Though nanowire shapes vary, we can get a good estimate by assuming a square wire cross section and using the well known quantized energies for an infinite square well of width a:

$$E_{N_x N_y} = \frac{\hbar^2 \pi^2 (N_x^2 + N_y^2)}{2 m_{xy}^* a^2} \tag{1.5}$$

where m_{xy}^* is the effective mass in cross-sectional plane of the wire. Although the transition from not quantum confined to confined is, of course, gradual, it is worthwhile to note at what a the first confinement energy is raised from the ground state by at least $k_B T$ at room temperature ($\sim$ 26 meV). These characteristic values of the square well width a for n-type Si, Ge, GaAs, InN, and InAs are 5 nm, 6 nm, 21 nm, 20 nm, and 35 nm respectively. Free carrier effective mass is the key material parameter that dictates at what wire diameters free carriers will become noticeably confined. For nanowire diameters at or above these a values, the quantum confinement subbands will be easily populated at room temperature and a classical density of states is sufficient (Chapter 2). Below these a values, however, the population of the density of states as a function of energy will start to become significantly altered compared to the classical density of states as a result of quantum confinement (Chapter 5). The nanowires measured or simulated in this dissertation have diameters above these characteristic a values unless otherwise noted and thus warrant the use of classical electrostatics to model them.

Though this work by no means completes the story of characterizing carrier concentration and mobility in semiconductor nanowires, it is the hope of the author that it serves as a good starting point for (1) questioning conventional methods of characterization and (2)

devising methods for improving upon conventional techniques. Thus, chapter 6, along with summarizing the work presented in earlier chapters, also presents ideas for future work on semiconductor nanowire electrical characterization.

Chapter 2

Capacitance of Semiconductor Nanowire Devices

As mentioned in the first chapter, a critical requirement for extracting μ and n from transconductance data is an accurate knowledge of the gate-nanowire capacitance, the device property that dictates the extent to which free carrier concentration in a nanowire can be modulated with a change in applied gate voltage, V_G. This chapter explores limitations in estimating this capacitance using analytical formulas, by presenting finite-element-modeling calculations of gate-nanowire capacitance for different NWFET device geometries. The results highlight the error in calculations of μ and n resulting from faulty capacitance estimates, and are presented so as to provide a set of numerical correction factors to the common capacitance formulas.

2.1 Analytical Expressions for Capacitance

First order estimates of the capacitance between a semiconductor and a gate electrode are made by employing analytical expressions that are valid under a specific set of assumptions. The most common field-effect device geometry used for nanowires is the back-gate geometry (Fig. 2.1 inset) for which the formula for the capacitance per unit length of an infinitely long conducting cylinder above an infinite conducting plane is most often used to estimate the gate-nanowire capacitance:

$$\frac{C}{L} = \frac{2\pi\epsilon_0\epsilon_r}{\cosh^{-1}((R+h)/R)} \tag{2.1}$$

where R is the nanowire radius, ϵ_r the relative dielectric constant of the gate dielectric, ϵ_0 the permittivity of free space, and h the distance between the cylinder and metal plane.

The use of Eq. 2.1 to estimate the gate-nanowire capacitance for backgate NWFETs implicitly requires three key assumptions:

1. It assumes that the gate dielectric (e.g. $\epsilon_r \approx 4$ for SiO_2) fills all space surrounding the nanowire and the gate. This is much different from the widely used, conventional back-gate geometry, where the gate dielectric exists only as a film separating the nanowire and the gate electrode, leaving the nanowire fully exposed to air, which has $\epsilon_r = 1$ (Fig. 2.1).

2. It assumes the nanowire is electrostatically metallic, such that the entire nanowire and the electrodes are an equipotential and the induced charges exist only on the nanowire surface [21]. In reality, however, the nanowire is typically a semiconductor with non-degenerate doping and non-ideal dielectric screening.

3. It assumes the nanowire is infinitely long, such that electric field distortions near the metal electrodes are neglected. However, because of the different geometries and dielectric properties of the electrodes from those of the nanowire, an edge effect, known as the fringe capacitance, perturbs the gate-nanowire coupling when the nanowire has limited length.

These three assumptions limit the accuracy of the gate-nanowire capacitance evaluated from Eq. 2.1. The first limitation due to the oxide geometry has been numerically analyzed in two dimensions (2D), and a factor of two reduction in capacitance was found to account for this limitation [22, 23]. Although the first limitation has been given increasing attention and been corrected for in back-gate experiments [24, 22, 23, 25, 26, 27], the other two assumptions are typically ignored.

In addition, although the back-gate is the most common scheme for gating nanowires, nanowires are also gated in top-gate (Fig. 2.1 (d)) and surround-gate (Fig. 2.1 (e)) geometries, which have higher capacitances than the back-gate setup and allow for easier modulation of nanowire carrier concentration. The common analytical expression used to estimate the capacitance for both top-gate and surround-gate geometries is the formula for the capacitance of an ideally conducting coaxial cable (i.e., a surround-gate geometry with an ideally conducting nanowire):

$$\frac{C}{L} = \frac{2\pi\epsilon_0\epsilon_r}{\ln((R+h)/R)} \tag{2.2}$$

where h is the distance between the inner and outer cylinders and R is the radius of the nanowire. In this case, the first and third assumptions associated with using Eq. 2.1 with a back-gated nanowire device have less of an impact since Eq. 2.2 more closely represents the actual gate geometry and finite length effects have less of an impact when the nanowire is completely shielded by the gate electrode. However, the second assumption, that the nanowire is an electrostatically ideal conductor, still leads to errors as discussed below.

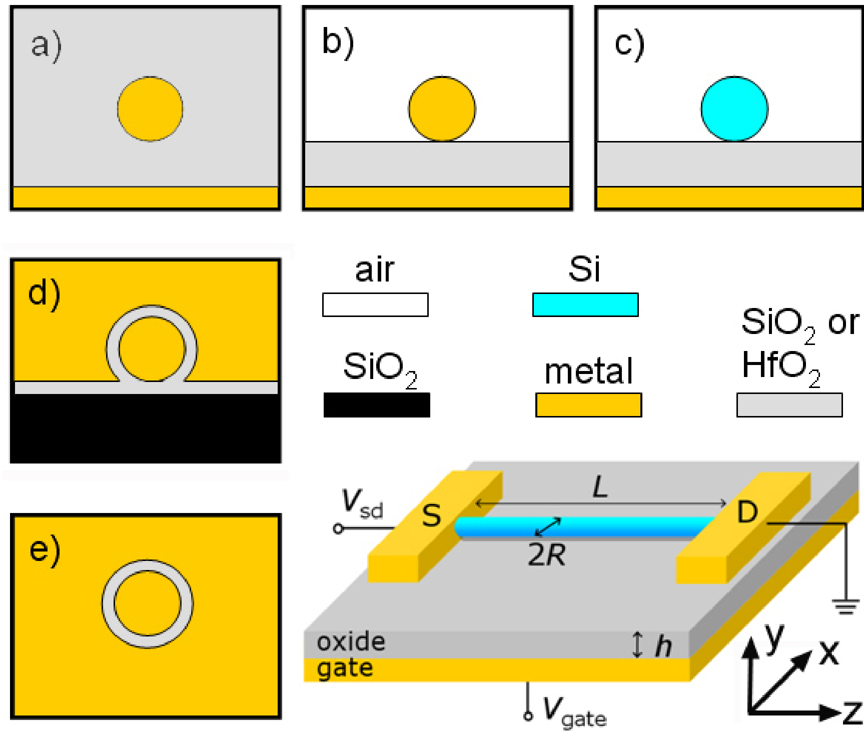

Figure 2.1. Cross-sectional schematics of different NWFET device models. (a) Back-gate nanowire embedded (BE) model, (b) back-gate metallic (BM) model, (c) back-gate semiconducting (BS) model, (d) top-gate metallic (TM) model, and (e) surround-gate metallic (SM) model. A 3D schematic of the BS model is shown with device dimensions. In the BE, BM, and BS models, h is the distance between the nanowire bottom surface and the gate plane; in the TM and SM models, h is the thickness of the oxide that wraps around the nanowire.

2.2 The Poisson Equation for Semiconductors

In this section, we present the electrostatics concepts that will be employed to quantify the limitations of the analytical capacitance expressions discussed above. From the common definition of capacitance, $C = Q/V$, one sees that capacitance is simply the relationship between applied voltage and charge for a capacitor of a given geometry. To be able to improve upon analytical estimates of capacitance, we must therefore start at a more fundamental relationship between potential (voltage) and charge. Fundamentally, that relationship is given by the Poisson equation,

$$\vec{\nabla} \cdot \vec{D} = \rho \tag{2.3}$$

where ρ is the net charge density and $\vec{D}$ is the electric displacement, which is related to the electric field via the dielectric constant, $\vec{D} = \epsilon \vec{E}$, where $\epsilon = \epsilon_r \epsilon_0$, and is therefore related to electric potential, ϕ, by $\vec{D} = -\epsilon \vec{\nabla} \phi$. Thus, the Poisson equation in a region of a uniform dielectric constant is often written

$$\nabla^2 \phi = -\frac{\rho}{\epsilon} \tag{2.4}$$

which more directly shows the relationship between electric potential and charge density. It is important to note that, in general, both ρ and ϕ vary through space (i.e. $\phi(x, y, z)$ and $\rho(x, y, z)$).

What makes solving this equation difficult is the functional form of ρ in a semiconductor. The net charge density in a semiconductor is the sum of charges from ionized impurities and free carriers:

$$\rho(x, y, z) = q(N_D - N_A - n(\phi(x, y, z)) + p(\phi(x, y, z))) \tag{2.5}$$

where N_D and N_A are the concentrations of ionized donors and acceptors, respectively, and the electron (n) and hole (p) concentrations are both functions of $\phi(x, y, z)$, and thus also vary in spatial coordinates. In general, the expressions for n and p are obtained by integrating the density of states (DOS) of the relevant band with the Fermi-Dirac distribution, where the Fermi level (E_F) is displaced by the potential, ϕ, with respect to the conduction band (CB) and valence band (VB) edges:

$$n(\phi) = \int_{-\infty}^{\infty} \frac{g_{CB}(E)}{1 + e^{\frac{E - E_F - \phi}{k_B T}}} dE \tag{2.6}$$

where $g_{CB}(E)$ is the density of states of the conduction band, k_B is the Boltzmann constant, and T is the temperature. Since the simulations in this section are limited to nanowires with $r \geq 10$ nm, we use the classical 3D density of states, as discussed in Chapter 1; the spacings of the first few subbands for a Si nanowire with $r \geq 10$ nm are less than 6 meV, well below $k_B T$ at room temperature. An equivalent expression can be derived for p by taking into account the heavy-hole, light-hole, and split off valence bands. Taking n-type Si as an example, both n and p as a function of local potential ϕ are plotted in Figure 2.2. Two distinct regimes are distinguishable: the nondegenerate regime where $\log(n)$ and $\log(p)$ exhibit a linear dependence on V in comparison with the nonlinear, degenerate regime where the bands are heavily populated. The crossing point of $\log(n)$ and $\log(p)$, when E_F is displaced to mid-bandgap, defines an intrinsic free carrier concentration of $\approx 10^{10}$ cm^{-3}

in Si at room temperature. The classical 3D DOS for both CB and VB are shown in the inset in Figure 2.2. After substituting Eqs. 2.5 and 2.6 into the Poisson equation (2.4), we

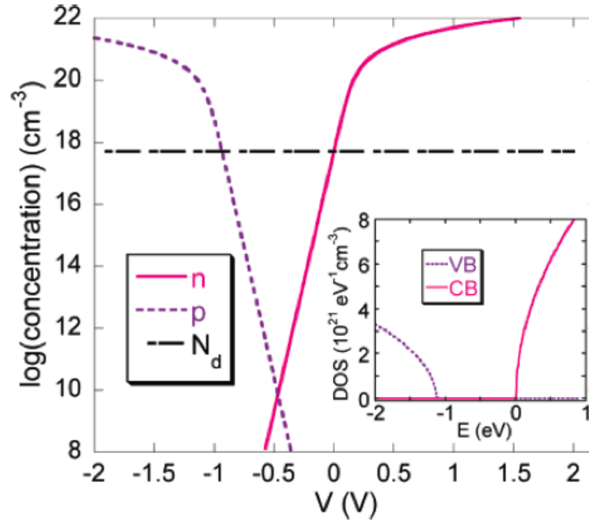

Figure 2.2. Electron and hole concentrations as a function of local potential in n-type Si doped with $N_D = 5 \times 10^{17}$ cm^{-3}. At $V = 0$, the Fermi level is positioned with respect to the CB and VB edges such that n is equal to N_D to maintain charge neutrality. Inset: The density of states for the conduction and valence bands of Si in the effective mass approximation. Here, for $N_D = 5 \times 10^{17}$ cm^{-3} and at room temperature, the natural Fermi level lies at $E_F = -0.11$ eV.

are left with a non-linear partial differential equation (PDE). The Poisson equation, in this form, has no analytical solution, so to obtain a solution (i.e., solve for $\phi(x, y, z)$ throughout the regions of interest) one is forced to either make analytical approximations or solve the equation numerically.

2.3 Finite Element Modeling

Numerical solutions to PDEs in complicated three-dimensional geometries (Fig. 2.1, for example) are most commonly obtained using finite-element modeling (FEM). Although numerical solutions to PDEs are by definition approximate, in cases where obtaining an analytical solution requires the use of (often multiple) assumptions, numerical solutions can provide much higher degrees of accuracy than approximate analytical solutions. The basic premise of using FEM to solve PDEs involves dividing the simulation region up into discrete elements, applying the appropriate boundary conditions, and using an iterative process to numerically approximate a solution to the governing equation at each element to a specified degree of accuracy. Taken together, the elements provide a psuedo-continuous solution to the governing PDE, *as long as* the size of the elements (mesh size) is significantly smaller than the minimum size of phenomena of interest. Otherwise, if the element size is too large, mesh-

induced artifacts will be present in the final solution and physically significant variations in the variables of interest (ϕ and n in our case, for example) will be lost.

Proper boundary conditions are, of course, crucial to obtaining a solution that correctly corresponds to the physical situation of interest. In solving the Poisson equation in our simulations, the following boundary conditions were used ("boundaries" corresponds to 2D surfaces in 3D simulations and 1D edges in 2D simulations):

- $\phi = 0$ was used at all grounded boundaries. In our simulations this includes the source and drain electrodes.
- $\phi = V_G$ was used at the boundary between the gate dielectric and gate electrode.
- $\vec{n} \cdot \vec{D} = 0$, where $\vec{n}$ is a unit vector normal to a surface, was used at all outer most boundaries of the simulation domain where ϕ is not otherwise specified. This ensures that there is no electric field perpendicular to the surface at these outer most boundaries. A good example of when this boundary condition is used is at the top and side surfaces of "air" in a 3D back-gated FET model. Experimentally, far away from the nanowire device, the electric field does go to zero, warranting this boundary condition. However, if the simulation domain is not drawn large enough, this boundary condition will result in the PDE solver converging to a solution that *forces* $\vec{E}$ to go to zero at these outer surfaces, and if they are too close to the nanowire device, the solution will not be physically realistic. To ensure the simulation domain is drawn acceptably large, a series of simulations with increasing domain size must be performed until the solution does not change to within the desired level of accuracy.
- $\vec{n} \cdot (\vec{D}_1 - \vec{D}_2) = 0$ was used at all interior boundaries between materials with different ϵ_r.
- $\vec{n} \cdot (\vec{D}_1 - \vec{D}_2) = Q_s$, where Q_s is a 2D charge density was used at all interior boundaries where there was a fixed surface charge, for example, semiconductor surfaces with Fermi level pinning (see Chapter 3 and 4).

2.4 Capacitance Calculations of Semiconductor Nanowire Devices

2.4.1 Introduction

In this section, to gauge and compare the magnitude of all three limitations to analytical capacitance equations discussed above, we summarize results from numerical simulations of back-gate nanowire field effect transistors by solving the classical Poisson equation in three dimensions (3D). Our simulations allow for a gate oxide in a film geometry, a semiconducting nanowire channel, and also a finite nanowire length. In this way, all of the assumptions

inherent to Eqs. 2.1 and 2.2 can be tested. Top-gate NWFETs are also simulated and compared to the back-gate devices. As a representative example, we use n-type Si as the nanowire material and SiO_2 or HfO_2 as the gate oxide in the simulations. The surface of the nanowire is assumed to be fully passivated, such that surface Fermi level pinning and other surface effects can be neglected.

In solving for the electric potential $\phi(x, y, z)$ in Poisson's equation (Eq. 2.4), the space charge density ρ is set to $q(N_D - n(\phi) + p(\phi))$ in Si and is otherwise zero. The metallic gate and source and drain electrodes are characterized with $\epsilon \to \infty$ to ensure that they are equipotential bodies, while all other materials (e.g. Si/SiO_2/air) are each set to their respective values of ϵ. The contacts between the electrodes and the nanowire are assumed to be ohmic so that no potential drop associated with a Schottky barrier exists on the contacts [28]. We ignore work function differences between the electrode, gate metal, and the semiconductor.

2.4.2 The Models

To compare the gate-nanowire capacitance under a variety of physical assumptions, we define five different models (Fig. 2.1):

1. The back-gate nanowire embedded (BE) model (Fig. 2.1 (a)) using the exact same assumptions implicit in Eq. 2.1, with the dielectric filling the entire space surrounding a metallic nanowire. The simulated capacitance from this model will be compared with the value calculated directly from Eq. 2.1 as a control for these simulations.
2. The back-gate metallic (BM) model (Fig. 2.1 (b)), where the gate oxide exists only as a film separating the nanowire and the gate plane, but the nanowire is still rendered electrostatically metallic. In this model, the first limitation to Eq. 2.1, which assumes that the nanowire is fully embedded in the gate dielectric, is lifted. The simulated capacitance from this model will be compared with previously reported simulations.
3. The back-gate semiconducting (BS) model (Fig. 2.1 (c)) to represent the realistic back-gate NWFET, where the oxide exists only as a film separating the nanowire and the gate plane, and the nanowire is semiconducting, with space charge governed by Eq. 2.5. In this model both limitations to Eq. 2.1 are lifted.
4. The top-gate metallic (TM) model (Fig. 2.1 (d)) [24, 29] to compare with the back-gate devices.
5. The surround-gate metallic (SM) model (Fig. 2.1 (e)), which can be experimentally fabricated [19] but is often used just as a simpler model to calculate the capacitance of top-gate NWFETs. Errors in computed capacitance when using the SM model to model a top-gate NWFET will be explored.

The simulation was carried out using the software Flex-PDE, which is a finite element partial differential equation solver. The back gate is held at V_G, and both the source and

drain electrodes are grounded such that no current flows, ensuring a constant E_F in the nanowire. We model the device at $V_{sd} = 0$ to simulate the small-bias, linear regime where carrier mobility is usually determined in experiments.

The potential contours in the $z = 0$ plane for the BE, BM, and BS models, simulated in 3D with identical parameters, are shown in parts a, b, and c of Fig. 2.3, respectively. As a consequence of both the different spatial arrangement of the gate oxide (in both the BM and BS models) and the semiconducting response in the nanowire (in the BS model), the potential distributions in these three models differ substantially. In the inset of each plot, a more detailed image of the nanowire potential distribution is shown.

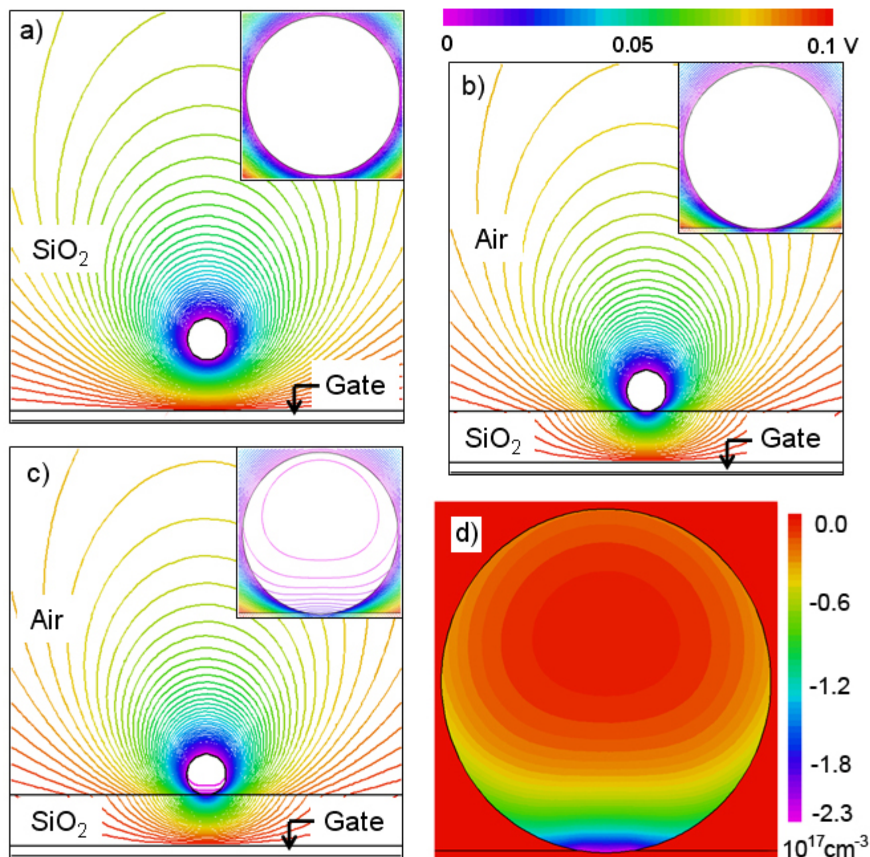

Figure 2.3. Equipotential contours of the (x, y) cross-sectional plane at the center of the nanowire ($z = 0$) for the BE (a), BM (b), and BS (c) models. The displayed area is 400 nm $\times$ 400 nm, out of a simulation domain of 500 nm in both x and y directions. The color bar is shown above (b). A magnified image of the Si nanowire is shown in the inset (color scale different from main image), with equipotential contour lines 1 mV apart from each other. In (d), the net space charge distribution in the nanowire in the BS model is shown. These figures were generated by simulating with the following parameters: $R = 20$ nm, $h = 50$ nm, $L = 1$ μm, $V_G = 0.1$ V,and $N_D = 5 \times 10^{17}$ cm^{-3} (for the BS model).

As expected, a nonuniform potential distribution is evident when the nanowire is semiconducting (Fig. 2.3). In this case, the minimum potential occurs at a point off the center of the nanowire, away from the gate. The potential reaches a maximum at the edge of the nanowire that touches the gate oxide. The voltage drop in this nanowire cross section is about 10% of the total V_G. The variation of ϕ in the Si nanowire translates to a net space charge distribution of $N_D - n(\phi) + p(\phi) \approx N_D - n(\phi)$ as shown in Fig. 2.3 (d). As expected, a dense negative space charge accumulates at the bottom of the nanowire due to the electrostatic attraction from the positive V_G, and the rest of the nanowire is largely charge neutral, with $n(\phi) = N_D$, as a result of screening of the applied electric field by the accumulated negative charge at the bottom surface. At smaller V_G or lower N_D, this space charge distribution becomes more uniform because the nanowire channel becomes increasingly nonmetallic. This space charge picture differs considerably from the metallic-nanowire model implied by Eq. 2.1, where induced charge would exist only on the nanowire surface, and also from the assumption of uniform charge distribution in the cross section, commonly used in analyses of nanowire carrier transport. This shows the importance of accounting for the semiconducting properties of nanowires in the discussion of device performance in NWFETs.

To compare these models in a quantitative manner, we determine the gate-nanowire capacitance by calculating the electrostatic energy stored in the system,

$$\frac{1}{2}C \cdot V_G^2 = \int \frac{1}{2}\epsilon[\vec{\nabla}\phi(x, y, z)]^2 \, dx \, dy \, dz \tag{2.7}$$

To model the capacitance with minimum disturbance from the edge effect, we construct the device in 3D (Fig. 2.1 inset) and choose a sufficiently long nanowire ($L = 1$ μm) to solve Eq. 2.3. A thin (x, y) plane slice in the middle of the nanowire (at $z = 0$), where the field distribution is nearly a constant along the z-direction, is sampled. The integration in Eq. 2.7 is limited to this slice, and the capacitance per unit length is obtained from dividing C by the thickness of the slice. For the metallic models, where the nanowire is an equipotential body with the electrodes, Eq. 2.7 precisely defines the capacitance between the gate and the nanowire. However, for the semiconducting model, because the potential varies inside the nanowire, the capacitance between the nanowire and the gate is no longer well defined. As such, for practical purposes, we define the capacitance of the middle slice for semiconducting nanowires using the total space charge induced within the slice divided by the voltage difference between the gate (V_G) and the electrodes (grounded),

$$C = \frac{q}{V_G} \int [N_D - n(\phi) + p(\phi)] \, dx \, dy \, dz \tag{2.8}$$

This definition allows one to determine the amount of induced charge in the nanowire at a given V_G.

2.4.3 Gate Voltage and Dopant Concentration Effects

In Fig. 2.4, we show the simulated capacitance for all three back-gate (BE, BM, and BS) models as a function of V_G. As expected, BE and BM capacitances remain constant when

V_G varies. The control, the simulated BE capacitance, agrees within 2% of the analytical expression Eq. 2.1. The deviation is caused by the limited size of the simulation domain; a willingness to devote more computation time could eliminate this 2% mismatch. Consistent with previous reports based on 2D simulations [22, 23] the BM capacitance is significantly lower than the BE capacitance (for these system parameters, by $\approx 48\%$), indicating a large overestimation of the capacitance for back-gate NWFETs when using Eq. 2.1. This results in both an underestimation of the carrier mobility and an overestimation of the doping level by approximately a factor of 2, which can have serious consequences for device engineering.

Figure 2.4 also shows the BS capacitance calculated from Eq. 2.8. It approaches the BM value in the accumulation regime ($V_G \lesssim 1$ V), as expected from the nearly metallic electrostatics in the nanowire. However, as the nanowire moves into the depletion regime with increasingly negative V_G, the BS capacitance deviates severely from the BM, decreasing to $< 65\%$ of the BM ($< 32\%$ of the BE) near the threshold voltage, reflecting weaker charge screening in the depleted nanowire. Such a capacitance decrease from the ON to OFF state is well-known in planar metal-oxide-semiconductor field-effect transistors [30] and has recently been experimentally observed in top-gate Ge NWFETs [20]. At further negative V_G, the n-type nanowire enters the inversion regime, where the valence bands start to be populated by free holes and the capacitance increases back toward the BM capacitance.

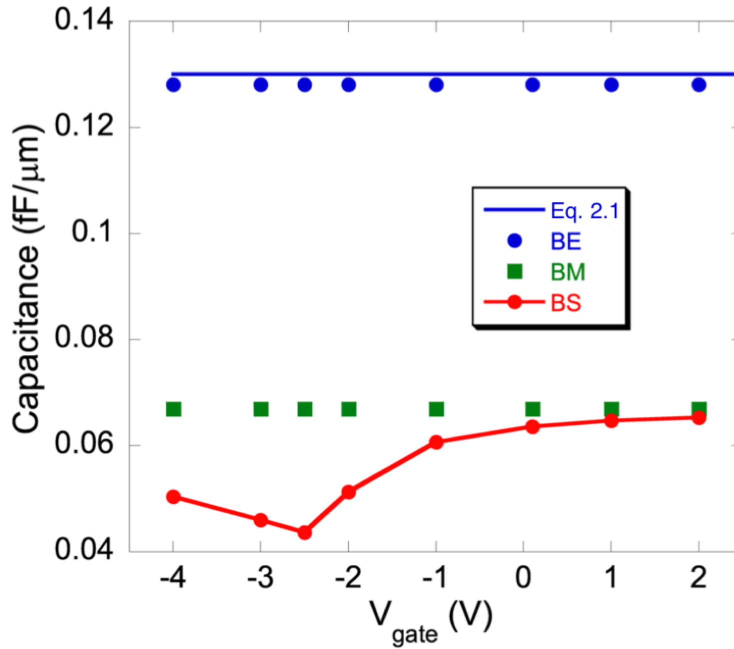

Figure 2.4. Capacitance per μm of nanowire length obtained as a function of V_G from simulations of the BE, BM, and BS models. Also shown is the capacitance calculated from Eq. 2.1 for the BE model. The parameters used were $R = 20$ nm, $h = 50$ nm, $L = 1$ μm, and a gate oxide of SiO_2. For the BS model, $N_D = 5 \times 10^{17}$ cm^{-3}.

We calculated these three capacitances (BE, BM, and BS) in the small V_G limit as a function of N_D and nanowire radius R, while keeping the gate-nanowire distance, h, constant. The dependencies are shown in Fig. 2.5, where the capacitance is normalized to the calculated

value from Eq. 2.1 and R is normalized to h. In agreement with Fig. 2.4, in the range of R/h investigated (0.1-0.8), the BM capacitance differs significantly from BE and hence a correction factor must be considered when using Eq. 2.1 to calculate the gate-nanowire capacitance in back-gate NWFETs. Specifically, in this case, ϵ_{eff} should be set to $\approx 0.48\epsilon_r$. This factor encapsulates the contributions of both the SiO_2 and air. This "effective" ϵ_r can be used to lift the gate oxide geometry limitation of Eq. 2.1, restoring the validity of Eq. 2.1 for the BM model.

Many groups have implemented this correction to Eq. 2.1 in calculating an experimental mobility [25, 26], citing an "average" dielectric constant between the oxide and air. It should be noted, however, that although a simple mathematical average between the dielectric constants of SiO_2 and air happens to approximately correct for the error in capacitance from Eq. 2.1, such a mathematical average does not result in the appropriate correction for high-ϵ_r oxides as shown below. Additionally, when the semiconductivity (and finite length) of the nanowire are accounted for, one sees in Fig. 2.5 (and Fig. 2.8) that using a constant effective ϵ_r does not properly adjust for the capacitance at all values of V_G, N_D, R, and nanowire length.

The N_D dependence in Fig. 2.5 quantifies the second limitation of Eq. 2.1 that neglects the semiconducting nature of the nanowire. As demonstrated in Figs. 2.4 and 2.5, this correction is negligibly small for $N_D \gtrsim 5 \times 10^{17}$ cm^{-3} in the strong accumulation regime ($V_G \gtrsim 1$ V). However, this factor becomes significant and must be included when $N_D \lesssim 5 \times 10^{17}$ cm^{-3}, or when the device is operated near the threshold V_G. This effect is stronger for nanowires with smaller radii, consistent with results from Vashaee et al. [23], where 2D simulations of nonideal conducting cylinders of different diameters were performed. Figures 2.4 and 2.5 show the fundamental limitations to accuracy one can achieve in simulating the capacitance when the nanowire is modeled as a perfect conductor. Because this difference is caused by the semiconducting properties of the nanowire, rather than the device geometry, it is expected to be present in top-gate and surround-gate devices as well.

Lastly, the dependence on the radii of nanowires serves to highlight how these semiconducting effects are unique to materials with dimensions on the order of the electric field screening length. In non-degenerately doped semiconductors, the characteristic length required to screen electric fields is often approximated by the Debye screening length,

$$\lambda_D = \sqrt{\frac{\epsilon k_B T}{N q^2}} \tag{2.9}$$

where N is the density of mobile carriers, which for an n-type semiconductor is equal to the electron concentration n. For Si at room temperature, for example, the Debye length ranges from $\sim$ 4 - 130 nm for electron concentrations between 10^{15} - 10^{18} cm^{-3}. Figure 2.5 shows that in the limit of $R \gg h$ (i.e, when a "nanowire" becomes "bulk"), the capacitance of a semiconducting wire of almost any doping concentration will approach that of a metallic wire. This is because for very large material dimensions the Debye length is a negligible fraction of the total material size and any induced charge can be safely approximated as residing on the surface of the material. Thus, this semiconducting limitation to analytical capacitance formulas is a uniquely *nanoscale* effect.

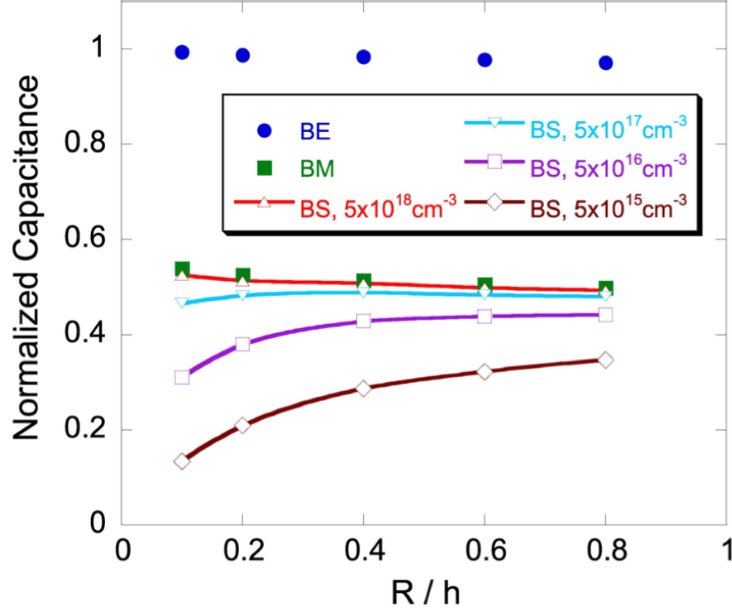

Figure 2.5. Capacitance normalized to the analytical value calculated from Eq. 2.1 as a function of R normalized to h over a wide range of N_D. The parameters used were $h = 50$ nm, $L = 1\mu$m, and $V_G = 0.1$ V. We note that for the points at $R/h = 0.1$, quantum confinement effects are expected to modify the capacitance values from the values shown here, calculated using a classical density of states.

2.4.4 Dielectric Constant and Gate Geometry Effects

In advanced NWFET technologies using high-ϵ_r dielectrics, the correction factors discussed above are found to be even more drastic and cannot be corrected by the simple mathematical averaging as can be done for SiO_2 and air. For example, by using the device parameters in Fig. 2.4 but replacing SiO_2 ($\epsilon_r \approx 4.5$) with HfO_2 ($\epsilon_r \approx 22$), the BM capacitance is further reduced from 52% to 31% of the BE capacitance (Fig. 2.6). A simple mathematical average of the dielectric constants of air ($\epsilon_r \approx 1$) and the gate dielectric will always, by definition, yield an effective dielectric constant (and thus capacitance) that is $\approx 50\%$ of the dielectric constant of the gate dielectric (i.e. $\frac{x+1}{2} \approx \frac{x}{2}$ when $x \gg 1$). Clearly, this does not suffice when HfO_2 is the gate dielectric. It is worth emphasizing here that percent errors in computed gate-nanowire capacitance lead to proportional mis-estimates of nanowire carrier mobility and carrier concentration, as per Eqs. 1.3 and 1.4. The normalized capacitance as a function of R/h is shown in Fig. 2.6 for both SiO_2 and HfO_2. Also shown in Fig. 2.6 is the capacitance of the TM device [24, 29], normalized by the value expected from a perfect surround-gate metallic (SM) device (Eq. 2.2). It can be seen that the correction for the top-gate device geometry is much smaller than that for back-gate due to the closer resemblance between the TM and SM geometries.

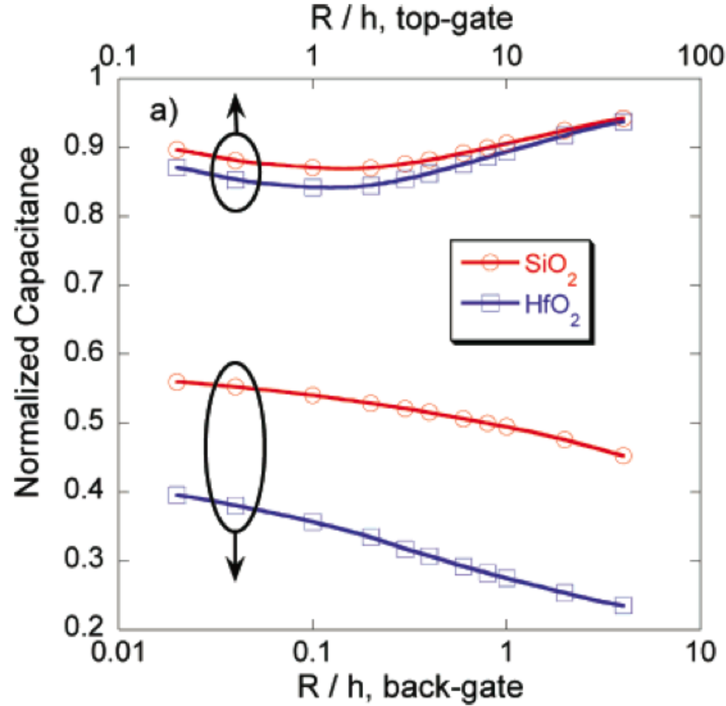

Figure 2.6. Normalized gate-nanowire capacitance as a function of R/h for the BM (bottom axis) and TM (top axis) models using SiO_2 and HfO_2 as the gate oxide. Note the different scale for these two axes. Here the BM and TM capacitances are normalized to the values calculated from Eqs. 2.1 and 2.2, respectively. In the simulation, $h = 50$ nm, $L = 1\mu$m, and $V_G = 0.1$ V.

2.4.5 Finite Length Effects

One can expect that the metallic electrodes used to contact the nanowire will cause a distortion of the nearby electric field. Thus for short-channel devices, it is expected that this will cause a significant change in the gate-nanowire capacitance. To quantify this "edge effect", we performed 3D simulations of nanowires with varying length. The potential distribution along the side-view (y, z) plane is shown in Fig. 2.7 for two devices, one with a nanowire of length 500 nm (main) and the other with a nanowire of length 50 nm (inset). A stronger variation of ϕ along z around the nanowire is evident for the shorter device. This comparison highlights the necessity of performing 3D simulations for devices with finite length. Moreover, for the semiconducting model, a 3D simulation is required *even for a long nanowire device*: A sufficiently long nanowire in the metallic models can be simulated in 2D in the (x, y) plane where, as a boundary condition, the entire nanowire is at the same potential as the electrodes (grounded). In the semiconducting model, however, such a boundary condition does not exist to justify a simplified 2D simulation. The entire nanowire is not, of course, at the same potential as the source and drain electrodes, as shown in Fig. 2.3c. But more importantly, in a 2D simulation, one does not know *a priori* what the potential distribution in the nanowire cross section is, thus inputs from a 3D simulation are required to locate the minimum potential point in the (x, y) plane and use that as a boundary condition

on ϕ. This is an important distinction between 2D and 3D simulations of semiconductor nanowires.

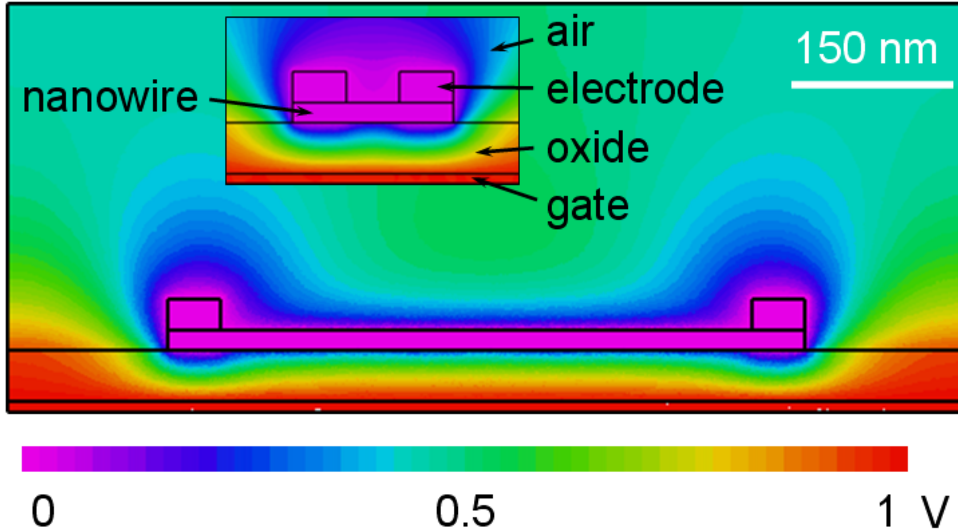

Figure 2.7. Electric potential distribution in the (y, z) plane in the BM model showing the potential variation along the nanowire due to the edge effect. In the simulation, the following parameters were used: $R = 10$ nm, $h = 50$ nm, $L = 500$ nm (main) or 50 nm (inset), $V_G = 1.0$ V, oxide is SiO_2, and the electrodes have dimensions of 500 nm (length), 50 nm (height) and 50 nm (width) in the x, y, and z directions, respectively.

The quantitative impact of the finite length effect is calculated by comparing the BM model in both 2D and 3D, as shown in Fig. 2.8. Here we used the BM instead of the BS model in order to decouple the semiconductivity and short-channel effects. As per Fig. 2.5, a metallic channel can be safely assumed in simulation of the realistic, semiconducting channel when $N_D \lesssim 10^{18}$ cm^{-3}. In the 2D simulation, the entire nanowire is set to ground potential when solving the Poisson equation, and the capacitance is calculated from Eq. 2.7. This capacitance corresponds to that of an infinitely long nanowire in a backgate device geometry and is identical to the value obtained by the 3D "slice method" described earlier for long ($\gtrsim$ 1μm) nanowires. For the 3D situation, Gauss's law was applied to the entire nanowire channel (but not the electrodes) to compute the total charge (Q) induced within the nanowire, and the gate-nanowire capacitance was obtained from $C = Q/V_G$. As expected, the 3D capacitance as a function of device length, L, deviates considerably from linearity for short L. At $L = 1\mu$m (i.e., the aspect ratio of the nanowire is $L/R = 100$), the 3D capacitance agrees well with the 2D capacitance, indicating a negligible edge effect. At $L = 20$ nm ($L/R = 2$), the 3D capacitance is only 16% of the 2D value. Here, the fringe capacitance effect is quantitatively exemplified using one size of the source-drain electrodes while varying the channel length. Previous work [31] on carbon nanotube transistors has demonstrated how the size and shape of source-drain contacts affect the capacitance. We expect similar capacitance variations with respect to electrode size and shape in NWFETs. Figure 2.8

therefore quantifies the third limitation of Eq. 2.1 due to electrostatic screening from the electrodes when the nanowire channel is short.

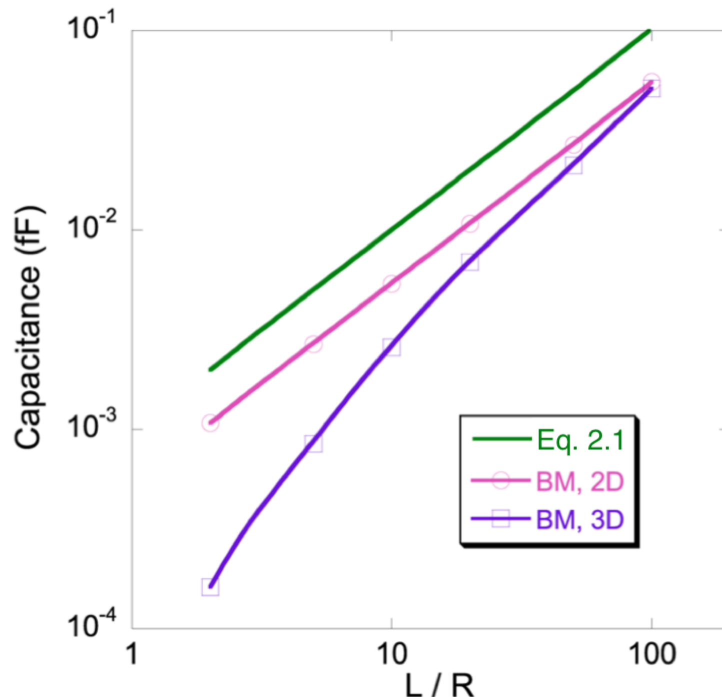

Figure 2.8. Capacitance between the back gate and nanowire as a function of L/R for the BM model. In the simulation, $h = 50$ nm, $R = 10$ nm, and $V_G = 0.1$ V, and the gate dielectric is SiO_2.

2.4.6 Conclusions

The finite element modeling results presented in this chapter highlight the limitations to using conventional analytical formulas for computing the capacitance of NWFETs. Specifically, it is worth emphasizing three major limitations to analytical formulas for capacitance:

1. The geometrical layout of all material components of the NWFET may not match the layout *assumed* by the formula. For example, Eq. 2.1, which is used for backgate devices, assumes the gate dielectric fills all space between the nanowire and gate electrode, when, experimentally, the gate dielectric exists only as a thin film between the nanowire and gate electrode.

2. Analytical formulas for capacitance necessarily assume the "plates" of the capacitor are ideal conductors. When one of these plates is a semiconductor with at least one dimension on the order of its Debye screening length, an additional correction to the analytical formula must be employed. This effect is highlighted in Figs. 2.4 and 2.5 for

nanowires, but it should be noted that such an effect is expected for other nanoscale semiconductors as well (e.g., ultra-thin films, tetrapods, quantum dots).

3. For short-channel devices, where the length of the FET channel approaches the length over which the electrodes perturb the surrounding electric field, further corrections to capacitance formulas are necessary, as presented in Fig. 2.8.

Together, these limitations to capacitance formulas serve to emphasize that in general, electrostatics approximations that work well for bulk semiconductors must be approached with caution before being used for nanoscale semiconductors.

Chapter 3

Quantifying Surface Fermi-level Pinning in Semiconductor Nanowires

3.1 Background

3.1.1 Importance in Nanoscale Materials

Surface Fermi level pinning has long been a major issue for semiconductors. Specifically, despite changes in the extrinsic doping level in the bulk of a semiconductor, the Fermi level at the surface, at a metal-semiconductor interface, or an oxide-semiconductor interface can remain pinned at a particular energy with respect to the band edges. This results in band bending in the near surface region of the semiconductor, required to accommodate different E_F values, with respect to the band edges, at the surface and in the bulk (Fig. 3.1). The magnitude and sign of this band bending expectedly depends on the magnitude and type of extrinsic doping.

The origin of this pinning effect is generally ascribed [32] to a large density of surface states with a narrow spread in energy that is located in the bandgap for most semiconductors, but can be located in a band for certain semiconductors (e.g., InN, InAs) (see, for example, Fig. 5.1 in Chapter 5). To maintain charge neutrality for the surface atoms, these states remain partially full, thus fixing E_F at a particular energy with respect to the conduction and valence band edges. Moreover, because the density of these surface states is large, when the semiconductor is contacted by a metal, the energy of the Fermi level with respect to the band edges at metal-semiconductor interfaces has been known to be largely independent of different metal work functions [33]. This gives rise to the term “pinning” to describe

the relative inability to control the energy of the Fermi level at a surface or interface by, for example, extrinsically doping the semiconductor or using metals with different work functions to achieve ohmic or Schottky contacts. In fact, the lack of significant Fermi level pinning at the Si/SiO_2 interface is one of the key reasons for the explosion of Si-based electronics.

This band bending can be detrimental for technological applications because it precludes external control of the surface electronic properties of the semiconductor. For example, it can be difficult or impossible to make a rectifying contact to an n-type semiconductor where the Fermi level is pinned above the conduction band minimum (e.g., InN) [34, 35]. Conversely, it can be difficult to make ohmic contact to an n-type semiconductor where the Fermi level is pinned close to the valence band minimum.

In conventional bulk semiconductors, though this intrinsic band bending can affect the electronic properties of the near surface region, a large part of the bulk remains relatively unaffected (Fig. 3.1 (a)). In nanoscale semiconductors such as nanowires, however, the dimensions of the material itself are often on the order of the Debye screening length, so the majority of the material volume can be under the influence of an intrinsic electric field due to surface Fermi level pinning. Thus, Fermi level pinning can have a dramatic influence on the electronic properties of nanoscale semiconductors and must therefore be characterized thoroughly (Fig. 3.1 (b)).

3.1.2 Band Bending Measurement Methods

One of the more direct electrical methods of measuring band bending in a semiconductor is through capacitance-voltage (C-V) measurements, which involve applying a DC voltage between a metal and semiconductor through a non-conducting interface (either an oxide or a Schottky barrier) and measuring the capacitance across a range of voltages. From the C-V data, one can extract the carrier concentration profile in the semiconductor, which is related to the band bending in the semiconductor through the Poisson equation [19]. In addition, information about density and energy of surface states can be gleaned from the frequency dispersion of C-V data [19]. Just like the carrier distribution, surface state density is directly related to the intrinsic band bending in a semiconductor through the Poisson equation. Though the C-V technique has been used extensively for charge profiling in bulk and thin film semiconductors, it has received only limited use so far for nanoscale semiconductors [19, 20]. This is because single nanostructure devices have very small capacitances, which makes experimental measurements difficult, as discussed in the previous chapter. This difficulty also motivates the exploration of more experimentally accessible methods of deducing band bending and surface charge of single nanostructure devices[1].

[1] This size issue of nanostructures also makes optical methods for determining surface band bending, such as x-ray photoemission spectroscopy, difficult on a single-nanostructure level. To circumvent these issues, ensemble measurements on arrays of nanostructures can be performed, but less information about the material is obtained from ensemble measurements than from single-nanostructure measurements because of averaging effects (for example information about the scatter in data from individual nanostructures is reduced to a single average value).

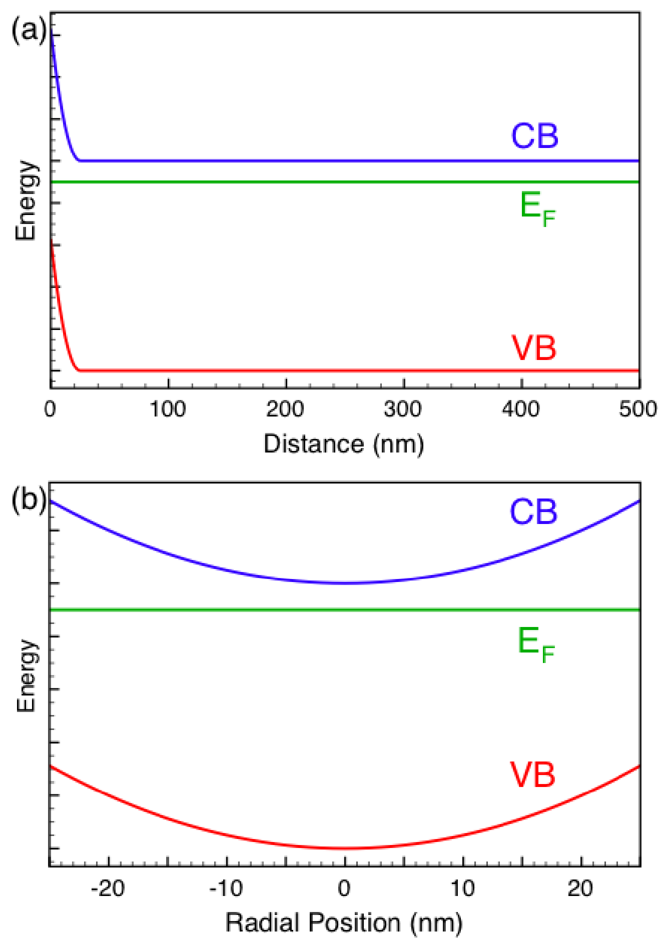

Figure 3.1. Band bending schematics for (a) a film and (b) a nanowire. The magnitude and spatial extent of band bending in both (a) and (b) are the same. In this case, the Fermi level is shown to be pinned inside the bandgap, corresponding to surface states that have a narrow density of states inside the bandgap. The energy scale is intentionally left blank, so as to be semiconductor independent. One can interpret energy differences as a fraction of the bandgap.

The more commonly used experimental technique for extracting materials properties from semiconductors is the FET measurement, as discussed in previous chapters. Field-effect transistor measurements are electrostatically similar to C-V as both involve externally applying an electric field to modulate charge in the semiconductor. In FET measurements, however, the charge in the semiconductor is monitored via a current instead of capacitance, which, although experimentally easier to measure, has the disadvantage that information regarding the carrier concentration is coupled with the carrier mobility. These two material parameters can be decoupled by *calculating* the capacitance in the FET technique instead of measuring it as in the C-V technique. For many thin film device geometries, sufficiently accurate estimates of the semiconductor-gate capacitance can be obtained from analytical equations. However, as discussed in Chapter 2, for nanoscale semiconductor devices, more careful numerical modeling is required to obtain reliable values of semiconductor-gate capacitances.

Nevertheless, because FET measurements also involve the modulation of free carrier concentration in the semiconductor, one can expect that surface Fermi level pinning in semiconductor nanostructures will have a significant influence on the FET data. Why must this be the case? This is best understood qualitatively by remembering that *free charge screens electric fields*, and therefore, the more free charge a material has, the less its total free carrier concentration will be affected by an externally applied electric field. For example, metals have an abundance of free charge that completely screens external electric fields in a very short distance from the surface ($\approx$ 1 nm), and thus applying an external electric field will not change a metal's total free carrier density significantly. An insulator or lightly doped semiconductor is at the opposite end of the spectrum. A relatively small electric field can penetrate a great distance and have a significant effect on its total free carrier density. But the free carrier concentration in a semiconductor with band bending near the surface has a *varying* degree of free charge as a function of position. Thus, if a gate voltage is applied, the amount of total charge induced in the semiconductor will change as this voltage is swept and its electric field penetrates deeper and deeper into the material, probing different free carrier concentrations along the way. Thus the current versus gate voltage data must be characteristic of the particular charge profile in that semiconductor, and consequently its Fermi level pinning position.

However, as mentioned, current is the product of both carrier concentration *and* mobility. Therefore, if carrier concentration and mobility can be separated through proper electrostatics modeling, one can expect that the Fermi level pinning position can be extracted from FET data. In the following section, using InN nanowires as an example material system and a polymer based electrolyte as the gating medium, we report results on the extraction of the Fermi level pinning position in single nanowires from FET measurements.

3.2 Measuring Band Bending in InN Nanowires

3.2.1 InN Nanowires

On one hand, InN is an ideal material system to study intrinsic band bending because the Fermi level at the surface is pinned at a very high energy above the CB minimum (~ 0.9 eV) [34] in all polar (c-plane) thin films and non-polar (a/m plane) films exposed to ambient [36, 37], so if we predict that Fermi-level pinning will effect the FET characteristics of a nanowire, we are most likely to see such an effect in InN compared to other semiconductors. On the other hand, however, this property, combined with the propensity of native defects to dope InN n-type, makes InN nanowires display degenerately doped (or near-metallic) characteristics. As such, it is difficult to fully deplete InN nanowires with a conventional back-gate, and a dielectric with a larger permittivity or a device geometry with a higher capacitance, such as an electrolyte gate, is required to significantly change the electron concentration and obtain useful FET data.

For reasons discussed earlier, the unusual surface E_F pinning in InN is generally considered detrimental for technological applications [35], and therefore a tremendous amount of work has gone into characterizing and attempting to control this E_F pinning in InN thin films [38, 35, 34, 36]. Unfortunately, eliminating this E_F pinning has proved difficult, although a sulfur-based surface treatment has been reported to be able to reduce the E_F pinning position by a few tenths of an eV [39]. The only report to date of no surface pinning at an InN surface was by Gwo et. al. [36], who reported that non-polar surfaces cleaved and measured in ultrahigh vacuum displayed no evidence of E_F pinning at the surface. As a result of these issues, the growth of InN nanowires with non-polar sidewalls [40, 41] has been accompanied with attempts to characterize their surface electronic behavior and deduce whether InN nanowires have similar surface electron accumulation at their non-polar sidewalls as their thin film counterparts [42] .

Several reports on characterizing the surface electronic properties of InN nanowires through electrical measurements have consisted of exploring the dependence of nanowire resistivity (or conductivity) on radius [42, 43, 44]. The most detailed and latest such paper by Werner et. al. [44] reported an observed power law relationship between conductance normalized by length and nanowire radius, r_{nw}. They noted that for current flow through the bulk of a wire, the conductance should scale as r_{nw}^2 whereas, for conduction through a 2D sheet on the surface of a wire, the conductance should scale as r_{nw}. But their data shows conductance scaling as r_{nw}^{β}, where $\beta = 1.6$, indicating that in the range of r_{nw} measured, conduction through their InN nanowires has contributions from both the core and the surface accumulation layer. Although suggestive of conduction through a surface accumulation layer, these results do not provide an understanding of the nature and extent of this surface accumulation (e.g., depth into the wire, E_F pinning energy, density of electrons).

3.2.2 Device Fabrication and Conductivity Measurements

InN nanowires were grown by plasma-assisted molecular beam epitaxy (PA-MBE) on (100) Si substrates. The nanowires grow in the c-direction, show clear hexagonal facets, uniform lengths, and are free of extended defects as detailed in Ref. [40]. Figure 3.2 shows SEM images of the as-grown nanowires. Nanowires were removed from their growth substrate by ultrasonication in an IPA solution and subsequently dropcast onto SiN (~200 nm)/Si device chips for device fabrication. Contacts to nanowires were defined by electron beam lithography. The wires were dropped onto a pattern consisting of the larger electrodes ending in 20 squares and an array of numbers in the center. After imaging the positions of the wires with respect to the numerical grid, a second layer of contacts to individual wires were drawn lithographically. After developing the contact pattern for the second layer, the device chips were treated with an O_2 plasma (70W) for 30 seconds to remove organic surface contaminants, and Ti/Au metal contacts were deposited by electron-beam evaporation, as shown in Fig. 3.3.

Figure 3.4 (a) shows typical current-voltage ($I(V_{SD})$) characteristics of an InN nanowire. All devices measured showed linear $I(V_{SD})$ behavior with resistances on the order of kΩ, corresponding to conductivities in the range of 700 $(\Omega\text{-cm})^{-1}$ to 2300 $(\Omega\text{-cm})^{-1}$, which is typical of InN nanowires [44, 43, 45]. Extrapolating the resistance of over 30 devices to zero-length (Fig. 3.4 (b)), we obtained a contact resistance of 440 Ω which is non-negligible compared to the lowest resistance in some of the nanowires and must be included in the modeling as discussed in the following section.

As discussed previously Werner et al. ascribed a conductance versus nanowire radius scaling parameter, β, to describe the relative contributions of surface versus bulk conductance in their InN nanowires. A similar analysis on our wires yields $\beta = 1.4$, in decent agreement with their result ($\beta = 1.6$). However, as acknowledged in their paper, this method of ascribing a single β value to multiple nanowires with a range of r_{nw} is dubious because for increasing nanowire radii, the relative contribution to current flow from the core with respect to the surface increases, and thus β is itself a function of r_{nw}. This shortcoming highlights the need for single nanowire analyses, where band bending and electron concentration can be extracted for one wire without being convoluted by bulk averaging and radius varying effects. Thus, we performed transconductance measurements using an electrolyte gate on our nanowires.

3.2.3 Electrolyte Gating and Simulations

A schematic of the electrolyte gating setup is shown in Fig. 3.5 (a). A small source-drain voltage (V_{SD}) was applied across the nanowire to monitor the current while a third, gate electrode was used to modulate the potential of the polymer electrolyte relative to source-drain. The electrolyte was $KClO_4^-$ in 1000 MW polyethylene oxide (PEO) with a [K]:[O] ratio of 100:117. When a positive (negative) voltage (V_G) is applied to the gate electrode, cations (anions) in the electrolyte migrate to the nanowire surface and induce

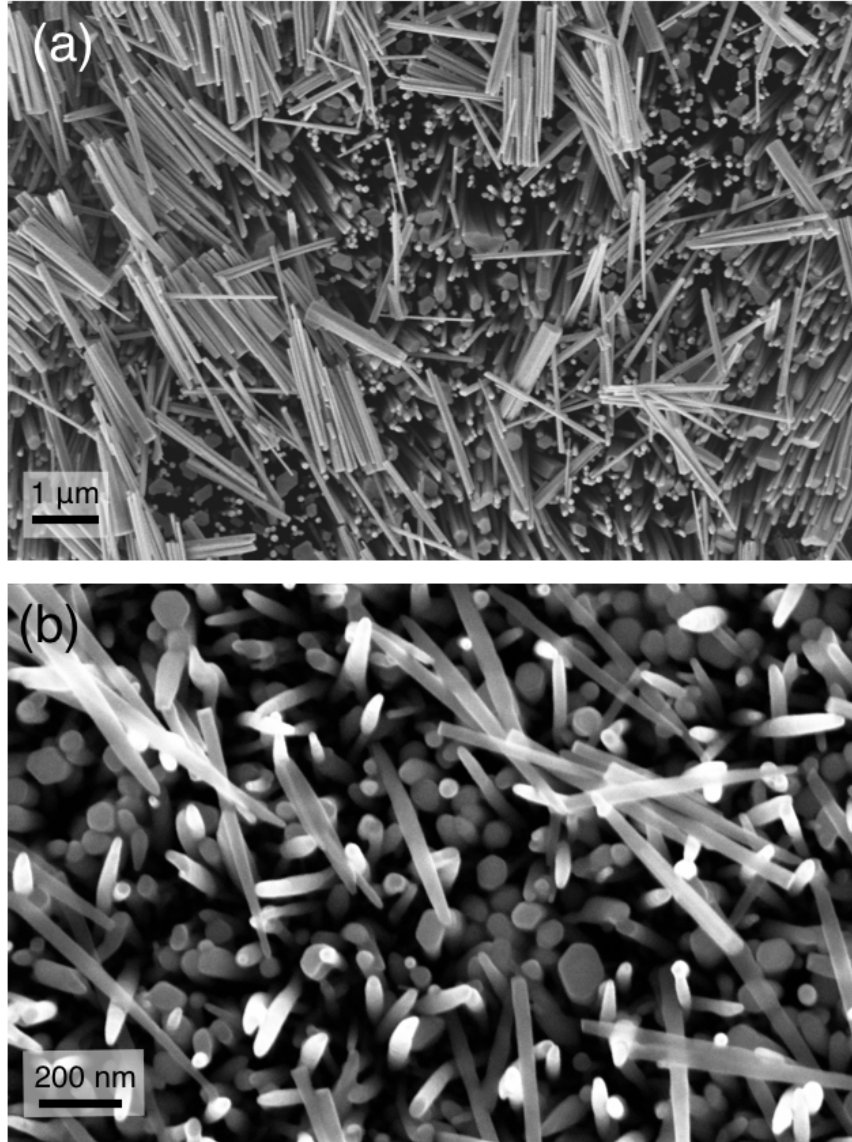

Figure 3.2. Top-down SEM image of as-grown InN nanowires from two different growth runs. (a) InN nanowires with a $50-70$ nm AlN buffer layer between the InN nanowires and Si substrate. These wires were used for the work in Chapter 4. (b) InN nanowires with no buffer layer; used in this work.

negative (positive) charges inside the nanowire channel. At sufficiently low gate voltages, this process happens without appreciable exchange of charge (leakage current) between the ions in the electrolyte and the semiconductor nanowire. In this way, the electrolyte gate is electrostatically analogous to a solid surround gate with a gate dielectric thickness equal to the solvation shell of the ions in the electrolyte (≈ 1 nm) [46]. A schematic of an ionic layer at the surface of a nanowire and the equivalent surround-gate model used for simulations is shown in Fig. 3.5 (b) and (c).

Figure 3.6 shows typical $I(V_G)$ curves of our InN nanowires. A small source drain voltage

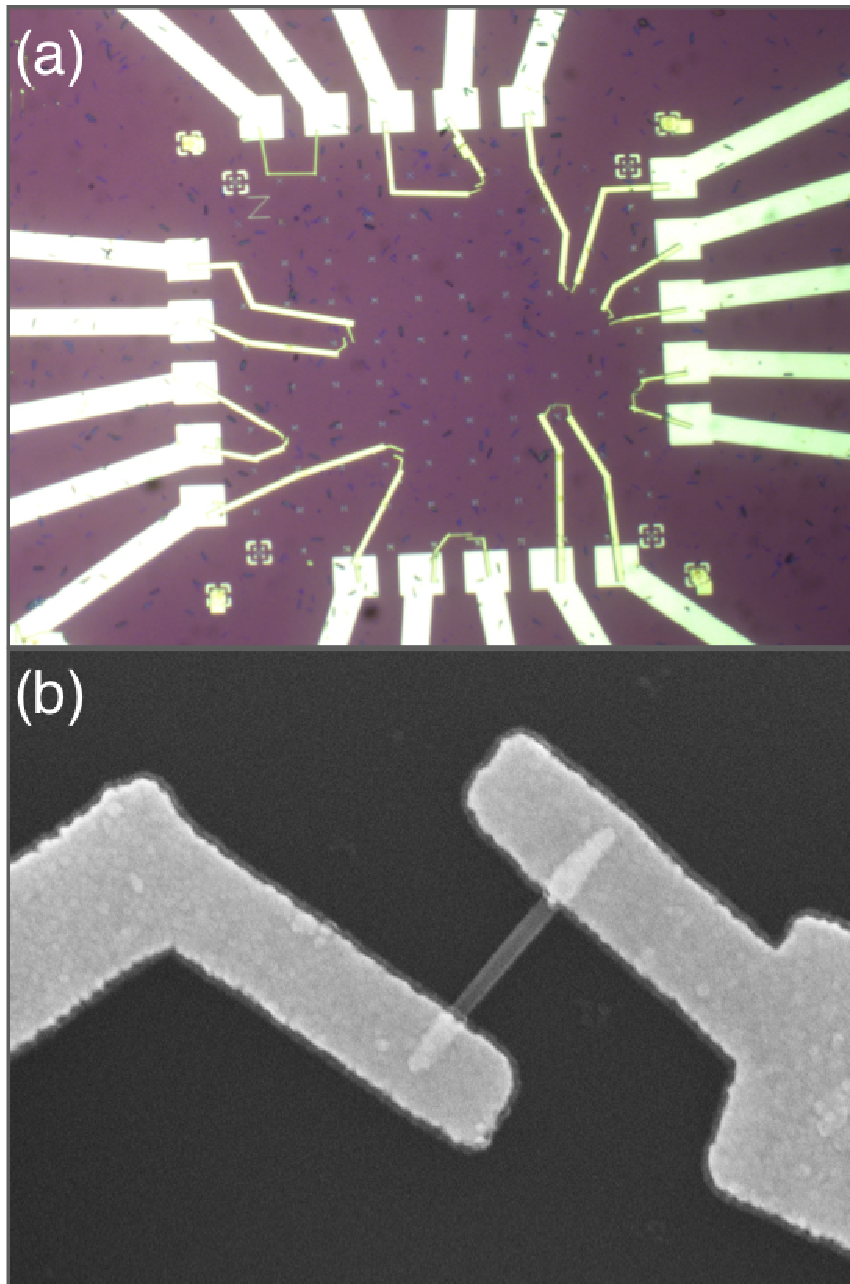

Figure 3.3. (a) Optical image of electron beam lithography pattern used to make electrical contact to nanowires. Each of the 20 squares has 8 μm sides. (b) SEM image of an InN nanowire contacted with Ti/Au contacts. Nanowire diameter is 58 nm.

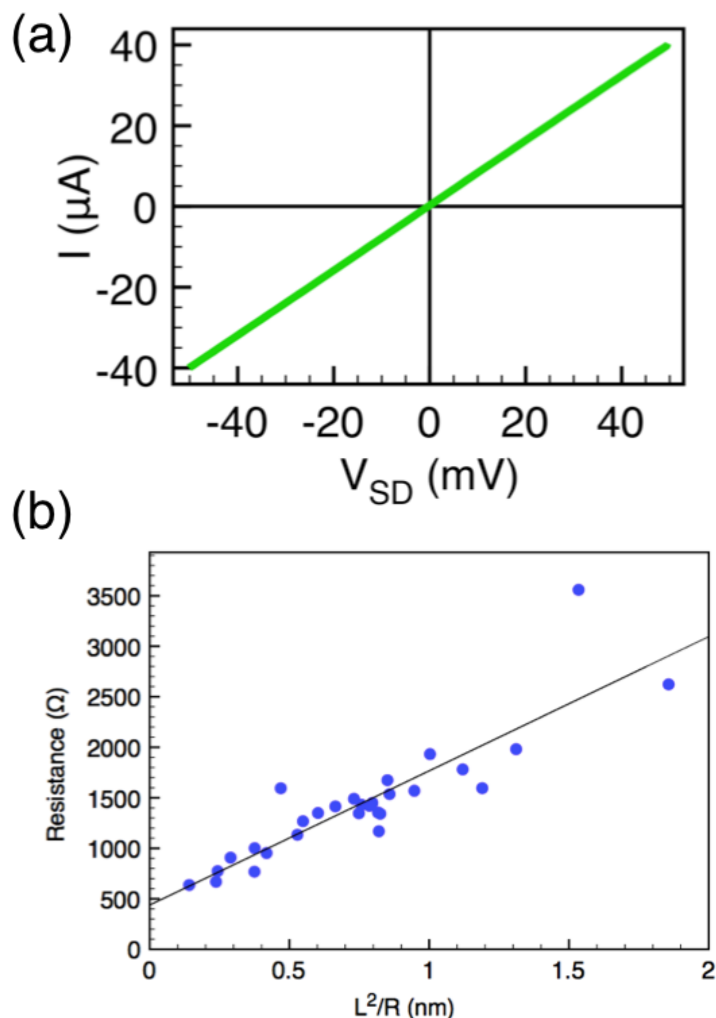

Figure 3.4. (a) Typical $I(V_{sd})$ behavior of InN nanowires measured in this study. (b) Resistance versus R^2/L where R is the radius and L is the length of the nanowire showing a zero length resistance of $\sim 440\ \Omega$

was applied across the nanowire (20 mV) and the gate voltage was first scanned from 0 V to -1.5 V, then scanned in reverse to +1 V before returning to 0 V. Note that the hysteresis of the curve in Fig. 3.6 is minimal. This was only achieved by slowing the scan rate down to 4 mV/s. At faster scan rates the $I(V_G)$ curves had heavy hysteresis (the reverse scan current was lower than the forward scan) and we were not able to deplete the nanowire as completely. This highlights a well-known property of polymer electrolyte gating, slow ion diffusivity, which has been shown to be a function of the ambient environment and temperature [47]; measurements in this chapter were done in air at room temperature. It should also be noted that even at slow scan rates, about half of the nanowires tested still showed some hysteresis between forward and reverse scan directions ($\approx$ 1 - 4 μA at 0 V_G), though the hysteresis was smaller and the shape of the curve well-behaved (i.e., a similar slope and curvature in both scan directions) compared to faster scan rates. It is possible that there is an energy barrier to desorption of the anions from the surface of the semiconductor, which prevents

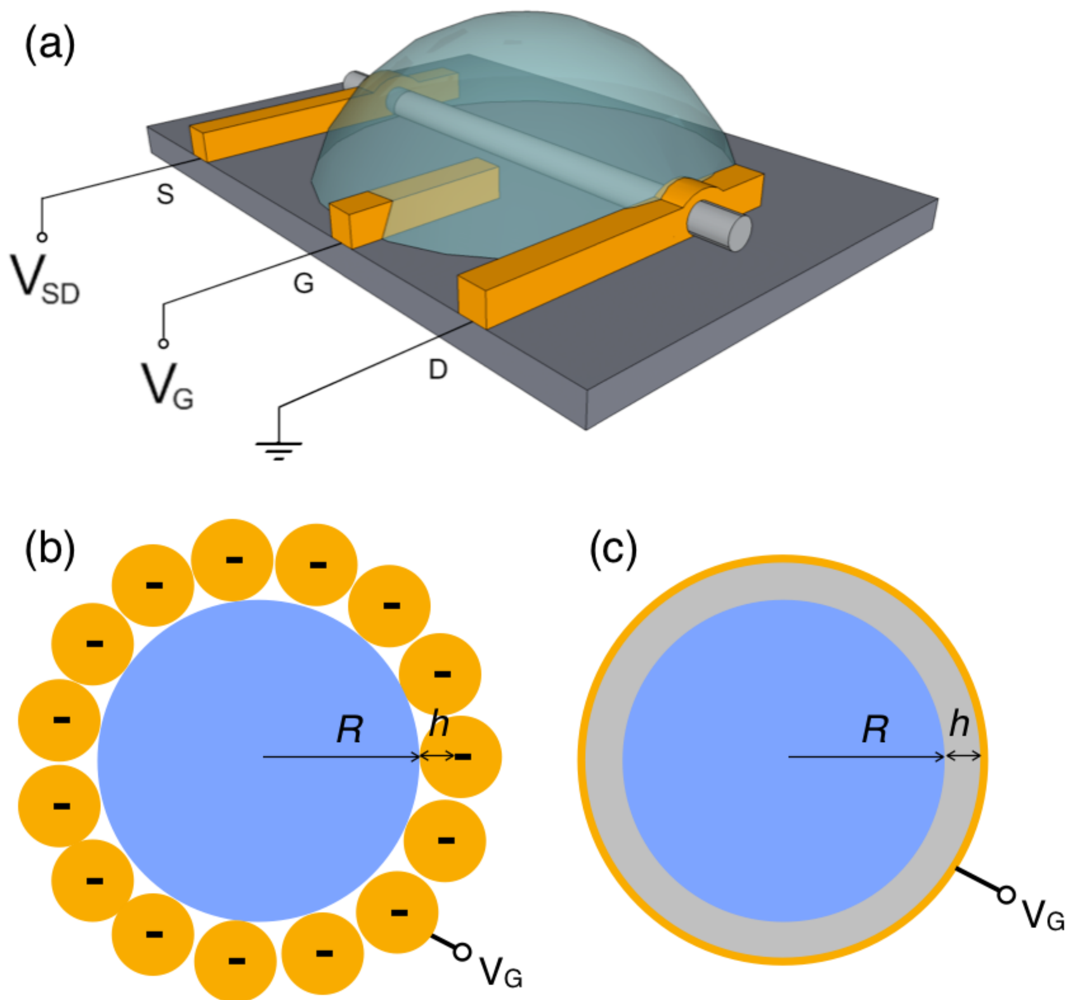

Figure 3.5. (a) A drawing of the electrolyte gating setup. The semi-transparent hemisphere is the electrolyte. (b) A schematic of a Helmholtz layer of ions near the nanowire surface, where the charge on the ion (-) is separated from the surface of the semiconductor by a distance h, which is attributed to the solvation shell of the ions in the electrolyte (orange). In this case, anions are shown, which would be balanced by band bending in the nanowire that results in a net positive charge in the wire to maintain charge neutrality. (c) A schematic of the simulation geometry used in our FEM model, where the gate voltage is a boundary condition applied to the outer edge of a dielectric of thickness h.

the reverse scan from returning to the same current value as the forward scan. Slowing the scan rate beyond 4 mV/s did not have an appreciable effect on the residual hysteresis of these nanowires. In Chapter 4, however, $I(V_G)$ curves of InN nanowires taken at 50°C that consistently showed minimal hysteresis across almost all devices measured are shown. One can expect that higher temperatures will allow for ions to more easily drift through the electrolyte and overcome desorption energy barriers, resulting in reduced hysteresis.

In order to quantify the effect of Fermi level pinning and dopant concentration on the depletion characteristics of these nanowires, $I(V_G)$ curves were simulated for different ionized dopant concentrations and surface Fermi level pinning positions. Current was calculated using a standard Drude model of conductivity, $\sigma = ne\mu$, while allowing the electron concentration, n, to be a function of radial position across the nanowire. Integrating, in cylindrical coordinates, over radial position yields an equation for current as a function of gate voltage:

$$I(V_G) = \frac{2\pi V_{SD}}{L} \int_0^R rn(r, V_G)e\mu \, dr \tag{3.1}$$

where V_{SD} is the source-drain voltage, L the length of the nanowire channel, e the electron charge, and R the radius of the nanowire. The radial electron distribution is, of course, different for different V_G, making current a function of gate voltage. The contact resistance, R_C, shifts V_{SD} by an amount IR_C, which was also taken into account.

Holes do not contribute to the current, despite the possibility of inducing inversion in our intrinsically n-type InN nanowires at large negative gate voltages. This is because pinning of the Fermi-level above the conduction band at the metal-InN interface will prevent the collection of holes, a property of InN that has long been established in thin films [35, 34]. For our InN nanowires, even if we make no a priori assumptions in our model as to the existence of surface pinning that would prevent contact with holes, fitting our model to the data with and without the inclusion of holes can verify the validity of the original assumption that holes are not collected. As it turns out, the simulations do predict an inversion effect at gate voltages within our experimental scan range, but inversion was never observed in our transconductance measurements, validating this assumption.

The key to simulating $I(V_G)$ as per Eq. 3.1 is calculating $n(r, V_G)$, which was done by solving the Poisson equation in three dimensions using finite-element modeling software (COMSOL Multiphysics) for a surround-gate FET geometry as described in Chapter 2. The non-parabolicity [34] of the InN conduction band was also included in calculating the conduction band density of states. The relative dielectric constant of InN [34] and PEO [46] were set to 10.5 and 10, respectively, and the thickness of the surround-gate dielectric was set to 1 nm. The gate voltage, V_G, was applied to the outer edge of the 1 nm gate dielectric (Fig. 3.5) and was set relative to the grounded source and drain, which corresponds physically to the PEO electrolyte maintaining an equipotential with the metal gate electrode up to the last 1 nm from the semiconductor surface. Setting both source and drain to ground is a fair assumption considering V_{SD} is two orders of magnitude lower than the range of V_G used in the scans.

The initial surface E_F pinning position (E_{pin}) is the energy of E_F relative to the conduction band minimum at the surface (Fig. 3.6a inset). In these simulation, E_{pin} was adjusted

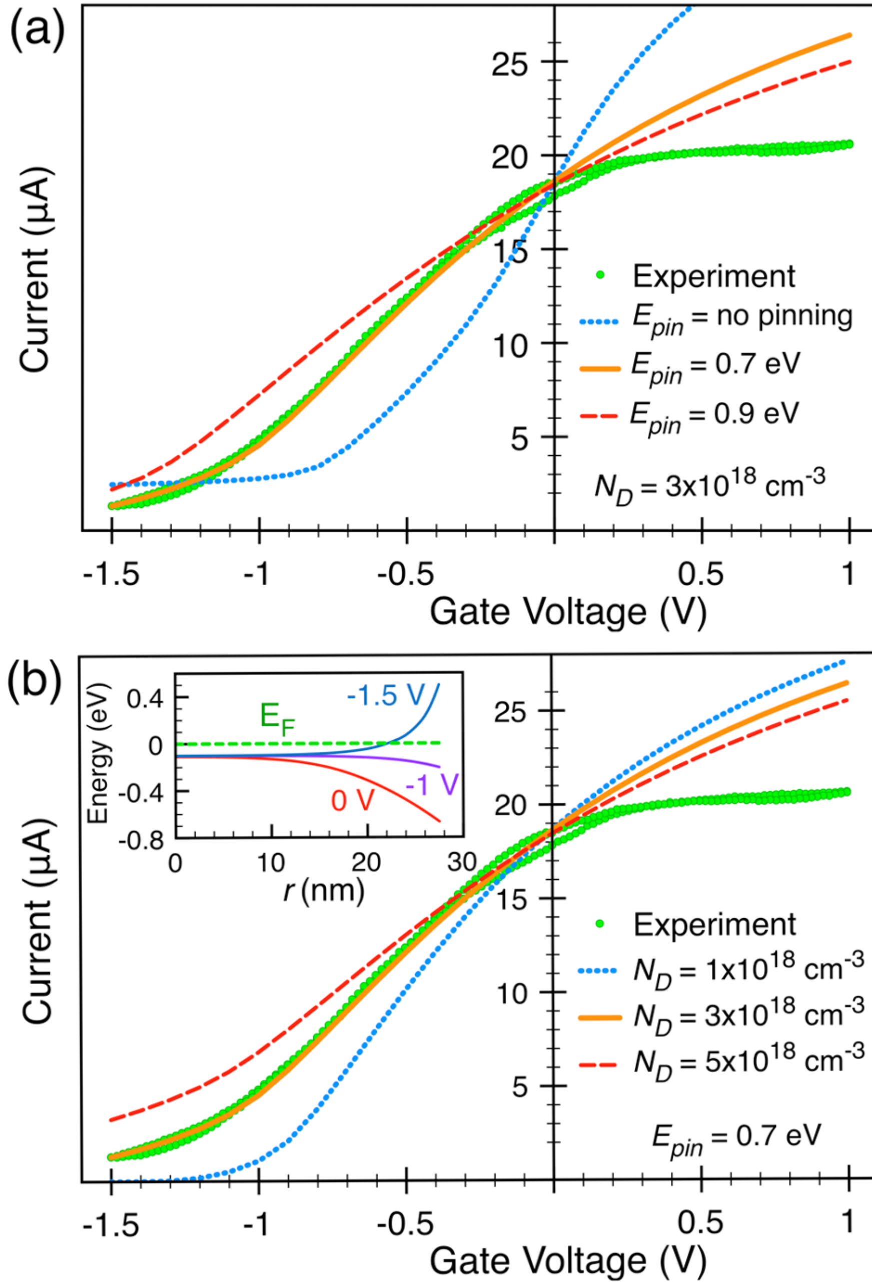

Figure 3.6. (a) Experimental $I(V_G)$ curves from an InN nanowire (27.5 nm radius) along with simulated $I(V_G)$ curves assuming an N_D concentration of 3×10^{18} cm^{-3} and E_{pin} values of no pinning ($\mu = 1600$ cm^2/Vs), 0.7 eV ($\mu = 340$ cm^2/Vs), and 0.9 eV ($\mu = 240$ cm^2/Vs). (b) Same experimental $I(V_G)$ as (a) with simulated curves assuming $E_{pin} = 0.7$ eV and N_D values of 1×10^{18} cm^{-3} ($\mu = 440$ cm^2/Vs), 3×10^{18} cm^{-3} ($\mu = 340$ cm^2/Vs), and 5×10^{18} cm^{-3} ($\mu = 280$ cm^2/Vs). Inset: conduction band bending versus radial position (r) for three V_G values (0 V, -1 V, -1.5 V) from the best-fit simulation with $N_D = 3 \times 10^{18}$ cm^{-3} and $E_{pin} = 0.7$ eV.

by varying the fixed surface charge concentration on the nanowire, which, as discussed above, is positive for InN and induces a surface accumulation of free electrons on the order of 10^{12} cm^{-2} even at zero V_G [48, 38]. For a given N_D and E_{pin}, the Poisson equation was solved for a range of V_G. The resulting electron distribution n for each V_G was then substituted into Eq. 3.1, yielding $I(V_G)$ curves for a given N_D and E_{pin}. The mobility used for each $I(V_G)$ curve was that which made the simulated curve agree with the experimental curve at $V_G = 0$. Simulated $I(V_G)$ curves for different values of N_D and E_{pin} were then compared with the experimental $I(V_G)$ curve to find the ranges of N_D and E_{pin} that best fit the experimental data.

Figure 3.6 (a) shows the effect of E_{pin} on $I(V_G)$ for a given N_D (3×10^{18} cm^{-3}). The three E_{pin} curves are representative of the range of E_{pin} values tested for each nanowire, from no surface E_F pinning to $E_{pin} = 0.9$ eV. Figure 3.6 (a) shows that the best fit is achieved with an E_{pin} in between the two extremes, at approximately $E_{pin} = 0.7$ eV. The flattening out of the simulated $I(V_G)$ curves at positive V_G is due to the inclusion of contact resistance in Eq. 3.1. However, this limiting of current by contact resistance is still insufficient to fit the experimental curve at positive V_G. This current saturation is due to a reduction in effective electron mobility by surface roughness scattering at high levels of band bending and is discussed in detail in the following chapter. Figure 3.6 (b) shows the effect of varying N_D on $I(V_G)$ with E_{pin} held at 0.7 eV. We see that the fit is quite sensitive to the background donor concentration and the best fit at this particular value of E_{pin} is 3×10^{18} cm^{-3}.

Figures 3.6 (a) and (b) suggest that we could also obtain good fits to the experimental data with other combinations of N_D and E_{pin}. We tested this by varying the N_D from 5×10^{17} cm^{-3} to 1×10^{19} cm^{-3}, and for each N_D finding the E_{pin} that resulted in the best fit, if at all possible. As expected, at the extreme values of both N_D and E_{pin}, no combination of the two parameters reasonably fit the experimental data, but there was a range of values for the two parameters that yielded equally good fits to the experimental data. For example, Figs. 3.7 show attempted fits with E_{pin} values of 0 V and 0.8 V, respectively. It is clear that regardless of the choice of N_D, those two pinning levels cannot result in a simulated $I(V_G)$ curve that fits the data well.

This result highlights the difference between a flat electron concentration originating from ionized dopants and a non-uniform electron distribution originating from surface state induced band bending; these two situations have different depletion characteristics from the perspective of an FET measurement. Since there is a unique mobility associated with each simulated curve, we can also extract a range of values for electron mobility from this fitting technique.

This analysis was performed on three nanowires from the same growth and device chip with radii of ≈ 26 nm and resulted in E_{pin} values of (0.6 - 0.7 eV), N_D values of (2×10^{18} cm^{-3} $- 4 \times 10^{18}$ cm^{-3}), and mobilities of ($400 - 550$ cm^2/Vs). We note that the E_{pin} range determined for the nanowires is slightly lower than is commonly reported for InN thin films (0.9 eV) [34]. It has been suggested that non-polar planes of InN could display E_F pinning at lower energies with respect to the conduction band minimum than the polar c-plane [49]. However, we also note that this discrepancy can be attributed to the limited accuracy of the

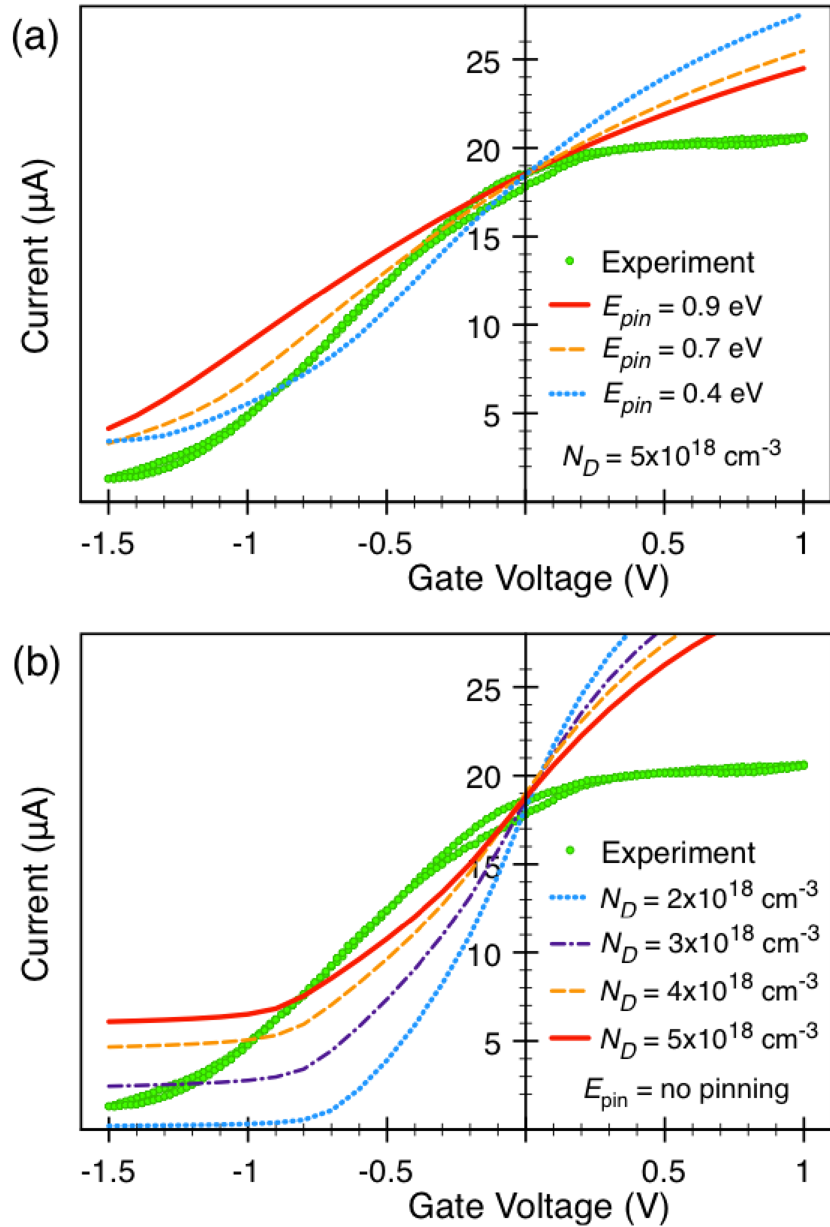

Figure 3.7. (a) Same experimental $I(V_G)$ curve as Fig. 3.6 with simulated curves assuming $N_D = 5 \times 10^{18}$ cm^{-3} and different E_{pin} values ranging from 0.4 to 0.9 eV. Clearly this value of N_D cannot fit the experimental data regardless of the E_{pin} value chosen. (b) Same experimental $I(V_G)$ curve, but with simulated curves using no pinning (flat bands at $V_G = 0$) and a range of N_D showing that simulated $I(V_G)$ curves from a wire with no pinning cannot fit the experimental data regardless of N_D.

material parameters used in the simulations, most notably the relative dielectric constants of the electrolyte and semiconductor and the thickness of the dielectric.

3.2.4 Mobility Comparison with InN Thin Films

The obtained mobilities fall within a much narrower range than previous reports on InN nanowires [50, 45]. We compare the mobility values of these three nanowires with Hall mobilities of InN thin films [51, 52] in Fig. 3.8. The nanowire mobilities agree with mobilities for InN thin films with similar N_D, with slightly lower values due possibly to the small diameter of nanowires (Fig. 3.8 inset). This agreement suggests that electron mobility in InN nanowires is also limited by scattering from charged point defects, similar to InN thin films [51]. The analysis in the next chapter shows that this is indeed the case.

Lastly, we note that calculating a mobility from the data in Fig. 3.6 through the conventional method [45] of measuring the slope of the $I(V_G)$ curve and using an analytical expression for a surround gate capacitance (Eq. 2.2), we obtain a mobility of 195 cm^2/Vs, which is more than a factor of two lower than the mobility calculated from our numerical modeling (550 cm^2/Vs). This difference arises from the erroneous estimate of the total gate-channel capacitance with an analytical equation, which completely ignores the contribution to capacitance from band bending inside the semiconductor nanowire [53]. More importantly, the free electron concentration (between 1 and 5×10^{19} cm^{-3}, determined at zero V_G using either of the above mobilities) originates from both ionized donors (N_D) and E_{pin}-induced band bending. If the effect of the surface E_F pinning is ignored, all electrons would be attributed to N_D, and N_D would be severely over-estimated as shown in Fig. 3.8. This analysis highlights the importance of band bending effects and surface E_F pinning in considering the electronic properties of semiconductor nanowires and the performance of nanowire devices.

In summary, we performed field-effect transistor measurements on InN nanowires using a polymer electrolyte gate, and taking this system as an example, provided a strategy for quantitative estimate of the surface Fermi level pinning position in the nanowires through numerical electrostatic modeling. By varying N_D and E_{pin} and generating simulated $I(V_G)$ curves, we conclusively showed that one can quantitatively determine the N_D and E_{pin} range that fits an experimental $I(V_G)$ curve. This result highlights how the ionized dopant concentration and Fermi-level pinning from surface states effect the depletion characteristics of a nanowire in different and *distinguishable* ways and how one can therefore quantitatively extract the Fermi level pinning position in nanowires from FET measurements. We also showed improved estimation of the doping level and electron mobility that result from taking into account the band bending in these nanowires. This analysis is of general importance as it can be applied to understanding electrostatic effects of the surface on the electronic properties of other material systems engineered with nanomaterial dimensions.

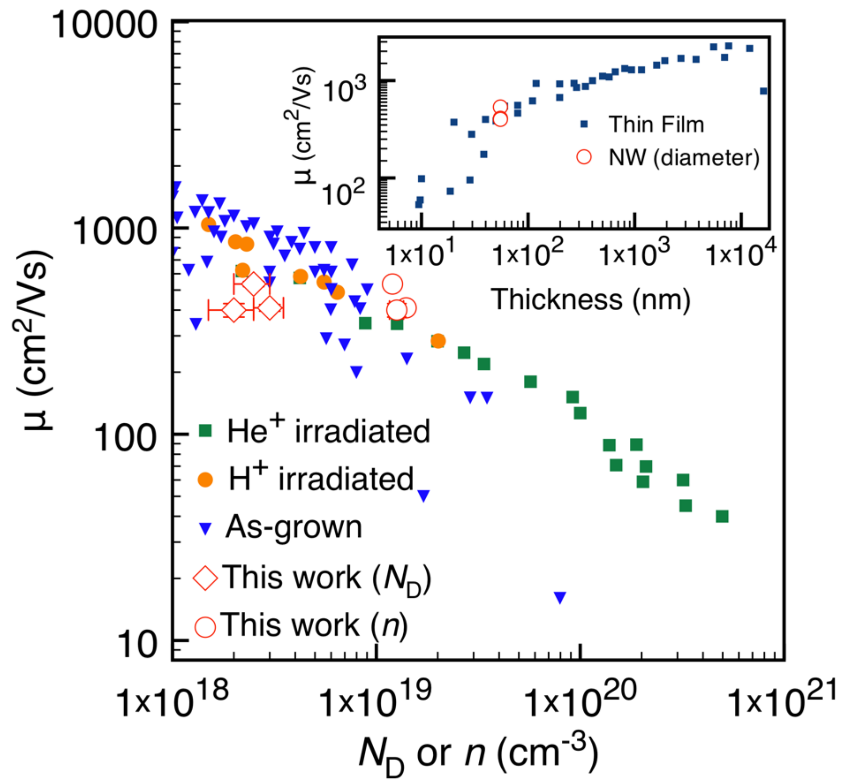

Figure 3.8. Mobility vs. electron or donor concentration of InN thin films from Ref. [21] plotted with mobilities of three InN nanowires of radii 26 1.5 nm studied in this work. Inset: Mobility vs. thickness of InN thin films from Ref. [22] plotted with mobility vs. diameter of these three nanowires.

Chapter 4

Universal Mobility Analysis in InN Nanowires

4.1 Background

The last two chapters have dealt with improving estimations of carrier mobility in semiconductor nanowires by improving calculations of nanowire-gate capacitance as well as accounting for surface Fermi level pinning in nanowires. The scattering mechanisms that are responsible for limiting carrier mobility, however, have yet to be discussed. A comprehensive understanding of scattering mechanisms is essential in realizing next-generation nanowire-based device applications because it allows for the systematic engineering of nanowire electronic properties by adjusting nanowire growth, processing, and device fabrication parameters.

Understanding which scattering mechanisms dominate in semiconductors has been studied extensively for decades, but is of renewed interest in nanowires, due to the increased impact of surface roughness scattering on the overall carrier mobility. For temperature ranges where shallow dopants are still ionized, the three most common scattering mechanisms for electrons and holes in semiconductors are coulombic scattering, phonon scattering, and surface roughness scattering. The relationship between mobilities limited by these different scattering mechanisms to the overall carrier mobility (μ) in a semiconductor is described by Matthiesen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{4.1}$$

where μ_c is the coulombic scattering limited mobility (from ionized impurities as well as trapped charge at nearby oxides and interfaces), μ_{ph} is the phonon scattering limited mobility

(which can be further separated into different phonon modes if needed), and μ_{sr} is the surface roughness limited mobility.

The issue of surface roughness scattering in nanowires has been explored experimentally by several groups [54, 55, 56], who noticed a decrease in field-effect mobility with decreasing nanowire diameter, which they attributed to an increase in surface roughness scattering for smaller nanowire radii. In particular Ford et al. [54] did a series of temperature dependent transport measurements to show that surface roughness scattering was indeed the limiting scattering mechanism. These techniques, which involve observing a trend in field-effect mobility as a function of nanowire diameter do not, however, allow one to quantify the magnitudes of different scattering mechanism *at the single nanowire level*, nor do they address the effects of radial carrier distribution on dictating which scattering mechanisms are dominant.

The latter issue is especially important in nanowires due to their small size. The radial carrier density profile can be affected by a variety of growth and post-processing parameters, including doping conditions, surface treatments, and alloying. Perhaps more importantly, the carrier profile can be dramatically modified in device applications. For example, by the adsorption of chemical species in nanowire sensors, or most dramatically, by an applied electric field in an FET, as has been illustrated in Chapters 2 and 3. In all of these situations, a slight change in band bending can change whether the majority of free carriers are pushed to within a few nanometers of the surface or a depletion region of a few nanometers is shielding them from the surface. This is in contrast with many bulk and thin-film semiconductors where current can flow many nanometers or even microns from the surface, and thus changes in the surface band bending over a few nanometers have a negligible effect on the overall measured current.

This is illustrated in Fig. 4.1 where two radial conduction band profiles and corresponding electron distributions for an InN nanowire are presented. Figure 4.1 shows clearly how a reversal of band bending from surface accumulation to surface depletion can dramatically change the distribution of free carriers relative to the nanowire surface. In the context of surface roughness scattering, it should be expected that the two electrostatic situations presented in Fig. 4.1 for the *same* nanowire do not have the same carrier mobility when current is passed along the length of the wire. Therefore, assigning a given nanowire a single value of mobility irrespective of particular device parameters such as gate voltage is dubious. Similarly, when comparing different semiconductor nanowires, one cannot make universal statements about what wire diameters correspond to a transition from phonon or coulombic scattering limited mobility to surface roughness limited mobility, because as suggested in Fig. 4.1, semiconductors with different radial band profiles (but the same diameter) cannot be expected to have a similar influence on mobility from the surface. In other words, the common practice of assigning one peak field effect mobility, μ_{FE}, to a given nanowire as discussed in Chapter 1, is an incomplete description of nanowire conduction and a method for quantitatively distinguishing between different scattering mechanisms that limit mobility as a function of band bending would therefore be beneficial.

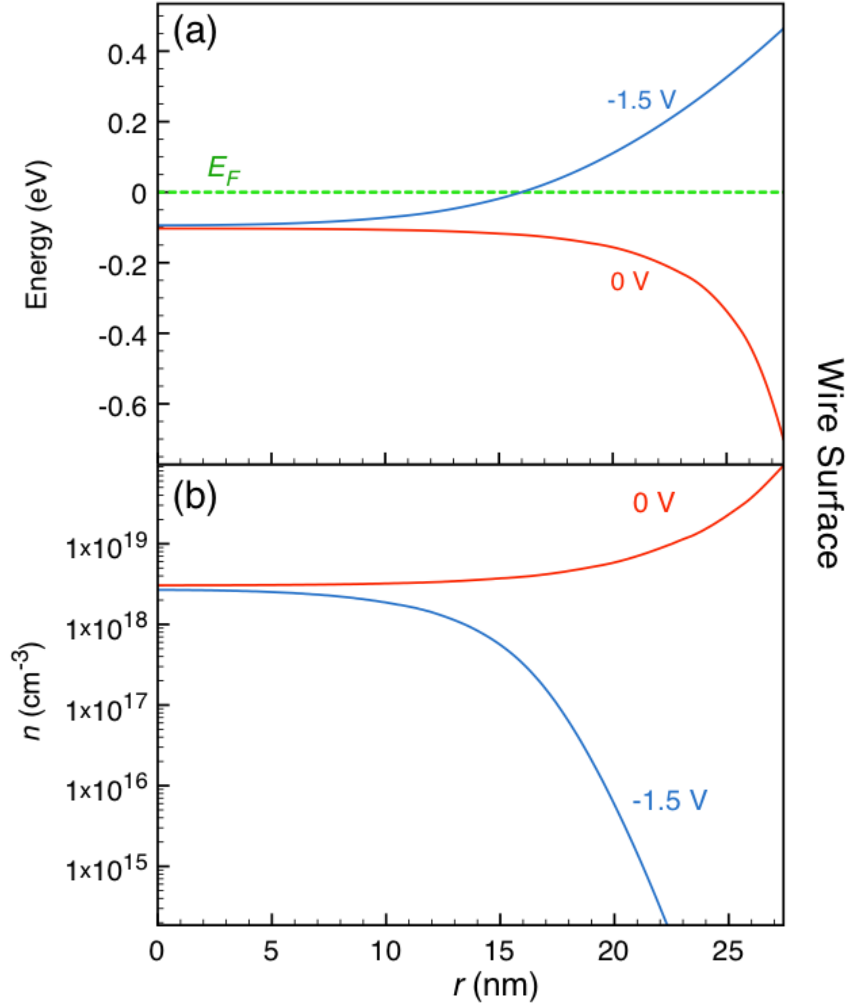

Figure 4.1. Conduction band profiles (a) and carrier distributions (b) for a surround gated InN nanowire at gate voltages of 0 V and -1.5 V. The curves were generated from the best fit simulation (orange curve) in Figure 3.6, in Chapter 3. The wire core is at $r = 0$ nm and the wire surface is at $r = 27.5$ nm.

4.2 Universal Mobility Behavior of Silicon MOSFETs

Fortunately, the issue of mobility dependence on band bending and carrier distribution in a semiconductor has been studied in detail for Si MOSFETs since the 1970s. The channel mobility is a critical device parameter that must be understood to have an adequate control of drain current. Therefore, extensive research has gone into characterizing the effect of different device properties such as channel doping and surface roughness on MOSFET carrier mobilities.

A key observation was made by Sabnis and Clemens in 1979 [57], who noticed that when the effective mobility of the channel is plotted versus the average (or "effective") electric field (E_{eff}) in the inversion layer, the mobility curves of samples with different background dopant concentrations merge onto a single curve, referred to as the universal mobility curve. The E_{eff} in the universal mobility curve is the effective field in the band bent region of the channel (inversion region) due to the applied gate voltage. Further studies by multiple groups not only confirmed this result but also found that three distinct regimes were present in this universal mobility curve (Fig. 4.2): an upward slope at low effective fields ascribed to coulombic scattering limited mobility, a shallow downward slope at slightly higher effective fields ascribed to phonon scattering limited mobility, and a steeper downward slope at high effective fields ascribed to surface roughness scattering [58].

From Fig. 4.2 (a), we see that the universality of this curve is broken at the lowest fields for each doping level[1]. This is to be expected, since higher dopant concentrations should lead to a lower mobility in E_{eff} regimes where coulombic scattering is dominant. In other words, the "universality" of the curve refers to how regardless of different doping concentrations in different MOSFETS, at higher fields, all curves merge into one. In fact, the breaking off from the universal curve at low fields for different dopant concentrations is useful in that it confirms that the upward sloped, low-field region is indeed due to coulombic scattering. Similarly, the lack of a phonon scattering limited regime for the mobility curve at 77K confirms that the slight downward slope ($\propto E_{eff}^{-0.3}$) at midrange effective fields is due to phonon scattering.

Since the nanowire devices studied in this work are gated in accumulation-mode, not inversion-mode, it is instructive to show the differences in the universal mobility behavior of accumulation-mode Si MOSFETs relative to inversion-mode. In accumulation mode MOSFETs, the carriers in the channel are of the same type as the background doping. From an electrostatics perspective, the major difference between accumulation and inversion-mode MOSFET channels is the degree of band bending (and thus electric field) required to reach the ON-state. Figure 4.3 shows electron mobility data from accumulation mode MOSFETs from McKeon et al. [59] plotted with the 300 K inversion-mode data of Takagi et al. from Fig. 4.2. The accumulation and inversion mode data agree almost exactly for electric fields of 10^5 V/cm and greater, showing that at sufficiently high fields, phonon and surface roughness

[1]Note that for n-channel inversion-mode FETs such as in Fig. 4.2 (a), the background doping concentration is of acceptors and higher doping leads to a higher minimum effective field in the channel required to induce inversion, so the data for lower dopant concentrations spans a wider range of effective fields.

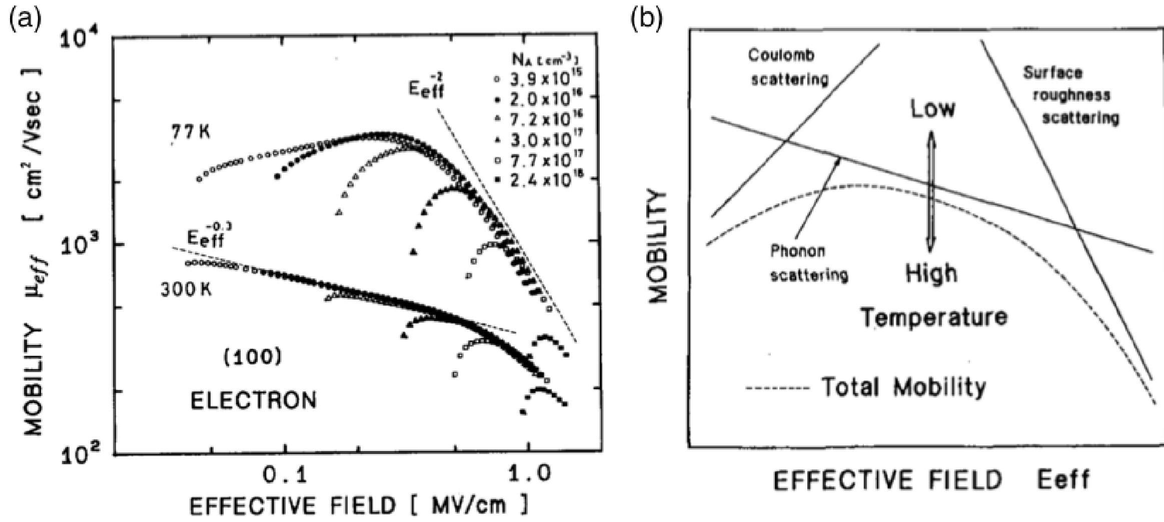

Figure 4.2. (a) Universal mobility behavior of n-channel inversion-mode MOSFETs at 300K and 77K from Ref. [58]. (b) Schematic of the shape of a mobility vs. effective field plot showing the dominant scattering processes for each of the three slope (Ref. [58]).

scattering dictate the mobility of carriers in a consistent fashion, regardless of the background doping type.

At lower fields ($< 10^5$ V/cm), however, the mobility curves for the accumulation-mode MOSFETs flatten out instead of decreasing with lower field. This is a result of the screening of ionized dopants by free carriers. That is, in inversion layers, the free carrier-to-ionized dopant ratio is very small at the onset of inversion and grows as the gate voltage is increased. As the free carrier concentration increases, so does the screening of ionized dopants by the carriers, and consequently the coulombic limited mobility increases. In contrast, the free carrier concentration in accumulation-mode channels is already sufficiently high even at zero gate voltage to screen the ionized dopants and further accumulation of those majority carriers has a negligible effect on ionized dopant screening, so mobility remains roughly constant until the field is high enough for phonon and surface roughness scattering to limit the mobility. For the highest dopant concentrations, McKeon et al. reported that the low-field mobilities approach the bulk mobilities of Si for each dopant concentrations [59].

4.3 Electrical Properties of Irradiated InN Nanowires

In this section, using InN nanowires as an example system, we use universal mobility analysis to separate the effects of surface roughness and coulombic scattering on carrier mobility by analyzing the dependence of mobility on the average electric field in the nanowires. We show that this universal mobility analysis can be used to distinguish between different carrier scattering mechanisms as a function of radial band bending inside a nanowire. For

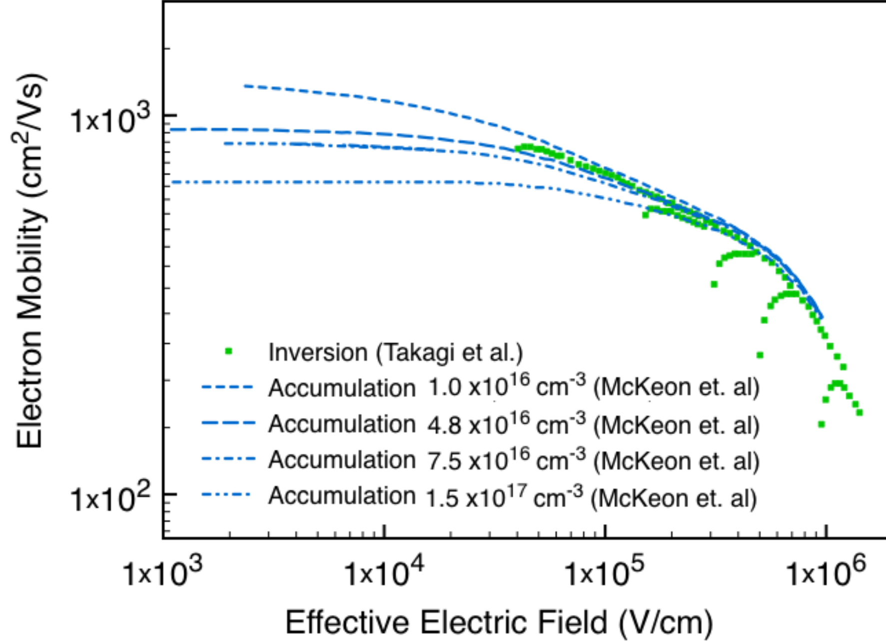

Figure 4.3. (a) Universal mobility behavior of accumulation mode n-channel MOSFETs from Ref. [59] compared with 300 K inversion mode curves from Ref. [58] (Fig. 4.2 (a)).

the nanowire diameters studied (30 - 50 nm), our results indicate that the dominant carrier scattering mechanism is dependent on band bending in the wire and that surface roughness scattering limits free carrier mobility at high surface fields, similar to Si MOSFETs. The presented results serve to emphasize the importance of considering surface states, Fermi level pinning, and band bending when quantifying the electrical properties of semiconductor nanowires, which have a high surface area to volume ratio. Overall, universal mobility analysis is shown to be a useful platform for quantifying individual mobility components in semiconductor nanowires.

Molecular beam epitaxy grown InN nanowires, described in Chapter 3, were used. The strong intrinsic downward band bending at the surface of these natively n-type nanowires makes them convenient for universal mobility analysis because large internal electric fields are experimentally accessible with only moderate gate voltages. Electrolyte gating, as described in detail in Chapter 3, was also used. Unlike in Chapter 3, in these studies, $I(V_G)$ measurements were performed at 50 ^{o}C, which is above the melting point of the PEG electrolyte. Keeping the electrolyte in a liquid phase during the gating measurements minimized hysteresis in the $I(V_G)$ curves for the vast majority of wires and allowed for faster gate voltage scan speeds, unlike the room temperature measurements in Chapter 3, where very slow scan speeds were necessary and only a few nanowires showed minimal $I(V_G)$ hysteresis.

The dopant concentration of the nanowires was varied by irradiation with 2 MeV alpha particles, which multiple reports [60, 51, 61] have shown increases the point defect concentration in InN thin films. These charged point defects act as donors in InN. Thus, high energy ion irradiation can be used to increase the donor concentration in InN. In this work,

multiple irradiation steps were done on a single device chip allowing us to measure the *same* nanowires through a range of dopant concentrations.

Figure 4.4 shows $I(V_G)$ curves (at 50 ^{o}C) of a typical InN nanowire as a function of irradiation dose. A drop of the PEG electrolyte was only applied for a short time after each irradiation to measure the $I(V_G)$ behavior and then immediately dissolved and rinsed in deionized water ($\sim$1 min for the electrolyte to dissolve), so each irradiation step was performed on the device chip with no PEG drop covering the wires. To ensure the change in $I(V_G)$ comes from irradiation and not consecutive rinsing and reapplication of PEG droplets, we measured $I(V_G)$ curves from two different PEG droplets without an irradiation step in between for the fluence of 2.1×10^{14} cm^{-2}; the difference in these two curves is clearly negligible compared to the effect of irradiation. The fact that the nanowire is systematically harder to deplete with increased irradiation dose is consistent with the expectation of increased donor concentration with increasing irradiation fluence.

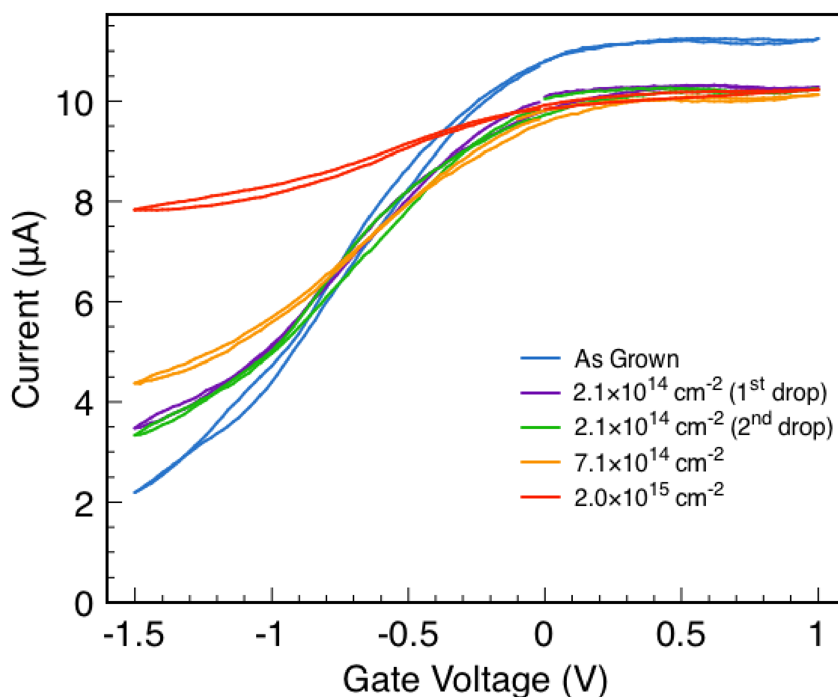

Figure 4.4. Current versus gate voltage of an x nm diameter InN nanowire for a series of alpha particle irradiation fluences. $I(V_G)$ curves are shown for two separate drops of electrolyte for the fluence of 2.1×10^{14} cm^{-2} to show the magnitude of variability in $I(V_G)$ curves from rinsing and reapplying the electrolyte.

In order to quantify the change in donor concentration with irradiation fluence, we fit the $I(V_G)$ curves from different fluences for three wires with the method described in Chapter 3 and extracted the donor concentration, N_D, and Fermi level pinning position, E_{pin}. The change in N_D with fluence for all three wires is plotted in Fig. 4.5. We see that although the as-grown nanowires start with a higher N_D than the InN film data, upon irradiation, the N_D versus fluence for our nanowires agrees very well with the InN thin films from Refs. [60, 61],

which were measured by Hall effect, where $N_D \approx n$ for most film thicknesses. The vertical error bars in Fig. 4.5 show the range of N_D that fit the experimental data. As the $I(V_G)$ flattens out for more heavily doped wires, a wider range of N_D was able to generate suitable fits the experimental data. We can see from Fig. 4.4 that for doses higher than $\approx 10^{15}$ cm^{-2}, it becomes very difficult to modulate the current even with our electrolyte gating setup. Thus, we were not able to probe fluences as high as Refs. [60, 61]. The Fermi level pinning position that best fit the experimental data for all wires and doses was 0.8 +/- 0.1 eV, in decent agreement with results in Chapter 3.

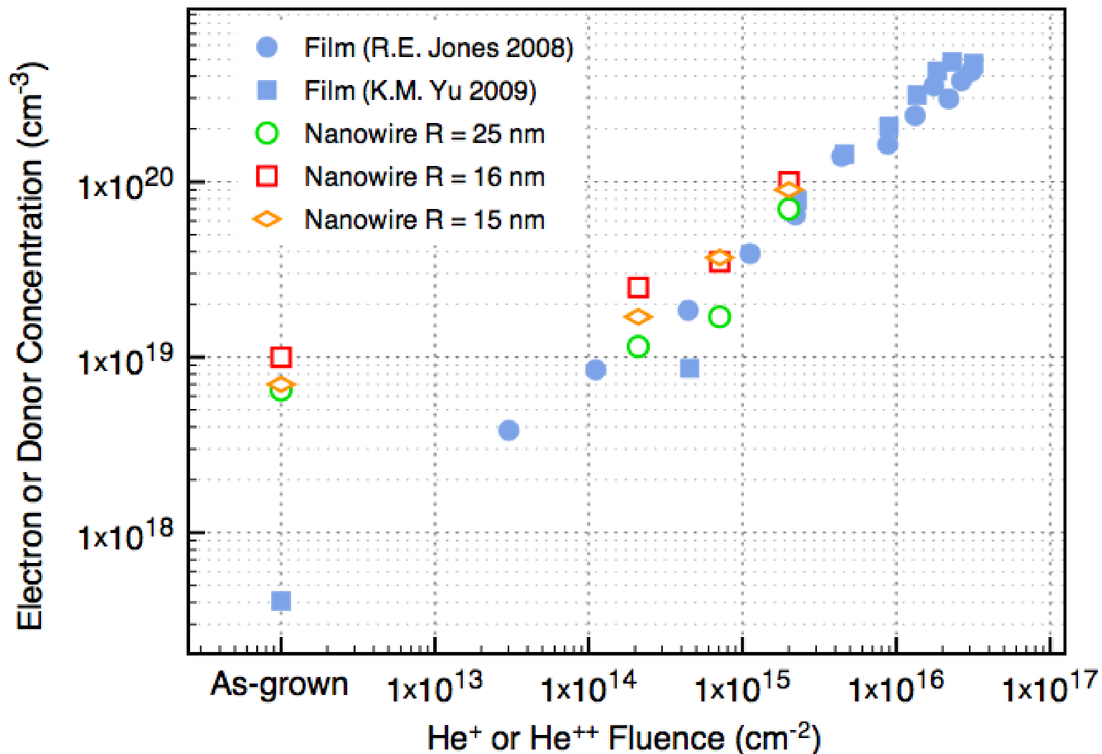

Figure 4.5. Donor concentration versus He^{++} fluence for three InN nanowires compared to electron concentration versus He^{+} fluence for InN thin films from Yu [60] and Jones [61].

Previous reports [62, 63] on 10 MeV proton irradiation of backgated ZnO nanowire and carbon nanotube (CNT) FETs attributed changes in $I(V_G)$ behavior upon irradiation to radiation-induced trapped charge in their dielectric (SiO_2) and nanowire-oxide interface. In this work, however, the excellent agreement of our N_D versus dose data with InN thin films combined with a consistent E_{pin} extracted from all three wires at all doses confirms that the change in our $I(V_G)$ characteristics is due to native defect generation and not trapped charge in the nitride or nanowire-nitride interface. If trapped charge in the silicon nitride substrate were responsible, we would have observed a change in E_{pin}, not N_D, as a function of irradiation fluence.

The discrepancy between our results and that of Refs. [62, 63] could be due to several

factors. Primarily, silicon nitride is known to be much more resistant to radiation induced changes in electrical behavior than silicon oxide [64, 65]. In addition, our gate voltage is applied through a surround-gate configuration from the electrolyte instead of via a backgate, which should prevent trapped charge in the nitride or interface from affecting the $I(V_G)$ behavior [2]. Lastly, the different ion mass (protons vs. He^{++}), energy (10 MeV vs. 2 MeV), fluence ($10^{11} - 10^{12}\text{cm}^{-2}$ vs. $10^{14} - 10^{15}\text{cm}^{-2}$), and the significant difference in conductivity between ZnO and InN nanowires may have also contributed to this discrepancy.

4.4 Universal Mobility Analysis of InN Nanowires

After quantifying the various electrostatic variables in the nanowire (N_D, E_{pin}, $\phi(r)$, $n(r)$) via finite element techniques as described in the previous section, the effective mobility and effective field were calculated as follows. The effective field is defined as the weighted average electric field experienced by accumulated electrons:

$$E_{eff}(V_G) = \frac{\int_0^R n(r, V_G) E(r)\, dr}{\int_0^R n(r, V_G)\, dr} \tag{4.2}$$

where $E(r)$ is the radial component of the electric field in the nanowire and R is the nanowire radius. Since, by definition, the electric field is non-zero only in the accumulation region, μ_{eff}, in this study, is defined as the effective mobility for only the *accumulated* electrons, that is, the electron concentration in excess of the background dopants:

$$I_{SD}(V_G) - I_0 = (n(V_G) - n_0)\frac{\pi R^2}{L} q \mu_{eff} V_{SD} \tag{4.3}$$

where $n_0 = N_D$ is the electron concentration from dopants, which explicitly excludes electrons induced by band bending from either surface states (intrinsic band bending) or an applied gate voltage, and can therefore be called the "flatband" electron concentration. Likewise, I_0 is the flatband current ($I_0 = I_{SD}(V_G = V_{FB})$). Since the electron concentration is a function of voltage, so is the effective mobility:

$$\mu_{eff}(V_G) = \frac{(I_{SD} - I_0)L}{(n(V_G) - n_0)\pi R^2 q V_{SD}}. \tag{4.4}$$

In all cases, V_{SD} was modified to account for contact resistance just as in Chapter 3. The relationship between n_r, n_0, and n_{acc} is represented graphically in Fig. 4.6. Note that in contrast to the definition of μ_{eff} in Chapter 1 (Eq. 1.4), the capacitance is not explicitly defined in Eq. 4.4. This is because our finite element simulations of the nanowire output $n(V_G)$ directly.

[2]Although the electrolyte does not penetrate completely under the wire, any "ungated" portion at the wire-substrate interface is likely negligible compared to total wire diameter, judging by our ability completely or near-completely deplete the InN nanowires with the electrolyte gate (Figs 3.6 and 4.4).

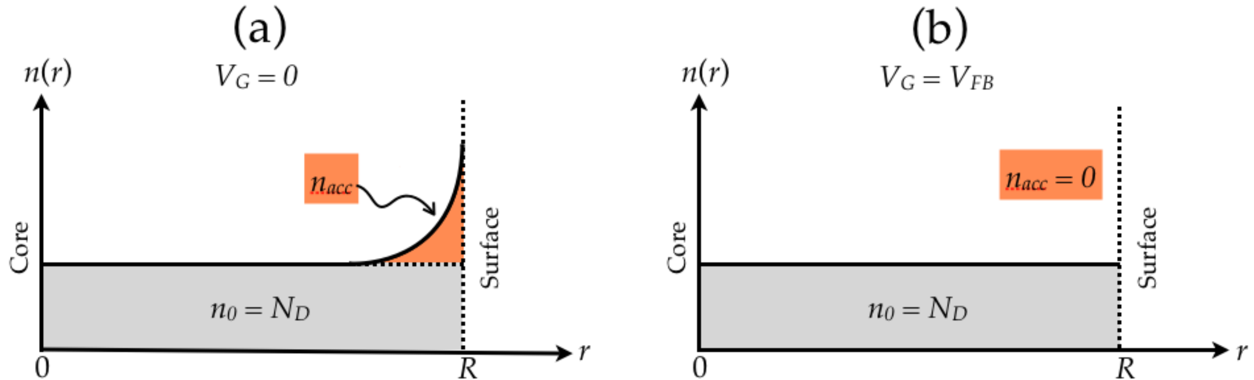

Figure 4.6. Schematic of the radial electron distribution for an InN nanowire at (a) $V_G = 0$, and (b) $V_G = V_{FB}$. n_0 and n_{acc} are highlighted in different colors. The flatband voltage, V_{FB} is defined as the condition that results in (b).

Figure 4.7 shows μ_{eff} as a function of E_{eff} for a range of He^{++} fluences. Similar to the accumulation-mode MOSFET curves in Fig. 4.3, we see a clear distinction between a flat, coulombic scattering limited regime at low E_{eff} and a surface roughness scattering limited regime at high E_{eff}. Phonon scattering limited mobility is not a limiting factor in our InN nanowires due to their heavy intrinsic doping as explained below. To gauge what scattering processes limit nanowire mobility under no applied field, the electric fields that correspond to zero gate voltage $V_G = 0$ V are marked for each mobility curve in Fig. 4.7. We see that μ_{eff} at $V_G = 0$ V is in a transition regime where both surface roughness and coulombic scattering likely contribute to limiting electron mobility. It is worth emphasizing that such intrinsically high fields in our nanowires are due to the unique surface pinning properties of InN. Clearly, when a negative gate voltage is applied and the bands flatten, μ_c is the only limiting factor.

In most semiconductors, the surface Fermi level is pinned near the middle of the bandgap, which usually (depending on doping) results in a slight surface depletion (of either electrons or holes). In these low-field surface accumulation or depletion conditions, it is clear from Fig. 4.7 that μ_c will dominate over μ_{sr} for nanowires with dopant concentrations $> 10^{18}\text{cm}^{-3}$ and diameters ($\sim 30 - 50$ nm) comparable to those in this work. For more lightly doped samples such as those presented in Fig. 4.3, the effective carrier mobility of carriers at low gate fields will be limited by μ_{ph} rather than μ_c. Thus, *a priori* assumptions about conduction in semiconductor nanowires being limited by surface roughness should be questioned for wire diameters on the order of tens of nanometers. For smaller diameter nanowires, where quantum confinement begins to significantly effect the density of states and the wavefunction of the electrons, a strictly classical approach as presented here does not apply and quantum mechanical considerations are necessary. Estimates of wire diameters where quantum effects will begin to dominate are listed in Chapter 1. For InN, the characteristic wire width where the first two quantum confinement-induced subbands are separated by k_BT at room temperature is 20 nm. The smallest wire studied in this chapter has a diameter of ≈ 30 nm, which is approaching this characteristic width. We expect that this will result in a slight quantitative shift in the results presented, but the qualitative trends should remain the same.

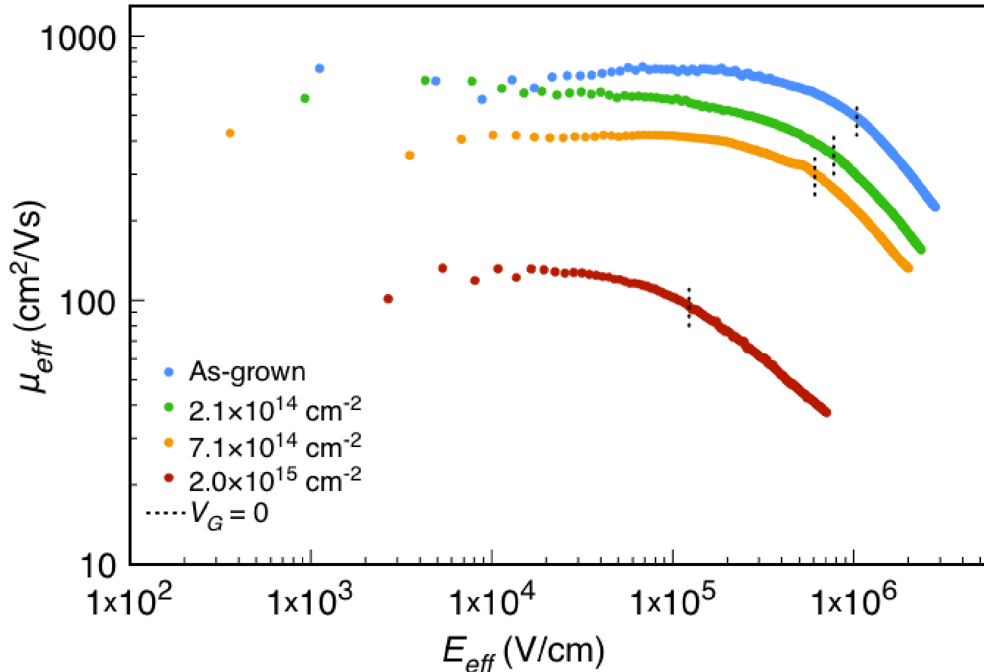

Figure 4.7. Effective mobility as a function of effective electric field for a 50 nm diameter InN nanowire for a range of irradiation fluences from 0 to 2.0×10^{15} cm^{-2}. The electric fields that correspond to $V_G = 0$ V are marked for each wire.

It is worth emphasizing that InN has a uniquely low effective mass and is merely used as an example semiconductor to present this technique. Lastly, although transistor-specific effects, such as an increase in source-drain contact resistance with increasing V_G could also cause a decrease in transconductance at high E_{eff}, we note that a similar decrease in mobility with increased surface accumulation was observed in gated Hall effect measurements in InN thin films [48], which at the time was not fully understood. Our decrease in mobility at positive gate voltages is consistent with this result and the agreement between both experiments (Hall mobility of gated InN thin films and effective mobility of gated InN nanowires) indicates strongly that the decrease in transconductance at positive gate voltage that we observe is not due to a transistor device artifact but rather an increase in carrier scattering.

At first glance, Fig. 4.7 indicates that the mobility curves at high fields do not seem to merge onto one universal curve as expected. To verify and quantify the extent of this lack of universal mobility behavior we fit the mobility data in Fig. 4.7 with Eq. 4.1. As explained earlier, μ_c has a negligible dependence on E_{eff} for accumulation-mode FETs and is therefore a constant. Calculations of InN mobilities at room temperature have shown that for dopant concentrations above $\sim \text{mid} - 10^{18}\text{cm}^{-2}$, phonon scattering is not a limiting factor [66]. Our measurements were performed at a slightly higher temperature (50° C), but with N_D approaching 10^{19} cm^{-3} in our nanowires (Fig. 4.5), this is still a valid assumption. The surface roughness scattering limited mobility is known [58] to depend on E_{eff} as

$$\mu_{sr} = \beta E_{eff}^{-\gamma} \tag{4.5}$$

where γ is approximately 2 and the coefficient β is inversely dependent on material parameters such as effective mass and surface roughness. Coulombic scattering is, as mentioned above, independent of E_{eff}, so a constant value of μ_c was chosen for each mobility curve that, together with μ_{sr} resulted in the best fit. An example fit to the as-grown mobility curve from Fig. 4.7 is shown in Fig. 4.8. We see that an excellent fit can be obtained with just μ_c and μ_{sr}, without explicitly including μ_{ph}, consistent with the assumption that the contribution from μ_{ph} is small at these dopant concentrations and temperature, although low temperature measurements are necessary to fully quantify the influence of μ_{ph}.

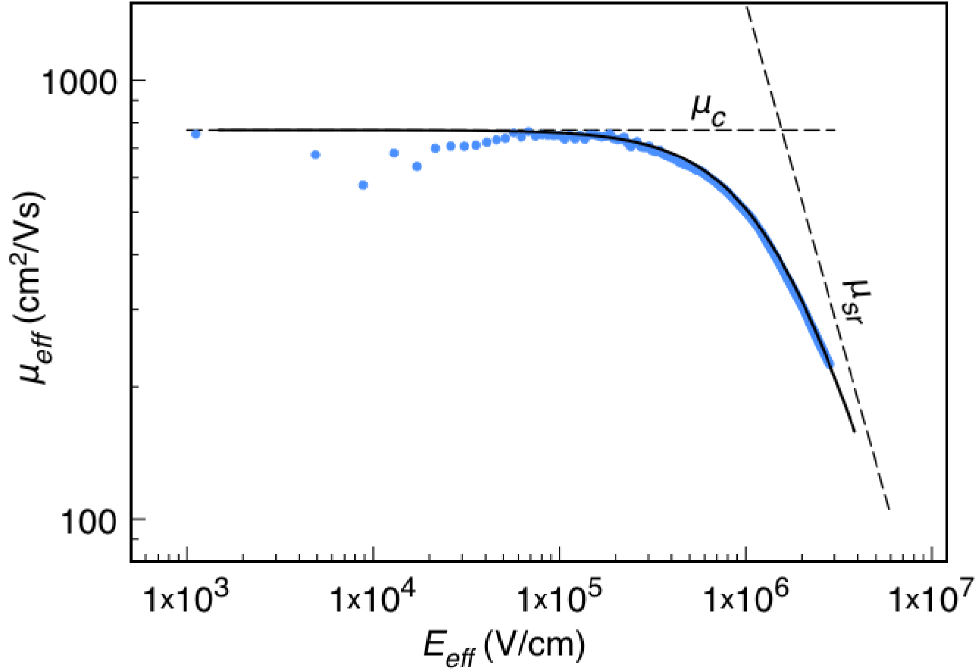

Figure 4.8. Effective mobility as a function of effective electric field for an as-grown 50 nm diameter InN nanowire along with a fit using Eq. 4.1 where μ_c is a constant and Eq. 4.5 is used for μ_{sr} with $\beta = 1.5 \times 10^{12}$ cm^3/V^{2}s and $\gamma = 1.5$.

The reduction in electron mobility due to an increase in ionized impurity scattering from high energy particle irradiation has been well characterized for InN thin films. Specifically, experimentally measured Hall mobilities of InN films as a function of electron concentration have been observed [60, 51, 61] to agree very well with theoretical calculations of mobility limited by triply charged donors, indicating that the donor-like defects created by ionized helium and proton irradiation are triply charged, not singly charged, as shown in Fig. 4.9. The calculations are based on a two-band Kane model where the conduction band dispersion was calculated using the $k \cdot p$ approximation, described further in Ref. [51]. Also shown in Fig. 4.9 is μ_c as a function of N_D for a range of irradiation fluences for three nanowires examined in this study. Because the Hall effect technique samples a large portion of the interior of a film, the Hall mobility of InN thin films is limited by coulombic scattering (at these high dopant concentrations), not surface roughness scattering, and is therefore comparable to the μ_c values of our nanowires. Similarly, the average electron concentration in thin films

measured by Hall effect is most comparable to N_D in our nanowires when the film thickness is greater than a few tens of nanometers and the "extra" electron concentration from the surface accumulation layer is negligible compared to the background donor concentration. We see that our μ_c versus N_D data agree very well with the experimental thin film data as well as the theoretically calculated triple charged donor limited mobility. This confirms that the native defects created by irradiation in our nanowires are the same as those in InN thin films.

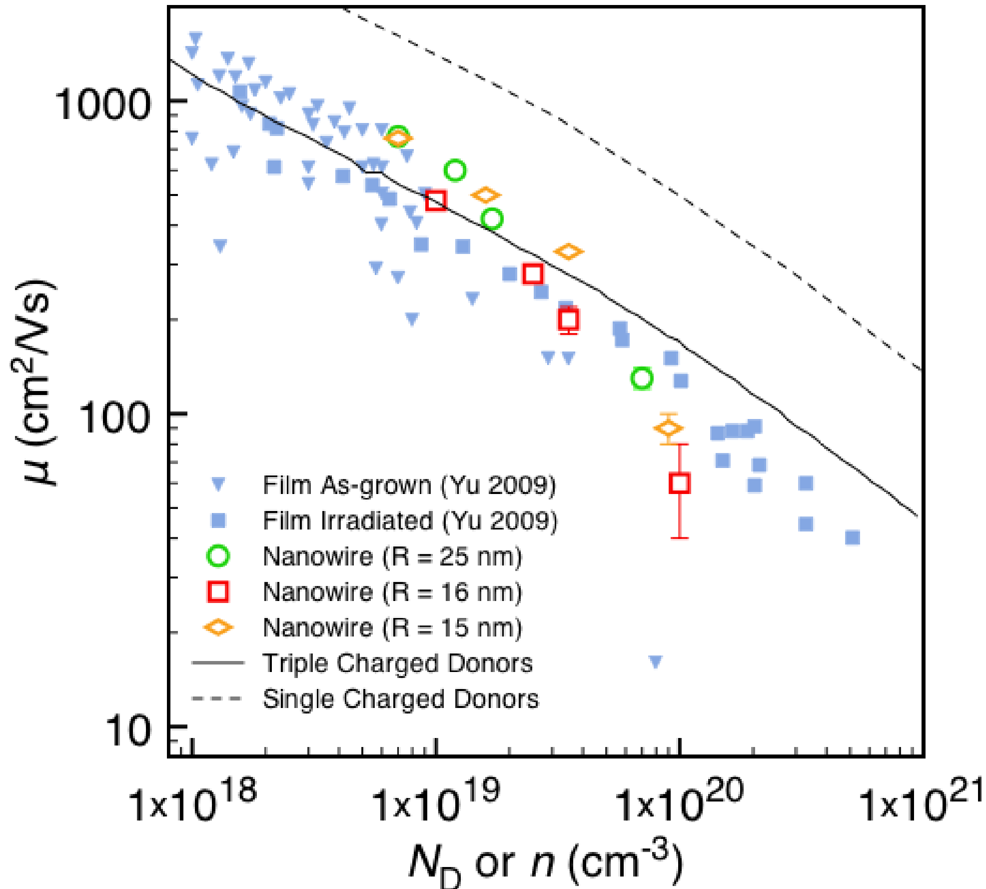

Figure 4.9. Experimentally measured mobilities as a function of carrier concentration (n) of as-grown and irradiated (2 MeV He^+) InN thin films as measured by Hall effect from Ref. [60] along with μ_c as a function of N_D of three InN nanowires studied in this work. The left-most data point for each nanowire is as-grown. The error bars on the right most data points represent uncertainty in μ_c due to the lack of a distinct flat region in the μ_{eff} vs. E_{eff} curves at low fields. The solid and dashed lines are theoretical calculations of mobility for InN thin films where the predominant native defects are triple and single charged donors, respectively.

Upon irradiation with He^{++}, we expect that while μ_c reduces as a result of an increase in N_D, μ_{sr} will remain unchanged, resulting in the universal mobility behavior observed for Si MOSFETs (Fig. 4.3) at high effective fields. Although the mobility curves for our InN nanowires do not fully merge onto a single curve at high fields (Fig. 4.7), the mobility

difference between the curves does reduce slightly at high fields, so we may expect that the curves for different fluences will merge, only at higher fields than what we achieved by electrolyte gating. We verified this quantitatively by fitting the mobility curves from all four fluences in Fig. 4.7 with Matthiesen's rule where μ_c changes with fluence but μ_{sr} is fixed for all fluences. This fitting is shown in Fig. 4.10. We can see that a single μ_{sr} cannot describe the high-field behavior of all of the curves. We found that each mobility curve for the different irradiation fluences can, however, be fit individually if μ_{sr} is adjusted independently. Fits to the first three mobility curves (as-grown, 2.1×10^{14} cm^{-2} and 7.1×10^{14} cm^{-2}) can each be fit independently by reducing β but fixing γ at 1.5[3].

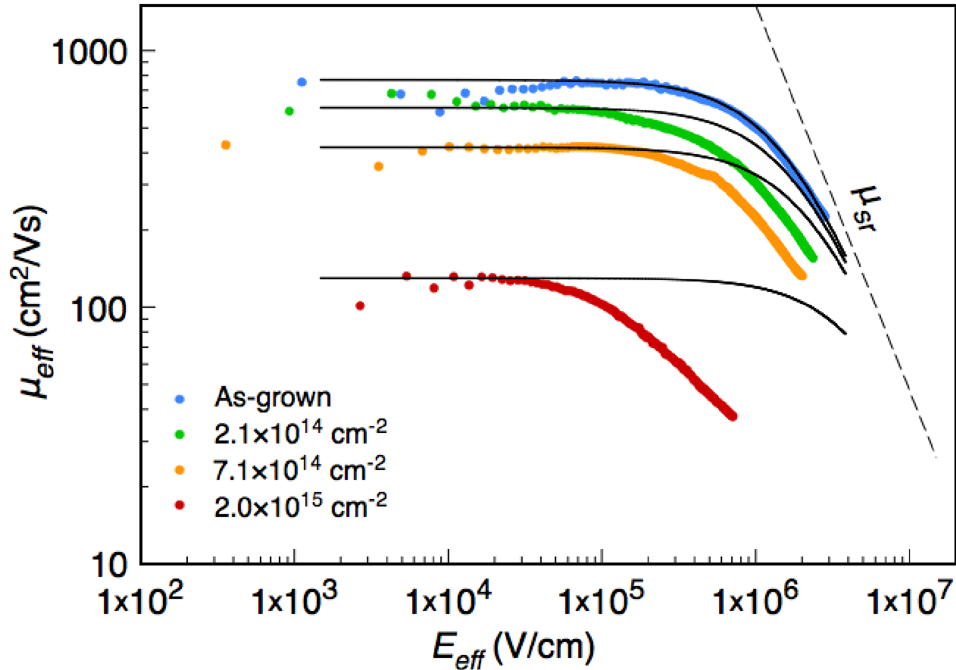

Figure 4.10. Effective mobility curves from Fig. 4.7, with fits (solid lines) where μ_c was varied for each fluence but μ_{sr} (dashed line) was held fixed.

To help explain this lack of universality at high fields, an understanding of the dependence of β on material parameters (that may be affected by irradiation) is necessary. Lee et al. [67], citing calculations by Cheng and Sullivan [68] of the electron scattering rate at Si MOFET surfaces, suggest that β is inversely proportional to the effective mass (m^*) and surface roughness as per

$$\beta \propto \frac{1}{m^* m_e (L\Delta)^2} \tag{4.6}$$

where m_e is the electron mass, while L and Δ are the correlation length and mean asperity

[3] The highest fluence (5×10^{15} cm^{-2}) mobility curve requires a reduction in γ to ~ 1 to be fit. The cause of this is not fully understood but could be due to such high carrier concentrations ($\geq 10^{20}$ cm^{-3}) that additional effects such as band renormalization are required to accurately describe the electrostatic behavior of the wire, especially at large positive gate voltages.

height, respectively, which are two parameters used to characterize surface roughness, shown schematically in Fig. 4.11. It should be noted that using L and Δ is only one of several ways to characterize surface roughness and a given nanowire's surface topology is not likely periodic or well-defined as the schematic in Fig. 4.11 shows. Nevertheless, Eq. 4.6 allows us to estimate whether reasonable variations in m^* or surface roughness upon irradiation can explain the differences in β observed after irradiation with different fluences. The β values that fit the mobility curves for the first two irradiation fluences, 2.1×10^{14} cm^{-2} and 7.1×10^{14} cm^{-2}, differ from the β value of the as-grown curve by 49% and 64%, respectively.

An increase in electron effective mass as a function of irradiation arises from the non-parabolicity of the conduction band minimum of InN. That is, an increase in electron concentration from irradiation pushes E_F higher into the conduction band, where m^* is larger, which causes a decrease in β as per Eq. 4.6. However, from the known dependence of electron effective mass on electron concentration in InN thin films [34], the expected change in electron effective mass in our nanowires from irradiation at fluences of 2.1×10^{14} cm^{-2} and 7.1×10^{14} cm^{-2}, is 4% and 8% respectively. Thus, effective mass changes alone cannot fully explain the lack of universal mobility behavior observed in our nanowires at high fields.

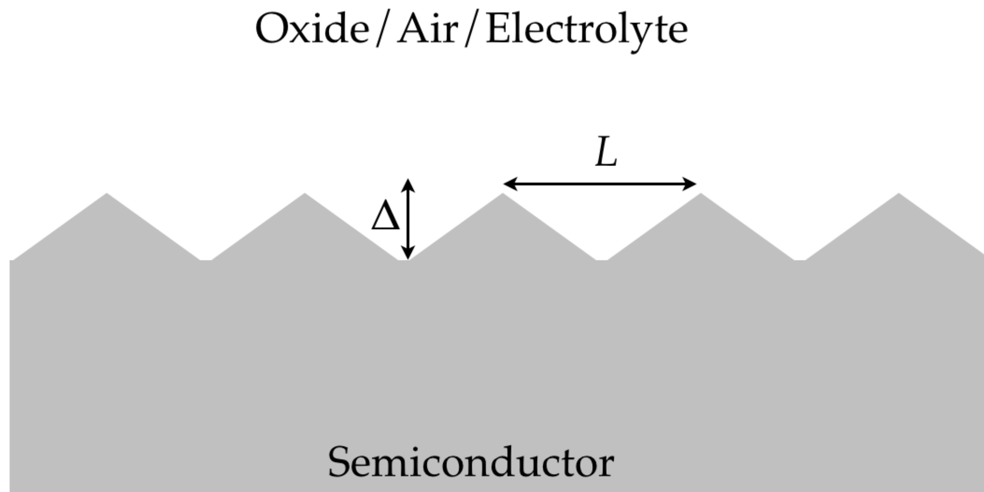

Figure 4.11. A model of surface roughness with parameters used by Cheng and Sullivan [68] and Lee et al. [67]. L is the correlation length and Δ is the mean asperity height.

The second possible explanation is that the 2 MeV He^{++} irradiation, along with increasing the native defect concentration in InN, also increases surface roughness. Though sputtering or etching of semiconductors and metals by high energy ions is generally considered to be minimal at MeV energies, we can see form Eq. 4.6 that only a slight increase in surface roughness is necessary to account for our observed changes in β. For example, using Δ as a parameter to track surface roughness, if Δ in an as-grown nanowire is ≈ 1 nm, an increase in Δ of only 7 angstroms to 1.7 nm upon irradiation would fully account for the observed 64% change in β.

Changes in surface morphology after irradiation with ions of $\approx$ MeV energies have, in fact, been reported in the literature. Maaza et al. [69] reported changes in indium tin oxide

(ITO) surface morphology after irradiation with 2 MeV He^+ ions with fluences comparable to this work ($2 - 6 \times 10^{15}$cm^{-2}). In addition, a monotonic increase in surface roughness of zirconia films irradiated with 250 - 450 keV He^+ ions was measured with atomic force microscopy (AFM) by Kuri et al. [70]. The RMS roughness of these samples increased from 0.17 nm to 0.4 nm, on the order of what is expected for our nanowires. Thus, we feel that an increase in surface roughness upon irradiation is the most likely explanation for the lack of universality in our mobility curves at high effective fields.

We performed AFM measurements to observe diameter or surface morphology changes upon irradiation. Similar to our electrical measurements, the exact same nanowires were measured before and after irradiation. No change in diameter was observed with irradiation, verifying that the nanowires are not significantly etched by the high energy particle irradiation. A change in surface roughness of a nanowire on the order of 1 nm or less is difficult to measure with conventional tapping-mode AFM, where the tip radius ($\sim$ 20 nm) is itself on the order of our nanowire radii. High-resolution transmission electron microscopy has been used to characterize surface roughness differences between nanowires grown by different techniques [71] and would be a useful future experiment to confirm a surface roughness increase upon irradiation.

4.5 Implications for Nanowire Transport

In this chapter, we have presented a technique for quantifying the magnitude of individual scattering mechanisms that limit carrier mobility in semiconductor nanowires. Using well-established universal mobility analysis, which involves examining the dependence of effective mobility on effective electric field in a gated semiconductor, we were able to distinguish between coulombic scattering limited mobility at low-fields and surface roughness limited mobility at high fields in MBE-grown n-type InN nanowires. Our results show that for nanowires with diameters larger than the free carrier Bohr radius, surface roughness scattering only limits carrier mobility when there is heavy band bending near the surface of the wire ($\approx 10^6$ V/cm). Thus, for most semiconductor nanowires with diameters of tens of nanometers, surface roughness scattering will not be the limiting factor of carrier mobility except for at large gate voltages. Instead, scattering from ionized dopants or phonons will limit mobility. These results have device implications. Namely, when engineering nanowires for high-mobility applications, optimizing dopant and defect concentrations should be given precedence over surface treatments.

In addition, our results demonstrate the utility of universal mobility analysis as a tool for characterizing electronic transport in semiconductor nanowires. Unlike previously reported methods for deconstructing mobility into individual scattering components, this method does not require the growth and measurement of a large set of nanowires with a wide range of diameters; a single nanowire is sufficient. Experimentally, this technique is based on $I(V_G)$ data from nanowire FET measurements, which is already the most widely used electrical characterization method for semiconductor nanowires. Lastly, although finite-element anal-

ysis was used to compute μ_{eff} and E_{eff} in this work, for semiconductors whose surface Fermi level pinning characteristics are already well known (e.g. Si), μ_{eff} and E_{eff} can be computed analytically to good accuracy, as the multitude of papers [58, 57, 18] on universal mobility of Si MOSFETs demonstrate. For these reasons, an extension of this work to other semiconductors, nanowire growth techniques, and surface treatments would be extremely valuable.

Chapter 5

Doping Limitations in Semiconductor Nanowires

5.1 Background

In previous chapters, we have explored different methods of characterizing the carrier distribution and mobility in semiconductor nanowires. In many situations, the ionized dopant concentration, N_D, was varied to very high values ($> 10^{20}$ cm^{-3}). Heavy doping is often necessary to successful realize some of the applications of semiconductor nanowires discussed in Chapter 1. Unfortunately, many semiconductors are notoriously difficult to dope even in bulk form [72]. For example, reliable and well-controlled p-type doping of ZnO and InN has not been experimentally demonstrated. In addition, using local density approximation calculations, it has been theoretically predicted that in GaAs quantum dots,quantum confinement tends to stabilize a deep defect, the DX center, which makes extrinsic doping less effective than in the bulk [73]. This is corroborated experimentally with a lack of reported high doping levels in semiconductor nanostructures. It is, therefore, of great importance to understand and predict the n and p-type doping limits of semiconductor nanostructures in terms of their fundamental material parameters.

5.2 Amphoteric Native Defects

Doping limits in various bulk semiconductors are well explained by the amphoteric nature of compensating native defects. The amphoteric defect model (ADM) [72, 74] asserts

that the formation energy of charged native defects, such as vacancies and anti-sites, depends linearly on the Fermi level in the crystal. In heavily damaged materials with high defect concentrations, it was discovered that the Fermi level always shifts toward the same energy value, known as the Fermi stabilization energy (E_{FS}) [72]. In all materials, including those without high defect concentrations, the further E_F moves away from E_{FS} by extrinsic doping, the lower the formation energy is for the system to generate native defects that act to compensate the extrinsic dopants. That is, native defects are generated in semiconductor materials in response to extrinsic doping so as to pull E_F back towards E_{FS}. Depending on whether E_F is above or below E_{FS}, acceptor- or donor-like native defects are predominant, giving these defects their amphoteric character. The net effect is that it is increasingly difficult to move E_F away from E_{FS} by adding external dopants as the dopants will be more easily compensated by native defects the farther E_F is from E_{FS}. In fact, in equilibrium conditions, after significant external doping, E_F eventually saturates at a limit value ($E_{F-limit}$) away from E_{FS}. At this point, the formation energy for native defects is sufficiently low so that any additional dopants will be fully compensated. This imposes an effective limit to E_F, and hence the free carrier concentration.

The Fermi stabilization level, also termed the branch point energy [33] or the charge neutrality level, has been shown to have a universal energy of about 4.9 eV below the vacuum level [72], independent of the particular semiconductor or dopant species. This is due to the fact that the amphoteric native defects are strongly localized in real space, similar to the universally aligned transition metal defect levels [75, 76]. Their wavefunctions in k-space thus sample the entire Brillouin zone, leading to an energy level that is determined by regions with a large density of states, and is insensitive to the band edges of the host, which have a small density of states. This universal alignment of E_{FS} is shown in Fig. 5.1 together with the natural band edge offsets of the different semiconductors investigated in this study [72].

Figure 5.1 is quite useful in explaining doping difficulties and disparities between different semiconductors. For example, in previous chapters we've discussed the strong propensity of native defects in InN and InAs to be n-type. We can see in Fig. 5.1 that this is because E_{FS} is located above E_C in these semiconductors, instead of in the bandgap, so native defects always assume an n-type character to drive E_F to that position. Also shown in Fig. 5.1 are the positions of $E_{F-limit}$, back-calculated using maximum reported electron or hole concentrations in bulk materials grown by equilibrium methods [77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87] . In n-type InAs and InN, $E_{F-limit}$ is located deep in the conduction band such that the strongly non-parabolic part of the conduction band is populated [85]. In Fig. 5.1 we show the range of $E_{F-limit}$ back-calculated for n-type InN and InAs, where the lower bar corresponds to $E_{F-limit}$ for the non-parabolic conduction band, and the upper bar is $E_{F-limit}$ when the band is approximated by a parabolic dispersion with electron effective mass equal to the mass at E_C .

The doping limits that are the subject of this chapter originate from the differing behavior of shallow and localized defects in response to the movement of the conduction and valence band edges. Specifically, shallow dopants closely follow the movement of E_C (for donors) and E_V (for acceptors). In contrast, the energy of strongly localized defects remains relatively

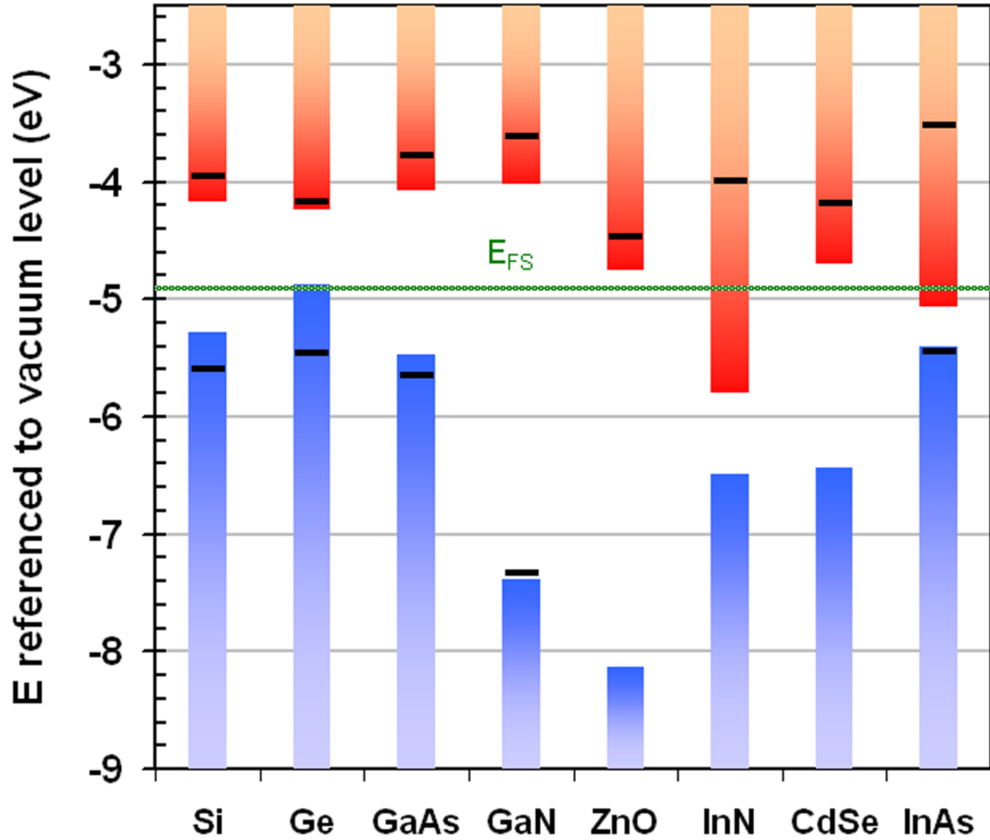

Figure 5.1. Band offsets and E_{FS} for the eight semiconductors studied. Red and blue bars represent the conduction and valence bands, respectively. Black lines within bands represent $E_{F-limit}$ in bulk obtained from literature values of maximum reported carrier concentrations for electrons and holes. For n-InN and n-InAs, two bars are shown, corresponding to calculated $E_{F-limit}$ using parabolic (upper bar) and nonparabolic (lower bar) conduction band dispersion, respectively. Reported electron concentrations for Si, Ge, GaAs, GaN, ZnO, InN, CdSe, and InAs were obtained from Refs. [77, 79, 81, 83, 84, 85, 86, 87], respectively. Reported hole concentrations for Si, Ge, and GaAs were obtained from Refs. [78, 80, 82], respectively.

constant under these external stimuli [88]. These distinctly different sensitivities of shallow and localized defect levels also hold true in the case of quantum confinement [73]. When size is reduced in semiconductor nanostructures, the density of states (DOS) is restructured and the energies of allowed states shift upward from the original E_C (for n-type) or downward from E_V (for p-type), as detailed in the next section; however, the Fermi stabilization energy and the Fermi level limits remain unchanged due to their origination from strongly *localized* defects with a spatial extension ($\sim$ a few atoms) much smaller than the spatial confinement of the system [73]. Consequently, the maximum achievable carrier concentration is suppressed for nanoscale materials of smaller and smaller dimension. In this chapter we show results that quantify this limit on maximum achievable carrier concentration due to quantum confinement in the context of the ADM. For simplicity, we assume no surface Fermi level pinning.

5.3 Quantum Confinement

Up to now, this dissertation has only modeled free carrier distributions using classical electrostatics. Electrons and holes are, of course, quantum particles, and their distributions are dependent on the potential distribution in which they reside. As outlined in Chapter 1, when the size of a nanostructure is reduced substantially, the free carriers in the nanostructure become confined by the walls of the material, which can be modeled as infinite potential barriers and their wavefunctions are affected accordingly. This confinement can be in one, two, or all three dimensions, depending on the particular nanostructure, from thin-film to quantum dot, as shown in Fig. 5.2.

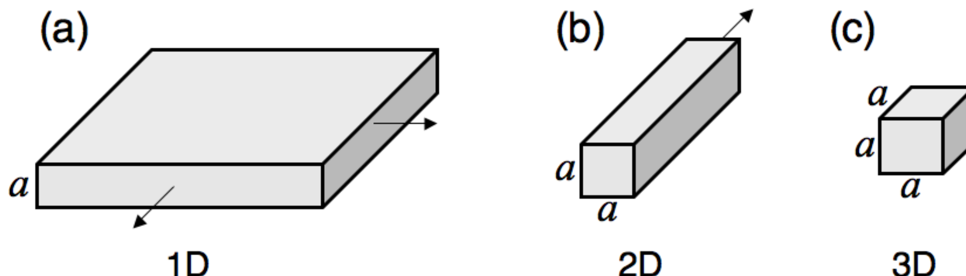

Figure 5.2. Schematics of semiconductor geometries with varying degrees of confinement: (a) 1D confinement in a thin film; (b) 2D confinement in a nanowire; (c) 3D confinement in a quantum dot. Dimensions are assumed to be rectangular with confined dimensions of length a marked.

Free carriers in nanowires are confined in the radial direction, allowing only one free dimension (z) and making nanowires a quasi-1D system. For simplicity, in this theoretical study, similar to Chapter 1, the nanowire is modeled as having a square cross-section (Fig. 5.2(b)), so that the confinement in the (x, y) plane is approximated by an infinitely deep square well with width a. Experimentally, nanowires of various materials have been grown with a wide variety of different facet arrangements, including rectangular [7], as mod-

eled here. Faceting differences can be expected to slightly effect the results of this study quantitatively but not qualitatively.

For this infinite square well potential, the 1D density of states (per volume) for a single valley in the band structure is the sum over multiple confinement subbands

$$g_{1D}(E) = \frac{1}{\pi\hbar a^2} \sum_{N_x N_y} \sqrt{\frac{2m_z^*}{E - (E_0 + E_{N_x N_y})}} \tag{5.1}$$

where E_0 is E_C (for n-type) or E_V (for p-type), m_z^* is the effective mass of carriers along the unconfined nanowire length direction. $E_{N_x N_y}$ is the quantized energy level, defined in Eq. 1.5, and m_{xy}^* is the effective mass in (x, y) plane, which can be different from m_z^* (or n-type indirect-bandgap semiconductors such as Si and Ge). When combining $E_{N_x N_y}$ as per Eq. 1.5 with Eq. 5.1, we see that quantum confinement in the (x, y) plane has the net effect of creating so-called van Hove singularities in the DOS corresponding to the onset of sequential confinement levels. In Fig. 5.3 the DOS is plotted for GaAs with two different nanowire widths and compared to the standard 3D DOS. As the nanowire dimensions increase, the 1D DOS begins to merge with the 3D DOS as expected.

5.4 Confinement Induced Limits to Carrier Concentration

The maximum achievable carrier concentration is obtained by integrating the 1D DOS shown in Eq.(1) from $E = E_0$ to $E_{F-limit}$. This is equivalent to treating the Fermi distribution as a Heaviside function, which is a fair assumption since all of the materials investigated have an $E_{F-limit}$ many $k_B T$ away from the conduction or valence band edge, so the temperature induced broadening of the Fermi distribution has a negligible influence on the total carrier concentration. The sum in Eq.(1) runs from (N_x, N_y) = (1,1) to the highest energy subband that is still below $E_{F-limit}$ (i.e.,$E_0 + E_{N_x N_y} \leq E_{F-limit}$). For tetrahedrally structured semiconductors, the valence band DOS is a sum of the DOS from heavy-hole, light-hole, and split-off bands with distinct effective masses. As shown in Fig. 5.3(b) for the 3D case, the total valence band DOS is dominated by the heavy-hole band, which has the greatest effective mass. Also, for n-type indirect-bandgap Si and Ge, multiple conduction band valleys were taken into account by including a multiplicative degeneracy factor in Eq. 5.1.

Figure 5.4 shows the dependence of maximum achievable carrier concentration (n_{lim} or p_{lim}) on nanowire width, a, for the semiconductors investigated. This maximum achievable carrier concentration is strongly suppressed when the nanowire width is below ~20 nm for GaAs. There is an onset width below which the carrier concentration is zero. This onset corresponds to the width where the ground level energy subband (E_{11}) is raised beyond $E_{F-limit}$ by quantum confinement. The fine features in the curves at very small widths reflect single subbands moving across $E_{F-limit}$ and causing sharp rises in the total carrier

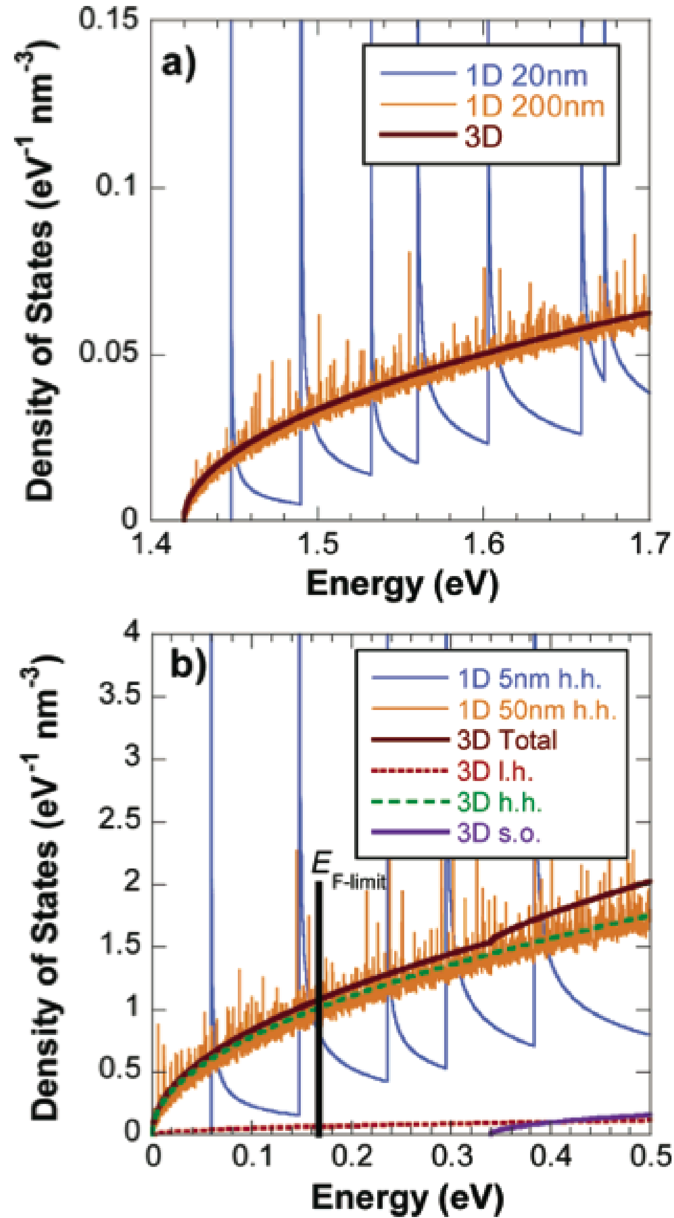

Figure 5.3. (a) One-dimensional conduction band DOS for GaAs nanowires of widths 20 and 200 nm plotted from the conduction band edge to $E_{F-limit}$ (1.705 eV). Three-dimensional DOS is also shown. (b) One-dimensional valence band DOS for nanowires of widths 5 and 50 nm compared to 3D DOS. $E_{F-limit}$ (0.167 eV) is shown. Density of states from heavy-hole, light-hole, and split-off bands are separately shown for 3D. The total valence band DOS is dominated by the heavy-hole band.

concentration. At large nanowire widths, the maximum achievable carrier concentrations quickly approach bulk values.

It should be noted, however, that Figures 5.4 (a) and (b) are plots of theoretical *limits* to carrier concentrations calculated in this model. Experimentally reported carrier concentrations can be substantially lower than these limits for a variety of reasons. First, during growth, most nanowires are not intentionally doped up to their maximum limit. Second, this model assumes complete passivation of surface states so as for E_F to be displaced solely by doping. Clearly from the extensive discussion in Chapter 3, this is not often the case, most semiconductors have band bending near the surface due to surface state induced electric fields. Although that chapter used InN as an example, most semiconductors have their E_F pinned inside the bandgap at the surface, resulting in a near surface depletion of carriers.

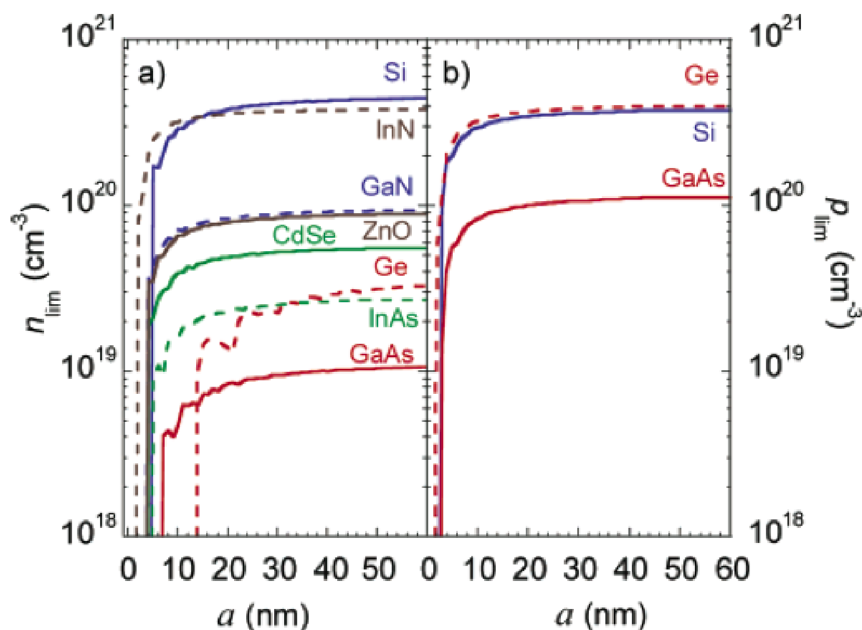

Figure 5.4. Maximum achievable electron (a) and hole (b) concentrations in different semiconductor nanowires as a function of nanowire width a.

We performed a survey of reported carrier concentrations in nanowires, and the obtained values are all within the limits shown in Fig. 5.4. For example, $n = 10^{18} - 10^{19}$ cm^{-3} in GaN with a diameter of 67 nm reported by Huang et al. [89], $n = 2 \times 10^{17}$ cm^{-3} in InAs with a diameter of 80 nm reported by Bryllert et al. [90], $n = 7 \times 10^{17}$ cm^{-3} in ZnO with a diameter of 42.5 nm reported by Yun et. al. [91], and $p = 10^{18}$ cm^{-3} in Si with a diameter of 15 nm reported by Cui et. al. [92].

5.5 Material Dependence of Doping Limits

Clearly, from Fig. 5.4, the rate at which the carrier concentration limit is reduced is not the same for all semiconductors. To help compare the reduction in n_{lim} and p_{lim} with nanowire size across different semiconductors, we can define a characteristic wire width (a_c) as the width at which the 1D carrier concentration limit equals half of the maximum bulk carrier concentration. It can be shown from Eq. 5.1 that the ratio of 1D to 3D doping limits is given by the following dimensionless expression,

$$\frac{n_{lim}^{1D}}{n_{lim}^{3D}} = \frac{6}{\pi}\xi \sum_{N_x N_y} \sqrt{1 - \xi(N_x^2 + N_y^2)} \tag{5.2}$$

where $\xi = (\hbar^2\pi^2/2m_{xy}^* a^2)/|E_{F-limit} - E_0| \leq 1/2$. Therefore, it is seen that the characteristic a_c that makes the ratio in Eq.(2) to be 0.5 obeys a scaling law as

$$a_c \propto \frac{1}{\sqrt{m_{xy}^* |E_{F-limit} - E_0|}} \tag{5.3}$$

Figure 5.5 clearly shows this linear dependence for the various n- and p-type semiconductors, where a_c was numerically determined from the curves in Fig. 5.4. A couple of notes should be made for this plot, first the non-parabolicity of the conduction band of InN and InAs was not factored into m_{xy}^*, but is expected not to change a_c for n-InN and n-InAs, as the increase in m_{xy}^* will be fully compensated by the reduction of $|E_{F-limit} - E_0|$. In addition, for p-type semiconductors under strong quantum confinement, the heavy and light hole effective masses undergo a mass reversal as well as an overall change in their values [88]. Its effect on the total DOS (thus on p_{lim}) that includes both heavy and light hole bands, however, is relatively small (e.g., estimated to be $< 20\%$ for GaAs). This is because the decrease in heavy hole mass is partially compensated by the increase in light hole mass [88]. We estimated the resultant maximum change in a_c from Fig. 5.4 and indicated the range by vertical bars in Fig. 5.5.

The conclusion we can draw from Eq. 5.3 and Fig. 5.5 is that the size effect on maximum achievable doping concentrations is simply determined by two inherent material properties, namely, the effective masses of free carriers, and $E_{F-limit}$ measured from the conduction or valence band edges. The latter is loosely a function of the band edge position alone because of the relatively weak variation of $E_{F-limit}$ over different materials on the absolute energy scale (Fig. 5.1). This convenient relationship can be used as a simple guide in estimating the size effect of doping limit in nanowires of various semiconductors and semiconductor alloys. For example, in n-type narrow-bandgap semiconductors such as InSb with a small electron effective mass ($< 0.02m_0$), the suppression of the doping limit should be readily seen at relatively large nanowire diameters. For p-type doping in the alloy $In_xGa_{1-x}N$, the heavy-hole effective mass does not change drastically from GaN ($\sim 1.3m_0$) to InN ($\sim 1.6m_0$), and $E_{F-limit}$ can be assumed to not vary as fast as the upward movement of E_V from GaN to InN; this results in an increasing $|E_{F-limit} - E_V|$ and thus a weaker size effect on the p-type doping limit with increasing x. Since the mechanism discussed here is not limited to the 1D

geometry, a similar doping trend is expected in semiconductor nanostructures with different geometries, such as quantum dots, tetrapods, core-shell structures, and ultra-thin layers.

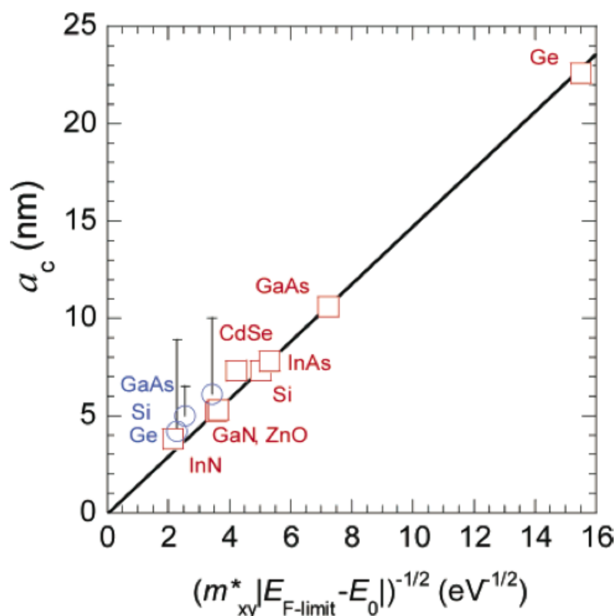

Figure 5.5. Characteristic nanowire width a_c for electron (squares) or hole (circles) doping as a function of conduction or valence band effective mass and relative Fermi level limit. Vertical bars indicate estimated range of a_c due to changes in hole effective mass caused by quantum confinement. Heavy-hole masses were used for valence band, and in-plane effective masses were used for the conduction band of indirect semiconductors. The straight line is a guide to the eye.

5.6 Additional Doping Limitations

In this chapter, we have shown that quantum confinement in semiconductor nanowires decreases the maximum achievable doping concentration, effectively making nanowires more difficult to dope than their bulk counterparts. We have quantified these effects and shown that the effect of quantum confinement on the doping limit is an intrinsic material property that depends on the effective mass of free carriers and the band edge positions of the semiconductor. We should note, however, that the mechanism of reduced doping outlined here is only one limit to maximum nanowire doping. Additional mechanisms of a reduction in doping or doping efficiency have been reported recently, including surface segregation [93] of dopants and dielectric confinement [16].

The latter effect is of particular importance as it has been observed to occur at relatively large radii before quantum effects, as discussed in this chapter, begin to take hold. The mechanism outlined by Bjork et al. cites an increase in the ionization energy of dopants due to

a mismatch in dielectric constant between the nanowire and its surroundings (air, oxide, etc.). They observed this effect in Si nanowires with radii as high as 15 to 20 nm. This dielectric confinement effect, in combination with the dopant compensation effect outlined in this chapter serve to emphasize that something as seemingly routine as doping of semiconductors can become a unique challenge when a material is engineered at nanometer dimensions. This challenge, in concert with pinning and surface mobility issues outlined in previous chapters must be accounted for when scaling semiconductors to nanometer dimensions.

Chapter 6

Impacts and Future Work

6.1 Impacts on Semiconductor Nanowire Technology

In the introduction, we outlined the main subject of this dissertation, which was to study methods of characterizing the basic electronic properties of semiconductor nanowires, most notably carrier concentration and mobility. This entails both improving the accuracy of existing methods of characterization as well as devising and testing new techniques that allow for the extraction of electronic properties previously left to assumptions or conjectures. Three projects that accomplished these goals were outlined in Chapters 2, 3, and 4. In all cases, we observed a recurring theme of how the "meso" size of our nanowires, which is significantly smaller than bulk semiconductors but not small enough to where quantum confinement effects completely dominate, created unique challenges in terms of characterization. In addition we saw how the aspect ratio of these nanowires makes surface effects quantifiably more important in understanding their electronic behavior.

Specifically, in Chapter 2, we showed how analytical approximations to nanowire-gate capacitance can lead to significant misestimations of carrier mobility and concentration. Figure 2.5 shows that for lightly doped silicon nanowires, the common back-gate capacitance formula (Eq. 2.1) results in up to an 80% overestimation of capacitance, which leads to an 80% underestimation of free carrier mobility. This error arises from both a misrepresentation of the device geometry as well as a neglect for the semiconducting properties of the nanowire. It is necessary to emphasize that the error from neglecting the semiconducting properties of the nanowire is a uniquely *nanoscale* effect. The main difference in electric field screening between a semiconductor and a metal is the Debye screening length (Eq. 2.9), which is generally on the order of tens of nanometers. Thus for micron scale or larger materials, band bending can largely be ignored as electric fields are fully screened within a small fraction of the total size of the material, but when working with nanoscale materials, surface band bending is critical to properly understanding their properties.

In chapter 3 we presented a method to extract the surface Fermi level pinning information from nanowires using only FET measurements and proper modeling. Despite the fact that Fermi level pinning is a difficult property to measure directly, this technique is very accessible since FET measurements are the most commonly performed electrical measurements on semiconductor nanowires. In addition, finite element modeling, although more complex than simple analytical calculations, can today be easily performed via a variety of of commercial software packages. The E_F extraction technique presented in this chapter falls into the category of a previously unmeasured nanowire property that is now experimentally obtainable.

In chapter 4 we delved deeper into the scattering mechanisms that limit carrier mobility in semiconductor nanowires. Existing reports on individual scattering mechanisms in semiconductor nanowires have been limited to observing a decrease in mobility with decreasing nanowire diameter and ascribing this behavior to increased surface roughness scattering in smaller diameter nanowires. A method of exploring how different scattering mechanisms dominate as a function of carrier distribution, which can be modified as a result of both intrinsic band banding and external electric fields had been lacking and is presented in Chapter 4. As was the case in the previous chapters, finite element modeling of the nanowire electrostatics was a key enabler, allowing a precise calculation both effective field and charge distribution in the nanowire. In addition universal mobility analysis, used in this chapter to extract information about nanowire scattering mechanisms had been used for decades in MOSFETs, which serves to highlight how existing semiconductor theory can still be exploited to characterize the electronic properties of semiconductor nanowires.

Lastly, in chapter 5, we presented a theoretical analysis showing that for very small nanowires, with diameters $\lesssim$ 10 nm, the conduction and valence band density of states will be significantly modified by quantum confinement, which results in a maximum doping limit due to the intrinsic propensity of semiconductors to generate compensating native defects when doped extrinsically. At the end of the chapter, we discussed additional doping limits presented in literature, all of which are a result of the unique size and aspect ratio of nanowires.

Taken together, the research presented in this dissertation serves to highlight the need for careful evaluation of semiconductor electrostatics as well as quantum mechanics when semiconductor materials are grown at nanometer dimensions. The latter, quantum mechanics, is well known to be an issue at small material dimensions, but the former, the increased impact of certain electrostatic phenomena is often overlooked. If however, we have hopes to develop unique semiconductor materials at nanometer sizes for the continuation of Moore's Law, special care must be taken to understand, characterize, and possibly control their electrostatic properties, especially those originating from the surface.

6.2 Future Work

Much of the work in this dissertation involves solving Poisson's equation to calculate the potential and charge distributions in nanowires. In chapter 1, we laid out why quantum confinement was ignored in these computations, citing the fact that at 30 - 100 nm diameters, the quantum confinement induced subbands in the density of states can be easily populated by thermal energy alone. Of course, quantum effects are not binary, they gradually become more important as a function of size, so for the smallest diameter wires measured or computed in this work, one expects that there will be some modification of the results presented herein due to confinement. Thus, in those situations, a more accurate solution would be obtained by solving a coupled Poisson-Schrodinger equation. Though such a problem is significantly more complex and computationally intensive, one would obtain a very accurate picture the behavior of charge densities and band bending as a function of material size.

The surface Fermi-level pinning extraction method in Chapter 3 was experimentally tested only on InN, which has strong downward band bending at the surface. An obvious next step is to apply this technique to other semiconductors. A comprehensive study of Fermi-level pinning behavior manifested in FET properties of a range of commonly studied semiconductors would be incredibly useful to the nanowire community.

In chapter 4, we noted that the lack of universality at high fields in the universal mobility curves was most likely due to an increase in surface roughness on the order of a single nanometer or less from high-energy ion irradiation. A thorough transmission electron mobility study of this effect could solidify this hypothesis. In the process, it may emerge that ion irradiation with varying energies may be a useful research tool for controllably modifying the surface roughness of semiconductors while also modifying native defect concentrations.

Lastly, it is the hope of the author that subsequent researchers studying nanoscale semiconductor materials will devise even more creative methods of probing their properties, and if the work presented in this dissertation can help guide such research or serve as a starting point, the author will consider it a success.

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