UNIVERSITY OF CALIFORNIA, SAN DIEGO

Inverter-Based Disturbance Rejection of Real and Reactive Power

A dissertation submitted in partial satisfaction of the

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by

Benjamin Thomas Gwynn

Committee in charge:

Professor Raymond A. de Callafon, Chair
Professor Mauricio de Oliveira
Professor Jan Kleissl
Professor Ramash Rao
Professor David Victor

2019

The Dissertation of Benjamin Thomas Gwynn is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2019

DEDICATION

To my mom and my wife.

”My son, the doctor!” she said.

If not for your reminders

I would have given up long ago.

EPIGRAPH

All progress is precarious,

and the solution of one problem brings us face to face with another problem.

—Martin Luther King, Jr.

Nothing happens quite by chance.

It's a question of accretion of information and experience.

—Jonas Salk

New knowledge is the most valuable commodity on earth.

The more truth we have to work with, the richer we become.

—Kurt Vonnegut

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Chapter 2 contains a reprint of the material as it appears in ”Xin Zhao, Benjamin T. Gwynn, Raymond A. de Callafon, and William Torre, Disturbance Rejection of Real Power Flow by Grid-Tied Inverter.” The dissertation author is the secondary author of the article. Additional original discussion is added at the end of the chapter to contextualize findings within the dissertation.

Chapter 5 in full, is a reprint of the material as it appears in ”Benjamin T. Gwynn, Raymond A de Callafon, Demodulation of Three-Phase AC Power Transients in the Presence of Harmonic Distortion” to appear in IEEE Transactions on Power Electronics. The dissertation author is the primary investigator and author of this article.

Chapter 6 in full, is a reprint of the material as it appears in ”Benjamin T. Gwynn, Raymond A

de Callafon, Robust Real-Time Inverter-Based Reactive Power Compensation" submitted to IEEE Conference on Decision and Control (CDC). The dissertation author is the primary investigator and author of this article.

VITA

2002	B.S. in Mechanical Engineering, California State University, Long Beach
2003-2008	Division Officer, US Navy
2009-Present	Mechanical Engineer, SSC Pacific
2014	M.S. in Engineering Sciences (Mechanical Engineering), University of California San Diego
2019	Ph.D. in Engineering Sciences (Mechanical Engineering), University of California San Diego

PUBLICATIONS

Benjamin T. Gwynn, Raymond A de Callafon, "Robust Real-Time Inverter-Based Reactive Power Compensation," Submitted to IEEE Conference on Decision and Control (CDC).

Benjamin T. Gwynn, Raymond A. de Callafon "Demodulation of Three-Phase AC Power Transients in the Presence of Harmonic Distortion," Submitted to IEEE Transactions on Power Electronics.

Xin Zhao, **Benjamin T. Gwynn**, Raymond A de Callafon, William Torre "Disturbance Rejection of Real Power Flow by Grid-Tied Inverter," In American Control Conference (ACC), 2016, Seattle, USA May 2017.

ABSTRACT OF THE DISSERTATION

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by

Benjamin Thomas Gwynn

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Professor Raymond A. de Callafon, Chair

Electric grid transients stress power systems and can have cascading effects leading to widespread damage. Transient effects and oscillations are made worse by an increased portion of power supplied by sources without any rotational inertia, such as DC to AC inverters connected to photovoltaics or energy storage media. Yet, the solid state architecture of modern inverters allows unprecedented response time, enabling novel control schemes.

It is difficult to leverage the speed of modern inverters because of the comparably slower response rate of microprocessors. Electric grid transients are characterized by a mix of grid-frequency and lower frequency components, and a high levels of harmonic distortion that accompanies the most common inverter architectures, forming challenges in signal processing. Furthermore, the complexity of electric grids makes model development and validation difficult.

This dissertation makes contributions toward overcoming these difficulties and demonstrates feasibility of controlling inverter output to mitigate transient effects on an electric grid.

A grid-connected reference circuit allows recreation of power oscillations when an inductive load is switched in. Parallel processing via a field programmable gate array allows signal processing that demodulates and filters inverter-supplied power, removing grid frequency components and higher harmonics. The result is clean real-time active and reactive power signals sent to a microprocessor for control. This data is used for system identification, greatly reducing the burden of model development. Finally the improved signal serves as input to a robust control scheme that adjusts inverter active and reactive power output for disturbance rejection of transients created by the reference circuit.

Chapter 1

Introduction

1.1 Motivation and Aim

On 8 September, 2011, an electric grid operator error caused a high voltage branch trip in Arizona. This triggered a series of automated protective actions that, over the course of 11 minutes, culminated in loss of power to 2.7 million people in the greater San Diego-Tijuana region [1]. Dubbed ”the Great Blackout of 2011,” the event was a worst case example of the potential cascading nature of electric grid transients. The research presented in this dissertation could not have prevented the blackout, but is motivated toward stifling the potential for similar chain reactions.

The research aims at operating DC-AC inverters to mitigate electric grid transients. Inverters are situated between DC power sources, such as photovoltaic (PV) arrays or batteries, and the AC electric grid. By converting DC power to AC, inverters allow these power sources to contribute to the distribution grid.

Acoustics provide inspiration in their use of active cancellation for noise suppression using a phenomenon known as destructive interference [2]. If two oscillatory signals are 180 degrees out of phase with each other, then when added together the sum of the signals is effectively null as troughs cancel peaks and vice versa. Similarly, the fluctuations attendant to electric grid transients may be minimized by meeting them with a complementary signal provided by an inverter.

1.2 Background

Concerns of global climate change and renewable energy initiatives have spurred the rapid adoption of wind and solar power as distributed energy resources (DER), as well as integration of storage media due to the intermittent nature of these renewable power sources [3]. On average, the total new solar installation cost halved in the United States between 2010 and 2014 [4]. In the same period the global total nameplate Megawatt peak solar capacity increased by more than 300% [5],[6]. An unfortunate side effect of this proliferation has been reduced stability of the connected electric grids [7].

Historically operators have had no means to counteract a transient while in progress because of the short duration of electric grid transients and slow response of conventional AC generators [8]. However, intervention is not always necessary; an advantage of conventional power generation is that it is accomplished by large spinning machines, which have considerable rotational inertia that serves to stabilize the electric grid. Connecting or disconnecting even large loads has limited impact on machine speed by virtue of the machines' rotational inertia [9]. However, modern inverters create an AC waveform through transistor switching, and thus have no similar inertia. As a result, connection of DER providing power via inverters reduces the proportion of inertia to total power available on the grid [10].

An effect of this change is that when there are more DER connected to the grid there are increased power oscillations upon a grid transient, as depicted in Fig. 1.1. The figure shows a long-lasting fluctuation in active power following a branch trip on the University of California San Diego microgrid.

Many efforts into overcoming the problems caused by inertia-less inverters have aimed at adding synthetic inertia, recreating the droop relationships of conventional generation [11], [12], [13], [14].

Droop is defined by the frequency change necessary to cause a generator prime mover control mechanism to fully open the throttle from fully closed [15]. Figure 1.2 is a 'house diagram' illustrating the power-frequency relationship. The figure appears simple, but there is a lot of infor-

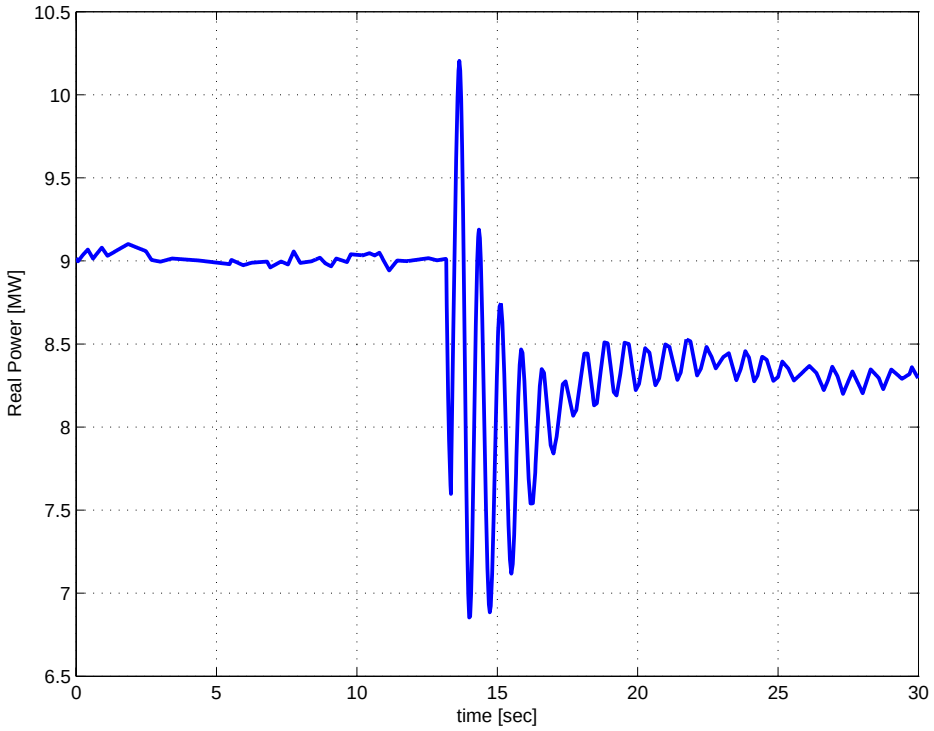

Figure 1.1: Measured active power oscillations on the main 3-phase interconnection of the UCSD Micro-Grid during a step-wise load demand change.

mation contained in it. Droop is represented by the slope of the diagonal line, the houses' roof, if you will. The 'roof' of the utility is essentially flat because the power supplied by all utility power sources is orders of magnitude greater than the single generator.

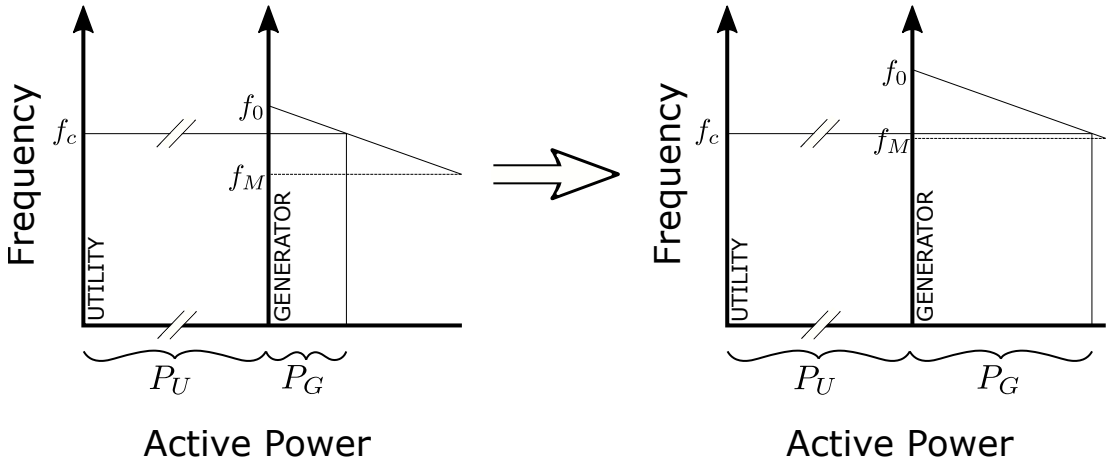

Figure 1.2: The generator no-load frequency is slightly above grid frequency on the left, then increased causing the generator to provide more power on the right.

When a generator is paralleled to the distribution grid, the force imparted by the prime mover is balanced by counter-electomotive force, maintaining the generator at grid frequency f_c [16]. In the figure, this is represented by the horizontal line starting at f_c on the utility frequency axis, passing through the generator frequency axis, and continuing to the droop diagonal. Referencing the figure, if the no-load frequency of the generator is increased, the intersection of grid frequency and the droop diagonal shifts right, and the generator assumes a greater portion of the active power load, as represented by the larger P_G on the figure right hand side. There is a similar voltage droop relationship between a conventional generators' voltage regulation system and reactive power output.

As an extension of the relationship between governor and throttle valve position, and dependence on force balance between the prime mover and EMF resulting from current induced in generator windings, droop control makes sense as a control strategy for operating multiple conventional generators at a common frequency. However, inverters have no valves, governors or prime movers, per se, making implementation of droop control a contrivance to assimilate into the status quo. Indeed, imposing droop control on an inverter is akin to operating an automobile so as to mimic a horse drawn carriage; a car can be driven this way without problem, but most the horsepower afforded by an internal combustion engine would be unutilized. The lack of inertia in inverters makes fast-acting control possible.

Synchrophasors are an emerging technology allowing detailed analysis of sequence of events after a grid event and showing great promise in helping operators identify grid instabilities in real time [17]. Typical phasor measurement units (PMUs) perform discrete Fourier transform (DFT) on voltage and current measurements over a sliding sample window. A sinusoid of form $x(t) = X_m \cos(\omega t + \phi)$ is expressed in phasor form as

$$\mathbf{X} = \frac{X_m(t)}{\sqrt{2}} e^{j\phi(t)}. \tag{1.1}$$

The amplitude $X_m(t)$ and phase $\phi(t)$ are then compared to a reference cosine at the grid nominal

frequency, generated from absolute time signals provided by Global Positioning System (GPS). A synchrophasor is defined as a phasor like that given in (1.1) where $\phi(t)$ is the instantaneous phase angle relative to the reference cosine with maximum at the top of each UTC second [18]. The time stamps make comparison of simultaneous measurements at geographically separated locations possible.

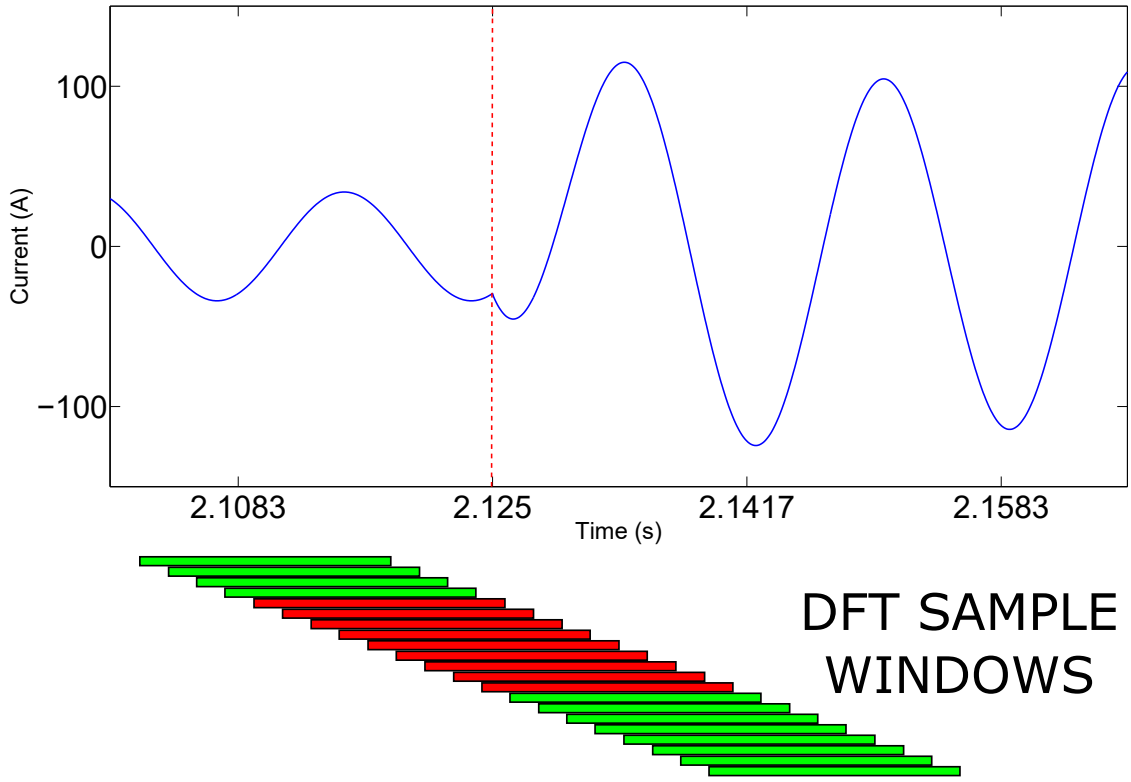

Figure 1.3: Phasors calculated from data either entirely preceding or entirely after the transient at t=2.125 are valid; those from data bracketing the fault contain a mixture of two waveforms making them unsound.

Some research [19] has indicated that immediately following a transient, phasor estimates made by a PMU are of poor data quality in terms of calculated values $X_m(t)$ and $\phi(t)$. Voltage and current are subject to instantaneous phase and magnitude changes upon a fault. By the nature of Fourier transforms, when the sample window contains data that is a mix from both before and after a fault, the two distinct waveforms make the DFT output invalid and inappropriate for use toward control [20]. Figure 1.3 illustrates a transient in current and the corresponding invalid windows containing mixed waveform data. Most PMUs use a sample window size matched to the nominal

cycle period, leading to an inherent delay of one cycle after a transient before reliable data is available for control or protective action.

Unfortunately the use of GPS also creates a liability. Monitoring or control systems utilizing synchrophasor data are susceptible to disruption by GPS spoofing, a problem that has been thoroughly discussed [21],[22],[23],[24], and demonstrated [25]. One benefit of inverter droop control is the dependence only on variables that can be measured locally, making it independent from external communication [26].

A novel approach to control of inverter power output that relies only on locally available signals while capitalizing on the rapid response of an inverter is presented in Chapter 2. This approach applied robust control methods to achieve active power disturbance rejection in response to connection of an inductive load. The load is a reference circuit specifically designed to have oscillatory transient dynamics similar to electric grids with reduced total inertia, but with parameters scaled to safely allow laboratory testing without disrupting neighboring grid customers. Unfortunately, the design relied on a poorly formulated demodulation algorithm, making results only intermittently reproducible.

The following summary of circuit physics is provided to support the discussion of the demodulation method; circuit physics are discussed in depth in Chapter 3, and the necessity of demodulation will be discussed in section 1.3: Reference circuit transient current is governed by an ordinary differential equation with solution

$$i(t) = i_p(t) + i_h(t), \tag{1.2}$$

where

$$i_p(t) = I_p \cos(\omega_c t - \psi - \phi_s) \tag{1.3}$$

is the particular solution and

$$i_h(t) = I_h(\phi_s) e^{-\eta(t)} \cos(\omega_0(t) - \beta(\phi_s)) \tag{1.4}$$

is the homogeneous solution. I_p and ψ are determined by circuit parameters while $I_h(\phi_s)$ and $\beta(\phi_s)$ result from initial conditions. Voltage is given by $v(t) = V\cos(\omega_c t - \phi_s)$ where ϕ_s is the phase of voltage when the transient initiates. Instantaneous power is given by $P(t) = v(t)i(t)$, resulting in transient active power on a single phase

$$P(t) = P_p(t) + P_h(t) \tag{1.5a}$$

$$P_p(t) = \frac{VI_p}{2}\cos(\psi) + \frac{V_{ss}I_p}{2}\cos(2\omega_c t - \psi - 2\phi_s) \tag{1.5b}$$

$$P_h(t) = [V\cos(\omega_c t - \phi_s)][I_h(\phi_s)e^{-\eta(t)}\cos(\omega_0(t) - \beta(\phi_s))] \tag{1.5c}$$

The method for demodulation of active power was presented in [27], with aim to remove the term $\cos(\omega_c t - \phi_s)$ from (1.5c). The procedure is summarized below:

- Active power on each phase $m = a, b, c$ is demodulated individually by multiplying power by the normalized voltage signal of the respective phase, and filtering:

$$P_{Vm}(t) = F_{LP}(q)F_{FIR}(q)v_m(t)i_m(t)\frac{v_m(t)}{V}.$$

  Terms $F_{LP}(q)$ and $F_{FIR}(q)$ respectively denote low-pass and finite impulse response (FIR) moving average filters. The FIR filter has window of one cycle, suppressing grid frequency terms and higher harmonics. The low-pass filter has cut off frequency near ω_c, suppressing high frequency terms. This combination of filters removes the grid frequency component of (1.5c) and removes (1.5b) entirely, leaving

$$P_{Vm}(t) = F(q)\frac{VI_h(\phi_m)}{2}e^{-\eta(t)}\cos(\omega_0 t - \beta(\phi_m)),$$

  where $F(q)$ denotes gain and delay effects of filtering. The phase terms ϕ_m are the respective voltage phases at time of transient, i.e. $\phi_a = \phi_s$, $\phi_b = \phi_s - \frac{2\pi}{3}$ and $\phi_c = \phi_s + \frac{2\pi}{3}$

- The $\frac{2\pi}{3}$ separation of phase terms ϕ_m makes the sum of demodulated power on all phases

equal zero. To overcome this, a novel use of Clarke transformation

$$\begin{bmatrix} P_{V\alpha} \\ P_{V\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{Va}(t) \\ P_{Vb}(t) \\ P_{Vc}(t) \end{bmatrix}$$

yields:

$$\begin{bmatrix} P_{V\alpha} \\ P_{V\beta} \end{bmatrix} = F(q)\frac{VI_h(t)}{2} e^{-\eta(t-t_s)} \cos(\omega_d t - \beta) \begin{bmatrix} \cos(\phi_s) \\ \sin(\phi_s) \end{bmatrix}$$

- Then the total demodulated power P_V is equal to the sum of orthogonal values $P_{V\alpha}$ and $P_{V\beta}$. The algorithm cancels the respective $\cos(\phi_s)$ and $\sin(\phi_s)$ terms of $P_{V\alpha}$ and $P_{V\beta}$, with trigonometric relation $\cos(\phi_s)^2 + \sin(\phi_s)^2 = 1$, using

$$|\cos(\phi_s)| = \sqrt{\frac{P_{V\alpha}^2}{P_{V\alpha}^2 + P_{V\beta}^2}}$$

and

$$|\sin(\phi_s)| = \sqrt{\frac{P_{V\beta}^2}{P_{V\alpha}^2 + P_{V\beta}^2}}$$

in

$$P_V = P_{V\alpha}\sqrt{\frac{P_{V\alpha}^2}{P_{V\alpha}^2 + P_{V\beta}^2}} + P_{V\beta}\sqrt{\frac{P_{V\beta}^2}{P_{V\alpha}^2 + P_{V\beta}^2}}.$$

The limitation of the method is that loss of sign due to squaring causes the algorithm to give proper demodulation only if $\cos(\phi_s)$ and $\sin(\phi_s)$ are positive, otherwise the demodulated power is inverted, has incorrect gain, or both. Figure 1.4 shows the demodulation in action given four different values for ϕ_s, along with the high-frequency sampled active power in the reference circuit that is being demodulated.

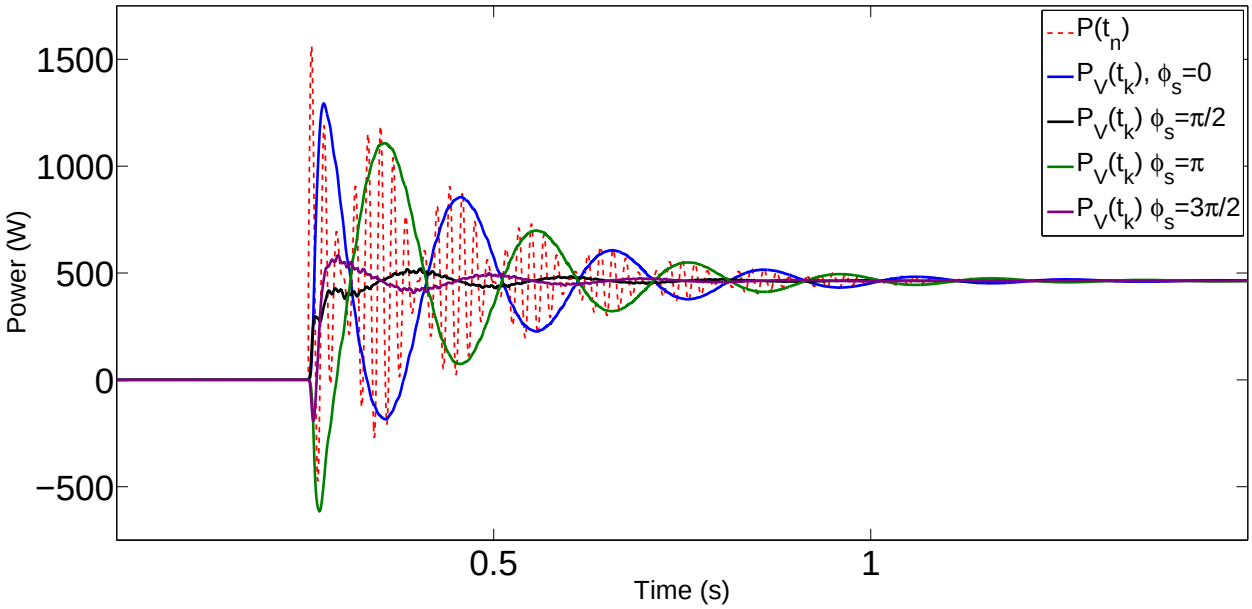

Figure 1.4: Three-phase reference circuit real power in response to switch closure at t_s=0.25s, with $P_V(t_k)$ subject to different voltage phase values at t_s.

1.3 Challenges

1.3.1 Harmonics

While inverter output response is extremely fast, there remain challenges. Implementation of control is usually done by digital filtering of measured power to adjust the power output signals sent to the inverter. This requires clean power measurements to be used for feedback, but current supplied by inverters is inherently non-sinusoidal. Most inverters parallel grid voltage with a square wave, modified sine wave or Pulse Width Modulation (PWM) [28]. These topologies lead to considerable harmonic distortion.

There are inverter designs that provide power with very good power quality. Multi-level inverter architectures have less harmonic distortion than those already mentioned [29], and active damping is a technique in which additional capacitors and resistors are rapidly switched in and out, resulting in suppression of harmonics [30], [31], [32]. However, interconnect standards in the United States are tolerant of harmonic distortion, creating minimal return on investment for the cost of implementation of these more sophisticated inverter designs.

Because of the preponderance of inverters with simpler architectures, this dissertation adopts and approach of distilling harmonic-laden signals into a clean signal useful for feedback control.

1.3.2 Signal Processing

Microprocessors are widely available but are optimized for data manipulation, display and communication rather than rapid, time-constrained calculations [33]. Because of its versatility, a microprocessor used for control may be multitasked with additional processes such as data manipulation for visualization or storage read/write operations. This can introduce jitter into the timing of the processor tasking, which becomes increasingly significant at higher data sample rates, and has traditionally limited the adoption of microprocessors for real time control [34].

Electric grids distribute power with voltage frequency f_c of 50 or 60 Hz. For the grid frequency to be apparent in data, the sample rate must be no less than $2f_c$. If the harmonics mentioned in the previous section are to be considered, sample rate may have to increase by an order of magnitude or more. Microprocessor jitter at this high sample rate could render the microprocessor ineffectual for signal processing, but does not preclude control at lower frequency. On the contrary, feasibility of microprocessor based control of a low frequency component of an electric grid transient is demonstrated in this dissertation. The signal processing necessary to provide the microprocessor a clean signal is a key innovation.

Discrete Digital Signal Processors (DSPs) are application specific integrated circuits (ASICs), designed to perform certain types of operations continuously and at very high frequency[33]. A limitation of DSPs is that they are constrained to a task or set of tasks without any customization available to the user. A field programmable gate array (FPGA) is an integrated circuit (IC) with many fundamental computing logic blocks such as adders, lookup tables and flip flops, with the main distinction from other ICs being configurable interconnects between these elements [35]. These interconnects allow the FPGA to be configured into prototype ASICs able to meet unique needs. The cost of this flexibility is that FPGAs are difficult to program, requiring a consider-

able knowledge base in a wide variety of computer engineering topics, including digital logic, data types and hardware level computing architecture. The research presented in this dissertation uses an FPGA for high frequency signal processing to filter harmonics and remove grid frequency components of an electric grid transient by demodulation, feeding the remaining low frequency component to an integrated microprocessor for disturbance rejection control.

1.3.3 Model development

Electric grids are very complex, highly integrated systems, in which interrelations between subsystems can be obscured by the shear number of loads, distribution lines, power sources, control apparatuses and simultaneously-occurring interactions [36]. Any attempt to gather all necessary parameters and map all relationships on a modern electric grid would be a monumental task. Were a model developed, many scenarios desired for analysis, such as faults resulting in protective action or branch trips would be difficult to validate due to utility customers' expectation of continuity of power.

System identification allows an input-output data-based approach to model development [37], that allows bypassing much of the painstaking work otherwise needed . In this dissertation, the clean signal provided by the FPGA mentioned in the previous section is used to create a system model that the controller implemented on the microprocessor uses to anticipate the evolution of an electric grid transient, adjusting inverter power output to correct it.

1.4 Problem Statement

The ability of a modern inverter to rapidly adjust active and reactive power output will be used to offset transient effects caused by connecting an inductive load to the electric grid. The inverter active and reactive power output will be adjusted using feedback control. Feedback control requires an input with much less harmonic distortion than found in active and reactive power supplied by an inverter, so power measurements must be filtered and demodulated. Demodulation

will use only locally available measurements, allowing the decentralized nature of droop control while avoiding limitations of synchrophasors. For feedback control to be effective, active and reactive power disturbances must be distinguishable in the demodulation, even if the measurements contain very high total harmonic distortion. Disturbance rejection control will be demonstrated in real-time on actual hardware.

The challenges to inverter based control of electric grid transients lay mostly in data acquisition and signal processing. With a clean signal for control, the effort resolves into a classic disturbance rejection problem.

For reproducibility, a grid-connected reference circuit is constructed with an inductive load that causes active and reactive power fluctuations when switched in. The test setup is completed with a controllable modern inverter and a controller consisting of an integrated FPGA/microprocessor packaged with current and voltage sensors and an input/output card for passing control signals to the inverter.

System identification is used for load and inverter model development, and the models are validated against circuit input-output data. Because system identification is used, any controller must be robust against model uncertainty inherent in system identification. The models serve as internal models for H_∞ and H_2 controllers, which are robust control schemes allowing loop shaping to achieve desired control performance. Robustness analysis is performed on the controllers, and simulation of disturbance rejection control is compared to live demonstration on the reference circuit.

1.5 Summary of Contributions

- Real Power Disturbance Rejection

  Robust control techniques leveraging the internal model principle are used to improve power system stability, providing damping and power transient mitigation to achieve disturbance rejection in Chapter 2. A three-phase active power disturbance is corrected in real-time using

feedback control of an inverter, demonstrating feasibility of the approach.

As mentioned, this design used a poorly formulated demodulation algorithm making results only intermittently reproducible. This motivates subsequent research.

- Open Loop Demodulation

  DC-AC inverters provide AC current that is inherently non-sinusoidal. Active and reactive power measurements may contain considerable harmonic distortion. This distortion may obscure transient effects of load switching. Costas Loop forms the basis of an algorithm presented in Chapter 5, which is used to demodulate power transients in spite of distortion. Additional discussion on the algorithm design process is provided Chapter 4. The algorithm provides a signal relatively free from harmonic distortion, suitable as input to a feedback controller.

- Reactive Power Disturbance Rejection

  Control using the signals provided by the algorithm described in Chapter 5 is presented in Chapter 6.

  System identification is used to formulate a model of load switching transient response as well as an inverter dynamic model. Due to uncertainty inherent in models developed via system identification, any control approach must be robust to model error. Robust control loop shaping techniques allow adjustment of control performance to limit amplification at certain frequencies, appropriate for minimizing fluctuations attendant to connecting a reactive load. Real-time reactive power disturbance rejection via inverter control is demonstrated.

Chapter 2

Disturbance Rejection of Real Power Flow by Grid-Tied Inverter

2.1 Introduction

A critical design consideration for an electrical grid is to maintain its stability, commonly defined as the balance between the consumption and generation [38]. Challenges arise due to power flow disturbances and fluctuations caused by possible contingencies in an electrical grid [39]. Although some of these disturbances are small, occasionally they are large enough to trigger system outage events [40].

Some of the major electrical grid collapses are attributed to lightly damped oscillations in power flow [41]. Conventionally, the rotational inertia used for power generation is used to stabilize the power flow through the system [9]. Emerging distribution systems with distributed energy resources (DER) challenge this paradigm, since Photovoltaics (PV), wind turbine, battery, and other DER are connected through inverters that do not have the benefit of the intrinsic stabilizing effect of the rotational inertia [42], [43].

The increased potential of instabilities attributed to heavy penetration of DER have been detected with experiments and motivate the research contributions of this chapter. As an example,

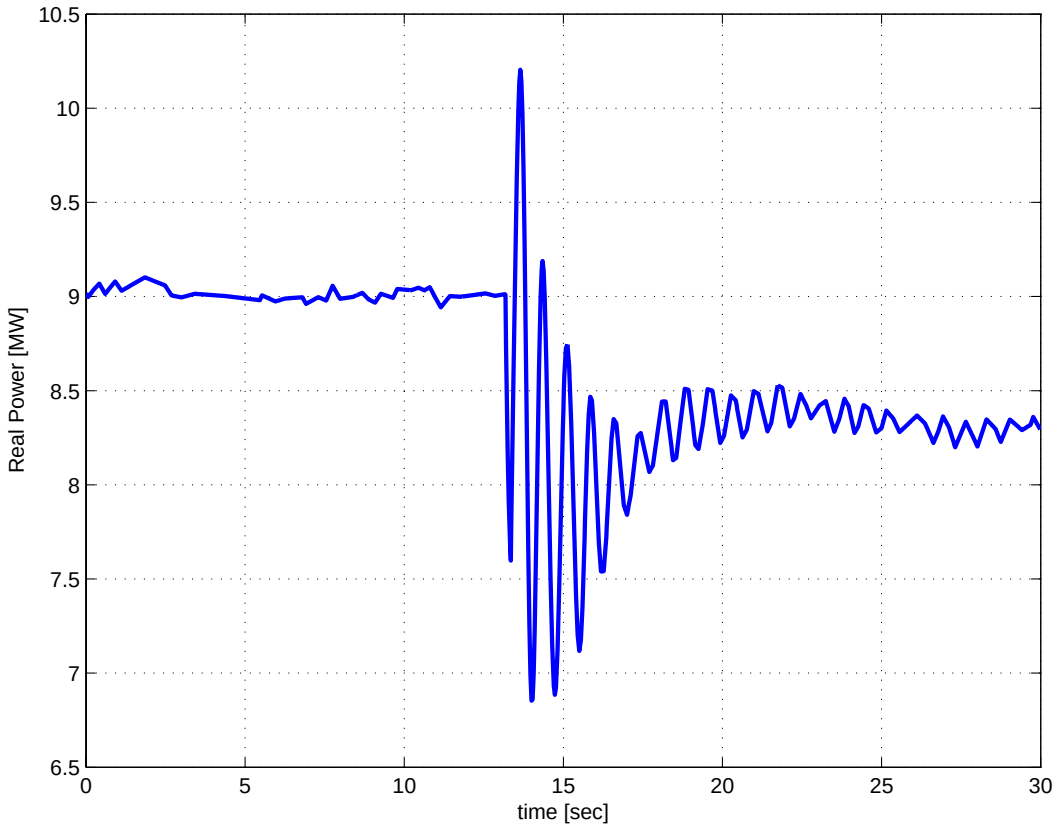

Figure 2.1: Measured power oscillations on the main 3-phase interconnection of the UCSD microgrid during an unanticipated step-wise load demand change.

a poorly damped power oscillation was observed on the three phase 12kV interconnection at the University of California, San Diego (UCSD) microgrid, as shown in Fig. 2.1. It was caused by an unanticipated load switching, whereas the real-time power measurement was recorded by a Phasor Measurement Unit (PMU).

Clearly, it is crucial to address volatile power oscillations in a distributed power generation system (DPGS). One possible approach is the use of a PMU to provide feedback information to control power oscillations with a fast inverter, as a PMU can be used to measure real-time power quality and power oscillations in a local electrical grid [44]. Currently, most inverters in distribution systems employ grid-tied control prescribed by IEEE 1547 standard. The improvement on stability of a DPGS has been studied with alternative solutions such as droop-controlled inverters [42], [45], but it is still of interest to enhance the capability of disturbance rejection by a grid-tied inverter (GTI).

The basic feature of a GTI is to control real power and reactive power while maintaining its synchronization with the grid voltage [43]. In a microgrid, the synchronization of local voltage needs to be properly controlled when switching between grid-tied and islanded modes [46], [47]. When operating in either grid-tied or islanded mode, the control of frequency or power flow of multiple GTIs are typically not linked [42]. Although rejection of real power fluctuations is of particular interest in this chapter, more factors need to be taken into account, especially the coupling between real power and reactive power, and the trade-off between power oscillations and current distortion [48].

The rejection of power flow perturbations and oscillations, collectively called 'disturbances' in the following, can be achieved through multiple control approaches. For instance, Chaudhuri et al. solve output disturbance rejection with respect to power system oscillations through a mixed-sensitivity based LMI approach [49]. Another group of design techniques is named Active Disturbance Rejection Control (ADRC) [50]. Chang et al. apply ADRC to improve the performance of a flywheel energy storage system (FESS) by estimating and compensating plant model uncertainties and unknown disturbances in real time [51]. Internal Model Control (IMC) is another kind of disturbance rejection controller structure employing an explicit model of the plant [52]. It has also been studied extensively in electric power components to solve disturbance rejection problems such as load frequency control [53], [54]. The listed three disturbance rejection controller design techniques above are well-known. They aim at solving general robust control problems [55], especially when the disturbance is uncertain or can only be estimated.

In most cases some *a priori* knowledge about the dynamic behavior of a disturbance may be available. For example, a load branch can be seen as a disturbance to the grid, and the dynamics of the loads contained in the branch may be modeled *a priori*. In this scenario, incorporation of a suitably (dynamic) model of a disturbance can be accomplished via the well-known internal model principle (IMP). The IMP states that a model of the disturbance is needed in the feedback path to regulate the output of a plant subjected to external deterministic disturbances [56]. Periodic external deterministic disturbances can be well rejected by repetitive control [57], which can be

viewed as an extension of IMP. But non-periodic external disturbances need to be dealt with by a general IMP-based controller. In particular, a general IMP-based controller consisting of both an internal model and a stabilizing feedback filter can be obtained through computations based on optimal control, utilizing the design freedom to meet additional control objectives [58], [59].

The H_∞ control framework can be utilized to compute a general IMP-based controller and allows (robust) control objectives to be specified as a maximum gain over frequencies [60]. However, the (battery) energy used to mitigate power oscillations with a controllable inverter, motivates the use of minimum variance or an H_2 optimal control framework. As a result, the approach of an IMP-based H_2 optimal controller is used in this chapter to reject power disturbance caused by an uncontrollable load.

With the development of emerging measurement technology (PMU) and power electronics technology (smart inverter), the IMP-based optimal H_2 controller algorithm enables feedback control in the scope of a microgrid [44], [20], [61]. An experimental setup with a commercial smart inverter is created in order to validate the control algorithm through on/off switching of a dynamic load. Despite noisy observations of power flow, the experimental results indicate the feasibility of the proposed controller for real-time mitigation of power oscillations.

The remainder of this chapter is organized as follows. First, the disturbance rejection control design problem is described in Section II, followed by a description of the experimental setup in Section III. The experimental validation of the disturbance rejection controller is presented in Section IV and the chapter ends with conclusions in Section V.

2.2 Disturbance Rejection Control Design

2.2.1 Problem Formulation

In typical local electric grids, multiple parallel branches are connected to the utility grid at the Point of Common Coupling (PCC) [62], [63]. A branch can be either a pure load or a combination of a DPGS and a (dynamic) load. In this chapter, a simplified branch with a single

DPGS and a single (dynamic) load shown in Fig. 2.2 is studied for the purpose of power flow disturbance mitigation.

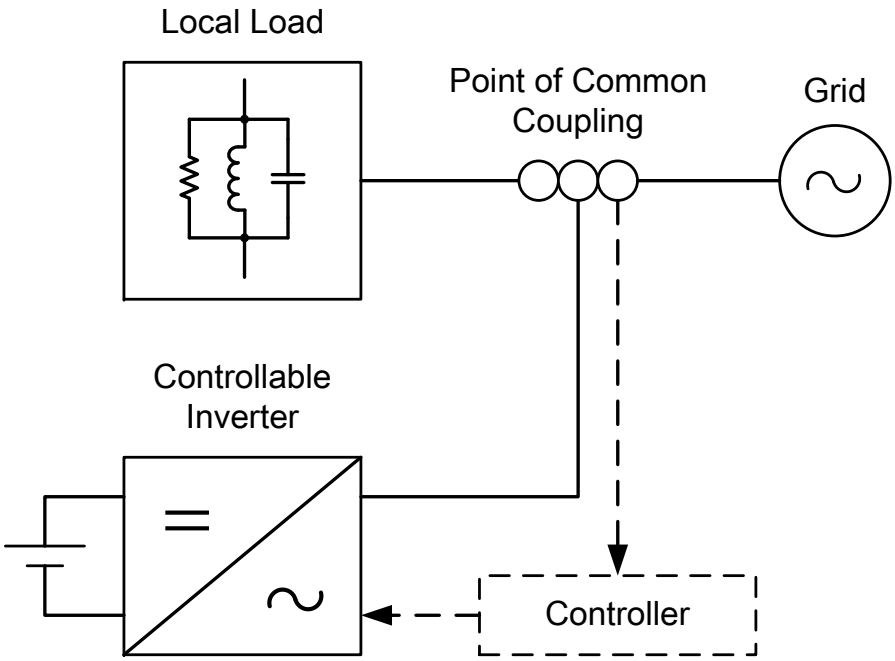

Figure 2.2: Diagram of a local branch consisting of a grid-tied controllable DPGS and a load.

While Fig. 2.2 shows the flow of power through the electric connection of the DPGS and load connected to the grid, the schematic diagram of Fig. 2.3 shows the information flow for the purpose of control. The controller depicted in Fig. 2.2 is now represented by C in Fig. 2.3 and the real power at the PCC is given by

$$P_k^{\text{GRID}} = P_k^{\text{LOAD}} + P_k^{\text{GTI}}, \tag{2.1}$$

as a sum of real power produced/consumed by the DPGS and the real power consumed by the unanticipated load switching.

Referring to the schematic representation of Fig. 2.3, the control objective is to reject the disturbance of real power introduced by the uncontrollable part of the branch. The unanticipated load switching is observed by real-time feedback measurements of power flow at the PCC. In other

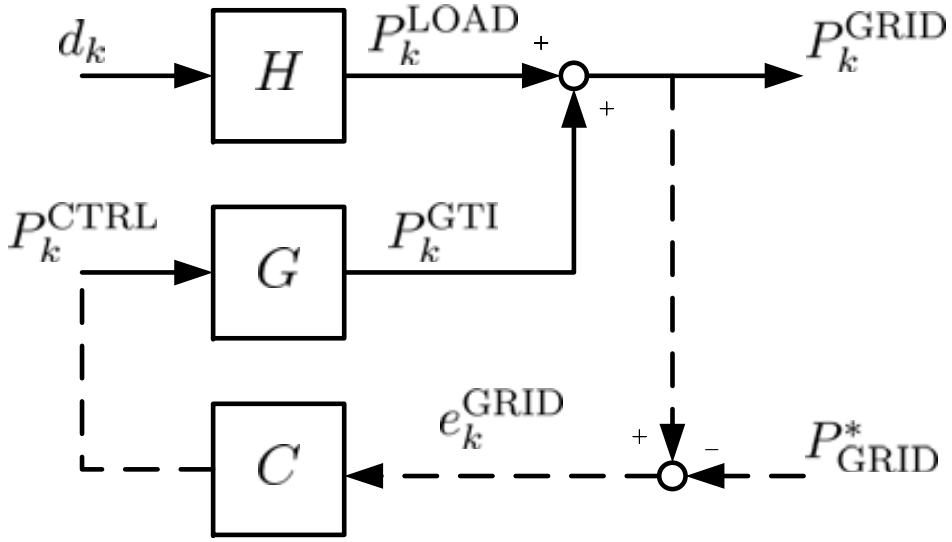

Figure 2.3: Control diagram of the study system.

words, the objective is to minimize the (weighted/filtered) error

$$e_k^{\mathrm{GRID}} = P_k^{\mathrm{GRID}} - P^*_{\mathrm{GRID}} \tag{2.2}$$

when the unanticipated load switching occurs, where P^*_{GRID} is the desired set point for the power flow at the PCC.

2.2.2 Modeling of System Dynamics

For the purpose of the control design, it is assumed that a dynamic disturbance model $\hat{H}$ for H is known. The filter H in Fig. 2.3 represents the dynamics of the power disturbance $P_k^{\mathrm{LOAD}} = Hd_k$ where d_k is an impulse input. Similarly, it is assumed that a dynamic actuator model $\hat{G}$ for G is known. The filter G represents the inverter/microgrid dynamics from the inverter demand input P_k^{CTRL} to the power flow at the PCC P_k^{GTI}. Without going into further details, it is worth noting that these models $\hat{H}$ and $\hat{G}$ can be estimated by utilizing either the step-based realization algorithm (SBRA) [27], [64] or other methods for model estimation based on the measured data obtained by open-loop dynamic tests [37].

2.2.3 Disturbance Rejection Controller Design

The aim of the controller design is to reject known disturbances and also to find an acceptable balance in the trade-off between mitigating the output fluctuation caused by disturbance and required energy produced by the inverter(s). Therefore, an IMP-based optimal controller is computed on the basis of an H_2 control design to formulate an optimal control algorithm. It allows use of an internal model filter and weighting filters on closed-loop transfer functions to compute an optimal controller [58], [65]. The control design can be further explained by the block diagram of the closed-loop system depicted as in Fig. 2.4. Without loss of generality, the power set point at the PCC is set to zero for the design.

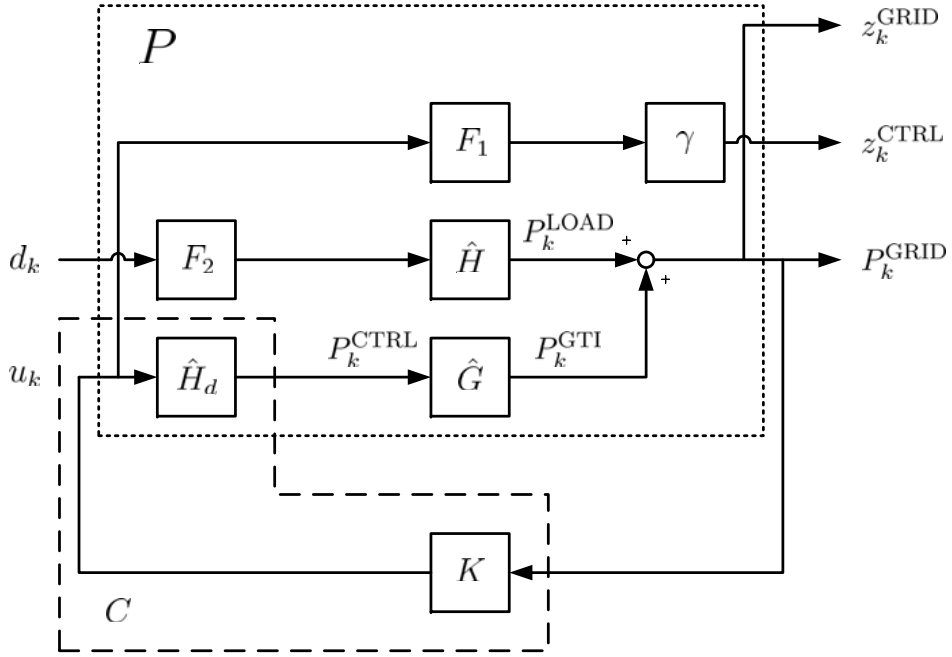

Figure 2.4: Block diagram of the closed loop system with internal model $\hat{H}_d$ in the feedback path during control design.

To obtain an H_2 controller, the system is formulated in a standard state-space form:

$$\begin{bmatrix} z_k^{\mathrm{GRID}} \\ z_k^{\mathrm{CTRL}} \\ P_k^{\mathrm{GRID}} \end{bmatrix} = \begin{bmatrix} \hat{H} \cdot F_2 & \hat{G} \cdot \hat{H}_d \\ 0 & \gamma F_1 \\ \hat{H} \cdot F_2 & \hat{G} \cdot \hat{H}_d \end{bmatrix} \begin{bmatrix} d_k \\ u_k \end{bmatrix}, \tag{2.3}$$

where $\hat{G}$ and $\hat{H}$ are actuator and disturbance models, respectively. The filter $\hat{H}_d$, which is utilized as the internal model, is a modified disturbance model that only contains the poles of $\hat{H}$ to represent the information on the free response (oscillations and off-set) of the disturbance.

Additional filters on control signals or closed-loop transfer functions are used to shape the control design. Within this context, F_1 is designed as a high-pass filter on the control signal that assists in limiting the high frequency contributions and finding a stable, stabilizing (strong stabilization) feedback controller. The filter F_2 is a low-pass filter that helps the achieved controller focus on attenuating oscillations at low frequencies. Finally, the scaler γ is an adjustable weighting scalar to provide a trade off between controller performance and the size of the control signals. The control is computed via

$$K^* = \arg \min_K \begin{matrix} T_{z_k^{\text{CTRL}} d_k} \\ T_{z_k^{\text{GRID}} d_k} \end{matrix}_2, \tag{2.4}$$

where $T_{z_k^{\text{CTRL}} d_k}$ and $T_{z_k^{\text{GRID}} d_k}$ are the transfer functions from d_k to z_k^{CTRL} and z_k^{GRID}, respectively. For computation of K^*, the dynamics is consolidated in a state-space model

$$\begin{bmatrix} z_k \\ P_k^{\text{GRID}} \end{bmatrix} = \left[\begin{array}{c|cc} A & B_1 & B_2 \\ \hline C_1 & D_{11} & D_{12} \\ C_2 & D_{21} & D_{22} \end{array}\right] \begin{bmatrix} d_k \\ u_k \end{bmatrix}, \tag{2.5}$$

where $z_k = \begin{bmatrix} z_k^{\text{GRID}} & z_k^{\text{CTRL}} \end{bmatrix}^T$, and K^* is computed by standard H_2 optimal control design approaches such as the LQG procedure [55], [66].

2.2.4 Order Reduction of Controller

The process of developing the filters for the mixed sensitivity problem results in a controller of high-order, having suffered from an 'inflation of states'. Therefore, a proper order reduction of the obtained controller is needed and performed as follows. A balanced realization C_{bal} of controller C with controllability and observability grammians W_c and W_o is found by comput-

ing similarity transformation matrix T such that the transformed controllability and observability grammians

$$\overline{W_c} = TW_cT^T \text{ and } \overline{W_o} = T^{-T}W_oT^{-1} \tag{2.6}$$

are equal and diagonal.

The values on the diagonal of $\overline{W_c}$ form a vector of the Hankel singular values in descending magnitude. The singular values with much less magnitude than that of the greatest singular value correspond with the order of the controller to be reduced. The reduced-order controller is calculated by taking state space form of C_{bal}:

$$\begin{aligned} \begin{bmatrix} x_{k+1}^{c1} \\ x_{k+1}^{c2} \end{bmatrix} &= \begin{bmatrix} A_{c11} & A_{c12} \\ A_{c21} & A_{c22} \end{bmatrix} \begin{bmatrix} x_k^{c1} \\ x_k^{c2} \end{bmatrix} + \begin{bmatrix} B_{c1} \\ B_{c2} \end{bmatrix} u \\ y_k^c &= \begin{bmatrix} C_{c1} & C_{c2} \end{bmatrix} \begin{bmatrix} x_k^{c1} \\ x_k^{c2} \end{bmatrix} + D_c u \end{aligned} \tag{2.7}$$

and assuming the states to be eliminated, x^{c2}, are unchanging ($x_{k+1}^{c2} = x_k^{c2}$). This makes

$$x_k^{c2} = (I - A_{c22})^{-1}A_{c21}x_k^{c1} + (I - A_{c22})^{-1}B_{c2}u \tag{2.8}$$

and the reduced-order system C_{red} is given in the state space format

$$\begin{aligned} x_{k+1}^{c1} =& (A_{c11} + A_{c12}(I - A_{c22})^{-1}A_{c21})x_k^{c1} \\ &+ (B_{c1} + A_{c12}(I - A_{c22})^{-1}B_{c2})u \\ y_k^c =& (C_{c1} + C_{c2}(I - A_{c22})^{-1}A_{c21})x_k^{c1} \\ &+ (D_c + C_{c2}(I - A_{c22})^{-1}B_{c2})u. \end{aligned} \tag{2.9}$$

2.2.5 Robustness Analysis

Performing a robustness analysis characterizes the capability of a given (reduced-order) controller C_{red} to handle uncertainty or modeling errors in either the disturbance model $\hat{H}$ or the actuator model $\hat{G}$. There are numerous ways to construct the uncertainty of a model [55]. In this chapter a frequency-dependent unknown dynamics is applied to characterize the uncertainty. With an inherently stable actuator model $\hat{G}$, an additive uncertainty

$$\tilde{G} = \hat{G} + W_G \Delta, \quad \|\Delta\|_\infty < 1 \tag{2.10}$$

with a stable filter W_G can be used to describe actuator model errors. Application of the small gain theorem

$$\left\| \frac{W_G C_{red}}{1 + \hat{G} C_{red}} \right\|_\infty < 1$$

can be used to verify stability robustness of the reduced-order controller C_{red}.

2.3 Experimental Setup

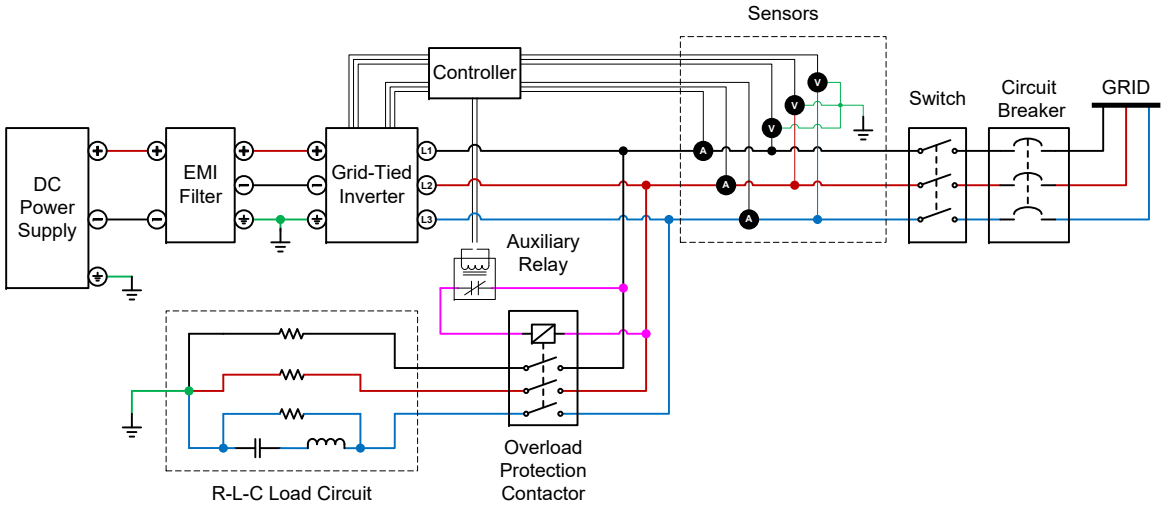

Figure 2.5: Diagram of experimental setup. An R-L-C load circuit can be energized or de-energized by a contactor. The voltage and current sensors are placed at the grid side of the experimental setup.

An experimental setup is built to produce a power disturbance qualitatively similar in terms of frequency to that shown earlier in Fig. 2.1. For that purpose, the circuit topology of Fig. 2.5 is built into an experimental setup with a commercial GTI. For testing purposes, a 10kW programmable DC power source substitutes as the DER. The commercial GTI is a GTI3100A6208/ 3652IR-PQ of One-Cycle Control Inc. and equipped with four-quadrant power control. Additional EMI filters FN2200B are placed between the DC source and the inverter to eliminate the effect of common mode current. The output of the inverter is connected to the grid through a three-phase switch with a circuit breaker for over-current protection.

A three-phase load circuit is designed and integrated into the test bed to act as the source of a power disturbance. As depicted in Fig. 2.5, one phase is composed by a bypass resistor of 100 Ω that is in parallel with a series connection of a capacitor of 0.01 F and an inductor of 0.1 H, while the rest two phases have only bypass resistors of 100 Ω. The Inductor-Capacitor (LC) circuit was designed to generate a resonance; the bypass resistor consumes real power and also discharges the LC circuit when not energized. The circuit is connected to the output of the grid-tied inverter through an overload protection relay.

A National Instruments (NI) myRIO embedded device is integrated into the test bed for data acquisition and controlling the GTI. Three-phase AC voltage and current signals at PCC are conditioned and measured by the myRIO, which acts the function of a PMU in this experimental setup. The embedded device also computes the control signals that are sent via a current loop circuit to drive the GTI. The load circuit of the system is energizing the overload protection contactor via an auxiliary relay.

2.4 Experimental Validation of Disturbance Rejection Control

Based on the measured data obtained in initial open-loop tests, a 4th-order disturbance model $\hat{H}$ is estimated by SBRA; and a 2nd-order output error (OE) model is utilized to capture the dynamics of GTI. which is the actuator model $\hat{G}$. The identified models are validated by a step

respeonse experiment shown in Fig. 2.6.

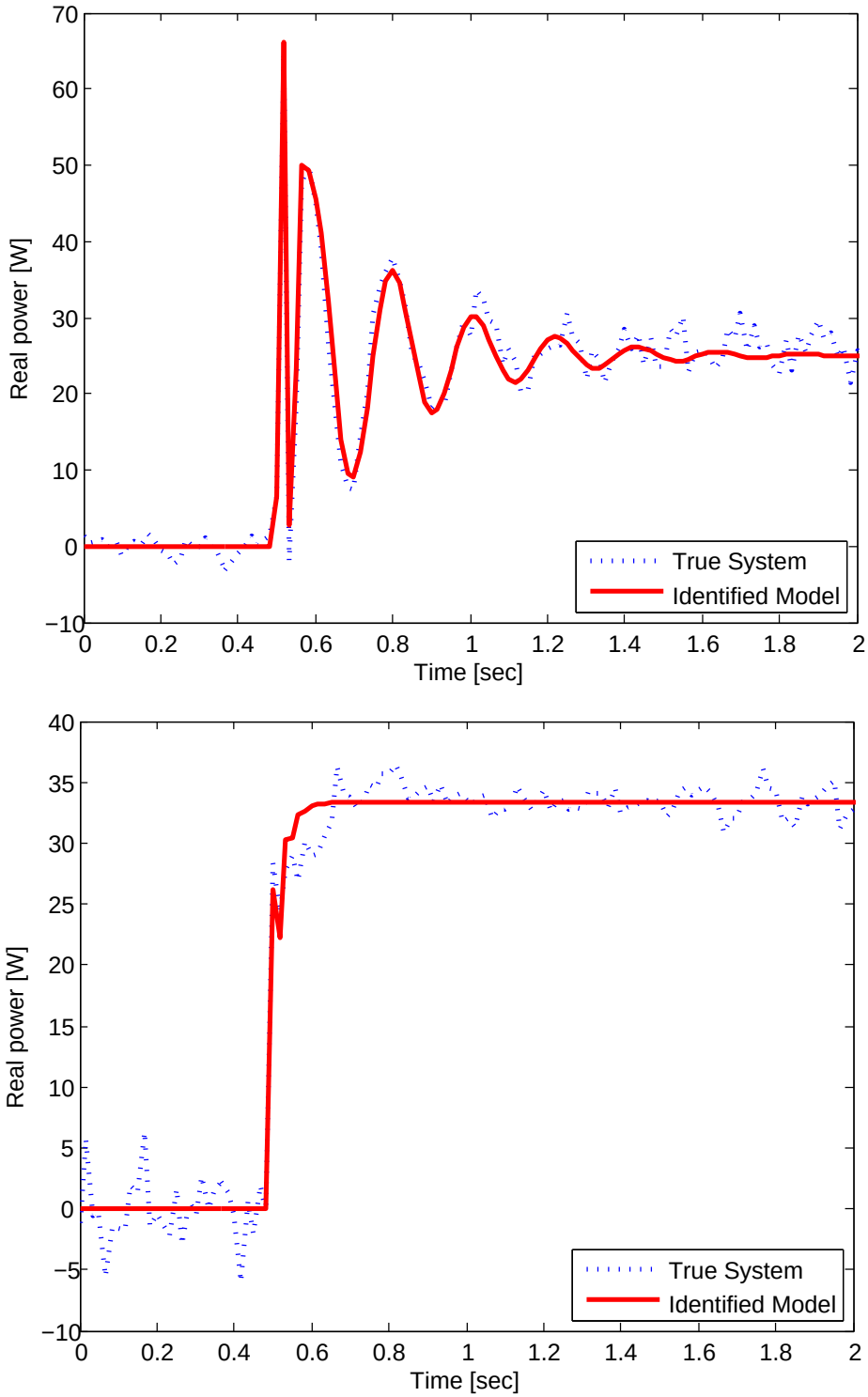

Figure 2.6: Validation of identified models: Top Disturbance model $\hat{H}$; bottom Actuator model $\hat{G}$.

For the control design, the weighting function F_1 is a 2nd-order high-pass filter with a

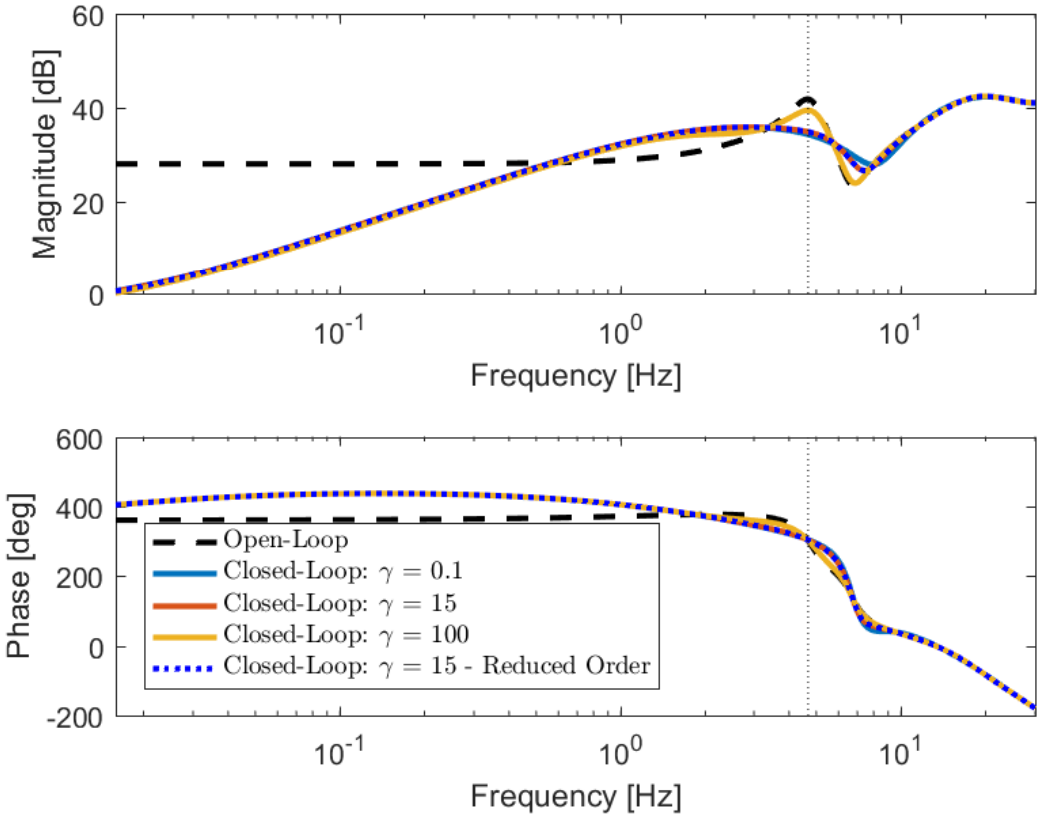

Figure 2.7: Sensitivity of the open-loop and closed-loop systems.

cut-off frequency of 5 Hz to lower the effect of integrator in control input. The filter $F_2 \cdot \hat{H}$ forms a re-shaped disturbance model including oscillations and offset. The scalar control gain γ is tuned in order to obtain a stable H_2 controller with desired performance. The resulting error rejection functions $1/(1 + C\hat{G})$ for $\gamma = 0.1, 15, 100$ are shown as in Fig. 2.7. When $\gamma = 100$ the magnitude attenuation at the oscillation frequency is not quite significant; while for $\gamma = 0.1$ the resulting attenuation at approximately 8 Hz is lower. Therefore the resulting controller with $\gamma = 15$ is selected for the final control design. Through the order reduction technique introduced in Section 2.2.4, a reduced-order controller is obtained and Fig. 2.7 also shows the error rejection function for the reduced order controller.

It can be observed from Fig. 2.7 that the open-loop (uncontrolled) disturbance model exhibits a resonance mode at approximately 4.7Hz and a DC-gain of approximately 30dB. The res-

onance mode models the oscillation dynamics whereas the DC-gain model the offset of the disturbance. It can also be observed from Fig. 2.7 that the closed-loop system with either C or C_{red} designed with $\gamma = 15$ eliminates the offset introduced by the disturbance and also dampens the oscillations of the disturbance at 4.7 Hz. The simulated step response of the error term e_k^{GRID} given in (2.2) also validates these observations and is shown in Fig. 2.8.

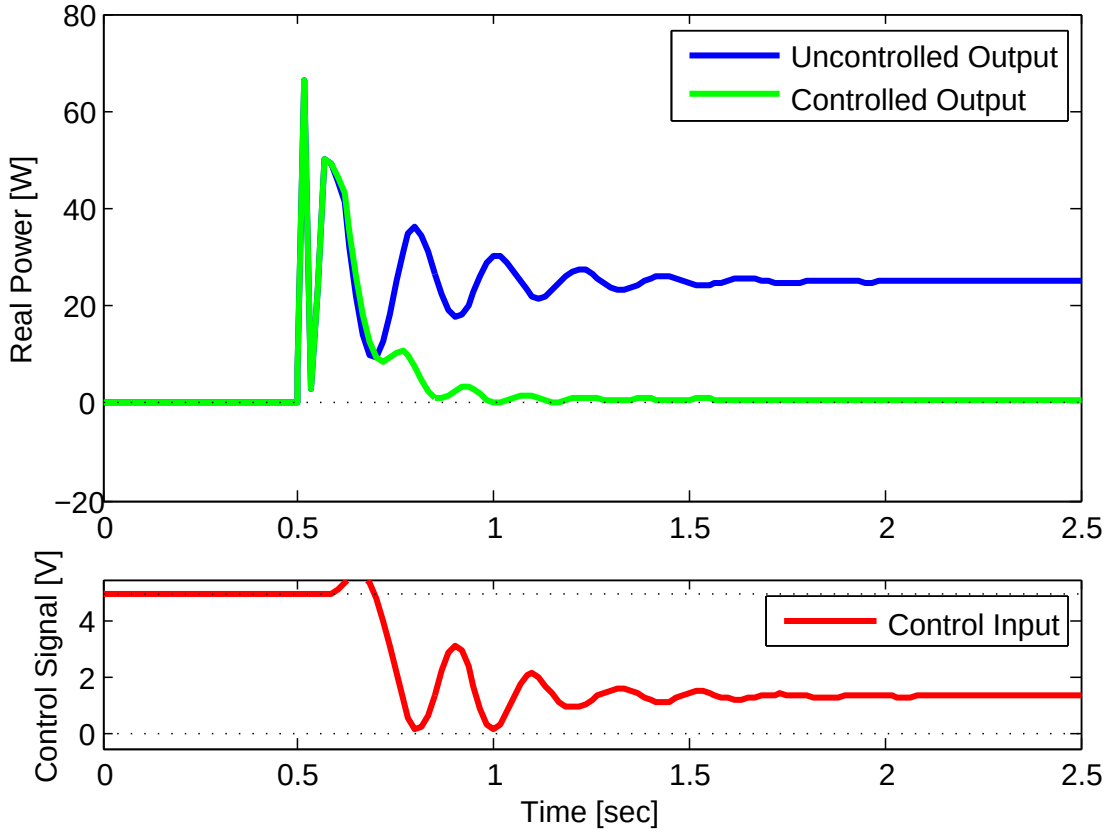

Figure 2.8: Simulation results of the error response of e_k^{GRID} due to a power disturbance in either the open-loop (uncontrolled) or closed-loop (controlled) power system.

For the actual experimental verification of the proposed power disturbance mitigation, the control algorithm is implemented on the myRIO embedded system and three phase on/off load switching are carried out with the experimental setup. As illustrated in Fig. 2.9, the designed controller is able to reject the disturbance by tracking the set point and also dampen the oscillations caused by the load switching. The actual control performance is limited by the control resolution of the high-power GTI used in the test setup.

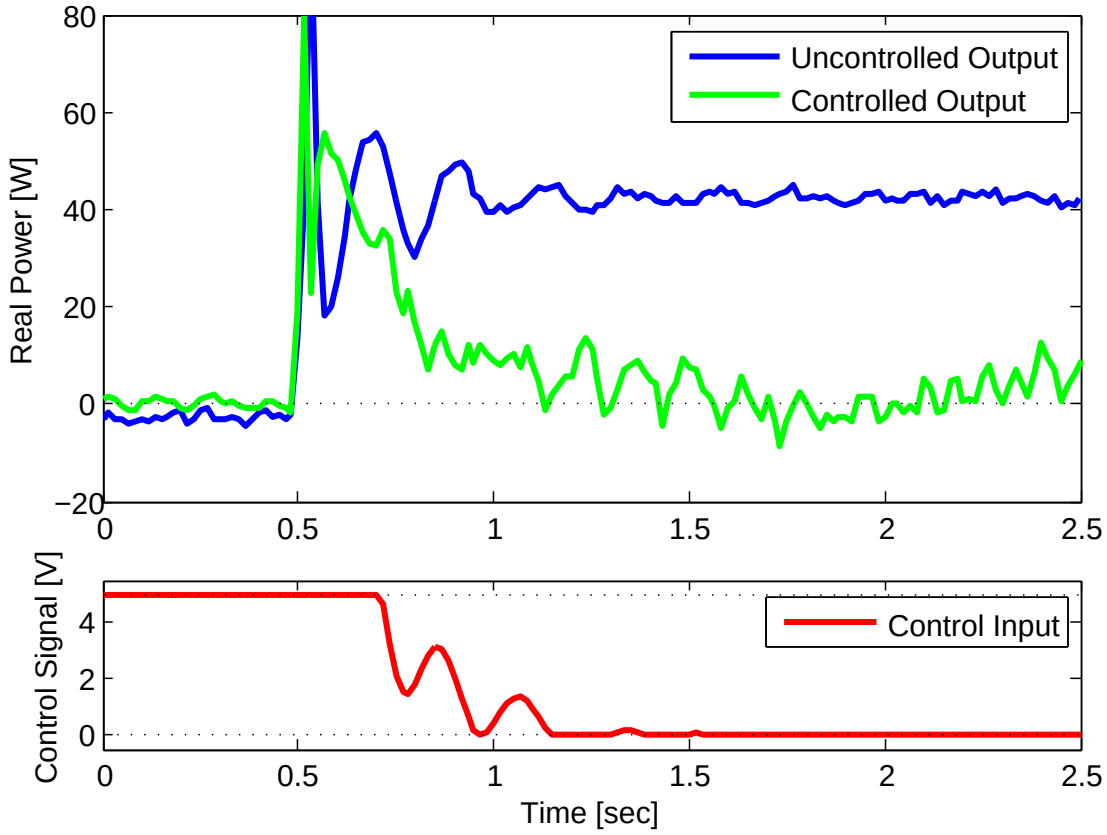

Figure 2.9: Experimental results of the error response of e_k^{GRID} due to a power disturbance in either the open-loop (uncontrolled) or closed-loop (controlled) power system.

2.5 Conclusions

Optimal real power disturbance mitigation has been formulated by a three-phase real power controller that uses the internal-model-principle to reduce power oscillations and mitigate steady-state power disturbances. The numerical values of the controller are found by an H_2 optimal formulation and designed to operate with a grid-tied inverter in order to reject power disturbance created by a dynamic load in an electrical grid. Experimental results verify the proposed control algorithm to mitigate both steady state and oscillations in real power fluctuations. Factors that may affect the disturbance rejection control need to be taken into account in the future research, e.g. the coupling between real power and reactive power and the trade-off between power oscillations and current distortion.

ACKNOWLEDGMENTS

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This chapter contains a reprint of the material as it appears in ”Xin Zhao, Benjamin T. Gwynn, Raymond A. de Callafon, and William Torre, Disturbance Rejection of Real Power Flow by Grid-Tied Inverter.” The dissertation author is the secondary author of the article. Additional original discussion is added at the end of the chapter to contextualize findings within the dissertation.

2.6 Author's Note

The author took a leave of absence to attend to a family matter during the time between the development of the demodulation method discussed in Chapter 1 and initial efforts at active power control. Upon return from leave of absence the author was referred to [27], and encouraged to assist with authoring a manuscript describing initial control efforts presented in this chapter. At the time of publication, the author was not aware of the limitations of the demodulation method presented in [27] nor the selective presentation of results in [67], which became the basis of this chapter. The author asserts that in spite of the restricted reproducibility of results in this chapter, the controller design process presented is sound, and that the limitations are purely due to the demodulation algorithm discussed in Chapter 1 and load construction, which is discussed at length in Chapter 3. Emphasis on the importance of consistently reproducible results will be made throughout this dissertation because of the intermittent reproducibility of the control results presented in this chapter, as this limitation motivated the author in subsequent research.

Chapter 3

Power Transients and the Problem with Reproducibility

Modern electric grids are expansive systems consisting of multitudes of power sources, loads, and sprawling interconnections. They are subject to ongoing reconfiguration and upgrades, and grid customers pay for power to be available when needed, precluding any testing that might interrupt service [36]. Because of their complexity and requirements for continuity of operation, computer simulations are a preferred medium for analysis of electric grids, but the same reasons can make validation of computer models difficult: a model may be fit to transient data, but if the transient resulted in loss of power it will not be deliberately repeated.

A grid-connected circuit with transient effects qualitatively similar to those seen on electric grids, but with circuit parameters selected to avoid protective actions that might disturb neighboring grid customers serves as a reference circuit. The reference circuit will enable reproducible testing while facilitating validation of computer models.

Chapter 2 presented a robust control design process allowing rapid adjustment of a DC-AC inverter active power output to mitigate a power transient caused by connection of the reference circuit. The results were only sporadically reproducible because of the reliance on the demodulation algorithm discussed in Chapter 1, as well as use of an unbalanced implementation of the

v	120V RMS AC at 60Hz
R_1	100 Ω s
R_2	2 Ω
L	.1 H
C	.01 F

Table 3.1: Reference Circuit Parameters

reference circuit. Unfortunately, the current response in a particular phase of a load connecting to an AC electric grid varies depending on the phase of grid voltage at the time of connection.

This chapter solves the ordinary differential equation describing current in the reference circuit, extends that analysis into active power, and then considers a balanced, three-phase architecture for the reference circuit as solution to the issue of reproducibility of reference circuit power dynamic response. The chapter concludes with discussion on how to address the timing limitations of a microprocessor caused by harmonics and high frequency components of power signals, to allow use of a microprocessor to serve control commands to a modern DC-AC inverter.

3.1 Reference Circuit and Governing Equations

3.1.1 Reference Circuit

Accepting that any distribution electric grid of reasonable size will have a combination of inductive, capacitive and resistive elements, a series RLC circuit presents a starting point for analysis of circuit power during a transient. RLC circuits are well known for their oscillatory behavior [68]. The circuit depicted in Fig. 3.1 is an RLC load that causes active and reactive power oscillations when energized. The inclusion of a purely resistive branch increases the active power at steady state, allowing a realistic scenario in which an attempt at disturbance rejection control might aim to return power to pre-transient levels in addition to minimizing fluctuations.

A physical implementation of the reference circuit was constructed in three-phase wye-configuration. The RLC branch is comprised of thirty-seven 270μF Aluminum Electrolytic capacitors per phase, wired in parallel to form the 0.01H Capacitive elements, in series with 0.1H

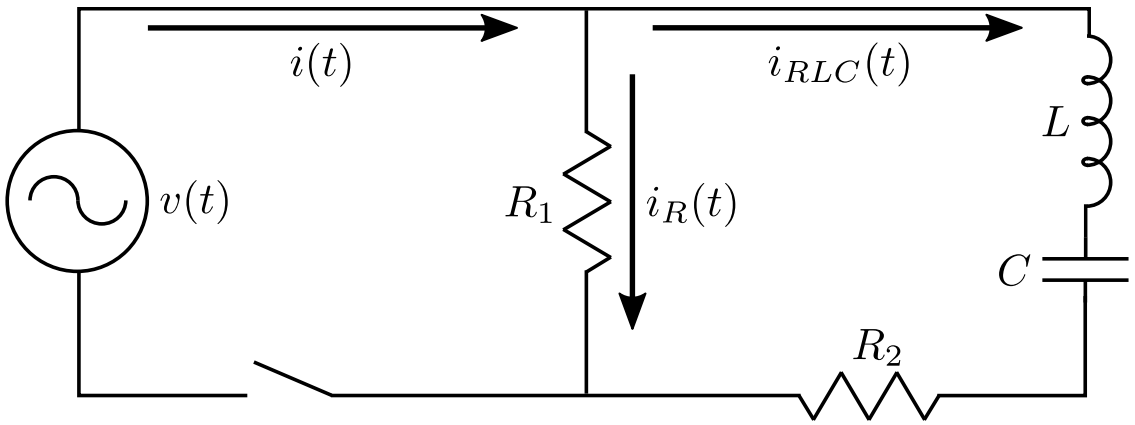

Figure 3.1: Reference circuit.

inductors. 2Ω resistors represent resistance of the wiring and circuit contacts. An additional benefit of the 100Ω resistor placed parallel to the RLC branch is creation of a path allowing energy discharge when the switch is open. The load circuitry is isolated from the utility power by a relay actuated switch. A Grid Tied Inverter is connected parallel to the utility 110 VAC, 60Hz power source.

3.1.2 Circuit Physics

The following discussion applies to $t \geq t_s$, where t_s denotes the time of switch closure, and is set $t_s = 0$ for simplicity. By Kirchoff's current law, total current is equal to the sum of branch currents:

$$i(t) = i_{RLC}(t) + i_R(t). \tag{3.1}$$

Applying Kirchoff's voltage law, the voltage across resister R_1 is equal to $-v(t)$; current through the resistive branch $i_R(t)$ is governed by Ohm's law $v(t) = i_r(t)R_1$ and will not be discussed further.

Current through the reactive branch $i_{RLC}(t)$ is governed by ordinary differential equation (ODE)

$$v(t) = L\frac{d}{dt}i_{RLC}(t) + R_2 i_{RLC}(t) + \frac{1}{C}q_e(t), \tag{3.2}$$

where the charge on the capacitor $q_e(t)$ is related to current by $i_{RLC}(t) = \frac{d}{dt}q_e(t)$.

Then, in terms of charge, the ODE is

$$v(t) = L\frac{d^2}{dt}q_e(t) + R_2\frac{d}{dt}q_e(t) + \frac{1}{C}q_e(t). \tag{3.3}$$

By differentiating with respect to time we can substitute $i_{RLC}(t) = \frac{d}{dt}q_e(t)$ and put the ODE it in terms of current:

$$\frac{d}{dt}v(t) = L\frac{d^2}{dt}i_{RLC}(t) + R_2\frac{d}{dt}i_{RLC}(t) + \frac{1}{C}i_{RLC}(t). \tag{3.4}$$

Voltage is given by $v(t) = V\cos(w_c t - \phi_s))$, where V is amplitude, ω_c is the angular frequency, and ϕ_s is the phase of the voltage signal at the time of switch closure. This definition of voltage is differentiated easily, resulting in second order ODE with forcing function:

$$-V\omega_c\sin(w_c t - \phi_s) = L\frac{d^2}{dt}i_{RLC}(t) + R_2\frac{d}{dt}i_{RLC}(t) + \frac{1}{C}i_{RLC}(t). \tag{3.5}$$

3.1.3 Particular Solution

A well known approach to finding the particular solution of a differential equation of this form is to assume the solution $i_p(t)$ to be similar to the forcing function, a sinusoid with amplitude I_p and phase α to be determined [69]: $i_p(t) = I_p\cos(\omega_c(t)-\alpha)$. Then, $\frac{d}{dt}i_p(t) = -\omega_c I_p\sin(\omega_c t-\alpha)$ and $\frac{d^2}{dt}i_p(t) = -\omega_c^2 I_p\cos(\omega_c t - \alpha)$, which can be substituted into (3.5):

$$-V\omega_c\sin(w_c t - \phi_s) = -L\omega_c^2 I_p\cos(\omega_c t - \alpha) - R_2\omega_c I_p\sin(\omega_c t - \alpha) + \frac{1}{C}I_p\cos(\omega_c(t) - \alpha). \tag{3.6}$$

Recognizing that the left hand side of (3.6) can be written as $-V\omega_c\sin(w_c t - \phi_s + \alpha - \alpha)$, angle-sum trigonometric identity

$$\sin(\theta_1 + \theta_2) = \sin(\theta_1)\cos(\theta_2) + \cos(\theta_1)\sin(\theta_2) \tag{3.7}$$

allows equation (3.6) to be written as

$$\begin{aligned}&-V\omega_c[\sin(w_c t-\alpha)\cos(\alpha-\phi_s)+\cos(w_c t-\alpha)\sin(\alpha-\phi_s)]\\&=[\frac{1}{C}I_p-L\omega_c^2 I_p]\cos(\omega_c t-\alpha)-R_2\omega_c I_p\sin(\omega_c t-\alpha).\end{aligned}\tag{3.8}$$

Unknown parameters I_p and α are determined by matching coefficients of $\cos(\omega_c(t)-\alpha)$ and $\sin(\omega_c(t)-\alpha)$ on each side of the equality of (3.8):

$$V\omega_c\sin(\alpha-\phi_s)=[L\omega_c^2-\frac{1}{C}]I_p \tag{3.9a}$$

$$V\omega_c\cos(\alpha-\phi_s)=R_2\omega_c I_p. \tag{3.9b}$$

Defining $\psi=\alpha-\phi_s$, then dividing (3.9b) by (3.9a) gives

$$\begin{aligned}\psi&=\tan^{-1}\left[\frac{L\omega_c^2-\frac{1}{C}}{R_2\omega_c}\right],\text{ or}\\\alpha&=\tan^{-1}\left[\frac{L\omega_c^2-\frac{1}{C}}{R_2\omega_c}\right]+\phi_s.\end{aligned}\tag{3.10}$$

A brief discussion is merited here, as (3.10) holds for $-\frac{\pi}{2}\leq\psi\leq\frac{\pi}{2}$ only. A quick analysis reveals that this condition is satisfied for the reference circuit, as it is comprised only of loads, and current leading or lagging more than $\frac{\pi}{2}$ radians is only possible if there is a net active power being added to the circuit.

Determination of I_p requires careful consideration as well: Squaring (3.9b) and (3.9a) and summing gives

$$(V\omega_c)^2[\sin^2(\alpha-\phi_s)+\cos^2(\alpha-\phi_s)]=I_p^2[(L\omega_c^2-\frac{1}{C})^2+(R_2\omega_c)^2]. \tag{3.11}$$

Applying trigonometric identity $\sin^2(\theta)+\cos^2(\theta)=1$ and taking square root gives:

$$I_p=\frac{V\omega_c}{\sqrt{(L\omega_c^2-\frac{1}{C})^2+(R_2\omega_c)^2}}, \tag{3.12}$$

where the positive value of the square root is accepted, because a negative current amplitude is equivalent to lead/lag greater than $\frac{\pi}{2}$.

Then, the assumed solution can be written $i_p(t) = I_p \cos(\omega_c(t) - \psi - \phi_s)$, confirming what might have been intuited, that at steady state, current will have constant amplitude I_p and phase which differs from that of voltage by constant parameter ψ, irrespective of the phase of voltage at time of switch closure ϕ_s.

3.1.4 Homogeneous Solution

The complementary homogeneous equation to (3.5) is

$$\frac{d^2}{dt} i_{RLC}(t) + \frac{R_2}{L} \frac{d}{dt} i_{RLC}(t) + \frac{1}{LC} i_{RLC}(t) = 0. \tag{3.13}$$

Defining damping factor $\eta = R_2/2L$, and natural frequency $\omega_n^2 = 1/LC$, then prospective solution $i_h(t) = e^{rt}$ has auxiliary equation

$$r^2 + 2\eta r + \omega_n^2 = 0, \tag{3.14}$$

with solutions

$$\begin{aligned} r &= -\eta \pm \sqrt{\eta^2 - \omega_n^2}, \text{ or.} \\ r &= -\eta \pm j\omega_0 \end{aligned} \tag{3.15}$$

where it is recognizing the reference circuit is underdamped by design and thus defining damped resonant frequency $j\omega_0 = \sqrt{\eta^2 - \omega_n^2}$.

Then,

$$i_h(t) = A_1 e^{(-\eta + j\omega_0)t} + A_2 e^{(-\eta - j\omega_0)t}, \tag{3.16}$$

which can be expanded by Euler's formula:

$$i_h(t) = A_1 e^{-\eta t}[\cos \omega_0 t + j \sin \omega_0 t] + A_2 e^{-\eta t}[\cos \omega_0 t - j \sin \omega_0 t]. \tag{3.17a}$$

$$= e^{-\eta t}[B_1 \cos \omega_0 t + B_2 \sin \omega_0 t]. \tag{3.17b}$$

The sum of two sinusoids of the same frequency is another of the same frequency [70] per trigonometric identity

$$\Phi \cos \omega t + \Psi \sin \omega t = \sqrt{\Phi^2 + \Psi^2} \cos[\omega t - \tan^{-1}(\Psi/\Phi)], \tag{3.18}$$

allowing equation (3.17b) to be expressed as

$$i_h(t) = I_h(\phi_s) e^{-\eta t} \cos(\omega_0 t - \beta(\phi_s)), \tag{3.19}$$

where $I_h(\phi_s)$ and $\beta(\phi_s)$ depend on initial conditions, but because voltage was defined with a generic phase ϕ_s at time of switch closure these parameters depend on that value.

3.1.5 Initial Conditions and the General Solution

The general solution for (3.5) is the sum of particular and homogeneous solutions:

$$\begin{aligned} i_{RLC}(t) =& i_p(t) + i_h(t) \\ =& I_p \cos(\omega_c t - \psi - \phi_s) + I_h(\phi_s) e^{-\eta t} \cos(\omega_0 t - \beta(\phi_s)). \end{aligned} \tag{3.20}$$

To determine $I_h(\phi_s)$ and $\beta(\phi_s)$, initial conditions must be considered. The reactive branch is a series connection of an inductor, capacitor and resistor. Since the behavior of an inductor is to oppose change in current, a reasonable initial condition is that at $t = 0$, current through the reactive branch $i_{RLC}(0) = 0$. Then (3.20) becomes

$$0 = I_p \cos(-\psi - \phi_s) + I_h(\phi_s) \cos(-\beta(\phi_s)). \tag{3.21}$$

Noting that cosine is an even function and rearranging gives expression

$$I_h(\phi_s) = - \frac{I_p \cos(\psi + \phi_s)}{\cos(\beta(\phi_s))}. \tag{3.22}$$

Because the circuit is deenergized prior to switch closure, another reasonable initial condition is zero initial charge on the capacitors, $q_e(0) = 0$. Insertion of this initial condition and the

first initial condition into (3.2) gives

$$\frac{V\cos(\phi_s)}{L} = \Big[I_p\omega_c\sin(\psi+\phi_s) - I_h(\phi_s)\eta\cos(\beta(\phi_s)) + I_h(\phi_s)\omega_0\sin(\beta(\phi_s))\Big]. \tag{3.23}$$

where the right hand side is the derivative terms of i_{RLC} given in (3.20) evaluated at $t = t_s$ and again leveraging evenness of cosines and oddness of sines.

Substitution of (3.22) for I_h and rearranging yields

$$\frac{\sin(\beta(\phi_s))}{\cos(\beta(\phi_s))} = \frac{\left[I_p\omega_c\sin(\psi+\phi_s) + I_p\eta\cos(\psi+\phi_s) - \frac{V\cos(\phi_s)}{L}\right]}{I_p\omega_0\cos(\psi+\phi_s)}, \tag{3.24}$$

or

$$\beta(\phi_s) = \tan^{-1}\left(\frac{\left[I_p\omega_c\sin(\psi+\phi_s) + I_p\eta\cos(\psi+\phi_s) - \frac{V\cos(\phi_s)}{L}\right]}{I_p\omega_0\cos(\psi+\phi_s)}\right). \tag{3.25}$$

Finally, substituting (3.25) into (3.22) gives

$$I_h(\phi_s) = -I_p\cos(\psi+\phi_s)\sqrt{1+\left[\frac{\left[I_p\omega_c\sin(\psi+\phi_s) + I_p\eta\cos(\psi+\phi_s) - \frac{V\cos(\phi_s)}{L}\right]}{I_p\omega_0\cos(\psi+\phi_s)}\right]^2}, \tag{3.26}$$

where trigonometric identity

$$\cos(\tan^{-1}(x)) = \frac{1}{\sqrt{1+x^2}} \tag{3.27}$$

was used.

The fact that the values of β and I_h are dependent on the voltage phase at time of switch closure ϕ_s is belabored because reproducibility of the transient effects on current caused by closing the reference circuit switch is critical to modeling those effects, and a model of system dynamics is an integral piece to controller development.

3.2 Power in the Reference Circuit

3.2.1 Single Phase RLC Circuit

As seen in (3.5), the transient response of current in an underdamped RLC circuit such as the reference circuit is made up of exponential decay multiplied by a sinusoid with the damped resonant frequency defined by the circuit parameters. The steady-state current response manifests as a sinusoid at voltage frequency with amplitude and phase dependent on circuit parameters.

Having described current in terms of the homogeneous and particular solutions to the governing ODE, we can extend those terms into discussion of instantaneous active power:

$$P_{RLC}(t) = v(t)i_{RLC}(t) = P_p(t) + P_h(t) \tag{3.28a}$$

$$P_p(t) = V\cos(\omega_c t - \psi - \phi_s)I_p\cos(\omega_c t - \phi_s) \tag{3.28b}$$

$$P_h(t) = V\cos(\omega_c t - \phi_s)I_h(\phi_s)e^{-\eta(t)}\cos(\omega_0(t) - \beta(\phi_s)) \tag{3.28c}$$

Trigonometric identity

$$\cos(\theta_1)\cos(\theta_2) = \frac{1}{2}\Big[\cos(\theta_1+\theta_2) + \cos(\theta_1-\theta_2)\Big] \tag{3.29}$$

allows expansion of he right hand side of (3.28b) into two terms: the DC offset and a sinusoid with frequency $2\omega_c$

$$P_p(t) = \frac{VI_p}{2}\cos(\psi) \tag{3.30a}$$

$$+ \frac{V_{ss}I_d}{2}\cos(2\omega_c t - \psi - 2\phi_s) \tag{3.30b}$$

Working with single phase power is made marginally more difficult because 3.30b obscures the remainder of the signal.

In practice, the double frequency component can be removed with a band-stop filter with stop band centered on $2\omega_c$ as shown in Figure 3.2.

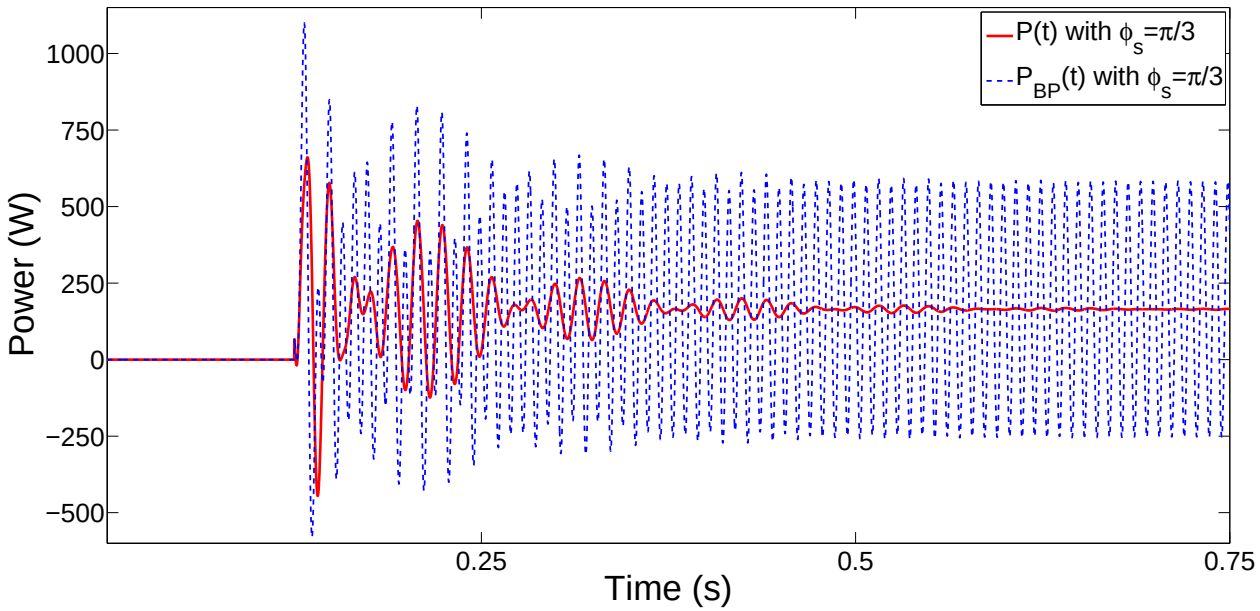

Figure 3.2: The single-phase reference circuit active power response to closing the switch at time t=0.125s.

While complications from 3.30b can be overcome with filtering, variations in ϕ_s change the amplitude term $I_h(\phi_s)$ and phase term $\beta(\phi_s)$ of (3.28c), making modeling much more difficult. Figure 3.3 illustrates how the circuit dynamic response is dependent on the phase of the voltage when the switch is closed. This dependency makes dynamic modeling more difficult. However, in balanced, poly-phase circuits, these terms counteract one another, greatly simplifying modeling of disturbance response.

3.2.2 Three-phase balanced RLC circuit

Akagi's p-q theory [71] provides a direct instantaneous active and reactive power calculation for balanced circuits:

$$P_{3\Phi}(t) = v_a(t)i_a(t) + v_b(t)i_b(t) + v_c(t)i_c(t) \tag{3.31a}$$

and

$$Q_{3\Phi}(t) = \frac{1}{\sqrt{3}}(v_{bc}(t)i_a(t) + v_{ca}(t)i_b(t) + v_{ab}(t)i_c(t)), \tag{3.31b}$$

where the voltage terms in (3.31b) are line voltages.

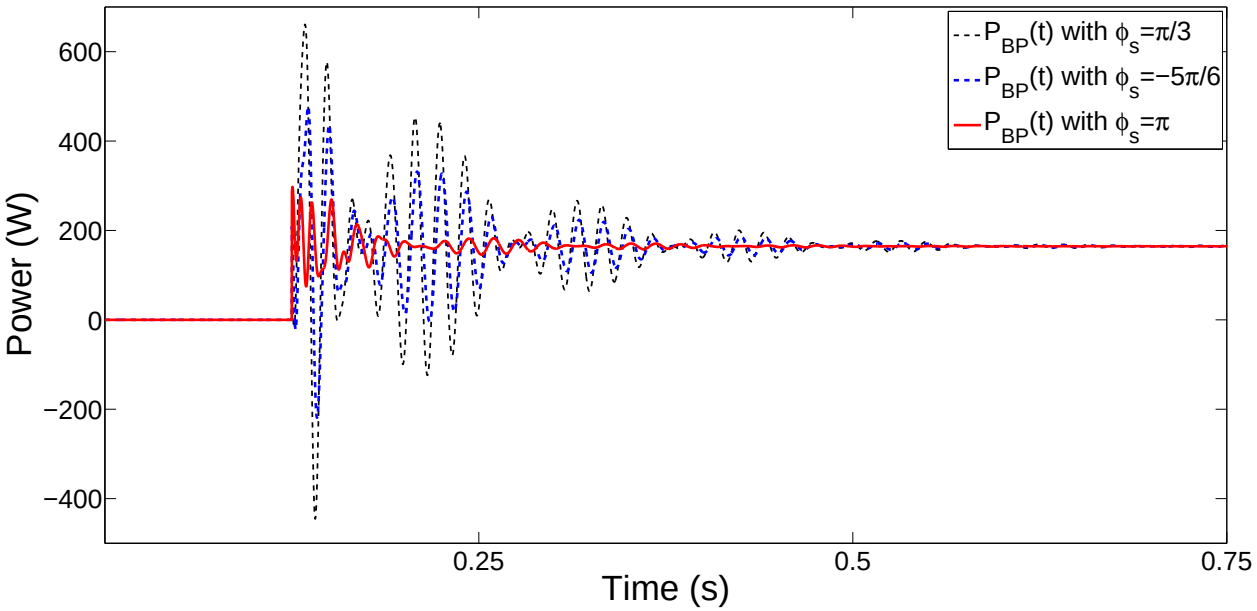

Figure 3.3: The single-phase reference circuit active power response to closing the switch at time t=0.125s, band-stop filtered with different voltage phases ϕ_s at time of switch closure.

Taking phase 'a' as the single phase case ($v_a(t) = v(t) = V\cos(\omega_c t - \phi_s)$), then $v_b(t) = V\cos(\omega_c t - \phi_s - \frac{2\pi}{3})$ and $v_c(t) = V\cos(\omega_c t - \phi_s + \frac{2\pi}{3})$. Similarly, we will denote current through the respective RLC branches of the reference circuit $i_a(t), i_b(t)$ and $i_c(t)$, noting that we have dropped the RLC subscript with justification that discussion of current on the purely resistive branches is trivial whether in single or three phase cases.

The separation of particular and homogeneous solutions of the governing ODE (3.2) used for analysis of single-phase is extended into the three-phase case. The interaction of the particular solutions of three balanced phases counteract the double frequency components of each phase, negating the need for band-pass filtering. Expanding (3.28b) to three phases and again leveraging (3.29) yields

$$P_{p3\Phi}(t) = v_a(t)i_{pa}(t) + v_b(t)i_{pb}(t) + v_c(t)i_{pc}(t) \tag{3.32a}$$

$$= VI_p \begin{bmatrix} \cos(\omega_c t - \psi - \phi_s)\cos(\omega_c t - \phi_s) \\ +\cos(\omega_c t - \psi - \phi_s - \frac{2\pi}{3})\cos(\omega_c t - \phi_s - \frac{2\pi}{3}) \\ +\cos(\omega_c t - \psi - \phi_s + \frac{2\pi}{3})\cos(\omega_c t - \phi_s + \frac{2\pi}{3}) \end{bmatrix} \tag{3.32b}$$

$$= 3\frac{VI_p}{2}\cos(-\psi) + \frac{VI_p}{2}\Big[\cos(2\omega_c t) + \cos(2\omega_c t - \frac{4\pi}{3}) + \cos(2\omega_c t + \frac{4\pi}{3})\Big] \tag{3.32c}$$

where the term inside the braces in (3.32c) is equal to zero for all t.

Similarly, the dynamic response governed by the homogeneous solution of (3.2) loses dependence on ϕ_s in the balanced three phase case, though the algebra and trigonometry required to show it are much more involved.

The three phase power resulting from the homogeneous solution to the ODE governing current is given by:

$$P_{h3\Phi}(t) = v_a(t)i_{ha}(t) + v_b(t)i_{hb}(t) + v_c(t)i_{hc}(t) \tag{3.33a}$$

$$= Ve^{-\eta(t)} \begin{bmatrix} \cos(\omega_c t - \phi_s)I_h(\phi_s)\cos(\omega_0(t) - \beta(\phi_s)) \\ +\cos(\omega_c t - \phi_s - \frac{2\pi}{3})I_h(\phi_s - \frac{2\pi}{3})\cos(\omega_0(t) - \beta(\phi_s - \frac{2\pi}{3})) \\ +\cos(\omega_c t - \phi_s + \frac{2\pi}{3})I_h(\phi_s + \frac{2\pi}{3})\cos(\omega_0(t) - \beta(\phi_s + \frac{2\pi}{3})) \end{bmatrix}. \tag{3.33b}$$

The terms inside the braces in (3.33b) can be expressed as the sum of three cosines with equal frequencies but different functions governing their respective amplitudes and phases.

As seen in (3.18), two sinusoids of same frequency can be summed to make a single sinusoid with the same frequency. A similar but slightly more generalized identity is given [70] by:

$$\begin{aligned} \Phi\cos(\omega t + \gamma) + \Psi\cos(\omega t + \delta) =& \sqrt{[\Phi\sin(\gamma) + \Psi\sin(\delta)]^2 + [\Phi\cos(\gamma) + \Psi\cos(\delta)]^2} \\ & \cdot \cos\left[\omega t + \tan^{-1}\left[\frac{\Phi\sin(\gamma) + \Psi\sin(\delta)}{\Phi\cos(\gamma) + \Psi\cos(\delta)}\right]\right]. \end{aligned} \tag{3.34}$$

Since two cosines with equal frequency but different amplitudes and phases sum to a cosine with the same frequency but amplitude and phase governed by (3.34), then three cosines of equal

frequency but different amplitudes and phases sum to one as well. By using (3.34) on two eligible cosines, then using that result with a third eligible cosine, in (3.34) again, it can be shown

$$\begin{aligned}
&\Phi\cos(\omega t+\gamma)+\Psi\cos(\omega t+\delta)+\Theta\cos(\omega t+\lambda)\\
=&\sqrt{[\Phi\sin(\gamma)+\Psi\sin(\delta)+\Theta\sin(\lambda)]^2+[\Phi\cos(\gamma)+\Psi\cos(\delta)+\Theta\cos(\lambda)]^2}\\
&\cdot\cos\left[\omega t+\tan^{-1}\left[\frac{\Phi\sin(\gamma)+\Psi\sin(\delta)+\Theta\sin(\lambda)}{\Phi\cos(\gamma)+\Psi\cos(\delta)+\Theta\cos(\lambda)}\right]\right].
\end{aligned}\tag{3.35}$$

To evaluate the term inside the braces in (3.33b) using (3.35), the following mapping is adopted:

$$\begin{aligned}
\Phi_A=&\ \cos(\omega_c t-\phi_s)I_h(\phi_s), & \gamma_a=&\ \beta(\phi_s),\\
\Psi_B=&\ \cos(\omega_c t-\phi_s-\tfrac{2\pi}{3})I_h(\phi_s-\tfrac{2\pi}{3}), & \delta_b=&\ \beta(\phi_s-\tfrac{2\pi}{3}),\\
\Theta_C=&\ \cos(\omega_c t-\phi_s+\tfrac{2\pi}{3})I_h(\phi_s+\tfrac{2\pi}{3}), & \lambda_c=&\ \beta(\phi_s+\tfrac{2\pi}{3}).
\end{aligned}\tag{3.36}$$

Note that both the amplitude and phase of the resulting cosine from (3.35) are expressed only in terms of $[\Phi\sin(\gamma)+\Psi\sin(\delta)+\Theta\sin(\lambda)]$ and $[\Phi\cos(\gamma)+\Psi\cos(\delta)+\Theta\cos(\lambda)]$. Then, if $[\Phi_A\sin(\gamma_a)+\Psi_B\sin(\delta_b)+\Theta_C\sin(\lambda_c)]$ and $[\Phi_A\cos(\gamma_a)+\Psi_B\cos(\delta_b)+\Theta_C\cos(\lambda_c)]$ can be shown to have no ϕ_s terms, then the balanced three-phase reference circuit dynamic response to switch closure is independent of voltage phase at time of switch closure.

Starting with $[\Phi_A\cos(\gamma_a)+\Psi_B\cos(\delta_b)+\Theta_C\cos(\lambda_c)]$, and noting similarity in the three component terms, evaluation of $\Phi_A\cos(\gamma_a)$ allows some simplification:

$$\begin{aligned}
\Phi_A\cos(\gamma_a)&=\cos(\omega_c t-\phi_s)I_h(\phi_s)\cos(\beta(\phi_s))\\
&=-\cos(\omega_c t-\phi_s)I_p\cos(\psi+\phi_s),
\end{aligned}\tag{3.37}$$

where the expressions for $I_h(\phi_s)$ given in (3.22) was substituted.

The relationship between $I_h(\phi_s)$ and $\beta(\phi_s)$ given in (3.22) holds irrespective of the argument, so having evaluated $\Phi_A\cos(\gamma_a)$, $\Psi_B\cos(\delta_b)$ and $\Theta_C\cos(\lambda_c)$ are identical but for their respective phase shifts:

$$\begin{aligned}
&\Phi_A \cos(\gamma_a) + \Psi_B \cos(\delta_b) + \Theta_C \cos(\lambda_c) \\
&= - I_p \begin{bmatrix} \cos(\omega_c t - \phi_s)\cos(\psi + \phi_s) \\ + \cos(\omega_c t - \phi_s + \frac{2\pi}{3})\cos(\psi + \phi_s - \frac{2\pi}{3}) \\ + \cos(\omega_c t - \phi_s - \frac{2\pi}{3})\cos(\psi + \phi_s + \frac{2\pi}{3}) \end{bmatrix}.
\end{aligned} \tag{3.38}$$

The terms in the braces in (3.38) can be expanded using product-to-sum trigonometric identity (3.29), resulting in

$$\begin{aligned}
&\Phi_A \cos(\gamma_a) + \Psi_B \cos(\delta_b) + \Theta_C \cos(\lambda_c) \\
&= - \frac{3I_p}{2} \cos(\omega_c t + \psi) + \begin{bmatrix} \cos(\omega_c t - \psi - 2\phi_s) \\ + \cos(\omega_c t - \psi - 2\phi_s + \frac{4\pi}{3}) \\ + \cos(\omega_c t - \psi - 2\phi_s - \frac{4\pi}{3}) \end{bmatrix},
\end{aligned} \tag{3.39}$$

The terms in braces in (3.39) sum to zero for all t and any ϕ_s, making $[\Phi_A \cos(\gamma_a) + \Psi_B \cos + \Theta_C \cos(\lambda_c)]$ independent of ϕ_s.

Similarly to (3.37) to show $[\Phi_A \sin(\gamma_a) + \Psi_B \sin(\delta_b) + \Theta_C \sin(\lambda_c)]$ independence of ϕ_s begins with evaluation of $\Phi_A \sin(\gamma_a)$:

$$\Phi_A \sin(\gamma_a) = \cos(\omega_c t - \phi_s) I_h(\phi_s) \sin(\beta(\phi_s)). \tag{3.40}$$

As with (3.37), the expression for $I_h(\phi_s)$ from (3.22) is substituted:

$$\Phi_A \sin(\gamma_a) = - \cos(\omega_c t - \phi_s) I_p \cos(\psi + \phi_s) \tan(\beta(\phi_s)). \tag{3.41}$$

Recalling that $\beta(\phi_s)$ is defined in terms of inverse tangent in (3.25), by substitution of that definition, (3.41) becomes

$$\Phi_A \sin(\gamma_a) = -\frac{\cos(\omega_c t - \phi_s)}{\omega_0} \Big[I_p \omega_c \sin(\psi + \phi_s) + I_p \eta \cos(\psi + \phi_s) - \frac{V \cos(\phi_s)}{L} \Big]. \tag{3.42}$$

Using related product-to-sum trigonometric identities (3.29) and

$$\cos(\theta_1)\sin(\theta_2) = \frac{1}{2}\Big[\sin(\theta_1+\theta_2) - \sin(\theta_1-\theta_2)\Big], \tag{3.43}$$

equation (3.42) expands to

$$\begin{aligned}\Phi_A \sin(\gamma_a) = &-\frac{I_p\omega_c}{2\omega_0}\Big(\sin(\omega_c t+\psi) - \sin(\omega_c t - 2\phi_s - \psi)\Big)\\ &-\frac{I_p\eta}{2\omega_0}\Big(\cos(\omega_c t+\psi) + \cos(\omega_c t - 2\phi_s - \psi)\Big)\\ &+\frac{V}{2L\omega_0}\Big(\cos(\omega_c t) + \cos(\omega_c t - 2\phi_s)\Big).\end{aligned} \tag{3.44}$$

Just as the relationship between $I_p(\phi_s)$ and $\beta(\phi_s)$ given in (3.22) allowed bypassing the expansion of $\Psi_B\cos(\delta_b)$ and $\Theta_C\cos(\lambda_c)$ given $\Phi_A\cos(\gamma_a)$, $\Psi_B\sin(\delta_b)$ and $\Theta_C\sin(\lambda_c)$ are identical to $\Phi_A\sin(\gamma_a)$ but for their respective phase shifts, leading to:

$$\begin{aligned}&\Phi_A\sin(\gamma_a) + \Psi_B\sin(\delta_b) + \Theta_C\sin(\lambda_c)\\ &= -\frac{3I_p\omega_c}{2\omega_0}\sin(\omega_c t+\psi) - \frac{3I_p\eta}{2\omega_0}\cos(\omega_c t+\psi) + \frac{3V}{2L\omega_0}\cos(\omega_c t)\\ &\quad+\frac{I_p\omega_c}{2\omega_0}\begin{bmatrix}\sin(\omega_c t - 2\phi_s - \psi)\\ +\sin(\omega_c t - 2\phi_s - \psi + \frac{4\pi}{3})\\ +\sin(\omega_c t - 2\phi_s - \psi - \frac{4\pi}{3})\end{bmatrix}\\ &\quad-\frac{I_p\eta}{2\omega_0}\begin{bmatrix}\cos(\omega_c t - 2\phi_s - \psi)\\ +\cos(\omega_c t - 2\phi_s - \psi + \frac{4\pi}{3})\\ +\cos(\omega_c t - 2\phi_s - \psi - \frac{4\pi}{3})\end{bmatrix}\\ &\quad+\frac{V}{2L\omega_0}\begin{bmatrix}\cos(\omega_c t - 2\phi_s)\\ +\cos(\omega_c t - 2\phi_s + \frac{4\pi}{3})\\ +\cos(\omega_c t - 2\phi_s - \frac{4\pi}{3}).\end{bmatrix}\end{aligned} \tag{3.45}$$

In (3.45), each of the sets of braces sum to zero for all t and any ϕ_s, making $[\Phi_A\sin(\gamma_a) + \Psi_B\sin(\delta_b) + \Theta_C\sin(\lambda_c)]$ independent of ϕ_s.

With back substitution of $[\Phi_A \sin(\gamma_a)+\Psi_B \sin(\delta_b)+\Theta_C \sin(\lambda_c)]$ and $[\Phi_A \cos(\gamma_a)+\Psi_B \cos(\delta_b)+\Theta_C \cos(\lambda_c)]$ into (3.35), it can be shown (with considerable algebra and trigonometry which is irrelevant to the discussion on reproducibility and thus omitted) that

$$P_{h3\Phi}(t) = V \sin(\omega_c t) I_{h3\Phi} e^{-\eta(t)} \cos(\omega_0(t) - \beta_{3\Phi}) \tag{3.46}$$

where $I_{h3\Phi}$, and $\beta_{3\Phi}$ are determined solely by circuit parameters. Then, in three-phase active power we find a signal has consistently reproducible behavior on the balanced instance of the reference circuit when the switch is closed, without consideration of voltage phase at the time of switch closure. This greatly reduces the complexity of model development and thus makes possible model-based control design.

Similar reproducibility can be found in three-phase reactive power. The line voltages used in (3.31b) merit a brief discussion. Without loss of generality, ϕ_s can be assumed zero. Then another sum of sinusoids with equal frequencies is found,

$$\begin{aligned} v_{bc}(t) =& v_b(t) - v_c(t) \\ &= V \cos(\omega_c t - \frac{2\pi}{3}) - V \cos(\omega_c t + \frac{2\pi}{3}), \end{aligned} \tag{3.47}$$

meaning (3.34) applies. Using (3.34) to simplify (3.47) gives

$$\begin{aligned} &V \cos(\omega t - \frac{2\pi}{3}) - V \cos(\omega t + \frac{2\pi}{3}) = \\ &\sqrt{[V \sin(-\frac{2\pi}{3}) - V \sin(\frac{2\pi}{3})]^2 + [V \cos(-\frac{2\pi}{3}) - V \cos(\frac{2\pi}{3})]^2} \\ &\cdot \cos\left[\omega t + \tan^{-1}\left[\frac{V \sin(-\frac{2\pi}{3}) - V \sin(\frac{2\pi}{3})}{V \cos(-\frac{2\pi}{3}) - V \cos(\frac{2\pi}{3})}\right]\right]. \end{aligned} \tag{3.48}$$

Evaluation of (3.48) results in $v_{bc}(t) = \sqrt{3} v_a^{-90}(t)$, where the superscript -90 denotes a phase shift of $-\pi/2$. The relation is similar for the other line voltages, meaning (3.31b) can be written

$$Q_{3\Phi}(t) = v_a^{-90}(t) i_a(t) + v_b^{-90}(t) i_b(t) + v_c^{-90}(t) i_c(t), \tag{3.49}$$

The value of (3.49) will become apparent in Chapters 4 and 5.

3.3 Limitations to Data Acquisition

The reproducibility of three phase power transients on balanced loads facilitates modeling, but, as seen in (3.46), these transients are composed of a grid frequency component that could cause problems with data acquisition and control by a microprocessor due to jitter. However, jitter would be of little concern when considering the oscillation at the underdamped resonant frequency ω_0. Because the discussion now concerns sampling and sample timing, discrete time variables are introduced: t_n denotes high frequency sampling while t_k denotes sampling at grid frequency $f_c = \omega_c/2\pi$.

Sampling at $t_k = \frac{\pi}{2\omega_c} + k2\pi, k \in \mathbb{Z}$, so that the sine term in (3.46) is equal to one at the time of each sample would return $VI_{h3\Phi}e^{-\eta(t_k)}\cos(\omega_0(t_k) - \beta_{3\Phi})$, exactly the part of the signal that could be controlled by a microprocessor. However, having no prescience about when a transient may come makes this ideal sample timing impossible in real-time.

The notation adopted has assumed that the transient occurs at time $t = 0$, but electric grids are operated continuously and normal operations aim to avoid large, disruptive transients; then it must be assumed that occurrence of such a transient would only happen unexpectedly. Fig 3.4 shows the impact of variation in sample timing when sampling at grid frequency: changes in the sampled signal are illustrated by varying the timing of data acquisition by a quarter cycle.

It is tempting to suggest a step detection algorithm to identify the initiation of an electric grid transient, but we must recall that the aim is to use a DC-AC inverter for control, and would necessarily be subject to harmonic distortion caused by the inverter. Figure 3.5 shows a power transient initiated by switching in the reference circuit while power is supplied by a nearby grid-tied inverter. Clearly, with so much distortion, step detection or attempts to identify peaks in the transient response would be severely impacted. Furthermore, the reference circuit is designed to provide a specific transient response that is able to be recreated as needed, while a live electric grid

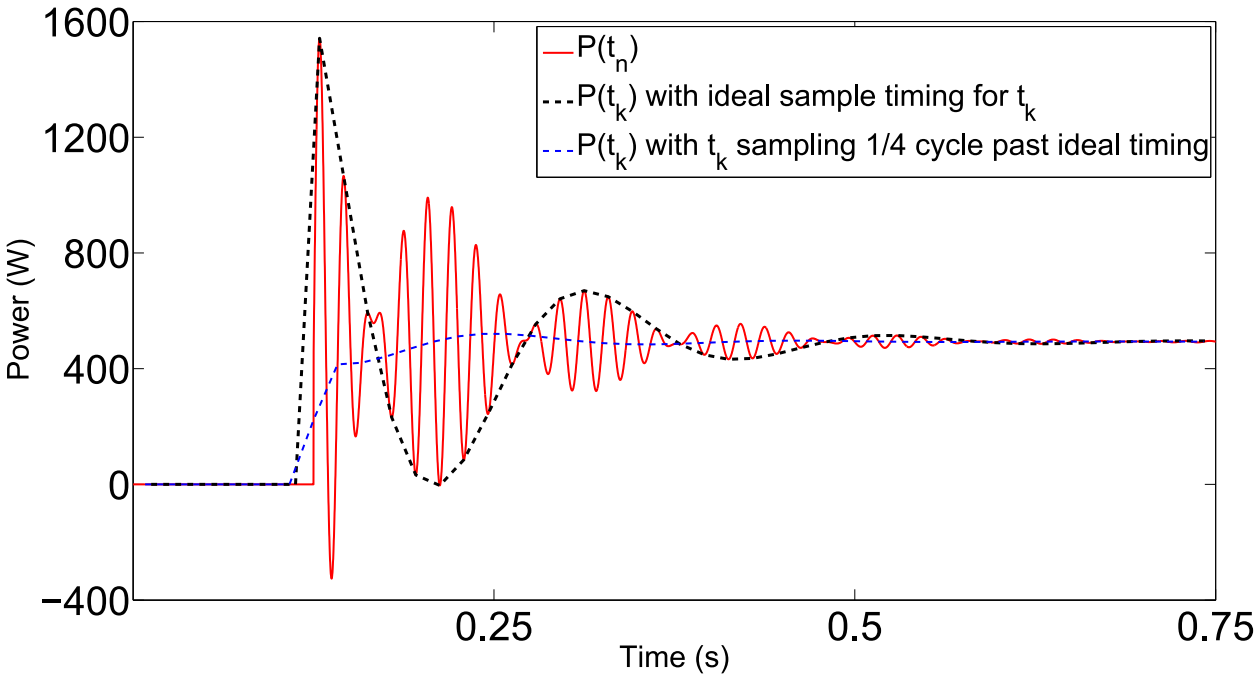

Figure 3.4: Three Phase Reference Circuit Real Power in response to switch closure at t_s=0.1875s, with grid-frequency sampling done at different times within each period.

is subject to countless possibilities that might lead to disturbances of all magnitudes and subject to vastly different parameters. Then, determination of a step detection threshold on the specific case allowed by the reference circuit would be of little value for the greater electric grid.

3.3.1 Amplitude Modulation

Equation (3.46) can be interpreted as the amplitude term $\frac{3}{2}I_{h3\Phi}e^{-\eta(t)}\cos(\omega_0(t)-\beta_{3\Phi})$ acting on $\sin(\omega_c t)$. Because of the product-sum relationship of sinusoids seen in (3.29), the frequency content is concentrated at $\omega_c+\omega_0$ and $\omega_c-\omega_0$ making filtering unhelpful toward extracting the component of active power oscillating at the damped resonant frequency ω_0. The problem is one of amplitude modulation (AM), extensively utilized in the field of radio communications. In AM terms, the low frequency component to transient response of active power modulates the grid frequency carrier ω_c, into a dual sideband, suppressed carrier (DSB-SC) signal. Reactive power transient response is corollary.

In generic terms, the mechanism of amplitude demodulation is described as follows: an

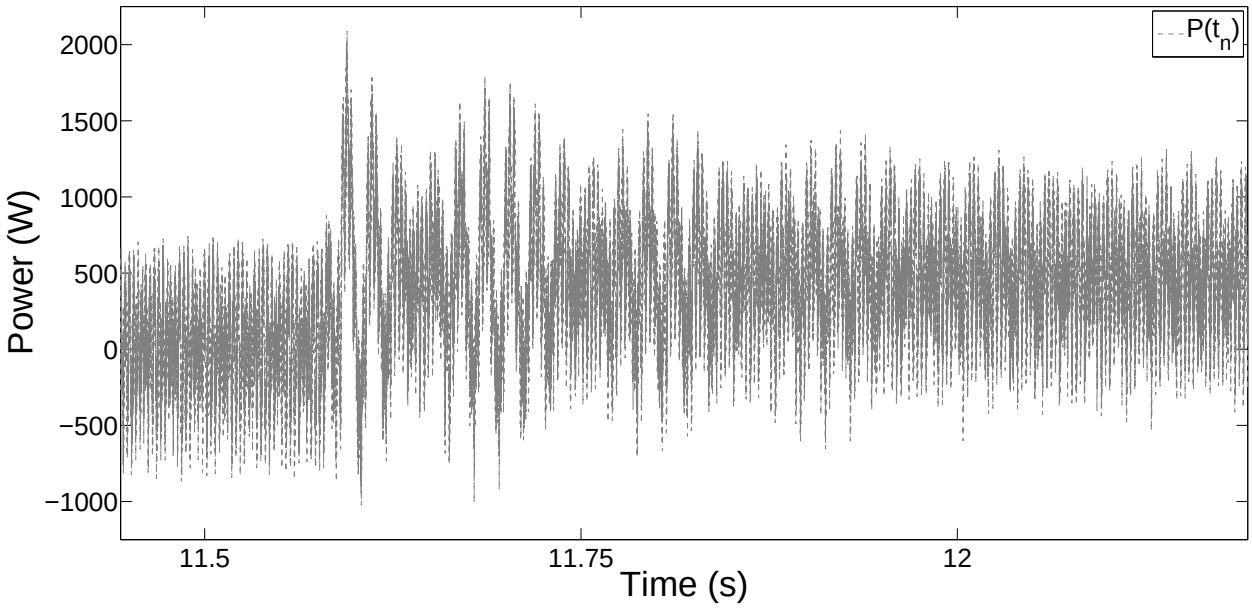

Figure 3.5: Measured active power during reference circuit switch closure while an adjacent grid-tied inverter supplies power.

information signal $I(t)$ acts as the amplitude term of (i.e. modulates) a sinusoidal carrier given by $\cos(\omega_c t)$ then by multiplying by another sinusoid at the same frequency (3.29) yields

$$I(t)\cos(\omega_c t)\cos(\omega_c t) = I(t)\frac{1}{2}[1+\cos(2\omega_c t)]. \tag{3.50}$$

The double frequency term is filtered leaving $\frac{1}{2}I(t)$, which can be amplified with gain 2 to retrieve the original information signal. A phase difference ϕ between carrier and demodulating signal would appear as an additional cosine term, reducing the amplitude and/or inverting information signal. I.e. the right hand side of (3.50) would be $\frac{1}{2}I(t)[\cos(\phi)+\cos(2\omega_c t+\phi)]$. In this dissertation, demodulation with minimum (or zero) phase difference between carrier and demodulation signal may be referred to as the 'best' demodulation because of greater certainty of the amplitude of the demodulated signal. Since the aim is to meet electric grid oscillations with matching oscillations with π phase difference, correct magnitude is crucial for the desired nullification.

It should also be noted that every demodulation method discussed in this dissertation includes low-pass filtering and/or moving average filtering that removes any DC offset from the signal being demodulated. This is inherent in the mechanism of demodulation. Referring back to

(3.50), a DC component has no carrier so the attempt at demodulation actually ends up modulating the input. That would be $I(t)\cos(0)\cos(\omega_c t) = I(t)\cos(\omega_c t)$. Subsequent filtering destroys the modulated signal: $F_{LP}(q)I(t)\cos(\omega_c t) \approx 0$. This component can be recreated by low-pass filtering the signal prior to demodulation. More details on amplitude modulation are included in Appendix A.

3.4 Conclusions

In this chapter a reference circuit was presented that, by switching in an inductive load, can create electrical power transients that are qualitatively similar to transients seen on electric grids. The ordinary differential equation governing current in the circuit was solved, revealing that the current transient response in a single phase instance of the reference circuit is affected by the phase of voltage when the load is switched in. This behavior translates into similar variations in active power dynamic response in the single-phase circuit.

Analysis of power in a balanced three-phase version of the reference circuit showed that identical transients could be expected regardless of the timing of switch closure as it relates to voltage phase. This motivates efforts to use balanced three phase power as the metric to be controlled in a disturbance rejection controller.

Sampling and response limits of microprocessors dictate that control efforts focus on a low frequency component of transient effects on the balanced three-phase reference circuit. As discussed in Chapter 1, the demodulation algorithm utilized for the implementation of the control design discussed in Chapter 2 isolates this component correctly 25% of the time. This unreliability undermines design goal of consistently reproducible controller performance. Clearly, a more consistent demodulation method is called for.

Chapter 4

GOLD Method Design, Optimization and Implementation

Techniques used in radio communications provided a starting point for demodulating power transients, but the short-lived nature of electric grid power disturbances caused additional challenges. AM demodulation methods have an underlying assumption that the audio signal that is decoded is effectively infinitely long when compared to the carrier frequency in the range of 540-1600 kHz. For an AM demodulation method that takes half-a-dozen cycles to synchronize, the frequency and phase matching between carrier and demodulating signal is imperceivable to an AM radio listener [72]. When the same methods are used at 50-60Hz to decode a transient that lasts less than a second, the synchronization occurs during the most dynamic part of the event. Any effort at demodulation of power transients must synchronize very quickly to be useful.

The discussion begins with Costas Loop, a well known method for demodulation of dual-sideband suppressed carrier (DSB-SC) radio signals. Discussion of a major component of Costas Loop, the Phase Locked Loop (PLL) is provided in Appendix B, along with expanded discussion of DSB-SC signals vs a more prevalent approach to AM radio broadcast and receiving in Appendix A.

4.1 Costas Loop

Costas loop was presented in [72], for use in a context in which the carrier signal is not available and must be reconstructed such as in DSB-SC demodulation. Figure 4.1 shows the basic architecture of Costas Loop. The block labeled VCO is a Voltage Controlled Oscillator, LPF denotes low-pass filters, the block labeled -90^o is a -90 degree phase shift, and $\otimes$ indicates multiplication.

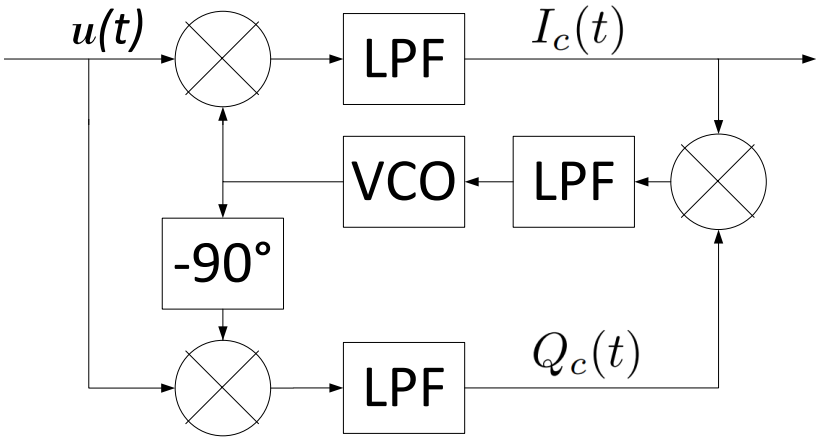

Figure 4.1: Classical Costas Loop. $u(t)$ is a generic input, $Q(t)$ is the quadrature branch and $I(t)$ is the in-line branch as well as output.

Costas loop essentially combines two PLLs, denoted as the in-phase PLL and quadrature PLL because, when synchronized, their respective signals are in-phase or have a $\pi/2$ phase difference from the signal being demodulated. Referring back to the generic expression for AM demodulation (3.50) the phase of the in-phase PLL is perfectly matched with the carrier, the output is the demodulated signal, while the output of the quadrature PLL is zero:

$$\begin{aligned}
&I(t)\cos(\omega_c t)\cos(\omega_c t) = I(t)[\frac{1}{2} + \cos(2\omega_c t)],\\
&F_{LP}(q)I(t)\frac{1}{2}[1+\cos(2\omega_c t)] \approx \frac{1}{2}I(t);\\
&I(t)\cos(\omega_c t)\cos(\omega_c t - \frac{\pi}{2}) = I(t)\frac{1}{2}[\cos(\frac{\pi}{2}) + \cos(2\omega_c t)],\\
&F_{LP}(q)I(t)\frac{1}{2}[0+\cos(2\omega_c t)] \approx 0.
\end{aligned} \tag{4.1}$$

As shown in Fig. 4.1, the product of in-phase and quadrature outputs is the VCO input. The demodulation of the input by the quadrature PLL acts as the feedback mechanism: If the VCO output becomes unsynchronized from the carrier the quadrature PLL output becomes nonzero, causing the VCO output to adjust and resynchronize; by contrast, were the quadrature PLL synchronized with the carrier then a minor perturbation would cause the in-phase PLL to become nonzero and the feedback would drive the VCO output in the wrong direction.

The use of two PLLs causes 'lock points' when the phase difference between the carrier and the VCO output is either 0 or pi radians [73]. The effect of two lock points is phase ambiguity, as there is no inherent way to know whether signals synchronized with phase difference of 0 or π radians. If the phase difference is π the demodulated signal is inverted.

Costas loop was initially applied to audio communication via AM radio, where an inverted signal is not cause for concern, but inversion of a demodulated power transients would be. A standard solution to phase ambiguity is sending a test signal and checking for inversion [74], but this is not viable for demodulating a power transient in real time.

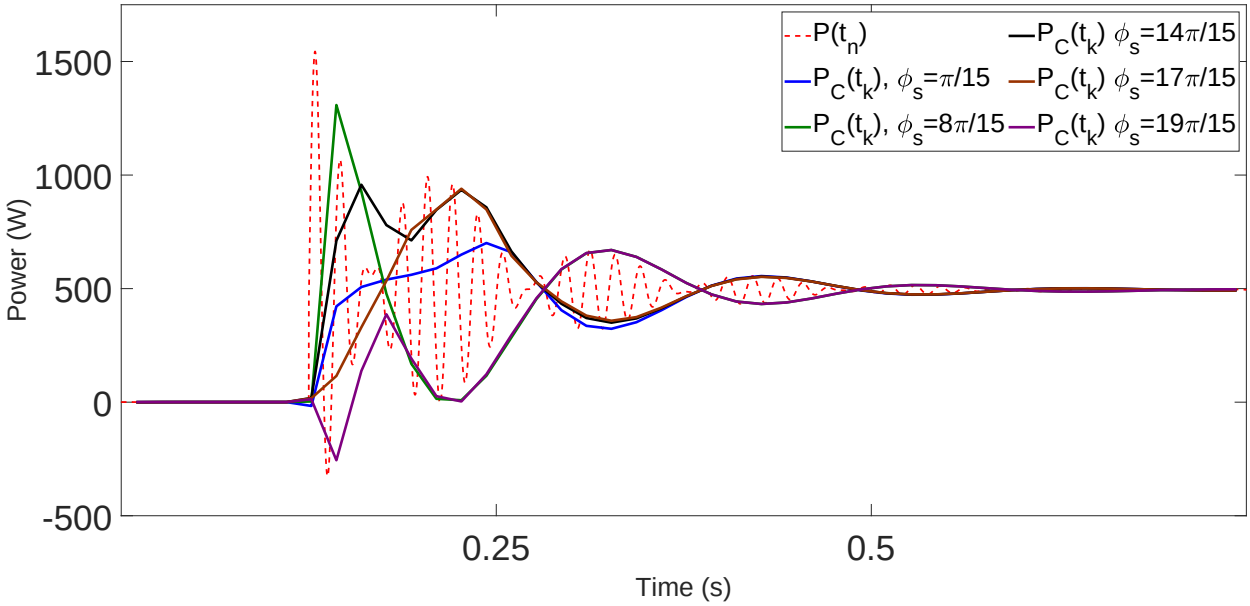

Figure 4.2: Three phase real power in the reference circuit in response to closing the switch at time $t_s = 0.125$s demodulated using Costas loop with various ϕ_s values.

Implementation of a Costas loop for power transient demodulation revealed that phase

ambiguity is not the only limitation of Costas loop making it unsuitable for the application. As seen in Fig. 4.2, Costa's loop takes 6-9 cycles to synchronize the VCO output to the carrier. The simulations depicted in Fig. 4.2 were performed with optimized VCO sensitivity, and were selected from a larger set of simulations to illustrate the phase ambiguity and long synchronization times of Costas loop.

The optimum VCO sensitivity was defined as that resulting in least time to synchronize to the desired signal (or its inverse, due to phase ambiguity), within a specified error value, for several different VCO output phases ϕ_s at time of reference circuit switch closure.

The range of VCO sensitivities for simulation was determined by first performing coarse tuning to find upper and lower limits that resulted in convergence to the desired signal, then iterating through that range, increasing sensitivity from the lower limit. Through this iteration, thirty simulations were performed per sensitivity level, incrementing ϕ_s by 12^o each simulation to test values through the full 360^o range. Figure 4.3 is a plot of convergence times of all simulations, with the simulations with fastest convergence over all ϕ_s values highlighted.

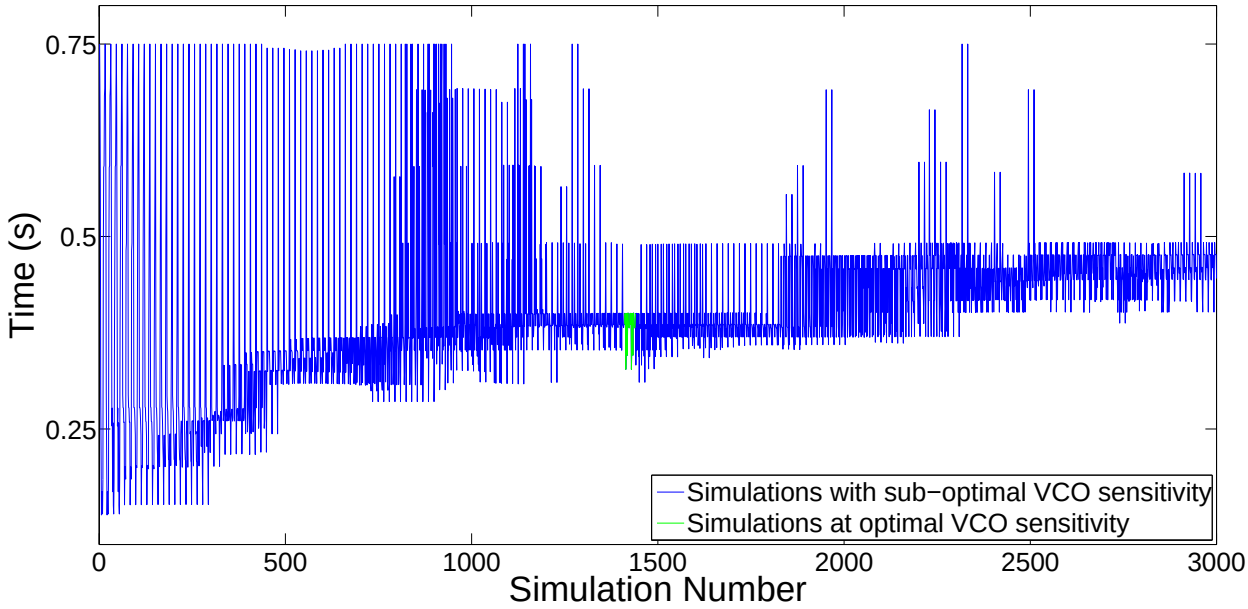

Figure 4.3: Costas loop synchronization time for 3000 simulations. Simulations are subdivided into sets of 30 simulations varying VCO starting phase ϕ_s while incrementally increasing VCO sensitivity.

An issue underlying this discussion of optimal VCO sensitivity is the third limitation of

Costas loop: the Costa loop performance for a given VCO input sensitivity depends on the amplitude of the input, making one VCO sensitivity setting optimal for the power transient caused by reference circuit switch closure, while that setting may be completely ineffective for another transient.

Finally, as discussed in Chapter 3, the signals in Fig 4.2 are the sum of the Costas loop output and a recreation of $P_{p3\Phi}(t_k)$, the steady state active power.

4.2 Departures from Classical Costas Loop

4.2.1 Approach

While the demodulation method presented in Chapter 1 does not provide consistent demodulation, one aspect of that method is leveraged to overcome the slow synchronization of Costas loop. The use of normalized voltage signals for demodulation is a crucial innovation. We know from (3.2) that voltage is the forcing function of current, and this carries through to the three phase power transient given in (3.46), which is the signal to be demodulated. Then, normalized voltage signals have the desired frequency for demodulation, reducing the problem to a single variable: phase. The conception of what became the Gwynn Open Loop Demodulation (GOLD) method lay in the hypothesis that for demodulating power transients, the basic Costas loop architecture might synchronize faster using normalized voltages rather than a VCO.

A drawback of using normalized voltages rather than a VCO is that there is no obvious feedback mechanism. While one avenue for feedback would be to adjust delay in real time, this could not be practically implemented on an FPGA. FPGA programming involves assigning discrete units of computing hardware to perform tasks, making it very fast but much less flexible than most computer programming, in which all instructions are enqueued and performed by a central processor. Implementing feedback by changing delays illustrates FPGA inflexibility, as delay values are hard-coded and implemented during FPGA program compiling, precluding adjustment at run-time. Use of a shift register might be possible, but that approach was not pursued in favor

of a simpler open-loop design.

The remainder of this chapter will discuss design choices, and investigate how GOLD method signals are used to identify the best demodulation in qualitative terms, while Chapter 5 provides mathematical analysis supporting the discussion.

4.2.2 Performance

While there are only three grid voltage signals in a three-phase circuit, signals with other phases can be formed via delay. A fundamental concession of the open loop approach is that the algorithm will not demodulate perfectly. Demodulation is done concurrently with multiple signals with different phases, and the best demodulation done by those signals is identified. These signals will be referred to as 'candidate' signals, and will be denoted by $\tilde{v}_m(t_n) = \cos(\omega_c t_n - \phi_m)$, with $C \in \mathbb{Z}$ is number of candidates and $m \in \{1, 2, ..., C\}$. The quadrature signals are denoted $\tilde{v}_m^{-90}(t_n)$ and best signal for demodulation is denoted $\tilde{v}_G(t_n)$.

As mentioned in Chapter 3, demodulation done with minimum phase difference between carrier and demodulating signal is considered 'best,' because it minimizes the amplitude reduction caused by any $\cos(\phi_m)$ term, where ϕ_m is the phase difference between the carrier and candidate 'm'. Now, a performance measure to quantify the best demodulation is introduced.

If there are C candidates with phases evenly distributed across 2π radians, the maximum phase difference between the carrier and the best candidate $\tilde{v}_G(t_n)$ is

$$\theta_{max} = \frac{\pi}{C}, \tag{4.2}$$

i.e. half the phase difference between candidates. Then the maximum amplitude error due to phase difference is given by

$$e_{max} = 100\%(1 - \cos\theta_{max}). \tag{4.3}$$

Pragmatically, the number of demodulating signals C is constrained by subsequent signal processing operations and computing resources needed to perform them. For initial design, simula-

tions were performed with five delays per phase, forming $C = 18$ candidate signals. Delays were chosen so that the candidates phases were uniformly spaced with 20^o phase difference between adjacent candidates, with maximum error $e_{max} = 1.5\%$.

4.3 Initial Design

An initial modification to Costas loop replacing the VCO with normalized voltages is depicted in Fig 4.4. In the figure, the blocks marked 'MA' are finite impulse response (FIR) moving average filters, the block marked 'BPF' is a band-pass filter and 'A' denotes voltage normalizing gain. This architecture will be referred to as 'mk0.'

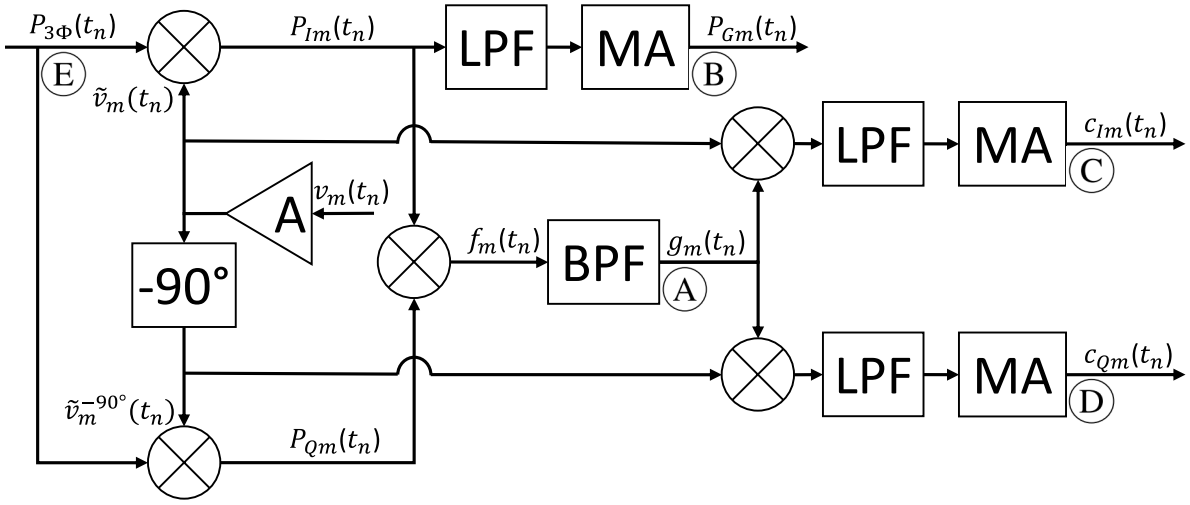

Figure 4.4: Initial modification to Costas loop, with the VCO removed in favor of normalized voltages.

Several observations can be made from the results of these simulations. Figure 4.5 shows band-pass filter output $g_m(t_n)$ located at position marked (A) in Fig. 4.4, upon switching in the reference circuit with zero active power prior to switching. The approach is validated because, as seen in Fig. 4.5, the band-pass filter does, indeed, separate a grid-frequency component with phase related to the demodulating signal. As will be discussed in greater detail in Chapter 5, the phase of $g_m(t_n)$ is actually a function of $2\phi_m$. Because of this, if the difference in phases of two candidates is π, the respective band-pass filter output signals coincide (i.e. if $\phi_2 = \phi_1 - \pi$ then

$2\phi_2 = 2\phi_1 - 2\pi$). As seen in Fig. 4.5, for 18 candidates, rather than 18 signals there are only 9 visible, because pairs with phase difference π overlap.

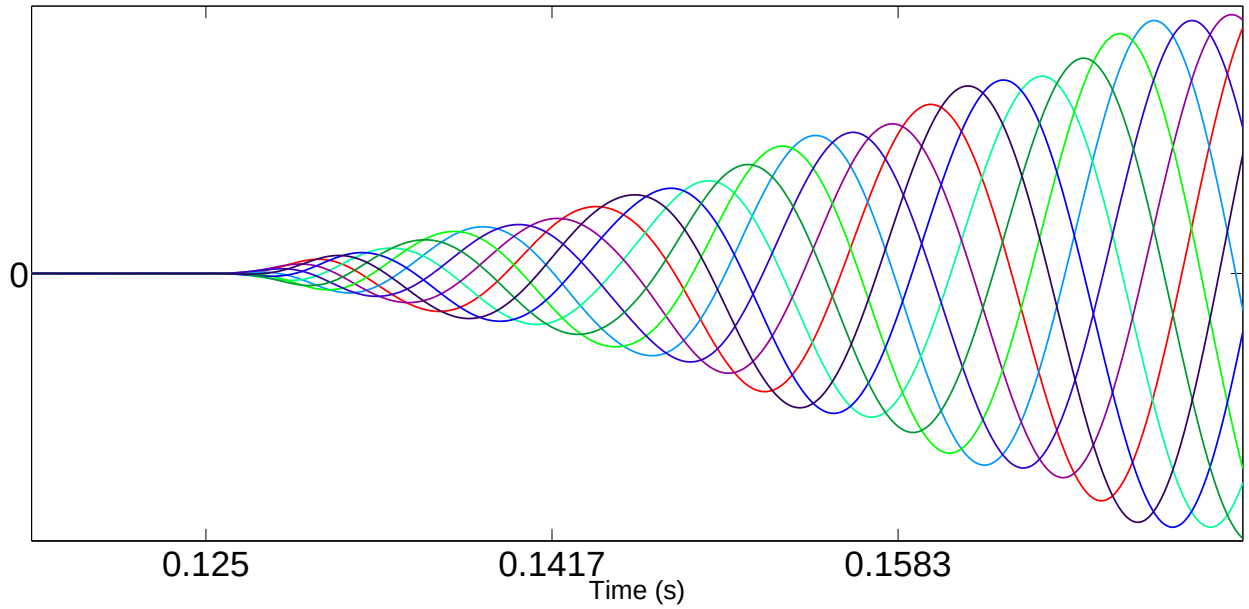

Figure 4.5: Output of the band-pass filter with reference circuit switch closure at $t_s = .125$ and zero initial power $P_{3\Phi}(t_s^-) = 0$.

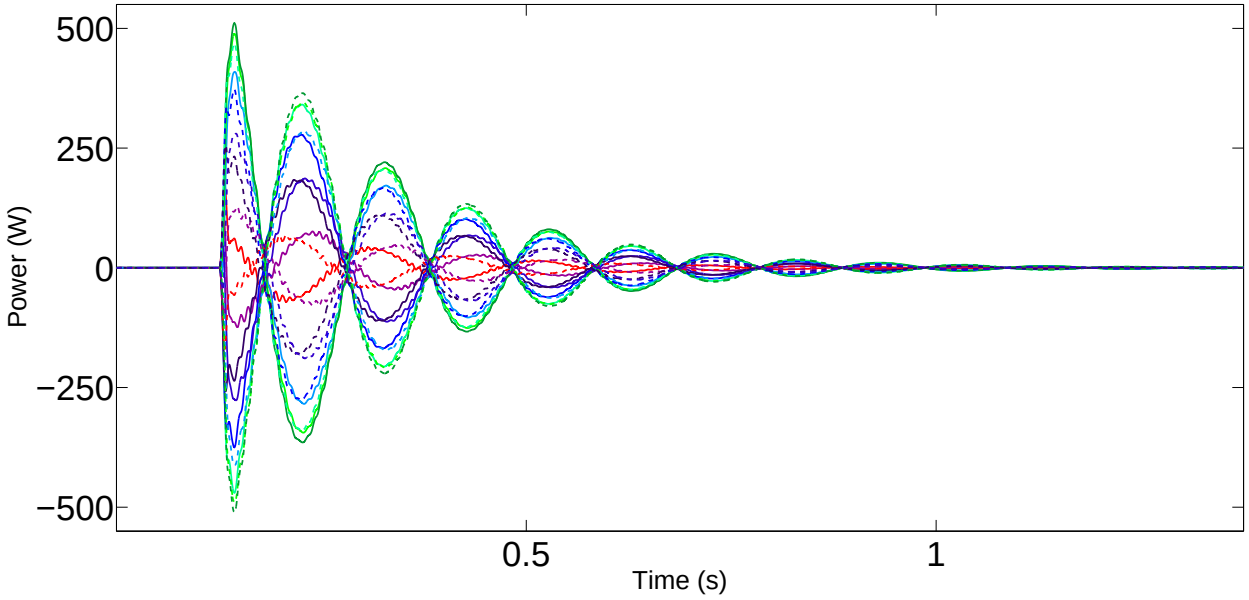

Figure 4.6: Demodulated active power transient $P_{Gm}(t_n)$ for all candidates $m \in 1, 2, ..., 18$.

As seen in Fig 4.6, these π-radian phase differences between candidates result in symmetry around zero in the respective demodulated power transients $P_{Gm}(t_n)$. Signals $P_{Gm}(t_n)$ are

found at position (B) in Fig. 4.4. The differences in amplitude of $P_{Gm}(t_n)$ signals result from the different $\cos(\phi_m)$ terms as discussed in Section 3.3.1. Revisiting the generic description of AM demodulation from (3.50):

$$\begin{aligned} I(t)\cos(\omega_c t)\cos(\omega_c t) &= I(t)\frac{1}{2}[1+\cos(2\omega_c t)], \\ I(t)\cos(\omega_c t)\cos(\omega_c t-\pi) &= -I(t)\frac{1}{2}[1+\cos(2\omega_c t)]. \end{aligned} \tag{4.4}$$

This will be leveraged.

As mentioned in Chapter 3, demodulation destroys any DC offset in a signal, so the signals in Fig 4.6 represent only the demodulation of the transient response $P_{h3\Phi}(t_n)$; the steady state part $P_{p3\Phi}(t_n)$ will be addressed later. In Fig 4.6, symmetric signals are color-matched, and the color assignments are consistent for all figures pertaining to the mk0 loop architecture for ease of interpretation. Of the color-matched signals, one is solid, the other dashed to allow differentiation.

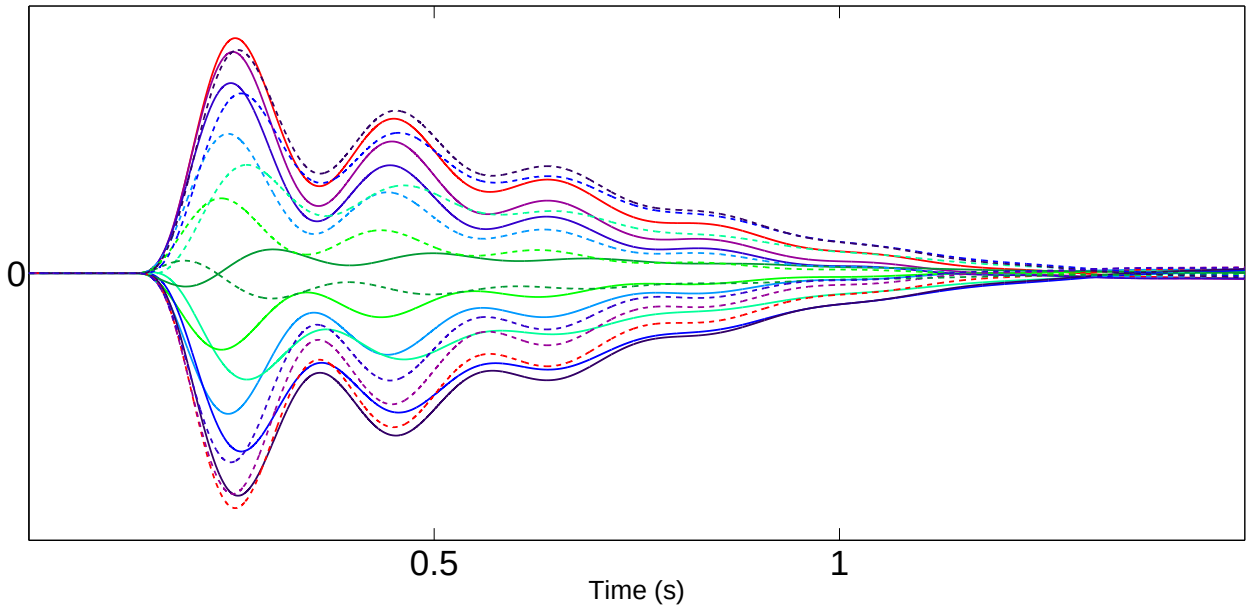

Figure 4.7: Band-pass filter output demodulated with the in-phase candidate signals $c_{Im}(t_n)$ for all candidates $m \in 1, 2, ..., 18$.

As seen in Fig. 4.4, at location (C), the signals $c_{Im}(t_n)$ are the band-pass filter output $g_m(t_n)$ demodulated by in-phase candidates $\tilde{v}_m(t_n)$. Comparison of demodulated power $P_{Gm}(t_n)$

in Fig. 4.6 and $c_{Im}(t_n)$ signals shown in Fig. 4.7 reveals approximate proportionality

$$\cos(\phi_m) \propto \left| \frac{1}{c_{Im}(t_n)} \right|. \tag{4.5}$$

Relationship (4.5) could be helpful for identifying the best demodulated signal $P_G(t_n)$. Unfortunately, the minimum $c_{Im}(t_n)$ has zero crossings which would prevent using it to identify if $P_G(t_n)$ is inverted or not, so phase ambiguity remains an issue.

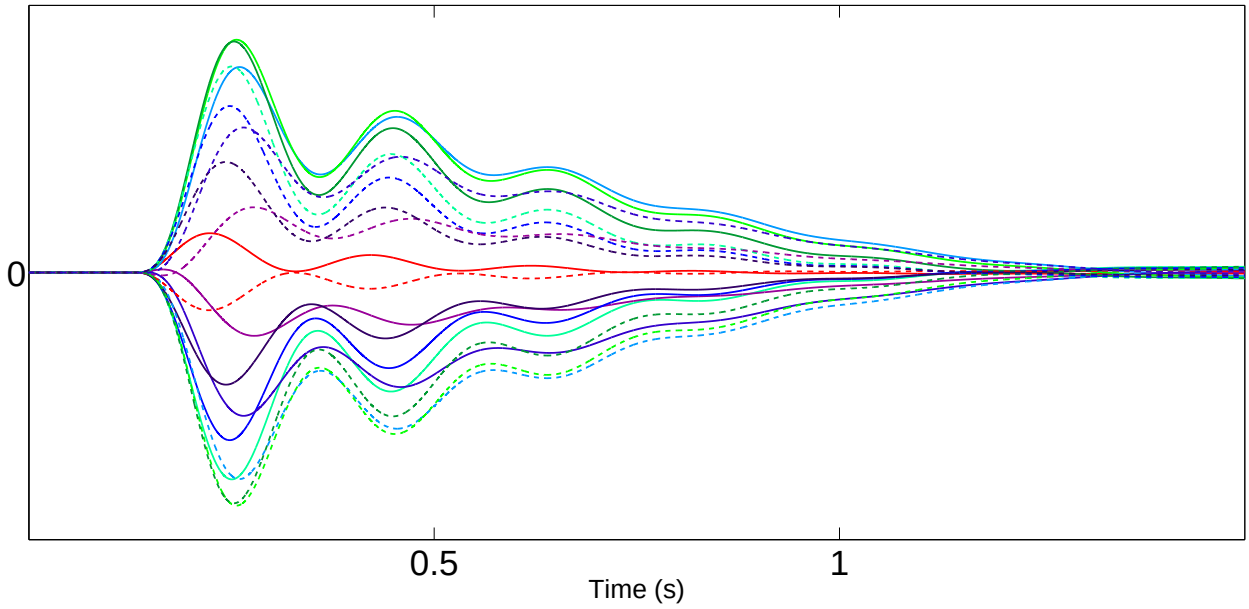

Figure 4.8: Band-pass filter output demodulated with the quadrature candidate signals $c_{Qm}(t_n)$ for all candidates $m \in 1, 2, ..., 18$.

A more valuable observation comes from comparison of Figs. 4.6 and 4.8, where

$$\cos(\phi_m) \propto c_{Qm}(t_n). \tag{4.6}$$

Signals $c_{Qm}(t_n)$ at position (D) in Fig. 4.4, are $g_m(t_n)$ demodulated by candidate quadrature signals $\tilde{v}_m^{-90}(t_n)$. The $c_{Qm}(t_n)$ signal corresponding to the best demodulation $P_G(t_n)$ remains negative through the duration of the transient if $P_G(t_n)$ is inverted, and positive if not. Then, the sign of this signal may be used to determine if $P_G(t_n)$ is inverted, overcoming the issue of phase ambiguity. Unfortunately, as seen in Fig. 4.8, the $c_{Qm}(t_n)$ with maximum magnitude does not consistently

correspond to the best demodulation $P_G(t_n)$.

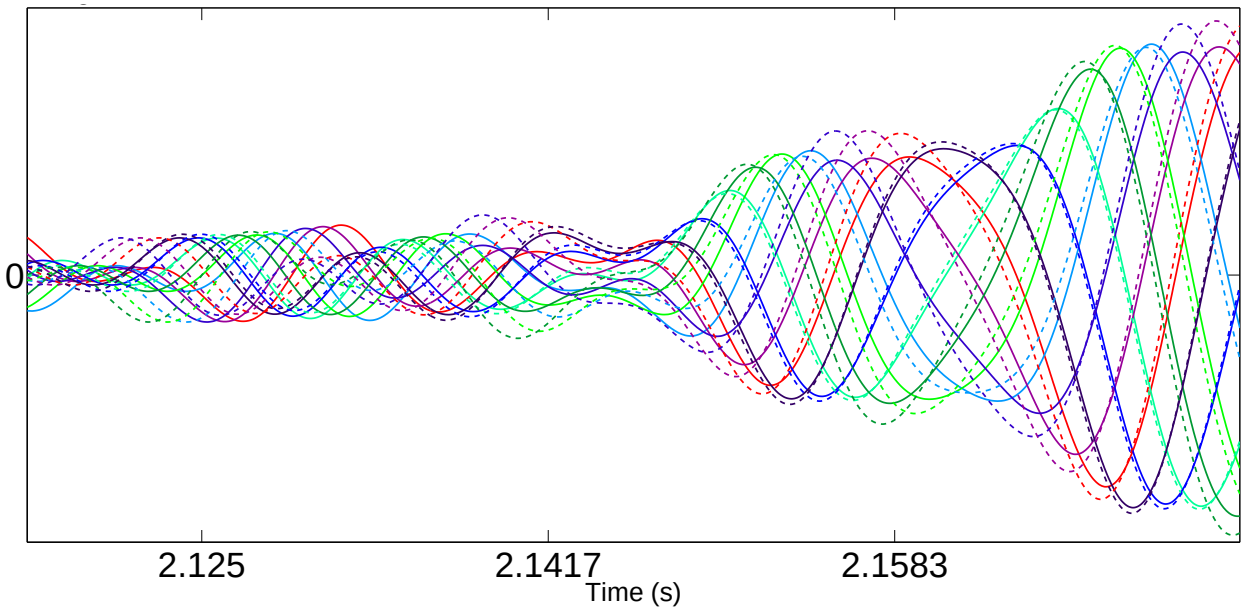

Figure 4.9: Output of the band-pass filter with reference circuit switch closure at $t_s = 2.125$ and nonzero initial power $P_{3\Phi}(t_s^-) \neq 0$.

A severe limitation of the mk0 architecture is that it only functions correctly when the active power input at (E) in Fig. 4.4 is initially zero, i.e. $P_{3\Phi}(t_s^-) = 0$. Figure 4.9 depicts the band-pass filter outputs $g_m(t_n)$ when $P_{3\Phi}(t_s^-) \neq 0$. While, in Fig 4.5, the $g_m(t_n)$ signals immediately resolved into grid frequency sinusoids with phase differences dependent on those of the respective candidates, interference from grid-frequency components of nonzero initial power delays that resolution, notable in the non-sinusoidal shapes of signals in Fig 4.9. In the figure, the $g_m(t_n)$ signals do not take on a sinusoidal shape for more than two cycles into the transient. The nonzero initial condition also causes divergence of signals demodulated by candidates with π-radian phase differences. This results in poor correlation in terms of relations (4.5) and (4.6) and degrades the feasibility of making use of symmetry of signals. This limitation makes the mk0 architecture not viable. If selection of the best demodulation $P_G(t_n)$ is based off the minimum valued $c_{Im}(t_n)$ and inversion determined by sign of the corresponding $c_{Qm}(t_n)$, then the selection will be sub-optimal if there is nonzero initial power. Fortunately this limitation is solved with a straightforward change to the algorithm input.

4.4 Optimization

The mk0 architecture depicted in Fig. 4.4 validated the approach, but suffers crippling limitations. The aim is to implement a demodulation algorithm on an FPGA, so improvements to the design have competing needs between overcoming limitations and reduction of the computational load.

The GOLD method loop architecture depicted in Fig. 4.10 capitalizes on the observations discussed in the previous section. In the figure, the block marked 'SIGN' is a sign function, the block marked 'ID' identifies the best demodulation and the 'CH' blocks are channel selectors where the output is the channel selected by the ID block. Note the (#) markers will not all be discussed in this section, but are made consistent with those used in the discussion in Chapter 5 for ease of reference.

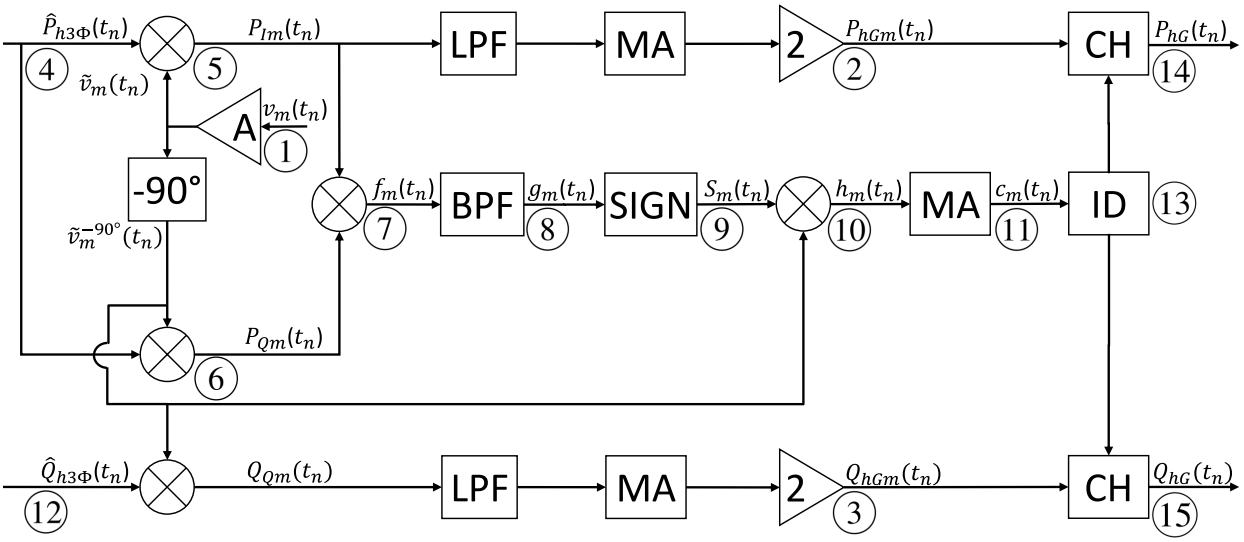

Figure 4.10: The final GOLD method architecture.

In the mk0 architecture, the amplitudes of band-pass filter outputs $g_m(t_n)$ survived demodulation into $c_{Qm}(t_n)$, preventing use of those signals to identify the best demodulation $P_G(t_n)$. At (9) in Fig. 4.4, a sign function applied to the band-pass filter output signals $g_m(t_n)$ removes the unwanted amplitude effects while retaining the desired phases in square waves $S_m(t_n)$. Formation of a square wave from sine functions is a common introductory lesson in Fourier series [69].

Recall, the solution to the exercise is

$$\text{Sign}(\sin(\omega t)) = \frac{4}{\pi}\sum_{r=0}^{\infty}\sin[(2r+1)\omega t]. \tag{4.7}$$

As seen at (10) in Fig. 4.10, these signals are multiplied by candidate quadrature signals $\tilde{v}_m^{-90}(t_n)$ forming signals $h_m(t_n)$. Application of the product-sum trigonometric identity (3.43) on the candidate quadrature signal $\tilde{v}_m^{-90}(t_n)$ and the individual sines forming the argument of the sum in (4.7) guarantees that the frequency content of $h_m(t_n)$ signals consists entirely of $2\omega_c$ and higher harmonics, making the moving average filter at (11) ideal for smoothing the signal and making the low-pass filter used in mk0 unnecessary. Figure 4.11 is the Bode magnitude plot of a FIR moving average filter, note the effect of suppressing frequencies $M\omega, M \in \mathbb{Z}$ where $\omega = 2\pi/P$ is the angular frequency corresponding to period P of the filter window. In the figure, $P = .016$s, $\omega = 120\pi$.

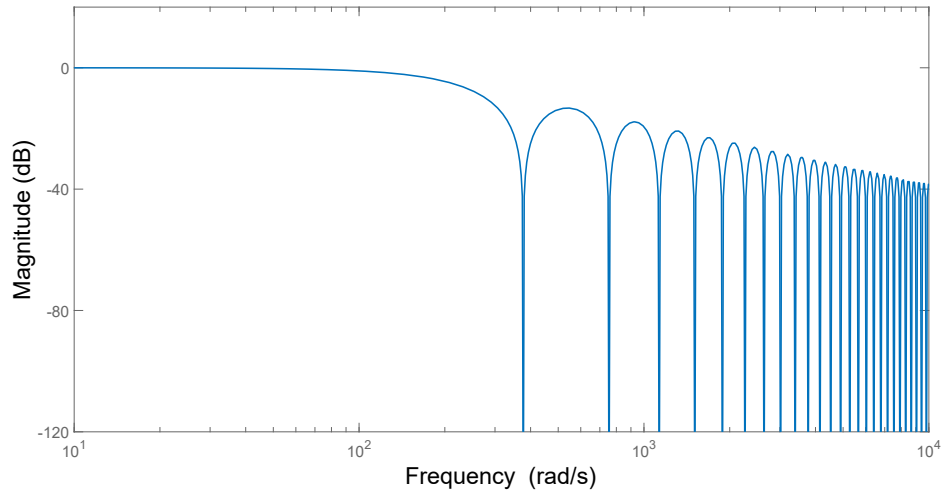

Figure 4.11: FIR moving average filter Bode magnitude plot.

The moving average is denoted by $c_m(t_n)$, and has proportionality relationship

$$\cos(\phi_m) \propto c_m(t_n). \tag{4.8}$$

The relation between sign of $c_m(t_n)$ and inversion of $P_{Gm}(t_n)$ is also maintained, Fig. 4.12 shows demodulation done by the GOLD method and the corresponding $c_m(t_n)$ signals, illustrating these

properties. Since the best candidate for demodulation can be determined from $c_m(t_n)$, as well as whether the signal is inverted, the $c_{Im}(t_n)$ branch (Ⓒ in Fig. 4.4) of the mk0 architecture is superfluous. Use of a sign function has made the in-phase demodulation branch of the mk0 obsolete, and simplified the demodulation of the quadrature branch, significantly reducing the FPGA footprint.

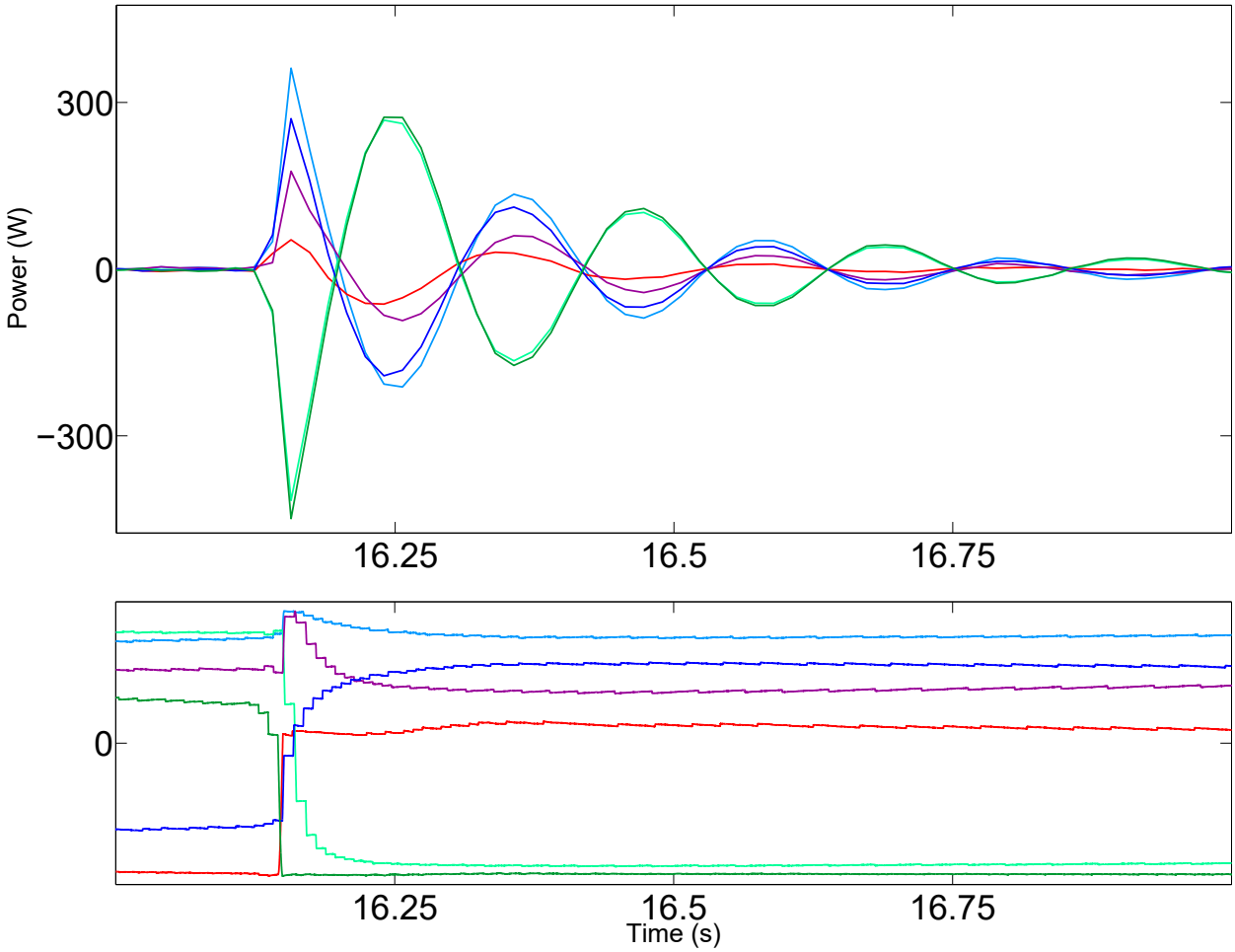

Figure 4.12: GOLD method demodulation active power demodulation signals $P_{Gm}(t_k)$ and candidate selection signals $c_m(t_n)$.

Use of symmetry further reduces FPGA resources needed. For demodulation by candidates $\tilde{v}_1(t_n)$ and $\tilde{v}_2(t_n)$ with $\phi_1 = \phi_2 - \pi$, from (4.4) $P_{G1}(t_n) = -P_{G2}(t_n)$. Thus $P_{G2}(t_n)$ comes free with a sign change of $P_{G1}(t_n)$ rather than separate demodulation. Note that the demodulated signals depicted in Fig. 4.12 are no longer mirrored by symmetric signals as in the mk0. This allows equal performance in terms of e_{max} with half the candidates.

Recall that in (4.2), max error e_{max}, was defined under the assumption that candidates be evenly spaced across 2π radians. With use of symmetry

$$\theta^*_{max} = \frac{\pi}{2C}. \tag{4.9}$$

With this use of symmetry, the logic implemented in the ID block at (13) of Fig. 4.10 determines $c_G(t_n) = \max_{m\in\{1\ldots C\}} |c_m(t_n)|$, as well as the sign of $c_G(t_n)$. This information is sent to the channel selector block marked CH at (14) in the figure where the quadrature candidate $\tilde{v}_G^{-90}(t_n)$ resulting in $c_G(t_n)$ corresponds to in-phase candidate $\tilde{v}_G(t_n)$ resulting in best demodulation $P_G(t_n)$. The sign of $c_G(t_n)$ determines if correction for inversion is called for. As can be seen in the figure, there is a similar channel selector box for reactive power at (15), where instantaneous reactive power $Q(t_n)$ is demodulated by the candidate quadrature signals $\tilde{v}_1^{-90}(t_n)$, making use of the quadrature relationship established in (3.49).

The simulations of the mk0 architecture used number of candiates $C = 18$, reducible to 9 using symmetry. As seen in Fig. 4.12, only six candidates are used. Reduction from nine candidates to six has corresponding increase of maximum amplitude error e_{max} from 1.5% to 3.4%, but this increase in error is tolerated to reduce FPGA resources needed while making possible another improvement.

The delay used for formation of candidate quadrature signals is fairly long at a quarter cycle. This delay can be reduced to 1/12 cycle through use of symmetry and selecting candidate phase differences at $\pi/6$ as shown in Fig. 4.13. Take as example candidate formed from phase 'a' voltage denoted in the figure by $\tilde{v}_a$: As can be seen in the figure, the phase of quadrature signal $\tilde{v}_a^{-90}$ coincides with $-\tilde{v}_b^{-30}$. However, this is only possible if three candidates have phase/delay of $\pi/12$. That phase would not occur with nine candidates evenly spaced similar to those in Fig. 4.13, and reduction of candidates was preferred to conserve FPGA resources.

Finally, since the steady state part of power causes problems in the mk0 performance, removal of the steady state part is a reasonable solution, especially since the demodulation was

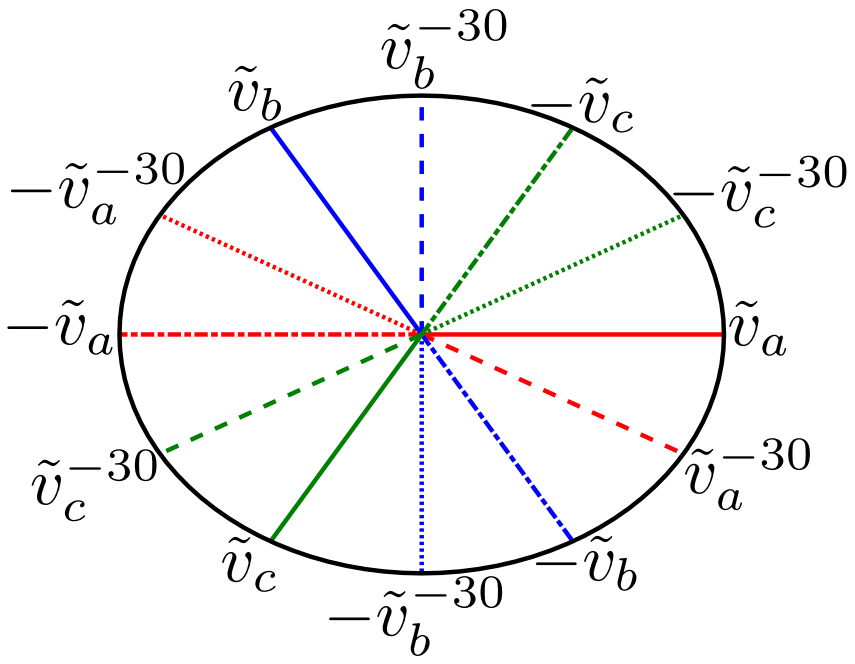

Figure 4.13: The phases of candidates.

only intended to capture transient effects anyway. Since demodulation removes the DC offset from a signal, recreation of the steady state part of the power signal was already necessary. A low-pass filter and moving average filter applied to power approximate the steady state part:

$$\hat{P}_p(t_n) = F_{MA}(q)F_{LP}(q)P(t_n). \tag{4.10}$$

Then the transient response can be approximated by

$$\hat{P}_h(t_n) = \hat{P}(t_n) - \hat{P}_p(t_{n-1}). \tag{4.11}$$

The term $\hat{P}(t_n)$ is active power filtered to remove harmonics, and will be discussed in Chapter 5. Note $\hat{P}_p(t_{n-1})$ has one sample delay, as the value calculated on one sample may be held in memory, making it immediately available for subsequent use. This is justified because the combination of moving average and low-pass filter causes the signal to vary only slightly from one sample to the next, particularly when sampling is done at high frequency.

At steady state $\hat{P}_h(t_n)$ is zero, overcoming the greatest limitation of the mk0 loop architecture at cost of a single subtraction operation per (4.11).

4.5 Comparison to Ideal

The Step-Based Realization Algorithm (SBRA) presented in [64] is used to form a model from demodulated power, and [75] provides a method for extracting model parameters (Damping Attenuation, Natural Frequency) from realized models. Use of SBRA allows data from a complex system to be used to form a reduced-order model without intimate knowledge of the architecture of the system; in the case of the reference circuit, the architecture is intimately known, and familiarity provides way points in analysis. The SBRA procedure is summarized in Chapter 6.

Table 4.1: Parameters of Realized Models

	$f_0 = \frac{1}{2\pi\sqrt{RL}}$	$\eta = \frac{R}{2L}$
Theoretical Values	5.033	10.000
Ideal sample timing	5.033	10.000
GOLD method with C=6		
Max	5.115	10.704
Min	5.012	9.826
Median	5.048	10.373
Mean	5.056	10.289
Standard deviation	0.032	0.236

Realization was performed on averaged signal data taken over 3600 simulations. The realization parameters are compared to theoretical values and those of ideally timed sampling discussed in Chapter 3, allowing a gauge of how well the GOLD method reproduces the desired signal. As expected, when realization was performed on data taken with ideal sample timing, the SBRA provided a second order model for the reference circuit. The natural frequency and attenuation factor from the resulting model match with theoretical values with minimal difference.

Realization performed on GOLD method simulations resulted in third order models, the higher order due to delay/filtering effects. Statistical details are provided in Table 4.1. As can be seen in the table, the variation of natural frequency from the ideal is less than 2% in the most

extreme case, while averaging less than 0.5%. The damping attenuation varies by as much as 7% from the ideal case, but averages less than 3%. The higher variation of damping attenuation is caused by filter and initial condition effects, as well as the inherent error in the GOLD method as an open loop approach.

4.6 Implementation

The design choices discussed in the previous section significantly reduced the FPGA footprint of the open loop demodulation method depicted in Fig. 4.10. As mentioned in Chapter 1, FPGA programming depends on in-depth understanding of how computing hardware performs mathematical functions. While it is general knowledge that computers handle information in purely binary form, FPGA programming requires specific understanding of how binary operations accomplish desired effects in order to make appropriate use of those operations.

A simple example is bit shifting. At the hardware level, a number is represented by a binary sequence, referred to as a 'word' with whole numbers denoted 'integers' and fractional numbers 'fractions.' E.g. the number 23.5 is 10111.1 in binary, with word 101111, integer 10111 and fraction 1. Each binary value, i.e. each one or zero in the word is referred to as a 'bit.'

Just as a base 10 number can be quickly divided or multiplied by powers of 10 by shifting the position of the decimal point, a fast way to perform multiplication (or division) of binary numbers by a multiplier (or divisor) of form $2^n, n \in \mathbb{Z}$ is also by moving the decimal point. E.g. 23.5/8 has binary representation 10.1111, the word remains the same, while the decimal shifted three bits to the left when dividing by 2^3. Bit shifting is valuable because it requires very little computing effort compared to normal division [76].

Of course, if division requires a divisor that is not an exact power of two, bit shifting cannot be invoked. However, as will be shown, often in FPGA programming division is done with aim of adjusting scale of a number. In these cases an appropriate power of two is selected, and scale adjusted via bit shifting, sparing FPGA resources for use elsewhere. Naturally, any scaling would

be reversed later as needed.

These sort of scaling operations are important because of the data types used by an FPGA. Typically, an FPGA has no floating point processor. Implementation of a floating point processor within the FPGA would be time consuming, but more importantly it would require allocation of finite FPGA resources. Rather than floating point numbers, an FPGA uses fixed point. When a number is represented in fixed point, word length can be specified by the precision needed in the application, and a separate sequence specifies the radix point, i.e. the position of the decimal. By contrast, floating point numbers consist of two fixed point numbers of prescribed length, the significand and exponent, and the precision and range of values that can be expressed is a matter of the total number of bits of floating point number. Most floating point numbers use a total 32 or 64 bits, referred to as single and double precision, though formats with greater and lesser precision exist as well [77]. As example, double precision floating point numbers use 53 bits to express the significand, 10 bits for exponent and one bit for sign.

Double precision floating point numbers are suitable for most applications, and because modern microprocessors have integrated floating point calculation units, for mathematical operations performed on microprocessors, concerns with precision might never arise. A major benefit of floating point is that when working with floating point numbers one need not worry about overflow, underflow or round off error [33] except in the most extreme cases. By contrast, these are all ever present concerns when working with fixed point numbers. Fixed point numbers have no exponent, greatly reducing the range of numbers that can be represented. Overflow and underflow are related concepts; overflow occurs when a number is larger than can be represented with given integer length, while underflow occurs when a number is too small to be represented with given fraction length. Standard responses to overflow are truncation of the greatest bits, or by imposing a saturation condition; in either case it is better avoided if possible.

Figure 4.14 shows the FPGA implementation of the GOLD method in the LabVIEW graphical programming environment. Blocks marked 'LP' are low-pass filters, 'BP' band-pass filters, 'FIR' FIR moving average filters, '$\otimes$' multiplication and the '?' block selects the best demodulated

signals.

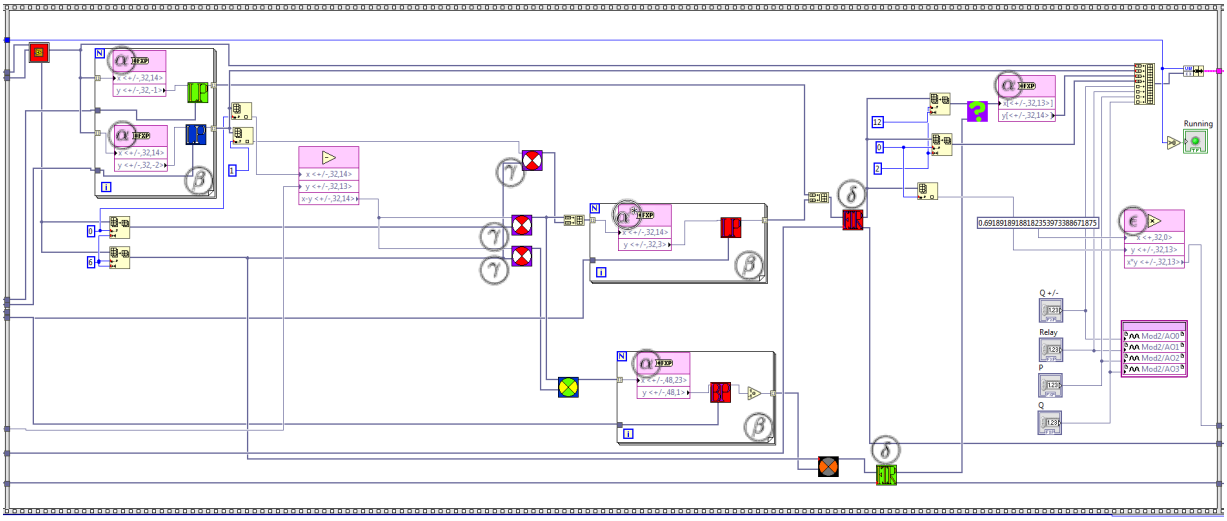

Figure 4.14: LabVIEW FPGA implementation of the GOLD method.

A concrete example of where scaling becomes important is the band-pass filter used in the GOLD method. The filter input values can vary over a very broad range: from order 10^0 since $\hat{P}_h(t_n) = 0$ at steady state, up to order 10^6 immediately following closure of the reference circuit switch. The value 10^6 comes from the following rationale:

- From simulations, $\max_{t_n > t_s} [P(t_n)] \approx 1540W$.
- As will be discussed in Chapter 5 equation (5.12) gives the band-pass filter input $f_m(t_n) = \frac{1}{2}\hat{P}_h^2(t_n)\sin(2\omega_c t_n - 2\phi_m)$.
- From equation (4.11), algorithm input $\hat{P}_h(t_n) = \hat{P}(t_n) - \hat{P}_p(t_{n-1})$.
- But the low-pass and moving average filters used to form $\hat{P}_p(t_{n-1})$ cause it to have much more delay than $\hat{P}(t_n)$, making $\hat{P}_h(t_s^+) \approx \hat{P}(t_s^+)$
- Then, the band-pass filter input $f_m(t_n) \leq \frac{1540^2}{2}$.

For acceptable accuracy of band-pass filter input $f_m(t_n)$ across the entire range from order 10^0 up to order 10^6, input precision must be enough to be useful at both extremes. Integer length 23 assures greater than 100% margin of error to overflow if $f_m(t_n) = \frac{1540^2}{2}$, while an additional

25 bits to the right of the decimal assures accuracy to seven significant figures (base 10), for total precision of 48 bits.

Simultaneously, band-pass filter coefficients are on order of 10^{-7}, and need a high degree of precision. As shown in Fig. 4.15, the band-pass filter has poles very near the unit circle, and rounding error could lead to instability.

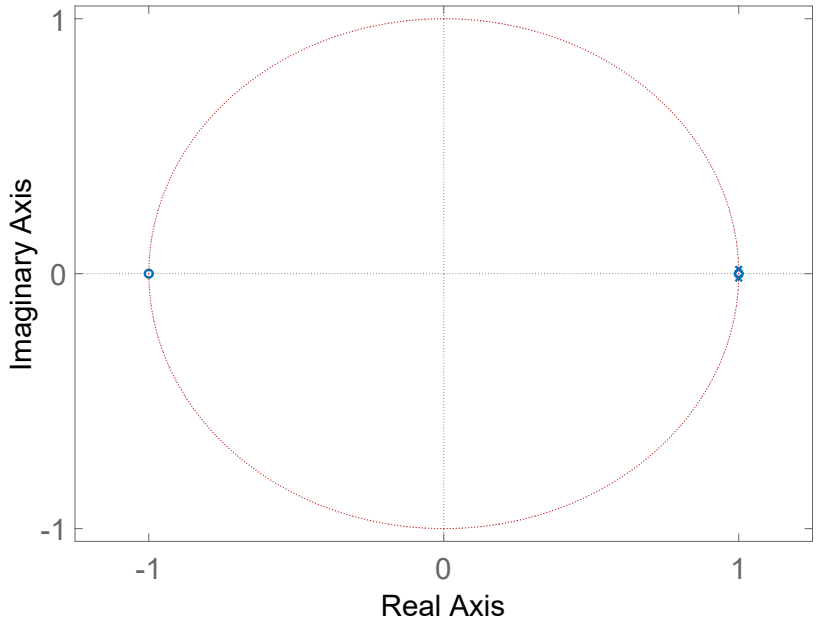

Figure 4.15: Pole-Zero map of band-pass filter

Coefficients are stored as fixed point numbers with 40 bit word length and decimal at -22 bits. It is tempting to retain all precision in the product, that is 23 bit word length of the input, plus 40 bit fractional precision of the coefficients, plus 22 bits between the decimals, for total of 85 bits precision. Not only would this exceed the 64 bit precision limit for fixed point numbers, it fails to appreciate that the respective scales of the input and coefficients offset one another. 85 bit precision would lead to roughly 21 bits of integer precision that would be unused even at the highest power output, as well as another 16 bits on the product fraction that would be carrying a level of precision that loses meaning due to the lesser precision of the multipliers.

A solution to this inflated precision is to bit shift the filter input $f_m(t_n)$ down by 22 bits as seen at the position marked $\textcircled{\alpha^*}$ in Fig. 4.14. To compensate, the coefficients are shifted up by 22 bits in a separate section of the FPGA program. Then a 48 bit result has no unused bits, and is

most accurate when $f_m(t_n)$ is near 10^6, while remaining accurate near steady state values. Similar scaling was done on other filter inputs and coefficients to limit the precision needed for all signals, marked by (α) in Fig. 4.14.

Up to this point selecting a precision of signals that is no more precise than necessary has been presented as a design goal without explicitly stating the motivation. On the FPGA, multiplication and addition are performed by DSP48 logic blocks. DSP48 logic blocks have limited precision for inputs, and the FPGA compiler will arrange for mathematical operations with greater precision than available in a single DSP48 by cascading excess bits into additional DSP48s [78], making a small increase in precision potentially lead to doubling the number of DSP48s used. The GOLD method algorithm requires many concurrent mathematical operations, so a doubling of DSP48s can quickly exceed those available on the FPGA.

Besides careful attention to the precision of all signals, the consumption of FPGA resources can be limited by coding for reuse of resources. Rather than true simultaneous operations, for-loops are utilized when possible. This slows down cycle time, and complicates filter implementation slightly, as delays must be adjusted for looping. For instance, given a delay operation q^{-1} in a filter transfer function, if the filter is used by six channels in a loop the delay must be implemented as q^{-6} to actually capture the respective single-cycle delay of each channel, and similarly for higher delay values. For-loops containing filters are marked by marked by (β) in Fig. 4.14.

Another opportunity for reuse of FPGA resources is construction of reusable functions and setting execution as 'non-reentrant,' meaning that the FPGA compiler will implement the function once and reuse that implementations rather than creating another. The $\otimes$ blocks marked by (γ) in Fig. 4.14 were implemented this way, greatly reducing the number of DSP48s required.

The FIR moving average filters at positions (δ) in Fig. 4.14 are important for removing frequency content matching to the windows size, and higher harmonics thereof. Inefficient implementation of a moving average could call for many more computing resources than available. A moving average filter is given by

$$F_{MA}(q) = \frac{1}{N}[1 + q^{-1} + ... + q^{-N+1}] \tag{4.12}$$

where N is the windows size. The GOLD method uses a FIR filter with N_1 corresponding to the number of samples per cycle for demodulation at (2) and (3) in Fig. 4.10, and another with $N_{\frac{1}{2}}$ set to a half cycle at (11), discussed above.

Implementation as written in (4.12) would require $N-1$ addition operations for every signal filtered. However, an efficient algorithm recognizes that only the first and last values change on any given cycle, and the filter can be implemented by keeping a running sum in memory and only adding the most recent value and subtracting the q^{-N} value:

$$F_{MA}(q) = \frac{1}{N}[\sum_{k=-1}^{N-1} q^{-k} + 1 - q^{-N}] \tag{4.13}$$

thus reducing the filter from $N-1$ addition operations to two. Of course, an N value that is a power of two also allows division by bit shifting.

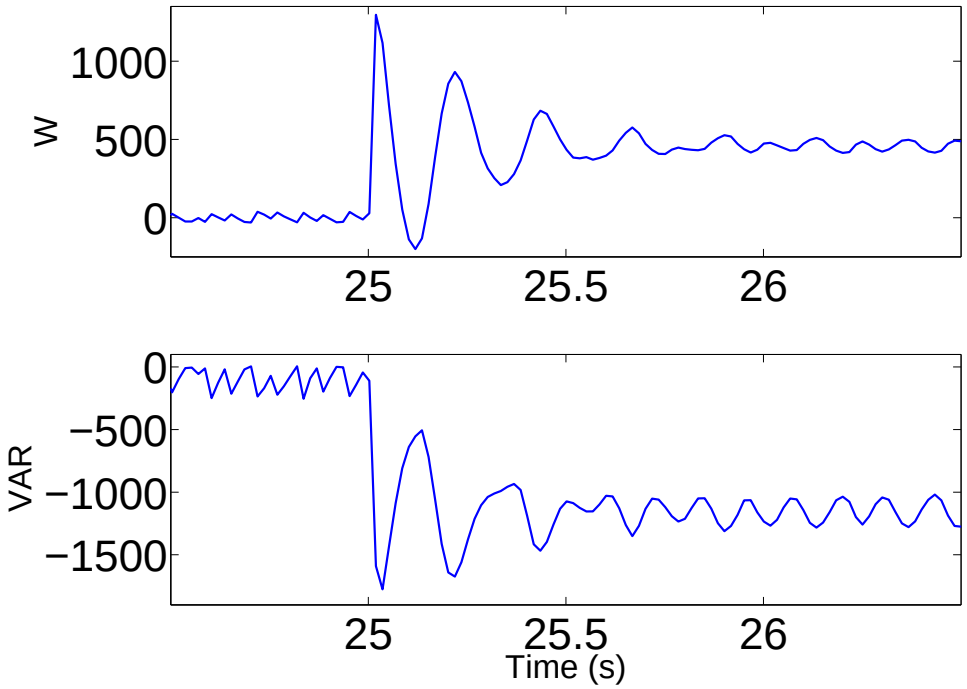

Figure 4.16: Demodulated active (top) and reactive power with 256 samples per cycle.

Unfortunately, when sampling at 256 samples per cycle considerable aliasing effects were encountered, as shown in Fig. 4.16. FPGA timing limits were exceeded with 512 samples per

cycle, introducing sample jitter. The highest sampling rate possible without jitter was 370 samples per cycle, found by iterative timing adjustment and checking for jitter. To scale down the running sum from (4.13), 256 bit bit-shifting was used and a single multiplication operation (i.e. by 256/370) at $\textcircled{\epsilon}$ in Fig. 4.14 was used to correct the scale of $\hat{P}_p(t_n - 1)$, required for (4.11). All other corrective scaling was performed by the microprocessor on down sampled algorithm outputs. Figure 4.17 illustrates the improvement in signal quality achieved by operating the FPGA at its sample timing limit.

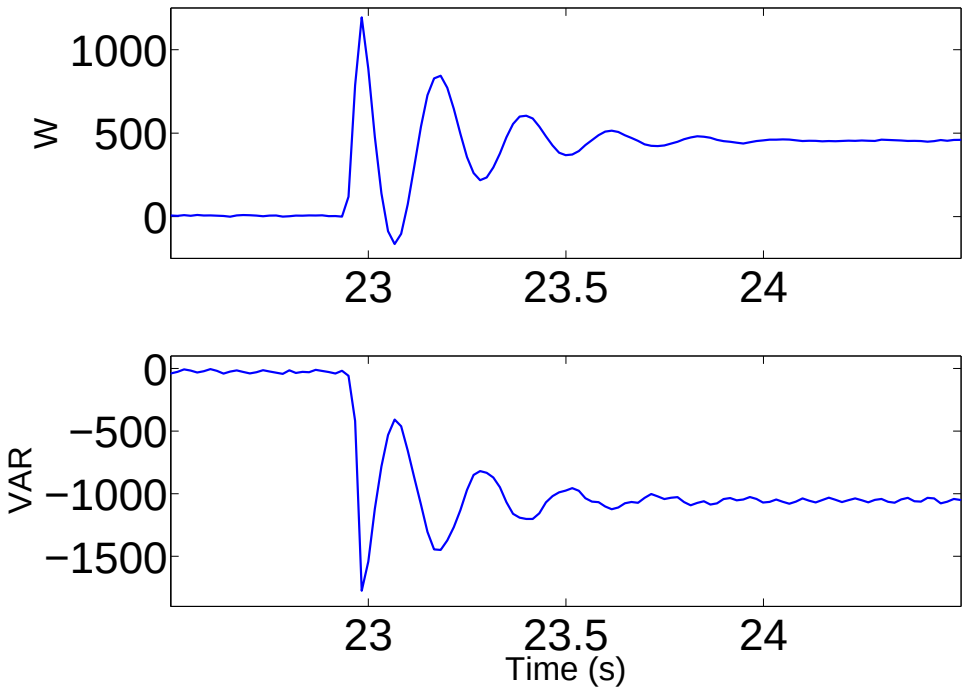

Figure 4.17: Demodulated active (top) and reactive power with 370 samples per cycle.

Figures 4.16 and 4.17 show the demodulated active and reactive power signals as they are read by the microprocessor. That is, the best demodulation $P_G(t_n)$ selected, added to the reconstructed DC offset $\hat{P}_p(t_n)$, this sum is down-sampled to a single value per cycle. The control discussed in Chapter 6 is a simple implementation of a controller transfer function on the microprocessor. As mentioned in Chapter 1, the outstanding data manipulation and visualization capabilities of microprocessors allows data read-write operations to be performed simultaneously with control.

4.7 Conclusions

This chapter presented Costas loop as an existing solution to demodulating DSB-SC signals, and demonstrated limitations when it was applied to demodulation of power transients. The first limitation, the effect of signal magnitude one the voltage control oscillator output, was overcome by using normalized voltage signals rather than a VCO. The second limitation was partly overcome simultaneously, as normalized voltage signals have the correct frequency exactly, since voltage is the forcing function of power transients; the aim of the research presented in this chapter was to determine, as close as possible, the correct phase to use for demodulation. The final limitation of Costas loop, phase ambiguity, was overcome by recognizing a relationship between voltage quadrature signals and the output of the band-pass filter placed where the VCO input is on a Costas loop.

Chapter 5 presents the Gwynn Open Loop Demodulation (GOLD) method in its final form, but of course the design process was incremental, only arriving at the form presented in Chapter 5 after considerable analysis. This chapter discusses the evolution of the design from conception through its fully functioning implementation on the field programmable gate array (FPGA).

Particularly important was consideration of the constraints caused by limited FPGA resources. Several FPGA implementation strategies were presented, which were used to limit the number of logic blocks used and reuse already deployed hardware when possible. Chapter 5 presents mathematical analysis of how the signal processing done in the GOLD method algorithm accomplishes the qualitative behavior discussed in this chapter, as well as one key issue that has not been discussed. An adjacent DC-AC inverter creates considerable harmonic distortion on power signals, severely complicating the task of demodulation.

Chapter 5

Demodulation of Three-Phase AC Power Transients in the Presence of Harmonic Distortion

5.1 Nomenclature

This table of nomenclature is not comprehensive. It is provided to define symbols not explicitly defined elsewhere in the chapter, and as reference for symbols that are used outside the context of their initial definition within the text.

f_c	Grid frequency
N	Number of samples per f_c cycle
ω_c	Angular frequency of voltage input, $2\pi f_c$
ω_0	Reference circuit natural frequency

t_s	Time of reference circuit switch-closure
t_n	Discreet time variable with time step $\frac{1}{f_c * N}$
t_k	Discreet time variable with time step $\frac{1}{f_c}$
v_p	Voltage on phase 'p' where $p = a, b,$ or c
v_p^{-90}	Superscript '-90' indicates $-\pi/2$ radian phase shift on the signal
v_{pp+1}	Line voltage, $p = a, b,$ or c and $p + 1 = b, c,$ or a, respectively
V	Input voltage amplitude
$\tilde{v}_m$	'Candidate' signal 'm': normalized voltage, may be delayed
ϕ_s	Voltage phase at time of switch closure.
i_p	Current on phase 'p'
I_p	Steady-state current amplitude
I_h	Transient current amplitude
η	Reference circuit damping attenuation $\frac{R}{2L}$
α	Phase difference between steady-state current and voltage
β	Phase of three-phase power fluctuation
P	Three-phase instantaneous active power
P_p	Steady-state component of active power
P_h	Transient component of active power

$\hat{P}$	Filtered three-phase instantaneous active power
$\hat{P}_p$	Reconstruction of steady-state component of active power
$\hat{P}_h$	Estimated transient component of active power
P_{hGm}	Transient component of active power demodulated by $\tilde{v}_m$
P_G	Decoded active power signal
Q	Three-phase instantaneous reactive power
$\hat{Q}_h$	Estimated transient component of reactive power
f_m	Band-pass filter input 'm'
g_m	Band-pass filter output 'm'
F	Filter transfer function. Subscript denotes type:'LP'-low-pass; 'MA'-moving average; 'BP'-band-pass
B	Function representing error due to filtering
H	Harmonic order. $H \in 2, 3, 4...$

5.2 Introduction

With the advent of integration of renewable energy resources, more fluctuations and transient effects are observed on the electric grid [79], [80]. Operators have traditionally had no operational option to counteract them while in progress because of their short-lived nature and slow response of conventional AC generators [8]. Direct action is not always necessary though, because the large spinning mass of conventional generators possesses considerable rotational inertia, serving to help stabilize the grid [9]. However, the ever expanding penetration of renewable distributed

generation counteracts this effect, as it is predominantly in the form of photo-voltaic (PV) cells with little inertia [42]. As a greater portion of power provided to the grid comes from PV there is less rotational inertia per unit of energy distributed. This is of utmost concern as transients stress power systems and can result in cascading effects [81] and widespread damage [82].

Despite the low inertial effect, modern inverters could be programmed or controlled to simulate synthetic inertia [83]. Examples include droop control emulating generator response [12], [84]. Unfortunately, current supplied by typical PV inverters is inherently non-sinusoidal and may have multiple higher harmonics, distorting power quality and the ability to measure power fluctuations accurately. Such higher harmonics are caused by the use of square waves, modified sine waves or pulse width modulation (PWM) to create an AC current [28].

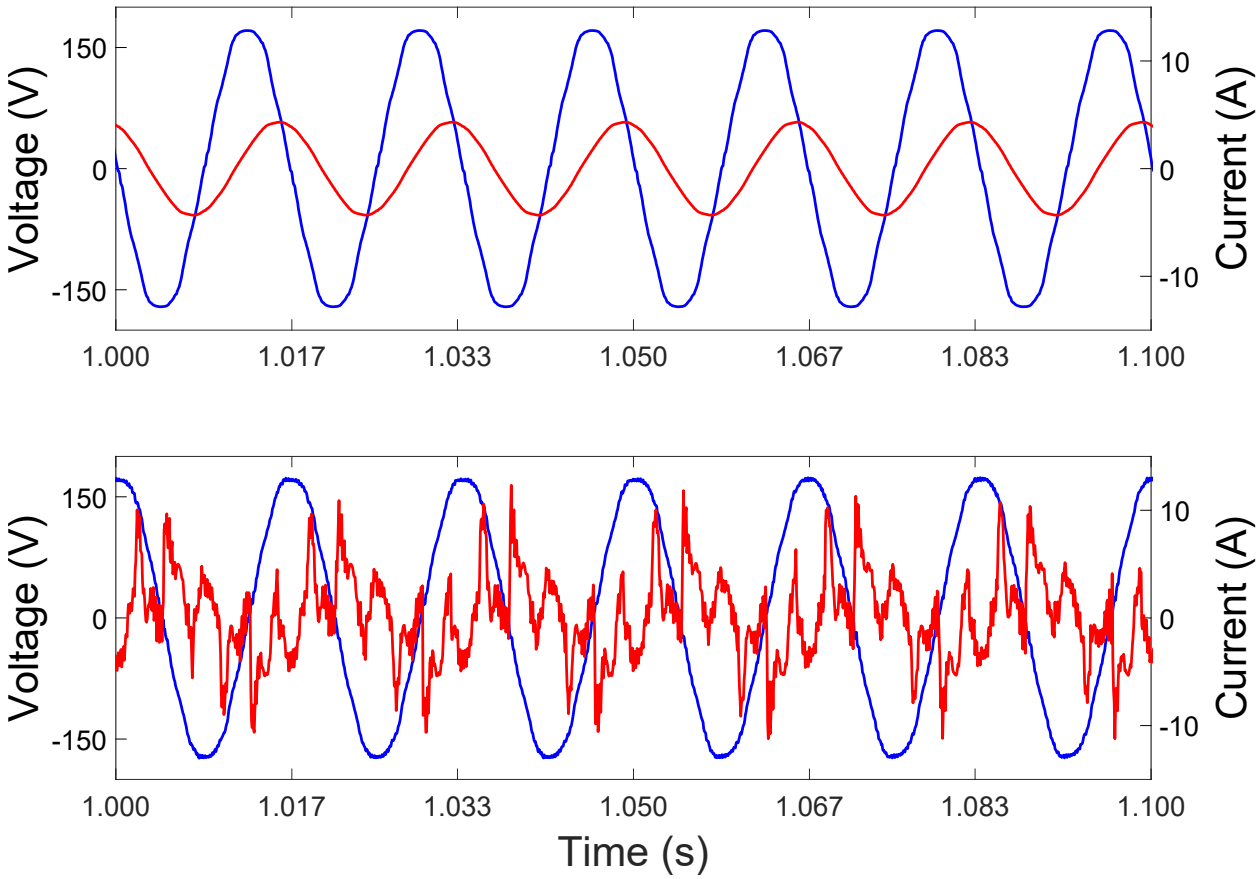

Figure 5.1: Wave form signals when inverter is off (top) and supplying power (bottom), illustrating harmonic distortion on inverter current.

An example of the distortion in AC current of a smart inverter is illustrated in Fig. 5.1,

where measurements of voltage and current waveforms are taken at 256 samples/cycle over a resistive and inductive load. The measurements are taken at the Synchrophasor Grid Monitoring and Automation (SyGMA) Lab at the University of California, San Diego (UCSD) and a comparison is made between grid supplied power (top) and inverter supplied power (bottom). It is clear that the inverter creates several harmonics on the current and it will be harder to qualify the active and reactive power flow produced by the inverter.

Despite the harmonic distortion that may be introduced by a smart inverter, the aim is to use the inverter to provide synthetic inertia to controlled active and reactive power in order to mitigate power oscillations. Such mitigation is typically done via feedback of measured power oscillations to the power demand signals sent to the inverter [67]. This necessitates clean power measurements to be used for feedback.

Active damping for the purpose of improving power quality from PWM inverters with inductor-capacitor-inductor (LCL) filters has been discussed in [30], [31], [32], among many others. However, in the United States power quality is regulated by standards tolerant of harmonic distortion [85], limiting adoption of those methods. Furthermore, retrofitting inverters with additional active damping components would be cost prohibitive. Instead, development of a method to extract high quality power flow signals and provide real-time damping control to the inverter is more practical.

One obvious way to eliminate the effect of higher harmonics is simple filtering of voltage and current signals. However, such filtering may influence and eliminate the measurement of power fluctuations or adversely impact the feedback control needed to mitigate power oscillations by the inverter.

Parameter uncertainty inherent in power systems dictates use of a controller utilizing the internal model principle [53], which can be implemented on a microprocessor as shown in [67]. However, demodulation of power is necessary for real time control [27] due to the response time of the microprocessor. As such, processing of three phase voltage and current signals with harmonics must be a trade-off between filtering and power oscillation demodulation.

Given the trade-off between filtering of harmonics and the need to demodulate power oscillations, this chapter describes an algorithm that extracts active and reactive power fluctuations in the presence of distortion with the aim of using the acquired signal for control of a smart inverter. The algorithm is a modification to Costas Loop to demodulate active and reactive power without need of *a priori* knowledge about the disturbance. Demodulation in the context of power calculations has been explored extensively for use in determining voltage frequency in Phasor Measurement Units [86], [87], [88], but limitations in the method for demodulating transients presented in [27] motivates the research presented in this chapter.

The demodulation approach from [27] makes an unconventional use of the Clarke transformation, mapping active power into the Clarke domain. Due to squaring and a subsequent square root operation, that algorithm provides accurate demodulation only when a transient initiates while both α and β Clarke components of active power are positive. An experimental setup can be contrived to assure this condition is met, but variations in grid parameters common in day-to-day operation make the algorithm unfit for general usage.

The contribution of this chapter is the formulation of a decoding algorithm characterizing real and reactive power flow even in the presence of large harmonic distortions as illustrated in Fig. 5.1. The novel decoding algorithm presented in this chapter allows characterization of the transient effect in power flow when loads are switched in without explicit knowledge of the dynamic parameters of the loads. Furthermore, unlike [27], reactive power is demodulated concurrently. Clearly, with better information on active/reactive power, control applications that use such active and reactive power measurements will also benefit.

To illustrate the effectiveness of the algorithm proposed in this chapter, the modified Costas Loop is implemented on a field-programmable gate array (FPGA) for real time processing and tested on power oscillations induced by switching in a three-phase reference circuit. The three-phase reference circuit is an RLC load that produces known oscillations in both active and reactive power and will serve as a reference to the actual demodulated active and reactive power.

5.3 AC Power Flow and Demodulation

5.3.1 Reference Circuit

Transient data from a live electric grid in response to a major disturbance such as a branch trip is sparse because such incidents are unplanned and most utilities use supervisory control and data acquisition systems sampling only every 2-4 seconds [89]. Such transient data is irreproducible due to utility obligations and customer expectations of continuity of service. However, any distribution electric grid of reasonable size will have a combination of inductive, capacitive and resistive elements, making a series RLC circuit a reasonable reference point for analysis of power flow during a transient. An RLC circuit allows design parameter selection such that transient response remains within limits of protective devices, minimizing impact on other grid customers while enabling laboratory recreation of fluctuations qualitatively similar to those witnessed on the local microgrid as shown in [67] and [27].

Consider Fig. 5.2, depicting a circuit with an ideal RLC series branch parallel with a purely resistive branch. This circuit serves as a reference in computer simulations and an actual physical implementation, at the SyGMA lab. Simulation of the reference circuit is used as a baseline for the power oscillations to be demodulated. The actual three-phase RLC circuit at the SyGMA lab is equipped with a smart inverter to provide realistic AC signals with possible distortion. Circuit parameters are as follows: v = 120V RMS AC at 60Hz, R_1 = 100 Ω, R_2 2 Ω, L = 0.1 H, C = 0.01 F. Note that L and C are higher than typical electric grid values, but were selected to allow reproduction of fluctuations with greater amplitude than otherwise possible on a low voltage circuit.

For $t \geq t_s$ (the time of switch closure) with $v(t) = V\sin(\omega_c t)$, current response is governed by an ODE with general solution

$$i(t) = I_p \cos(\omega_c t - \alpha) \tag{5.1a}$$

$$+ I_h(t_s) e^{-\eta(t-t_s)} \cos(\omega_0(t-t_s) - \beta_\phi(t_s)), \tag{5.1b}$$

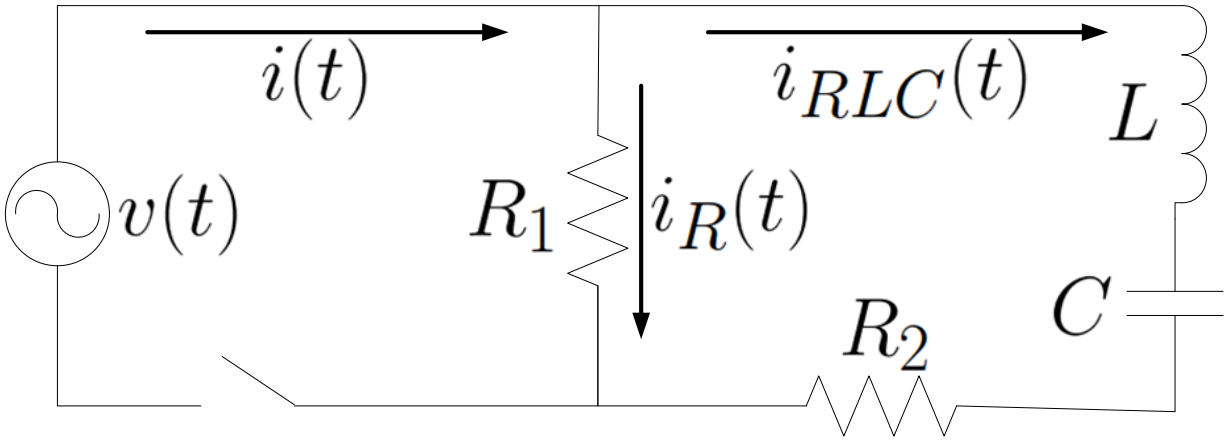

Figure 5.2: Reference circuit for creating a power oscillation.

where (5.1a) is the particular solution and (5.1b) is the homogeneous solution.

In 3-phase, consider $v_a(t) = v(t) = V\sin(\omega_c t))$, $v_b(t) = V\sin(\omega_c t - \frac{2\pi}{3})$ and $v_c(t) = V\sin(\omega_c t + \frac{2\pi}{3})$. Expressions for phase currents are omitted for brevity, noting each will be composed of the homogeneous and particular ODE solutions given respective initial conditions. Instantaneous active power in three-phase circuits can be calculated [71] as follows:

$$\begin{aligned} P(t) &= v_a(t)i_a(t) + v_b(t)i_b(t) + v_c(t)i_c(t) \\ &= P_p(t) + P_h(t). \end{aligned} \tag{5.2}$$

Where

$$P_p(t) = \frac{3}{2}VI_p\cos(\alpha), \tag{5.3}$$

and

$$\begin{aligned} P_h(t) = \frac{3}{2}VI_h e^{-\eta(t-t_s)} \\ \cdot \cos(\omega_0(t-t_s) - \beta)\sin(\omega_c t - \phi_s), \end{aligned} \tag{5.4}$$

making $P(t)$ independent of the time of switch closure.

As seen in equation (5.4), the transient power flow $P_h(t)$ is made up of three components: exponential decay multiplied by a sinusoid at grid angular frequency ω_c and another sinusoid at

the circuit natural frequency ω_0, much lower than the grid frequency in practice [41] and by design in the reference circuit.

Consensus on a comprehensive theory of instantaneous reactive power in three-phase systems has not been reached, as illustrated by disagreements between [90], [91], and [92] among others. Disagreements notwithstanding, the equation for instantaneous reactive power

$$Q(t) = \frac{1}{\sqrt{3}}\Big[v_{bc}(t)i_a(t) + v_{ca}(t)i_b(t) + v_{ab}(t)i_c(t)\Big] \tag{5.5}$$

in a balanced three-phase system presented in [71] holds.

It can be shown that in a balanced circuit the product of phase currents and line voltages is equivalent to that of phase currents and phase voltages with a $-\pi/2$ radian phase shift and scaling factor of$\sqrt{3}$, yielding:

$$Q(t) = v_a^{-90}(t)i_a(t) + v_b^{-90}(t)i_b(t) + v_c^{-90}(t)i_c(t), \tag{5.6}$$

consistent with theorems in [90] showing reactive current to be orthogonal to voltage. This orthogonality will be leveraged later.

5.3.2 Power Demodulation

The power flow fluctuation $P_h(t)$ in (5.4) can revealed by sampling at $t = \frac{n}{f_c} + \frac{\phi_s}{2\pi}$, insuring $\sin(\omega_c t - \phi_s) = 1$. Unfortunately, without knowledge of ϕ_s and the timing of switch closure, it is not realistic.

Figure 5.3 shows simulations of reference circuit active power after switch closure with high-speed sampling at $256f_c$, and sampling at grid-frequency f_c with sample timing varied by a quarter cycle. The figure illustrates the unacceptable changes in the signal caused by timing variations, comparing sampling timed to perfectly capture the signal envelope to sampling that almost entirely fails to capture the transient dynamics.

The amplitude term $\frac{3}{2}VI_he^{-\eta(t-t_s)}\cos(\omega_0(t-t_s)-\alpha)$ acts on $\sin(\omega_c t - \phi_s)$ in (5.4). By

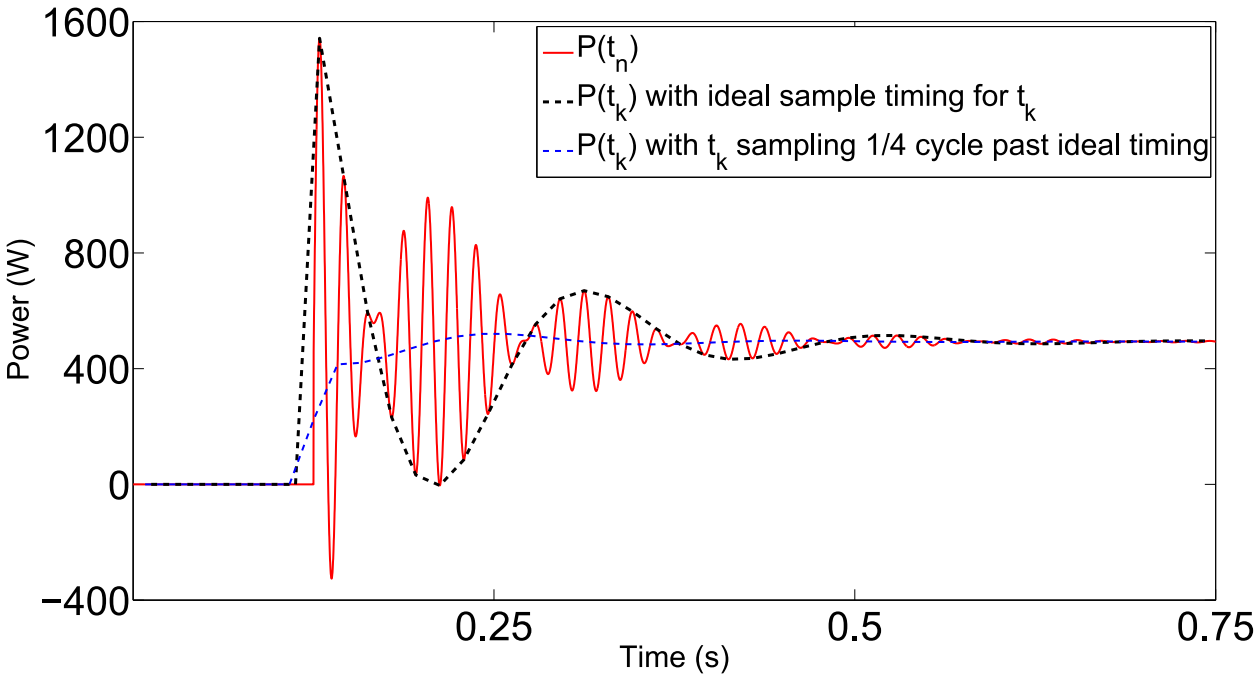

Figure 5.3: Effect of sample timing, illustrating the correct power envelope only when sampled at the correct timing relative to start of power disturbance.

trigonometric identities

$$\begin{aligned}\cos(\theta_1)\sin(\theta_2) &= \frac{1}{2}\Big[\sin(\theta_1+\theta_2)-\sin(\theta_1-\theta_2)\Big]\\ \cos(\theta_1)\cos(\theta_2) &= \frac{1}{2}\Big[\cos(\theta_1+\theta_2)+\cos(\theta_1-\theta_2)\Big]\\ \sin(\theta_1)\sin(\theta_2) &= \frac{1}{2}\Big[\cos(\theta_1-\theta_2)-\cos(\theta_1+\theta_2)\Big]\end{aligned} \tag{5.7}$$

the frequency content is concentrated at $\omega_c+\omega_0$ and $\omega_c-\omega_0$, making simple low-pass filtering ineffective for isolating the fluctuation at reference circuit natural frequency ω_0. Furthermore, the effect of harmonics in the AC current provided by a PWM inverter, as illustrated earlier in Fig. 5.1 must also be taken into account. Without careful design, simple low-pass filtering to remove harmonic distortion may also remove the relevant power oscillation to be demodulated. It also introduces a time delay in the power measurement signal as indicated in Fig. 5.4, comparing measured inverter-supplied three-phase active power $P(t_n)$ upon switch closure and the same signal low-pass filtered, denoted $\hat{P}(t_n)$. Such filtering is straightforward to implement, but requires

careful consideration of trade-offs between delay and filter performance.

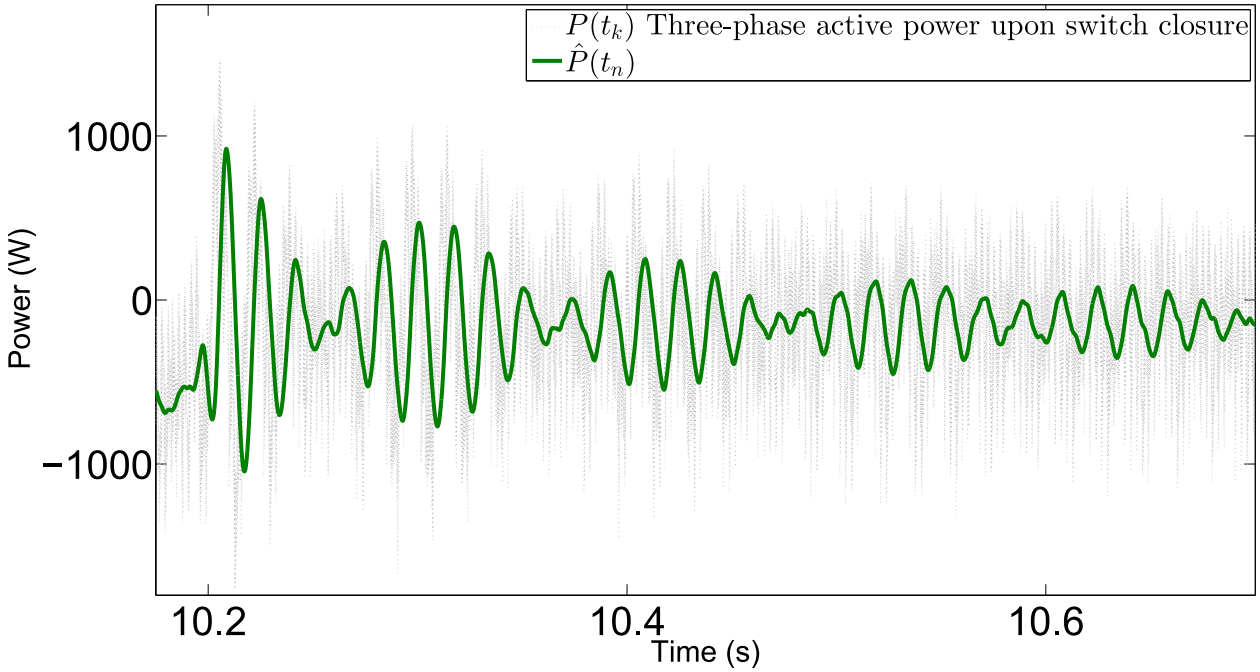

Figure 5.4: Actual real-time measured three-phase active power compared to the filtered three-phase active power.

A promising alternative is Amplitude Modulation (AM), as AM tools used for radio communications are faced with the same challenge in reconstructing signal envelope. In AM terms, the low-frequency component of active power transient response modulates a grid-frequency carrier in a dual sideband, suppressed carrier (DSB-SC) signal [93].

However, radio communications carriers are much higher frequency and transient effects in demodulation exhibited over several carrier cycles are therefore very short lived and imperceivable to the listener [72]. Control efforts for power systems with a carrier frequency of 50 or 60 Hz cannot afford several cycles as power transient effects must be controlled in real-time. This chapter explores the possibility of adapting AM tools to demodulate active and reactive power flow fluctuations.

5.4 Demodulation via Costas Loop

Drawing similarities between AM communications signals and power system fluctuations, we first present Costas Loop [72] used for demodulation of DSB-SC signals.

A DSB-SC signal exhibits π radian phase-shifts at zero crossings of the information signal [94], preventing demodulation with a phase-locked loop (PLL) [95]. Costas loop overcomes this limitation by combining two PLLs, denoted in-phase and quadrature PLLs, as shown in Fig 5.5. In Fig. 5.5 $u(t)$ is a DSB-SC input, $Q_c(t)$ is the quadrature branch and $I_c(t)$ is the in-phase branch as well as output. The -90° block indicates a $-\pi/2$ radian phase shift, LPF is a low-pass filter, VCO is a Voltage Controlled Oscillator and $\otimes$ denotes multiplication.

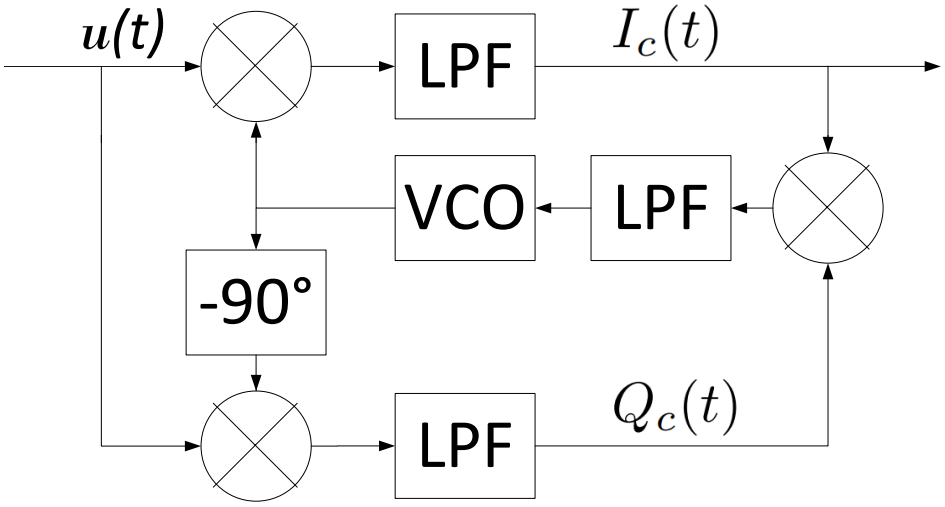

Figure 5.5: Classical Costas Loop for demodulating a dual sideband, suppressed carrier (DSB-SC) signal $u(t)$.

Costas Loop 'locks' when the phase difference between the carrier and the in-phase PLL is either 0 or π radians [73] making phase ambiguity an issue if signal inversion is significant. There are three main reasons why Costas Loop cannot be applied directly to demodulation of power signals:

- Costas loop exhibits transient effects itself, and these transient effects interfere with the desired demodulation of power flow transient effects.

- Costas loop demodulates the amplitude with an ambiguous sign: the phase of the demodulated signal may be misread by π radians, causing a sign mismatch in the demodulated signal.

- The magnitude of the feedback signal is dependent on that of the input; the VCO sensitivity may be optimal for one transient while completely ineffectual for another.

These effects are detrimental if the demodulated signal is to be used for real time control to suppress or dampen power oscillations. The standard solution to phase ambiguity is sending a test signal and checking for inversion [96], not viable for power fluctuations. The following section describes a modification to Costas Loop that overcomes these limitations, hereafter referred to as the 'Group Open-Loop Demodulation' or GOLD method.

5.5 The GOLD Method

5.5.1 Rationale

Voltage acts as a forcing function of active and reactive power transients. The carrier frequency is the voltage frequency, and as such a VCO, as used in Costas Loop of Fig. 5.5 is not needed. The power calculation used in [27] recognized that each voltage signal could be normalized, making local generation of a demodulation signal unnecessary.

We introduce sampling t_n and normalized voltage signals ($\tilde{v}_m(t_n) = v_m(t_n)/V$) for demodulation. Here, subscript m indicates signals formed from voltage data such as $v_a(t_n)$, $v_b(t_n)$, and $v_c(t_n)$ or delayed versions of the same. These signals will be referred to as 'candidates' with the aim of determining which candidate best demodulates $P_h(t_n)$. This allows deviation from the operating concept of Costas Loop (as a closed-loop system in which feedback adjusts phase and frequency to match the carrier) to a battery of open-loop calculations on demodulation signal candidates. Figure 5.6 is a block diagram of the GOLD method algorithm. Voltage normalization occurs at position (1) in the figure, where A is unitizing gain. In Fig. 5.6 BPF is a band-pass

filter, MA is a moving average filter, SIGN is a sign function. * denotes 6x zoom on the signal wave-form time axis.

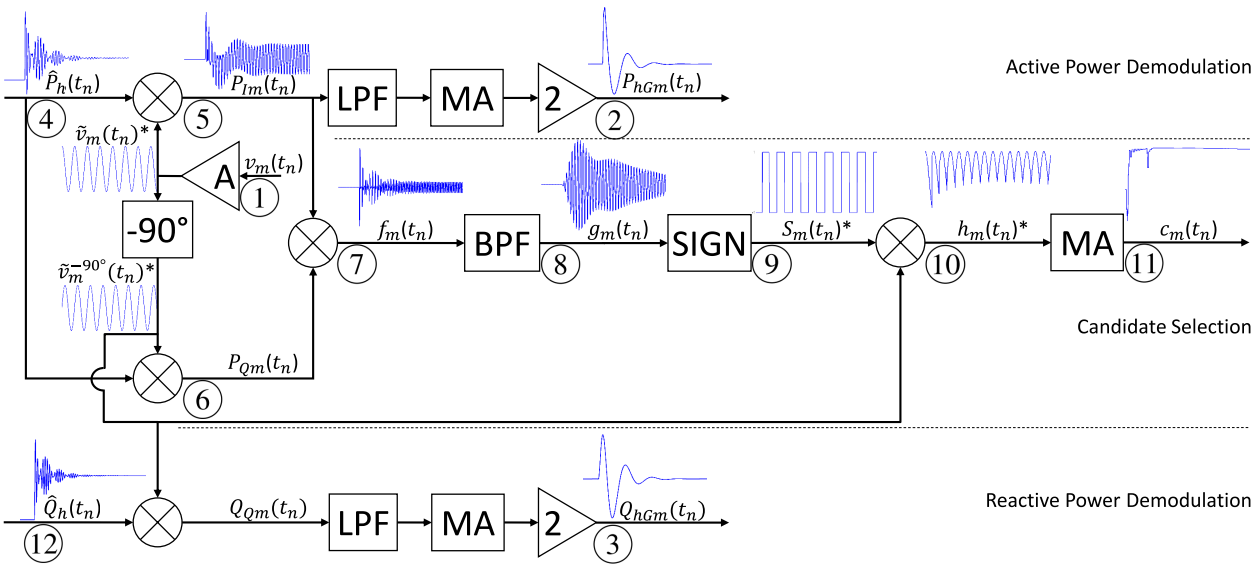

Figure 5.6: The GOLD method algorithm.

The GOLD method algorithm accomplishes three functions: Given generic candidate with in-phase signal $\tilde{v}_m(t_n) = \sin(\omega_c t - \phi_m)$ and quadrature signal $\tilde{v}_m^{-90}(t_n) = -\cos(\omega_c t_n - \phi_m)$, the top (2) and bottom (3) branches of Fig. 5.6 demodulate and filter active and reactive power, respectively. The middle section of the figure quantifies the phase difference between $\tilde{v}_m(t_n)$ and the fluctuation carrier, the $\sin(\omega_c t_n - \phi_s)$ term from (5.4).

5.5.2 Algorithm

Demodulation operations remove DC components, so these are reconstructed by

$$\hat{P}_p(t_n) = F_{MA}(q)F_{LP0}(q)P(t_n), \tag{5.8}$$

where $F_{MA}(q)$ and $F_{LP0}(q)$ represent transfer functions of a moving average filter and low-pass filter, respectively.

$P_h(t_n)$ is the part of $P(t_n)$ requiring demodulation. It is approximated by

$$\begin{aligned}\hat{P}_h(t_n) &= \hat{P}(t_n) - \hat{P}_p(t_{n-1}),\\ &= D(q)P_h(t_n) + B(t_n),\end{aligned} \tag{5.9}$$

where $D(q)$ represents delay due to filtering $P(t_n)$ to get $\hat{P}(t_n)$ and $B(t_n)$ represents the error introduced by imperfections in filtering to get $\hat{P}(t_n)$ and $\hat{P}_p(t_n)$. The use of $\hat{P}_p(t_{n-1})$ facilitates parallel operations on the FPGA. $\hat{P}_h(t_n)$ is the input signal to the algorithm at (4) in Fig. 5.6.

Applying (5.7) to the top/in-phase branch at (5), the demodulated active power in the branch is given by $P_{Im}(t_n) = \hat{P}_h(t_n)\tilde{v}_m(t_n)$. Combining (5.4), (5.9) and the definition of $\tilde{v}_m(t_n)$, $P_{Im}(t_n)$ can be expanded as

$$P_{Im}(t_n) = B(t_n)\cos(\omega_c t_n - \phi_m) \tag{5.10a}$$

$$+ D(q)\big[\frac{3}{2}VI_h e^{-\eta(t_n - t_s)}\cos(\omega_0(t_n - t_s) - \beta) \tag{5.10b}$$

$$\cdot \frac{1}{2}[\cos(\phi_m - \phi_s) - \cos(2\omega_c t_n - \phi_s - \phi_m)]\big].$$

At (6), the quadrature branch $P_{Qm}(t_n) = \hat{P}_h(t_n)\tilde{v}_m^{-90}(t_n)$ could be expanded similarly.

The fluctuation (5.10b) is approximated at (2) by

$$P_{hGm}(t_n) = 2 \cdot F_{MA}(q)F_{LP}(q)P_{Im}(t_n), \tag{5.11}$$

where a moving average filter and low-pass filter remove the ω_c and $2\omega_c$ frequency sinusoids of (5.10a) and (5.10b), respectively. Gain of 2 counteracts coefficient $\frac{1}{2}$ in (5.7).

Clearly (5.10b) has greatest magnitude when $\phi_m = \phi_s$. For best demodulation we must identify the candidate with phase closest to meeting this condition. This is the purpose of the candidate selection section of the GOLD method algorithm, made up of points (7) - (11) of Fig. 5.6.

Relationship $\sin(\theta) = \cos(\theta - \pi/2)$ coupled with (5.7) allows $\tilde{v}_m(t_n)\tilde{v}_m^{-90}(t_n)$=-$\frac{1}{2}\sin(2\omega_c t_n - 2\phi_m)$. Then at (7)

$$
\begin{aligned}
f_m(t_n) &= P_{Im}(t_n) P_{Qm}(t_n) \\
&= -\frac{1}{2} \hat{P}_h^2(t_n) \sin(2\omega_c t_n - 2\phi_m).
\end{aligned}
\tag{5.12}
$$

Expanding $\hat{P}_h^2(t_n)$ by inserting (5.4) into (5.9), successive multiplication operations lead to an inflation of frequencies. Higher frequency terms will be omitted for brevity, but the cross terms from $\hat{P}_h^2(t_n)$ lead to the retention of one important component:

$$
\begin{aligned}
f_m(t_n) = -B(t_n)\frac{3}{2} V I_h D(q) \Big[& e^{-\eta(t_n - t_s)} \\
& \cdot \cos(\omega_0(t_n - t_s) - \beta) \\
& \cdot \sin(\omega_c t_n - \phi_s) \sin(2\omega_c t_n - 2\phi_m) \Big] \\
& + \text{[omitted higher-frequency terms]}.
\end{aligned}
\tag{5.13}
$$

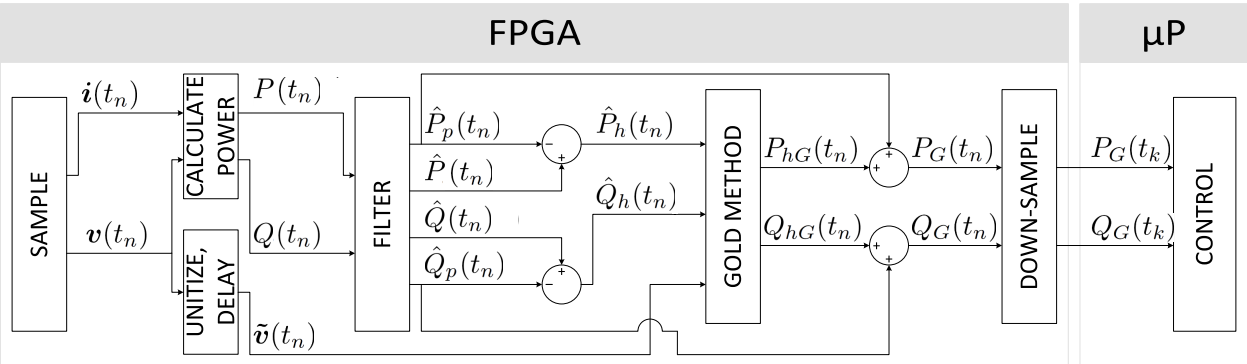

Figure 5.7: Hardware implementation and signal conditioning for the GOLD method algorithm.

Using (5.7) again, the third line of (5.13) is equal to $-\frac{1}{2}[\cos(\omega_c t_n - 2\phi_m + \phi_s) + \cos(3\omega_c t_n - 2\phi_m - \phi_s)]$. The $\cos(\omega_c t_n - 2\phi_m + \phi_s)$ term is the key to calculating which candidate is closest in phase with the fluctuation carrier, the $\sin(\omega_c t - \phi_s)$ term from (5.4). This term is isolated through band-pass filtering of $f_m(t_n)$ at (8):

$$
\begin{aligned}
g_m(t_n) &= F_{BP}(q) f_m(t_n) \\
&= -G(t_n) \cos(\omega_c t_n - 2\phi_m + \phi_s)
\end{aligned}
\tag{5.14}
$$

where $G(t_n)$ is introduced to denote the unwanted dynamic effects of the band-pass filter.

The effect of $G(t_n)$ is minimized by subjecting $g_m(t_n)$ to a sign function, forming square wave $S_m(t_n) = -\text{sgn}(\cos(\omega_c t_n - 2\phi_m + \phi_s))$ at (9).

$S_m(t_m)$ is multiplied by $\tilde{v}_m^{-90}(t_n)$ at (10). The resulting signal can be rearranged as

$$\begin{aligned} h_m(t_n) =& |\tilde{v}_m^{-90}(t_n)| \\ & \cdot\text{sgn}\Big[-\tilde{v}_m^{-90}(t_n)\cos(\omega_c t_n - 2\phi_m + \phi_s)\Big]. \end{aligned} \tag{5.15}$$

This shows that $h_m(t_n)$ is a bounded, periodic function. Once more using (5.7) on the argument of the sign function in (5.15) yields $\frac{1}{2}(\cos(\phi_m - \phi_s) + \cos(\omega_c t_n - 3\phi_m + \phi_s))$, which is positive for the greatest part of its cycle when $\phi_m - \phi_s$ is minimized.

At (11) a moving average of $h_m(t_n)$ provides $c_m(t_n) = F_{MA}(q)h_m(t_n)$, a metric inversely proportional to the difference $\phi_m - \phi_s$.

Defining $\tilde{v}_G$ as the candidate with greatest $|c_m(t_n)|$ value, the corresponding $P_{hGm}(t_n)$ is selected as the algorithm output. If $c_m(t_n)$ is negative, the output is inverted, making use of symmetry of demodulated signals.

The algorithm output is added to $\hat{P}_p(t_n)$ forming $P_G(t_n)$, the best approximation of $P(t_n)$ which will be the controller input.

The calculation of reactive power in the bottom branch starting at (12) is corollary to active power in the top branch, using input $\hat{Q}_h(t_n)$ and demodulating signal $\tilde{v}_m^{-90}(t_n)$. However, with $\tilde{v}_G(t_n)$ identified and $\tilde{v}_G^{-90}(t_n)$ already available from the quadrature branch, no comparison of candidates is necessary for reactive power because of the quadrature relation established in (5.6).

Figure 5.8 shows simulation data of $P(t_n)$ overlaid by the $P_G(t_n)$ (top), as well as grid-frequency sampling of $P(t_k)$ ideally timed to capture the signal envelope compared with down-sampled $P_G(t_k)$ (bottom).

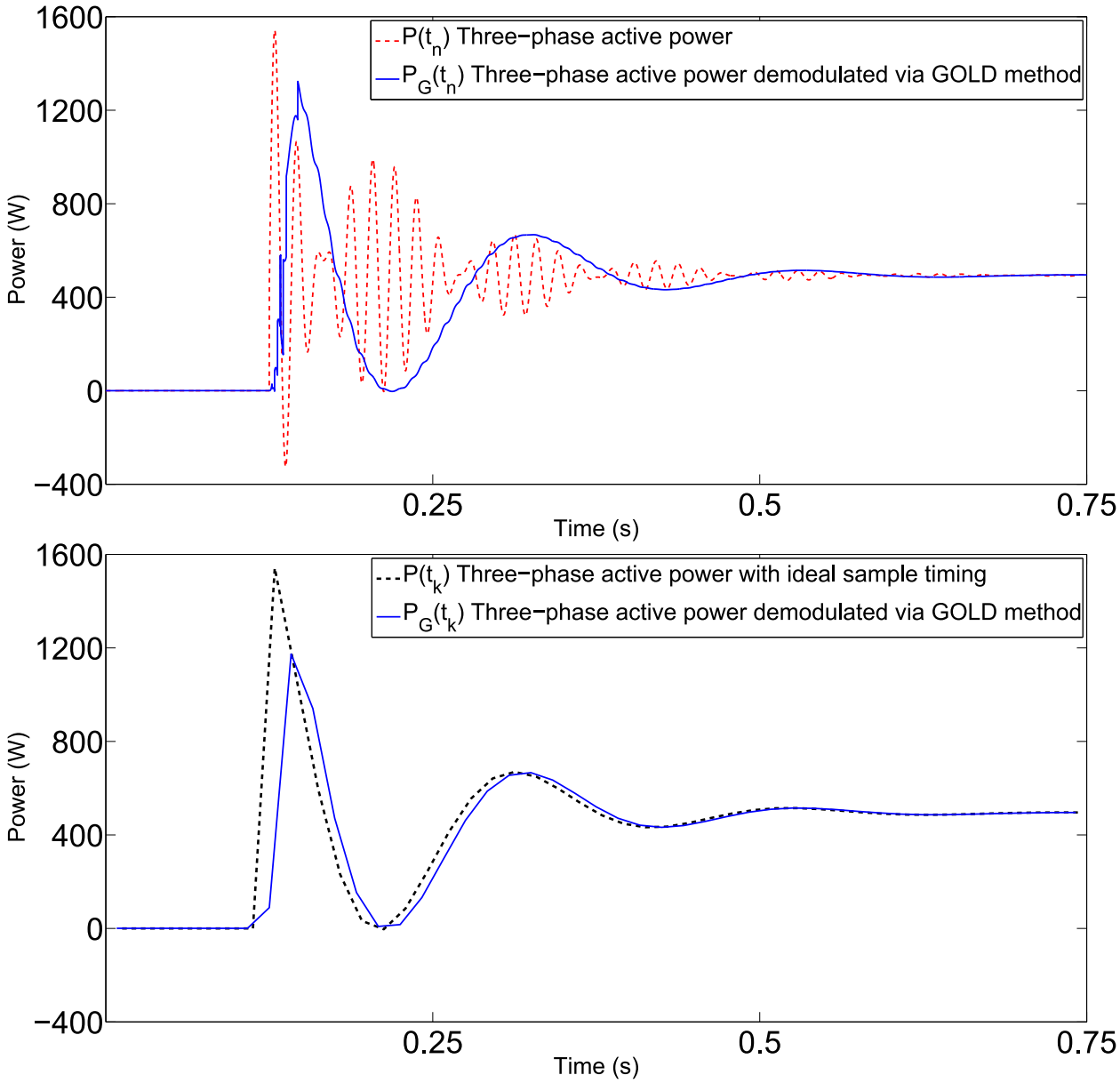

Figure 5.8: Simulated performance of the GOLD method, comparing actual computed power disturbance with demodulated power disturbance.

5.6 Demonstration of GOLD Method

5.6.1 Hardware Implementation

National Instruments graciously provided a microcontroller with integrated FPGA. The FPGA facilitates high speed signal processing and full implementation of the GOLD method algorithm as depicted in Fig. 5.7. A three-phase implementation of the reference circuit depicted in

Fig. 5.2 was constructed at the SyGMA lab.

A 3-level PWM Grid-Tied Inverter with 6-switch topology was donated by industry partner One-Cycle Control. The inverter has low Total Harmonic Distortion of current (THD_i) at rated power, but when operating at low power output THD_i is considerable, as seen in Fig. 5.1. To assure that the GOLD algorithm functions throughout the inverter operating range, testing was conducted with the inverter operating at low power output levels where signal to noise ratio and THD_i are worst.

At 5% rated power THD_i was calculated to be 103.1% using

$$THD = \frac{\sqrt{\sum_{H=2}^{\infty} \lambda_H^2}}{\lambda_1}, \tag{5.16}$$

where λ_1 is the magnitude of the fundamental f_c, and λ_H indicates magnitudes of harmonics $H * f_c$, $H \in 2, 3, 4....$ Total Harmonic Distortion of voltage was calculated to be 1.8% with inverter power output at 5%.

A distorted oscillation is produced when the reference circuit is switched in while the inverter supplies power. That oscillation is suitable for testing robustness of the GOLD method implemented on the FPGA.

5.6.2 Robustness

Unbalanced loads present a robustness concern. The imbalances in the reference circuit implementation were assumed to be small enough to be neglected up to this point, but DSB-SC oscillations occur when unbalanced loads are switched in as well. Since demodulation is done on a full three-phase power basis, unbalanced circuits can also be analyzed. As seen in Fig. 5.9 the demodulation succeeds in simulation. For the figure, the reference circuit was made unbalanced by opening the reactive branch on two phases. Note the double-frequency component characteristic of unbalanced loads has not prevented demodulation.

The more severe aspect of robustness is harmonic distortion. Harmonic distortion most

adversely affects the GOLD method algorithm at the band-pass filter.

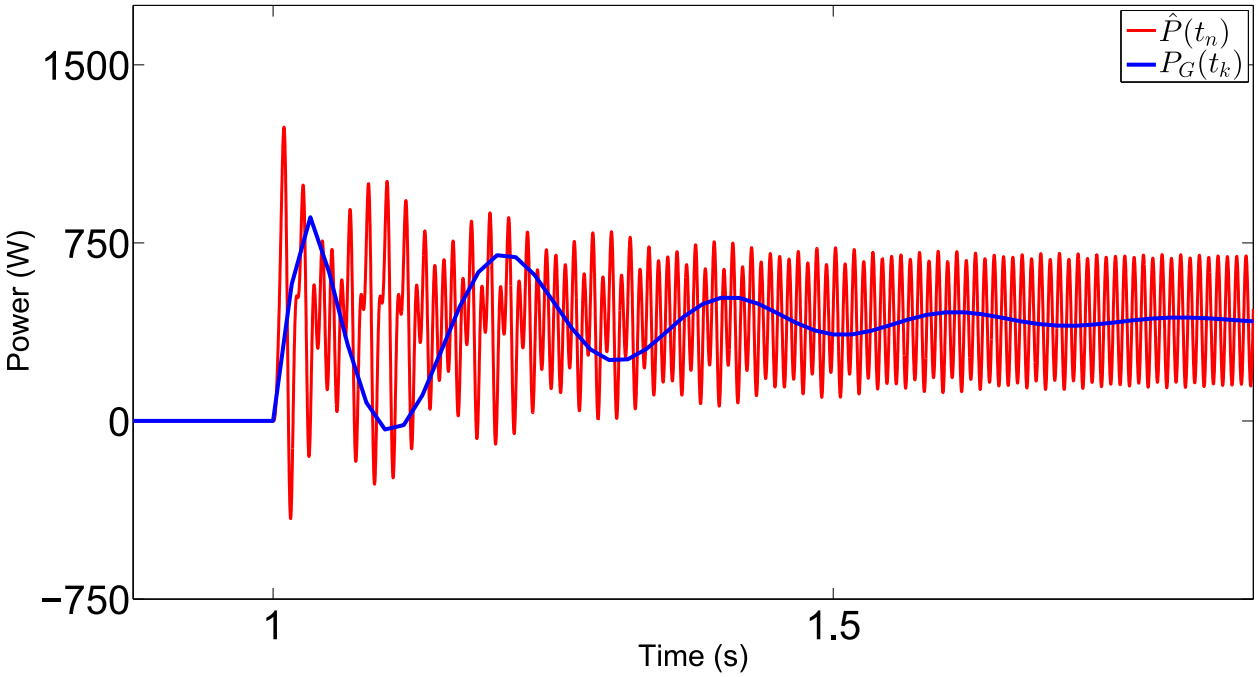

Figure 5.9: GOLD method performance for an unbalanced load: Correct power demodulation $P_G(t_k)$ despite harmonics in instantaneous power $P(t_k)$.

The choice of $\hat{P}_h(t_n)$ as algorithm input rather than $\hat{P}(t_n)$ limits filter input during steady state: if $P_h(t_n) = 0$ then by combining (5.9) and (5.12) the filter input becomes $f_m(t_n) = B^2(t_n)\tilde{v}_m(t_n)\tilde{v}_m^{-90}(t_n)$. At steady state $B(t_n)$ is made up of only what cannot be filtered from the distorted power signal. However, immediately following a transient $B(t_n)$ is dominated by $P_p(t_n) - \hat{P}_p(t_{n-1})$, making band-pass filter output $g_m(t_n)$ most appreciable after a transient.

Despite algorithm input choice, signal processing capability is limited by FPGA resources, making admittance of some harmonic distortion inevitable.

To analyze the effect of harmonic distortion, we introduce notation

$$P^{(2)}(f_c, 3f_c) = \sum_{p=a}^{c} i_p(2f_c)v_p(f_c), \tag{5.17}$$

based on (5.2), indicating the $H = 2$ harmonic of phase current i_a, i_b and i_c interactions with the $H = 1$ (non-Harmonic) phase voltages v_a, v_b and v_c. By application of (5.7) it is clear that this

product contains harmonics with frequencies f_c and $3f_c$ as indicated by $P^{(2)}(f_c, 3f_c)$.

As an update to (5.9), imperfect filtering leads to these harmonics appearing in

$$\hat{P}_h^{(2)}(f_c, 3f_c) = \hat{P}^{(2)}(f_c, 3f_c) - \hat{P}_p^{(2)}(f_c, 3f_c), \tag{5.18}$$

the GOLD algorithm input at (4) in Fig 5.6. Further application of (5.7) for the product at (5) in the same figure begets

$$\hat{P}_h^{(2)}(f_c, 3f_c)\tilde{v}_m(f_c) = P_{Im}^{(2)}(2f_c, 4f_c) + ... \tag{5.19}$$

Here and forthwith, the ellipsis encapsulates terms not relevant to the discussion such as higher frequency or DC terms.

The same process can be repeated for the $H = 3$ harmonic in the quadrature branch at (6):

$$P^{(3)}(2f_c, 4f_c) = \sum_{p=a}^{c} i_p(3f_c)v_p(f_c) \tag{5.20a}$$

$$\hat{P}_h^{(3)}(2f_c, 4f_c)\tilde{v}_m^{-90}(f_c) = P_{Qm}^{(3)}(f_c, 3f_c) + ... \tag{5.20b}$$

Then at (7) the interrelation of the harmonics from (5.19) and (5.20b) manifests as a grid-frequency component in the band-pass filter input:

$$P_{Im}^{(2)}(2f_c, 4f_c)P_{Qm}^{(3)}(f_c, 3f_c) = f_m(f_c) + ... \tag{5.21}$$

With this observation, the design problem becomes a trade-off between signal delay from filtering vs. response of band-pass filter output into the desired signal upon switch closure, both constrained by FPGA resources.

The grid-frequency f_c component of $P^{(2)}(f_c, 3f_c)$ from (5.17) is particularly vexing, because it cannot be removed through filtering since it is the carrier frequency that we aim to identify in our demodulation. However, $v_a(t_n), v_b(t_n)$ and $v_c(t_n)$ present as comparatively undistorted si-

nusoids at f_c, and can again be leveraged given the observation that harmonics in $i_a(t_n), i_b(t_n)$ and $i_c(t_n)$ arise from deterministic processes.

Subtraction of appropriate weightings of $v_a(t_n)$, $v_b(t_n)$, and $v_c(t_n)$ from $P^{(2)}(f_c, 3f_c)$ allows suppression of the f_c component without filtering. The sum of two sinusoids of equal frequency is another sinusoid at the same frequency [70], and the $2\pi/3$ radian phase difference between voltages facilitates construction of a sinusoid fit for canceling the undesired part of $P^{(2)}(f_c, 3f_c)$. This is easily implemented and requires few additional FPGA resources by merging the process with the power calculation:

$$\begin{aligned}&\sum_{p=a}^{c} v_p(t_n)(i_p(t_n) + b_p)\\ &\quad = P(t_n) + \sum_{p=a}^{c} b_p v_p(t_n).\end{aligned} \tag{5.22}$$

Determining weightings b_p is achieved by iteration upon steady-state data, seeking values resulting in the minimum-valued DFT bin corresponding to f_c.

Removal of the f_c component of $P(t_n)$ allows a higher cut-off frequency for a low-pass filter applied to $P(t_n)$ to make $\hat{P}(t_n)$. This filtering further improves robustness against THD_i. Filter design is a compromise between minimizing distortion on $\hat{P}(t_n)$ while limiting filter impact on oscillations due to load and circuit dynamics. Filtering of $P(t_n)$ rather than raw current and voltage signals uses fewer FPGA resources, results in less delay of $\hat{P}(t_n)$, and facilitates near immediate band-pass filter response to transient by minimizing filter input $f_m(t_n)$ during steady state operation. Critically, a well-designed filter enables the GOLD method to accurately decode power transients even with extreme distortion on the algorithm input, as with THD_i as high as 103.1%.

The GOLD algorithm operates on power signals, making THD an impractical metric for discussion of the effect of distortion on algorithm signals: At steady-state the power draw of a balanced load has no fundamental frequency, making (5.16) undefined. However, improvement in

signal quality can be quantified with root mean square error of instantaneous active power $P(t_k)$

$$RMSE_{raw} = \sqrt{\frac{1}{K}\sum_{k=1}^{K}[P(t_k) - \overline{P}(t_k)]^2} \tag{5.23}$$

compared to the similarly-defined $RMSE_G$ of demodulated power $P_G(t_k)$. In each case the mean is used as estimator at steady state. Recall, per (5.2), $P(t_k)$ is calculated from raw voltage and current signals. As mentioned, at 5% inverter power output, the inverter-supplied current is subject to 103.1% THD_i, causing the correspondingly high $RMSE_{raw}$ of 356W; at the same power, $RMSE_G$ = 2.94W, or a reduction in RMSE of 99.2%.

5.6.3 Demonstration on Reference Circuit

Referring back to Fig. 5.3, when switching in the RLC load, the power oscillation should have frequency of approximately 5 Hz. Demonstration of power demodulation in presence of harmonic distortion is now shown in Fig. 5.10, where indeed the anticipated oscillation of 5 Hz can be seen. The figure shows measurements of distorted active power $P(t_n)$ (top) and reactive power $Q(t_n)$ (bottom) after switch closure, along with each low-pass filtered ($\hat{P}(t_n)$ and $\hat{Q}(t_n)$, respectively) and GOLD method demodulation of the respective filtered signals $P_G(t_k)$ and $Q_G(t_k)$.

The GOLD method demodulates the 5 Hz oscillation with fidelity regardless of harmonic distortion on the current supplied by the inverter. Figure 5.11 shows measurements of distorted active power $P(t_n)$ after switch closure with the reactive branch open on two phases, along with demodulated power $P_G(t_k)$ and again showing filtered power $\hat{P}(t_n)$ for reference, demonstrating robustness against unbalanced loading despite harmonic distortion.

The delay predicted in the simulation shown in Fig. 5.8 is made marginally worse by additional delay from filtering necessary to limit harmonic distortion on the algorithm input. However, the harmonic distortion shown on Fig. 5.10 obscures the transient dynamics severely, making the trade-off of delay for a clean signal acceptable.

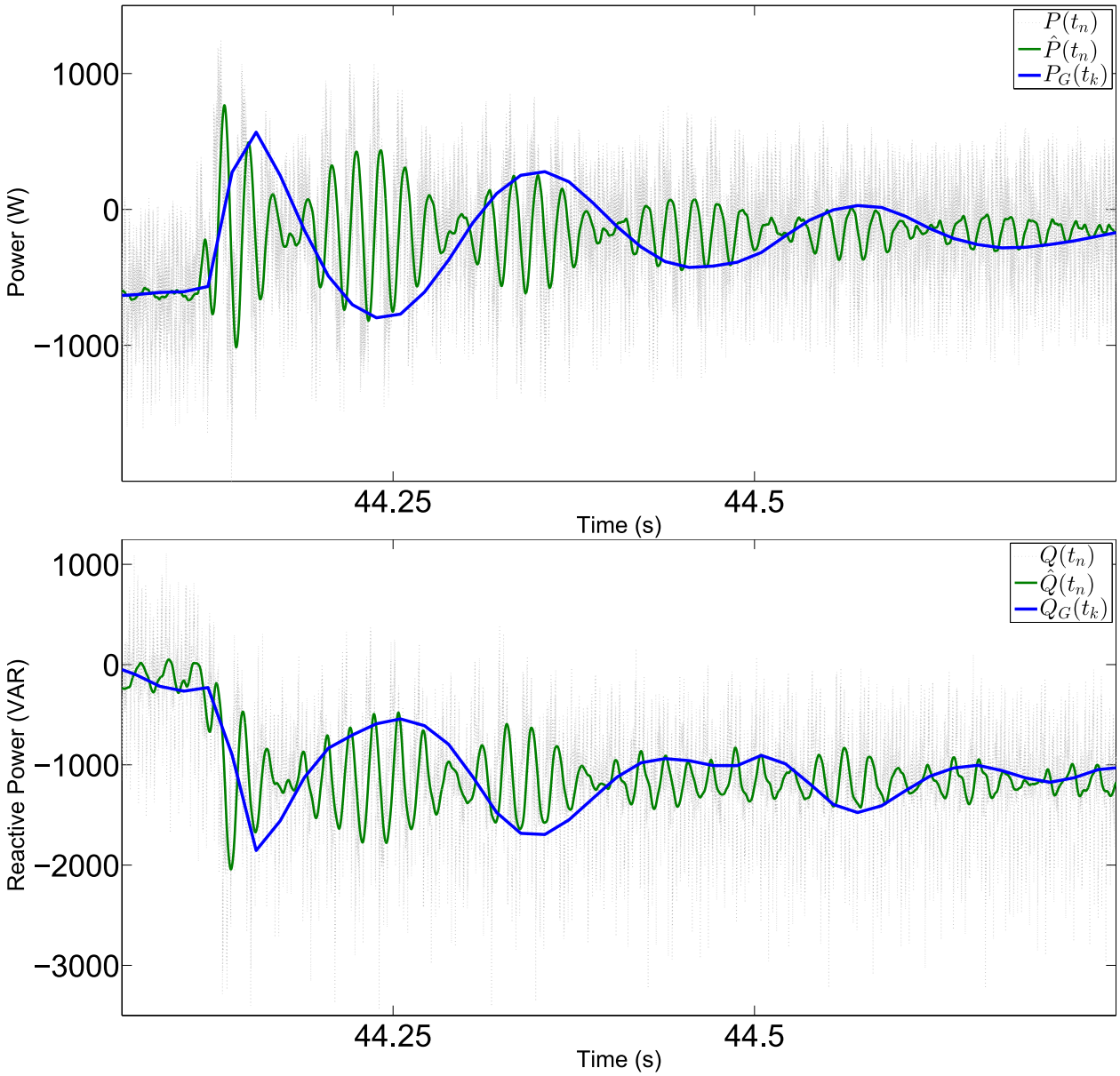

Figure 5.10: GOLD method actual performance, illustrating both real (top figure) and reactive (bottom figure) power disturbance demodulation.

5.7 Conclusions

The results presented in this chapter show that the GOLD method provides rapid decoding of active and reactive power transients on balanced and unbalanced loads. Simple filtering and signal conditioning allow the algorithm to function despite considerable harmonic distortion on inverter current. Experiments using active and reactive power decoded by the GOLD method as

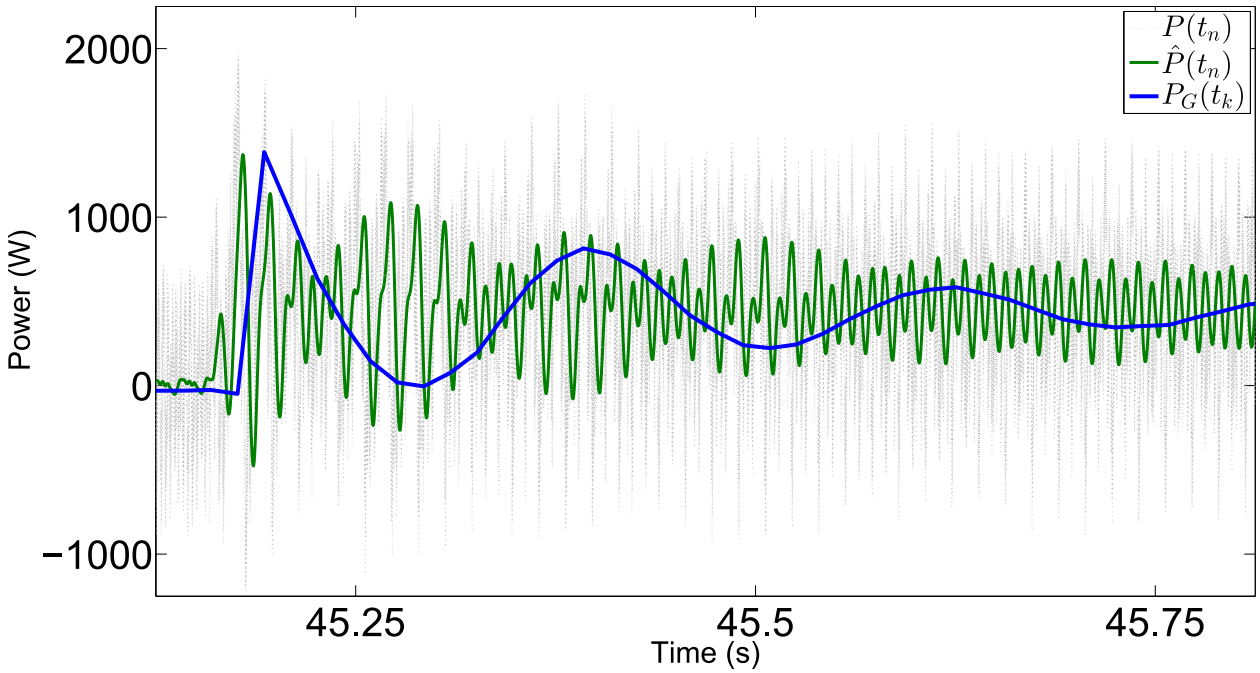

Figure 5.11: GOLD method actual performance for an unbalanced load, illustrating real power disturbance demodulation.

controller inputs are presented in Chapter 6.

ACKNOWLEDGMENTS

This chapter, in full, is a reprint of the material as it appears in ”Benjamin T. Gwynn, Raymond A de Callafon, Demodulation of Three-Phase AC Power Transients in the Presence of Harmonic Distortion” to appear in IEEE Transactions on Power Electronics. The dissertation author is the primary investigator and author of this article.

Chapter 6

Robust Real-Time Inverter-Based Reactive PowerCompensation

6.1 Introduction

Large reactive loads can cause voltage irregularities when connecting or disconnecting from an electric grid. Severe cases can cause degraded load performance, loads dropped on protective action, insulation damage, or, in extreme cases, grid collapse[97].

Induction motors are a ubiquitous example of large inductive loads. An effective approach to offset the voltage variations that accompany switching of an induction motor is simultaneous switching of compensating capacitors or use of a static VAR compensator (SVC) [98]. An SVC is one of many devices in the flexible AC transmission system (FACTS) family of compensators. FACTS devices allow control of shunt and series impedance, current, voltage, phase angle and can dampen low frequency oscillations [99]. Generally speaking, when compensating reactive loads, FACTS devices use various methods to adjust switching of capacitor banks or variable inductors.

Capacitive compensation loads are inherently limited to discrete reactive power increments as banks are made up of individual capacitors. Discrete reactive power levels may also occur in inductive compensating loads, as multiple-tap designs are widely commercially available, with

advantage of no-moving-parts over sliding arms or ferrite-core variable inductors, and have no requirement for external current source as seen in saturable core reactors [100]. Many modern inverters are capable of providing reactive power to the grid, with advantage that reactive power supplied can be varied continuously[101].

Many distributed energy resources (DER) supply grid power through inverters. The interconnect standard has transitioned from prohibition of voltage regulation by DER in 2003 [102] to mandate DER have this capability in the current release, though the capability remains off by default and only for use at the discretion of local operators [103].

Use of inverters for reactive power compensation has been subject of considerable research. The prohibition on use of DER for voltage control was one of the motivations for control aimed at maintaining unity power factor for inverter output as described in [104]. The revision to the standard makes droop methods of volt/VAR control discussed in [105] and [106] increasingly relevant. A centralized control scheme is proposed in [107], while distributed control is discussed in [108] and [109]. Many attempts at reactive power compensation/voltage control via DC-AC inverter consider time frames on order of minutes or hours [109],[110], though [111] and [112] demonstrate inverter control for demand step changes on shorter time frames.

Within the scope of inverter-based reactive power compensation, this chapter focuses on control of reactive power flow at the point of interconnect of a single DER. The aim is to provide sub-second timescale disturbance rejection when a highly inductive load is switched in. The contribution of this chapter is presentation of a robust control design framework allowing reactive power compensation by a four-quadrant capable inverter. An added benefit of the approach is that it leverages system identification for model development. This approach only requires subsystems' input/output data, allowing a designer to bypass the in-depth analysis often considered critical. A controller designed using the framework is demonstrated on a live, grid-connected test circuit. Figure 6.1 shows the architecture of the testbed used for demonstrating control.

The design framework outlined in this chapter is suitable for application toward active and reactive power control, but the discussion will focus on reactive power, as active power control is

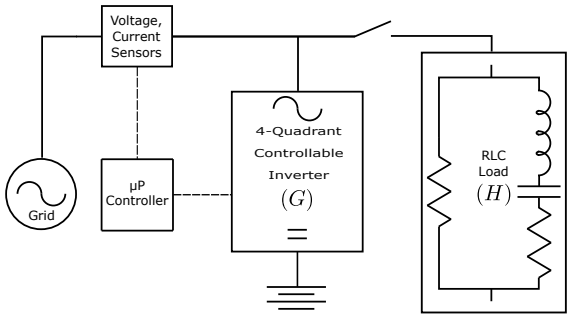

Figure 6.1: Diagram of the interconnection between inverter, grid, load and controller used for testing at SyGMA Lab at UCSD. G and H denote dynamics of the inverter and load, respectively.

subject to additional constraints that reactive power does not suffer: Use of an inverter to absorb active power is complicated by associated energy sources - batteries/storage have charging limits, while other sources (e.g. photovoltaic cells) cannot absorb energy at all. Reactive power does not suffers these constraints. Parts of the approach have been discussed elsewhere: A method for decoding power transients was presented in [113]. While [27] presents a less-consistent demodulation algorithm, it also outlines usage of the system identification methods used for development of the models of inverter and load dynamics. The controller design process is a variation on that presented in [67], refocusing on reactive power over active power, using a balanced load rather than unbalanced, and making use of H_∞ control to achieve robustness.

6.2 Model Development

6.2.1 Reference Circuit

The balanced, three-phase RLC circuit depicted in Fig 6.2 is used as a test case.

Use of a reference circuit for testing allows comprehensive understanding of load dynamics, enabling validation of system identification results. This approach for controller design is intended for application in contexts where the system dynamics may not be perfectly known; system identification may often be preferable to the extensive data collection otherwise necessary for development of a model.

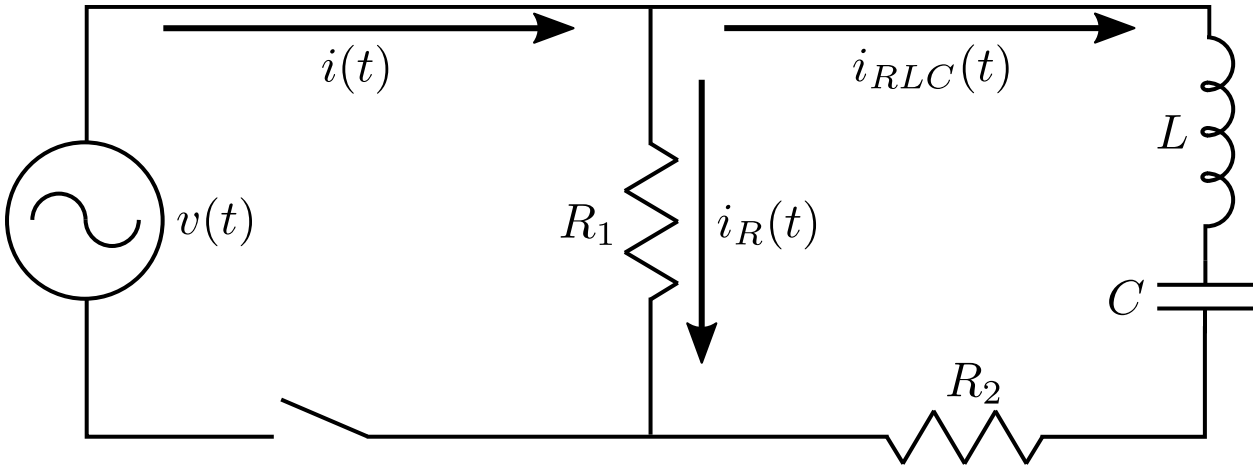

Figure 6.2: Reference circuit for creating a power transient. The voltage source is the local utility, v = 120V RMS AC at 60Hz. R_1 = 100 Ω, R_2 2 Ω, L = 0.1 H, C = 0.01 F.

Reference circuit parameters were selected to avoid protective action, preventing disturbance of other grid customers during testing. The resistive branch allows for a parallel study on active power, and the combination of inductor and capacitor is used to make a more dynamic control problem than possible with a purely inductive or capacitive load.

The reference circuit voltage source is the local utility servicing the Synchrophasor Grid Monitoring and Automation (SyGMA) Lab at the University of California, San Diego (UCSD). The utility grid is stiff, so while the well-known relationship between voltage and reactive power motivates the research, the remainder of the chapter focuses only on control of reactive power.

For time after switch closure $t \geq t_s$ with voltage $v_m(t) = V\cos(\omega_c t - \phi_m)$ for phase $m = a, b, c$, current response is governed by an ODE with general solution

$$i_m(t) = I_{p,m}\cos(\omega_c t - \alpha - \phi_m) \tag{6.1a}$$

$$+I_{h,m}(t_s)e^{-\eta(t-t_s)}\cos(\omega_0(t-t_s) - \beta_m(t_s)), \tag{6.1b}$$

where (6.1a) is the particular solution and (6.1b) is the homogeneous solution.

While there is debate over a comprehensive definition of instantaneous reactive power

[90],[92], the equation for balanced loads found in [71] holds:

$$Q(t) = \frac{1}{\sqrt{3}}\Big[v_{bc}(t)i_a(t) + v_{ca}(t)i_b(t) + v_{ab}(t)i_c(t)\Big]. \tag{6.2}$$

The line voltage $v_{ab}(t)$ in (6.2) is defined as $v_{ab}(t) = v_a(t) - v_b(t)$, and similarly for $v_{bc}(t)$ and $v_{ca}(t)$. Inserting these definitions and currents from (6.1), then total reactive power is given by

$$\begin{aligned} Q(t) &= \frac{3}{2}VI_p\cos(\alpha) \\ +\frac{3}{2}VI_h e^{-\eta(t-t_s)} &\cdot \cos(\omega_0(t-t_s)-\beta)\cos(\omega_c t - \phi_s). \end{aligned} \tag{6.3}$$

Here we note that the interrelation between phases removes the transient dependence on time of switch closure seen in (6.1b), as well as cancelling double grid-frequency components of power in each individual phase.

The Gwynn Open Loop Demodulation (GOLD) method presented in [113] uses a modified Costa's loop to remove the grid-frequency component of a power transient. The demodulation works in discrete time, so discrete time variable t_k is introduced. The cost of demodulation is additional dynamics due to discrete filtering, denoted by transfer function $D(q)$. The error is denoted by function $e(t_k)$ in equation

$$\begin{aligned} Q_G(t_k) &= D(q)\Big[\frac{3}{2}VI_p\cos(\alpha) \\ +\frac{3}{2}VI_h e^{-\eta(t_k-t_s)} &\cos(\omega_0(t_k-t_s)-\beta) + e(t_k)\Big], \end{aligned} \tag{6.4}$$

describing demodulated reactive power Q_G upon switch closure.

Since three-phase power transients are independent of time of switch closure, data was collected over J closures and re-openings of the switch. Averaging with respect to time-step after switch closure minimizes $e(t_k)$ from (6.4):

$$\overline{Q}_G(t_k) = \frac{1}{J}\sum_{j=1}^{J} Q_G(t_k^{(j)}) \tag{6.5}$$

where superscript (j) indicates the jth switch closure.

It should be noted that some power transients on a live electric grid may not be readily reproducible. E.g. a branch trip would be accidental and customers expect continuity of service precluding repetition. In such cases, a single data set would have to suffice; since reproduction is possible with the reference circuit $\overline{Q}_G(t_k)$ is the system response used for identification of the state-space dynamic load switching model:

$$\hat{H}: \begin{cases} x(t_{k+1}) = \hat{A}_H x(t_k) + \hat{B}_H u(t_k) \\ y(t_k) = \hat{C}_H x(t_k) + \hat{D}_H u(t_k) + v(t_k). \end{cases} \tag{6.6}$$

collectively denoted by $\hat{H}$ in the remainder of the chapter.

6.2.2 Realization

The theory supporting the Step-Based Realization Algorithm (SBRA) is presented in [64]. In terms of reactive power, the RLC Load depicted in Fig. 6.1 can be expressed as a linear, time-invariant single-input, single-output system. Switch closure is a step change in power demand, making SBRA well suited for model development. The algorithm is summarized as follows:

- For $t_s = 0$, $M_H = \{\overline{Q}_G^H(0), \overline{Q}_G^H(1), ..., \overline{Q}_G^H(N)\}$ are system response measurements. Here the H superscript indicates the data pertains to block H in Fig 6.1. The data points of M_H are used to populate Hankel matrices

$$Y = \begin{bmatrix} \overline{Q}_G^H(1) & \overline{Q}_G^H(2) & \cdots & \overline{Q}_G^H(l) \\ \overline{Q}_G^H(2) & \overline{Q}_G^H(3) & \cdots & \overline{Q}_G^H(l+1) \\ \vdots & \vdots & \ddots & \vdots \\ \overline{Q}_G^H(r) & \overline{Q}_G^H(r+1) & \cdots & \overline{Q}_G^H(N-1) \end{bmatrix}$$

and

$$\overline{Y} = \begin{bmatrix} \overline{Q}_G^H(2) & \overline{Q}_G^H(3) & \cdots & \overline{Q}_G^H(l+1) \\ \overline{Q}_G^H(3) & \overline{Q}_G^H(4) & \cdots & \overline{Q}_G^H(l+2) \\ \vdots & \vdots & \ddots & \vdots \\ \overline{Q}_G^H(r+1) & \overline{Q}_G^H(r+2) & \cdots & \overline{Q}_G^H(N) \end{bmatrix},$$

as well as matrices

$$M = \begin{bmatrix} \overline{Q}_G^H(0) & \overline{Q}_G^H(0) & \cdots \\ \overline{Q}_G^H(1) & \overline{Q}_G^H(1) & \cdots \\ \vdots & \vdots & \ddots \\ \overline{Q}_G^H(r-1) & \overline{Q}_G^H(r-1) & \cdots \end{bmatrix}$$

and

$$\overline{M} = \begin{bmatrix} \overline{Q}_G^H(1) & \overline{Q}_G^H(1) & \cdots \\ \overline{Q}_G^H(2) & \overline{Q}_G^H(2) & \cdots \\ \vdots & \vdots & \ddots \\ \overline{Q}_G^H(r) & \overline{Q}_G^H(r) & \cdots \end{bmatrix}.$$

- These matrices allow differences:

$$R = Y - M \text{ and } \overline{R} = \overline{Y} - \overline{M}.$$

- The singular value decomposition of R

$$R = [U_n U_s] \begin{bmatrix} \Sigma_n & 0 \\ 0 & \Sigma_s \end{bmatrix} [V_n V_s]$$

allows determination of system order n by inspection of singular values, recognizing near-zero entries have minimal effect.

- Estimates of state-space matrices are given by

$$\begin{aligned}\hat{A}_H =& \Sigma_n^{-\frac{1}{2}} U_n^T \overline{R} V_n \Sigma_n^{-\frac{1}{2}} \\ \hat{B}_H =& [\Sigma_n^{\frac{1}{2}} V_n^T]_{(1,:)} \\ \hat{C}_H =& [U_n \Sigma_n^{\frac{1}{2}}]_{(:,1)} \\ \hat{D}_H =& \overline{Q}_G^H(0)\end{aligned}$$

- Matrices $\hat{B}$ and $\hat{D}$ can be improved by least squares minimization between values $\overline{Q}_G^H(t_k)$ and estimates $\hat{Q}_G^H(t_k)$

Figure 6.3 allows comparison of the step response of the realized model to the averaged step-responses $\overline{Q}_G^H(t_k)$. The figure clearly illustrates that a realized model can recreate system dynamics with high fidelity by using only system output data. This bypasses the need for precise understanding of all system parameters, often erroneously considered crucial for model development.

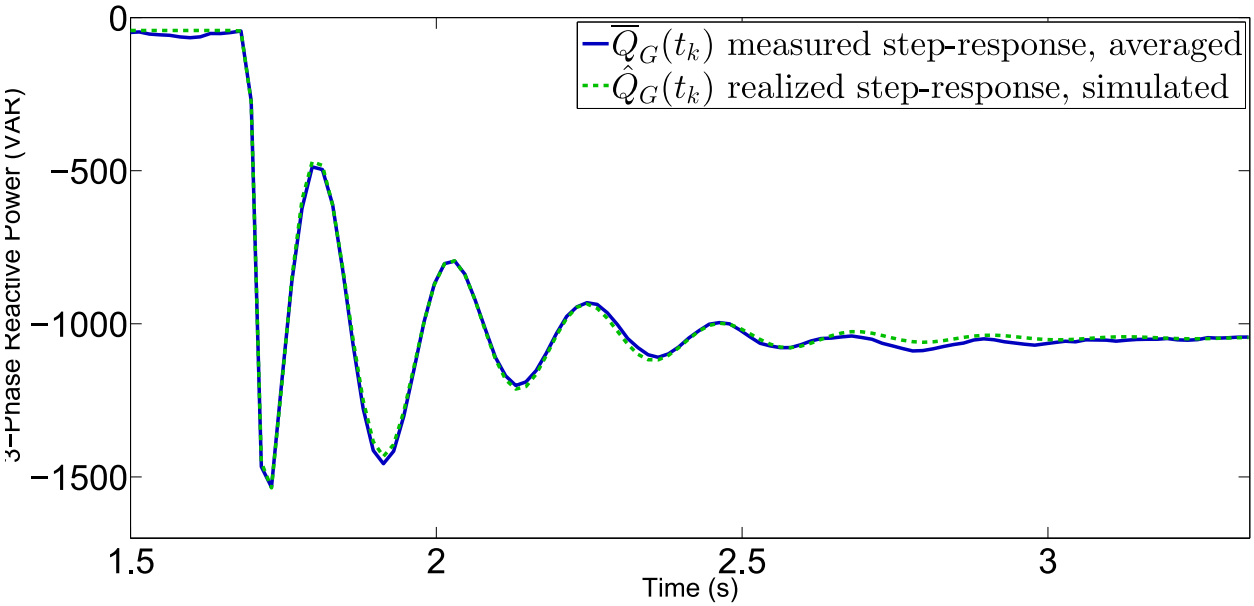

Figure 6.3: Comparison of the averaged actual measurements taken after switch closure $\overline{Q}_G(t_k)$ and the step response of the forth-order dynamic model realized via SBRA $\hat{Q}_G(t_k)$.

Similarly to the load dynamics, a model of the inverter dynamics can also be obtained via

system identification. This allows treatment of the inverter as a black box, which may be necessary for commercial devices with proprietary designs.

As before, error is minimized by averaging data taken during changes in inverter output to form measurement data set $M_G = \{\overline{Q}_G^G(0), \overline{Q}_G^G(1), ..., \overline{Q}_G^G(N)\}$. The inverter at SyGMA lab has very short rail-to-rail time and dynamics might be approximated as simply a step with delay, but for better control results the response can be recreated with SBRA or by using the Output Error (OE) method.

The OE method assumes output is governed by a filter placed on system input, with some degree of measurement error:

$$\hat{Q}_G^G(t_k) = \frac{\hat{F}(q)}{\hat{E}(q)} u(t_k) + e(t_k). \tag{6.7}$$

The order of the numerator and denominator polynomials may be specified based on knowledge of the system, inspection of data, or adjusted iteratively until a satisfactory fit is found. Coefficients are calculated by minimizing mean-squared error (MSE) given by

$$MSE = \frac{1}{N} \sum_{k=1}^{N} [\overline{Q}_G^G(t_k) - \hat{Q}_G^G(t_k)]^2. \tag{6.8}$$

Several methods for performing this minimization with related constraints and performance analysis are presented in [114]. The state space model of inverter dispatch dynamics satisfying this minimization is given by

$$\hat{G} : \begin{cases} x(t_{k+1}) = \hat{A}_G x(t_k) + \hat{B}_G u(t_k) \\ y(t_k) = \hat{C}_G x(t_k) + \hat{D}_G u(t_k) + v(t_k). \end{cases} \tag{6.9}$$

hereafter denoted $\hat{G}$.

Figure 6.4 illustrates that inverter dynamics can be modeled well with only input and output data.

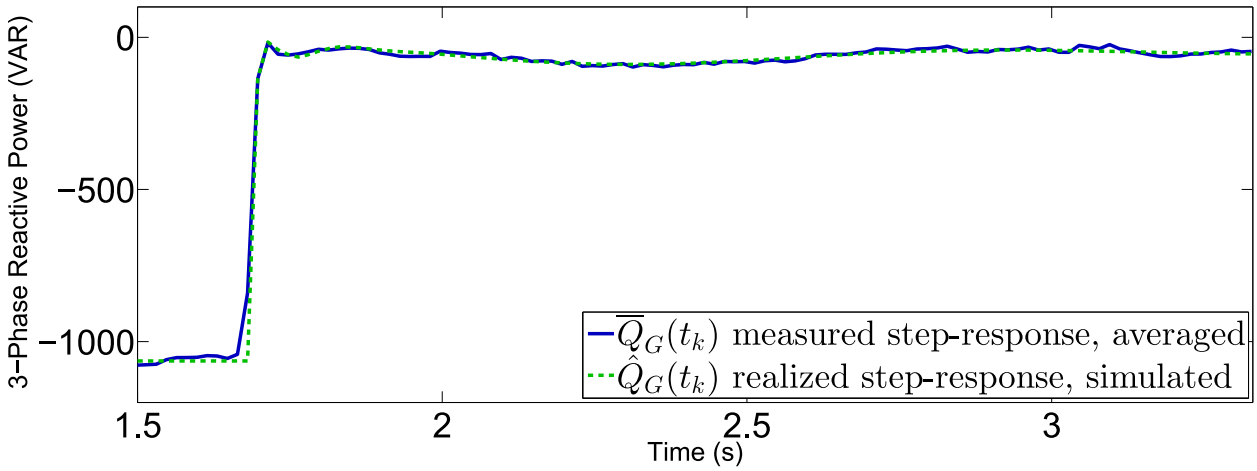

Figure 6.4: Comparison of the averaged actual measurements taken during a step change in inverter reactive power output $\overline{Q}_G^G(t_k)$ and the response of the model calculated using OE method to the same input $\hat{Q}_G^G(t_k)$.

6.3 Robust Controller Design

The model of load switching dynamics $\hat{H}$ and the model of inverter dispatch dynamics $\hat{G}$ provided by system identification are imperfect. The aim of robust control theory is to develop controllers tolerant of model error. An H_∞ controller limits maximum possible amplification across the frequency spectrum [115], making H_∞ control well suited to our system.

The H_∞ design process frames a problem in a standard form depicted in Fig 6.5. In the figure, $w(t_k)$ indicates an exogenous disturbance input, $u(t_k)$ a control input, $z(t_k)$ the output(s) to be controlled and $y(t_k)$ the output to be used for feedback.

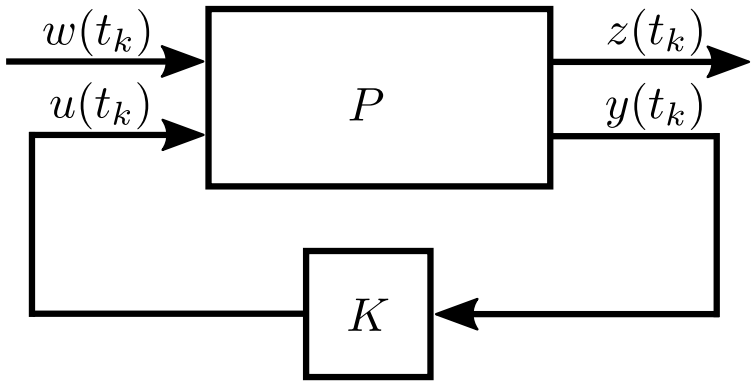

Figure 6.5: The standard block diagram of plant and controller structure assumed for calculation of an H_∞ controller.

The disturbance input maps to the load switching. System total reactive power is to be controlled and the penalty on the control signal will be adjusted to achieve desired performance, making these signals the controlled outputs. Measurements of system reactive power also serve as the controller input, allowing expression of the problem in standard form:

$$\begin{bmatrix} z_Q(t_k) \\ z_C(t_k) \\ y_Q(t_k) \end{bmatrix} = \begin{bmatrix} \hat{H}_d F_{LP} & \hat{G} \cdot \hat{H}_d \\ 0 & \gamma F_{HP} \\ \hat{H} F_{LP} & \hat{G} \cdot \hat{H} \end{bmatrix} \begin{bmatrix} w(t_k) \\ u(t_k) \end{bmatrix}, \tag{6.10}$$

where $\hat{H}$ and $\hat{G}$ denote the realized dynamic models discussed in the previous section, F_{HP} and F_{LP} are high and low-pass filters, respectively, and γ is a scalar gain. The $\hat{H}_d$ term is a system internal model containing the poles of load switching dynamic model $\hat{H}$. As discussed in [56], this structure drives the controller calculation to return a controller with closed-loop transmission zeros corresponding to the disturbance poles. Fig 6.6, illustrates how the standard form expressed in (6.10) relates to the standard plant depicted in Fig. 6.5.

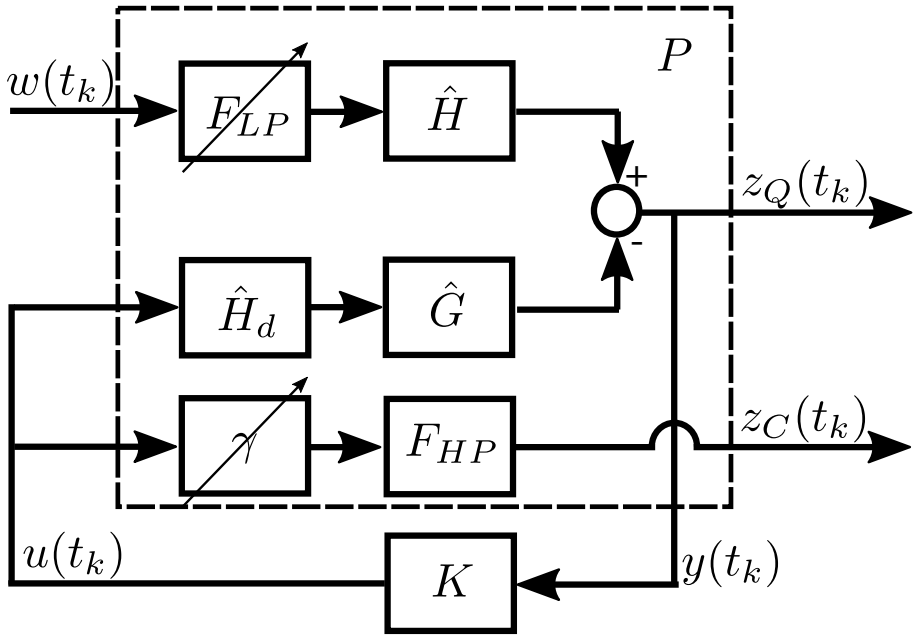

Figure 6.6: Block diagram of the test apparatus, annotated to show relation to the standard plant used in H_∞ control design.

Adjustable parameters γ and the coefficients in low-pass filter F_{LP} allow loop shaping as

discussed in [116]. Coarse tuning of γ modifies the penalty on control signal $z_c(t_k)$ vs total reactive power $z_Q(t_k)$. A well-selected γ value minimizes the oscillatory dynamics of the load switching in closed loop. High-pass filter F_{HP} is applied to the controller output to emphasize the penalty on the control signal at high frequency.

The low-pass filter F_{LP} serves as an accumulator to correct for the DC component to the load switching. For simplicity, the filter is designed in continuous time as

$$F_{LP} = \frac{s + \lambda_n}{s + \lambda_d}, \tag{6.11}$$

where λ_n allows adjustment of where the filter transitions from integration to unity gain, and λ_d is kept at the minimum value that results in a stable controller.

As discussed in [55], there is a waterbed effect between loop shaping parameters γ and λ_n, where a change in one affects tuning already done on the other. The interrelation of these parameters is subject to local minima in closed-loop DC gain and gain at the natural frequency of the load. A Monte Carlo approach or brute force iteration can be used to optimize, or hand-tuning may suffice if computing resources are limited or optimization is not critical.

The calculation of H_∞ controller K^* can be expressed as

$$K^* = \underset{K}{\operatorname{argmin}} \left\| \begin{matrix} T_{Qw}(q) \\ T_{Cw}(q) \end{matrix} \right\|_\infty, \tag{6.12}$$

where $T_{Qw}(q)$ and $T_{Cw}(q)$ are the closed-loop transfer functions from disturbance input $w(t_k)$ to reactive power $z_Q(t_k)$ and the control signal $z_C(t_k)$, respectively. The minimization may be accomplished using the two-Riccatti method discussed in [117] or using Linear Matrix Inequalities as in [118]. As seen in Fig. 6.6, the internal model is not included in the calculated controller K^*, so the controller to be implemented is defined as $C = K^*\hat{H}$.

Computer simulation of reactive power in response to switch closure with controller C providing closed-loop feedback is presented in Fig. 6.7. As seen in the figure, controller C greatly reduces the oscillations and DC offset, settling in approximately half a second.

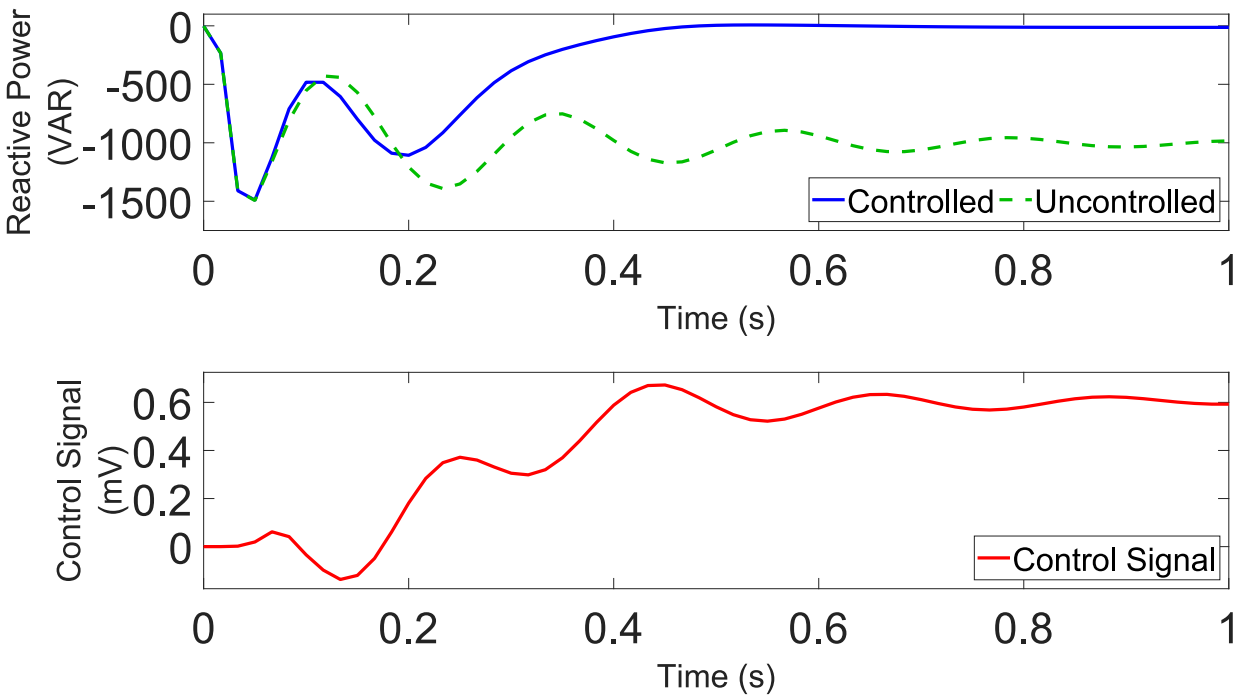

Figure 6.7: Simulated reactive power after switch closure with H_∞ controller controlling inverter reactive power output alongside simulated open loop response for reference (top), and the simulated control signal to the inverter.

Figure 6.8 shows Bode magnitude plots for controller C and open and closed loop dynamic response of reactive power when the load is connected. As can be seen in the figure, the controller has the desired properties mentioned above: The low-pass filter assures accumulation at low frequencies to correct the DC aspect of the load, and a resonance at the natural frequency of the load, approximately 4.5 Hz, corrects the oscillatory behavior. Filter F_{HP} of Fig 6.6 drives the high-frequency roll off as shown in the figure, focusing control action at the load natural frequency as seen in the lower half of Fig. 6.7.

Controller robustness to perturbation of the load model are illustrated in Fig. 6.10. In the figure, model of load switching dynamics $\hat{H}$ was altered by small shift of model poles, with the difference denoted by subscripts ϵ. Models $\hat{H}_{\epsilon 2}$ and $\hat{H}_{\epsilon 4}$ shift poles along the real axis, $\hat{H}_{\epsilon 1}$ and $\hat{H}_{\epsilon 3}$ along the complex; $\hat{H}_{\epsilon 1}$ and $\hat{H}_{\epsilon 2}$ shift poles toward zero , $\hat{H}_{\epsilon 3}$ and $\hat{H}_{\epsilon 4}$ away.

As can be seen in the figure, the controller corrects the disturbance despite changes in disturbance dynamics, though the correction for the oscillation suffers most. This is expected,

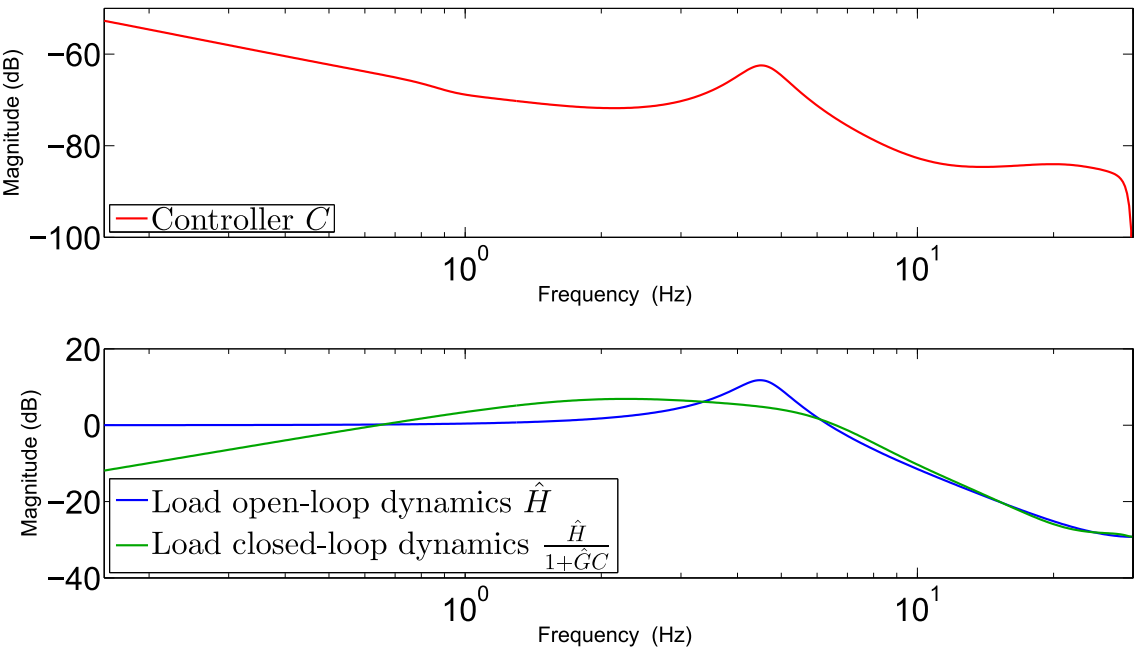

Figure 6.8: Bode magnitude plot of controller (Top), and open and closed loop dynamic response when the load is switched in.

since the natural frequency of the load switching dynamic model was changed, and the controller was specifically designed to compensate at that natural frequency of the nominal model via the internal model principal.

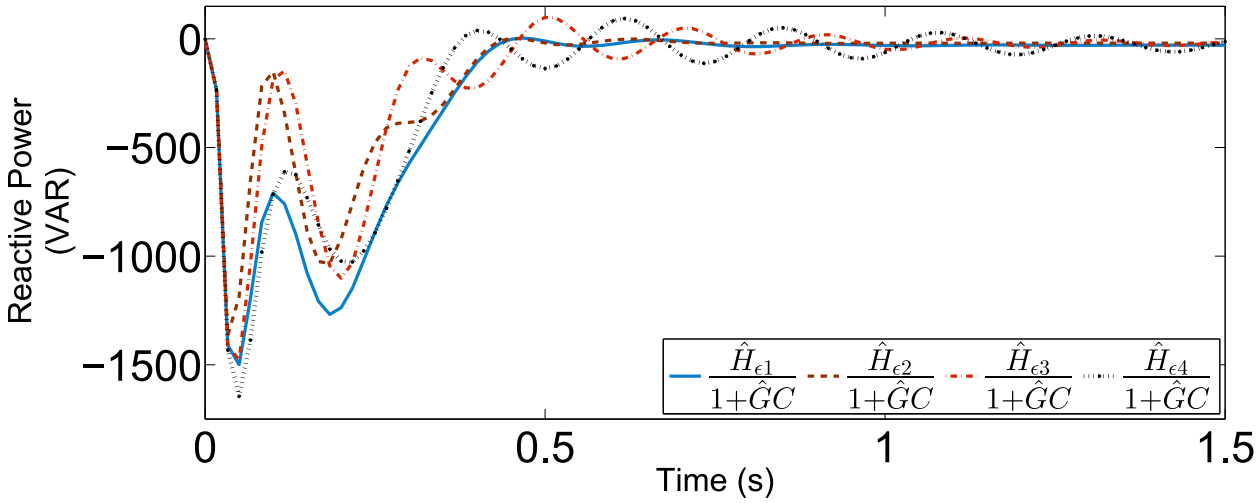

Figure 6.9: Dynamic response to load switching with perturbed disturbance oscillation models.

6.4 Implementation and Testing

The SyGMA Lab is equipped with a Grid-Tied Inverter (GTI) capable of four quadrant control, kindly donated by industry partner One-Cycle Control. The inverter uses three-level pulse-width modulation in a six-switch topology. The controller is implemented on a Compact RIO (cRIO) microcontroller graciously provided by National Instruments. The microcontroller is equipped with a micro processor and integrated field programmable gate array (FPGA), as well as current and voltage sensors and an analog output card used to interface with the inverter. A physical implementation of the reference circuit, a DC power supply, switchgear, and connection to utility power make up the remaining blocks from Fig. 6.1.

The cRIO analog output card is capable of providing a 0-20mV signal. The GTI acts as a current source, with power controlled by four voltage inputs. One input maps 4-20mV linearly to reactive power from 0 to 100A at 120 V. Another does the same mapping for active power, but was set to constant zero power output during reactive power control. One digital input communicates to supply or consume active power, and another to lead or lag with reactive power. Taken together, these signals enable four-quadrant power output from the GTI.

The controller C was implemented as a transfer function in the microprocessor. The integrated FPGA supplies demodulated reactive power $Q_G(t_k)$ as input, and the controller supplies inverter input signals using a small piece of additional code that was needed to shift the transfer function output into gain and lead/lag signals that could be interpreted by the GTI.

As seen in Fig 6.10, the response of the live circuit is very similar to that predicted by the simulation of the nominal load depicted in Fig 6.7.

6.5 Conclusion

This chapter presents an input/output data-based approach to formulate dynamic models of a reactive load and an inverter using realization and optimization. The dynamic model of the reactive load serves as an internal model for design of a feedback controller to dispatch reactive

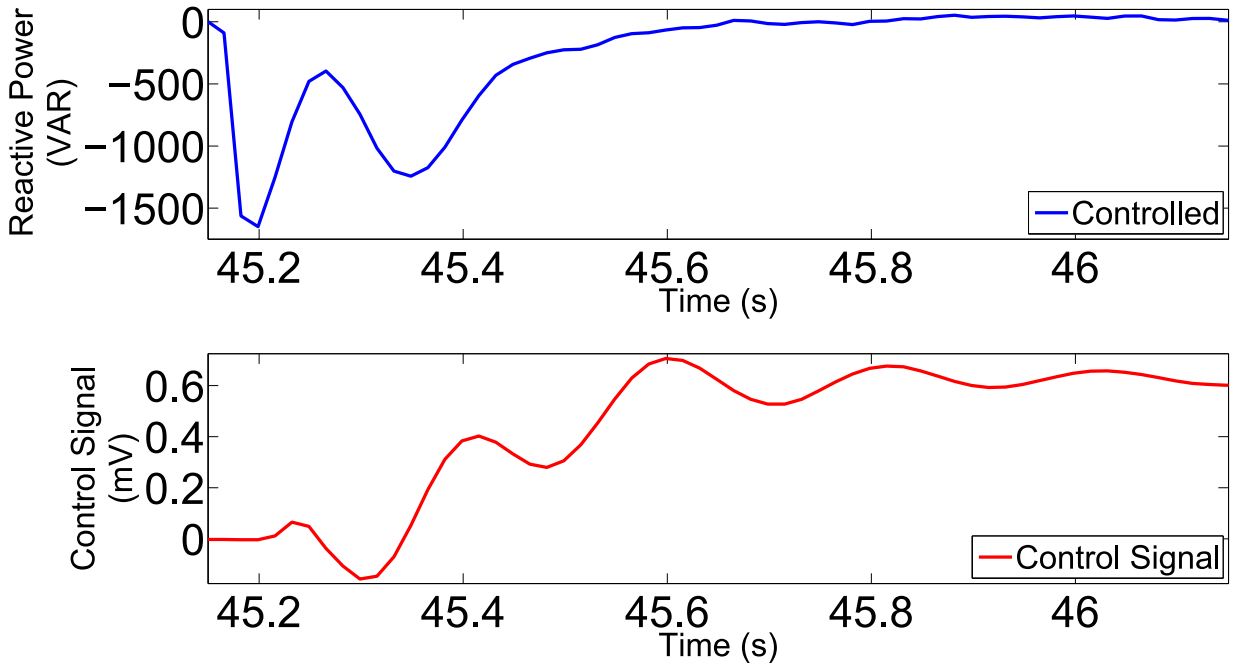

Figure 6.10: Actual reactive power after switch closure with H_∞ controller controlling inverter reactive power output (top), and the actual control signal to the inverter.

power from the inverter. As a result, the inverter/controller combination mitigates reactive power oscillations and DC offset caused by switching in the dynamic load. Controller performance is demonstrated on a live circuit and is shown to be robust against model uncertainty. The similarity between simulated and actual performance validates assumptions used in controller development, particularly demonstrating the synergy between system identification and robust control.

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Chapter 7

Conclusions

Increased adoption of renewable energy resources acting through DC-AC inverters has reduced the proportion of inertia stabilizing electric grids. One approach has been to reproduce the droop relationship of conventional generators in inverters. This approach is backward facing and does not utilize the fast control of power output possible with inverters. Synchrophasors are an emerging technology in electric grid monitoring and control, but have poor data quality at the initiation of power transients and are susceptible to injection of false data through GPS spoofing.

Signal processing limitations made initial efforts discussed in Chapter 2 only sporadically reproducible. These limitations are overcome with a combination of radio communication technology and novel use of locally available signal data. Chapters 4 and 5 of this dissertation discuss an improved demodulation algorithm. The improved signal processing algorithm distinguishes between active and reactive power disturbances and harmonic distortion, even when total harmonic distortion on input signals is very high. The algorithm supplies an input suitable to subsequent feedback control efforts.

Chapter 6 uses the algorithm as input to robust reactive power disturbance rejection control. Open loop algorithm outputs serve as input-output data for model development via system identification. Those models are then used as internal models of controllers robust against model uncertainty. Controller robustness is analyzed and real-time feedback control of a modern inverter

is demonstrated on actual hardware, with close fidelity between simulation and actual results. Rapid changes in inverter power output are shown to neutralize transient oscillations, and can be used to quickly return power to pre-transient levels.

The contributions of this dissertation are ennumerated as follows:

- **Active Power Disturbance Rejection**

  High penetration of distributed and renewable power generation systems challenges the conventional paradigm of stabilizing power systems with the standard rotational inertia used in power generation. To improve the stability of a power system, advanced disturbance rejection control techniques are used to provide damping and power disturbance mitigation. An approach for three-phase (real) power disturbance mitigation using real-time feedback control is outlined in Chapter 2.

  The control algorithm for power disturbance rejection is formulated via the internal model principle, computed via minimum variance control and designed to operate with a commercial grid-tied inverter. The end result is a real-time controlled inverter that is able to reduce power disturbances created by unanticipated load changes in an electrical grid.

  An experimental setup is used to validate the proposed control algorithm through on/off switching of a dynamic load and the results illustrate the feasibility of the proposed controller for real-time mitigation of power flow oscillations.

- **Open Loop Demodulation**

  Load switches in power systems may cause oscillations in active and reactive power flow. Such oscillations can be damped by synthetic inertia provided by smart inverters providing power from DC sources such as PV or battery storage. However, AC current provided by inverters is inherently non-sinusoidal, making measurements of active and reactive power subject to harmonic distortion. As a result, transient effects due to load switching can be obscured by harmonic distortion.

An RLC circuit serves as a reference load. The oscillation caused by switching in the load presents as a DSB-SC signal. The carrier frequency is available via voltage data but the phase is not. Given a group of candidate signals formed from phase voltages, an algorithm based on Costas Loop that can quickly quantify the phase difference between each candidate and carrier (thus identifying the best signal for demodulation) is presented in Chapter 5. Algorithm functionality is demonstrated in the presence of inverter-induced distortion.

- **Reactive Power Disturbance Rejection**

  Most devices in use for providing reactive power compensation or volt-var control do so in discrete steps due to underlying switching architecture. DC to AC inverters offer an advantage in that they can provide reactive power over a continuous range. The contribution of Chapter 6 is to present a data-based method to control reactive power compensation with an inverter.

  System identification methods are leveraged to develop a dynamic load switching model and inverter dispatch model, relieving the burden of detailed analysis of inner workings of these elements. Because of uncertainty inherent in the models developed, a robust control approach is used. Robust control reduces amplification across certain frequencies, making it suitable for limiting oscillations caused by switching in a reactive load. Loop shaping allows controller tuning to balance between compensating for DC components and transient dynamics.

  The performance of a controller designed using the method is validated by implementation on a live, grid-connected circuit with a switching inductive load.

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Appendices

A Products of Sinusoids and Amplitude Modulation

This appendix is included to help visualize the effect of multiplying two sinusoidal signals, with impact on Amplitude Modulation techniques. Consider trigonometric identities:

$$\begin{aligned}\cos(\theta_1)\sin(\theta_2) =& \frac{1}{2}\Big[\sin(\theta_1+\theta_2)-\sin(\theta_1-\theta_2)\Big]\\ \cos(\theta_1)\cos(\theta_2) =& \frac{1}{2}\Big[\cos(\theta_1+\theta_2)+\cos(\theta_1-\theta_2)\Big]\\ \sin(\theta_1)\sin(\theta_2) =& \frac{1}{2}\Big[\cos(\theta_1-\theta_2)-\cos(\theta_1+\theta_2)\Big]\end{aligned} \tag{A.1}$$

Methods for demodulating an amplitude modulated signal are based on the resultant behavior of the product of two sinusoidal signals as expressed in A.1. Two cases will be discussed: Behavior when $\theta_1 << \theta_2$ is fundamental to how information is encoded in AM signals, and behavior when $\theta_1 = \theta_2 + \phi$ is leveraged to decode the information.

A.1 Modulation: $\omega_1 << \omega_2$

Amplitude modulation is used to transmit information by varying the amplitude of a higher frequency carrier signal via a lower frequency information signal. When multiplied, the amplitude of the information signal limits the amplitude of the carrier. The envelope of the combined signal is dictated by the information signal. Figure A.1 illustrates with an AM signal defined by A.1 with a 5Hz sinusoid as the information signal, $\omega_I = 10\pi$ and a 60Hz sinusoid as the carrier $\omega_C = 120\pi$.

Note, in the figure the carrier signal phase shifts π radians at the zero crossings of the information signal. This complicates the reconstruction of the information signal. In AM radio broadcasting, the information signal is given a DC offset such that zero crossings are entirely avoided. Figure A.2 illustrates with the information signal given a DC offset of 2, making the left hand side of A.1 $\big[\cos(\omega_I t)+2\big]\cos(\omega_C t)$. The information signal then can easily be isolated with a diode envelope detector.

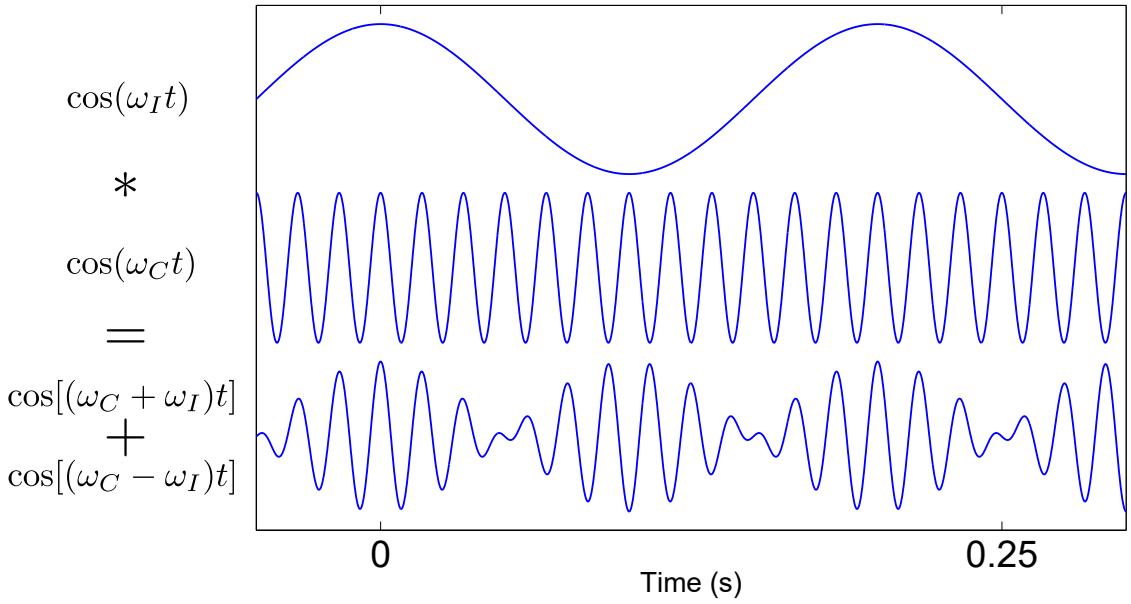

Figure A.1: Equation A.1 visualized

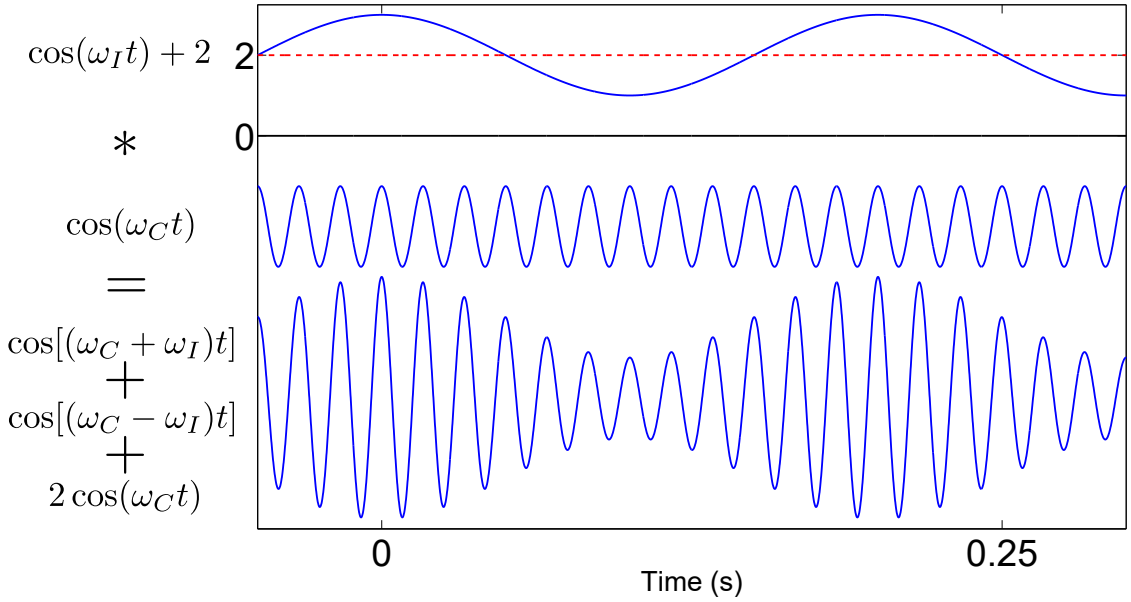

Figure A.2: AM with MI=0.5

In AM terms, an input signal without a DC offset is referred to as Dual Sideband Suppressed Carrier, discussed in Section A.3. If there is no DC offset, or if the DC offset is insufficient to avoid zero crossings, then an envelope detector cannot be used to isolate the information signal and demodulation using the methods of section A.2 must be used.

A.2 Demodulation: $\omega_2 = \omega_1$

Demodulation of an AM signal with zero crossings of the information signal is accomplished by multiplying by another sinusoid at the carrier frequency. Returning to the AM signal plotted in Figure A.1, then Equation A.1 multiplied by $\cos(\theta_2 + \phi)$ (where θ_2 is variable and ϕ is a constant phase offset) becomes

$$I(t)\cos(\omega_1 t)\cos(\omega_1 t + \phi) \tag{A.2a}$$

$$= \frac{1}{2} I(t)\Big[\cos(2\omega_a + \phi) + \cos(\phi)\Big]. \tag{A.2b}$$

The information signal in (A.2b) is no longer multiplied by the carrier and can be isolated by low-pass filtering. The amplitude of the extracted signal is reduced by factor $\frac{1}{2}\cos(\phi)$. Then, if the amplitude of the signal is important, or if inversion might cause problems, knowledge of ϕ is necessary. The resolution of the information signal will be greatest when ϕ is equal to zero, referred to as the 'best' demodulation in this dissertation.

A.3 DSB-SC vs Conventional AM

The meaning of the term Dual Side Band - Suppressed Carrier can be intuited from A.1: The sum and difference of carrier and information each form a side band of the carrier, but the carrier itself does not appear. Figure A.3 shows the Fourier transforms of a DSB-SC signal and an AM signal for comparison. The suppressed carrier of a DSB-SC signal make demodulation with a PLL impossible due to π radians phase shift at the zero crossings of the information signal.

B Phase locked loops

A Phase Locked Loop (PLL) is a standard tool for reproducing a carrier wave-form at a location where the broadcast carrier is not available. They are well suited to frequency demodulation [119] and have benefits over amplitude demodulation done by a diode detector [120]. In a PLL, the

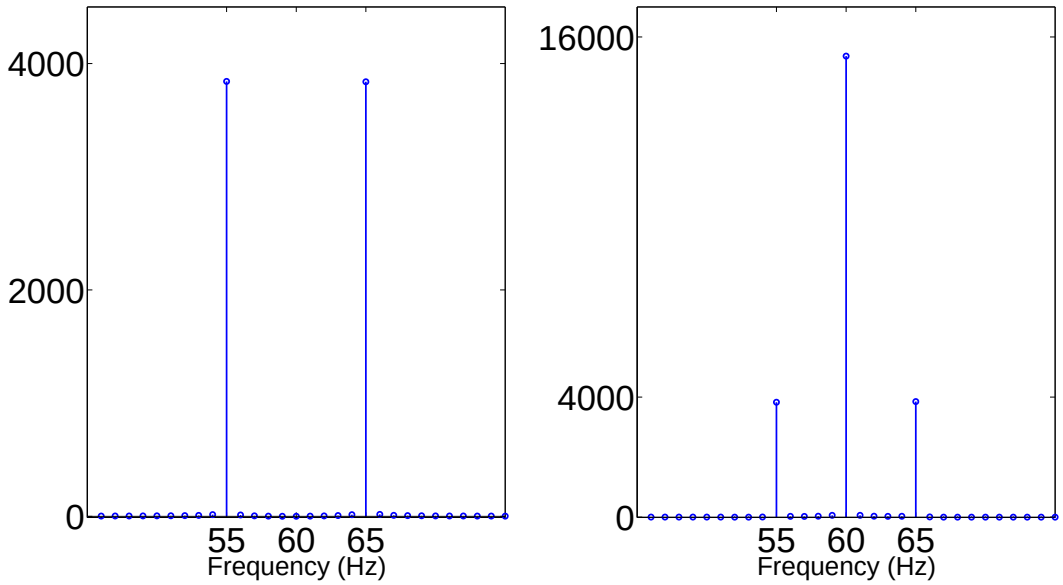

Figure A.3: DFT of DSB-SC and conventional AM signals.

input signal is multiplied by a voltage controlled oscillator (VCO) output, then passes through a low-pass filter as shown in Fig. B.4. This signal is then applied to VCO input as feedback, and also serves as the output. Consider (A.1) with a phase difference and small variation in input frequency:

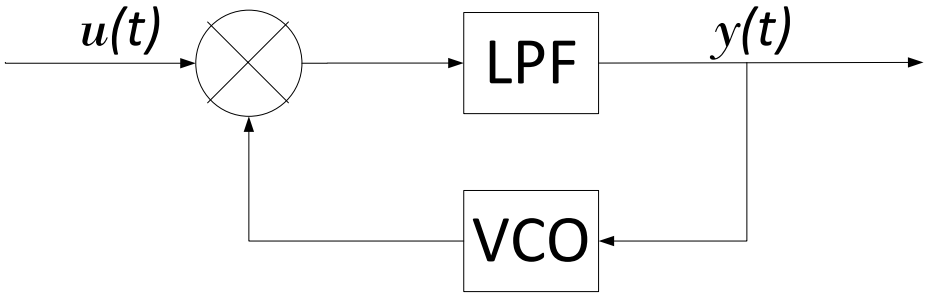

Figure B.4: A phase-locked loop used for demodulation. $u(t)$ is a generic input, $y(t)$ is a generic output.

$$\underbrace{I(t)\cos[(\omega_c \pm \epsilon)t]}_{\text{input}}\underbrace{\cos(\omega_c t + \phi)}_{\text{VCO}} = \frac{1}{2}[\cos(2\omega_c + \phi)t + \cos(\phi)]. \tag{B.3}$$

Then, with low-pass filtering:

$$F_{LP}(q)\frac{1}{2}[\cos(2\omega_c + \phi)t + \cos(\phi)] \approx \frac{1}{2}I(t)\cos(\phi). \tag{B.4}$$

The low-pass filter output varies with the phase difference between the VCO and input signal, forming the feedback mechanism. Referring to (B.3), if the input frequency increases, the phase difference would decrease, leading the $\cos\phi$ term to increase, speeding up the VCO output to match frequency of the input. The reverse is true for input frequency decreases. Unfortunately, for dual-sideband suppressed-carrier signals the carrier makes π radian phase shifts at zero crossings of the demodulated signal, making PLLs ineffective for demodulation.