Title

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An Ultra Compact Watt-Level Ka-Band Stacked-FET Power Amplifier

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***Abstract*— An ultra-compact watt-level Ka-band monolithic microwave integrated circuit (MMIC) power amplifier (PA) is demonstrated using a 0.15 µm Gallium Arsenide (GaAs) stacked field effect transistor (stacked-FETs) configuration. The fabricated PA exhibits 31.5 dBm output power, 17 dB gain and 33% power added efficiency (PAE). The bandwidth is from 26 GHz to 31 GHz. The PA achieves 0.7 Watt/mm^2 power density at 28 GHz. To the best of our knowledge, this PA achieves the highest power density among reported GaAs Ka-band PAs.**

***Index Terms* — Power Amplifer, Stacked-FET, Ka-band, Gallium Arsenide, MMIC.**

I. Introduction

Millimeter-wave PAs have been the focus of research for the emerging 5G wireless communications in recent years. GaAs is attractive for PAs and is a relatively low bandgap material that can limit the voltage swing of a transistor. Most GaAs PAs operating at Ka-band have a rated 4 V or 5 V maximum drain bias which limits the output power. Stacked-FETs are an alternative approach to handle high voltage swing for devices. Stacked-FETs have been introduced primarily in Silicon complementary metal–oxide–semiconductor (Si CMOS) [1] to enhance the output power while very few GaAs stacked-FET PAs have been reported in literature. The works in [2] demonstrated a basic triple stacked-FET topology which achieved low gain. In [3], stacked-FET cells were employed in a single-stage PA at K-band along with Wikinson power combiners at the output. In both works, the overall power density is low or not reported. A V-band PA using stacked-FET reported in [4] has achieved 25 dBm output power and 100 mW/mm^2 power density at 61 GHz.

In this paper, we present the design and development of a fully integrated stacked-FET PA using 0.15 µm GaAs technology at Ka-band. The PA utilizes stacked-FETs with a novel layout configuration to achieve high isolation and high power in a compact design. The fabricated chip exhibits measured gain of 17 dB, maximum output power of 31.5 dBm and power density of 700 mW/mm^2. To the best of our knowledge, this is the first report of a stacked-FET power amplifier that achieves the highest power density at Ka-band among GaAs processes.

II. Circuit Design

Fig. 1a shows the proposed PA circuit. The amplifier is designed with two stages to provide a gain of 17 dB at Ka-band. The first stage (Q1) uses a 8 x 75 µm pseudomorphic high-electron-mobility transistor (pHEMT) to drive the second stage of stacked-FETs. The 8 x 75 µm device size is also chosen for each transistor in the stacked-FET configuration (Q2, Q3 and Q4, Q5). The gate bias of the common source (CS) transistor is 0.9 V so that the PA operates in class AB for balancing gain and efficiency. The common gate (CG) transistor biasing network will be discussed in the next section. The two devices are identical to ensure equal current handling capabilities and prevent one device from being saturated before connected the other. The source of the upper transistor is connected to the drain of the lower transistor. The layout and interconnection of two FETs strongly affect the PA overall performance. The connection used in previous arts [1]-[3] is the bridge-type shown in Fig. 1c. The bridge-type connection gives poor isolation and thermal characteristics. On the contrary, our layout having a short transmission line between the source and drain (Fig. 1b) would reduce the cross-talk between the gate and the source of a CG transistor by 7 dB as compared to the conventional bridge-type connection in Fig 1c. The high isolation gives the stacked FETs the approximate unilateral characteristic that eases the design of a multi-stage matching network and improves gain. Furthermore, the 70 µm thick transmission line used in our proposed connection would guarantee current handling capability and improve heat dissipation at high power operation. Thermal simulations were done for the two configurations in Fig. 1b and Fig. 1c at V_{d1} = 5 V, V_{d2} = 12 V, I_{d1} = 50 mA, I_{d2} = 90 mA using the SYMMIC thermal simulation package [5]. The simulation results show that our proposed layout configuration can reduce the maximum temperature by 18° Celsius as compared to the bridge-type approach.

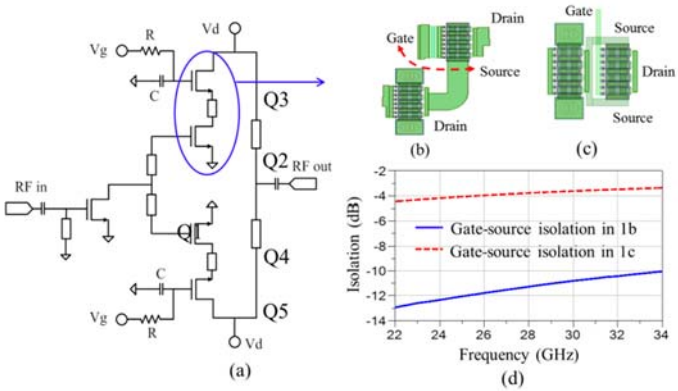

Fig. 1. (a) Proposed PA circuit, (b) Novel stacked-FET layout, (c) Stacked-FET layout in literature [2, 3], and (d) Simulated gate-source isolation of two configurations

A. Common gate transistor biasing circuit

The two most critical concerns in designing a high power stacked-FET PA are stability and voltage swing. A main source of the stability in a cascode-like configuration is that the input impedance of the CG transistor can possibly be negative because its source is loaded by the output capacitance of the preceding transistor. In a conventional cascode amplifier, the gate of the CG transistor is RF

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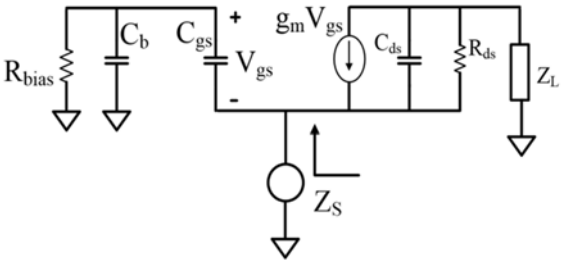


Fig. 2. Common-gate transistor equivalent circuit

grounded which would make the gate-drain voltage swing of the CG transistor exceed the breakdown at high power operation. On the contrary, in the stacked-FET configuration, a small capacitor is placed at the gate to control both the impedance and gate-drain voltage swing. Let's consider a simple equivalent circuit of a CG FET as shown in Fig. 2. At high frequency, the parasitic capacitance C_{gs} and C_{ds} would have the dominated effect. Therefore, if we neglect the effect of the bias resistor R_g and output resistance R_{ds}, the input admittance of the CG transistor in Fig. 2 can be given as

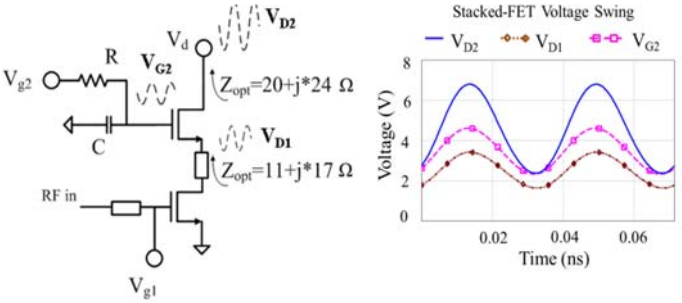
$$Y_S = \frac{\frac{C_b}{C_b + C_{gs}}(g_m + \omega^2 C_{gs} C_{ds}) + (\frac{C_b C_{gs}}{C_b + C_{gs}} + C_{ds})S}{1 - SC_{ds}} \qquad (1)$$

where Y_S is the admittance looked into the source of the upper transistor, ω is the frequency and S is the Laplace transform of the capacitors. If we consider C_{ds} is small enough and have negligible effect, (1) will reduce to:

$$Y_S = \frac{C_b}{C_b + C_{gs}}(g_m + SC_{gs}) \qquad (2)$$

According to equation (1), the value of the gate capacitor C_b would be chosen so that the real part of the impedance will be positive at all frequency to assure unconditional stability. In (2), the value of the gate capacitor also determines the optimum load seen by each transistor in the stacking topology. As seen in Fig. 3a, the optimum terminating impedance Z_{opt_Q3} at the drain of the upper FET (Q_3) of the stacked-FETs is (20+ j24) Ω. Note that Z_{opt_Q3} of the stacked-FETs is usually twice as large as the impedance of a single FET alone. Therefore, the output matching network has a lower impedance transformation ratio and can achieve a wider bandwidth.

The second issue of the high voltage GaAs PA is reliability. The gate-drain breakdown voltage of GaAs processes ranges from 10 V to 14 V. Therefore, when biasing the top drain at 12 V, there is a high risk that the upper FET would enter the breakdown region and would be damaged. To alleviate this problem, a large resistor is placed in parallel with the capacitor at the gate of the CG transistor to allow some voltage swings at the gate. The voltage swing at the gate and the drain are in-phase, thus reduces the gate-drain voltage difference and secures reliable operation at high power. Typically, equal voltage swings between the two transistors are desired to avoid early breakdown or early saturation. The gate bias of the CG transistor is a critical design parameter that would ensure equal voltage swing division. Voltage swings at each node in the stacked-FETs are shown in Fig. 3b.



(a) *(b)*

Fig. 3. Stacked-FET cell and voltage swing at each node

B. Power combining and matching network

A stacked FET (two FETs) can give an output power of 29 dBm. Hence, we only need a 2 to 1 power combiner for the two stacks (four transistors) to achieve a 32 dBm output power. To achieve the same output power in a conventional design, four FETs must be used in parallel with a 4 to 1 power combiner which will significantly increase the circuit size. Because the impedance matching ratio of the stacked FETs is two times smaller than that of a single FET, we can further reduce the chip size. The other advantage of using the 2 to 1 power combining scheme as compared to a triple stacked-FET in [2], [3] is that we can maintain high power added efficiency.

The value of the gate resistor and capacitor are 1 Kohm and 0.3 pF, respectively. An interdigitated capacitor is used to realize a 0.3 pF capacitance with minimal variation sensitivity. The output matching network contains one shunt stub TL1 to move the optimum impedance (20+ j24) Ω to the real axis and one series transmission line TL2 to rotate the impedance of each stacked-FET to 100 Ω. Since the two arms are completely identical, the impedance represented at the connecting point RFout would be matched to the 50 Ω. The inter-stage and input matching network utilizes several capacitors and dual shunt stubs to ensure symmetrical design.

III. Experimental Results

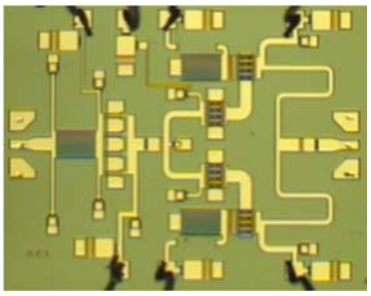


Fig. 4. Chip photo of the fabricated amplifier (1.6 mm x 1.3 mm)

The chip is fabricated in a 0.15-μm GaAs process. The chip size is 1.6 mm x 1.3 mm. The PA was measured using a Keysight network analyzer PNA-X N5247A and PXA Signal Analyzer N9030A. Fig. 5 shows the small signal performance of the PA at V_{d1} = 5 V; I_{d1} = 50 mA; V_{d2} = 12 V; I_{d2} = 90 mA. The maximum gain is 17 dB and maintains above 13 dB over a wide range of frequency from 26 GHz to 31 GHz. The input and output return loss is better than -10 dB. The stability factor K is larger than unity from DC to 35 GHz

TABLE I
COMPARISON TO OTHER PUBLISHED MILLIMETER-WAVE POWER AMPLIFIERS

Ref	Frequency (GHz)	Psat (dBm)	Gain (dB)	PAE (%)	Chip size (mm^2)	Power density (Watt/mm^2)	Structure	Technology
[2]	20-23	31.8	9.5	27	NA	NA	3-stacked	0.15 μm GaAs
[3]	16.5-22.5	33.7	14	29.5	11.2	0.21	4x3-stacked	0.15 μm GaAs
[6]	26.5-31.5	36	22	28	16.3	0.25	Parallel combining	0.2 μm GaAs
[7]	30-37	31	10	NA	10	0.13	Parallel combining	0.25 μm GaAs
[8]	34-38	30.1	9.5	NA	7.2	0.14	CPW combining	0.15 μm GaAs
[9]	32-36	37	24	30	14.93	0.33	Parallel combining	0.15 μm HV GaAs
[10]	27-31	33	20	NA	6.2	0.32	Parallel combining	0.25 μm GaAs
This work	**26-31**	**31.5**	**16.7**	**33**	**2**	**0.7**	**2-stacked + parallel combining**	**0.15 μm GaAs**

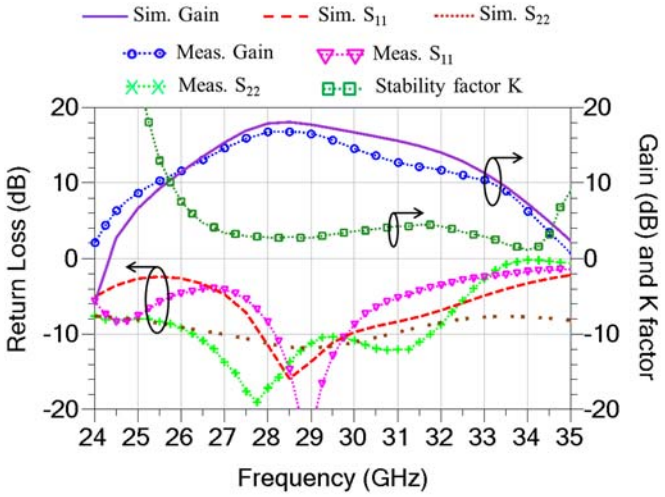


Fig. 5. Simulated and measured S-parameters

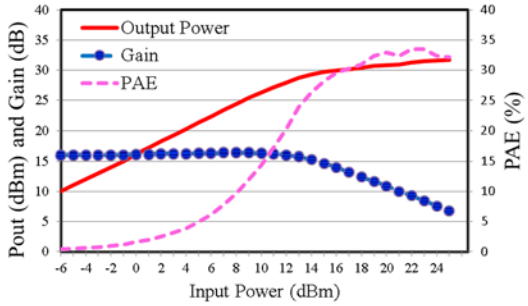


Fig. 6. Measured output power, gain and PAE at 28 GHz

to guarantee unconditional stability. In Fig. 5, the simulated and measured S-parameters from 24 GHz to 35 GHz are also compared. It can be seen that the measured results are well correlated with simulations.

Fig. 6 presents the output power, gain and efficiency of the PA at 28 GHz with the bias conditions as mentioned above. The output power at 1 dB compression point (OP1dB) is 29.5 dBm and the saturation power is 31.5 dBm. The maximum PAE is 33%. Fig. 7 shows the output power and PAE at 2 dB gain compression point from 26 GHz to 31 GHz. While the output power at 2 dB gain compression point exhibits over 29 dBm, the PAE maintains higher than 24% in the entire frequency range. The PA presents a wideband performance at Ka-band. Table I shows the comparison of our work to other millimeter-wave PAs published in literature.

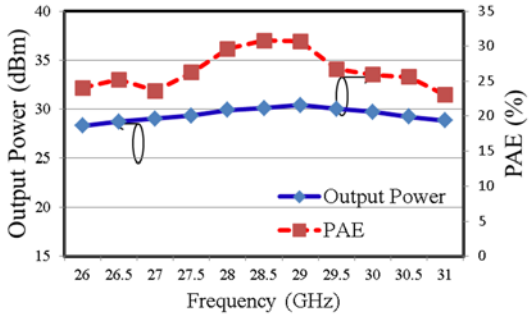


Fig. 7. Measured output power and PAE at 2 dB gain compression

IV. Conclusion

We demonstrate an ultra-compact stacked-FET PA which exhibits a measured gain of 17 dB, output power of 31.5 dBm and peak PAE of 33% at 28 GHz. The PA exhibits wideband performance which covers from 26 GHz to 31 GHz. The die size is 1.6 mm x 1.3 mm, making the power density 0.7 Watt/mm^2. To the best of our knowledge, this is the highest power density reported of all PAs at Ka-band up to date.

References

[1] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, P. M. Asbeck, "A Watt-Level Stacked-FET Linear Power Amplifier in Silicon-on-Insulator CMOS", *IEEE Trans. Micro. Theory Tech.,* vol.58, no.1, pp.57-64, Jan. 2010.

[2] T. Fersch, R. Quaglia, M. Pirola, V. Camarchia, C. Ramella, A. J. Khoshkholgh, G. Ghione, R. Weigel, "Stacked GaAs pHEMTs: design of a K-band power amplifier and experimental characterization of mismatch effects", *in IEEE Int. Micro. Symp. (IMS),* pp.1-4, May 2015.

[3] Y. Park, Y. Kim, W. Choi, J. Woo and Y. Kwon, "X-to-K band Broadband Watt-Level Power Amplifier Using Stacked-FET Unit Cells", in *2011 IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, pp.1-4, June 2011.

[4] M. Gavell; I. Angelov; M. Ferndahl and H. Zirath, "A high voltage mm-wave stacked HEMT power amplifier in 0.1 μm InGaAs technology," in *IEEE Int. Micro. Symp. Dig. (IMS),* pp.1-3, May 2015.

[5] http://www.capesym.com/symmic.html

[6] F.Y. Colomb; A. Platzker, "2 and 4 watt Ka-band GaAs PHEMT power amplifier MMICs," *in IEEE Int. Micro. Symp. Dig. (IMS),* pp.843-846, June 2003.

[7] C. W. Huang, S. J. Chang, W. Wu, C. L. Wu, and C. S. Chang, "Ka-Band 1-W pHEMT MMIC Power Amplifiers on 2mil-thick GaAs substrates", *Microwave And Optical Technology Letters*, vol. 45, no. 3, pp. 181-185, May 2005.

[8] A. Bessemoulin.; H. Massler; A. Hulsmann and M. Schlechtweg, "Ka-band high-power and driver MMIC amplifiers using GaAs PHEMTs and coplanar waveguides," *IEEE Microwave and Guided Wave Letters,* vol.10, no.12, pp.534-536, Dec. 2000.

[9] C.F. Campbell, D.C. Dumka, M.Y. Kao, D.M. Fanning, "High Efficiency Ka-Band Power Amplifier MMIC Utilizing a High Voltage Dual Field Plate GaAs PHEMT Process," *in IEEE Comp. Semi. Integrated Circuit Symp. Dig. (CSICS),* pp.1-4, Oct. 2011.

[10] TGA4513 (http://www.triquint.com/power-amplifiers)