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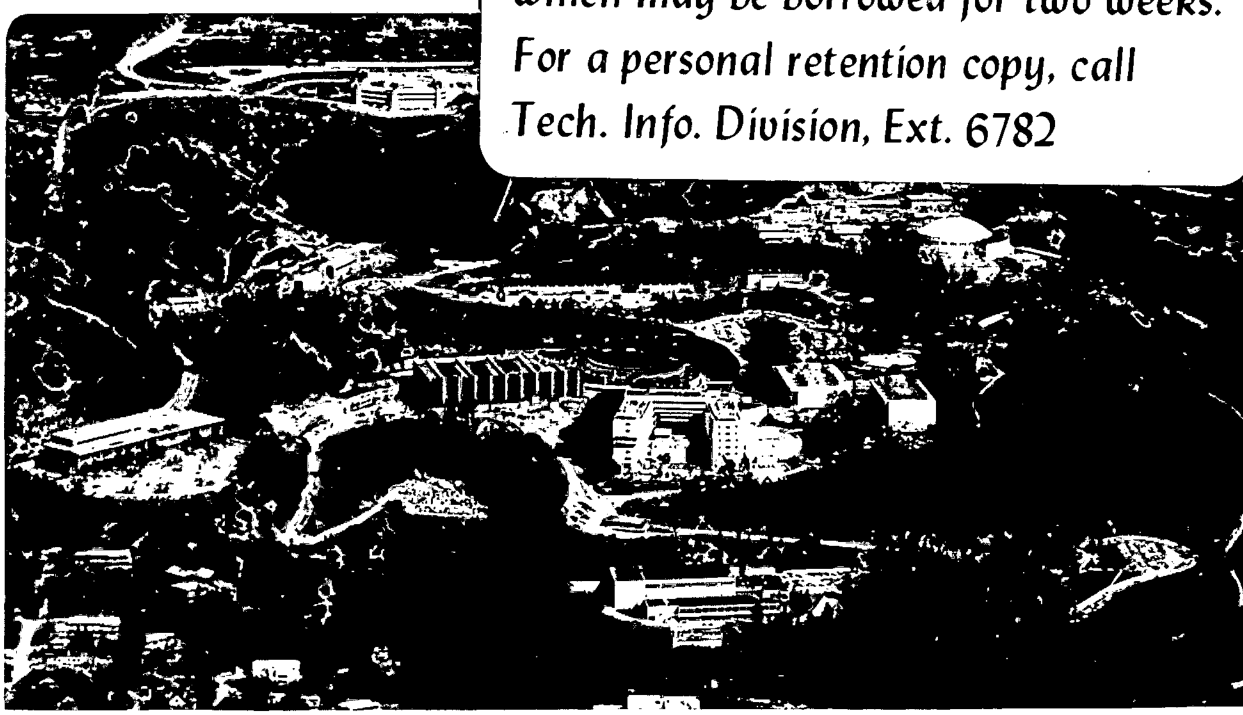

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Summary

The special problems associated with the Time Projection Chamber resulted in the development of a new preamplifier/amplifier system which is discussed here. The need for 16,000 channels of low noise electronics imposed serious constraints on the cost, size, and power consumption of the circuits. Also the preamplifiers are designed to work inside the detector chamber. This chamber operates at 10 atmosphere pressure and is sensitive both to the presence of magnetic materials that distort the drift field, and to the effects of gas contamination. These problems resulted in the use of new components and fabrication techniques as described in the paper. The large number of units involved requires automatic testing as discussed in the paper.

Introduction

The Lawrence Berkeley Laboratory Time Projection Chamber (TPC) being installed in PEP-4 at SLAC requires over 16,000 channels of low noise electronics in order to obtain the required energy, and position resolution. The basic features of the Time Projection Chamber are described in another paper in this issue.[1] There are approximately 1200 wires and 15,000 pads in the end caps mounted inside the gas volume with a low noise preamplifier closely connected to each. The wire signal amplitudes measure dE/dx along the track of the charge particles in about 4 mm radial segments. The delay time of the wire signals from a fast trigger measures the drift time of charge in the chamber and hence the axial position of a track. Finally, the distribution of signals in the pads determines the azimuthal position of a track.

Two slightly different types of preamplifiers are used, one matched to the pad and the other to the wire signals. The outputs of the preamplifiers pass through the detector pressure wall, and through approximately 30 m of coaxial ribbon cables to the shaping amplifiers that produce pseudo Gaussian pulse shapes peaking in about 250 ns. These shaped signals are sent to charge coupled devices (CCD) used as analog shift registers. Details of this portion of the system are given in another paper in this issue.[2]

Preamplifiers

The low noise preamplifiers have an equivalent input noise of 500 and 1000 electrons RMS (referred to the input), for the pad (5 pF load) and wire (20 pF load) respectively. Rise times are ≤ 50 ns and the operating power is nominally 100 mW. The preamplifiers use discrete components mounted on small plug-in P.C. boards. Miniature solid tantalum capacitors, 1/8 W resistors and SOT-23 packaged transistors are employed. The subminiature SOT-23 packaged transistors[3] were 100% factory electrically pretested; they have identical electrical specifications (excepting power ratings) in the equivalent devices in more conventional packages. The production cost of the preamplifiers, including parts, fabrication, and testing, was $13. This is about 1/2 to 1/3 the estimated cost of a comparable hybrid version of the unit.

Careful attention has been paid to components that might desorb electronegative materials into the TPC, as these would poison the counting gas. The long drift distance (1 meter) makes this particularly important in TPC. Also, components containing Kovar were excluded from the preamplifiers as ferromagnetic materials would distort the uniformity of the internal magnetic field of the TPC.

Figure 1 shows a photograph of the pad and wire preamplifier along with a scale to illustrate the small size. The pins on the wire preamplifiers are offset relative to the pad preamplifiers so that the preamplifiers can be plugged into both sides of the mother board. Figure 2 shows a photograph of a mother board with forty channels of preamplifiers plugged into both sides. This illustrates the preamplifiers' packing density in TPC. It also shows the integral shields used on the preamplifiers. Calibration test inputs for pad preamplifiers are on the mother board.

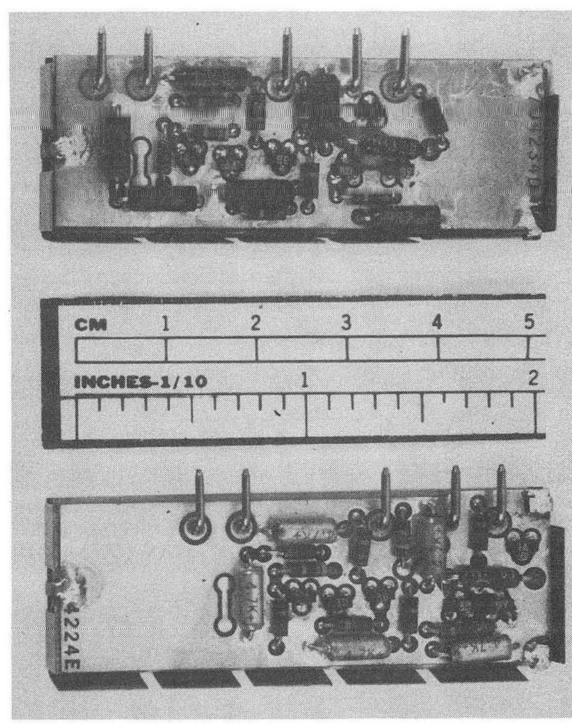

Fig. 1 Photograph of wire preamplifier (upper) and pad preamplifier (lower) along with a scale.

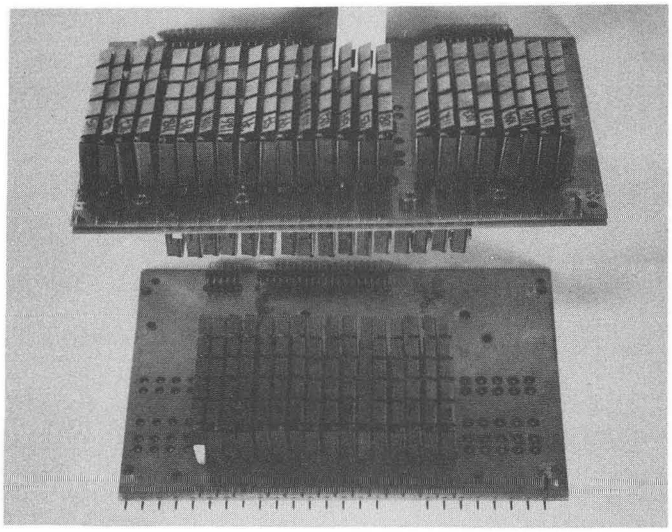

Fig. 2 Photograph of "mother board" with 24 pad preamplifiers and 16 wire preamplifiers with back side of mother board shown in a mirror.

Figures 3 and 4 are schematics of the pad and wire preamplifiers. A few differences exist between the pad and wire preamplifiers. Since the pad and wire signals are of opposite polarities, the output signals (linear current) are of opposite polarities for the two configurations. The feedback capacitors are of different values 0.5 pF for the pad and 1.0 pF for the wire preamp to partially compensate the difference in (input) signal amplitudes. Also an FET (Q5) is used as a level shifter in the wire preamplifier in order to provide adequate dynamic range.

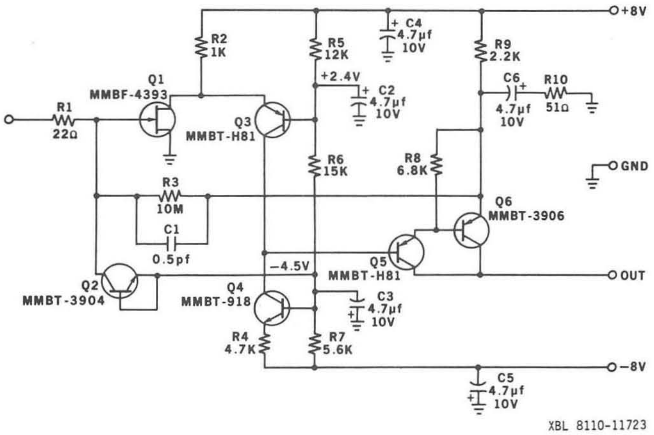

Fig. 3 Schematic of pad preamplifier

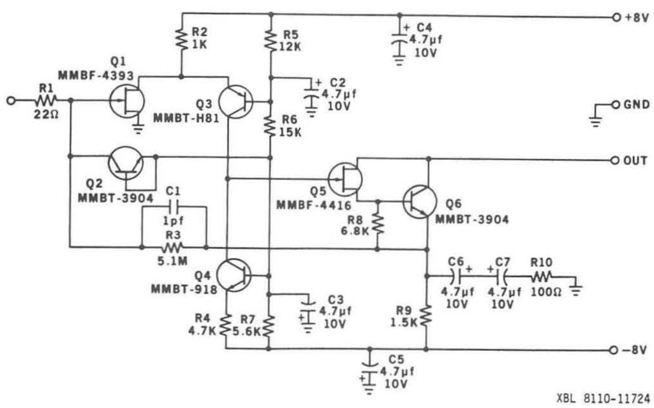

Fig. 4 Schematic of wire preamplifier

Prototyping and a preproduction batch of 200 preamplifiers was accomplished by hand soldering of the components. Wave soldering was used in the production phase. The circuit board is 1/16" thick Nema G-10 with plated-through holes. The SOT-23 transistors are placed on the ground plane side of the circuit board, the preformed leads sit in the plated-through holes. At this point a single lead on each device is hand soldered; this ensures correct positioning for the subsequent wave soldering.

Substantial cost savings were made by correct choice of two potentially expensive components. First the collector base junction of an SOT-23 transistor is used as the input protective diode. Secondly, rather than using a miniature low loss, expensive feedback capacitors, we chose to use a simple parallel plate capacitor using a small area of the printed circuit board. The dielectric is Nema G-10 and the capacitor plates are etched copper foil on either side of the P.C. board. This type of capacitor is suitable only for short peaking times as it can exhibit high losses and poor charge soakage properties.

Preamplifier Testing

The preamplifiers were tested simply by measuring the supply currents, then the high frequency gain was measured by injecting a 10 MHz calibrated amplitude signal into the preamplifier and measuring the output on a RMS voltmeter.

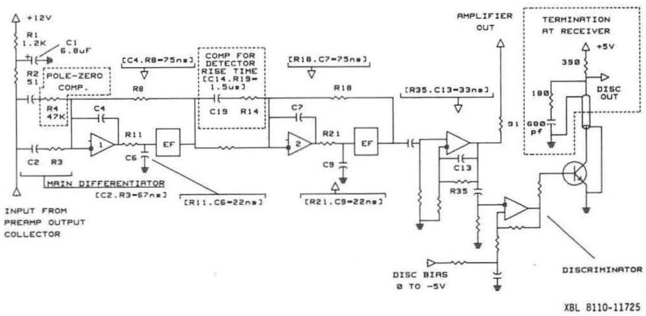

Fig. 5 Block diagram of wire shaping amplifier.

Shaping Amplifiers

The pad and wire shaping amplifiers are similar to each other except for the higher gain and input polarity reversal of the pad amplifiers. Both amplifiers use three amplifying and shaping stages and they produce negative going (approximately 5 Pole symmetrical Gaussian) output pulses with 250 ns peaking times. The voltage gain of the pad amplifier is roughly 220 and that of the wire amplifier is 160. Figure 5 shows the block diagram of the wire amplifier with the time constants of the shaping stages presented. The 51 ohm resistor at the input is the load resistance for the current ouput stage of the preamplifier. The preamplifier signal is differentiated and pole zero compensated (for the 5 µs decay of the preamplifier) at the input to the stage. The first and second stages contain active integration with each having two complex poles and a combined voltage gain of about 36. The output stage is non-inverting with a gain of roughly 4 for the wire amplifier and with a gain of roughly -6 (i.e., inverting) for the pad amplifier. The output stage has an additional RC integrator of 33 ns. The amplifier output is back terminated in 91 ohms and will drive a 2.5 V negative going pulse into a 90 ohm terminated coax cable or 5 V into an open circuit. The 1.5 μs differentiating time constant between the first and second stages is used to partially compensate for the slow components of the detector signal.[1] The wire amplifier also has a simple leading-edge discriminator on its output which is used in the trigger electronics system for TPC.

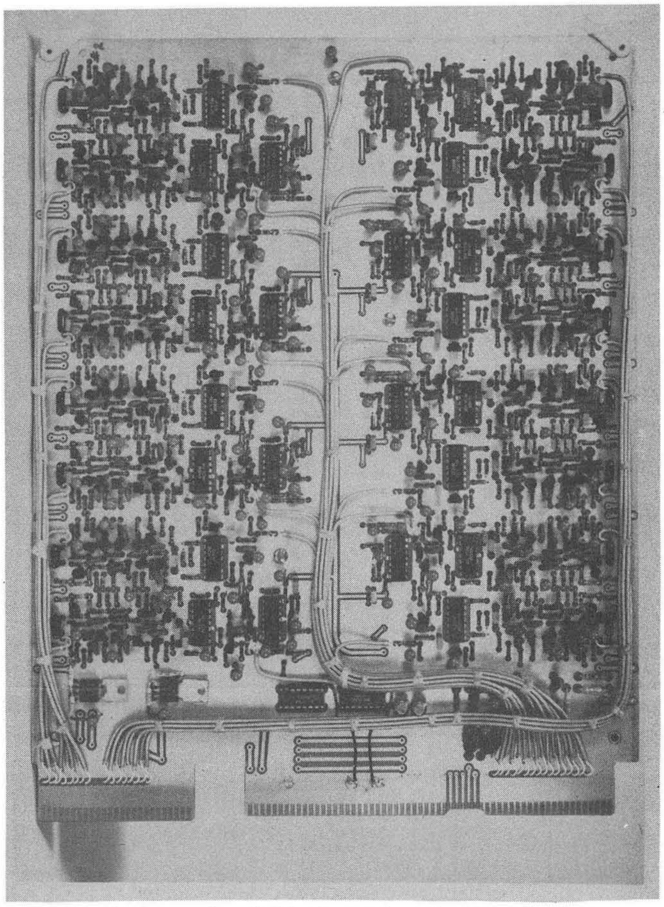

Fig. 6 Photograph of 16 channels of wire shaping amplifier.

Figure 6 shows a photograph of a 16 channel wire amplifier card. The card also contains the positive and negative 8 volt regulators for 16 preamplifiers and the temperature-compensated positive and negative 6 V rails needed for the amplifier stages. The schematic for one channel of the pad amplifier is shown in Fig. 7. The amplifiers use standard small inexpensive parts. The cost of the shaping amplifier, including the components, manufacturing and testing of the boards, was $400 for a board or equivalent to $28 per channel.

Computer Controlled On-Line Testing

TPC has an extensive computer-controlled pulser system for calibration and diagnostics of the elements in the linear channels. The 100 K ohm resistor and diode at the input of the first stage is used to supply a pulser signal to each amplifier. The pulser signal is generated (under computer control) in the 17th card in a bin containing 16 amplifier cards. A separate pulser signal is generated for each card of 16 amplifiers, but all 16 amplifiers on the same card are pulsed at the same time. A similar pulser system is used at the input of the CCD channel and also of the digitizer. These pulser signals are used to locate nonfunctioning boards in the system.

Automatic Production and Testing

All amplifier testing is performed in an automatic tester controlled by a small personal microcomputer (16K PET*). The manufacturer of both the wire and pad shaping amplifier boards used the automatic tester to control the quality of the boards and to provide a printed record of all the tests. The test time per board is less than two minutes. The memory expansion part of the PET computer was interfaced to four 8255 programmable periperhal interface chips that provided twelve 8-bit I/O ports to the tester. The 8255 was controlled and read by poke and peek commands in the "Basic" language of the PET computer.

A block diagram of the automatic tester is shown in Fig. 8. The following tests were performed on each amplifier.

(i) The power supply currents were checked several times through the testing period to check for leaky tantalum capacitors (which might have been inserted in the reverse direction during fabrication).

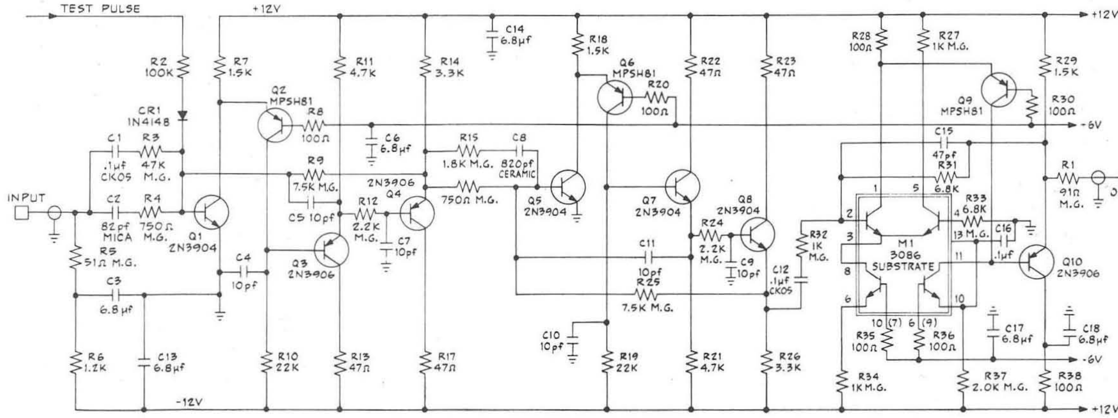

Fig. 7 Schematic of one channel of pad amplifier

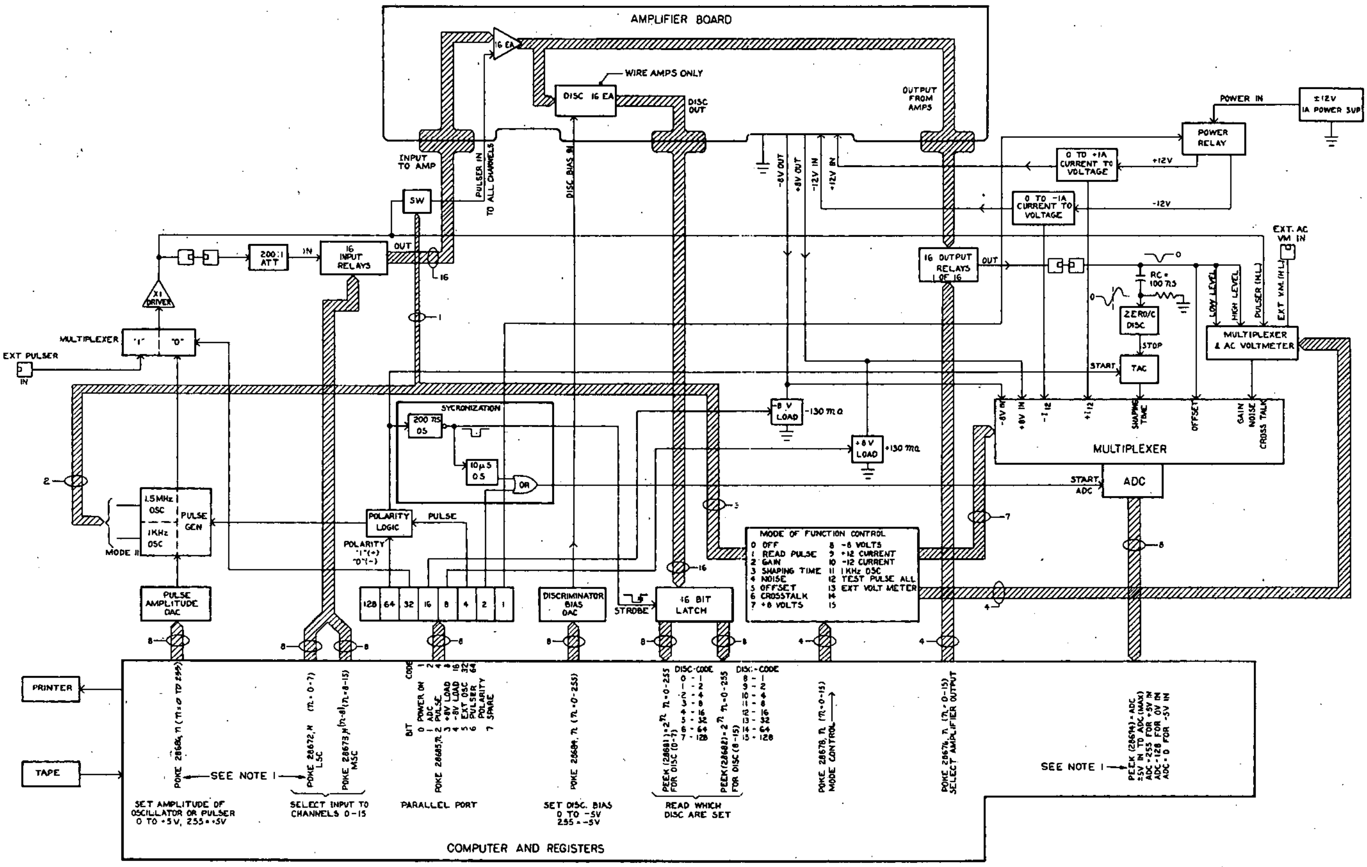

Fig. 8 Block diagram of automatic tester used to test shaping amplifiers

(ii) The ± 8 V regulator output voltages generated on the amplifier boards for the preamplifiers were checked.

(iii) D.C. offset at the amplifier output was measured.

(iv) The gain of each amplifier channel was measured.

(v) The noise was measured for each channel.

(vi) Crosstalk was checked by pulsing every channel except the one being tested.

(vii) The pulse shape of the output pulse was measured.

(viii) The input test pulser was checked.

(ix) In the case of the wire amplifiers the output discriminator operation was checked.

The tests results were compared with a set of limits stored in the program and all measurements were printed out with error messages. A typical printout is shown in Table I.

Conclusion

The Time Projection Chamber represents the first use of low noise electronics in large numbers of channels in high energy physics experiments. The design of the amplifiers and preamplifiers discussed here meet all requirements at the very low cost as required in these applications.

Wire Amp. Board 31X1501P-1 SN#-42

+Current is 710 MA (Initial Readings)
-Current is -563 MA (Initial Readings)
+8.5 Volt Reg. (Unloaded) is 8.4 Volts
+8.5 Volt Reg. (Loaded) is 8.3 Volts
-8.5 Volt Reg. (Unloaded) is -8.6 Volts
-8.5 Volt Reg. (Loaded) is -8.6 Volts
+Current is 710 MA (Recheck)
-Current is -563 MA (Recheck)

Amp #	Offset Volts	Gain V/V.	Nois NV	S/T NSEC.	C/T %	DISC. 2^N	T/P VOLTS
0	.02	166	9	510	.7	0	142
1	.02	174	11	510	.9	0	137
2	.02	166	9	517	1.2	0	129
3	.04	170	9	510	1.3	0	141
4	.04	174	11	517	1.4	0	150
5	.04	166	9	517	1.4	0	131
6	.02	170	14	510	1.5	0	127
7	.02	166	9	510	1.4	0	128
8	0	170	11	510	1.3	0	128
9	.02	170	14	510	1.5	0	136
10	.02	170	9	510	1.4	0	138
11	.04	174	9	510	1.5	0	148
12	.04	155	9	510	1.2	0	141
13	.02	170	7	502	1	0	132
14	.04	178	7	510	.7	0	138
15	.02	166	11	510	.9	0	127

+Current is 695 MA (Recheck)
-Current is -563 MA (Recheck)

List of Tests and Limits are -
1 DC Offset (-.2 to +.2V)
2 Gain (150 to 190)
3 Shaping Time (475 to 530 ns)
4 Crosstalk (0 to 5.0%)
5 Noise (0 to 25 MV)
6 Discriminator (0 if OK)
7 Pulser Input (75 to 160)
8 Current Limits are -
+(750-600)MA -(600-500)MA
9 Reg. (8V) Limits are (8.8-7.8)V

Tests for wire Amp SN#42 are within limits
0 Tests Failed

TABLE 1

Acknowledgments

This work was carried out as part of a close collaboration with the TPC physics group headed by D. Nygren. R. Jared, the project engineer for the TPC electronics and F. Petro played important parts in expediting and supervising the production of the units. A Jue and E. Converse fabricated early prototypes.

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*References to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

References

1. R.C. Jared, D.A. Landis, and F.S. Goulding, "Analog Signal Processing for the Time Projection Chamber." To be published in IEEE Trans. Nucl. Sci., NS-29, February 1982.

2. R.C. Jared, T.Y. Fujita, H.G. Jackson, S.B. Sidman, F.S. Goulding, "Use of CCDs in the Time Projection Chamber." To be published in IEEE Trans. Nucl. Sci., NS-29, February 1982.

3. SOT-23 Transistors obtained from Motorola Hybrid Component Marketing Division, P.O.Box 2453, Phoenix, Arizona 85062.