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Scanned Probe Characterization of Semiconductor Nanostructures

A dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

James Jeremy MacDonald Law

Committee in charge:

Professor Peter M. Asbeck, Co–Chair

Professor Edward T. Yu, Co–Chair

Professor Prabhakar R. Bandaru

Professor Andrew C. Kummel

Professor Deli Wang

2009

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The dissertation of James Jeremy MacDonald Law is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Co–Chair

____
Co–Chair

University of California, San Diego

2009

Dedication

To my friends, family, and loved ones.

Epigraph

Two roads diverged in a yellow wood,
And sorry I could not travel both
And be one traveler, long I stood
And looked down one as far as I could
To where it bent in the undergrowth;

Then took the other, as just as fair,
And having perhaps the better claim,
Because it was grassy and wanted wear;
Though as for that the passing there
Had worn them really about the same,

And both that morning equally lay
In leaves no step had trodden black.
Oh, I kept the first for another day!
Yet knowing how way leads on to way,
I doubted if I should ever come back.

I shall be telling this with a sigh
Somewhere ages and ages hence:
Two roads diverged in a wood, and I—
I took the one less traveled by,
And that has made all the difference.

–Robert Frost

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LIST OF ABBREVIATIONS AND SYMBOLS

AFM	Atomic force microscopy
CAFM	Conductive atomic force microscopy
CBE	Chemical beam epitaxy
CL	Cathodoluminescence
CNT	Carbon nanotube
CVD	Chemical vapor deposition
EBL	Electron beam lithography
FWHM	Full width at half maximum
FE–SEM	Field emission scanning electron microscopy
HVPE	Hydride vapor phase epitaxy
LEO	Lateral epitaxial overgrowth
LSS	Ligand–aided solution–solid
MBE	Molecular beam epitaxy
MIS	Metal–insulator–semiconductor
MOCVD	Metal organic chemical vapor deposition
MQW	Multiple–quantum–well
NWFET	Nanowire filed effect transistor
OMVPE	Organo–metallic vapor phase epitaxy
PAMBE	Plasma assisted molecular beam epitaxy
QCSE	Quantum–confined Stark effect

RMS	Root mean squared
SA–OMVPE	Selective area organo–metallic vapor phase epitaxy
sccm	Standard cubic centimeters per minute
SCM	Scanning capacitance microscopy
SCS	Scanning capacitance spectroscopy
SEM	Scanning electron microscopy
SKPM	Scanning Kelvin probe microscopy
slm	Standard liters per minute
SPM	Scanning probe microscopy
SPS	Scanning probe spectroscopy
STM	Scanning tunneling microscopy
TEM	Transmission electron microscopy
TMI	Trimethylindium
UHF	Ultra high frequency
UID	Unintentionally doped
VLS	Vapor–liquid–solid
VSS	Vapor–solid–solid
XTEM	Cross–sectional transmission electron microscopy

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Like any long journey, this one was not undertaken without the guidance, help, reassurance, and support of many of my friends, family and colleagues. Looking back, I have some fervent memories and some mere wisps, but chances are, if you have taken the time to read this, whether for academic or personal reasons, I must thank you.

Any graduate student can plainly tell you that their time and experience in graduate school, whether good or bad, was shaped most primarily by their interactions with their adviser. I am, therefore, very happy to thank Professor Ed Yu for all the positive encouragement he has given me. His insight, intelligence, patience, and thoroughness have been invaluable to me in all aspects of my work, and his example is an archetype which I continually seek to emulate. I am sure he would say that he was just doing his job, a testament to his humility, but I believe he has greatly exceeded that standard for me and every other student he has had the chance to mentor.

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VITA

2004	B. S., Electrical Engineering (*magna cum laude)*, University of Pennsylvania
2007	M. S., Electrical Engineering, University of California, San Diego
2008	C. Phil., Electrical Engineering, University of California, San Diego
2009	Ph. D., Electrical Engineering, University of California, San Diego

Journal Publications

1. J. J. M. Law, E. T. Yu, B. A. Haskell, P. T. Fini, S. Nakamura, J. S. Speck, and S. P. DenBaars, "Characterization of nanoscale electronic structure in nonpolar GaN using scanning capacitance microscopy," *J. Appl. Phys.* **103**, 014305 (2008), doi: 10.1063/1.2828161.

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3. J. J. M. Law, E. T. Yu, G. Koblmüller, F. Wu, and J. S. Speck, "Low dislocation–mediated reverse bias leakage in (0001) GaN via high–temperature MBE growth," to be submitted to *Appl. Phys. Lett.*

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4. J. J. M. Law, S. A. Dayeh, D. Wang, and E. T. Yu, "Scanning capacitance characterization of potential screening in InAs nanowire devices," *Proceedings of the 8th IEEE Conference on Nanotechnology (2008 IEEE NANO), 2008*, pp. 569–572, doi: 10.1109/NANO.2008.168.

Conference Presentations

1. J. J. M. Law, S. A. Dayeh, D. Wang, and E. T. Yu, "Scanning capacitance characterization of potential screening in InAs nanowires," presentation at 2008 Electronic Materials Conference, Santa Barbara, CA, June 2008.

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4. J. J. M. Law, G. Koblmüller, F. Wu, J. S. Speck, and E. T. Yu, “Low dislocation mediated reverse bias leakage in (0001) GaN via novel high–temperature MBE growth,” presentation at 2009 Electronic Materials Conference, University Park, PA, June 2009.

5. G. Koblümuller, J. J. M. Law, F. Wu, R. Chu, A. Raman, U. K. Mishra, E.T. Yu, and J. S. Speck, “High–temperature PA–MBE growth of (Al)GaN–based electronic structures on (0001) GaN templates and dislocation mediated effects,” presentation at 8th International Conference on Nitride Semiconductos, Jeju, Korea, October 2009 (*accepted)*

ABSTRACT OF THE DISSERTATION

Scanned Probe Characterization of Semiconductor Nanostructures

by

James Jeremy MacDonald Law

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University of California, San Diego, 2009

Professor Edward T. Yu, Co–Chair

Professor Peter M. Asbeck, Co–Chair

Advances in the synthesis of materials and device structures have accentuated the need to understand nanoscale electronic structure and its implications. Scanning probe microscopy offers a rich variety of highly spatially accurate techniques that can further our understanding of the interactions that occur in nanoscale semiconductor materials and devices.

The promising nitride semiconductor materials system suffers from perturbations in local electronic structure due to crystallographic defects. Understanding the electronic properties and physical origin of these defects can be invaluable in mitigating their impacts or eliminating them all together. In the second chapter of this dissertation, scanning capacitance microscopy (SCM) is used to characterize local electronic structure in *a*–plane *n*–type gallium nitride. Analysis reveals the presence of a linear, positively charged feature aligned along the $[\bar{1}100]$ direction which likely corresponds to a partial dislocation at the edge of a stacking fault. In the third chapter, conductive atomic force microscopy is used to determine the effects of Ga/N flux on the conductive behavior of reverse–bias leakage paths in gallium nitride grown by molecular beam epitaxy (MBE). Our data reveal a band of fluxes near Ga/N $\approx$ 1 for which these pathways cease to be observable. These observations suggest a method for controlling the primary source of reverse–bias Schottky contact leakage in *n*–type GaN grown by MBE.

A deeper understanding of the interaction between macro–scale objects and nanoscale electronic properties is required to bring the exciting new possibilities that semiconductor nanowires offer to fruition. In the fourth chapter, SCM is used to examine the effects of micron–scale metal contacts on carrier modulation and electrostatic behavior in indium arsenide semiconductor nanowires. We interpret a pronounced dependence of capacitance spectra on distance between the probe tip and nanowire contact as a consequence of electrostatic screening of the tip–nanowire potential difference by the large metal contact. These results provide direct

experimental verification of contact screening effects on the electronic behavior of nanowire devices and are indicative of the importance of accounting for the effect of large–scale contact and circuit elements on the characteristics of nanoscale electronic devices.

1 Introduction

1.1 Introduction

The ongoing struggle to understand and synthesize matter at increasingly smaller scales was well articulated by Richard Feynman with his 1959 address to the American Physics Society, "There's Plenty of Room at the Bottom: An Invitation to Enter a New Field of Physics."[1] Feynman postulated about the possible methods for achieving exacting control of matter at the molecular and atomic scale such that one could fit the entire Encyclopedia Britannica on the head of a pin, while simultaneously extolling the virtues of achieving such fine control over matter at that scale. This goal was first achieved in 1985 when the opening pages of Dickens' A Tale of Two Cities were written by electron beam lithography in an area of 5.9 µm × 5.9 µm (each letter was approximately 50 nm tall).[2] Since then, scanned probe techniques have had the distinction of creating the highest information storage densities. In 1990, a scanning tunneling microscope (STM) was used to position single xenon atoms on a nickel surface to spell the acronym IBM, with each letter being approximately 5 nm in height.[3] In 2008, the record was reset, again with STM, with letters being made by the interference of electron waves at different frequencies to achieve densities higher than previous thought possible (each letter was measured approximately 1.25 nm in height).[4] Aside from the honor of creating very small letters, scanned probe techniques enable a plethora of analytical tools with vast applications.

Perhaps the semiconductor industry has best exemplified the goal of unrelenting miniaturization suggested by Feynman 50 years ago. The trend, coined in 1970 by Carver Mead as Moore's Law, of doubling the number of transistors on an integrated circuit every two years has allowed the utter permeation of our daily lives with inexpensive and reliable electronic devices with a myriad of functionality. As semiconductor devices scale to increasingly infinitesimal dimensions, the importance of understanding and synthesizing matter at these scales has necessitated the inception of highly spatially accurate, localized nondestructive microscopy and spectroscopy techniques. Accordingly, scanned probe techniques have come to offer a wonderful synergy of basic science and engineering capabilities.

Scanning probe microscopies (SPM) and spectroscopies (SPS) offer access to a broad spectrum of analytical tools with an ever increasing plethora of applications. Scanned probe techniques typically utilize a stylus probe, with apex varying between 5 nm and 1 μm in radius, held in contact or close proximity to a surface of interest. The material composition of the probe tip dictates the nature of the physical interaction that occurs between the tip and sample, and thus, they can vary drastically depending on the application spanning the range of insulator,[5] semiconductor,[6] and metal.[7] Different embodiments of scanning probe techniques rely on different physical interactions to relay information about the sample under investigation. STM utilizes tunneling currents[8] to investigate the local density of states of a sample.[9] Other proximal probe techniques examine vertical[10] and lateral forces[11] and force gradients,[12] resulting from van der Waals,[10] electrostatic,[13] and magnetic

interactions.[14, 15] The probe tip can also be used to measure electrical characteristics such as conductance[16] and capacitance[17] by incorporating additional circuitry. Atomic force microscopy (AFM) is a technique that leverages the advantages of many of the interactions described above. It was originally conceived as a way of measuring very small vertical forces between a small probe tip and a solid sample,[10] and it generated topographic images similar to STM but was capable of operating on insulating surfaces that yielded little tunneling current. Later, AFM was further modified to measure many of the interactions described above.

1.2 Constant Contact Atomic Force Microscopy

AFM typically utilizes a sharp probe tip with radius of curvature between 5 and 50 nm mounted to a cantilever with small mass in order to minimize the force required for high sensitivities. The cantilever–tip assembly is brought near the surface of the sample to be studied. Since the cantilever is a spring, any force acting on the probe tip will deflect the cantilever beam. In this case, repulsive forces from the surface deflect the cantilever. Topographic images can be made by utilizing the deflection of a cantilever beam and feedback to maintain a constant force on the surface. This deflection is most commonly measured by laser deflection, optical interferometry, or tunneling current.

Figure 1.1 shows an illustration of the type of AFM used in the experiments described in this dissertation. A sample is mounted to a chuck which sits on top of a piezoelectric tube. This piezoelectric motor can by actuated in x, y, and z independently by application of an appropriate voltage. The probes utilized in these

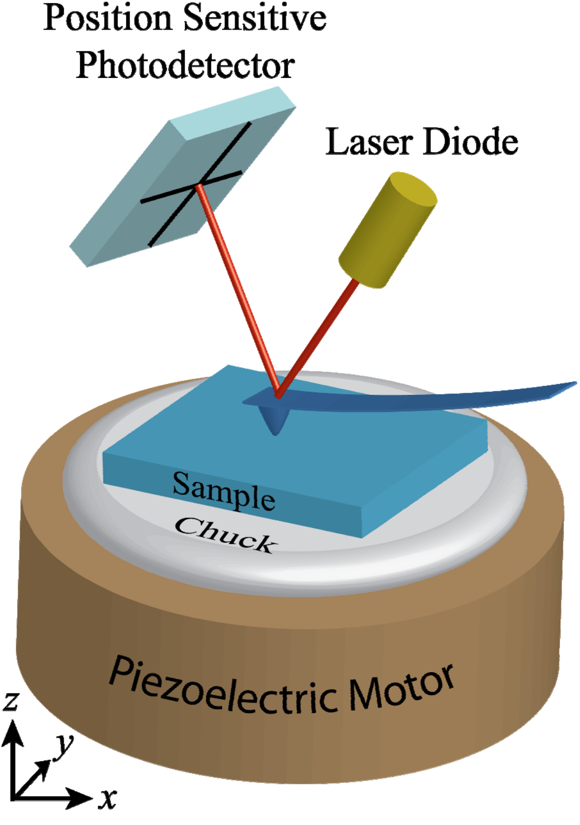

Figure 1.1. Schematic diagram of an atomic force microscope. The scanning probe tip is placed on or near the sample surface with the cantilever's deflection being monitored by the laser beam's position in the position–sensitive photodetector. The piezoelectric motor is used to raster the tip across the sample surface and measure topography by maintaining a constant position of the reflected laser in the photodetector.

studies are single crystal silicon processed with standard clean–room processing techniques and typically coated by either a metal or diamond. A laser is reflected off the back of the cantilever beam into a position sensitive (four–quadrant solid–state) photodetector. Typically, the position of the laser beam is adjusted until it falls in the center of the photodetector prior to bringing the sample in contact with the probe tip. After the probe is brought into contact with the sample, a feedback loop is established in order to maintain a constant position of the reflected laser beam in the photodetector

by changing the voltage that controls the vertical (z direction) piezoelectric position. By assuming that the movement of the piezoelectric is roughly linear with voltage and the use of precise calibration samples, the voltage applied to the piezoelectric motor can be converted into a measure of distance and recorded. This method of recording topography is known as constant contact mode AFM.[10] Due to the small area at the apex of the tip, tip degradation is a major concern for this type of measurement.

1.3 Tapping Atomic Force Microscopy

Since the cantilever is nothing more than a spring with a weight attached to its end, it has a natural resonance frequency. While the cantilever is not near the surface, it can be vibrated at its resonance frequency by applying an ac bias of the form $A\sin(\omega t+\phi)$ to another piezoelectric motor attached to the cantilever holder. The amplitude, frequency, and phase of the cantilever's movement can be detected using the position sensitive photodetector. Far from a surface, the cantilever is oscillated at its resonance frequency at a certain amplitude set by the user. As the cantilever is moved closer to a surface, the van der Waals forces between the tip and the surface will attract the probe tip to the surface thus changing its resonant amplitude, frequency, and phase. Using a root mean squared (RMS) amplitude detection scheme and a feedback loop, constant RMS amplitude of the cantilever's oscillation can be maintained by adjusting its height above a sample surface with the piezoelectric tube. The voltage applied to the piezoelectric tube can be converted to height and recorded as a function of the tips position to yield a topographic image of the samples surface. This type of measurement is known as tapping AFM.[18] Feedback on the tip's

frequency and phase can also be used to reconstruct surface topography. However, for the purposes of this dissertation, tapping mode AFM will refer exclusively to RMS amplitude detection. Tapping and contact mode AFM enable topographic measurements with height resolution on the order of angstroms and lateral resolutions limited by the radius of the tip (≈10–25 nm). Tapping AFM topographic measurements generally yield more accurate topographic information than constant contact AFM. Secondary imaging techniques such as magnetic, electrostatic, and electrical characterization are obtained by incorporation of the tip into specialized secondary circuit and feedback techniques.

1.4 Conductive Atomic Force Microscopy

The scanning probe tip naturally lends itself to local electrical characterization because of the highly accurate spatial positioning system of the AFM. The simplest of these techniques is the use of a conductive tip as a local electrical contact to probe sample conductivity. Figure 1.2 shows an illustration of probe and sample biasing arrangement for conductive AFM (CAFM). In CAFM measurements, an ohmic contact is fabricated on the sample, and the tip is used as the second, repositionable electrode. The nature of the contact that is made between the sample and the tip is determined by their respective material compositions and resulting work functions. The current generated from the application of a dc voltage between the two contacts is amplified and converted into a voltage by a transimpedance amplifier, and this signal is recorded simultaneously with topography, revealing the physical origin of local changes in sample conductance, with spatial resolution dictated by the tip size and any

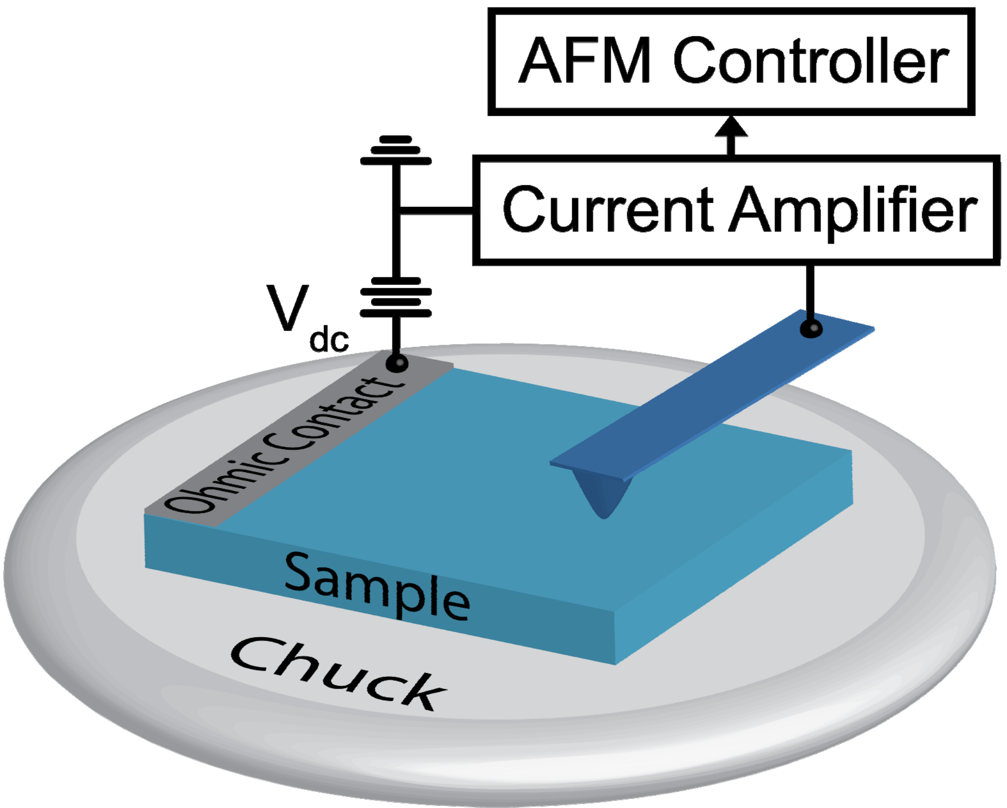

Figure 1.2. Schematic diagram of conductive atomic force microscopy. A bias is applied to the ohmic sample contact while current through the tip is amplified, converted to voltage, and recorded providing a measure of changes in local sample conductivity.

depletion region present in the sample beneath the probe tip. CAFM measurements are carried out in contact mode to ensure that the contact area between the tip and sample is kept as invariant as possible, for any significant change in the contact area between the two (resulting in a change of contact resistance) could be misinterpreted as an anomalous change in sample conductivity. The degradation of the tip coating and the tip itself is a serious concern for CAFM measurements, especially when measuring hard samples such as gallium nitride. The biasing arrangement between the

tip and sample need not be limited only to dc voltages: ac voltages may be used to do ac spectroscopy in order to determine sample impedance.

1.5 Scanning Capacitance Microscopy and Spectroscopy

The capacitance versus voltage, *C(V)*, behavior of a metal–insulator–semiconductor structure (MIS) can yield information about dopant/impurity distributions inside a structure,[19, 20] compositional distribution of the material itself,[21] and charge variation near defects or material inhomogeneities.[22] With the advent of the AFM, it became possible to use the AFM probe tip as a repositionable electrode to do highly spatially accurate *C(V)* measurements. In its modern incarnation, scanning capacitance microscopy (SCM) utilizes contact mode AFM in conjunction with a highly sensitive capacitance sensor such that the signal of the capacitance sensor is recorded in parallel with topography.[23] Thus, one can obtain the distribution of capacitance and topography over a surface. The sensor itself is a high Q resonant circuit which includes the capacitance of the sample–probe system and is excited by a UHF source. Because the resonance of the circuit is so sharp, small changes in the sample–tip capacitance cause small changes in the resonance frequency of the circuit which results in large changes of the output voltage of the circuit, which is recorded by a peak detector. Analysis of the capacitance sensor is beyond the scope of this introduction, but the general process is schematically illustrated in Figure 1.3. The initial resonance peak of the circuit is at a frequency f_0 as shown by the black line in Figure 1.3. A small change in the tip–sample capacitance results in a shift in the resonant frequency of the circuit as indicated by the red dotted line in Figure 1.3.

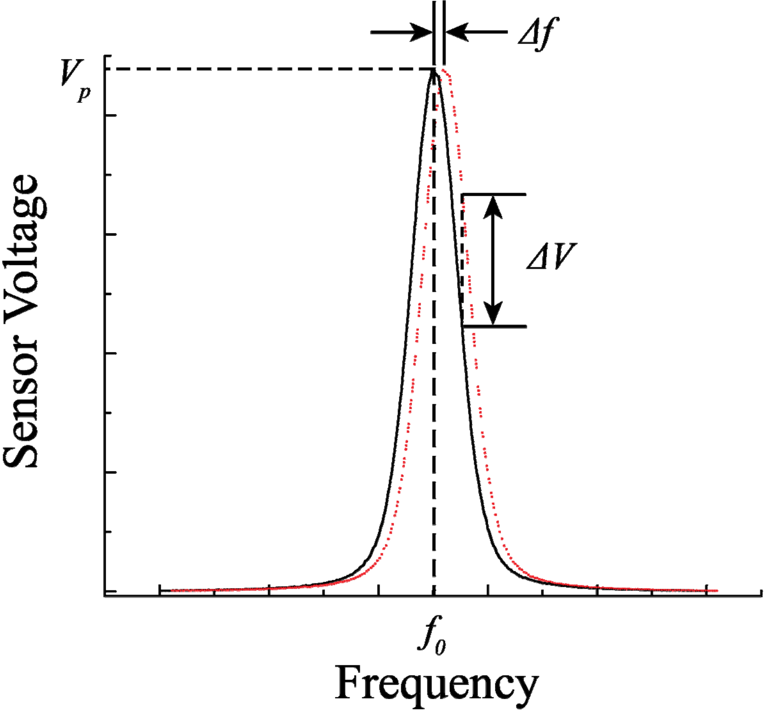

Figure 1.3. Capacitance sensor voltage response as a function of frequency. Shifts in resonant frequency (red dotted line) due to additional capacitive loading cause large changes in sensor output voltage.

Since the capacitance sensor circuit is operated at a fixed frequency, this small change in resonant frequency is accompanied by a large change in the sensor output voltage as indicated by ΔV in Figure 1.3. The stray capacitance between the cantilever and the sample is far larger than the small capacitance between the tip and the sample. Since the stray capacitance is so large, it is only possible to measure changes in capacitance. A detailed analysis of the SCM detection method[24] shows that the output of the sensor, ΔV, is given by:

$$\Delta V = \frac{1}{2}\left| c\gamma_0 f_D \frac{1}{C}\frac{dC}{dV}\bigg|_{V_{DC}} V_{AC} \right|$$

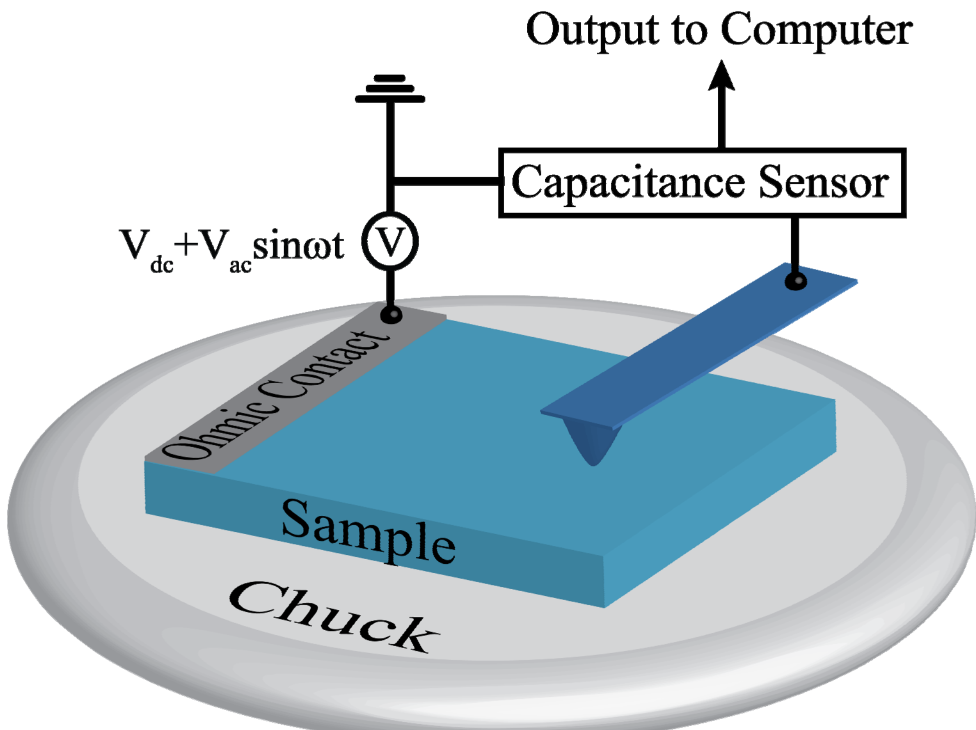

Figure 1.4. Schematic diagram of scanning capacitance microscopy. An ac bias is applied to the ohmic sample contact while changes in capacitance are detected using the resonant capacitance circuit and recorded simultaneously with topography.

where f_D is the drive frequency, c is a measured constant,[25] γ_0 is the frequency sensitivity,[25] which is approximately constant and equal to ½ for $f=f_D$, and C is the tip–sample capacitance. We see explicitly from the above equation that the measured change in sensor output voltage is proportional to dC/dV of the tip–sample capacitance at a given dc bias V_{dc}. Incredibly, commercial SCM sensors are capable of measuring capacitance on the order of 10^{-21} F.[26]

Figure 1.4 shows a schematic diagram of a typical SCM measurement geometry and voltage biasing arrangement. Typically, SCM functions by applying an ac voltage, V_{AC}, at a quiescent dc voltage V_{DC} and rastering the probe tip across the

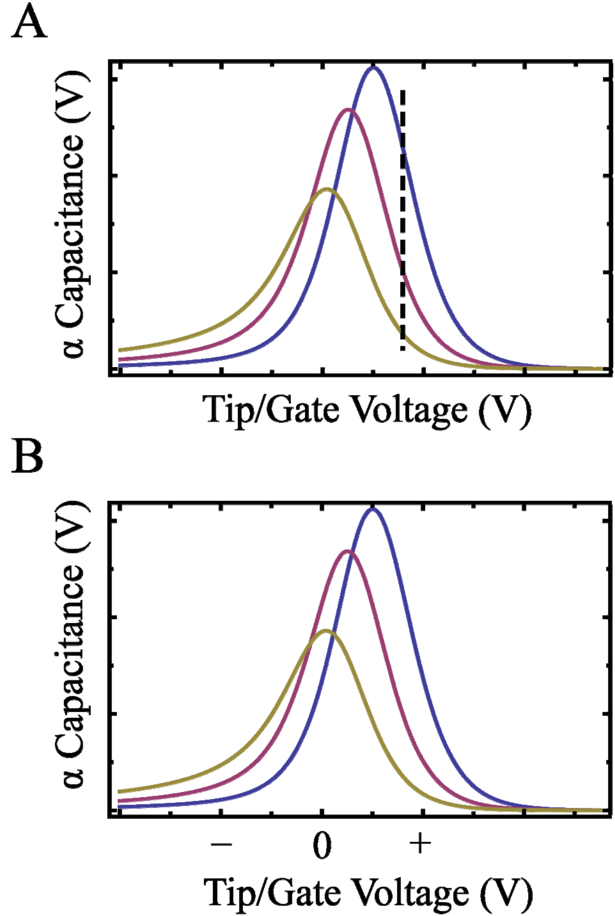

Figure 1.5. Schematic illustrating the difference between SCM and SCS with *dC/dV* curves of several *n*–type MIS structures with increasing doping from blue to violet to yellow. Dashed line in (a) represents SCM operation at a single dc bias showing different contrast levels for varying dopant concentrations while the entire *dC/dV* curve is obtained while the tip is in a fixed position during SCS in (b).

area to be scanned. The capacitance signal that is recorded as a function of position is then proportional to only one point of the *dC/dV* curve. Figure 1.5(a) attempts to convey what is happening in SCM by showing the *dC/dV* curves for several *n*–type MIS structures of increasing dopant density from blue to violet to yellow and a dashed line representing the dc quiescent point V_{dc}. At this quiescent point represented by the dotted line, different dopant concentrations would yield different contrast levels in the

SCM image. For instance, if the background doping in the structure were represented by the blue line and some portions of the structure had higher doping as represented by the violet line, at the dc voltage indicated by the dotted line, the regions with lower dopant concentration would appear brighter while the regions with higher dopant concentration would appear less bright. If the dc voltage is varied, then the level of contrast represented by each dopant concentration will change accordingly. If the tip is held in a fixed position, it is possible to ramp through the entire range of dc biases and record, for this fixed position only, the *dC/dV* spectrum as seen in Figure 1.5 (b). This mode of operation is known as scanning capacitance spectroscopy (SCS).

1.6 Scanning Kelvin Probe Microscopy

Scanning Kelvin probe microscopy (SKPM) is a method of measuring the contact potential difference between two materials derived from the method known as the dynamic capacitor suggested by Lord Kelvin in 1898.[27] The original method utilizes the notion that two mechanically oscillating plates of different work function will cause a charge to arise on the plates' surface and this capacitance varying with distance will give rise to a time varying voltage. By applying a dc voltage $V_{app} = -V_{CPD}$, where $eV_{CPD} = \phi_1 - \phi_2$ is the contact potential difference and ϕ_n is the work function of material *n*, the work function difference between the two materials is cancelled out and the voltage oscillation ceases. This situation can be applied directly to a metallic AFM probe tip and a metal or semiconductor sample by considering the general expression for the electrostatic force between the tip and the sample derived from the method of virtual work:[28]

$$F = -\frac{1}{2}V^2\frac{\partial C}{\partial z},$$

where C is the capacitance of the tip–sample system and $V = V_{app} + V_{CPD}$ is the overall potential difference between the tip and sample. By applying an oscillating voltage, $V_{app} = V_{dc} + V_{ac}\sin\omega t$, the total force on the probe tip can be written as the sum of three different frequency components: $F = F_{dc} + F_{\omega} + F_{2\omega}$, where

$$F_{dc} = -\frac{1}{2}\frac{\partial C}{\partial z}\left[\left(V_{CPD} + V_{dc}\right)^2 + \frac{1}{2}V_{ac}^2\right],$$

$$F_{\omega} = -\frac{\partial C}{\partial z}\left(V_{CPD} + V_{dc}\right)V_{ac}\sin\omega t,$$

and $$F_{2\omega} = \frac{1}{4}\frac{\partial C}{\partial z}V_{ac}^2\cos 2\omega t.$$

This means that an application of an ac bias with frequency ω to the conductive cantilever will excite mechanical resonances at ω and 2ω and a static deflection. The large, sharp resonance characteristic of the cantilever beam eliminates most resonances that are not at the natural frequency of the cantilever. Therefore, if the frequency of the ac bias, ω, is the same as the resonant frequency of the tip, then any 2ω resonances do not vibrate the cantilever with much amplitude. By changing the dc bias applied to the tip in such a way that $V_{dc} = -V_{CPD}$, the F_{ω} term will be minimized and the mechanical vibration at that frequency will cease.

The force between the probe tip and a semiconductor sample can be understood by considering the band diagrams in Figures 1.6(a)–(c). Figure 1.6(a) shows a metal tip and an n–type semiconductor which are not electrically connected.

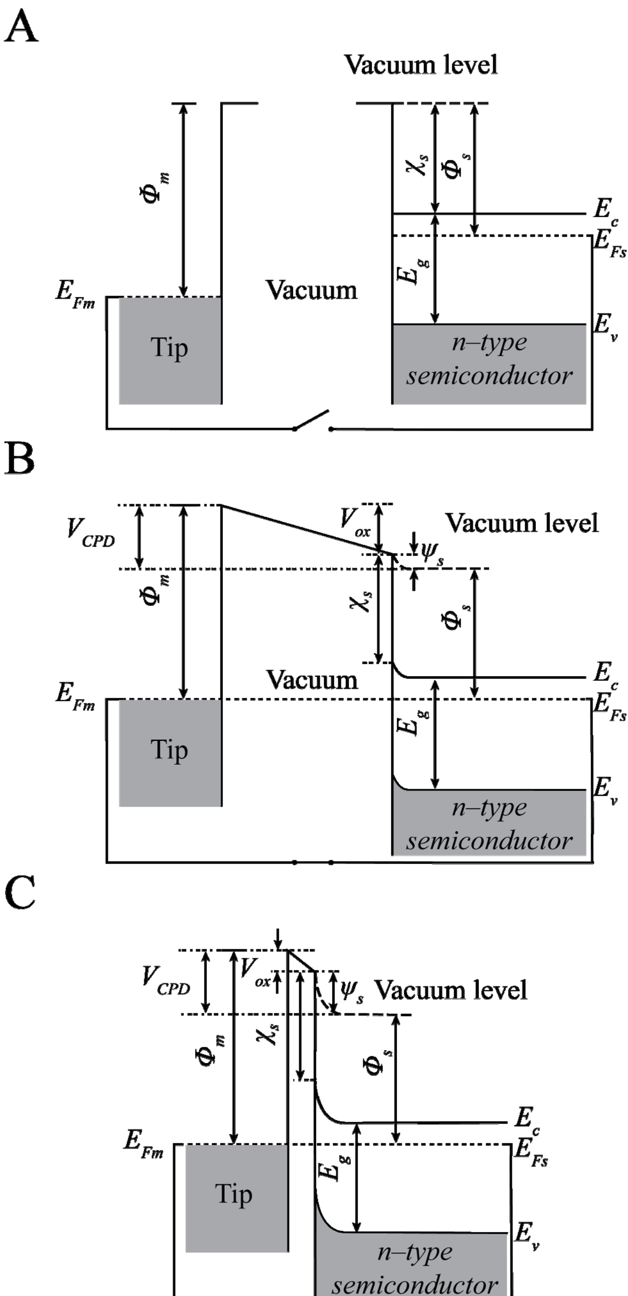

Figure 1.6. Illustration of the formation of a contact potential difference V_{CPD} between a metal and an *n*–type semiconductor. E_{Fm} is the Fermi level in the metal; E_{Fs} is the Fermi level in the semiconductor; Φ_m is the metal work function which is larger than Φs, the semiconductor work function; E_c is the conduction band; E_v is the valence band; E_g is the energy band gap; χ_s is the semiconductor electron affinity; V_{ox} is the voltage drop across the vacuum; and ψ_s is the surface potential of the semiconductor. (a) No electrical connection between the metal and semiconductor. Electrical contact between the metal and semiconductor spaced by (b) a larger distance and (c) a smaller distance.

In Figure 1.6(b), the two are separated by some distance but are electrically connected. Such a system is considered to be in thermal equilibrium which means that the electro–chemical potential, represented by the Fermi level in this case, must be constant across the entire system. Another way to think of this is to consider that the potential energy of an electron in each material must be the same; therefore, when they are electrically connected, electrons will flow from lower potential energy in the semiconductor (small work function Φ_m) to the higher potential energy of the metal (larger work function Φ_s) until the potential energy across the system is the same, i.e. an electric field arises between the two materials that opposes the further transfer of electrons. This electron transfer causes a voltage drop to occur between the two materials, V_{CPD}, which appears partially across the vacuum between the two materials and partially as a depletion region in the semiconductor, V_{ox} and ψ_s, respectively. This potential difference between the two materials means that there is a force between them. It is this force that causes the tip to mechanically oscillate when an ac voltage is applied between the tip and the sample. Figure 1.7 shows a schematic of the feedback mechanism for measuring work function differences using SKPM.

While the probe tip is raised above the sample surface, an ac bias is applied to the tip. Because of the work function difference between the probe and the sample, this ac voltage causes a mechanical oscillation. By applying a dc offset voltage to the tip through a feedback loop, the mechanical oscillations of the probe tip can be reduced until they cease, at which point $V_{app} = -V_{CPD}$. The computer records the applied dc voltage, V_{app}. In practice, this process is completed after the tip makes one

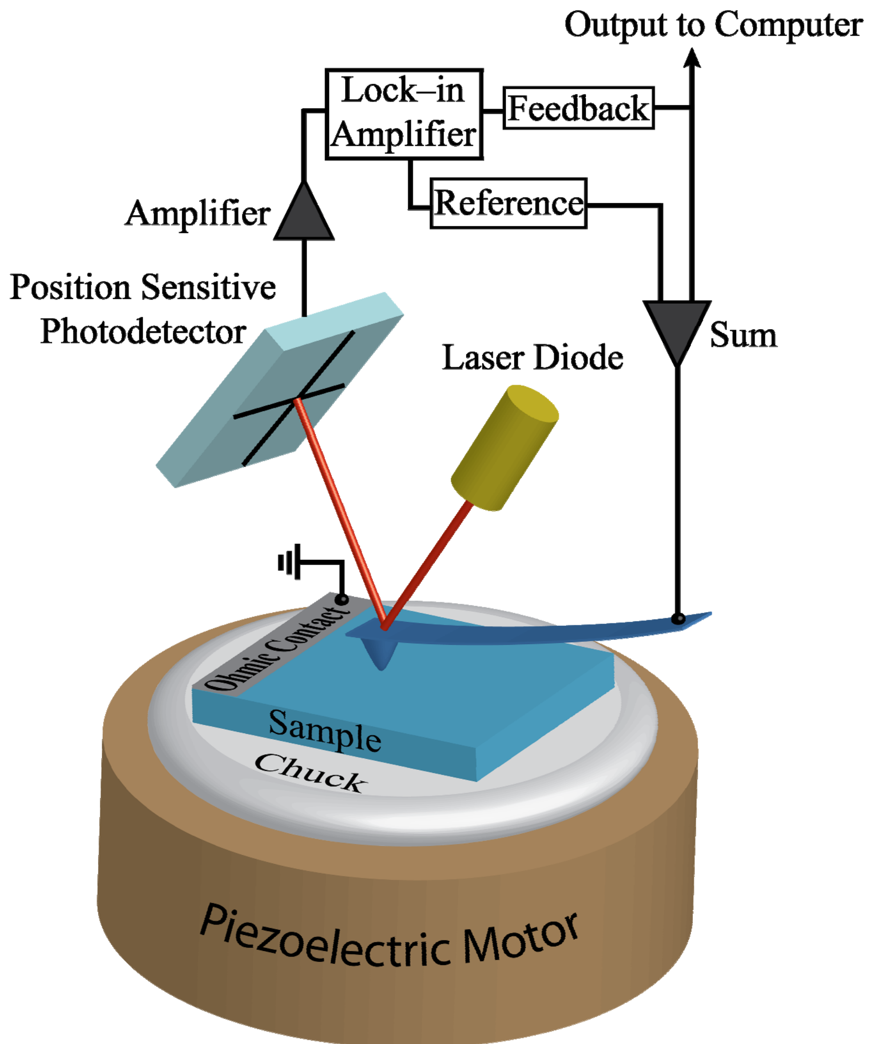

Figure 1.7. Schematic diagram of scanning Kelvin probe force microscopy. Ac and dc biases are applied to the probe tip while the amplitude of the mechanical deflection is monitored by the photodetector. The mechanical oscillation ceases when the feedback adjusts the applied dc bias such that it equals the contact potential difference between the probe tip and the sample.

topographic pass in tapping mode. In order to minimize the spurious effects of $\partial C/\partial z$, the tip is lifted a set amount (typically 5–50 nm), and the tip retraces the topographic line it just recorded. It is during this second pass that the surface potential difference is measured.

1.7 Dissertation Overview

Utilizing the scanning probe microscopy and spectroscopy analysis techniques, this dissertation examines the impacts and implications of local inhomogeneities in nanoscale electronic properties on two semiconductor material systems. The first portion concerns itself with the charge characteristics of partial dislocations in $\left(11\bar{2}0\right)$ gallium nitride grown by hydride vapor phase epitaxy and the conductive properties of dislocations in (0001) gallium nitride grown by high–temperature molecular beam epitaxy.

Group III–nitride semiconductor materials and devices are candidates for a broad range of device applications from blue to ultraviolet light–emitting diodes[29] and laser diodes[30] to high–power, high–speed electronic devices.[31] Dramatic progress has been made in improving the epitaxial material quality and device performance of nitride based devices; however, the persistent lack of readily available homoepitaxial substrates still necessitates growth on Al_2O_3 or SiC. The large lattice mismatch between GaN and Al_2O_3 or SiC causes material degradation predominately through the presence of high densities of threading dislocations, which ultimately lessen device performance through carrier scattering,[32] nonradiative recombination,[33] and increased reverse bias leakage.[34–36] Because the densities and types of defects, as well as their electrical behavior, can be highly dependent on growth conditions and technique, characterization of the electronic properties of defects in nitride films grown with varying techniques and in different orientations is likely to be essential to their successful application in devices.

In chapter two, we have used AFM and SCM to perform detailed studies of the electronic properties, specifically local, nanoscale charge distributions, in *n*–type GaN grown in the *a*–plane orientation with lateral epitaxial overgrowth (LEO) employed to reduce overall dislocation density. AFM and SCM imagings reveal the presence of a linear feature aligned along the $[\bar{1}100]$ direction, exhibiting bias–dependent SCM contrast arising from an elevated local concentration of positive charge. Defects of the same line direction have been observed using transmission electron microscopy and cathodoluminescence in LEO and non–LEO *a*–plane GaN[37, 38] and concluded to be the termination of basal plane stacking faults, suggesting a similar structural origin for the feature we observe. The observation of positive line defect charge is in contrast to the electrical behavior of dislocations observed in (0001) GaN thin films, in which threading dislocations propagating along the [0001] direction are typically either neutral or negatively charged.[36, 39, 40]

In chapter three, we have used AFM and CAFM to examine the effects of Ga/N flux ratio for growth at temperatures >750 ºC on the local conduction properties of (0001) GaN. Analysis of AFM and CAFM images showed that for samples grown at these elevated temperatures there exists a narrow band of fluxes near Ga /N ≈ 1 where no local reverse–bias leakage occurred at the detection limit of our instrument. Field–emission scanning electron microscopy and x–ray diffraction revealed consistent densities of open–core, screw–component threading dislocations across the range of Ga/N flux ratios. The observation of consistent densities of screw–component and open core threading dislocations and absence of local reverse–bias

leakage in MBE GaN are in stark contrast with previous studies (performed on material grown at lower temperatures) that suggested that the conductivity of dislocations was determined predominately by the dislocation type, with only pure screw dislocations exhibiting highly conductive behavior.[16, 41]

The fourth chapter of the dissertation is concerned with the impacts of large macroscopic electrical contacts to indium arsenide nanowires. Semiconductor nanowires offer promising capabilities for future high–performance electronic[42], optoelectronic[43], biomedical[44], and thermoelectric[45, 46] devices and platforms for basic investigations of electronic structure and carrier transport in low–dimensional systems. InAs nanowires, in particular, are a superb candidate for high speed, high density, ultra–low power circuits due to their narrow band gap (0.354 eV at 300 K)[47], high electron mobility–in excess of 33,000 cm^2/Vs in bulk material[48]–and surface Fermi–level pinning[49] in the conduction band, which allows for formation of ohmic contacts with relative ease. Because of the geometries often employed in nanowire–based devices, understanding the interaction and influence of nearby macro–scale objects, such as bulk contacts, on nanowire behavior is of paramount importance. Conventional macroscopic electrical characterization techniques yield only limited and/or indirect understanding of the interactions and influences of macro–scale and nano–scale objects, while scanning probe measurements of local electronic properties enable highly spatially accurate, non–destructive, and direct experimental characterization of these interactions.

In chapter four, we have used SCM and SCS in conjunction with finite–element numerical simulations, to examine the effects of micron–scale metal contacts typically present in nanowire–based electronic devices on carrier modulation and electrostatic behavior in semiconductor nanowires. Our results reveal a remarkably strong dependence of the capacitance spectra on the distance separating the probe tip and the metal contact, extending to distances of 3–4 μm and beyond. This dependence is revealed, by comparison of the SCM/SCS data with finite–element electrostatic simulations, to be a consequence of electrostatic screening of the tip–nanowire potential difference by the large metal contact. These results provide direct experimental verifications of contact screening effects such as those postulated for carbon nanotube (CNT) based devices.[50] The design and expected performance of nanowire–based electronic devices, most notably nanowire field–effect transistors (NWFET), may be strongly influenced by these screening effects, and they are indicative of the importance of mitigating the effects of large–scale contacts and circuit elements on the performance of nanoscale electronic devices.

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2 Characterization of Nanoscale Electronic Structure in Nonpolar Gallium Nitride Using Scanning Capacitance Microscopy

2.1 Introduction

Group III–nitride semiconductor materials and devices have emerged as outstanding candidates for a broad range of device applications, with particular success thus far in blue and ultraviolet light–emitting diodes,[1] laser diodes,[2] and high–speed electronic devices.[3] The spontaneous and piezoelectric polarization fields present in nitride heterostructures,[4] while typically being advantageous[5, 6] in electronic devices such as nitride–based field effect transistors, can detract from the performance of light emitters based on nitride quantum–well structures due to the built–in electric field created within the quantum well by the polarization–induced charges at the heterojunction interfaces. Specifically, the built–in electric field reduces electron–hole wave function overlap, lowers radiative recombination efficiency within the quantum well,[7] and shifts light emission to longer wavelengths relative to polarization–free heterostructures.[8, 9]

One possible method to address the performance degradation due to polarization fields entails the growth of nitride semiconductor heterostructure thin films in the so–called nonpolar orientations, e.g., on the $(10\overline{1}0)$ or $(11\overline{2}0)$ plane, referred to as the *m*–plane and *a*–plane, respectively, of the wurtzite crystal structure, rather than on the (0001) *c*–plane as is most typically done. Growth and luminescence studies have shown that $In_yGa_{1-y}N/GaN$ quantum–well structures are free of such

polarization–induced internal electric fields when grown in the *m*–plane[10] or *a*–plane[11, 12] orientation. However, the continuing need to perform growth of nitride semiconductors on lattice–mismatched substrates such as sapphire or SiC leads to the presence of high densities of threading dislocations and other linear or planar defects, many of which can exhibit prominent electrical activity.[13–18] Because the densities and types of such defects, as well as their electrical behavior, can be highly dependent on growth conditions and technique, characterization of the electronic properties of defects in nonpolar nitride films is likely to be essential to their successful application in devices.

We have used atomic force microscopy (AFM) and scanning capacitance microscopy (SCM) to perform detailed studies of the electronic properties, specifically local, nanoscale charge distributions, in *n*–type GaN grown in the *a*–plane orientation with lateral epitaxial overgrowth (LEO) employed to reduce overall dislocation density. AFM and SCM imagings reveal the presence of a linear feature aligned along the $[\bar{1}100]$ direction, exhibiting bias–dependent SCM contrast arising from an elevated local concentration of positive charge. Based on comparison of our SCM data and other experiments done on similar *a*–plane GaN, we hypothesize that this positive charge is possibly due to the presence of a series of dislocations, a single dislocation, or a partial dislocation at the edge of a stacking fault aligned along the $[\bar{1}100]$ direction near the sample surface. Defects of the same line direction have been observed using transmission electron microscopy (TEM) and cathodoluminescence (CL) in LEO and non–LEO *a*–plane GaN[19, 20] and concluded to

be the termination of basal plane stacking faults, suggesting a similar structural origin for the feature we observe. The observation of positive line defect charge is in contrast to the electrical behavior of dislocations observed in *c*–plane GaN thin films, in which threading dislocations propagating along the [0001] direction are typically either neutral or negatively charged.[15, 18, 21]

2.2 Crystal Structure of (Al, In, Ga)N

Group III–nitrides have three common crystal structures: the wurtzite (α–InN/GaN/AlN)[22], zincblende (β–InN/GaN/AlN)[23, 24], and rocksalt structures (rs–InN/GaN/AlN).[25, 26] The wurtzite structure, as seen in Figure 2.1, is the thermodynamically favorable structure of InN, GaN, and AlN in bulk form under ambient conditions. Typically the zincblende structure is epitaxially grown on $\{001\}$ crystal planes of cubic substrates such as Si,[27] MgO,[23, 24] and GaAs,[28] while the rocksalt structures is induced under very high pressures.[25, 26] The wurtzite structure is comprised of two interpenetrating hexagonal close packed sublattices (each with six atoms), and thus has two lattices constants, *c* and *a*. The two sublattices are offset along the *c* axis by 5/8 of the cell height *c*. Any crystal structure can be uniquely described by only three Miller indices; however, the hexagonal symmetry of the wurtzite crystal structure lends itself well to being described by four lattice vectors (Bravais–Miller index notation). This notation consists of three equivalent basal plane lattice vectors $\mathbf{a_1}$, $\mathbf{a_2}$, and $\mathbf{a_3}$, each rotated 120º with respect to one another; and a fourth vector, **c**, normal $\mathbf{a_1}$, $\mathbf{a_2}$, and $\mathbf{a_3}$. For the wurtzite structure, the stacking sequence of

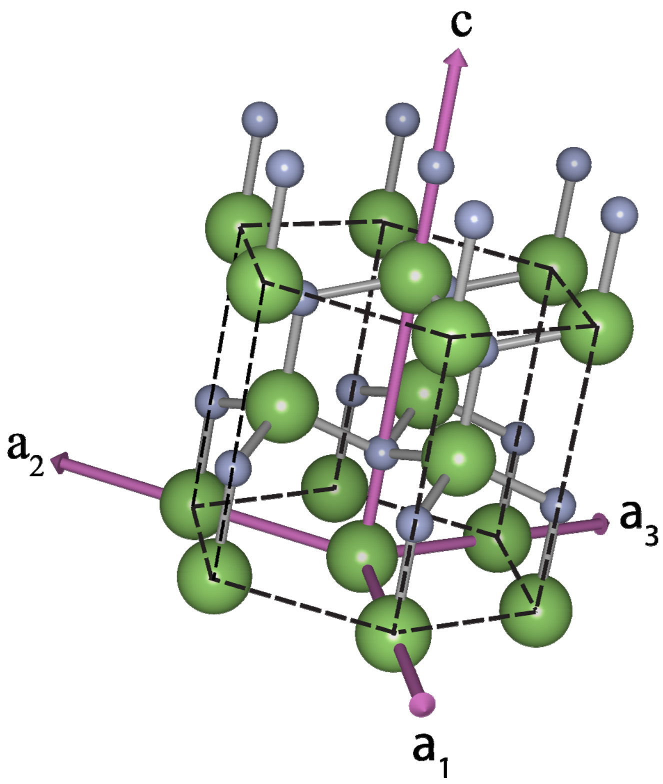

Figure 2.1. Wurtzite crystal structure with lattice vectors and unit cell (dashed black line) superimposed.

closest packed diatomic $\{0001\}$ planes is ABABAB in the $\langle 0001 \rangle$ direction. This is as opposed to the zincblende structure where the stacking sequence of the $\{111\}$ planes is ABCABC in the $\langle 111 \rangle$ direction. The wurtzite and zincblende structures differ only in the bond angle of the second–nearest neighbor because a 60º rotation of the second A plane in ABA will cause the stacking to become ABC. Figures 2.2(a)–(c) show three crystal planes that are of particular interest: (a) the $(1\bar{1}00)$ *m*–plane, (b) the $(11\bar{2}0)$ *a*–plane, and (c) the (0001) *c*–plane. One consequence of the two

interpenetrating hexagonal close–packed lattices, the electronegativity difference between gallium and nitrogen, and the inherent asymmetry in the wurtzite crystal structure is that (Al, Ga, In)N crystals spontaneously polarize along the *c*–axis. In addition to this spontaneous polarization, the wurtzite structure exhibits piezoelectric

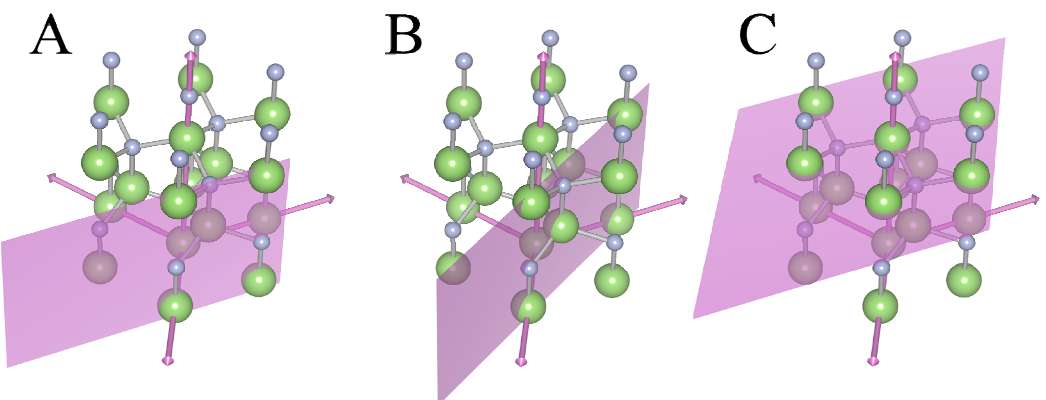

Figure 2.2. Wurtzite crystal structure with plane illustrating the (a) *m*–plane, (b) *a*–plane, and (c) *c*–plane

polarization in the *c*–axis direction when strained. The spontaneous and piezoelectric polarization charges have a profound impact on the electrical behavior of the III–N materials system.

2.3 Polarization Effects in (Al, In, Ga)N

Optical devices based on ternary alloys of the $In_yGa_{1-y}N$ material system can encompass the entire visible spectrum from infrared to ultraviolet due to the large range of direct band gaps available, from 0.7 eV for InN[29–32] to 3.42 eV for GaN.[33] Most of these devices are based on multiple–quantum–well structures. The relatively large lattice mismatch between InN and GaN, combined with the aforementioned piezoelectric effect of the wurtzite crystal structure, induces a great deal of

polarization charge, and thus, large electric fields at a heterojunction interface. Additionally, spontaneous polarization charges, more specifically the difference in spontaneous polarization charges between InN and GaN, play a lesser role in this

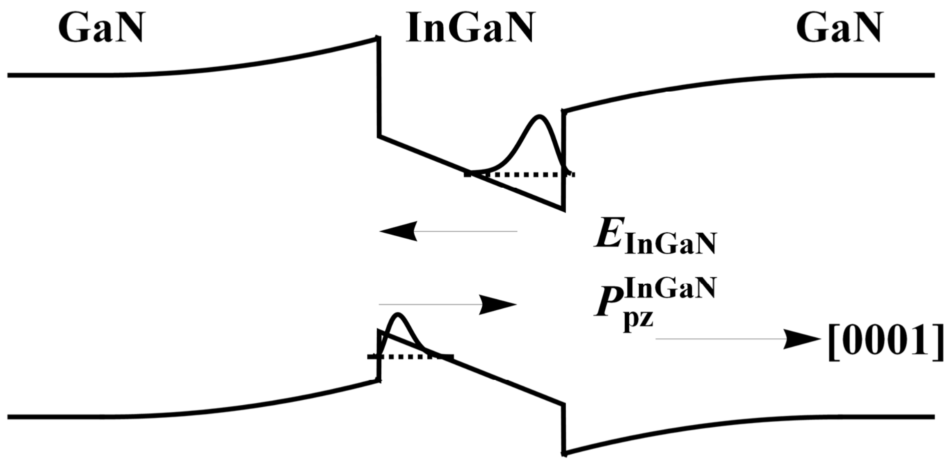

Figure 2.3. Band diagram of a GaN/InGaN/GaN quantum well illustrating the effect of spontaneous and piezoelectric polarization charges on the band structure at the heterojunction interfaces and the corresponding reduction of electron and hole wavefunction overlap.

process. This effect can be beneficial in some electronic devices,[5, 6] but in the case of optoelectronic devices, they are detrimental.[7–9] The quantum–confined Stark effect (QCSE)[34] is one manifestation of the polarization charge in the nitride materials system. Any heterostructure formed with a component in the $\langle 0001 \rangle$ direction will have its electronic band structure distorted by the presence of the spontaneous and piezoelectric polarization charges that accumulate at the interfaces between dissimilar materials. These charges create large electric fields at the heterojunction interface which reduce the spatial overlap of electron and hole wave functions, as in Figure 2.3.[35] The radiative recombination lifetime in these structures increases due to the

reduced overlap of electron and hole wave functions, which increases the chance of nonradiative recombination and decreases light emission efficiency.[7] These same polarization charges also shift light emission to longer wavelengths.[8,9]

2.4 Nonpolar Gallium Nitride

As the polar axis of the wurtzite structure is along the $[0001]$ direction, any direction that lies perpendicular to this direction will not have polarization effects. This means that structures grown perpendicular to the $[0001]$ direction will have polarization vectors that lie within the plane rather than normal to the plane, relieving the heterostructure interfaces of any deleterious polarization–charge induced effects and, potentially, making optoelectronic devices grown in these directions more efficient. The lowest index family of nonpolar directions are the $\langle 1\bar{1}00\rangle$ *m*–directions and the $\langle 11\bar{2}0\rangle$ *a*–directions. The planes that lie along these directions are the $\{1\bar{1}00\}$ *m*–planes and $\{11\bar{2}0\}$ *a*–planes, which are shown in Figure 2.2(a) and Figure 2.2(b), respectively. These nonpolar planes contain equal numbers of group III and group V elements. Samples with surface quality comparable to that of *c*–plane GaN films were grown in 2000 when Waltereit *et al.* reported molecular beam epitaxy (MBE) growth of *m*–GaN on (100) $LiAlO_2$ and the elimination of polarization fields in their heterostructures.[35] The *m*–plane samples showed promising optical qualities with emission energies blue shifted by 100 meV and radiative lifetimes shortened by one to two orders of magnitude as compared to traditional *c*–plane structures. In 2002, H. M.

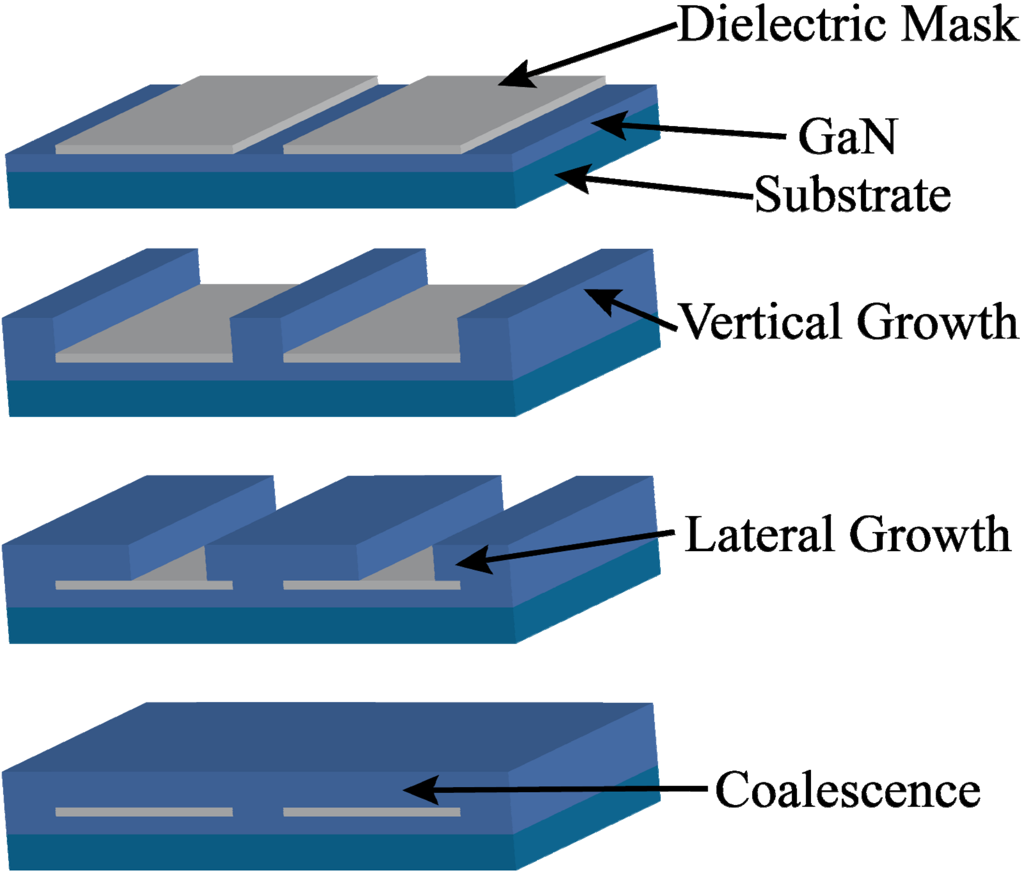

Figure 2.4. Schematic illustration of the LEO growth process. The process begins by patterning an amorphous dielectric layer on a growth substrate followed by vertical growth in the window regions, lateral overgrowth over the dielectric mask, and coalescence of the film to form a continuous layer.

Ng reported on the first MBE growth of *a*–plane GaN quantum wells on *r*–plane sapphire, which exhibited stronger intensity and blue shifted emission when compared to similar *c*–plane structures.[36]

2.5 Lateral Epitaxial Overgrowth

The lack of homoepitaxial substrates for growth results in a high density of dislocations being induced in epitaxial films of GaN. Threading dislocations in *c*–plane GaN have been found to act as nonradiative recombination centers, scattering

centers, reverse bias leakage paths, etc.,[13–18] which limits device speed, reliability, and efficiency. The reduction of dislocation densities in GaN–based devices is critical to improving device performance, reliability, and power consumption.[37] Significant defect reduction can be achieved in GaN growth by employing lateral epitaxial overgrowth (LEO) techniques. LEO has been demonstrated to reduce extended dislocation densities and improve device properties in *c*–plane GaN grown by metal organic chemical vapor deposition (MOCVD)[38–41] and hydride vapor phase epitaxy (HVPE).[42–44] Threading dislocations in GaN typically originate at the interface between the growth substrate and the initial layers of thin film growth and propagate vertically. By encouraging lateral growth, LEO leverages this tendency for dislocations to propagate vertically to yield laterally grown material containing substantially lower concentrations of dislocations than the initial, vertically grown material.

There are several techniques to encourage lateral growth; the most common is to lithographically pattern a growth substrate (this substrate could be sapphire, SiC, or even GaN grown on top of another substrate) with an amorphous dielectric material upon which GaN will not grow epitaxially. The dielectric material choice is critical, for if the growth is to occur preferentially in the window regions, it must be energetically unfavorable for GaN to grow on the dielectric mask. The general LEO process is illustrated in Figure 2.4. Once the dielectric mask is in place, GaN growth proceeds vertically through the window regions only and subsequently spreads laterally over the mask regions ultimately converging with other lateral growth to form

a continuous film. As the overgrown region shares no crystallographic orientation with the amorphous dielectric mask and since dislocations prefer to propagate vertically, the overgrown regions should be relatively free of defects.[45] The mask shape, orientation, size, and period can all have consequences on the resulting film.[46]

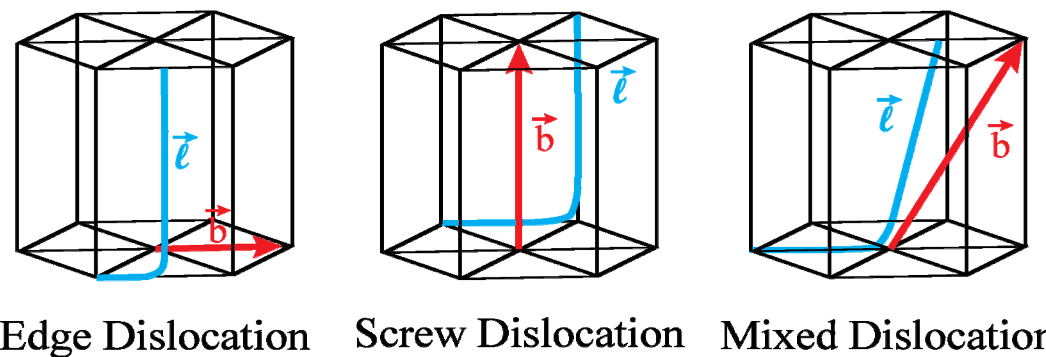

Figure 2.5. Schematic illustration of the Burgers and line vectors for edge, screw, and mixed dislocations in GaN.

2.6 Electronic Properties of Dislocations in Gallium Nitride

As threading dislocations are so prominent in III–N materials and often exhibit pronounced electrical behavior, it is crucial to understand and characterize the electrical properties of these defects. Figure 2.5 shows the three type of threading dislocations: edge dislocations with Burgers vector $\vec{b} = \frac{1}{3}\langle 11\bar{2}0 \rangle$ and line direction $\vec{\ell} = \langle 0001 \rangle$, screw dislocations with Burgers vector $\vec{b} = \frac{1}{2}\langle 0001 \rangle$ and line direction $\vec{\ell} = \langle 0001 \rangle$, and mixed dislocations with Burgers vector $\vec{b} = \frac{1}{3}\langle 11\bar{2}3 \rangle$ and inclined line direction. Depending on the growth method used (MBE, MOCVD, or HVPE) and the substrate, (sapphire, SiC, etc.) dislocations can show various electronic properties. The surface termination of these defects is nanoscale pits.[47] These topographic

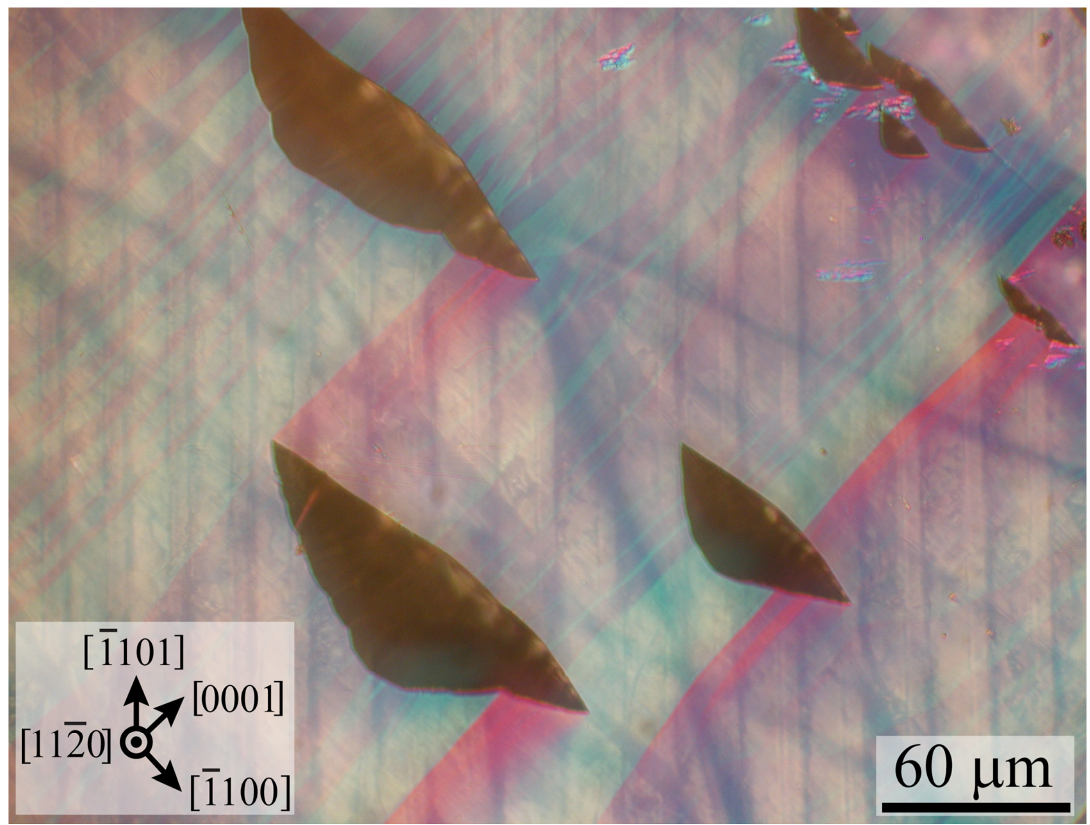

Figure 2.6. Two Nomarski optical contrast micrographs of the same area superimposed to demonstrate the correlation between window/stripe orientation and inverted pyramids.

features have been correlated with negative charge using scanning Kelvin probe microscopy (SKPM) on AlGaN/GaN heterostructures grown by MBE[48] and GaN grown by MOCVD[49] and MBE.[50] SCM has also been used to image negative dislocation charge on MOCVD–grown GaN on sapphire[15] and AlGaN/GaN heterostructures on SiC.[21] Pure screw dislocations which exhibit no surface termination have been shown to be a source of localized current leakage.[16,18] Dislocations have been shown by CL and TEM to be nonradiative recombination centers in GaN,[14] while charged dislocations have been shown to be responsible for carrier scattering in *n*–type GaN films.[13] All of these investigations were on material

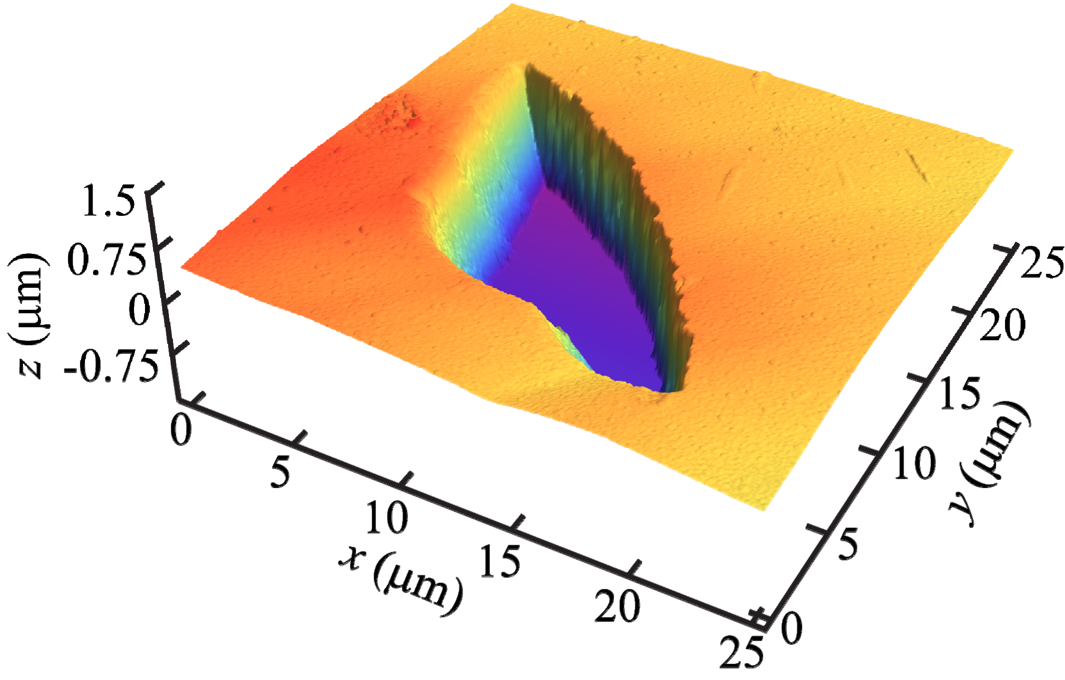

Figure 2.7. AFM topography of *a*–plane GaN showing different sidewall angles of inverted pyramids.

or structures grown in the *c*–axis direction, but the electronic properties of defects in GaN and related alloys grown in nonpolar directions are, as yet, unexamined.

2.7 Scanned Probe Experiment

The samples characterized in this dissertation were grown by HVPE, with LEO employed to improve surface morphology and reduce defect density.[45] A 120 nm thick SiO_2 layer was deposited on an *r*–plane sapphire substrate and then patterned with an array of stripe openings 5 μm in width with a 20μm period. The stripes were aligned along the $[\bar{1}101]$ direction, 43.2° from the *m*–axis, which corresponds to the $[\bar{1}100]$ direction. A 105 μm thick GaN film was then grown through the windows in

the mask layer. The sapphire substrate was removed through an in situ spontaneous film separation process. The resulting free–standing GaN film was unintentionally doped *n*–type with a carrier concentration in the high 10^{17} cm^{-3} range.

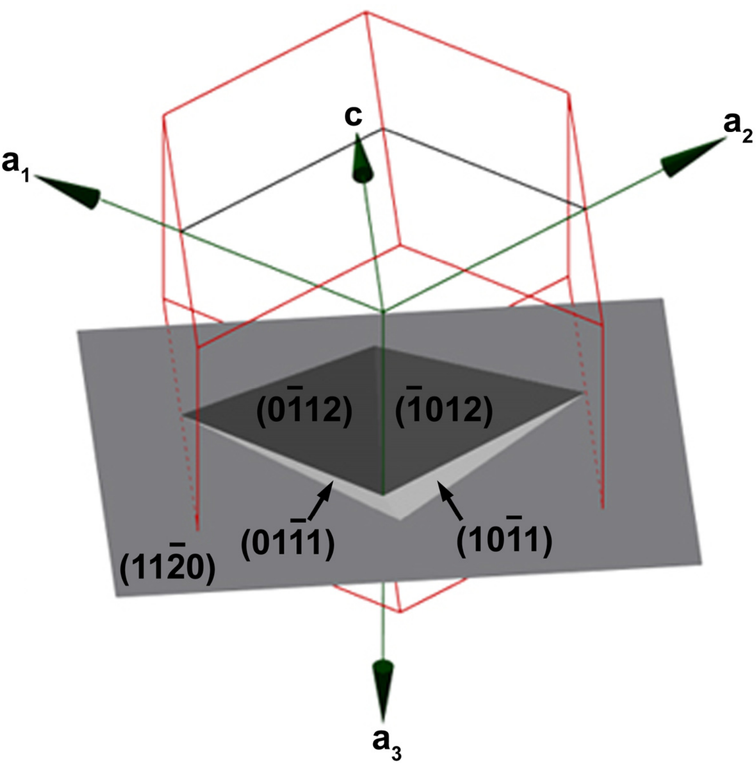

Figure 2.8. Schematic illustrating the crystallographic facets of the inverted pyramid pits visible in Figure2.6 and Figure 2.7 [Ref. 20].

The surface morphology of the sample was smooth except for the inclined sidewalls of inverted pyramids shown in Figure 2.6 and Figure 2.7. Figure 2.6 shows two Nomarksi optical contrast micrographs of the same area superimposed. Clearly visible in Figure 2.6 are both the stripes and the large inverted pyramids. This image demonstrates the correlation between the orientation of the stripe regions and the inverted pyramids. Figure 2.7 shows an AFM image of a smaller inverted pyramid

where the differently inclined facets of the pyramids are clearly delineated. Figure 2.8 shows the crystallographic Bravais–Miller indices of each of the inclined facets of the inverted pyramid.[20] These features in conjunction with the stripes can be used to determine the crystallographic orientation of other morphological features.

Figures 2.9(a) and 2.9(b) show AFM topographs of the window and wing region of the *a*–plane GaN film, respectively.[20] The surface roughness of both the window and the wing regions is excellent with RMS roughness less than 1 nm for a $5 \times 5\ \mu m^2$ area. Also evident in Figure 2.9(a) is nanometer–scale surface pitting with density of $\sim 1.3 \times 10^9\ cm^{-2}$, which is not apparent in Figure 2.9(b). These pits are the terminations of edge dislocations on the surface.[20] The faint lines in both images oriented in the $\left[\bar{1}100\right]$ direction are associated with the basal plane stacking faults observed in TEM. Basal plane stacking faults are present in equal concentrations in the window and wing regions. TEM data show the density of stacking faults to be approximately $3 \times 10^5\ cm^{-2}$. The termination of these basal plane stacking faults is a partial dislocation. Though not visible in Figure 2.7, the faint lines seen in Figure 2.9 are visible at higher magnifications on the flat surface near the edges of the inverted pyramid.

For fabrication of ohmic contacts, samples were rinsed and then sonicated in trichloroethylene, methanol, acetone, and isopropanol for one minute each. Then the samples were cleaned in oxygen plasma for five minutes. Ohmic contacts were then formed using 330 Å Ti/770 Å Al/330 Å Ti/880 Å Au metallization deposited by electron–beam evaporation and annealed at 400 °C for five minutes and then at 650 °C

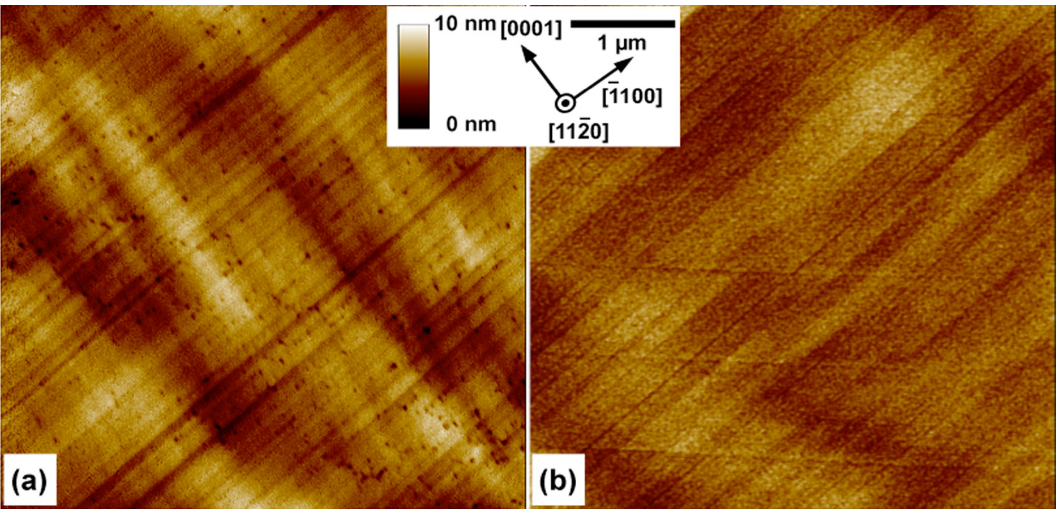

Figure 2.9. Atomic force micrograph of (a) a window region and (b) a wing region of the *a*–plane GaN film [Ref. 20].

for three minutes in an H_2/N_2 forming gas ambient. Prior to scanning probe characterization, samples were again cleaned using the procedure described above. AFM and SCM data were obtained using a Digital Instruments (Veeco) Nanoscope IIIa Dimension 3100 microscope with Pt/Ir–coated probe tips with a nominal radius of 25 nm at the tip apex. For the SCM measurements, a bias voltage consisting of a dc component with a small (~2 V) ac modulation, typically at a frequency of 20–95 kHz, was applied to the sample with the probe tip grounded. As discussed in detail elsewhere,[51–53] the SCM signal detection mechanism yields a voltage signal that is proportional, in our measurements, to dC/dV, where C is the tip–sample capacitance and V is the dc component of the applied bias voltage. Typical ambient conditions for these measurements were ~20 °C and ~50 % relative humidity. Figure 2.10 shows a schematic diagram of the sample and probe tip geometry employed in these measurements.

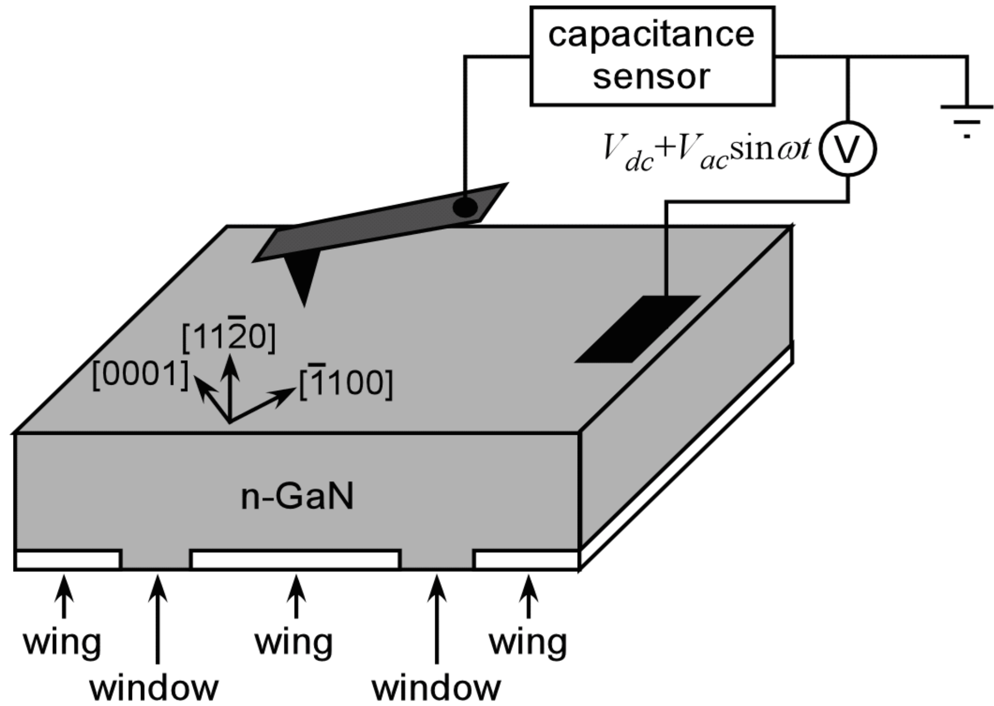

Figure 2.10. Schematic diagram of sample structure, scanning probe measurement geometry, and voltage biasing arrangement.

2.8 Results

Figure 2.11(a) shows a montage of AFM topographs of the sample near the border between a window region (the upper left portion of the montage) and an adjacent wing region (lower right). The crystal axis directions shown in Figure 2.11(a) were determined by analysis of several large, distinctive pyramidal depressions observable in large–area surface micrographs and topographs (shown in Figure 2.6 and Figure 2.7, whose facets were formed by $(0\bar{1}12)$, $(\bar{1}012)$, $(01\bar{1}1)$, and $(10\bar{1}1)$ crystal planes.[20] The angle between the flat film surface and the crystal facets of the inverted pyramids were calculated by fitting planes to each of the

pyramid facets and the surface. Once the planes in the AFM topographs were determined to correspond to the known planes in Figure 2.7, it was clear that the faint lines seen in Figure 2.11(a) were the same as those seen in Figures 2.9(a) and 2.9(b). Thus, we were able to duduce the crystallographic orientations noted in Figure 2.11(a). For ease of interpretation in terms of the analogous behavior of a conventional metal–insulator–semiconductor structure, for which it is typical to specify the voltage applied to the metal contact relative to the semiconductor, we will specify the potential of the probe tip relative to the sample in discussion and analysis of the SCM image data. Figures 2.11(b)–(f) show the SCM images of the area, or portions thereof, corresponding to the topographic image in Figure 2.11(a), obtained at dc bias voltages of +4 V to –4 V applied to the tip relative to the grounded sample.

At a tip dc bias voltage V_{tip} = +4 V, we expect that an electron accumulation layer is formed at the surface so that any subsurface electronic structure is not imaged, as is evident from the absence of contrast in Figure 2.11(b). As V_{tip} is decreased, the electron accumulation layer is gradually depleted and the tip–sample capacitance decreases. The resulting increase in dC/dV_{tip} increases the SCM signal level and enables inhomogeneities in charge distribution within the surface depletion layer to be imaged. For V_{tip} = +2 V, we see in Figure 2.11(c) that a linear region with decreased SCM signal, corresponding to a smaller value of dC/dV_{tip} relative to the surrounding areas, becomes visible. This feature is more prominent in Figure 2.11(d), obtained at a bias voltage V_{tip} = 0 V. We also see in Figure 2.11(d) that the region of decreased SCM signal either terminates or moves to a depth greater than that which the SCM

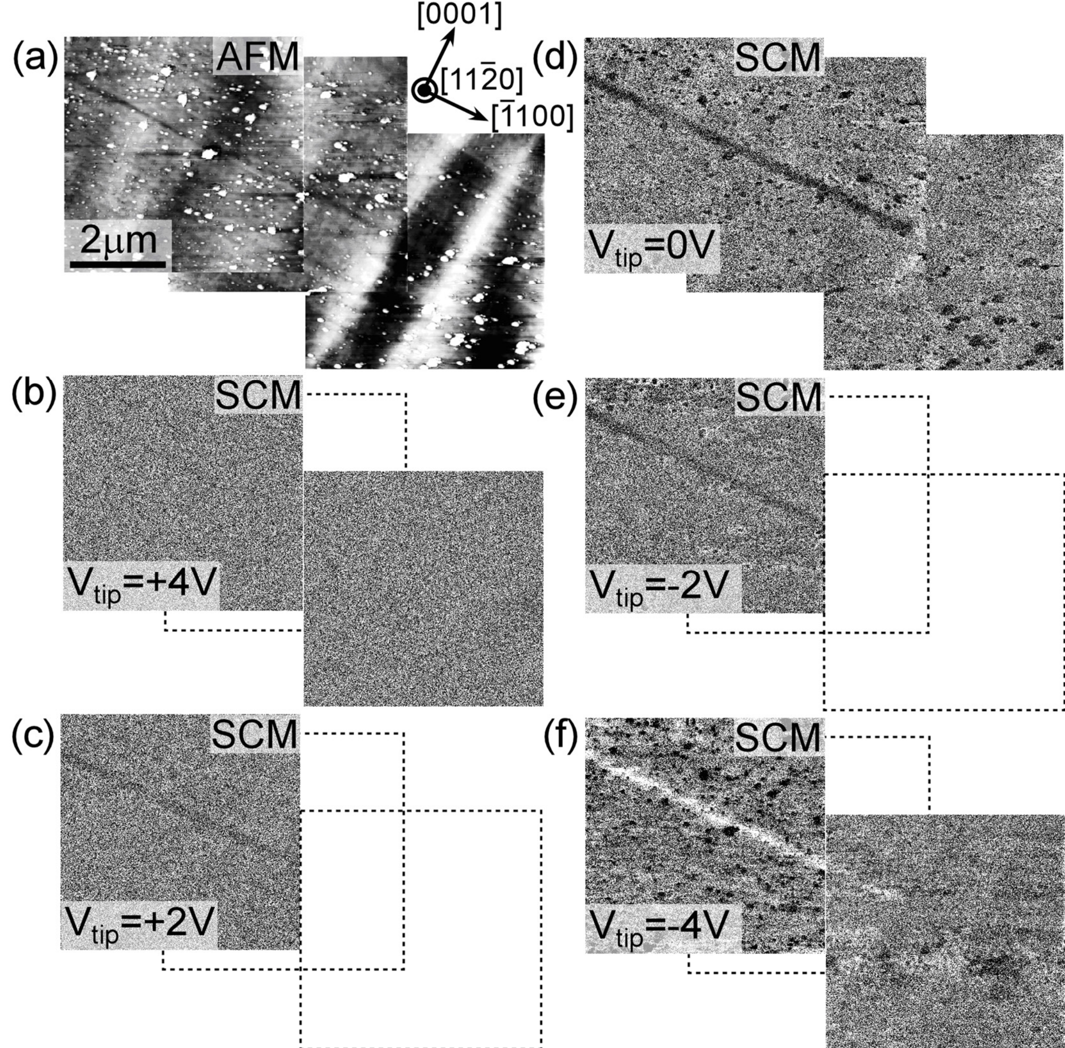

Figure 2.11. (a) AFM topograph and (b)–(f) SCM images obtained at tip dc bias voltages of +4V, +2V, 0V, –2V, and –4V. Dashed lines indicate areas in the topographic montage of (a) for which SCM data are not shown.

measurement is capable of probing, toward the lower right portion of the image area. Based on the observation by electron microscopy that defects in these samples can terminate after propagating a short distance into the wing region on a free surface such as a coalescence front or a pit sidewall and the relatively uniform contrast observed by SCM along the length of the feature prior to its disappearance, we believe that

termination of the feature is more likely than propagation to an increased depth to be responsible for its disappearance from the SCM image. Figure 2.11(e) shows the SCM image obtained with V_{tip} = –2 V, at which the region of decreased SCM signal is still evident, but less prominent than for V_{tip} = 0 V. Finally, we see in Figure 2.11(f) that for V_{tip} = –4 V, the SCM image contrast is inverted, i.e., the region that exhibited a lower SCM signal level at more positive values of V_{tip} yields a higher SCM signal at V_{tip} = –4 V.

The presence of SCM image contrast only for $V_{tip} \leq +2$ V, combined with the smooth evolution and inversion of contrast as V_{tip} is decreased, indicates that the features observed correspond to actual electronic structure within the sample rather than being topographically induced artifacts. The AFM topograph shown in Figure 2.11(a) does contain an area that is alternately depressed (upper–left portion of the image) and elevated (lower–right portion of the image) topographically compared to the surrounding region and that corresponds in location to the electronic feature imaged by SCM, suggesting a structural origin to the electronic feature.

2.9 Discussion

The electrical properties giving rise to the SCM contrast observed in Figure 2.11 can be determined by an analysis of the bias dependence of the SCM signal. Using the simple model of the tip–sample interface as a conventional, one–dimensional metal–insulator–semiconductor structure, we can compute the capacitance per unit area C as a function of tip voltage in the accumulation and depletion regimes and differentiate to obtain dC/dV_{tip}.[54] The presence of trapped

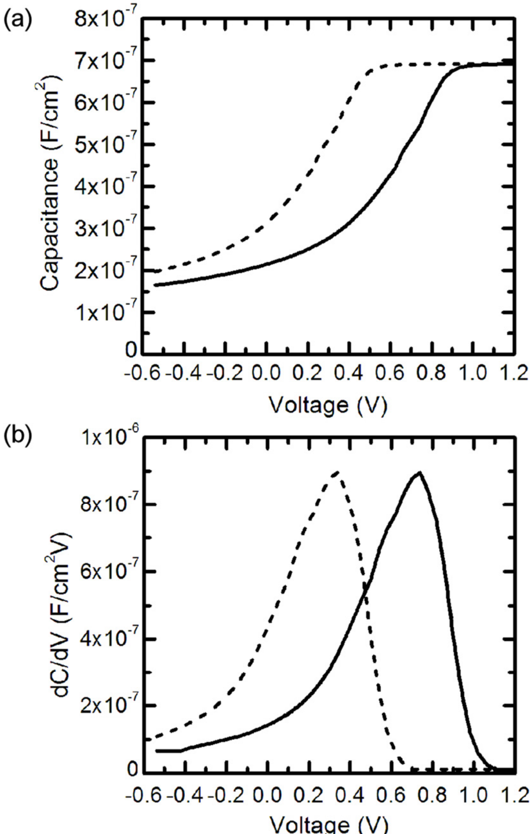

Figure 2.12. (a) Capacitance per unit area C and (b) dC/dV_{tip} computed using a one–dimensional model for the metal tip, an electrically insulating layer between the tip and sample surface, and n–type GaN (solid lines), and the same structure with a positive sheet charge present immediately below the GaN surface (dashed lines).

charge in such a structure, and its effect on C and dC/dV_{tip}, can then be analyzed in the usual manner to determine the origin of the observed SCM contrast in terms of electrical charge present along the observed feature. In the actual SCM experiment, the maxima in dC/dV_{tip} will be shifted in voltage and the width of the associated peak will be increased compared to their calculated values due to the effects of finite tip size on carrier modulation within the sample[55] and the possible presence of surface or interface charges between the probe tip and sample.

Figures 2.12(a) and 2.12(b) show capacitance per unit area and dC/dV_{tip} for an n–GaN metal–insulator–semiconductor structure, computed in our model as a function of bias voltage applied to the metal, assuming a dopant concentration of 5×10^{17} cm^{-3}, an ideal metal–semiconductor barrier height of 0.8 eV, and the presence of an insulating layer separating the tip and GaN surface 5 nm in thickness with dielectric constant $3.9\varepsilon_0$. Also shown are capacitance and dC/dV_{tip} for the same structure in the presence of an additional positive charge density $\Delta Q = 4\times10^{12}$ electron cm^{-2} just below the GaN surface, which shifts the voltage at which accumulation occurs by an amount $\Delta V \approx -\Delta Q/C_i$, where C_i is the capacitance per unit area of the insulating layer. This model is not, due to its extreme simplicity, expected to provide a quantitative description of the contrast observed in the SCM images shown in Figure 2.11. It is, however, adequate to explain qualitatively the bias–dependent contrast observed in terms of additional charge density associated with the near–surface line defect present in the images.

Specifically, we see from Figure 2.12(b) that a spatially localized shift in dC/dV_{tip}, i.e., the SCM signal level, induced by the presence of additional positive charge near the GaN sample surface, is expected to leave SCM signal contrast at large positive voltages unaffected, while yielding a depressed SCM signal level near the localized positive charge at lower voltages, with an eventual transition to elevated SCM signal levels near the localized positive charge as the voltage is further reduced. This is precisely the evolution in SCM contrast that is observed in the vicinity of the line defect imaged in Figure 2.11, indicating the presence of positive charge in or near

the core of the defect. An analogous evolution of SCM signal contrast with bias voltage has been employed in earlier studies to identify the presence of negative charge associated with threading dislocations in *n*–type GaN and $Al_yGa_{1-y}N$/GaN heterostructures grown in the *c*–plane (0001) orientation.[15,18,21]

In contrast to conventional thin film growth, the LEO growth procedure results in much more inhomogeneous spatial distributions of dislocations. Characterization by transmission electron microscopy (TEM) reveals very low dislocation densities, approximately 10^6 cm^{-2}, near the surface of the "wing" regions of the sample, while in the "window" regions the dislocation density typically exceeds 10^9 cm^{-2}. For *a*–plane LEO GaN films grown using $\left[1\bar{1}01\right]$–oriented stripes, dislocations typically emerge from the window regions and propagate at sharply inclined angles below the surface,[20] resulting in a very low dislocation density within the surface depletion layer–the region accessible for characterization of electronic structure by SCM. For the dopant concentrations present in the samples studied, the surface depletion layer under equilibrium conditions is expected to be 30–40 nm in thickness. However, TEM has also shown that stacking fault densities are comparable in wing and window regions.[20]

Figure 2.13 shows SEM and CL images of a sample grown in an identical manner to that employed in the present study, but with a 5 μm stripe opening and a 40 μm period to provide for increased lateral growth. These images reveal the presence of line–like regions of nonradiative recombination of which the projection onto the surface is along the $[\bar{1}100]$ direction. TEM analysis revealed that these features are the edges of basal plane stacking faults which terminate on partial edge

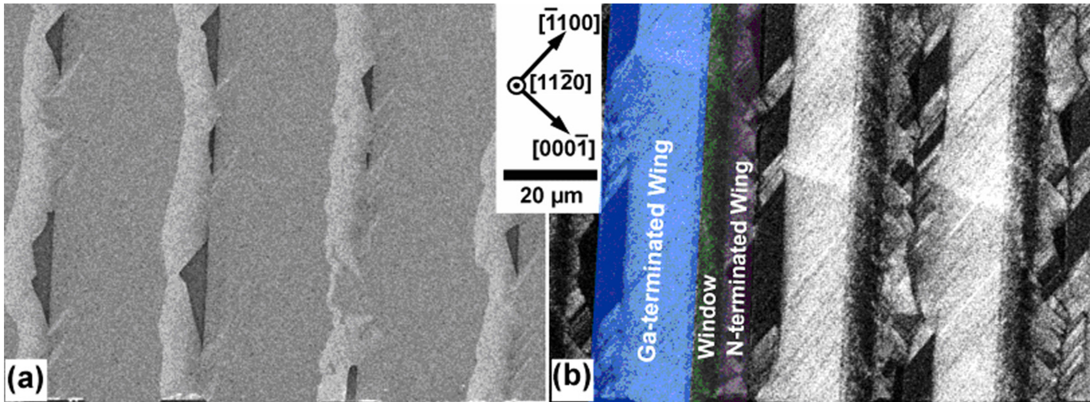

Figure 2.13. (a) Scanning electron micrograph and (b) polychromatic cathodoluminescence image of nonpolar LEO GaN sample revealing defects that act at nonradiative recombination centers aligned in the $[\bar{1}100]$ direction [Ref.20].

dislocations.[19,20] The AFM image of Figure 2.11(a) reveals the presence of an array of linear topographic features aligned along the $[\bar{1}100]$ direction with density comparable to that of the linear features observed by CL in Figure 2.13. With regard to the SCM contrast shown in Figure 2.11, it should be noted that both CL and TEM have a significantly larger penetration depth: several to tens of microns[56] and up to several hundred nanometers depending on sample thickness, respectively. In contrast, SCM is sensitive to features within the surface depletion layer—approximately 30–40 nm thick in this case. Thus, the apparent density of such features in an SCM image is expected, and found, to be much lower than in CL or TEM.

Given the one–dimensional nature of the feature we observed, its orientation along the same direction as that of the lines of nonradiative recombination observed by CL, and the prevalence of defects expected to be present within the surface depletion layer of the sample, we attribute the electronic structure we observe in Figure 2.11 to the presence of a partial dislocation at the edge of a stacking fault. Comparing the CL

and SCM findings, we note that in all cases the observed structure has the same line direction and similar dimensionality. Thus, it is likely that the defect observed SCM is a partial dislocation at the edge of a basal plane stacking fault.

The observation of a positively charged feature is striking in that prior studies of the electronic structure of threading dislocations in GaN grown in the *c*–plane orientation have revealed that those dislocations, typically propagating along the [0001] direction, are either negatively charged or electrically neutral, with the former behavior being associated with the presence of deep acceptor states within the dislocation core.[57, 58] The defect structure we observe in these studies may therefore be of a type not previously characterized, but perhaps present in significant concentrations in GaN grown by LEO in nonpolar orientations.

2.10 Future Work

A great deal is still unknown about III–N materials grown in nonpolar orientations. Additionally, many scanned probe characterization techniques have not been fully leveraged to investigate these materials. In this study we were able to characterize a partial dislocation at the edge of a stacking fault using SCM; however, in the window regions of these materials there are high densities of threading dislocations of which the surface termination are nanoscale pits. As the results in this study demonstrated unexpected positive fixed charge, it would be beneficial to do a correlated SCM, SKPM, and CAFM study of the window and wing regions of both *a*– and *m*–plane LEO GaN to distinguish what the electronic properties of line defects are in these orientations and with this growth technique.

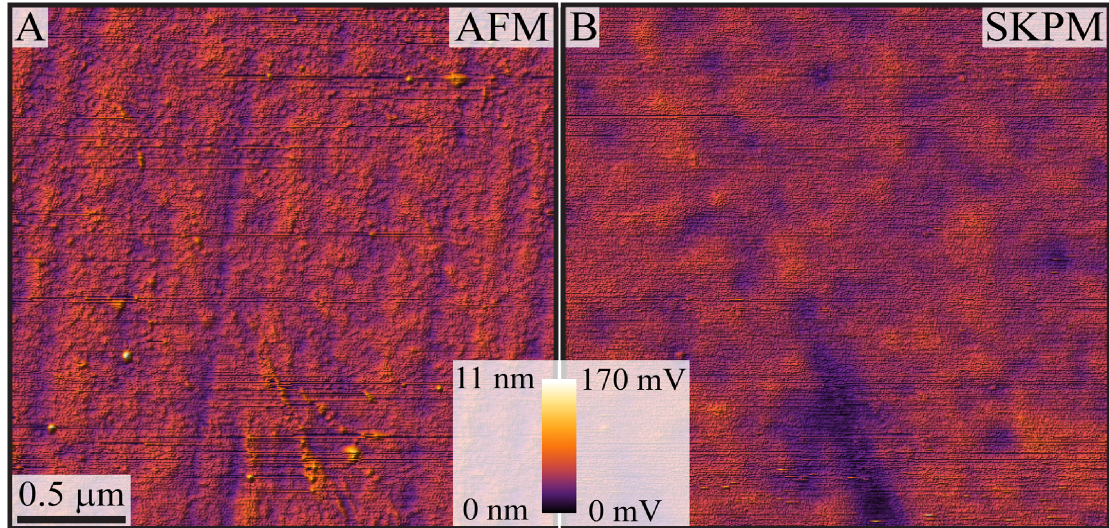

Figure 2.14. (a) AFM topograph and (b) SKPM image of *a*–plane GaN showing regions of negative fixed charge on the sample surface.

Figures 2.14(a) and 2.14(b) show an AFM topograph and an SKPM voltage map of the surface of *a*–plane GaN, respectively. Striations in topography are clearly visible in Figure 2.14(a), but also present are small pits or depressions. A fraction of these depressions correspond to regions of depressed voltage in Figure 2.14(b). In our measurement technique, lower contrast corresponds to increased surface potential. The depressions imaged in the surface potential image could then be indicative of negative fixed charge. If this were the case, it could be that these pits and surface potential depressions are the termination of threading edge dislocations. This signifies that dislocations in *a*–plane GaN may, unlike partial dislocations, have similar electronic behavior as their counterparts in (0001) GaN.[48, 49] Further extensive study is needed to confirm and understand all the electronic structure associated with defects in GaN grown in nonpolar orientations.

2.11 Conclusion

In summary, we have used scanning capacitance microscopy to characterize local nanoscale electronic structure in free–standing, *a*–plane, *n*–type GaN grown by hydride vapor phase epitaxy with lateral epitaxial overgrowth employed to reduce defect density. A linear feature containing positive charge is observed propagating from a window region into the adjacent wing region along the $[\bar{1}100]$ direction. This feature is present within the surface depletion layer in the sample, estimated to be approximately 30–40 nm in thickness, and appears to either terminate or move below the surface depletion layer within a few microns of the window edge. Cathodoluminescence data indicate that substantial concentrations of linear defects acting as nonradiative recombination centers are present in samples grown in this manner and that these defects propagate along the $[\bar{1}100]$ direction. Transmission electron microscopy data show that the linear defects observable in cathodoluminescence are the terminations of basal plane stacking faults. On the basis of these observations and related studies of *a*–plane GaN, we interpret the electronic feature observed by SCM as being associated with a partial dislocation at the edge of a stacking fault. The observation of a positively charged linear defect in this material is significant in two respects. First, it represents the first characterization of electronic structure associated with line defects in nonpolar GaN. Second, the observation of positive charge associated with the defect is quite striking, as linear defects such as threading dislocations in *c*–plane *n*–GaN are nearly universally observed to be either electrically neutral or negatively charged.

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3 Low Dislocation–Mediated Reverse–Bias Leakage in (0001) Gallium Nitride via High–Temperature Molecular Beam Epitaxy Growth

3.1 Introduction

Group III–nitride semiconductor materials and devices are candidates for a broad range of device applications from blue to ultraviolet light–emitting diodes[1] and laser diodes[2] to high–power, high–speed electronic devices.[3] Dramatic progress has been made in improving the epitaxial material quality and device performance of nitride based devices; however, the persistent lack of readily available homoepitaxial substrates still necessitates growth on Al_2O_3 or SiC. The large lattice mismatch between GaN and Al_2O_3 or SiC causes material degradation predominately through the presence of high densities of threading dislocations, which ultimately lessen device performance through carrier scattering,[4] nonradiative recombination,[5] and increased reverse bias leakage.[6–8] Disproportionate reverse–bias leakage current in *n*–type Schottky contacts to GaN grown by molecular beam epitaxy (MBE)—thought to be primarily due to conduction associated with high concentrations of screw component threading dislocations—is a conspicuously unsolved and acute problem for nitride based electronic devices. Traditionally, growth of GaN by MBE has occurred at low temperatures and under Ga–rich conditions to maintain good surface/interface morphology, which is in contrast to N–rich growth which minimizes reverse–bias leakage but leads to poor surface/interface morphologies.[9] Recent progress has been

made in MBE growth of (0001) GaN under N–rich conditions at temperatures above the thermal decomposition regime (> 750 ºC).[10] These conditions yielded 2D layer–by–layer growth, low surface roughness (<1 nm RMS roughness), and high electron mobilities (in excess of 1100 cm^2/V s for light doping at 300 K).[11] The local electronic properties of GaN grown under these conditions remain largely unexplored.

We have used atomic force microscopy (AFM) and conductive atomic force microscopy (CAFM) to examine the effects of Ga/N flux ratio for growth at temperatures >750 ºC on the local conduction properties of (0001) GaN. Analysis of AFM and CAFM images showed that for samples grown at these elevated temperatures there exists a narrow band of fluxes near Ga /N ≈ 1 where no local reverse–bias leakage occurred at the detection limit of our instrument. Field–emission scanning electron microscopy (FE–SEM) and x–ray diffraction (XRD) revealed consistent densities of open–core, screw–component threading dislocations across the range of Ga/N flux ratios. The observation of consistent densities of mixed and open core screw dislocations and the absence of local reverse–bias leakage in MBE GaN are in stark contrast with previous studies (performed on material grown at lower temperatures) that suggested that the conductivity of dislocations was determined predominately by the dislocation type, with only pure screw dislocations exhibiting highly conductive behavior.[9,12]

3.2 Crystal Structure of (Al, In, Ga)N

Group III–nitrides have three common crystal structures: the wurtzite (α–InN/GaN/AlN)[13], zincblende (β–InN/GaN/AlN)[14,15], and rocksalt structures (rs–

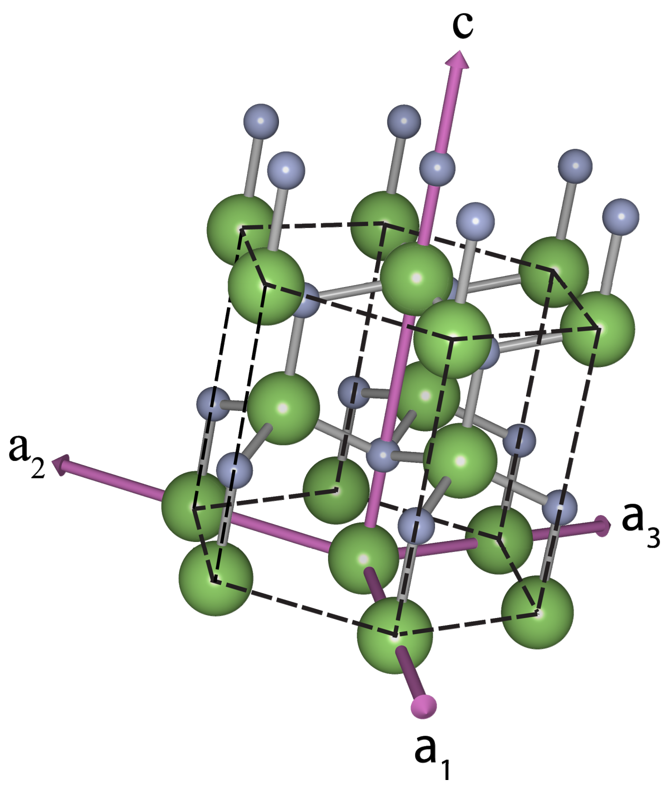


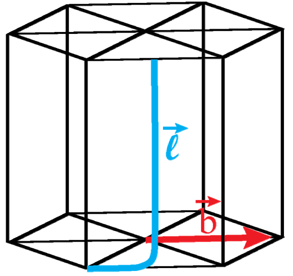
Figure 3.1. Wurtzite crystal structure with lattice vectors and unit cell (dashed black line) superimposed.

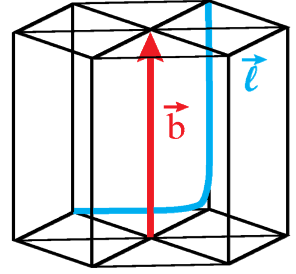
InN/GaN/AlN).[16,17] The wurtzite structure, as seen in Figure 3.1, is the thermodynamically favorable structure of InN, GaN, and AlN in bulk form under ambient conditions. Typically the zincblende structure can be epitaxially grown on $\{001\}$ crystal planes of cubic substrates such as Si,[18] MgO,[14,15] and GaAs,[19] while the rocksalt structures can be induced under very high pressures.[16,17] The wurtzite structure is comprised of two interpenetrating hexagonal close packed sublattices (each with six atoms), and thus has two lattices constants, c and a. The two sublattices are offset along the c axis by 5/8 of the cell height c. Any crystal structure can be

uniquely described by only three Miller indices; however, the hexagonal symmetry of the wurtzite crystal structure lends itself well to being described by four lattice vectors (Bravais–Miller index notation). This notation consists of three equivalent basal plane lattice vectors $\mathbf{a_1}$, $\mathbf{a_2}$, and $\mathbf{a_3}$, each rotated 120º with respect to one another; and a fourth vector, **c**, normal $\mathbf{a_1}$, $\mathbf{a_2}$, and $\mathbf{a_3}$. For the wurtzite structure, the stacking sequence of closest packed diatomic $\{0001\}$ planes is ABABAB in the $\langle 0001 \rangle$ direction. This is as opposed to the zincblende structure where the stacking sequence of the $\{111\}$ planes is ABCABC in the $\langle 111 \rangle$ direction. The wurtzite and zincblende structures differ only in the bond angle of the second–nearest neighbor because a 60º rotation of the second A plane in ABA will cause the stacking to become ABC. One consequence of the two interpenetrating hexagonal close–packed lattices, the electronegativity difference between gallium and nitrogen, and the inherent asymmetry in the wurtzite crystal structure is that (Al, Ga, In)N crystals spontaneously polarize along the *c*–axis. In addition to this spontaneous polarization, the wurtzite structure exhibits piezoelectric polarization in the *c*–axis direction when strained. The spontaneous and piezoelectric polarization charges have a profound impact on the electrical behavior of the III–N materials system. For a brief description, please see Section 2.3 of this dissertation.

3.3 Dislocations in (Al, In, Ga)N

A comprehensive review of all aspects of dislocations in the III–nitride materials system is beyond the scope of this dissertation, but a brief introduction with





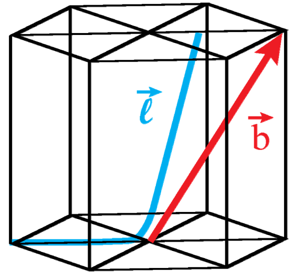


Figure 3.2. Schematic illustration of the Burgers and line vectors for edge, screw, and mixed dislocations in GaN.

points relevant to this document follows. Figure 3.2 breaks down threading dislocations into three different types: edge dislocations with Burgers vector $\vec{b} = \frac{1}{3}\langle 11\bar{2}0 \rangle$ and line direction $\vec{\ell} = \langle 0001 \rangle$, screw dislocations with Burgers vector $\vec{b} = \frac{1}{2}\langle 0001 \rangle$ and line direction $\vec{\ell} = \langle 0001 \rangle$, and mixed dislocations with Burgers vector $\vec{b} = \frac{1}{3}\langle 11\bar{2}3 \rangle$ and inclined line direction. Threading edge component dislocations are the dominant species of dislocation in the III–nitride materials system, often occurring at densities as high as 10^8–10^{11} cm^{-2} in hexagonal GaN grown by metal–organic chemical vapor deposition (MOCVD) on (0001) sapphire. These defects directly relieve the strain associated with the large lattice mismatch between GaN and the growth substrate and are thought to arise from the collisions of islands during growth.[20] Figure 3.3(a) shows a top view (along [0001]) of a theoretical model of the relaxed core threading edge dislocation.[21] Unlike edge dislocations, screw dislocations account for a small fraction of the total dislocation density. Since their

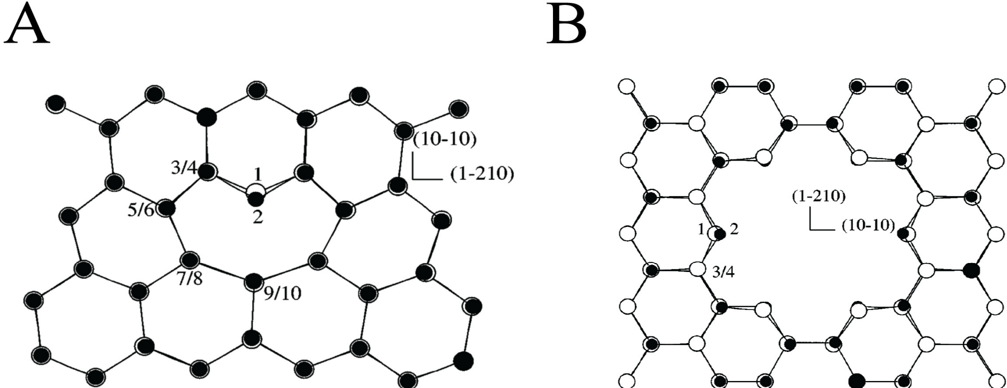


Figure 3.3. (a) Top view (along [0001]) of a theoretical model of the relaxed core of the threading edge dislocation and (b) top view (along [0001]) of a theoretical model of the relaxed core of the open–core screw dislocation [Ref.21].

Burgers vector is not in the plane of the growth direction, they do not directly relieve the strain associated with lattice mismatch, but instead they are thought to nucleate at the early stages of growth and to relieve twist misorientation between growth islands.[22] Screw dislocations with both open[23] and full[24] cores exist. Figure 3.3(b) shows a top view of a theoretical model of the relaxed core of the open–core screw dislocation.[21] Finally, mixed component threading dislocations share similarities between both of the aforementioned threading pure–screw and pure–edge dislocations. Threading dislocations of all types have varied surface terminations. The size of the surface depressions that form at the dislocation termination on the surface depends on the growth technique and the Burgers vector of the dislocation.[25] For MOCVD GaN films, small depressions were found at pure edge dislocations, and large depressions were found at mixed dislocations. The situation for MBE seems to depend mostly on the growth conditions, but pitting can be observed for MBE grown GaN as well. In

general, the physical manifestation of dislocations seems to depend heavily on the type of defect, the growth technique, and the growth conditions used.

3.4 Electronic Properties of Dislocations in (Al, In, Ga)N

As threading dislocations are so prominent in III–N materials and often exhibit pronounced electrical behavior, it is crucial to understand and characterize the electrical properties of these defects. Depending on the growth method used (MBE, MOCVD, or hydride vapor phase epitaxy (HVPE)) and the substrate, dislocations can show varied electronic properties. The surface termination of some of these defects can manifest as small surface pits.[26] These topographic features have been correlated with negative charge using scanning Kelvin probe microscopy (SKPM) on AlGaN/GaN heterostructures grown by MBE[27] and GaN grown by MOCVD[28] and MBE.[29] Scanning capacitance microscopy (SCM) has also been used to image negative dislocation charge on MOCVD–grown GaN on sapphire[30] and AlGaN/GaN heterostructures on SiC.[31] Pure screw dislocations which often exhibit no surface termination have been shown to be a source of localized current leakage.[12, 29] Figure 3.4 shows work demonstrating the existence of localized reverse bias leakage paths in the form of a topographic AFM (a), CAFM (b), and an overlay of topography and current maps (c) of GaN grown under Ga–rich conditions by MBE on top of an HVPE grown GaN template layer. The overlayed image in Figure 3.4(c) shows that the leakage paths, as seen as black dots, seem to correspond to the tops of mounds or peaks in the topography. Dislocations have been shown by CL and TEM to be

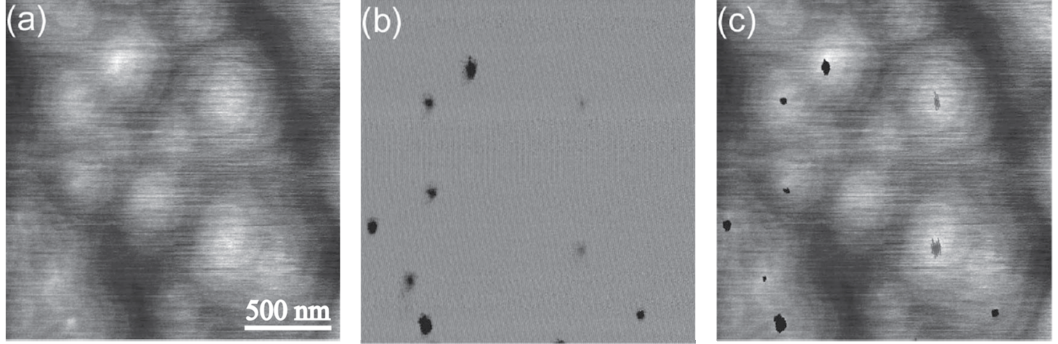


Figure 3.4. 2 µm × 2 µm (a) topographic images of Ga–rich MBE GaN on HVPE GaN template. (b) CAFM images with –6 V reverse bias. (c) Overlay of (a) and (b) showing regions of nonzero current [dark spots in (b)]. Vertical grayscales are 3 nm in (a) and 2 $\times 10^{-11}$ A in (b) [Ref. 12].

nonradiative recombination centers in GaN,[5] while charged dislocations have been shown to be responsible for carrier scattering in *n*–type GaN films.[4]

3.5 Epitaxy of (Al, In, Ga)N

The most commonly used methods to grow nitride semiconductor materials and devices are HVPE, MOCVD, and MBE. MBE can provide very precise control of growth parameters, in–situ monitoring techniques, and low background impurity concentrations. MBE is capable of producing excellent electronic devices with two–dimensional electron gas (2DEG) mobilities in excess of 160,000 $cm^2\ V^{-1}\ s^{-1}$ at 4.2 K for AlGaN/GaN heterostructures on GaN templates.[32] Native substrates are not readily available for growth of nitride materials, which necessitates growth on lattice mismatched substrates such as sapphire and SiC. Non–native substrates are partially a result of the low solubility of N in Ga and the high vapor pressure of N on GaN, which ultimately require high temperatures and high pressures to overcome. Sapphire, due to its lower cost, is the preferred substrate for growth of GaN and related materials. The calculated lattice mismatch between the basal plane of sapphire and the basal plane of

GaN is larger than 30 %, but the actual mismatch is smaller (~ 16 %) because the small cell of Al atoms on the basal sapphire plane is oriented 30º away from the larger sapphire unit cell.[33] The large strains involved in growing GaN on a sapphire substrate necessitate the formation of strain relieving defects such as threading dislocations. The effects on material quality of this lattice mismatch depend heavily on the growth method in question. The penalty for MBE growth is more onerous than other techniques with dislocation densities as high as $10^8 - 10^{10}$ cm^{-2} and increased electrical activity associated with these dislocations.[6, 34] Numerous techniques exist to mitigate higher defect densities such as the growth of an AlN buffer layer, but a more successful technique involves GaN growth by MBE on top of a preexisting GaN layer grown by either MOCVD or HVPE. While this technique may lower defect densities in MBE–grown GaN, it does not mitigate the added electrical activity associated with MBE–grown GaN.

Unlike MBE growth of traditional As, P, and Sb based compound semiconductors, MBE growth of III–N semiconductors yields the best surface, structural, and electrical properties under group III–rich conditions. In the case of GaN, this means that Ga rich growth yields the best material to date.[35, 36] Ga–rich growth conditions provide a Ga wetting layer (adlayer) on the surface[37, 38] which yields a two dimensional growth mode[39] and increased surface adatom diffusion[40, 41] with the ultimate result being smoother surface morphologies.[36, 42, 43] N–rich growth typically yields poor crystal quality with heavily pitted surfaces and a tilted columnar structure with a high density of stacking faults.[44] Electron mobilities reach peak

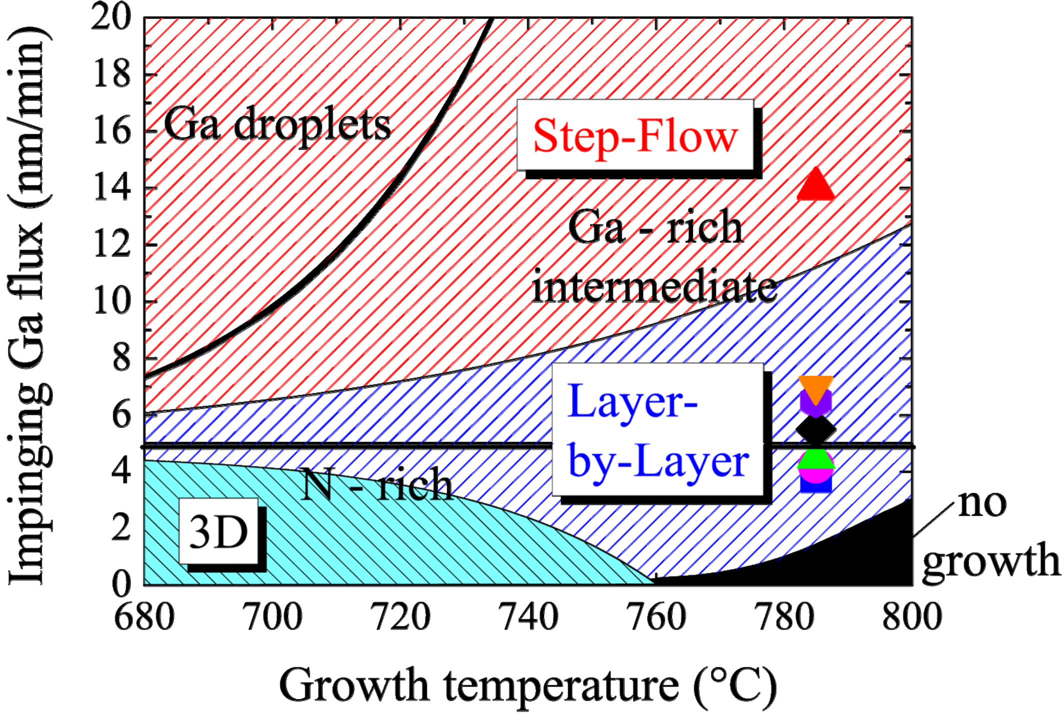


Figure 3.5. (0001) GaN growth diagram describing the dependence of Ga flux and growth temperature on the growth regime (N–rich vs. Ga–rich) and growth mode (3D vs. 2D layer–by–layer growth). Colored shapes indicate the growth conditions used in these experiments.

values under Ga–rich conditions near the limit for Ga droplet formation.[42] Typically, bilayer Ga coverage produces the best results with increasing coverage resulting in Ga droplets accumulating and degrading the device performance.[36, 38, 42, 43] Precise control of the growth conditions in the Ga–rich regime below the Ga droplet formation boundary is the standard practice for achieving high–quality GaN. To circumvent the rigors imposed by precise control of the Ga adlayer coverage growth can be done at temperatures above thermal decomposition (>750 ºC).[10, 45, 46]

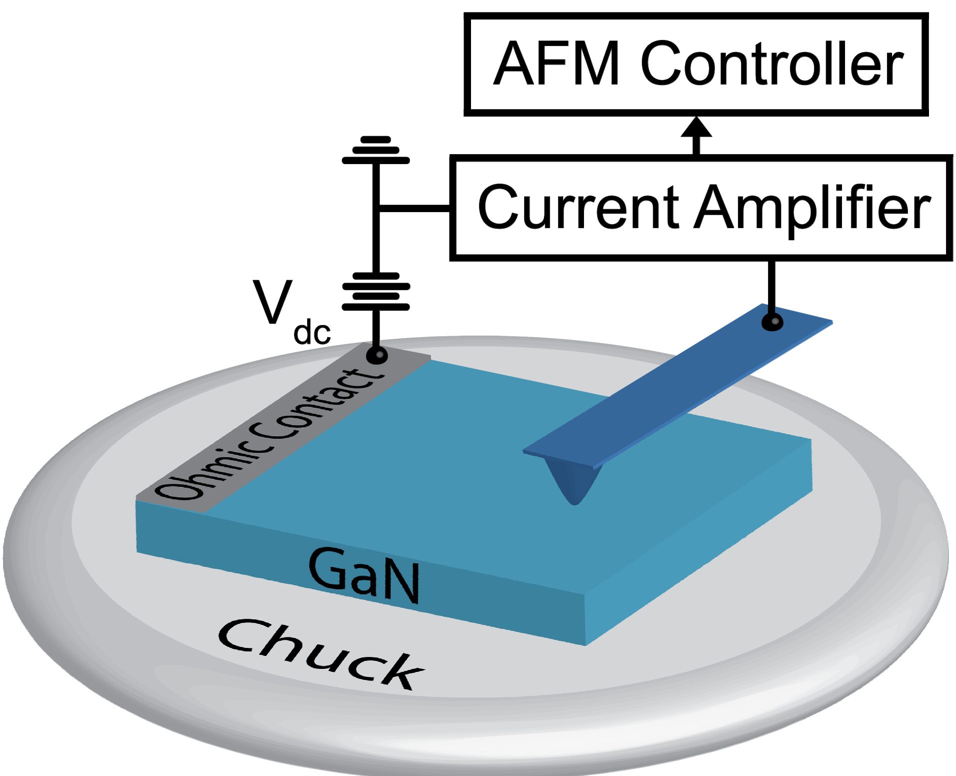


Figure 3.6. Schematic diagram of scanning probe measurement geometry and voltage biasing arrangement used in CAFM measurements.

3.6. Experiment

In this study, plasma–assisted MBE was used to grow 0.6–0.8 μm of Si–doped (low to mid 10^{16} cm^{-3}) (0001) GaN homoepitaxial layers. The growth substrates were in all cases semi–insulating GaN templates grown by metal–organic chemical vapor deposition on sapphire commercially available from Lumilog with total dislocation densities of approximately 5×10^{8} cm^{-2}. Figure 3.5 shows a growth mode map and colored shapes indicating the growth conditions for the samples in this study. All GaN layers were grown between 780 ºC and 790 ºC at constant nitrogen flux of 5.0 nm/min

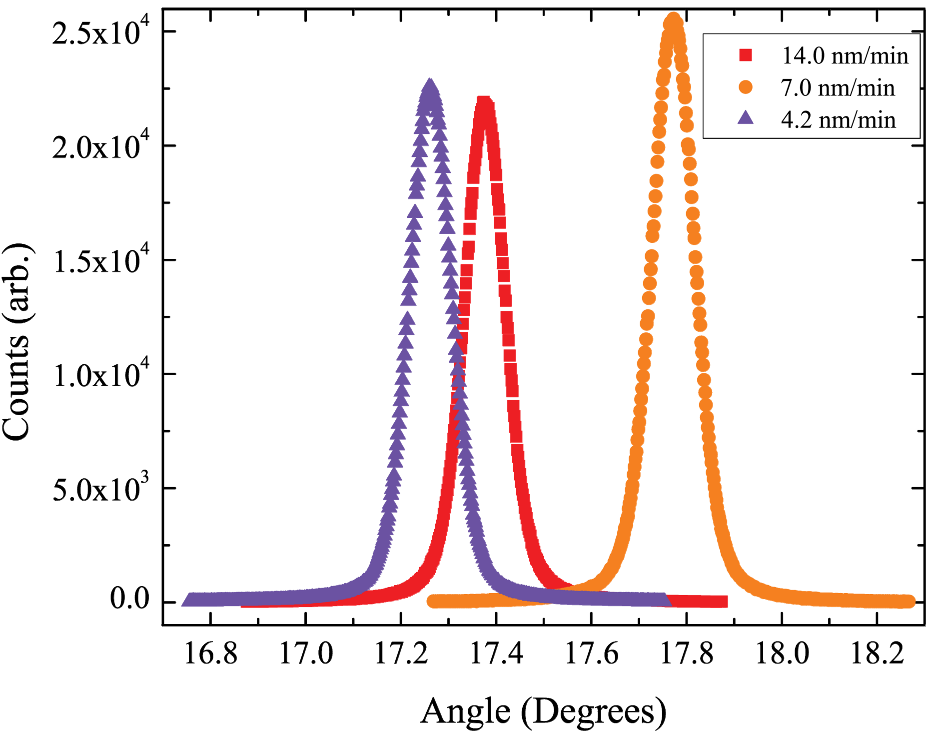


Figure 3.7. XRD data for samples grown at 14 nm/min (red squares), 7.0 nm/min (orange circles), and 4.2 nm/min (violet triangles) showing shifted peaks but similar full–width at half maximum for all growth conditions.

with gallium fluxes of 3.8 (blue square), 4.2 (pink circle), 4.5 (green upward pointing triangle), 5.5 (black diamond), 6.5 (violet hexagon), 7.0 (orange downward pointing triangle), and 14.0 nm/min (red upward pointing triangle). Details of the growth procedures and conditions have been described elsewhere.[10, 11] All samples having Ga flux larger than 5 nm/min were grown as one continuous layer with constant Si doping (low–to–mid 10^{16} cm^{-3}) on top of the MOCVD–GaN templates. The samples grown at Ga fluxes of 3.8 and 4.2 nm/min had the following layer structure: 50 nm of *p*–type (Mg doped) GaN, 200 nm UID GaN, and 650 nm of slightly Si–doped (mid 10^{16} cm^{-3}) GaN. The sample grown at a Ga flux of 4.5 nm/min had the following

layer structure: 50 nm of unintentionally doped (UID) GaN, 200 nm of highly Si–doped (mid 10^{18} cm^{-3}) GaN, and 550 nm of slightly Si–doped (mid 10^{16} cm^{-3}) GaN. In all cases, the top active layer of GaN was at least several times thicker than the expected depletion width given the layer's dopant concentration. Samples were cleaned and sonicated in trichloroethylene, acetone, isopropanol, methanol, and de–ionized water for 2 minutes prior to metallization by electron beam evaporation of 33 nm Ti, 77 nm of Al, 33 nm of Ti, and 88 nm of Au. The samples were then annealed at 650 ºC for 3 minutes in 5 % H_2/N_2 forming gas. AFM and CAFM images were obtained with a Veeco Multimode AFM with Nanoscope IIIa controller under ambient environmental conditions (approximately 20 ºC and 50 % relative humidity). A conductive diamond coated tip, which was kept in constant contact with the surface, acted as a Schottky contact to our sample; a reverse–bias condition was established by the application of a positive bias (12–22 V in steps of 2 V) to an Ohmic contact on the sample while the current through the tip was measured with a transimpedance amplifier and simultaneously recorded with topography. For ease of interpretation in terms of the analogous behavior of a conventional Schottky contact, for which it is typical to specify the voltage applied to the Schottky metal contact, we specify the potential of the Schottky probe–tip contact relative to the ohmic sample contact. As described elsewhere,[12] the CAFM signal reveals nonuniformities in sample conductivity. The specific features of interest in this work were localized, highly conductive current leakage paths thought to be associated with threading

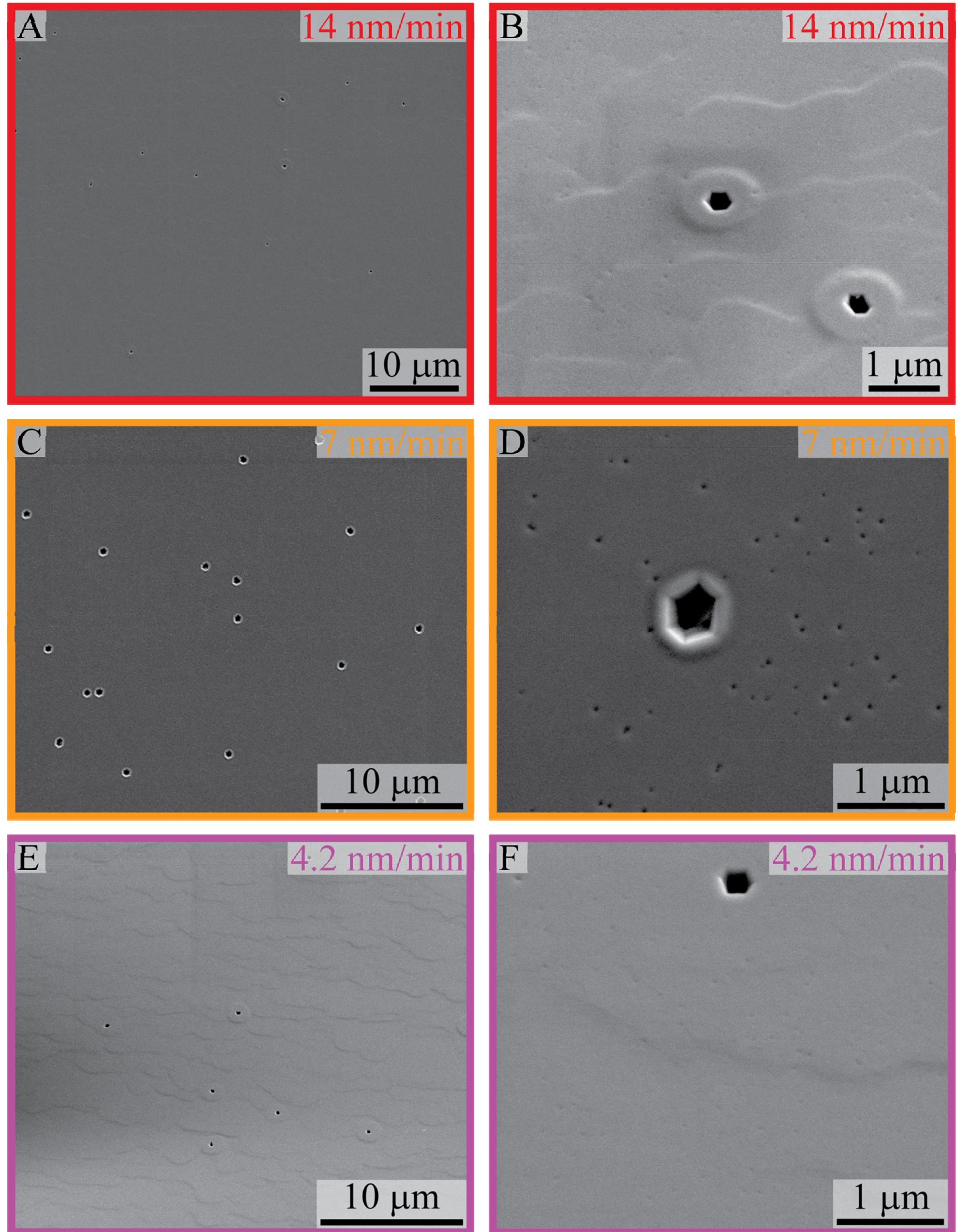


Figure 3.8. FE–SEM images of samples grown at (a) and (b) 14.0 nm/min, (c) and (d) 7.0 nm/min, and (e) and (f) 4.2 nm/min. The shape and size of the open core screw dislocations can be seen in (b), (d), and (f) while the density can be calculated from (a), (c), and (e).

dislocations.[47–50] Figure 3.6 shows a schematic diagram of the sample and probe geometry employed in these experiments.

3.7 Results & Discussion

3.7.1 X–Ray Diffraction

Figure 3.7 shows representative x–ray diffraction (XRD) scans performed on samples grown with 4.2, 7.0, and 14.0 nm/min of Ga flux which showed similar rocking curve widths for on–axis (0002) ω–scan reflections with full–width at half–maximum (FWHM) of 393, 399, and 380 arc seconds, respectively. The different peak values of each of the samples is likely due to slight sample tilt or slight sample rotation while mounting. Since the FWHM of the rocking curves can be used to calculate the total *c*–component (*c* and *a*+*c* components) of all dislocations, we conclude that the total *c*–component of all dislocations across all samples were similar.[51, 52]

3.7.2 Field–Emission Scanning Electron Microscopy

FE–SEM was utilized in order to determine the density of open–core screw–component threading dislocations across the range of growth conditions. Figures 3.8(a)–(f) show FE–SEM images of samples grown at 4.2 nm/min, 7.0 nm/min, and 14.0 nm/min Ga flux, illustrating the hexagonal, puckered nature of these defects. The density of these features was determined to be ~ 6×10^5 cm $^{-2}$, 2.5×10^6 cm $^{-2}$, 7×10^5 cm^{-2}, and 1×10^6 cm $^{-2}$ for the 4.2 nm/min, 7.0 nm/min, 14.0 nm/min, and Lumilog substrate (not shown here) samples, respectively. The lower magnification images in

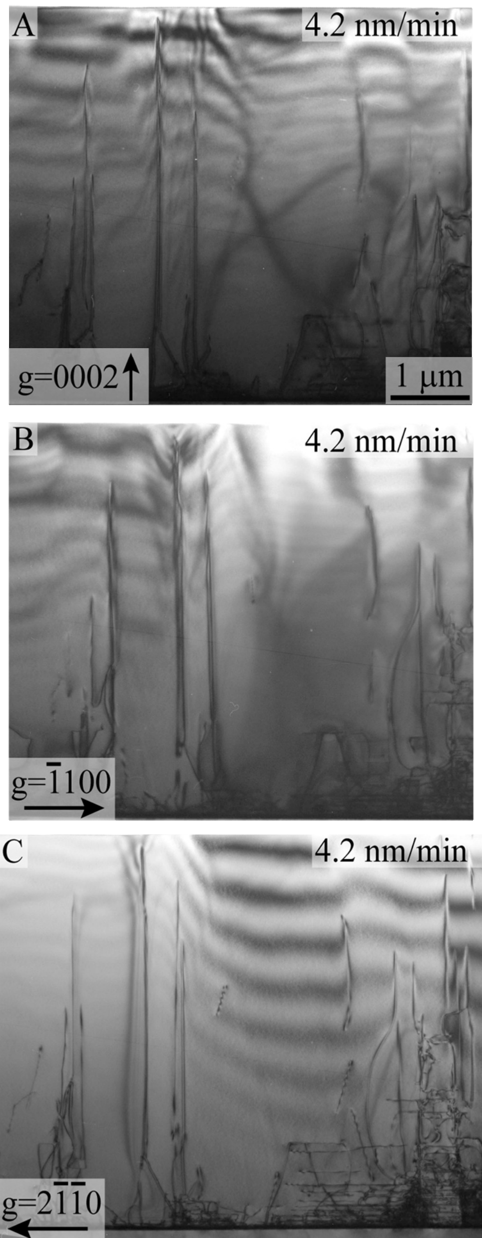


Figure 3.9. XTEM images of the sample grown with 4.2 nm/min Ga flux under (a) $g = \left(000\bar{2}\right)$, (b) $g = \left(11\bar{2}0\right)$, (c) $g = \left(000\bar{2}\right)$, and (d) $g = \left(\bar{1}100\right)$ diffraction conditions.

Figures 3.8(a), 3.8(c), and 3.8(e) were used to calculate the density of these features. The higher magnification images in Figures 3.8(b), 3.8(d), and 3.8(f) show the characteristic hexagonal opening along with surface puckering around the voids. Also apparent in these higher magnification images is the different opening size of the features according to growth conditions and the presences of small pits.

3.7.3 Cross–Sectional Transmission Electron Microscopy

Cross–sectional transmission electron microscopy (XTEM) was done under three diffraction conditions, $g=(0002)$, $g=(\bar{1}100)$, and $g=(11\bar{2}0)$, on samples with Ga–fluxes of 14.0, 7.0, and 4.2 nm/min to determine the relative composition of pure screw dislocations in each of the three samples and to ascertain why varying densities of leakage paths were detected across the range of growth conditions present in this study. Analysis of the XTEM data for samples grown with Ga–fluxes of 14.0 and 7.0 nm/min, as seen in Figure 3.9 and Figure 3.10, respectively, revealed that there were no pure screw dislocations detectible in the layers grown at elevated temperature within the measured areas at the detection limit of this technique. Instead, there were increased percentages of mixed and pure edge dislocations. Given the size of the samples measured, the detection limit of this technique was calculated to be roughly 5×10^{6} – 1×10^{7} cm^{-2} (i.e., 1% of the total dislocation density), which is significantly larger than the detection limit of CAFM; thus, it is not surprising that XTEM did not detect the presence of any screw dislocations in the sample grown at 14.0 nm/min while CAFM did. Figure 3.11 shows XTEM data from the sample grown at 4.2 nm/min, revealing the presence of pure screw dislocations with

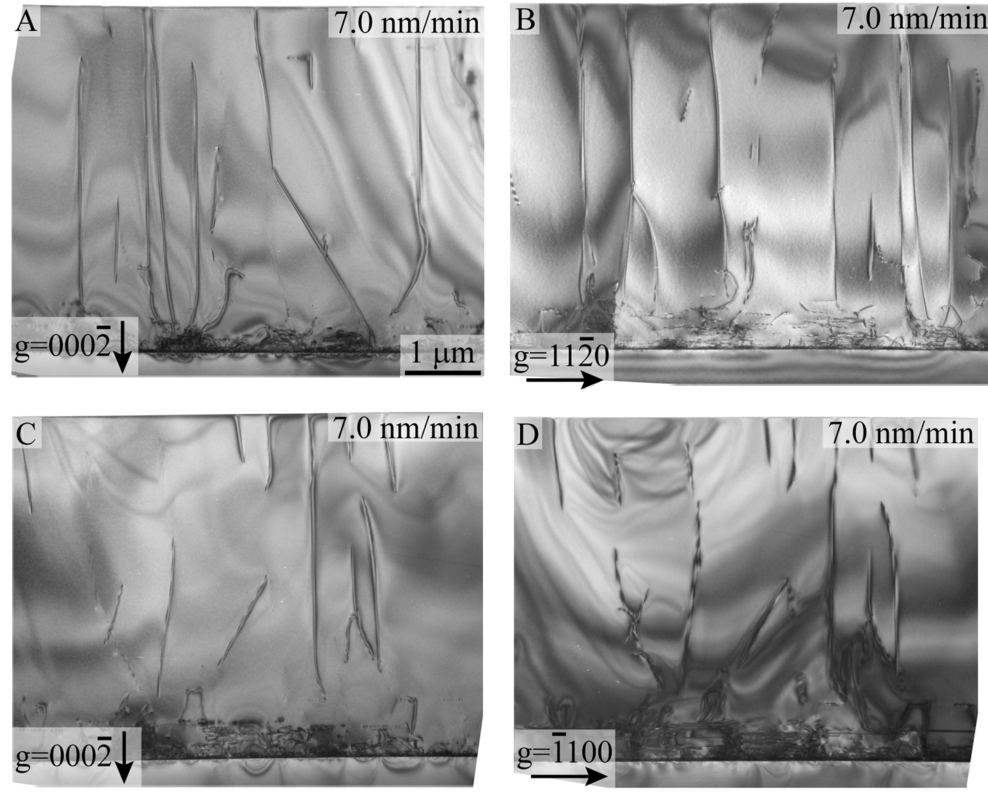


Figure 3.10. XTEM images of the sample grown with 7.0 nm/min Ga flux under (a) $g=\left(000\bar{2}\right)$, (b) $g=\left(11\bar{2}0\right)$, (c) $g=\left(000\bar{2}\right)$, and (d) $g=\left(\bar{1}100\right)$ diffraction conditions.

concentration of approximately 7×10^{6} cm^{-2}, which is in good agreement with the CAFM results at –20 V. Based on the large detection limit of this technique, we believe that the lack of pure screw dislocations in the images collected for samples grown at 7.0 nm/min and 14.0 nm/min is not evidence enough to conclude anything about the proportions of screw, edge and mixed dislocations in these samples.

3.7.4 Tapping Atomic Force Microscopy

Figures 3.12(a)–(g) show AFM images demonstrating that that none of the samples in this study exhibit spiral hillocks on their surfaces, which are typical on the

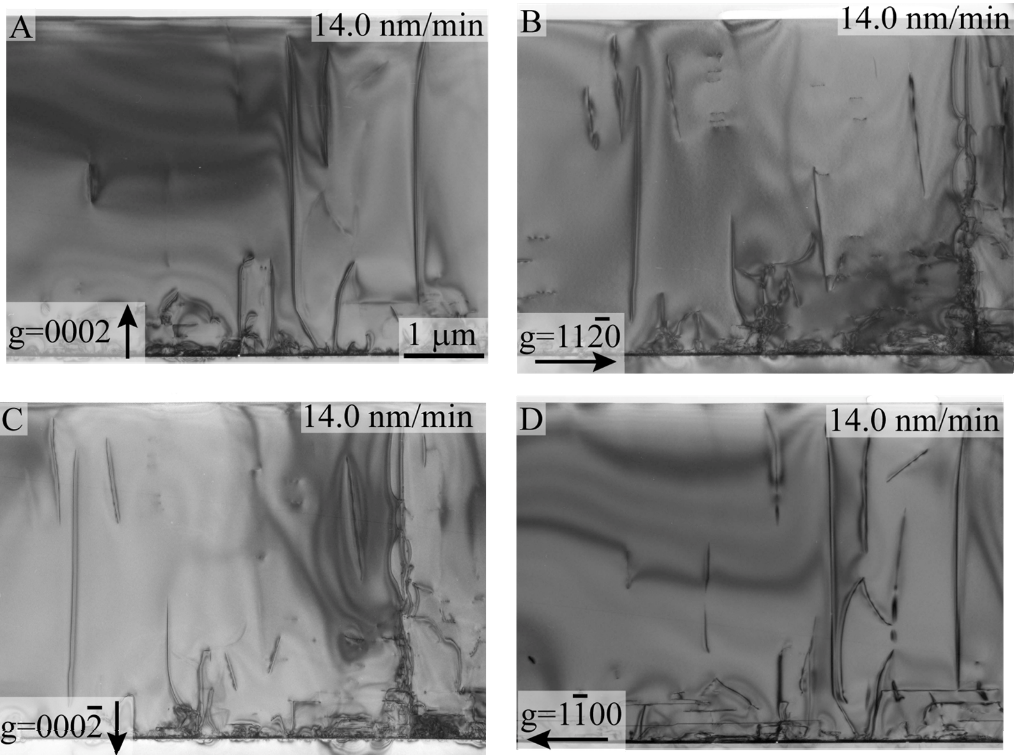


Figure 3.11. XTEM images of the sample grown with 14.0 nm/min Ga flux under (a) $g=\left(0002\right)$, (b) $g=\left(11\bar{2}0\right)$, (c) $g=\left(000\bar{2}\right)$, and (d) $g=\left(1\bar{1}00\right)$ diffraction conditions.

surfaces of GaN grown by MBE at lower temperatures under Ga–rich conditions;[53] however, all samples had smooth morphologies with nanometer–scale surface pit density matching the dislocation density of the substrates, ≈ mid 10^8 cm^{-2}. Figures 3.12(a)–(g) also show the evolution of surface morphology from step flow growth in Figure 3.12(a) to smooth surface morphologies at lower Ga fluxes. Also evident is the varied surface roughness across the range of growth conditions. Surface roughness was minimized for the slightly Ga–rich samples in Figures 3.12(b), 3.12(c), and

3.12(d) to around 1 nm root mean squared (RMS). Surface roughness increased at the crossover to N–rich growth in Figures 3.12(e), 3.12(f), and 3.12(g) to ≈ 1.5 nm RMS.

Based on the pit densities measured by AFM, the FWHM of (0002) rocking curves measured by XRD, and open core densities measured by FE–SEM, we conclude that the proportions of pure screw and mixed component dislocations are consistent across all of the samples in this study.

3.7.5 Conductive Atomic Force Microscopy

Figure 3.13(a) shows an AFM topograph of a sample grown with a Ga flux of 4.5 nm/min. Figures 3.13(b)–(f) show the corresponding CAFM images of the area in Figure 3.13(a), obtained at dc biases of –14 V, –16 V, –18 V, –20 V, and –22 V applied to the tip relative to the sample. The wavy lines in Figures 3.13(b)–(f) are 60 Hz noise. The diagonal line in Figures 3.13(c), 3.13(d), and 3.13(e) is a systematic shift in the detected current which was most likely due to an external electrical noise source. Figure 3.13(b) shows several small, dark features which correspond to localized reverse–bias leakage paths observable at –14 V bias. In Figure 3.13(c), the reverse–bias voltage magnitude was further increased and the density of observed conductive paths increased as well. This trend of increasing conductive path density as a function of increasing reverse–bias voltage magnitude is seen to continue in Figures 3.13(d), 3.13(e), and 3.13(f).

Figure 3.14(a) shows an AFM topograph of a sample grown with a Ga flux of 4.2 nm/min. Figures 3.14(b)–(f) show the corresponding CAFM images of the area in Figure 3.14(a), obtained at dc biases of –14 V, –16 V, –18 V, –20 V, and –22 V

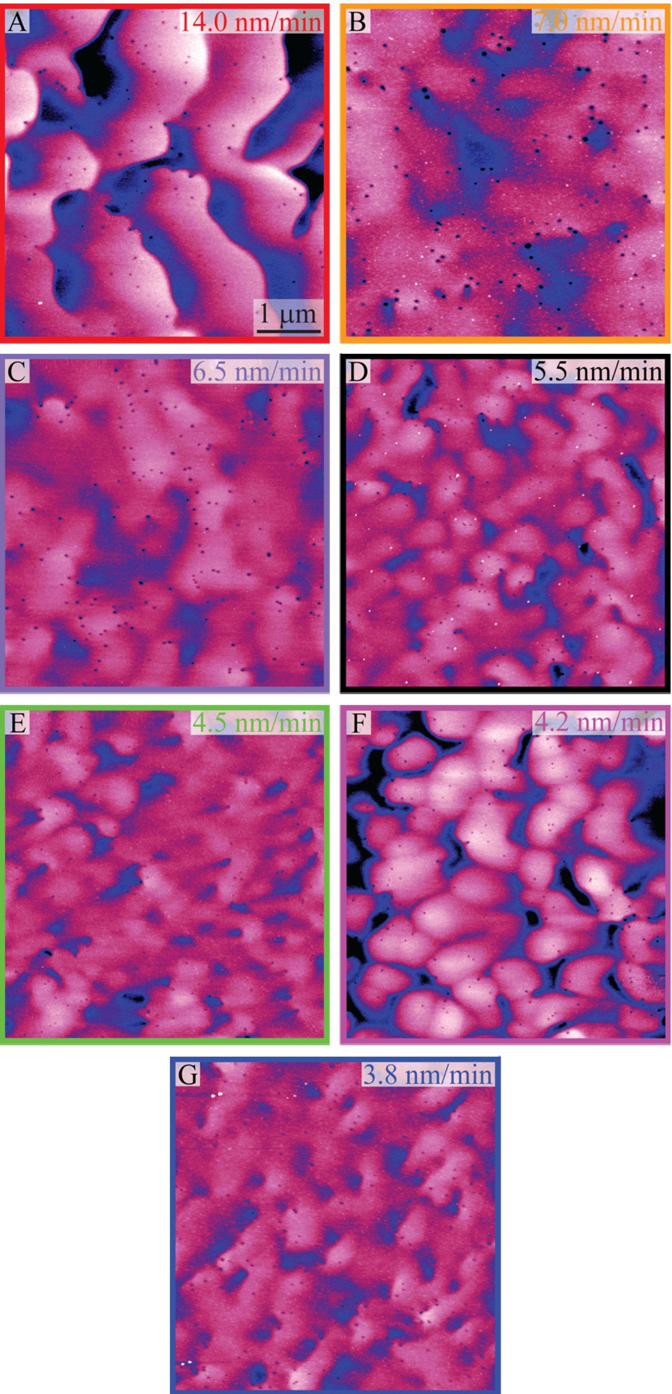


Figure 3.12. AFM images of samples grown at (a) 14.0, (b) 7.0, (c) 6.5, (d) 5.5, (e) 4.5, (f) 4.2, and (g) 3.8 nm/min showing the varying topographic features and roughness across the range of growth fluxes. The vertical scale for all these images is 10 nm.

applied to the tip relative to the sample. The noise sources and systematic shift present in Figures 3.14(b)–(f) are the same as those in Figures 3.13(b)–(f). The trend of increasing density of leakage paths with increasing magnitude of reverse bias is similar to Figures 3.13(b)–(f). However, in Figures 3.14(b)–(f), the size and shape of each leakage path changes as a function of the number of passes with the probe tip and the bias voltage. The corresponding topographic images (not shown here) show small elevated hemispherical regions that grow with increasing magnitude of bias voltage and number of scans.

Figure 3.15(a) shows an AFM topograph of a sample grown with a Ga flux of 3.8 nm/min. Figures 3.15(b)–(f) show the corresponding CAFM images of the area in Figure 3.15(a), obtained at dc biases of –12 V, –14 V, –16 V, –18 V, and –20 V applied to the tip relative to the sample. The noise sources and systematic shift present in Figures 3.15(b)–(f) are the same as those in Figures 3.13(b)–(f). The trend of increasing density of leakage paths with increasing magnitude of reverse bias is similar to Figures 3.13(b)–(f) and Figures 3.14(b)–(f). However, in Figures 3.15(d)–(f), the size of each leakage path grow more quickly than in Figures 3.14(b)–(f) with increasing magnitude of reverse bias. The shape of these features in Figures 3.15(b)–(f) (the outline of which can be seen in the current maps) changes to become more elliptical instead of hemispherical as in Figures 3.14(b)–(f). It is likely that there is some thin oxide layer forming due to presence of an anodizing voltage and a thin water layer on the surface of the samples due to the ambient humidity.[48]

A more general analysis of the CAFM images for all samples suggests that at these elevated growth temperatures there is a narrow band of fluxes near Ga/N ≈ 1 for which there was no detectable localized reverse–bias leakage conduction. Figure 3.16 and Table 3.1 show the conductive behavior of all the samples in this study as a function of reverse–bias voltage and Ga flux during growth. The very Ga–rich sample with high flux of 14.0 nm/min showed poor surface morphology—this sample was grown in the step–flow regime—with surface roughness ≈ 3 nm RMS (measured over a 5 × 5 μm^2 area), but reduced densities of leakage paths (low–to–mid 10^6 cm^{-2} conductive paths at –20 V). Slightly Ga–rich samples with Ga fluxes of 7.0, 6.5, and 5.5 nm/min showed excellent morphologies with roughness less than 1 nm RMS and no reverse–bias leakage at the highest level of sensitivity of our measurement technique (20 pA and ~ 5×10^5 cm^{-2}). The sample grown at 7.0 nm/min Ga flux showed no detectable leakage up to –28 V. N–rich samples (i.e., samples with Ga fluxes of 4.5, 4.2, and 3.8 nm/min) also showed excellent surface morphologies with roughness ≈ 1.5 nm RMS, but, in contrast to their Ga–rich counterparts, showed increased reverse–bias leakage. In general, decreasing the Ga flux from 14.0 nm/min reduced the density of reverse–bias leakage paths until the crossover to N–rich growth at which point the conductive path density began to increase dramatically. The decreased density of leakage paths in the sample grown at 4.2 nm/min, as compared to the sample grown at 4.5 nm/min, was most likely due to the differences in underlying layer structure (as explained in the Experiment section above). Qualitatively, the trend

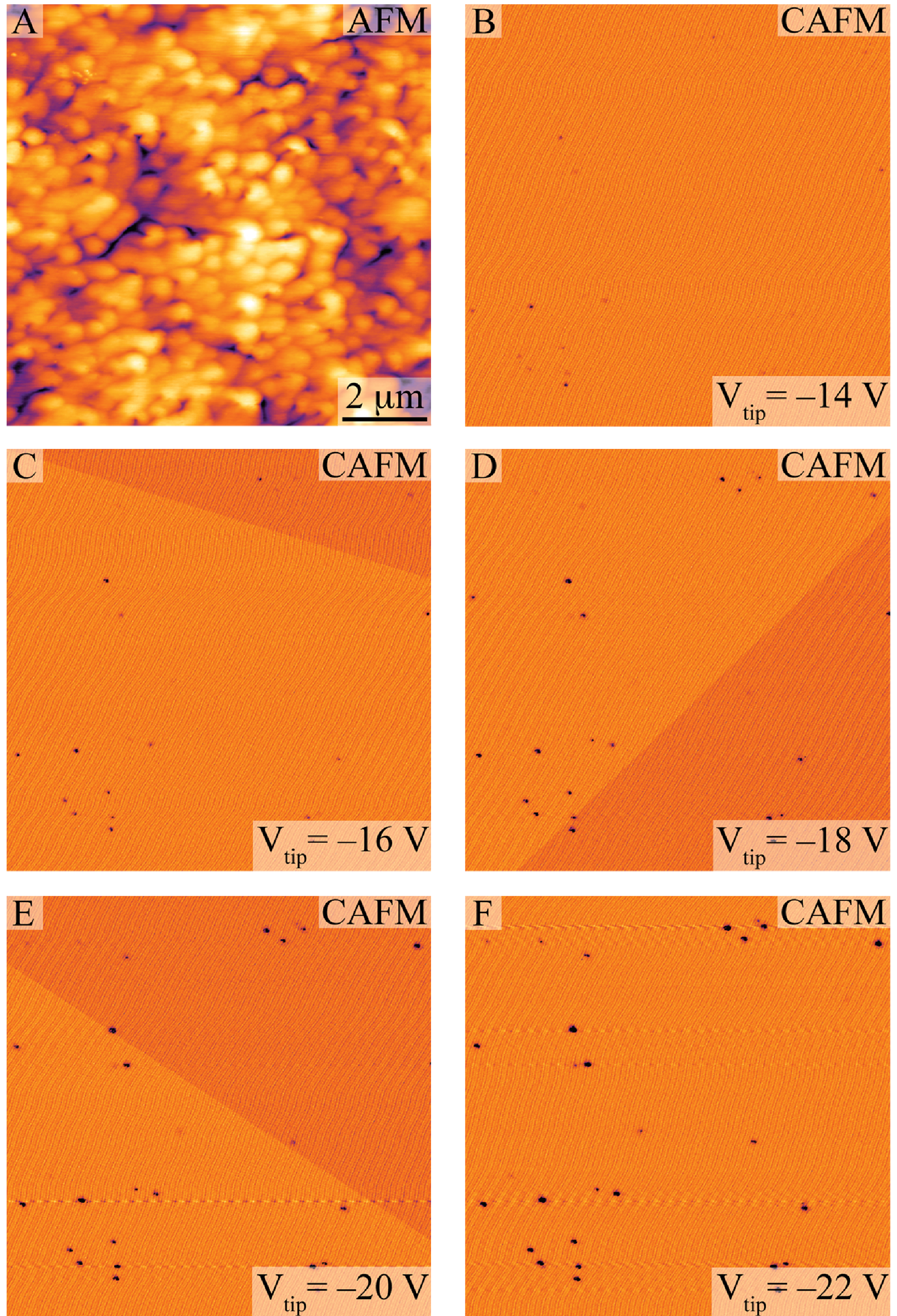


Figure 3.13. (a) AFM topograph and (b)–(f) CAFM images obtained at tip dc bias voltages of –14 V, –16 V, –18 V, –20 V, and –22 V for sample grown with 4.5 nm/min Ga flux. Wavy lines in (b)–(f) are 60 Hz noise. The scales correspond to range of 8 nm for topography and 5×10^{-11} A for the current map.

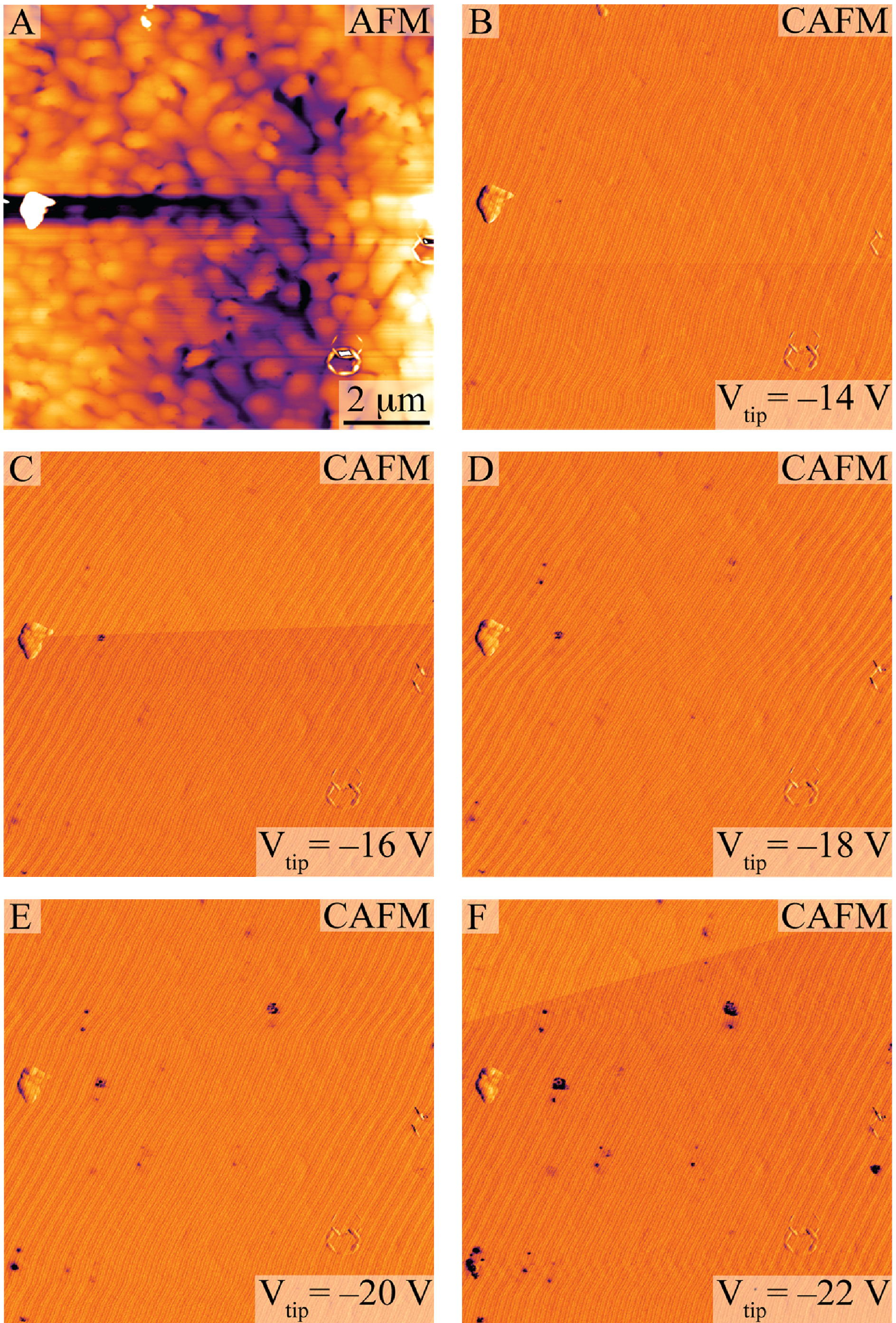


Figure 3.14. (a) AFM topograph and (b)–(f) CAFM images obtained at tip dc bias voltages of –14 V, –16 V, –18 V, –20 V, and –22 V for sample grown with 4.2 nm/min Ga flux. Wavy lines in (b)–(f) are 60 Hz noise. The scales correspond to range of 8 nm for topography and 5×10^{-11} A for the current map.

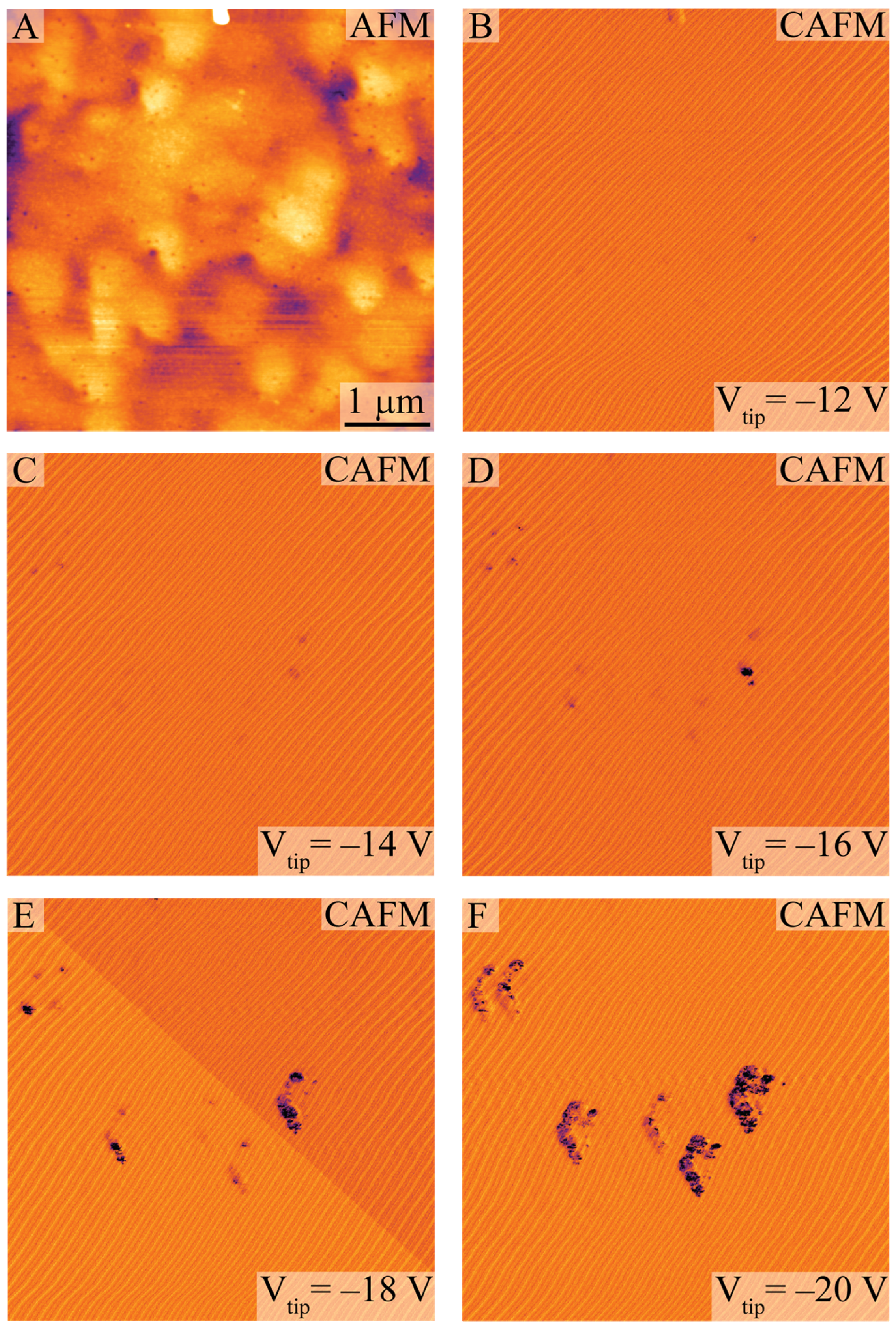


Figure 3.15. (a) AFM topograph and (b)–(f) CAFM images obtained at tip dc bias voltages of –12 V, –14 V, –16 V, –18 V, and –20 V for sample grown with 3.8 nm/min Ga flux. Wavy lines in (b)–(f) are 60 Hz noise. The scales correspond to range of 8 nm for topography and 5×10^{-11} A for the current map.

of increasing reverse–bias leakage path density with decreasing Ga–flux (increasing N–flux) was the same for all N–rich samples.

Table 3.1. Conductive paths versus bias voltage and Ga flux during growth corresponding to Figure 3.16.

	Reverse bias voltage				
Sample	**–12 V**	**–14 V**	**–16 V**	**–18 V**	**–20 V**
3.8 nm/min	**2.4×10^{6} cm^{-2}**	**9.8×10^{6} cm^{-2}**	**1.8×10^{7} cm^{-2}**	**3.4×10^{7} cm^{-2}**	**3.4×10^{7} cm^{-2}**
4.2 nm/min	**≈0**	**7.1×10^{5} cm^{-2}**	**4.6×10^{6} cm^{-2}**	**1.0×10^{7} cm^{-2}**	**2.0×10^{7} cm^{-2}**
4.5 nm/min	**1.2×10^{6} cm^{-2}**	**7.3×10^{6} cm^{-2}**	**1.4×10^{7} cm^{-2}**	**1.9×10^{7} cm^{-2}**	**2.4×10^{7} cm^{-2}**
5.5 nm/min	**≈0**	**≈0**	**≈0**	**≈0**	**≈0**
6.5 nm/min	**≈0**	**≈0**	**≈0**	**≈0**	**≈0**
7.0 nm/min	**≈0**	**≈0**	**≈0**	**≈0**	**≈0**
14 nm/min	**≈0**	**1.1×10^{6} cm^{-2}**	**3.0×10^{6} cm^{-2}**	**3.7×10^{6} cm^{-2}**	**4.8×10^{6} cm^{-2}**

Since the mechanism that allows for conduction from a dislocation into the bulk material has not been definitively established, we cannot be certain that the inconsistent layer structure of the samples grown with Ga fluxes of 3.8, 4.2, and 4.5 nm/min samples does not influence our data. If the leakage current from the dislocation enters the bulk material within the ~ 0.5–0.8 μm thickness of the top *n*–GaN layer, the current paths for all the samples should be similar and the lateral resistance in the sample should be substantially smaller than the resistance at the tip–sample junction. If the current from the dislocation enters the bulk material at greater depths where the sample structures differ, the samples with Ga fluxes of 3.8 and 4.2 nm/min should exhibit low leakage by virtue of having an additional electrically insulating junction below the top *n*–GaN layer. Nevertheless these samples exhibit high leakage currents, roughly consistent with the sample grown at a Ga flux of 4.5 nm/min which has a highly conductive n^{+}–GaN layer below the top *n*–GaN.

Therefore, we conclude that the current is leaving the dislocation and entering the bulk within the first ~ 0.5–0.8 μm thickness of the top *n*–GaN layer, which is consistent across all of the samples in this study.

These results are in contrast to prior results based on homoepitaxial MBE growth of (0001) GaN on MOCVD templates at lower temperatures, which suggested that Ga–rich growth yields higher carrier mobility due to good surface morphology, but increased reverse–bias leakage due to conductive dislocations, and that N–rich growth yields lower carrier mobility associated with poor surface morphology, but decreased reverse–bias leakage.[9] In the present studies, consistent pit densities (measured by AFM and FE–SEM) and FWHM of (0002) ω–scans (measured by XRD) across the range of growth conditions suggest that the defect densities and compositions of all samples grown at high temperature are comparable. Therefore, in the case of high growth temperatures, it is unlikely that the absence of leakage paths in the slightly Ga–rich samples was a result of defect reduction whether in the form of a reduction of the total number of defects or a change in the relative densities of screw or screw–component threading dislocations (i.e., a relative increase in one type of dislocation to compensate for a decrease in another). Because the maximum density of leakage paths (≈ mid 10^7 cm^{-2}) in the N–rich, high–temperature samples was significantly larger than the expected pure screw threading dislocation density (≈ mid 10^6 cm^{-2}), it is possible that both screw–component and pure screw threading dislocations are conducting.[54] This might indicate that it is not solely the Burgers vector of the defect that dictates its conductive behavior. Rather, we suggest that the

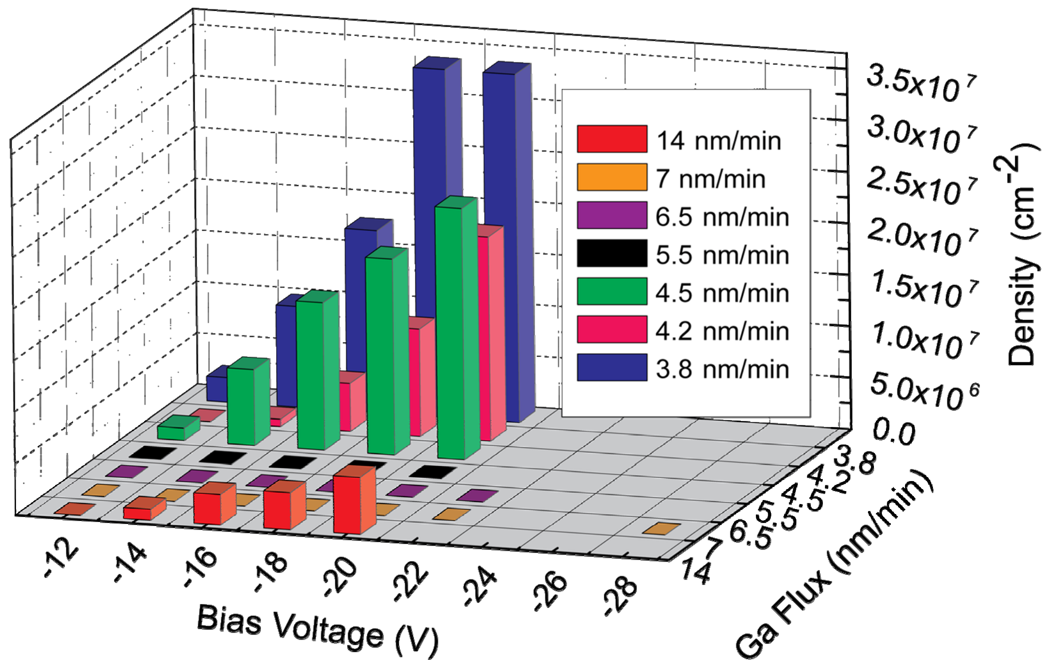


Figure 3.16. Conductive paths versus bias voltage and Ga flux during growth.

Ga–rich, high–temperature growth conditions have modified the aggregation of impurities along the dislocations or point defects surrounding the dislocations, with these impurities or defects being responsible for inducing local, reverse–bias leakage pathways in *n*–type GaN grown by MBE. Prior studies of conductivity associated with threading dislocations have in fact proposed that surface or near–surface defects can play an important role in controlling reverse–bias leakage currents associated with the presence of dislocations.[49, 55] From a surface growth kinetics point of view, this could be largely influenced by differences in thermal dissociation behavior observed under different Ga/N flux ratios at the high growth temperatures employed in this study.[56] This possibility is currently under further investigation. Furthermore, our data suggest an *in situ* method for suppressing threading dislocation leakage paths in

GaN grown by MBE via selection of appropriate ranges of temperature and Ga/N flux ratios, enabling elimination of a significant source of reverse–bias leakage at room temperature in Schottky contacts to *n*–type GaN.

3.8 Future Work

Further work should be done to ascertain the impact of the underlying layer structure on the conductive nature of these leakage paths. Though we conclude that the intermediate layers do not impact conduction, the only way to be certain is to eliminate any such layers from the samples. Additionally, performing a series of CAFM studies on growths carried out at lower temperatures on the same Lumilog substrates would directly correlate the growth temperatures and fluxes with the elimination of the leakage pathways. Explicitly determining whether it is impurities along the dislocation or point defects near the dislocation that are changed by the elevated growth temperatures would reveal why these particular growth conditions were successful at eliminating reverse bias leakage pathways. A better understanding of the surface terminations of the different dislocations types would greatly benefit future, similar studies. For instance, in this work, we are not clear about what the surface termination of edge, screw, and mixed dislocations should be. Also, there seems to be some debate about the nature and even existence of open versus full core screw dislocations.

3.9 Conclusion

In summary, AFM, CAFM, FE–SEM, and XRD were used to determine the effects of Ga/N flux ratio at elevated growth temperatures on the formation and

conductive behavior of pure screw and screw–component threading dislocations in GaN grown by MBE. Our data reveals a narrow band of fluxes near Ga/N ≈ 1 for which local reverse–bias leakage paths ceased to be observable. The evolution of local reverse–bias leakage path density as a function of Ga flux at elevated growth temperature in conjunction with the consistent densities of screw and screw–component dislocations might indicate that the conductive nature of these defects is determined by impurities along or point defects near dislocations. These observations are in contrast with previous studies that suggest it is not possible to simultaneously achieve smooth surfaces/interfaces and negligible local reverse–bias leakage,[9] and they could have substantial implications for the growth and expected performance of III–nitride based semiconductor devices.

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4 Scanning Capacitance Characterization of Potential Screening in Indium Arsenide Nanowire Devices

4.1 Introduction

Semiconductor nanowires offer promising capabilities for future high–performance electronic,[1] optoelectronic,[2] biomedical,[3] and thermoelectric,[4, 5] devices and platforms for basic investigations of electronic structure and carrier transport in low–dimensional systems. InAs nanowires, in particular, are a superb candidate for high speed, high density, ultra–low power circuits due to their narrow band gap (0.354 eV at 300 K),[6] high electron mobility—in excess of 33,000 cm^2/Vs in bulk material[7]—and surface Fermi–level pinning[8] in the conduction band, which allows for the formation of Ohmic contacts with relative ease. Because of the geometries often employed in nanowire–based devices, understanding the interaction and influence of nearby macroscale objects, such as bulk contacts, on nanowire behavior is of paramount importance. Conventional macroscopic electrical characterization techniques yield only limited and/or indirect understanding of the interactions and influences of macroscale and nanoscale objects, while scanning probe measurements of local electronic properties enable highly spatially accurate, nondestructive, direct experimental characterization of these interactions.

We have used scanning capacitance microscopy (SCM) and spectroscopy (SCS), in conjunction with finite–element numerical simulations, to examine the effects of micron–scale metal contacts typically present in nanowire–based electronic

devices on carrier modulation and electrostatic behavior in semiconductor nanowires. Our results reveal a remarkably strong dependence of the capacitance spectra on the distance separating the probe tip and the metal contact, extending to distances of 3–4 μm and beyond. This dependence is revealed, by comparison of the SCM/SCS data with finite–element electrostatic simulations, to be a consequence of electrostatic screening of the tip–nanowire potential difference by the large metal contact. These results provide direct experimental verification of contact screening effects such as those postulated for carbon nanotube (CNT) based devices.[9] The design and expected performance of nanowire–based electronic devices, most notably nanowire field–effect transistors (NWFET), may be strongly influenced by these screening effects, and they are indicative of the importance of mitigating the effects of large–scale contacts and circuit elements on the performance of nanoscale electronic devices.

4.2 Nanowire Growth Techniques

A myriad of growth techniques can be leveraged to synthesize semiconductor nanowires including solution methods,[10] laser ablation,[11, 12] wafer annealing,[13] chemical vapor deposition (CVD),[14] organo–metallic vapor phase epitaxy (OMVPE),[15–17] selective area OMVPE (SA–OMVPE),[18] and molecular[19] and chemical[20] beam epitaxy (MBE and CBE). The vast majority of these techniques rely on the use of a metal seed particle that acts as a catalyst and feed source from which high aspect ratio growth can proceed. The differences between these growth techniques are the form of the chemical reactants and how they are delivered to the growth particle.

Solution processing allows for the epitaxial growth of semiconductor nanowires by utilizing heated liquid solutions to transport reactants to a catalyst. This method should be somewhat familiar to anyone who has ever made rock candy as a child. Growth can be achieved with temperatures and pressures only slightly higher than room temperature; however, the technique does not provide good control over purity and crystallinity.

Higher control over purity and crystallinity can be achieved with techniques where a laser is used to ablate material from a target wafer. The material is then transported to a growth substrate where it can react to form an epitaxial layer. This technique is useful in that it allows for the use of a wide variety of target materials and compounds, so growth of more chemically complex structures is possible while maintaining the desired phase of the target material.

In wafer annealing, a solid source or wafer can be heated to high temperatures to sublime excess reactants into a vapor which is transported to a lower temperature area where growth can occur on another substrate. CVD is a similar process by which chemical reactant species are carried in gaseous form to a heated substrate where the precursors decompose on the surface of the heated substrate to form high quality epitaxial layers. CVD also has the added advantage of being able to handle many different precursor sources.

OMVPE utilizes the thermal decomposition of input reactants on the surface of a growth substrate to precipitate epitaxial growth. Typically, this technique is used in the growth of group III–V and group II–VI compound semiconductors. OMVPE uses

metal–organic species such as trimethylindium (TMI, $In(CH_3)_3$) for group III input precursors and hydrides such as Arsine (AsH_3) for group V input precursors, but group V metal–organics (tertiarybutylarsine, $C_4H_{11}As$, and trimethlyarsine, $As(CH_3)_3$) can also be used as chemical reactants. Selective area epitaxy can be achieved with OMVPE by either randomly or deliberately covering regions with thin dielectric layers upon which it is energetically unfavorable for growth to occur.

Ultra–high vacuum conditions allow for the formation and continuity of non–reactive elemental (Ga) and molecular (As_2) beams as reactants in MBE. The beams are directed towards a heated growth substrate where they condense and react to form epitaxial layer structures. MBE has much lower growth rates than OMVPE. At slightly higher pressures, like OMVPE, CBE (sometimes called metal–organic MBE) uses metal–organic and hydride sources with long diffusion lengths and highly directional species transport, like MBE, to achieve growth rates in between MBE and OMVPE.

The mechanism of reactant incorporation into the one–dimensional growth is still under scrutiny. Vapor–liquid–solid (VLS)[11,13,14,15,18,19,20] or vapor–solid–solid (VSS)[16, 21] growth is thought to be the mechanisms responsible for growth of the nanowire in the presence of a metal catalyst particle. Growth can occur without a metal catalyst in all the techniques described above. Group III autocatalyzed VLS growth,[17,22,23,24] defect– or dislocation–driven growth,[25] oxide assisted growth,[12] reactive Si–assisted growth,[14] and ligand–aided solution–solid (LSS) growth[10] are the

mechanisms that facilitate compound semiconductor nanowire growth in the absence of nanoparticle catalysts.

4.3 Vapor–Liquid–Solid Growth

Metal particle precipitated one–dimensional growth is known as the VLS growth process. The incipient work was conducted by Wagner and Ellis in 1964.[26] Their work took an Au particle deposited on the (111) surface of a Si wafer and heated it up to 950 ºC to form an Au–Si liquid droplet. This droplet acts as a decomposition catalyst for $SiCl_4$ and a sink for the resulting Si. This Si then diffuses into the particle eventually saturating the particle. Upon super–saturation, the liquid–solid interface between the particle and the substrate begins to precipitate excess Si where it freezes to form layers of solid Si between the particle and the droplet. As this process continues, the particle is lifted away from the substrate by successive layers of frozen Si. This process can be applied to other elemental semiconductor materials such as Ge. Wu and Wang demonstrated that the VLS process was the mechanism responsible for the formation and growth of nanowires in the presence of a metal catalyst.[27] Using a high temperature transmission electron microscopy (TEM), as shown in Figure 4.1, they showed the three distinct stages of VLS growth: metal alloying, crystal nucleation, and axial growth.

The VLS growth process, shown schematically in Figure 4.2,[28] for compound semiconductor nanowires such as group III–V (InAs, GaAs, InP, etc.) is similar to that described above for elemental semiconductors, but slightly more complicated due to the presence of both group III and group V reactants. Typically Au is used as the

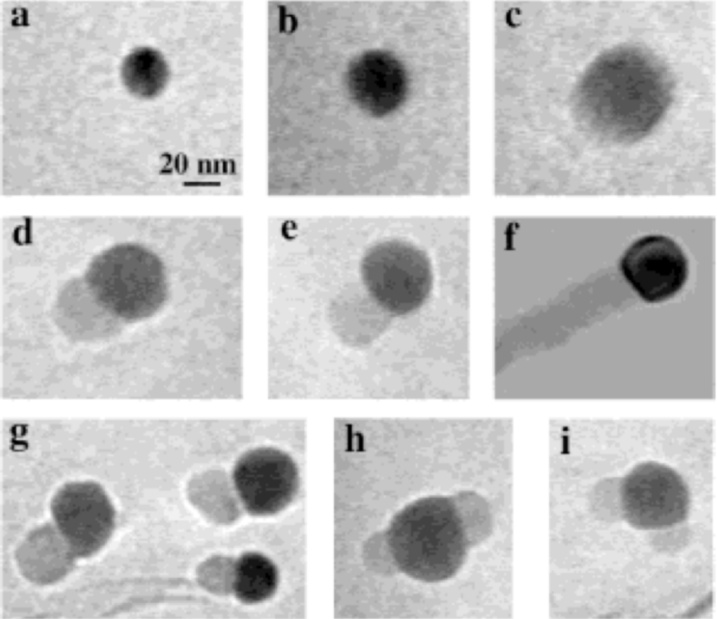

Figure 4.1. *In situ* TEM images recorded during the process of nanowire growth. (a) Au nanoslusters in solid state at 500 ºC; (b) alloying initiates at 800 ºC, at this stage Au exists in mostly solid state; (c) liquid Au/Ge alloy; (d) the nucleation of Ge nanocrystal on the alloy surface; (e) Ge nanocrystal elongates with further Ge condensation and eventually a wire forms (f). (g) Several other examples of Ge nanowire nucleation, (h), (i) TEM images showing two nucleation events on single alloy droplet [Ref. 27].

metal catalyst. During VLS growth of III–V nanowires, the group III element has a lower alloying temperature with Au. At nanowire growth temperatures during MOVPE VLS growth, the group III element is provided by the full decomposition of the metalorganic, e.g., TMI.[29] The group III element forms the critical alloy with the Au particle, while the group V precursor, e.g., AsH_3 or PH_3, is typically not fully decomposed at these temperatures and either undergoes 1:1 pyrolysis with TMI[30] or decomposes at the surface of the Au particle.[23] The group V element has low solubility in the Au–group III particle at these temperatures and it is forced to diffuse

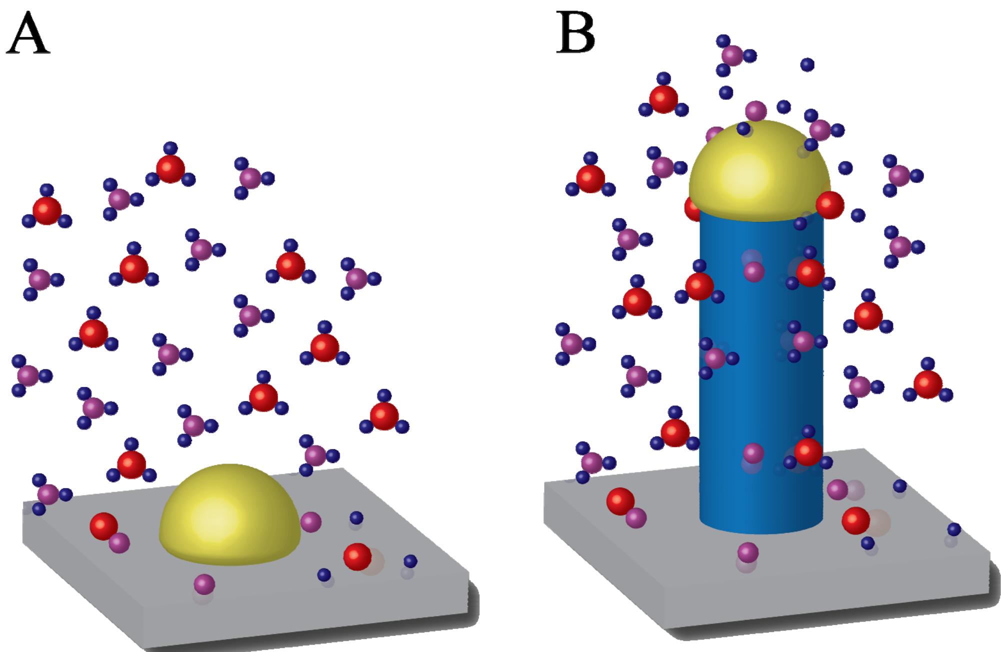

Figure 4.2. (a) Illustration of the decomposition of trimethylindium ( ) and arsine ( ), and alloying of Au and In to form supersaturated nanoparticles. (b) Illustration of the vapor–liquid–sold one–dimensional growth process showing reactant decomposition, In incorporation into particle, As diffusion along surface of particle to particle–wire interface, and surface diffusion along substrate and wire facets [Ref. 28].

along the surface of the particle.[31] Eventually, it either escapes the particle into the gas phase or arrives at the liquid–solid interface where it reacts with the frozen group III element recently forced out of the supersaturated particle, forming the compound semiconductor. Similar to the case for Si, this reaction between the group III and group V elements pushes the particle upwards and leaves behind a column of semiconductor material, or nanowire.

In principle, the VLS growth process is straightforward; however, there are many necessary prerequisites that must be satisfied in order for the process to actually occur. The nanoparticle must form a liquid solution with the material selected to be

grown. Contact angles between 95º and 120º with respect to the growth substrate enable the particle's rise above the surface.[32, 33] High supersaturations are required in the particle during initial stages of growth in order for the particle to rise above the substrate surface.[32] For the catalytic and adsorptive properties of the liquid particle to be effective in the decomposition of precursors, incorporation of constituent elements, and growth via precipitation, the chemical reactions that occur inside the growth system must all be kinetically unfavorable but thermodynamically possible.[34] Preferentially vertical growth with respect to the substrate surface necessitates an oxide free surface. In order to maintain growth stability and consistency for epitaxial nanowire growth on III–V substrates, $(111)\mathrm{B}$ surfaces are preferred because $(111)\mathrm{A}$ surfaces have two major drawbacks: a propensity towards easy oxidization and the metal nanoparticles form excessively large contact angles with these surfaces.[35] As a result of the aforementioned requirements, growth temperatures for nanowires are typically 100–300 ºC less than those of thin film growth. Nanowire nucleation and growth rates must be optimized within this temperature range as too low temperatures may not allow the formation of a liquid particle and oxide desorption, while too high temperatures reduce the group III supersaturation in the particle by increasing material solubility. Mastery of the morphological and electrical properties of the wires requires even more rigorous control over variables like temperature, pressure, and ratio of input species.

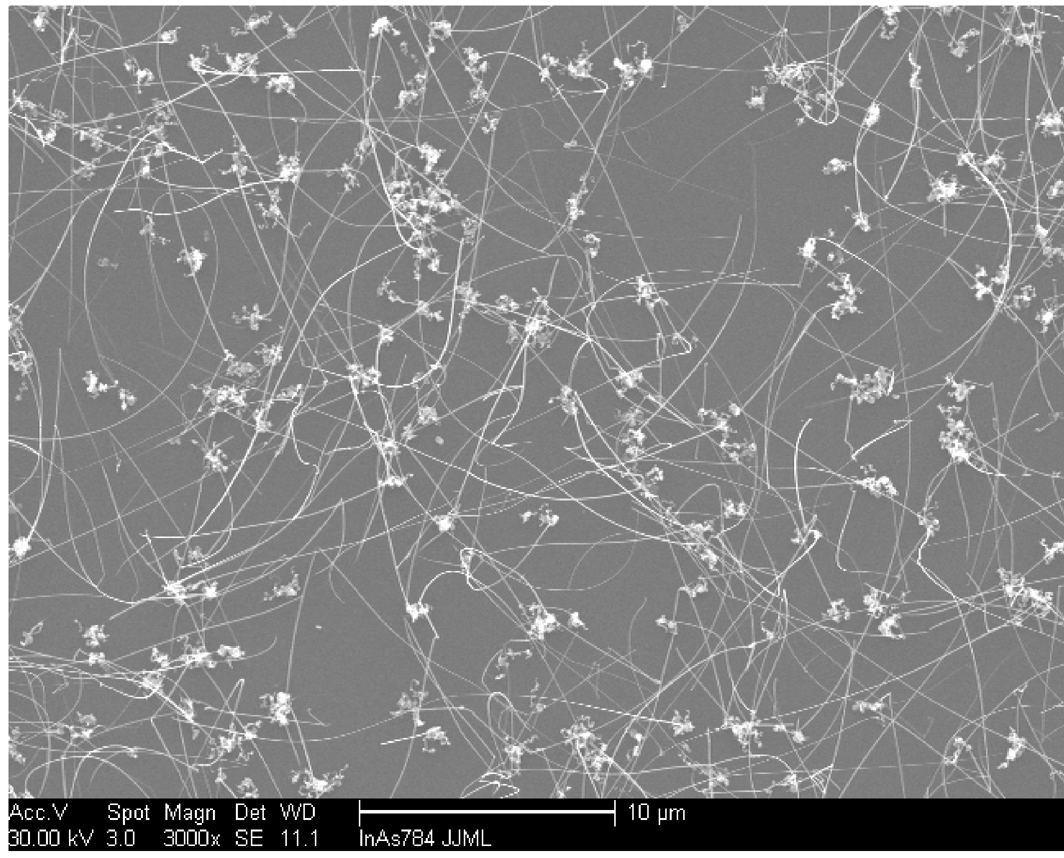

Figure 4.3. SEM image of a growth substrate taken immediately after growth showing multiple nucleations from single In islands and morphology of the individual wire.

4.4 Indium Arsenide Nanowire Growth

A horizontal flow OMVPE reactor was used to grow the InAs nanowires in this study. TMI and arsine were flown as precursors with 1.2 standard liters per minute (slm) of H_2 as the carrier gas. Si substrates with 600 nm thick thermally grown oxide were used as growth substrates. The substrates were cleaned by sonication for 2 minutes in trichloroethylene, acetone, methanol, and deionized water. Growths were carried out by dispersing 40 nm diameter Au nanoparticles from colloidal solution onto the oxide surface. Typical particle densities were $\approx$ 0.2 particles/μm^2.

Previously, great care was taken by Dayeh et al. to understand the role of Au nanoparticles in the growth of InAs nanowires on SiO_2 surfaces and to optimize the growth conditions for the wires presented in this work to achieve the best possible wire morphology.[23] Low surface roughness, minimal tapering, and sufficient length were achieved by growing at 350 ºC with an input V/III ratio of 50 for a time of 20 minutes. The temperature was ramped up at a rate of ≈ 2 ºC/s and allowed to stabilize in an H_2 ambient. After the growth, the sample was allowed to cool in an AsH_3 and H_2 ambient. Samples were left in N_2 flow prior to removal from the growth reactor. The resulting wires had lengths in excess of 10 μm and diameters between ≈ 60 – 120 nm. Figure 4.3 shows a scanning electron microscope (SEM) image of a representative growth substrate. The wires are not oriented to the surface but, instead, grow in random directions, and they are generally curved over some portion of their length. Small indium islands are apparent throughout the image and across the entire growth substrate, and multiple wires originate from these indium islands. TEM and electron diffraction showed the wires to be entirely zincblende crystal structure with a $\langle 110 \rangle$ growth orientation. The wires had twin boundaries along their growth–direction axis. Further details of the growth procedure, conditions, and resulting morphologies have been described elsewhere.[23, 28]

4.5 Electrical Device Fabrication

Electrical device structures were fabricated by placing the growth substrate in a small vial of ethanol and sonicating it. The force of the agitation was sufficient to break the wires free from the growth substrate and suspend them in the ethanol. The

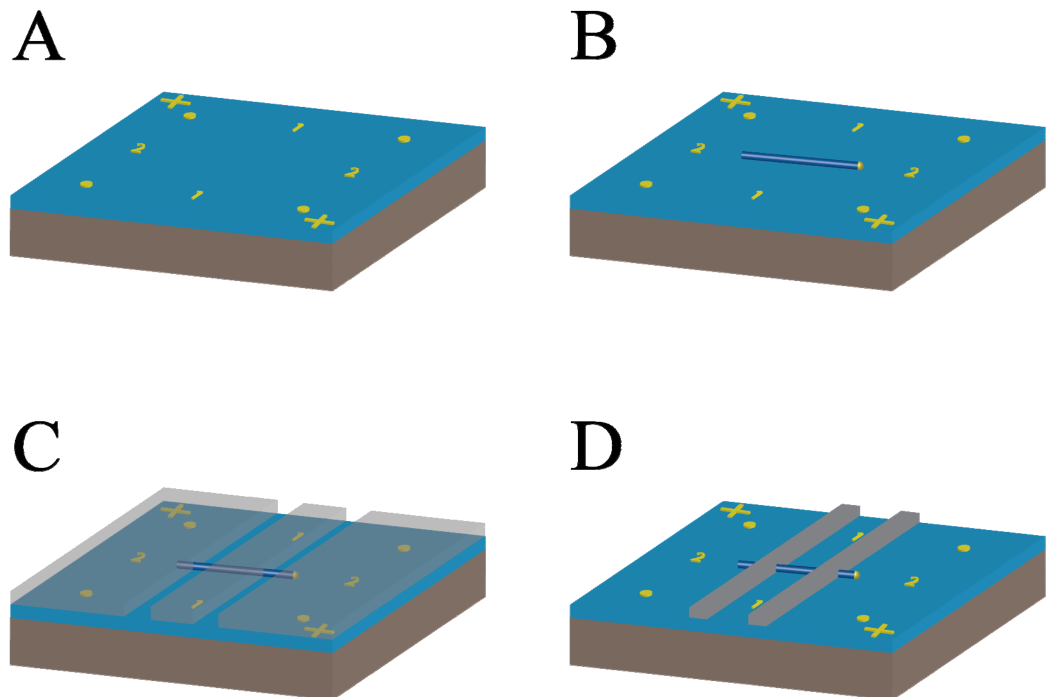

Figure 4.4. Schematic illustrating the nanowire alignment process. (a) Thermally oxidized silicon substrates patterned with numbered grids and alignment marks. (b) Nanowires are drop cast onto substrate. (c) Electron beam resist is spun, exposed, and developed. (d) Source and drain electrodes are deposited using electron beam evaporation and remaining metal is lifted off.

substrate was then removed from the vial. This process can be repeated multiple times to achieve the desired wire density in solution. The wires were drop cast by capillary tubes onto 600 nm thermally oxidized SiO_2/n^+–Si substrates that were pre–patterned with alignment marks and registration grid for later lithography. Figures 4.4(a) and 4.4(b) show schematics of the pre–patterned substrate before and after wires were randomly oriented on the surface. Once the wires were placed on the surface, the substrate was imaged using a Nomarski optical contrast microscope. A script written for the commercial plotting software Igor Pro version 4 combined with the numbered grids allowed the position of each wire to be input into a CAD file. The CAD file

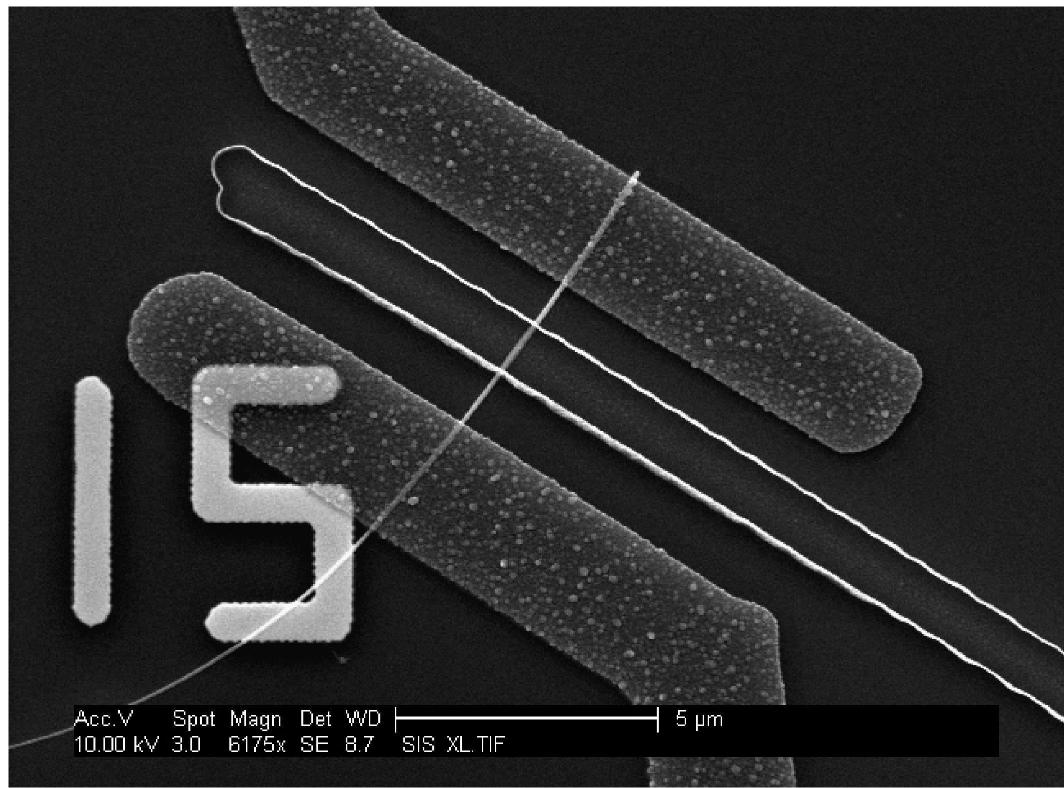

Figure 4.5. SEM image of a fully process nanowire field effect transistor showing source, drain, and top gate with a portion of the wire extending to the lower left of the image [Ref. 24].

would later be used to define a mask for electron–beam lithography of the source and drain electrodes, gate dielectric, and gate electrode. After spinning electron–beam resist on the sample, electron–beam lithography was used to define 2 μm wide openings in the resist for metal deposition of the source and drain electrodes, as seen in Figure 4.4(c). Ohmic contacts were made in Figure 4.4(d) by electron–beam evaporation of 15 nm of Ti and 85 nm of Al. A 73 nm Y_2O_3/ZrO_2 film, for which the relative dielectric constant is 12, was sputter deposited to act as the insulating layer between the probe tip and the nanowire surface and also as a gate dielectric. Electron–beam lithography was used to define 1 μm wide gate regions. A 100 nm thick Al

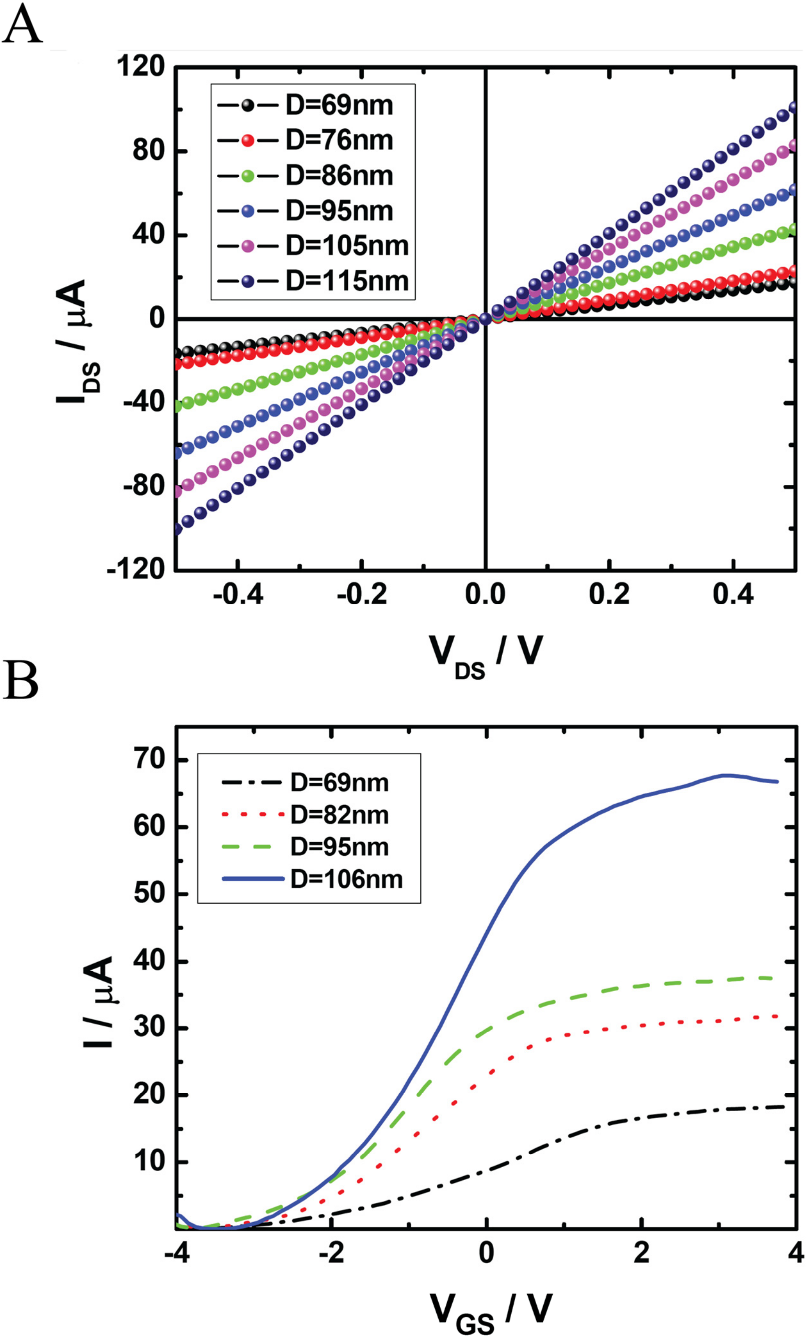

Figure 4.6. (a) I_{DS} versus V_{DS} at $V_{GS} = 0$ V for several InAs NWFETs with varying diameters. (b) I_{DS} versus V_{GS} at $V_{DS} = 0.5$ V for the same InAs NWFETs in (a) [Ref. 24].

layer was sputter deposited to act as the gate electrode. Figure 4.5 shows an SEM image of a completed device structure. Our scanned probe experiments utilized the portions of the wire that stuck out from one side of the device, as seen in the lower left portion of Figure 4.5 but were free from contact with other objects.[24] Top–gated current–voltage measurements of wire devices fabricated in this fashion were carried out to verify the ohmic nature of the contacts and extract important device parameters such as mobility and carrier concentration. Figures 4.6(a) and 4.6(b) were adapted from reference 24 and show I_{DS} versus V_{DS} at V_{GS} = 0 V and I_{DS} versus V_{GS} at V_{DS} = 0.5 V for top–gated nanowire devices of varying diameter.

4.6 Scanned Probe Experiment

A Digital Instruments (Veeco) Nanoscope IIIa Dimension 3100 microscope with a diamond–coated probe tip was utilized to probe the nanowire capacitance versus voltage characteristics near a single contact, yielding both scanning capacitance images at fixed bias voltages and local spectra of the scanning capacitance signal, dC/dV, as a function of bias voltage. For SCM measurements, a bias voltage consisting of a dc component with a small (≈2 V) ac modulation, typically at a frequencies of 20–95 kHz, was applied to the sample with the probe tip grounded. For SCS measurements, the probe tip was held at a fixed position while a low frequency (≈0.5 Hz) saw–tooth wave of amplitude varying between 6 and 12 V and a high frequency (20–95 kHz) ≈ 2 V–amplitude sine–wave bias were applied to the sample with the probe tip grounded. As discussed in detail elsewhere,[36–38] the SCM/SCS signal detection mechanism yields a voltage signal that is proportional, in our

measurements, to dC/dV, where C is the tip–sample capacitance and V is the dc component of the applied bias voltage. Typical ambient conditions for these experiments were ≈ 20 ˚C and ≈ 50 % relative humidity. For ease of interpretation in terms of analogous behavior of a conventional metal–insulator–semiconductor structure, for which it is typical to specify the voltage applied to the metal contact relative to the semiconductor, we at this point adopt the convention of specifying the potential of the probe tip, V_{tip}, relative to the sample in discussion and analysis of the SCM/SCS data. Figure 4.7 shows a schematic diagram of the sample and probe tip geometry employed in these experiments.

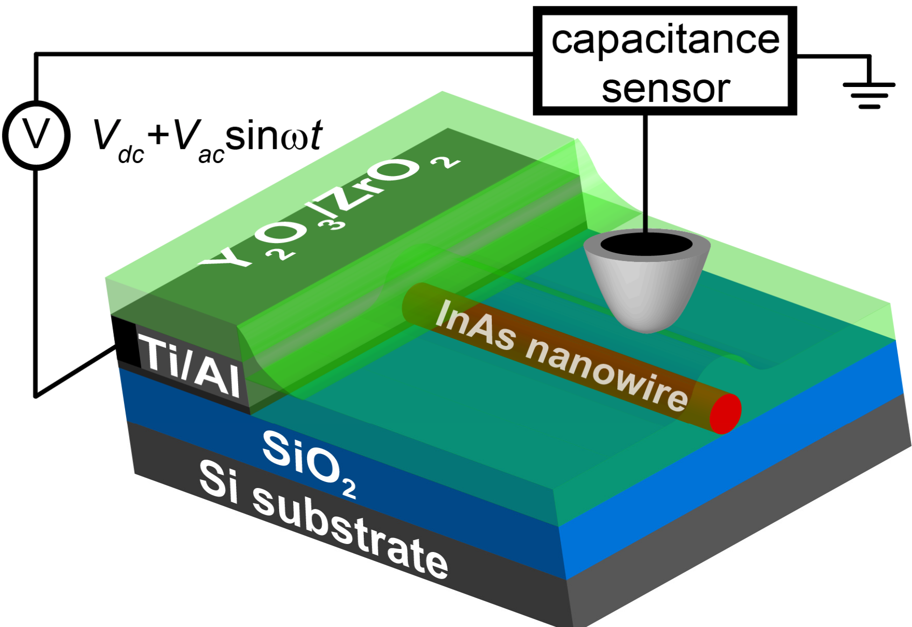

Figure 4.7. Schematic diagram of the sample structure, scanning probe measurement geometry, and voltage biasing arrangement.

4.7 Simulation Geometry

Finite–element electrostatic simulations were carried out using the commercial simulation package COMSOL Multiphysics. The simulation geometry sought to mimic the electrostatic environment in the experimental geometry as accurately as possible. Thus, a wire of 7 μm in length and 70 nm in diameter; a rectangular metallic contact 7 μm in length (perpendicular to the axial direction of the nanowire), 3 μm in width (parallel to the axial direction of the nanowire), and 70 nm in height; and a

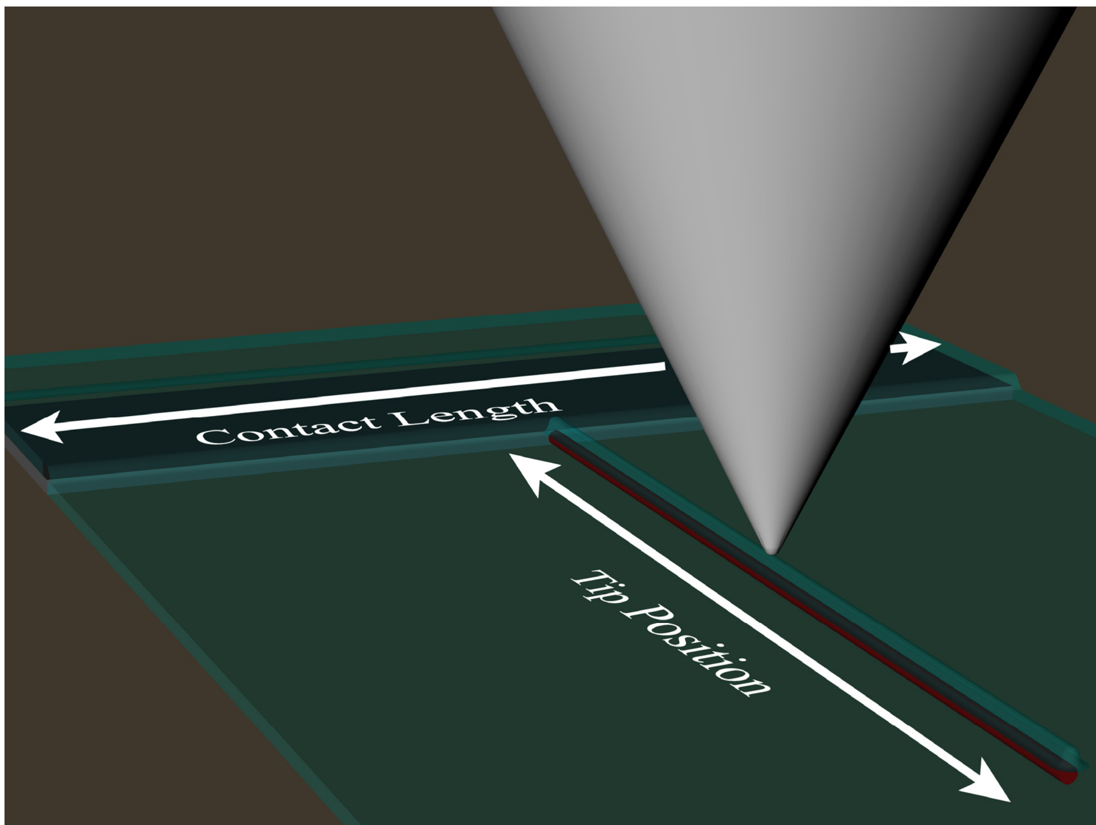

Figure 4.8. Scale illustration of the simulation geometry showing the nanowire in red, probe tip in light grey, contact in dark grey, and conformal oxide coating in green. Relevant geometric variables in the simulations, tip position and contact length, are shown in white.

probe with tip radius of curvature of 50 nm and of conical cross section 7μm in height and 3.5 μm in radius at the base were simulated. The wire and the contact were both conformally coated in a dielectric layer 73 nm in thickness with relative dielectric constant ε_r = 12. Further simulations were carried out with a smaller contact measuring 100 nm in length, 3 μm in width, and 70 nm in height in order reduce the cross–sectional area normal to the long axis of the wire. The wire was given the dielectric constant of bulk InAs (ε_r = 15)[7] and an electrical conductivity of 6×10^4 S/m, which is the value determined from current–voltage characteristics obtained from the wires in this experiment. Both the contact and the probe tip were treated as equipotential surfaces at varying static potentials with the contact permanently at ground while the tip was set at positive bias. The probe tip was placed at the apex of the wire/dielectric system and at regular intervals along the axial direction of the wire, as illustrated to scale in Figure 4.8. The simulation yielded the potential profile of the entire simulated geometry.

4.8 Results and Discussion

Figure 4.9(a) shows an AFM topograph of a nanowire and contact. Figures 4.9(b)–(j) show SCM images of the area corresponding to the topographic image in Figure 4.9(a), obtained at dc bias voltages of –4 V to +3 V applied to the tip relative to the sample. Figures 4.9(b) and 4.9(c) show no SCM contrast indicating that at these dc biases the *dC/dV* curve is flat, i.e., the wire is likely depleted or the capacitance change is no longer measurable by our instrument. With an increase of the dc bias to –1 V, corresponding to Figure 4.9(d), we begin to see a small amount of SCM

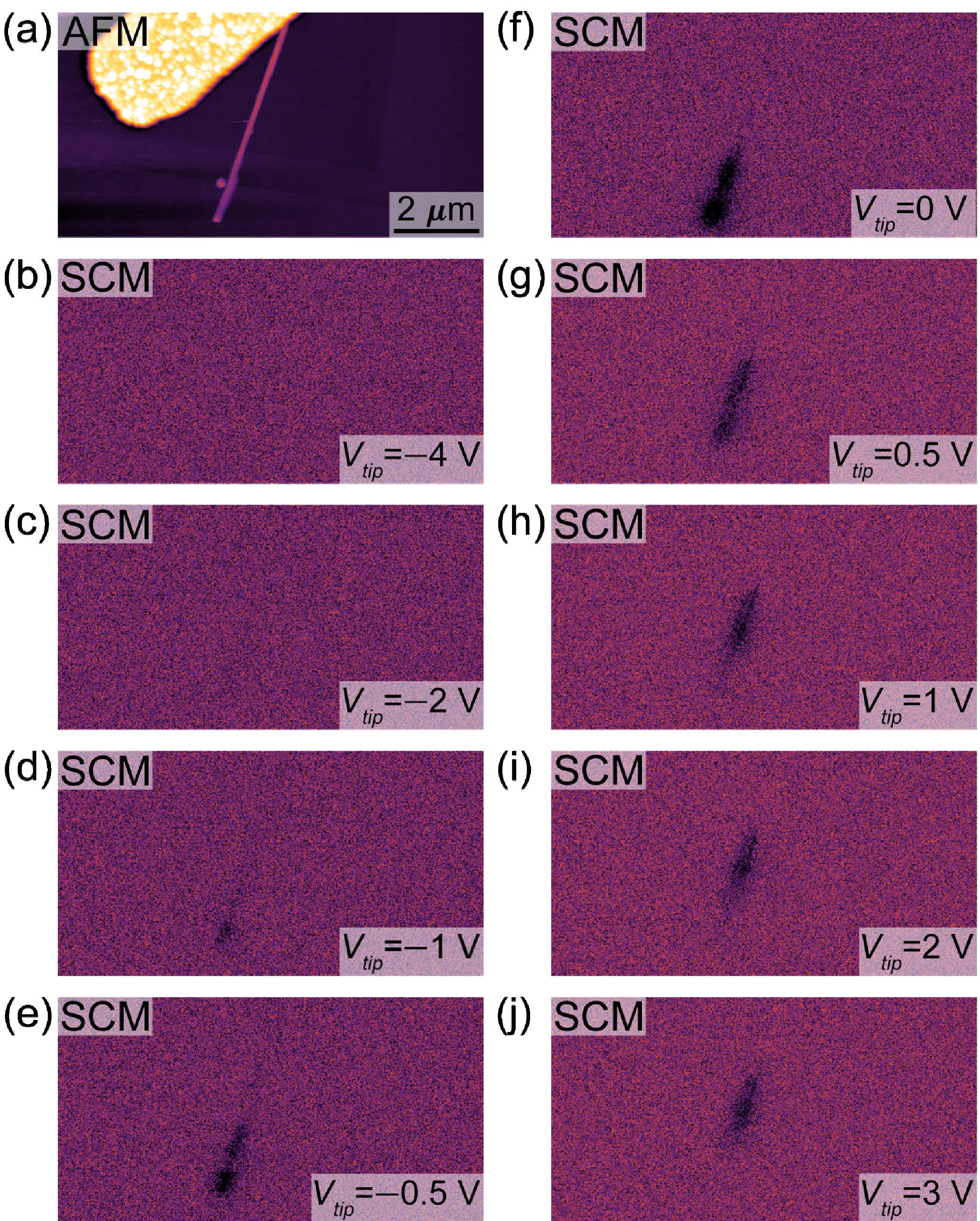

Figure 4.9. (a) AFM topograph with gray scale of 150 nm in height and (b)–(j) SCM images of an InAs nanowire and Al contact obtained at dc bias voltages of –4V, –2V, –1V, –0.5V, 0V, 0.5V, 1V, 2V, and 3V, respectively.

contrast. At –0.5 V and 0 V, shown in Figures 4.9(e) and 4.9(f), the contrast level has increased dramatically. In Figures 4.9(g)–(i), the contrast begins to decrease, but the center of the contrast area begins to move towards the contact. More generally, as the dc voltage is increased from –4 V to +3 V, the peak of the SCM signal contrast shifts closer to the metal contact. These results indicate that there is an additional influence on the device, for in a semiconductor nanowire (or planar device structure) of uniform doping and potential profile, *C(V)* and thus, *dC/dV*, should be invariant as a function of position, resulting in an SCM image of the nanowire that shows constant signal contrast across the entirety of the sample.

Figure 4.10(a) shows an AFM topograph of another InAs nanowire, in this case nearly perpendicular to the contact. The wire is approximately 6.5 μm in length and slightly tapered. Figure 4.10(b) shows a density plot of the SCS versus distance along the wire. Figure 4.10(b) consists of four separate plots, for which the data were collected, from top to bottom, in the following dc tip voltage ranges: –3 V to 7 V, –7 V to 7 V, –7 V to 10 V, and –5 V to 12 V. The topographic region that corresponds to each of these sections is marked by boxes in Figure 4.10(a). Some portions of the top– and bottom–most density plots contain areas where there was no wire. The black portions of Figure 4.10(b) indicate voltage ranges where no data was collected. It is evident from the density plot that the *dC/dV* versus *V* behavior of the wire is not uniform along the length of the wire. Near the contact, the peak of the SCS signal decreases in value and shifts towards higher voltages as the tip approaches the contact. There also appears to be a slight broadening of the peak in the *dC/dV* versus *V* curves

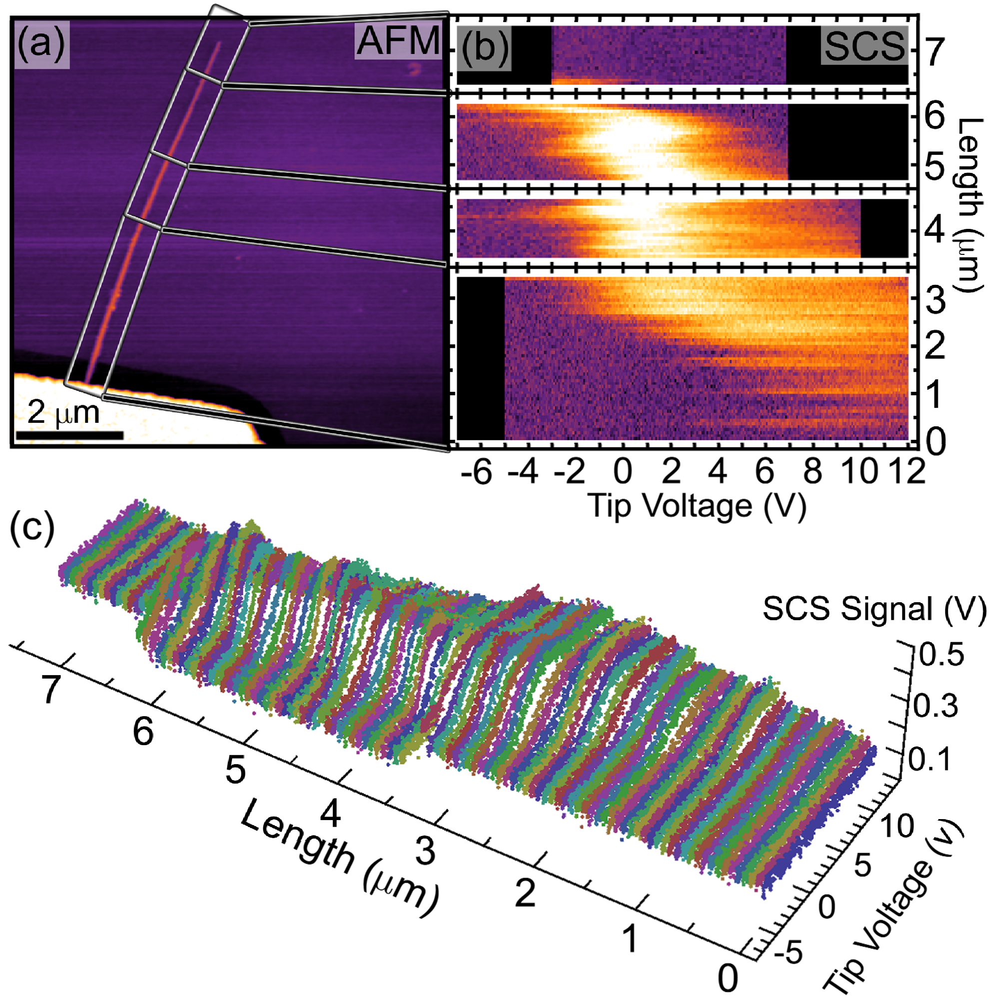

Figure 4.10. (a) AFM topograph with gray scale of 150 nm in height, (b) density plot of SCS signal versus length along the nanowire, and (c) individual line slices of SCS data as a function of tip voltage and length along the nanowire, black regions in (b) indicate data not collected.

near the contact. Several microns away from the contact, the SCM signal contrast is larger and varies little as a function of distance from the contact.

Figure 4.10(c) shows a three–dimensional plot of the scanning capacitance signal as a function of tip voltage and distance from the contact in 100 nm increments. From Figure 4.10(c), it is evident that the peak of the *dC/dV* versus *V* spectra shifts to

larger positive voltages as the tip approaches the contact. Qualitatively, this behavior is similar to that seen in Figures 4.9(b)–(j) leading us to conclude that the angle between the wire and the contact has relatively little influence on the qualitative behavior of the system. Each of the *dC/dV* spectra was fitted using a polynomial and subsequently differentiated to find the voltage at which the peak in the *dC/dV* occurs as a function of tip–contact distance. This voltage is plotted as a function of the tip distance from the contact in Figure 4.11(a). Spectra taken less than one micron away from the contact had peaks at voltages larger than the 12 V limit of our instrument, as shown in Figure 4.10(c); thus, they are not included in Figure 4.11(a). Some of the spectra near the non–contacted end of the nanowire had peaks that were too small to definitively extract a peak, and thus these values were also not included. We attribute the negative voltage of the peaks occurring at approximately 6 μm in Figure 4.11(a) to the presence of localized charge between the wire surface and the oxide, which would cause a shift in the associated *dC/dV* spectra. However, the overall trend of the curve remains the same. Figure 4.11(a) explicitly demonstrates that the maxima in the *dC/dV* spectra, and correspondingly the threshold voltage for electron accumulation at the InAs surface, shift substantially, in a highly nonlinear fashion, as a function of distance from the contact.

Examination of the tip–sample capacitance behavior as a function of distance between the probe tip and a nearby large–area contact reveals the strong influence of the large contact on the local electrostatic behavior of the nanowire. Local, nanoscale

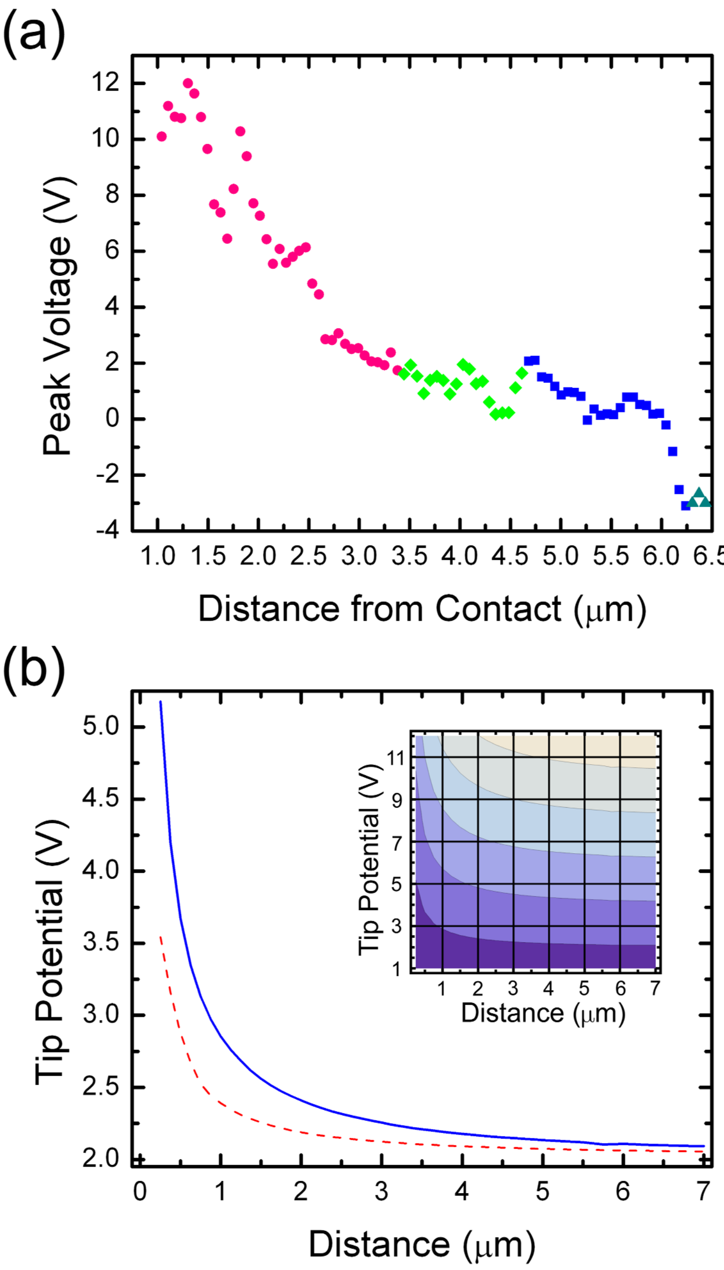

Figure 4.11. (a) Plot of the voltage of the peak of the *dC/dV* curve versus the tip distance from the contact with different shapes corresponding to the different sections in Figures 4.10(a) and 4.10(b). (b) Plot of tip voltage required to produce constant potential (2 V) at the nanowire surface directly below the tip for a 7 μm long contact (solid line) and a 100 nm long contact (dashed line) showing the reduced effects of the screening for the smaller contact geometry. (Inset) Plot of constant surface potential contours directly beneath the tip for a 7 μm long contact versus tip voltage and the separation between the tip and the contact.

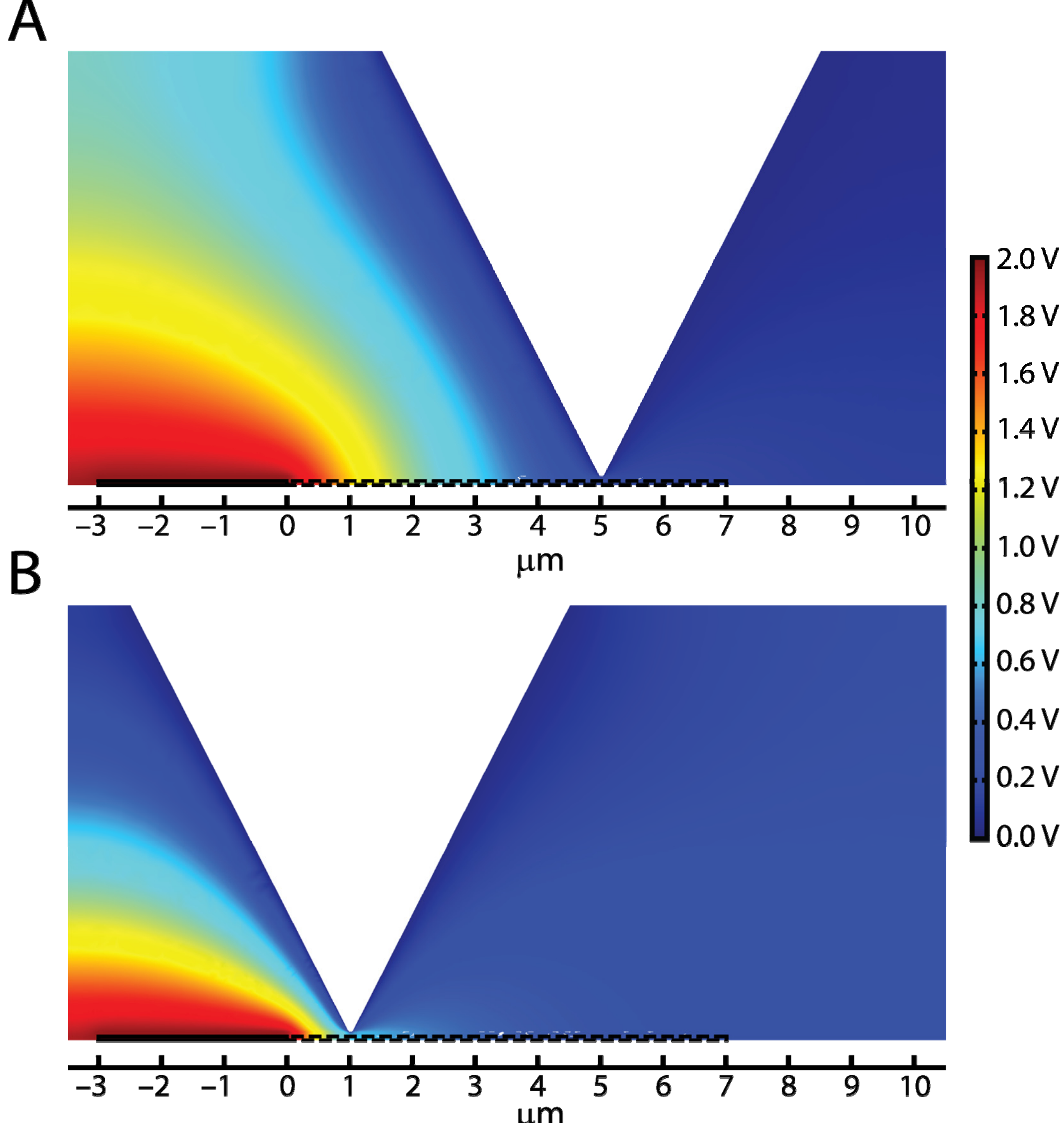

Figure 4.12. Density plots of potential slices through the apex of the wire and tip along the axial direction of the wire with the tip grounded and the source electrode at 2 V. The dashed region indicates the positon of the wire while the solid region indicated the position of the electrode. (a) The tip is positioned 5 µm away from the contact–nanowire interface and (b) the tip is positioned 1 µm away from the contact–nanowire interface. The potential profiles show an exponential increase in potential as a function of position between the contact and the probe in (a) and (b), and the decay length of that increase is nonlinearly dependent on the distance between the probe and the contact. The voltage drop across the oxide also scales nonlinearly as a function of the separation distance between contact and probe.

carrier modulation characteristics and electrostatic behavior of the nanowire vary substantially as a function of distance from the nanowire/contact interface. Specifically, the threshold voltage for carrier accumulation at the InAs surface shifts to lower voltages as the distance from the contact increases, indicating that the large contact screens a significant portion of the electric field from the scanning probe tip even at distances from the contact as large as a few micrometers. A highly nonlinear dependence of the screened potential on contact–tip spacing is observed. We note that the threshold voltage of our devices occurs at positive voltages despite negative threshold voltages in the literature for similar devices.[39] We speculate that this may be due to a combination of surface or interface charges, the small electron affinity of diamond, and, thus, the correspondingly large surface potential difference between our tip and the InAs nanowire. Finally, in our experimental geometry, the metal contact is 100 nm tall in the direction perpendicular to the substrate and the nanowire's diameter is 70 nm, also perpendicular to the substrate, and as a result, the sputter–coated oxide near the contact–nanowire interface has a shape that is a superposition of both the contact and the nanowire; thus, the increased thickness of the oxide near the contact changes the amount of screening by the large contact and complicates the electrostatic behavior of the nanowire very close to the contact.

Figure 4.11(b) shows the results of finite–element electromagnetic simulations of the tip–sample experimental geometry. Each simulation placed the tip at a different distance from the contact. The contact potential was kept at 0 V and the tip was held at potentials varying between 1 V and 12 V in increments of 1 V. Each simulation

generated the potential profile for the entire structure, and the inset in Figure 4.11(b) shows a plot of the constant potential contours for potentials directly beneath the tip at the interface between the nanowire and the oxide for each of the simulated tip–contact distances and tip potentials. Figure 4.11(b) shows a line of constant nanowire surface potential; in this case, the surface potential is 2 V and the applied tip voltage required to reach this potential value at the nanowire surface is plotted versus distance. The potential seen on the wire surface can deviate substantially from the potential applied to the tip, as evident in the inset of Figure 4.11(b). This effect is especially noticeable as the tip nears the contact. For distances less than one micron, the screening effect is such that the potential at the wire surface can be reduced by 60 % or more compared to the tip potential. This situation is somewhat analogous to drain induced barrier lowering seen in planar, short–channel metal–oxide–semiconductor field–effect transistors (MOSFETs).[40] Figure 4.11(b) demonstrates that in order to maintain a constant surface potential, as is required to operate a field effect transistor in any bias range (e.g. accumulation, depletion, or inversion), it is necessary to apply an exponentially increasing amount of voltage to the gate as the gate–source separation is decreased. Normally, there should be a voltage drop across the oxide which would never allow the potential at the wire–oxide interface to reach the potential on the metal gate. The dependence of this voltage drop on tip–contact distances, as shown in Figure 4.11(b), demonstrates that a dramatic electrostatic screening effect is present and that there is a highly nonlinear increase in the amount of electrostatic screening as the probe tip is moved closer to the large metallic contact. Figures 4.12 (a) and

4.12(b) show density plots of potential slices through the apex of the wire and tip along the axial direction of the wire with the tip grounded and the source electrode at 2 V when the tip is positioned 5 μm and 1 μm away from the contact–nanowire interface, respectively. The potential profiles show an exponential increase in potential as a function of position between the contact and the probe in Figures 4.12(a) and 4.12(b), and the decay length of that increase is nonlinearly dependent on the distance between the probe and the contact. The voltage drop across the oxide also scales nonlinearly as a function of the separation distance between contact and probe.

In order to achieve a given surface potential for the nanowire, one must apply a voltage to the tip that varies strongly with the distance separating the contact and the tip. In an idealized case of no screening, the voltage drop across the oxide would be constant regardless of the distance between the tip and the contact. These results demonstrate that the geometry of the contacts has a dramatic influence on screening of nanoscale contacts for a geometry similar to that of a nanowire field–effect transistor. A decrease in only the cross–sectional area of the contact facing the nanowire, and not necessarily the total volume of the contact, should reduce the amount of coupling that the large contact has on the device. The effect of changing the source geometry is demonstrated in simulations of devices with smaller contacts. Replacing the 7 μm by 3 μm by 70 nm contact in our simulations with a contact that is 100 nm by 3 μm by 70 nm dramatically reduces the screening effect, as demonstrated by the dashed line in Figure 4.11(b).

Charge transfer due to the difference in work function between the metal contact and the semiconductor nanowire can also result in an inhomogeneous potential profile along the nanowire,[9] which could be an alternate explanation for the trend seen in the data. This effect would persist regardless of the contact geometry and/or the presence of a scanning probe tip and is dependent only on the work function difference between the metal and the semiconductor. Thus, the variation of the effect with contact geometry, as shown in the simulations, and the SCS curve broadening near the contact suggest that the effect is more likely a result of contact potential screening. Other experimental results in the literature suggest that screening can be significantly reduced with a change in the gate and/or source/drain geometry as shown recently in studies revealing a reduction in the parasitic effects of source/drain field coupling to the nanowire by making nickel silicide source and drain contacts to group IV core–shell nanowires.[41] These effects are expected to have substantial implications for the design and performance of nanowire–based electronic devices, most notably nanowire field–effect transistors. More generally, these results are indicative of the importance of assessing and accounting for the effect of large–scale contact and circuit elements on the characteristics of nanoscale electronic devices.

4.9 Conclusion

In summary, we have used AFM, SCM, SCS, and finite–element electrostatic simulations to characterize and analyze the effects of micron–sized contacts to InAs nanowire devices in producing strong electrostatic potential screening that can have severe deleterious effects on nanowire device performance. A screening effect was

directly observed and found to shift the threshold voltage of the devices by several volts over distances of several microns. The screening effect was established to be present on multiple nanowires with differing contact geometries. This effect should not be limited to InAs and should persist in any semiconductor material system. Through simulation, these observations were shown to be a direct result of the relative size of the nanowire compared to the contact and the shape of the probe–tip gate. A simulated reduction in the cross–sectional area of the contact helped suppress the screening effect, consistent with behavior seen in recently reported experiments. These results have implications for the design and performance of a variety of nanowire–based electronic devices. Moreover, the results highlight the importance of understanding and accounting for the electrostatic interaction between nano– and macrosized objects in nanoscale devices.

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