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Electronically Reconfigurable Circuits for Millimeter-Wave and Beyond

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Tissana Kijsanayotin

Committee in charge:

Professor James F. Buckwalter, Chair
Professor Peter M. Asbeck
Professor Gert Cauwenberghs
Professor Chung-Kuan Cheng
Professor Gabriel M. Rebeiz

2015

The dissertation of Tissana Kijsanayotin is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2015

To grandma, whose love transcends distance and time.

EPIGRAPH

Vulnerability is the birthplace of creativity, innovation, and change.

—Brené Brown

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The material in this dissertation is based on the following manuscripts which are either published, submitted, or in preparation for publication. Chapter 2 is partially a reprint of the material as it appears in IEEE MTT-S International Microwave Symposium Digest (IMS), 2013, T. Kijsanayotin; J. F. Buckwalter and IEEE Transactions on Microwave Theory and Techniques, 2014, T. Kijsanayotin; J. F. Buckwalter. Chapter 3 and 4 are mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, 2014, T. Kijsanayotin; J. F. Buckwalter. The material in Chapter 5 is submitted for publication on IEEE Transactions on Microwave Theory and Techniques, 2015, T. Kijsanayotin; J. Li; J. F. Buckwalter. The material in Chapter 6 is in preparation for submission to the IEEE Transactions on Microwave Theory and Techniques, T. Kijsanayotin; K. N. Madsen; J. F. Buckwalter.

The dissertation author was the primary author of these materials, and co-authors have approved the use of the material for this dissertation.

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PUBLICATIONS

T. Kijsanayotin, K. Madsen, and J. F. Buckwalter, "A 50 GS/s Track-and-Hold Amplifier in 90-nm SiGe BiCMOS", *in preparation for IEEE Transaction on Microwave Theory and Technique.*

T. Kijsanayotin, J. Li, and J. F. Buckwalter, "A 70 GHz, LO Phase-Shifting, Bidirectional Front-End Using Linear Coupled Oscillators", *submitted to IEEE Transaction on Microwave Theory and Techniques*, October 2015.

P. Wu, T. Kijsanayotin and J. F. Buckwalter, "A 71–86-GHz, Switchless, Asymmetric Bidirectional Transceiver in 90-nm SiGe BiCMOS", *submitted to IEEE Transaction on Microwave Theory and Techniques*, September 2015.

T. Kijsanayotin, J. Li, and J. F. Buckwalter, "A 70 GHz Bidirectional Front-End for a Half-Duplex Transceiver in 90-nm SiGe BiCMOS', in *IEEE Compound Semiconductor Integrated Circuit Symposium Digest*, 2015.

T. Kijsanayotin and J. F. Buckwalter, "Millimeter-Wave Dual-Band, Bidirectional Amplifier and Active Circulator in a CMOS SOI Process", *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 3028-3040, December 2014.

T. Kijsanayotin and J. F. Buckwalter, "A 40/85 GHz Dual-Band Bidirectional Variable Gain Amplifier", in *IEEE MTT-S International Microwave Symposium Digest*, 2013.

T. Kijsanayotin and J. F. Buckwalter, "A 60 GHz BiFET Constructive Wave Power Amplifier", in *IEEE MTT-S International Microwave Symposium Digest*, 2012.

ABSTRACT OF THE DISSERTATION

Electronically Reconfigurable Circuits for Millimeter-Wave and Beyond

by

Tissana Kijsanayotin

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2015

Professor James F. Buckwalter, Chair

Millimeter-wave (mm-Wave) wireless communication systems often employ phased array architecture to overcome the high path loss and to provide spatial selectivity. As the number of elements in the array increases, the complexity as well as physical area required for the circuitry also increase. This calls for circuit blocks that are multifunctional and can be electronically reconfigured. This dissertation presents the analyses, designs and implementations of electronically reconfigurable circuit blocks that operate bidirectionally and at multiple frequency bands.

The first part of the dissertation discusses three mm-Wave reconfigurable circuit blocks realized using the constructive wave amplification technique (CCWA) in both SiGe BiCMOS and CMOS SOI processes. First, a power amplifier is de-

signed at 60 GHz in a 0.12-μm SiGe BiCMOS process that incorporates a CMOS-bipolar cascode (BiFET) feedback circuit topology. Second, a dual Q- and W-band, bidirectional amplifier is demonstrated in a 45-nm CMOS SOI process where operations at different bands and directions are realized by electronically configuring the feedback "field of FETs". The bidirectional concept is then extended to the design of a three-port V-band reconfigurable active circulator that directs traveling waves between different pairs of ports while providing isolation from the remaining ports.

Secondly, a switchless bidirectional front-end architecture is demonstrated in a 90-nm SiGe BiCMOS process. The proposed architecture enables a time-division duplexed (TDD) operation without the use of high-speed transmit and receive (T/R) switch. A passive transmission line matching network is used to isolate the power amplifier and low-noise amplifier and a bidirectional passive mixer is used for up- and down-conversion of the signal. The front-end is incorporated to a two-element linear coupled oscillator array to form a local oscillator beamforming transceiver.

Finally, a high-speed track-and-hold amplifier (THA) is demonstrated in a 90-nm SiGe BiCMOS process. This work demonstrates the competitiveness of advance integrated silicon processes when being benchmarked against high performance III-V processes. The continuous improvement of silicon-based transistors will allow integrated systems to operate at higher frequencies. All the circuits techniques present in this dissertation are applicable to the design at mm-Wave and beyond.

Chapter 1

Introduction: High-Speed Millimeter-Wave Wireless Communication

Rapid increases in demand for high data rate wireless communication in the past decade can largely be attributed to the popularity of the smart mobile devices. Many innovative solutions in both complex digital modulation techniques that aim to put more data in a limited amount of bandwidth and the multiple-input multiple-output (MIMO) systems that make use of the multipath effect have been employed to improve link capacity. However, these solutions only provide marginal improvements that does not coincide with the rate of growth in demand.

Shannon's Theorem states that channel capacity (C) is related to the channel bandwidth (BW), and the signal-to-noise ratio (SNR) as [3]

$$C = BW \log_2(1 + SNR) \qquad (1.1)$$

which suggests a simple solution: increase bandwidth to increase capacity. However, the traditional RF frequency bands (1–10 GHz) have become very congested and the cost of licensing to operate in these frequencies is large. Worse yet, it is very difficult to obtain a large amount of continuous bandwidth since the spectrum allocated are split into small, often 10–20 MHz wide channels. Where then can a large, continuous bandwidth be found?

1.1 Millimeter-Waves for Wireless Communication

Millimeter-wave (mm-Wave) frequency bands have emerged as a particularly attractive solution for this problem due to the large amount of continuous bandwidth available with minimal interference. Many mm-Wave frequency bands have been allocated for high data rate wireless communication systems as illustrated in Fig. 1.1. Q-band (33–50 GHz) is used for satellite communication and defense [4]. 60 GHz band is unlicensed and has been commercialized for short range, multi-gigabit communication systems for home (IEEE 802.11ad, WirelessHD) [5,6]. High capacity backhaul and mobile broadband are being explored in E-band (71–76 and 81–86 GHz) as a possible solution for the "last mile" gap [7,8]. The 77 GHz band is used for high resolution automotive radar for adaptive cruise control and collision avoidance [9,10]. Finally, W-band (92–95 GHz) is also used for point-to-point links [11] as well as passive imaging systems [12,13].
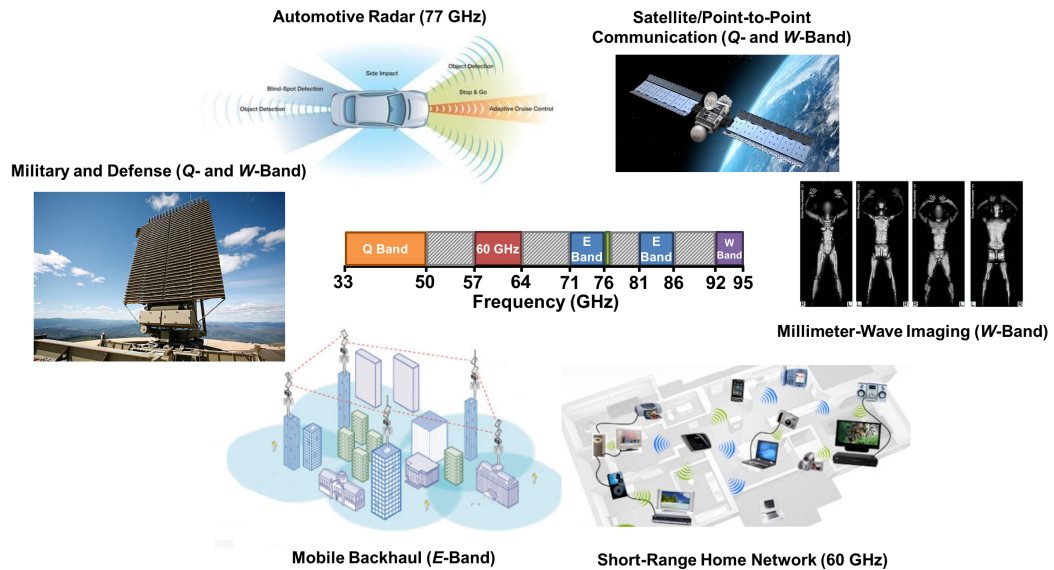
Figure 1.1: Millimeter-wave frequency bands and the different applications.

One of the challenges that comes with operating at high frequency is the increase in path loss. Friis transmission formula shows that the power available at

the receiving antenna (P_R) in relation to the transmit power (P_T) is

$$P_R = G_T G_R \left(\frac{\lambda}{4\pi R}\right)^2 P_T \tag{1.2}$$

which is directly proportional to the square of the wavelength (λ) and gain of the transmit and receive antennae (G_T) and (G_R). As a result, for a given distance between the transmitter and the receiver, the received signal at higher frequencies will experience higher attenuation due to the smaller wavelengths. Additionally, high frequency signals also experience additional attenuation from the atmosphere as shown in Fig. 1.2 [14]. These losses directly affected the SNR and ultimately reducing the link capacity.
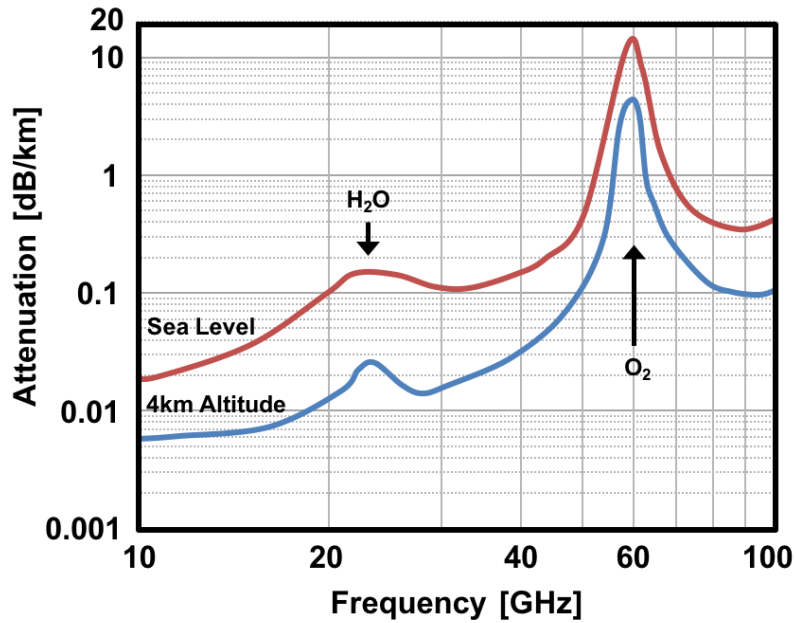
Figure 1.2: Atmospheric absorption as a function of frequency.

There are several ways to overcome the high path loss. First, the transmit power can be increased. However, this is difficult because the power handling capability of active devices also degrades at high frequency. Another way is to increase the antenna gain by means of beamforming using phased array. This is advantageous because mm-Wave antenna arrays can be realized on printed circuit board or even directly on the die due to the small wavelength. The array also provide

spatial diversity which help reducing the effect of multipath fading. As a result, many demonstrations of the mm-Wave communication systems both commercially and in research literatures employ the beamforming architecture.

1.2 Silicon Technologies for mm-Wave Designs

mm-Wave circuits have historically require III-V technologies such as gallium arsenide (GaAs) or indium phosphide (InP) due to the good high frequency performance of the devices. However, the high cost of these technologies prohibits large-scale manufacturing and commercialization of mm-Wave systems. Aggressive geometry scaling, although largely driven by the needs of digital applications, has improved the high frequency capabilities of silicon-based devices. This advancement made possible for CMOS and silicon germanium heterojunction bipolar transistor (SiGe HBT BiCMOS) technologies to be used in mm-Wave designs.

1.2.1 CMOS Devices
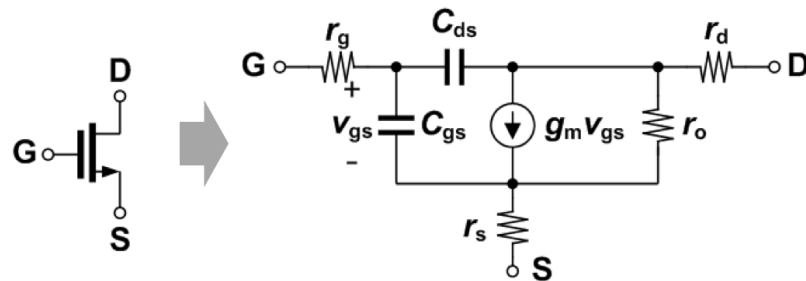
Figure 1.3: High frequency small-signal model of a CMOS device.

The scaling of CMOS devices follow the well-known Moore's Law, leading to increased integration and improved performance. The unity current gain frequency (f_t) is often used as a figure of merit (FOM) to compare high frequency performance of the device. f_t can be derived using the small-signal model shown in Fig. 1.3 as

$$\frac{1}{2\pi f_{t,MOS}} = \frac{C_{gs} + C_{gd}}{g_m} + C_{gd}\left(r_s + r_d\right) \tag{1.3}$$
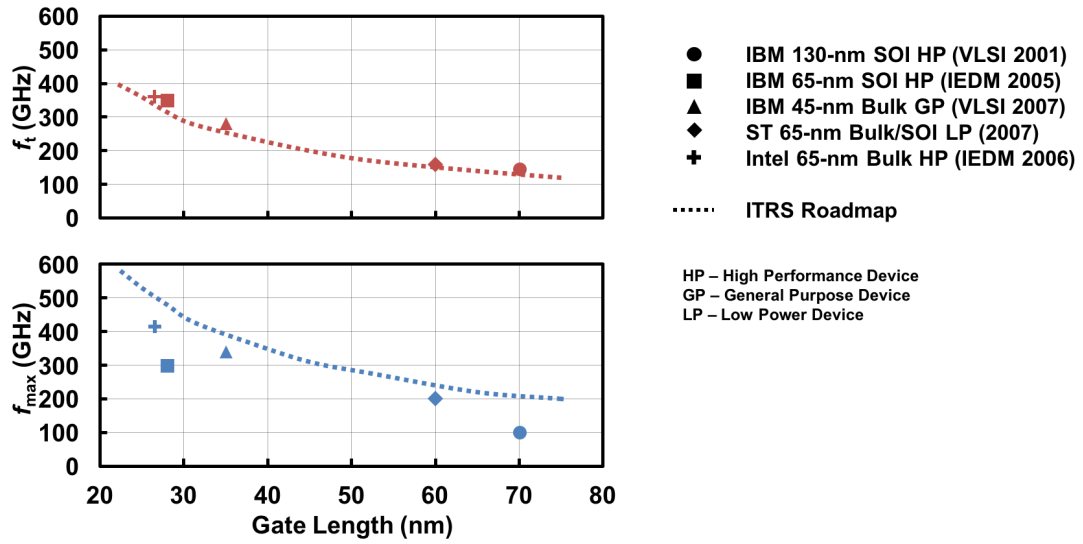
Figure 1.4: f_t and f_{max} as a function of effective channel length for different technology nodes and the ITRS roadmap [1].

which suggests that f_t increases as the gate length reduces due to the increase in device transconductance (g_m) [1]. It is also worth noting that parasitic drain and source resistances r_d and r_s act as degeneration, resulting in a degradation in f_t. The contribution from these resistances can be as much as 15–20% of the intrinsic cutoff frequency $f_c = g_m \backslash (C_{gs} + C_{gd})$ [15]. It is also apparent from (1.3) that f_t does not depend on the gate resistance and the output impedance of the device.

Power gain also plays an important role in high frequency design. The maximum oscillation frequency (f_{max}) is defined as the frequency at which the maximum available power gain (MAG) of the device is 1 and can be approximately expressed as [15]

$$f_{max,MOS} = \frac{f_{t,MOS}}{2\sqrt{(r_s + r_g)/r_o(1 + g_m r_s)}} \qquad (1.4)$$

State-of-the-art CMOS and CMOS silicon-on-insulator (SOI) has been shown by the foundries to have f_t and f_{max} in excess of 300 GHz. Fig. 1.4 shows the f_t and f_{max} performance with respect to the effective gate length of the CMOS device from different foundries along with the International Technology Roadmap for Semiconductor (ITRS) roadmap published in 2006 [16].

It is important to note that interconnect parasitics can have significant effect on the actual device performance at mm-Wave. An IBM 45-nm CMOS SOI process have been shown to have a measured f_t and f_{max} of around 200 GHz when all the interconnect parasitics are taken into account [17]. Therefore, careful characterization of the back-end-of-line (BEOL) through electromagnetic (EM) simulation must be done to ensure the correct device performance at mm-Wave.

1.2.2 SiGe HBT Devices
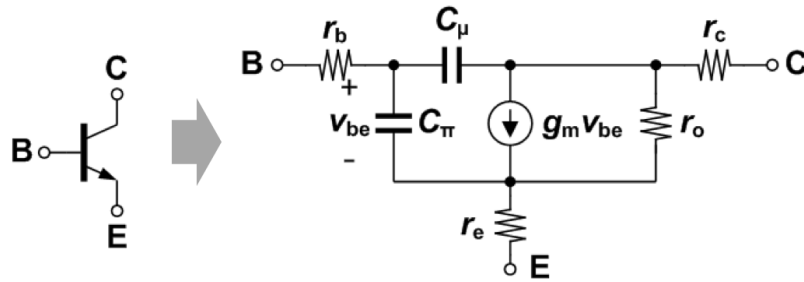
Figure 1.5: High frequency small-signal model of a HBT device.

Heterojunctiion bipolar transistors offer several benefit compared to CMOS devices such as high voltage handling capability, high output impedance, and low $1/f$ noise [18]. Fig. 1.5 shows the small-signal model of the HBT device. Similar to the CMOS device, $f_{t,\mathrm{HBT}}$ and $f_{\max,\mathrm{HBT}}$ can be expressed as

$$\frac{1}{2\pi f_{t,\mathrm{HBT}}} = \frac{C_\pi + C_\mu}{g_m} + C_\mu \left(r_e + r_c\right) \tag{1.5}$$

$$f_{\max,\mathrm{HBT}} = \frac{f_{t,\mathrm{HBT}}}{2\sqrt{\left(r_e + r_b\right)/r_o\left(1 + g_m r_e\right)}} \tag{1.6}$$

For a given bias current, a bipolar device have a higher g_m when comparing to a MOS due to its exponential IV characteristics. In fact, SiGe HBT can achieve comparable or better performance to a NFET device at twice the minimum feature size. For example, a measured f_t and f_{max} of 270 and 360 GHz has been shown for the IBM 90-nm SiGe BiCMOS process [19]. This relaxation in lithography dimension can make the cost comparable to that of the state-of-the-art CMOS processes.
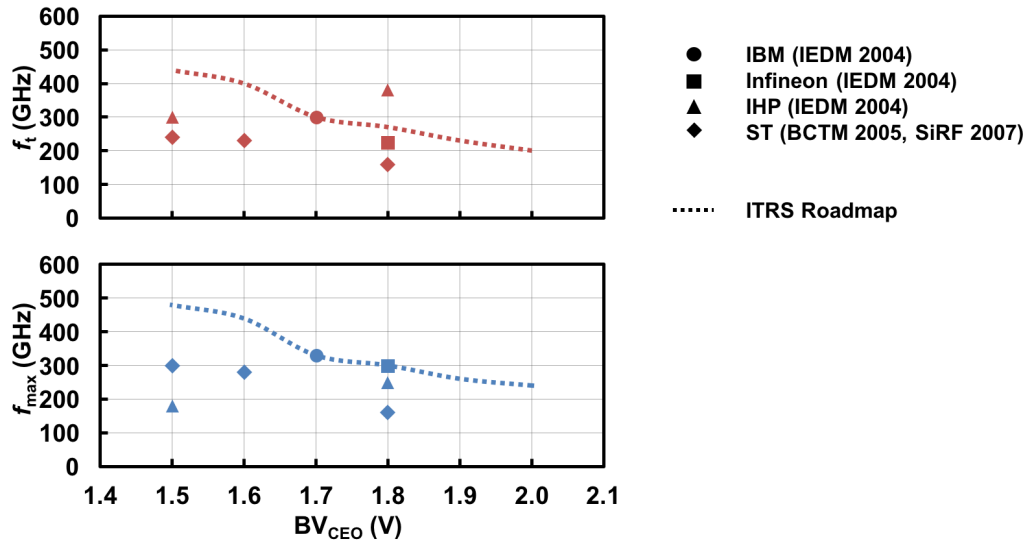
Figure 1.6: f_t and f_max as a function of BV_CEO for different technology nodes and the ITRS roadmap [2].

Fig. 1.6 shows the f_t and f_max performance from several foundries as a function of the base-emitter breakdown voltage BV_CEO and the ITRS roadmap. Advanced SiGe BiCMOS processes can have f_t that is comparable to that of III-V transistors. In this dissertation, the performance of a 90-nm SiGe HBT is benchmarked directly against InP dual-heterojunction bipolar transistor (DHBT) through the design of a high-speed track-and-hold amplifier (THA).

1.3 Electronically Reconfigurable Circuits for mm-Wave Applications

As previously mentioned, many mm-Wave communication systems employ beamforming architecture. These beamforming transceivers are highly integrated and as the number of transceiver element increases, so does the complexity as well as area and cost of the system. Additionally, as mm-Wave phased array systems evolves, circuit blocks will need to operate in multiple frequency bands to determine the best channels. As a result, mm-Wave silicon integrated circuits realized are particularly port limited, placing a premium on circuit design techniques which

minimize the number of transitions to a package or on-chip antennae. This dissertation presented several circuit techniques that aim to combine the function of the circuit blocks in the transmit and receive path into several bidirectional circuit blocks that can be electronically controlled to realized a specific operation.

1.3.1 Cascaded Constructive Wave Amplification-based Circuits

The cascaded constructive wave amplification technique (CCWA) is a traveling wave amplification technique that consists of a single transmission line between the input and the output around which active feedback circuits are shunted [20]. The active feedbacks establish directionality to the transmission line by amplifying the signal in one direction while simultaneously attenuating the signal traveling in the opposite direction. High gain can be achieved by cascading multiple constructive wave stages. The CCWA also offers a unique benefit of broadband matching to the loads since it effectively looks like a periodically loaded transmission line. In this dissertation, the CCWA technique is leveraged to implement three different mm-Wave reconfigurable circuits in both SiGe BiCMOS and CMOS SOI processes at multiple frequency bands.

First, a constructive wave power amplifier (CWPA) is demonstrated at 60 GHz in a 0.12-μm SiGe BiCMOS process. Previous demonstrations of the CCWA have used a two-stage emitter-follower, common-emitter cascade as a feedback circuit [20–22]. This structure is not optimized for high power handling and the two stage feedback greatly reduces the amplifier efficiency. Here, a common-source NFET and common-base HBT cascode (BiFET) feedback circuit which combines the high-impedance and thermal stability of the common-source NFET with the high breakdown behavior of the HBT is used to demonstrates the power handling and efficiency limits of the CWPA. The proposed amplifier remains operational when one or more stages degrade in performance as the remaining stages can be electronically tuned to compensate for the malfunctioning stages.

Second, a dual Q- and W-band bidirectional variable gain amplifier is demonstrated in a 45-nm CMOS SOI process. Multi-band amplifiers typically

use switched passive elements to realize a tunable load [23–26]. Load switching at mm-Wave bands introduce a severe performance penalty as the parasitics become significant in conjunction with the lower quality factor (Q) of the passives. Similarly, conventional bidirectional amplifiers comprise separate amplifying elements and switches to isolate the PA and the LNA [27]. These high-speed transmit/receive (T/R) switches tend to incur high loss [28–30] in highly-scaled silicon processes. The amplifier proposed here realizes a dual-band, bidirectional operation by a network of active devices on the transmission line to control the traveling waves, thereby eliminating the need for high-speed switches. The amplifier gain and isolation can also be adjusted electronically.

Finally, a V-band reconfigurable active circulator is demonstrated in a 45-nm CMOS SOI process. A circulator is three-port device that directs energy from one port to a neighboring port in only one direction. For simultaneous transmit and receive operation, a circulator isolates the transmit and receive path. Because a circulator is a non-reciprocal device, it can only be realized using non-reciprocal components. Traditional circulators are passive devices that rely on physical properties of ferromagnetic materials. These circulators have low insertion loss and high power handling but are large and difficult to integrated with silicon circuits. Earlier work [31–34] has demonstrated that active devices can be used to implement the circulator function. These active circulators are fully integrated, compact in size, and can maintain a relatively large fractional bandwidth at high operating frequencies. However, they do not allow for full circulation or any control over the direction of circulation. An active circulator proposed here not only provides complete circulation of the signal, but also can be electronically reconfigured to circulate in both directions.

1.3.2 Local Oscillator Phase-Shifting, Switchless mm-Wave Bidirectional Front-End Using Linear Coupled Oscillators

Half-duplex systems such as a time-division duplexed (TDD) communication and pulse-compression radar (PCR) [35] systems share a single antenna and requires a T/R single pole double throw (SPDT) switch to isolate the power amplifier (PA) and the low-noise amplifier (LNA). mm-Wave SPDTs have been demonstrated both in silicon [28–30] and as external MEMS devices [36]. Silicon-based switches, while more cost effective, suffer from high insertion loss, poor power handling, and poor linearity performance at mm-Wave frequencies. MEMS switches have better performance but requires additional back-end processing and thus do not easily integrated with the front-end circuitry.

In a linear array, a phase progression between each transceiver element is achieved in the signal path at RF [37] or through the local oscillator (LO) path [38, 39]. RF phase shifting has the benefit of excellent jammer rejection [40] but requires high-linearity phase shifters and power combiners/dividers and higher power consumption since the circuits are operating in the RF band. LO phase shifting eliminates the phase shifter in the RF path in favor of a phase shifter at the LO frequency. The distribution of LO to multiple mm-Wave front-ends in silicon requires LO phase rotators close to the mixer in order to maintain accurate phase relationship between each path [38].

An alternate method for generating a linear LO phase progression is by using bilateral coupled oscillators which was demonstrated in a discrete receiver [41]. The advantage of this architecture is that a continuous phase progression across the array occurs by controlling the oscillation frequency of only the edge elements. Additionally, the coupling array can be scaled linearly either on-chip or possibly from chip-to-chip [42]. Finally, the phase range can be increased using a frequency multiplier [43].

This dissertation proposes alternative approach in the front-end design by combining the transmit and receive path through the use of bidirectional circuit

blocks. A transmission line-based impedance transformation network is designed to provide isolation between the PA and LNA under different biasing condition, eliminating the need for the T/R switch at the front-end. The passive mixer is used for bidirectional up/down conversion of the signal. The switchless front-end is then integrated with a 2-element linear coupled oscillator array to demonstrate the beamforming capability by LO phase shifting. The prototype circuit is implemented in a 90-nm SiGe BiCMOS process and operated at 70 GHz.

1.4   Dissertation Organization

Background materials and motivation for electronically reconfigurable circuitry for mm-Wave applications has been mentioned in this first chapter.

Chapter 2 introduces the theory of operation of the cascaded constructive wave amplification (CCWA) technique and describes the design of the 60 GHz BiFET constructive wave power amplifier in a 0.12-μm SiGe BiCMOS process. The four-stage amplifier operates from 52–62 GHz with a peak small-signal gain of 10.7 dB at 60 GHz. Peak output saturation power (P_{sat}) is 16.4 dBm with associated power-added efficiency of 15.3%. The amplifier nominally consumes 52 mW (4 V $\times$ 0.13 mA) and the active area occupies only 0.074 mm^2 of die space.

The design of the dual Q- and W-band bidirectional variable gain amplifier and the device and passive characterization of a 45-nm CMOS SOI process is described in Chapter 3. The dual-band, bidirectional amplifier operates at 40 and 81 GHz, with peak gain of more than 4.2 dB in all modes of operation. The gain of amplifier is electronically tunable and the maximum gain and isolation variation of 20 dB is achieved. Linearity measurement at the 40 GHz band shows the amplifier has a peak P_{sat} of 3.9 dBm with an output 1-dB compression point (OP1dB) of 2.9 dBm and an output third-order intermodulation intercept point (OIP3) of 7.3 dBm. A minimum noise figure of 9 dB is measured at 38 GHz.

In Chapter 4, the V-band reconfigurable active circulator in a 45-nm CMOS SOI process is demonstrated. A small-signal scattering matrix of the circulator

is developed and 3-port stability analysis is presented. The active circulator is reconfigurable to operate in four different modes of operation: clockwise, counter-clockwise, quasi-circulation, and as a thru between port 1 and port 2. The circulator is measured to have an insertion loss of 7.4 dB with isolation between any pair of isolated ports better than 18 dB from 62–75 GHz.

A 70 GHz, LO phase-shifting, switchless bidirectional front-end using linear coupled oscillators in a 90-nm SiGe BiCMOS process is presented in Chapter 5. The bidirectional front-end operation relies on the switching of bias circuitry of the transmit and receive paths. Isolation between the PA and the LNA is achieved by using passive impedance transformation network which eliminates the need for the mm-Wave T/R switch. The transmitter has a measured peak P_{sat} of 7.2 dBm and a peak conversion gain of 14.5 dB while consuming 47 mA from a 1.8 V supply. The receiver has a peak conversion gain of 9.9 dB and a minimum noise figure of 8.6 dB with nominal current consumption of 18 mA from a 1.5 V supply. The front-end is integrated with a 2-element linear coupled oscillator array each consisting of a voltage-controlled oscillator (VCO), a frequency multiplier chain, and buffers. Each coupled oscillator chain nominally consume 117 mW from 1.4 V and 2 V supplies. The 2-element transceiver achieves a maximum phase scanning of $\pm 80°$.

Finally, a 50 GS/s track-and-hold amplifier (THA) in Chapter 6 demonstrates the practicality of using a SiGe BiCMOS process for high-speed, mm-Wave applications. The theory of operation of a THA is briefly reviewed and measurement result is presented. The 50 GS/s THA has a small signal 3-dB bandwidth of 25 GHz with an input range of 1 V_{pp} differential. The measured third harmonic distortion (HD3) is better than -40 dB up to 15 GHz input. Maximum input-referred 1-dB compression point (IP1dB) and third order intercept point (IIP3) are 5 dBm and 17.3 dBm, respectively. The THA demonstrates the sampling speed that is comparable with the reported state-of-the-art III-V InP DHBT THAs while consuming only 2.5 times less power.

Chapter 2

Constructive Wave Amplification for mm-Wave Power Amplifier

The cascaded constrictive wave amplification (CCWA) technique is a traveling wave amplification technique that consists of a single transmission line between the input and the output loaded with a series of shunt-shunt active feedback networks [20]. The active feedbacks add a small amount of energy to the traveling wave and establish directionality to the transmission line by amplifying the signal traveling in one direction and attenuate the signal traveling in the opposite direction. A block diagram of the CCWA is illustrated in Fig. 2.1.

The CCWA offers several benefits over other traveling wave amplification techniques. First, the use of a single transmission line implies an overall area reduction. Second, the gain is multiplicative as the number of stage increases unlike conventional distributed amplifier [44] where the gain is additive. Third, the amplifier provides a broadband matching to the loads since it looks like a periodically loaded transmission line. Finally, unlike traditional amplifier where the signal gets absorbed and then regenerated by the transistor, the signal travels uninterruptedly along the transmission line and the amplifier remains operational when one or more active feedback stages degrade in performance or malfunction.
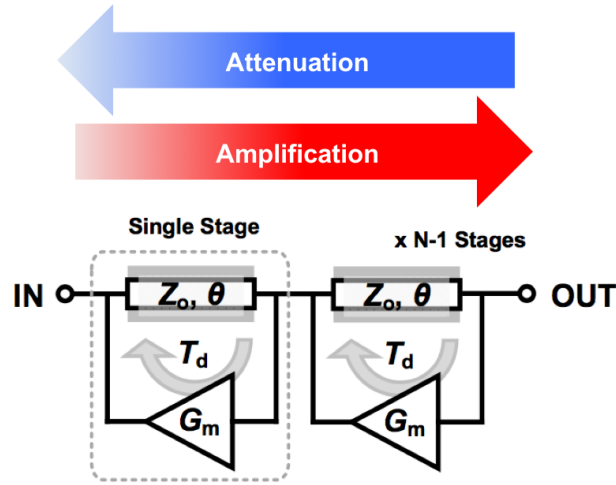
Figure 2.1: Block diagram of an N-stage cascaded constructive wave amplifier.

2.1 Principle of Operation

The equivalent circuit of an ideal single constructive wave stage is illustrated in Fig. 2.2. The amplifier stage comprises a transmission line with characteristic impedance Z_{o} and relative phase θ and an active *unilateral* feedback circuit modeled by an effective transconductance G_{m} with a finite feedback time delay T_{d}. In order for constructive interference to occur in the forward direction and destructive interference in the reverse direction, the transmission line length and feedback time delay must be designed such that $\theta + \omega_{\mathrm{o}} T_{\mathrm{d}} = \pi$ and $\theta - \omega_{\mathrm{o}} T_{\mathrm{d}} = 0$. In other words, the phase delay through the transmission line and the feedback amplifier are 90° at the center frequency of the amplifier ($f_{\mathrm{o}} = 1/4T_{\mathrm{d}}$ and $\theta = 90°$). The transmission line phase delay can be obtained by using a $\lambda/4$ section. The feedback voltage gain is determined by the product of the transconductance and the transmission line impedance ($A_{\mathrm{v}} = G_{\mathrm{m}} Z_{\mathrm{o}}/2$). The magnitude of the S-parameters can be expressed in terms of the feedback voltage gain as

$$|S| = \begin{bmatrix} \dfrac{A_v}{1 - A_v} & \dfrac{1 - 2A_v}{1 - A_v} \\ \dfrac{1}{1 - A_v} & \dfrac{A_v}{1 - A_v} \end{bmatrix}. \tag{2.1}$$
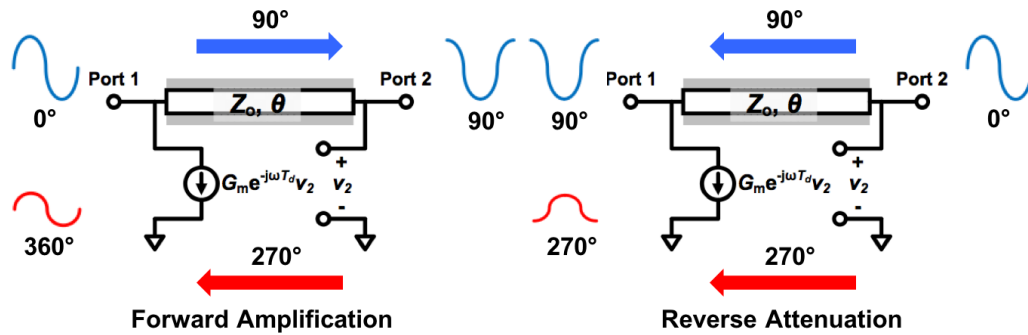
Figure 2.2: Small-signal equivalent circuit of a single constructive wave stage with the phase conditions for forward amplification and reverse attenuation.
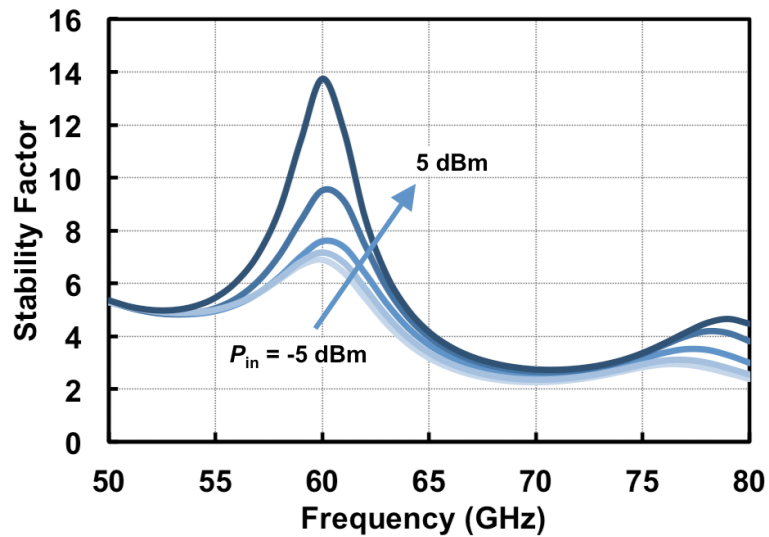
Figure 2.3: Large-signal S-parameters (LSSP) simulation of the stability factor (μ) of a 4-stage constructive wave amplifier.

Complete cancellation of the backward traveling wave (S_{12}) occurs when $A_v = 1/2$ while the forward transmission (S_{21}) is 2. The phase conditions and S-parameters in (2.1) suggest that the amplification happens through positive feedback of the wave from the output to the input of the stage. Input and output return losses (S_{11} & S_{22}) are inversely proportional to A_v and are equal to 1 when $A_v = 1/2$. In the limit of $A_v = 0$, the response in (2.1) resembles an ideal transmission line.

Stability factor (μ) of the stage can be expressed as

$$\mu = \frac{(1 + \alpha l)(1 + \alpha l - 2A_v)}{2\alpha l A_v + \left|1 - (\alpha l)^2 - 2A_v\right|} \tag{2.2}$$

where αl denotes the loss in the transmission line. It has been shown in [20] that in order to ensure unconditional stability, the feedback voltage gain must be bounded by $A_v \leq 1/2$. This serves as a practical limit for the feedback network design. As the input power increases, the traveling wave stage becomes more stable due to the compression of the active devices in the feedback amplifier. Fig. 2.3 shows the large-signal S-parameters (LSSP) simulation of the stability factor of a 60 GHz, 4-stage constructive wave amplifier at various input power levels.

The analysis of the constructive wave stage so far has ignored capacitive loading and assumed a unilateral feedback network. The small signal model presented in Fig. 2.4 must be carefully reconsidered for mm-Wave design to bound the tolerable loading and feedback capacitances. The plot in Fig. 2.4 shows the effect of increasing the loading and feedback capacitances C_L and C_f. Both capacitances introduce similar problems; the gain shifts to lower frequencies, the 3-dB bandwidth is reduced, and the matching degrades at high frequencies. This result suggests that the feedback network must be designed to have high input and output impedances and a two-stage feedback amplifier is required for isolation of the feedforward capacitance.

2.2 60 GHz Constructive Wave Power Amplifier

Earlier implementations [20–22] of the constructive wave amplifier in a SiGe BiCMOS process use a two-stage network realized with a cascaded emitter follower
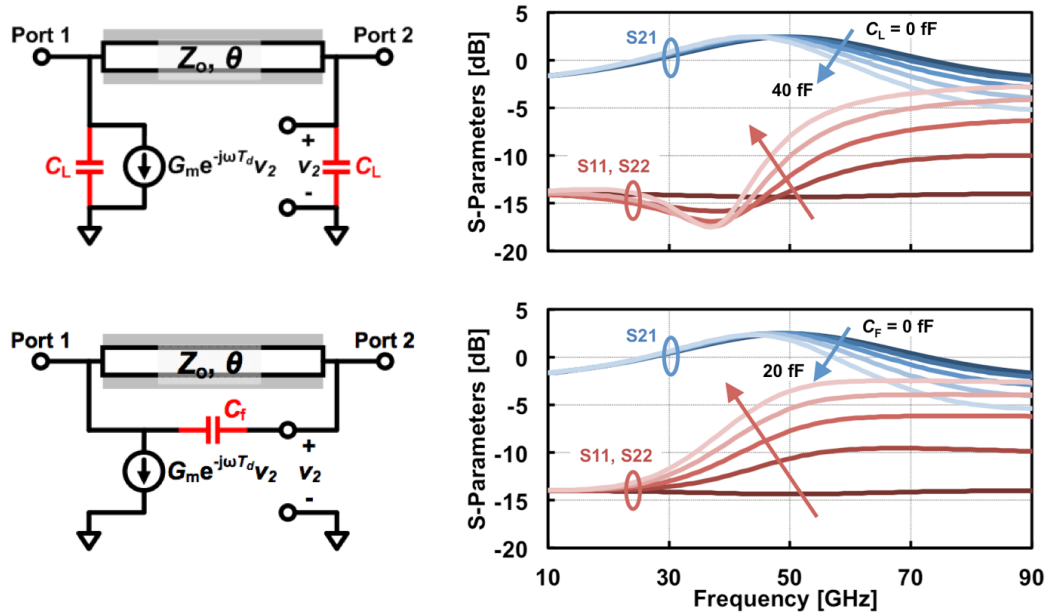
Figure 2.4: Small-signal model of a single constructive wave stage with loading capacitance (C_L) and feedback capacitance (C_f) and their effect on the single constructive wave stage response.

and common-emitter amplifier with emitter degeneration to satisfy the unilateral and time delay conditions imposed on the feedback network. The emitter follower provides a high impedance along the transmission line and a low impedance termination for the feedforward capacitance of the common-emitter stage while the degeneration of the common-emitter provides high output impedance. However, there are several drawbacks in this structure that make it not suitable for a power amplifier design. First, the cascaded feedback amplifier has two DC paths which greatly reduce overall efficiency. Second, the feedback network is not optimized for high power handling. Finally, the emitter follower stage is DC coupled to the transmission line where the swing of the traveling wave can put the emitter-follower device into saturation. This problem is more severe at the latter stages of the amplifier.

For the design of a 60 GHz power amplifier, a cascode topology offers the similar isolation to satisfy the unilateral condition as well as the control of the
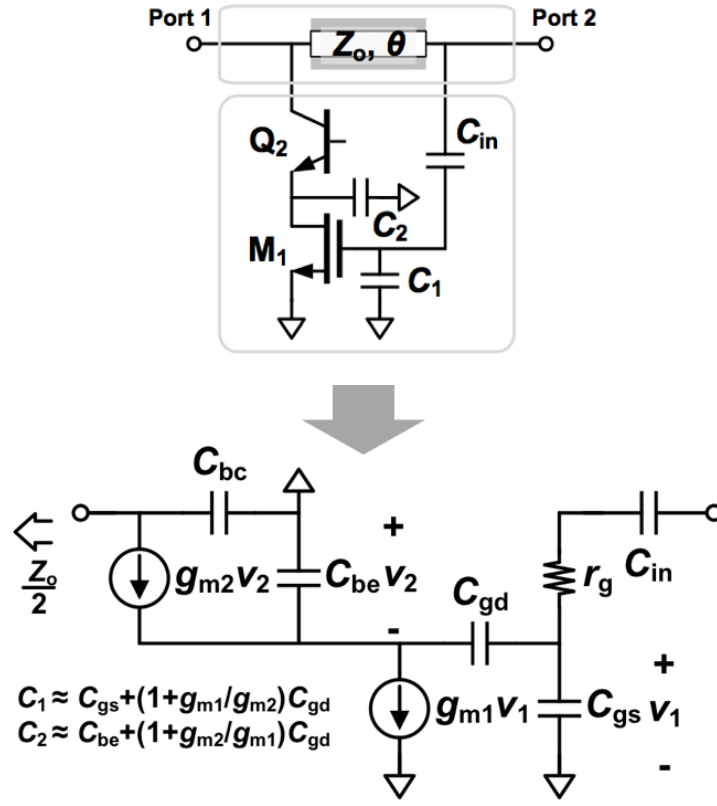
Figure 2.5: The NFET-HBT BiFET cascode feedback circuit and its small-signal model.

amplifier time delay. The cascode in a BiCMOS process is realized with a common-source NFET and a common-base HBT (BiFET) as shown in Fig. 2.5. Different permutations of the BiFET structure has been used in both low frequency LNA (HBT-NFET) [45] and wideband distributed power amplifier (NFET-HBT-HBT) designs [46]. The NFET-HBT BiFET structure is chosen for this design for several reasons.

First, the transconductor experiences a large voltage swing at the input of the device while the swing at the intermediate node is small due to the low impedance presented by the cascade device. Using a HBT as the transconductor is undesirable because when the input is high, the HBT will go into saturation region which takes a longer time to recover to a forward active mode comparing to

an NFET moving from triode to saturation. Additionally, while the NFET in this process ($L_\mathrm{g} = 120$ nm) is much slower ($f_\mathrm{t} \approx 120$ GHz) than the HBT, the high g_m of the HBT allows the NFET to have current gain near f_t. The cascode HBT also reduces the risk of an oxide breakdown of the NFET (typically much lower than a reverse-biased diode breakdown).

Second, the HBT is preferred as a cascode device for high power operation due to its high breakdown voltage. Breakdown of the HBT device typically occurs in the base-collector junction reverse-biased diode. With the HBT in a common-base configuration, the base impedance is low and the reverse-biased diode breakdown, BV_CBO, is 5.5 V. This is significantly higher than in a common-emitter configuration where high impedance of the base biasing circuit suggests that the emitter-collector breakdown is closer to BV_CEO, e.g. 1.8 V in this process.

Fig. 2.5 illustrates a small-signal model of the BiFET cascode active feedback circuit. An input capacitor C_in forms a capacitive divider with C_1, the combination of the gate-source and the Miller multiplied gate-drain capacitance of the NFET, to regulate the voltage swing presented at the gate-source junction and to reduce the capacitive loading on the transmission line. Additionally, C_in is required to isolate the DC bias of the common-source device from the collector of the cascode device. The voltage gain transfer function of this feedback circuit is

$$A_\mathrm{v} = \left(\frac{C_\mathrm{in}}{C_1 + C_\mathrm{in}} \right) \left(\frac{Z_\mathrm{o}}{2} \right) \frac{-g_\mathrm{m1}}{\left(1 + s r_\mathrm{g} \left(C_1 \| C_\mathrm{in}\right)\right) \left(1 + s \dfrac{C_2}{g_\mathrm{m2}}\right)} \tag{2.3}$$

The first term represents the capacitive divider; the second term is the characteristic impedance of the transmission line; and the third term represents the BiFET transconductance which is a second-order transfer function. A negative sign denotes the inverting gain of the cascode amplifier.

A guideline for the size of the NFET and the bias current is the desired magnitude of A_v. To keep the single stage CPWA unconditionally stable, $|A_\mathrm{v}|$ must not be greater than $1/2$ and the NFET g_m is bounded by

$$g_\mathrm{m1} \leq \frac{4|A_\mathrm{v}|}{Z_\mathrm{o}} \frac{C_1 + C_\mathrm{in}}{C_\mathrm{in}}, \quad \text{for } |A_\mathrm{v}| \leq \frac{1}{2} \tag{2.4}$$
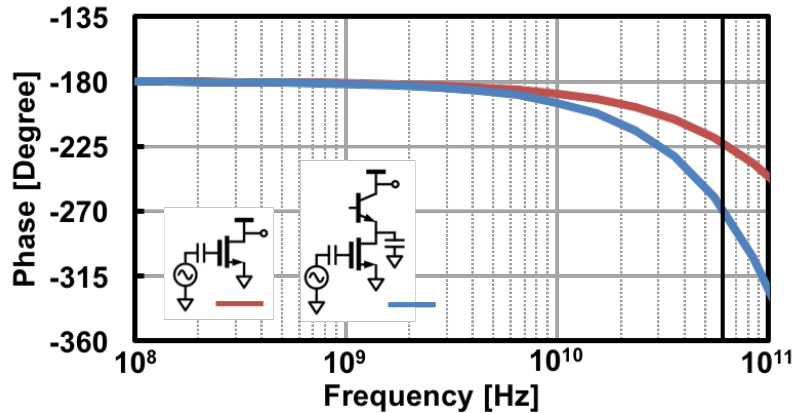
Figure 2.6: Simulated transconductance phase responses of a NFET and a BiFET structure as a function of frequency.

Simulation of the feedback network in Fig. 2.6 shows that the NFET, when sized appropriately using (2.4), contributes approximately 45° to the feedback voltage gain transfer function at 60 GHz. This is due to the pole formed by the gate resistance r_{g} and the effective input capacitance C_1. As shown in (2.3), the network has a second-order response with a pole at the interstage node of the value $g_{\mathrm{m2}}/sC_2 = f_{\mathrm{t2}}/jf$. At f_{o}, this pole can be tuned to contribute the additional 45° to the overall phase of A_{v}. In other words, the 3-dB bandwidth of the feedback network must be located approximately at f_{o} or

$$f_{\mathrm{t2,eff}} = f_{\mathrm{o}} \tag{2.5}$$

This suggests that the center frequency of the amplifier is chosen by appropriately sizing the cascode device. Since the parasitic capacitances at the drain of the NFET also contribute to C_2, $f_{\mathrm{t2,eff}}$ is much lower than the f_{t} of the native HBT ($f_{\mathrm{t}} \approx 200$ GHz).

It is difficult to simultaneously satisfy both (2.4) and (2.5) with a process that uses only NFET devices with a relatively low peak f_{t} (120 GHz) compared to the HBT because the drain current density required to provide high single-stage power gain is higher than the current density at which $f_{\mathrm{t,max}}$ occurs. This is an additional reason for using the HBT device as a cascode device.

The transmission line is implemented using a grounded coplanar waveguide

structure (G-CPW). The signal and side shields are implemented in the top alu-minum layer with the thickness of 4 μm with the bottom ground plane located 9.25 μm below. This structure provides good isolation between the signal and the lossy substrate as well as between neighboring signal lines. The G-CPW is meandered with the side shield shared between neighboring cells in order to save space and reduce the distance between the input and the output of the feedback network. The actual physical length of the transmission line is slightly less than the theoretical $\lambda/4$ line at the center frequency due to the capacitive loading of the active feedback on the transmission line structure. Fig 2.7 illustrates the G-CPW structure with the associated dimension and simulation result of the phase in both loaded and unloaded conditions.
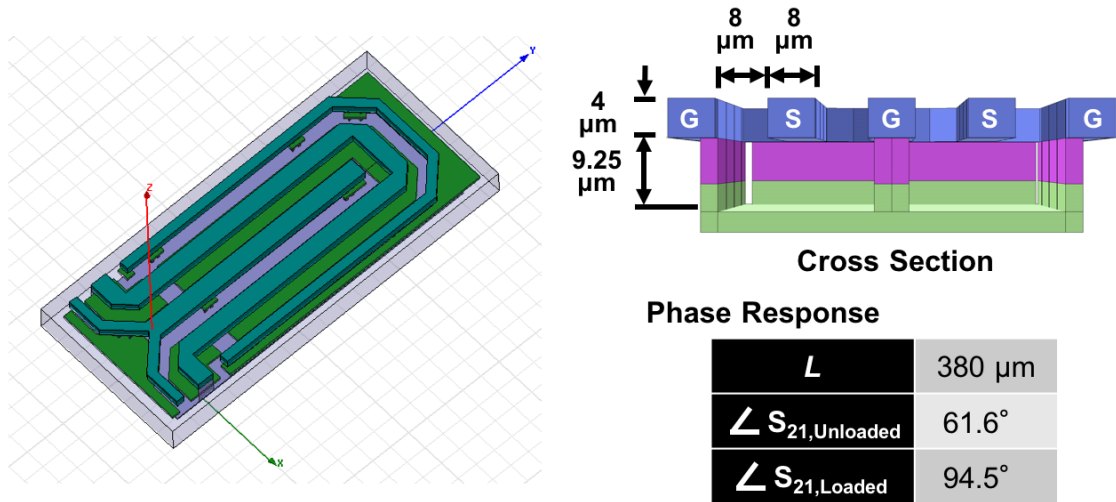
Figure 2.7: The grounded coplanar waveguide structure with the associated dimensions and simulated phase delays.

The schematic of the 60 GHz CWPA with all device sizing is shown in Fig. 2.8. The amplifier consists of four cascaded stages that are split into two clusters, each with its own gate and base bias controls. C_{in} in the final two stages are slightly smaller than those of the first two stages to allow for optimization of the feedback gain and linearity. All HBT collectors are biased through an on-chip $\lambda/4$ choke.
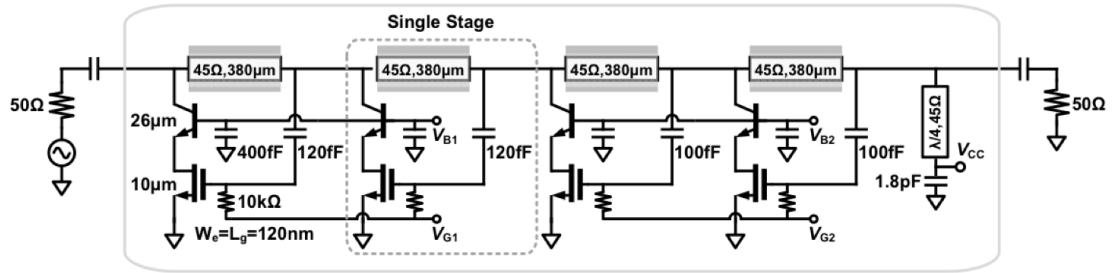
Figure 2.8: Schematic of a four-stage 60 GHz BiFET constructive wave power amplifier.

2.3 Experimental Result

The BiFET CWPA is fabricated in a 0.12-μm SiGe BiCMOS process. The die microphotograph is shown in Fig. 5.20. The circuit measures 0.64 mm $\times$ 0.53 mm (0.34 mm^2) including pads with an active area occupies only 0.28 mm $\times$ 0.26 mm (0.073 mm^2). Each stage of the CWPA consumes 3.25 mA of quiescent current for the total of 13 mA from a 4 V supply.
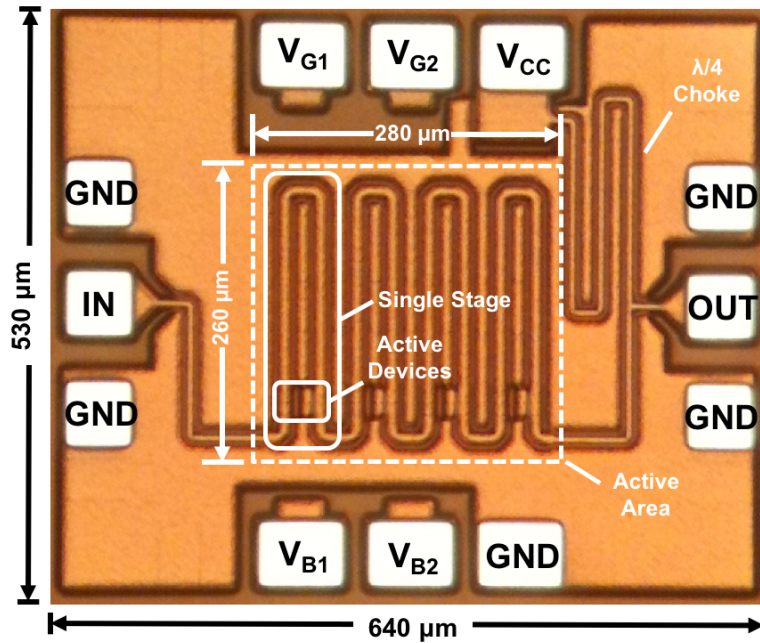
Figure 2.9: Die microphotograph of the 60 GHz BiFET CWPA implemented in a 0.12-μm SiGe BiCMOS process.
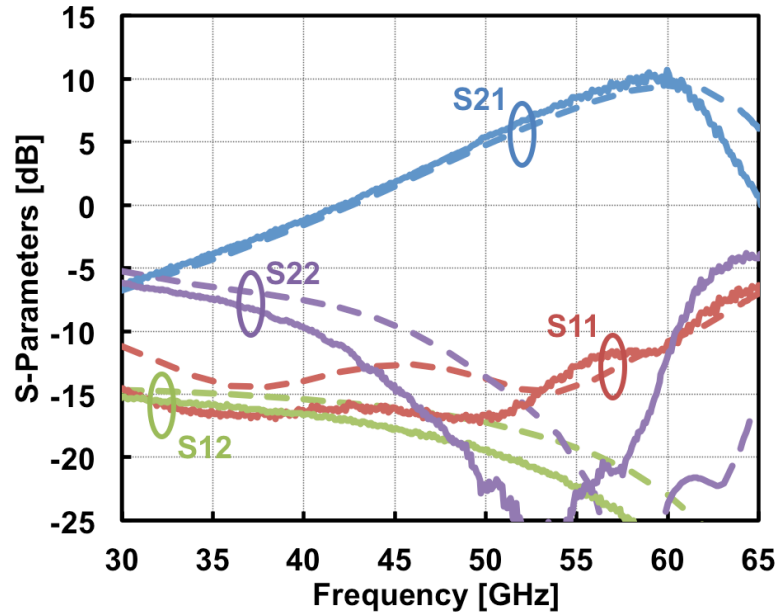
Figure 2.10: Simulated (dashed) and measured (solid) S-parameters of the 60 GHz BiFET CWPA.

S-parameters are measured with a GGB Model 67A ground-signal-ground (GSG) probes and an Agilent E8361A 67 GHz network analyzer. SOLT calibration is performed with a CS-5 standard substrate. The measured and simulated results are plotted in Fig. 2.10. A peak gain of 10.7 dB is achieved at 60 GHz with a 3-dB bandwidth of 10 GHz between 52 and 62 GHz. The circuit also exhibits a broadband input matching with input return loss less than 10 dB from DC to 62 GHz and output return loss less than 10 dB across the 10 GHz bandwidth. The output return loss is narrowband because of the frequency dependent impedance of the on-chip $\lambda/4$ choke.

The measured large-signal response at 60 GHz is plotted in Fig. 2.11. The losses of the test set-up are de-embedded to the probe tips. The circuit biasing is adjusted for maximum efficiency. This biasing reduces the gain by 1.5 dB relative to the S_{21}. The PA achieves a peak P_{sat} of 16.4 dBm and a peak PAE of 15.3%. Note the gain of the amplifier remains constant as the amplifier efficiency is reduced. Further gain reduction is limited by the pre-amplifier output power.

One unique characteristic of the CWPA is the ability for the amplifier to
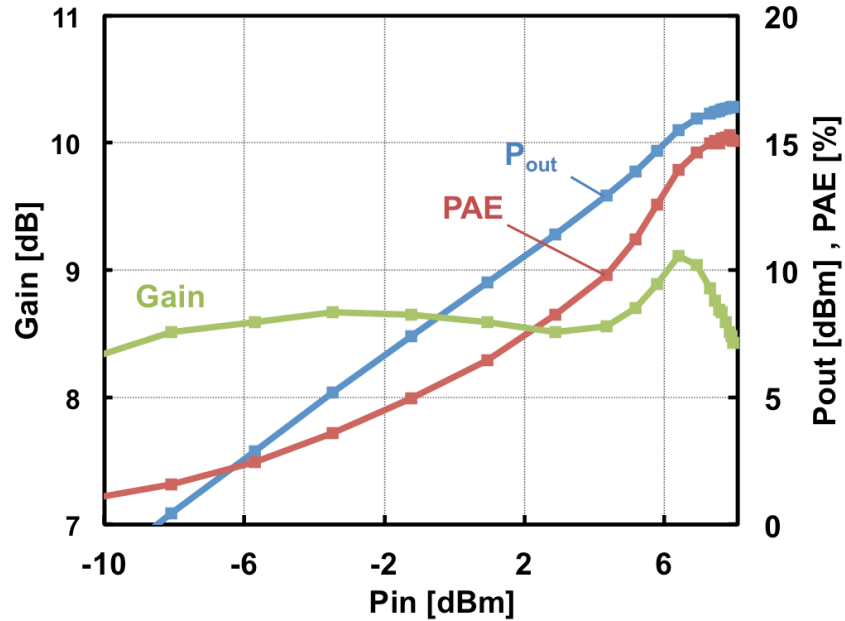
Figure 2.11: Measured large signal characteristics of the amplifier at 60 GHz.

remain operational in the event where one or more stages malfunction. To demonstrate this graceful degradation characteristic, the first two stages of the CWPA are turned off as shown in Fig. 2.12. In this condition, the input and output capacitances of the off feedback networks loaded the transmission line, resulting in an increased insertion loss. As a result, the measured S_{21} is reduced from 10 to 3 dB. This loss in gain can be partially compensated by adjusting the bias of the remaining stages. The measured S_{21} and simulated PAE of the CWPA with all stages on, first two stages off, and with compensation is plotted in Fig. 2.13.
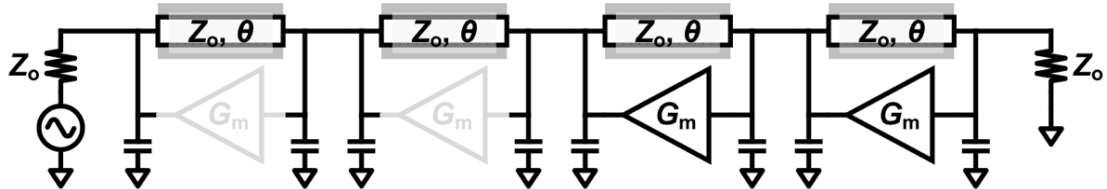
Figure 2.12: Block diagram of the setup to demonstrate the graceful degradation characteristic of the CWPA. The feedback stages in gray are turned off.
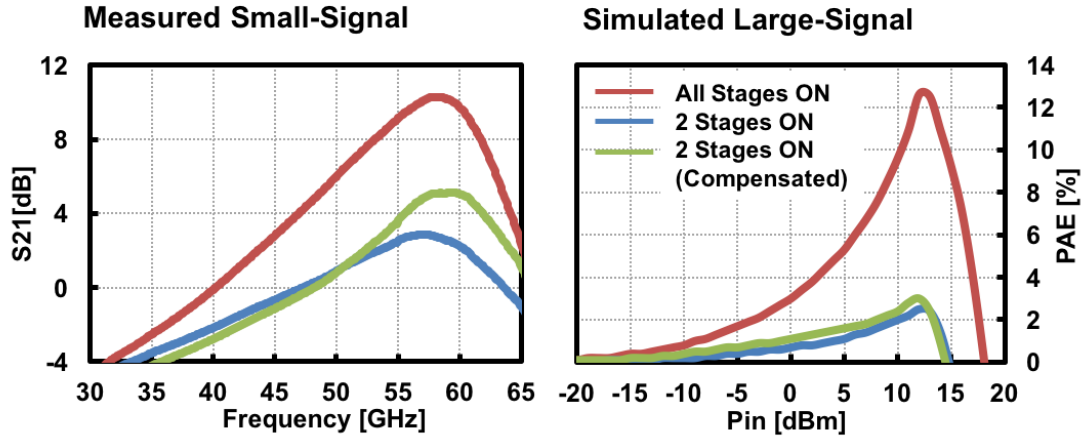
Figure 2.13: Measured S_{21} and simulated PAE of the CWPA with all stages on (red), first two stages off (blue), and with compensation (green).

2.4 Conclusion

This chapter presented the theory of operation of the cascaded constructive wave amplification (CCWA) technique and its application in the design of the 60 GHz constructive wave power amplifier (CWPA) in a 0.12-μm SiGe BiCMOS process. The amplifier achieved a peak gain of 10.7 dB at 60 GHz and a peak P_{sat} and PAE of 16.4 dBm and 15.3% respectively. The CWPA was shown to remain operational when one or more stages malfunction. This graceful degradation characteristic is unique to the amplifier designed using the CCWA technique.

Acknowledgements

Chapter 3

mm-Wave Dual-Band, Bidirectional Variable Gain Amplifier

Advanced RF integrated wireless systems are now capable of operating at multiple frequency bands. This is made possible by the technology scaling that allows a large number circuit blocks that operate at different frequencies to be placed inside a single chip. As mm-Wave beamforming system evolves, there will be a need to operate at multiple frequency bands to determine the best channels of operation. However, because a beamforming system already requires an array of transceivers, it is not feasible to add multiple circuit blocks into each channel of the array to enable the multi-band operation. This two-fold integration problem calls for circuit blocks that are capable of performing multiple tasks in the transceiver and can be electronically reconfigured as shown in Fig 3.1.

A multi-band amplifier can be implemented in several ways. Simultaneous multi-band operation has been demonstrated with narrowband amplifiers using multi-resonance peaking networks [47, 48], while band selectable operation has been demonstrated with a narrowband amplifier with tunable peaking circuit using switched passive elements [23–26]. Similarly, bidirectional amplifier are realized using switches to isolate the transmit and receive amplifiers [27]. The primary limitations of these switching techniques are the switch parasitics and the passive
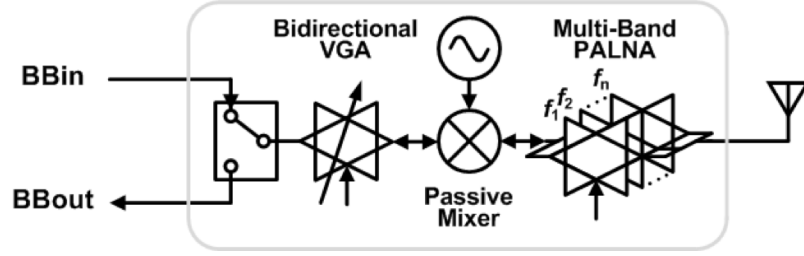
Figure 3.1: Block diagram of a multi-band, bidirectional transceiver.

area relative to active circuits. Therefore, reconfigurable blocks that use the same passives while incorporating a field of active devices to realize different circuit functions are desired. This chapter demonstrates a mm-Wave amplifier capable of dual-band and bidirectional operations without the use of mm-Wave switches.

3.1   Principle of Operation

The proposed dual-band, bidirectional amplifier is illustrated in Fig. 3.2 and consists of the cascade of constructive wave stages described in the previous chapter. In prior work, the constructive wave stage containes one feedback amplifier for amplification of the traveling wave in one direction [20, 21, 49] or anti-parallel feedbacks for bidirectional operation [22]. Here, the shunt feedback network incorporates nested anti-parallel feedback amplifiers that span different transmission line lengths. When the feedback amplifier spans two transmission line segments, the amplifier operates at the frequency $f_o/2$ to create a low frequency stage. When the feedback amplifier spans one transmission line segment, the amplifier operates at f_o. Only one feedback network is operating at a time for amplification in either the forward or reverse direction in either one of the bands.

The equivalent circuit for the high frequency (f_o) constructive wave stage is shown in Fig. 3.3. The amplifier stage comprises a transmission line with characteristic impedance Z_o and relative phase θ and two anti-parallel feedback amplifiers, each modeled as a transconductor $G_{\mathrm{mf}}/G_{\mathrm{mb}}$ with a time delay T_{d}. Only one of these feedback amplifiers is active at any given time depending on the direction of amplification. The operation principle of the forward amplification mode is the
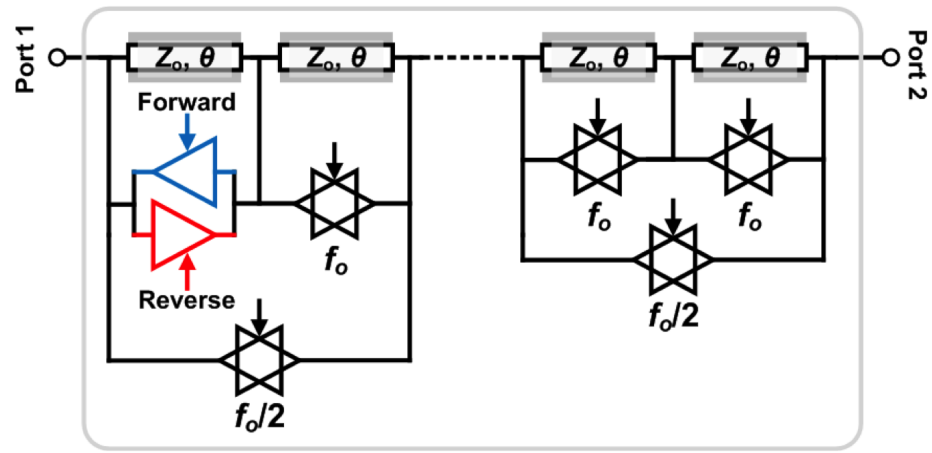
Figure 3.2: Block diagram of the dual-band, bidirectional constructive wave amplifier.
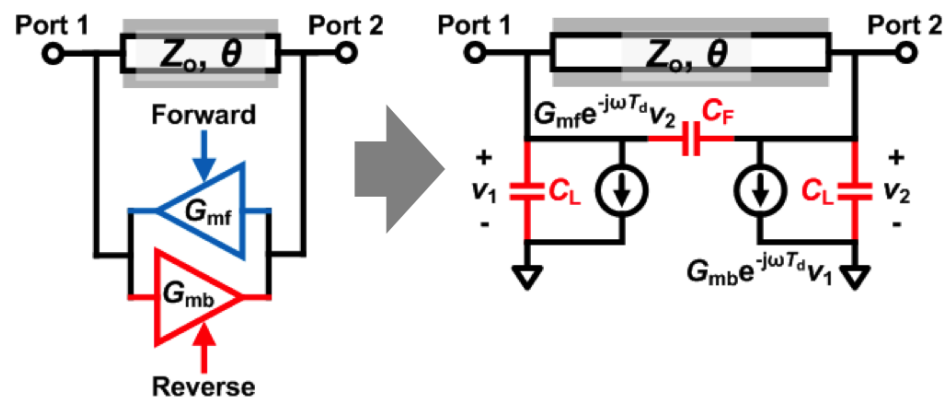
Figure 3.3: Small-signal model for individual bidirectional constructive wave amplifier stages.

same as described in Section 2.1. In reverse amplification mode, S_{21} and S_{12} are interchanged. The low frequency ($f_o/2$) amplifier operates under the same principle where the transmission line length and the feedback time delay must be *twice* as long as that of the high frequency stage. The low frequency feedback loop is placed around two consecutive high frequency stages. Therefore, for a given transmission line length, the dual-band, bidirectional amplifier contains *half* as many low frequency stages as the high frequency ones. For identical single-stage gain, overall high frequency gain will be *doubled* the low frequency gain in dB.

3.2   Circuit Design

The block diagram in Fig. 3.2 suggests that six separate feedback amplifiers are required for each stage of a dual-band, bidirectional amplifier. This implementation is not ideal due to the excessive capacitive loading effect that would degrade the performance of the amplifier. In this design in a CMOS SOI process, reconfigurability is introduced to the proposed circuit through a field of FETs which will engage different feedback paths along the transmission line. The field of FETs can reuse individual transistors to realize the six different feedback amplifiers as illustrated in Fig. 3.4(a). The proposed feedback network of a dual-band, bidirectional amplifier uses three common-source FETs (CS_X) each with a series input capacitor (C_{in}), four FET switches (SW_{1X}/SW_{2X}), and three cascode FETs ($CASC_X$). When the single stage is cascaded, each node on the transmission line is loaded with a maximum of two drains and two gates, with the exception of the middle node of the stage, which sees one drain and one gate.

Fig. 3.4(b) illustrates the four modes of operation of the amplifier with active FETs in saturation highlighted in black and inactive FETs in gray. In the high frequency (f_o) forward mode of operation, a pair of cascode amplifiers consisting of the devices ($CS_f/CASC_b$) and ($CS_b/CASC_f$) form the two feedback loops. The small-signal representation of the feedback network is illustrated in Fig. 3.5(a). For simplicity, a unilateral transistor model in [15] is used in the analysis as it provides reasonable accuracy for mm-Wave circuit design in deep
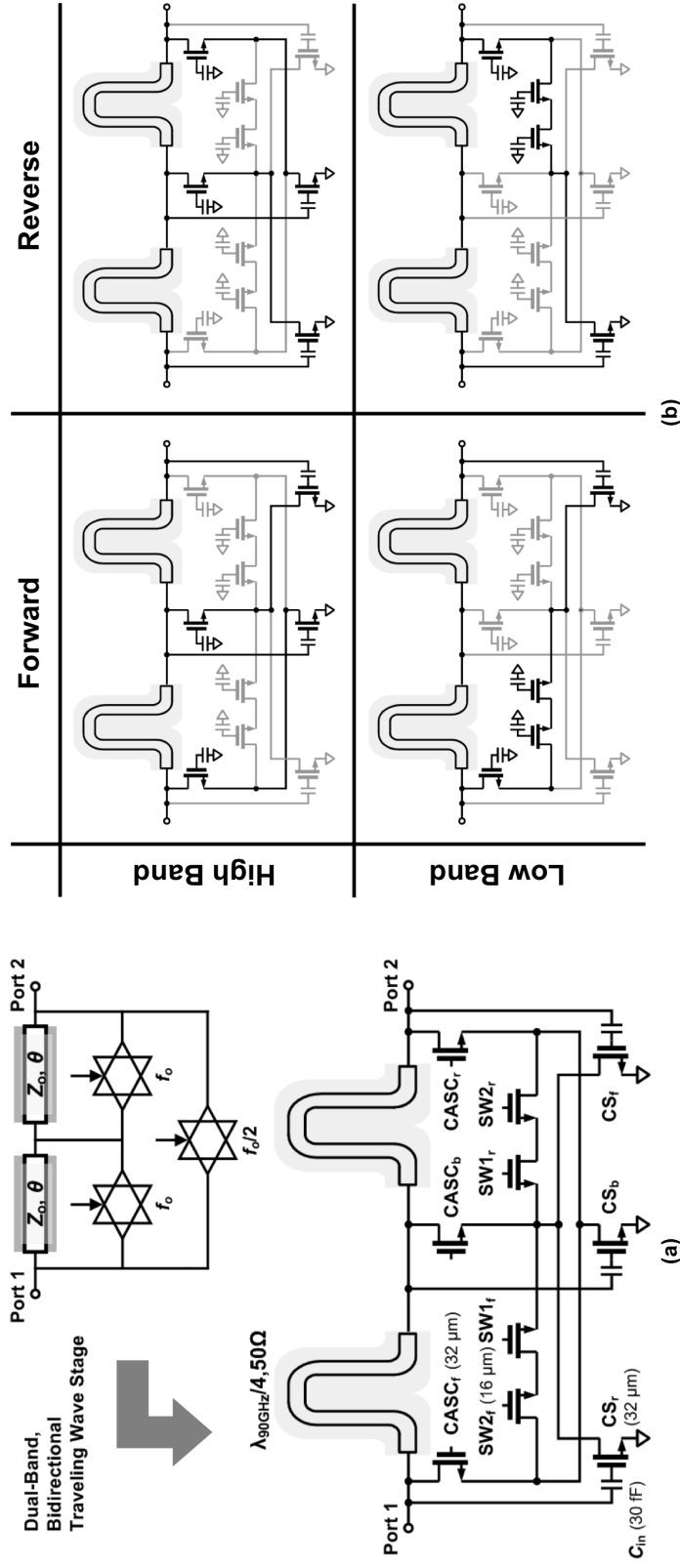
Figure 3.4: (a) A single dual-band, bidirectional stage (biasing omitted), and (b) an illustration of the four modes of operation.

sub-micron technology. The feedback open-loop voltage gain is expressed as

$$A_{\text{v}} = \left(\frac{C_{\text{in}}}{C_1 + C_{\text{in}}}\right)\left(\frac{Z_o}{2}\right)\frac{-g_m^2\,(R_{\text{D}} \parallel 1/g_m)}{(1 + sr_{\text{g}}\,(C_1 \parallel C_{\text{in}}))\,(1 + s\,(R_{\text{D}} \parallel 1/g_m)\,C_{\text{D1}})} \qquad (3.1)$$

where $C_1 = C_{\text{gs1}} + 2C_{\text{gd1}}$, $C_{\text{D1}} = C_{\text{gs2}} + 2C_{\text{gd1}}$. This expression consists of three parts: a capacitive division ratio between the input series capacitance and the effective gate shunt capacitance, the transmission line impedance, and a second-order low-pass effective transconductance transfer function. Note that the analysis for reverse mode feedback networks is identical with the exception that the pairs of devices forming the cascode amplifiers are $(\text{CS}_{\text{r}}/\text{CASC}_{\text{b}})$ and $(\text{CS}_{\text{b}}/\text{CASC}_{\text{r}})$.

For the low frequency $(f_{\text{o}}/2)$ and forward mode, a single feedback amplifier with the devices CS_{f}, SW_{1f}, SW_{2f}, and CASC_{f} spans two sections of the transmission line. Both of the switch devices are biased in saturation and behave as additional cascode devices. Additional delay through the switch devices is needed to maintain the phase delay through the feedback path. Similar expressions for the small-signal gain to (3.1) can be developed from the small-signal representation of this triple cascode structure in Fig. 3.5(b), but with a fourth-order effective transconductance transfer function. Two switch FETs are used for several reasons. First, they help improve the isolation between the two cascode amplifiers in the high frequency mode. Second, the use of two FET switches allows for a possibility of independently tuning the pole at the intermediate node by the addition of a capacitance (C_{X}) to the parasitic capacitance (C_{D2}) without affecting the poles in the high frequency feedback amplifier loops. However, this independent tuning was not needed in this particular design. The reverse mode operates in the same way but with the devices CS_{r}, SW_{1r}, SW_{2r}, and CASC_{r} forming the feedback amplifier. Fig. 3.5(c) shows the magnitude and phase of A_{v} in both high and low frequency modes. The analytical result agrees well with simulation and suggests that the simplified unilateral analysis provides a good approximation for the design of the feedback amplifier.
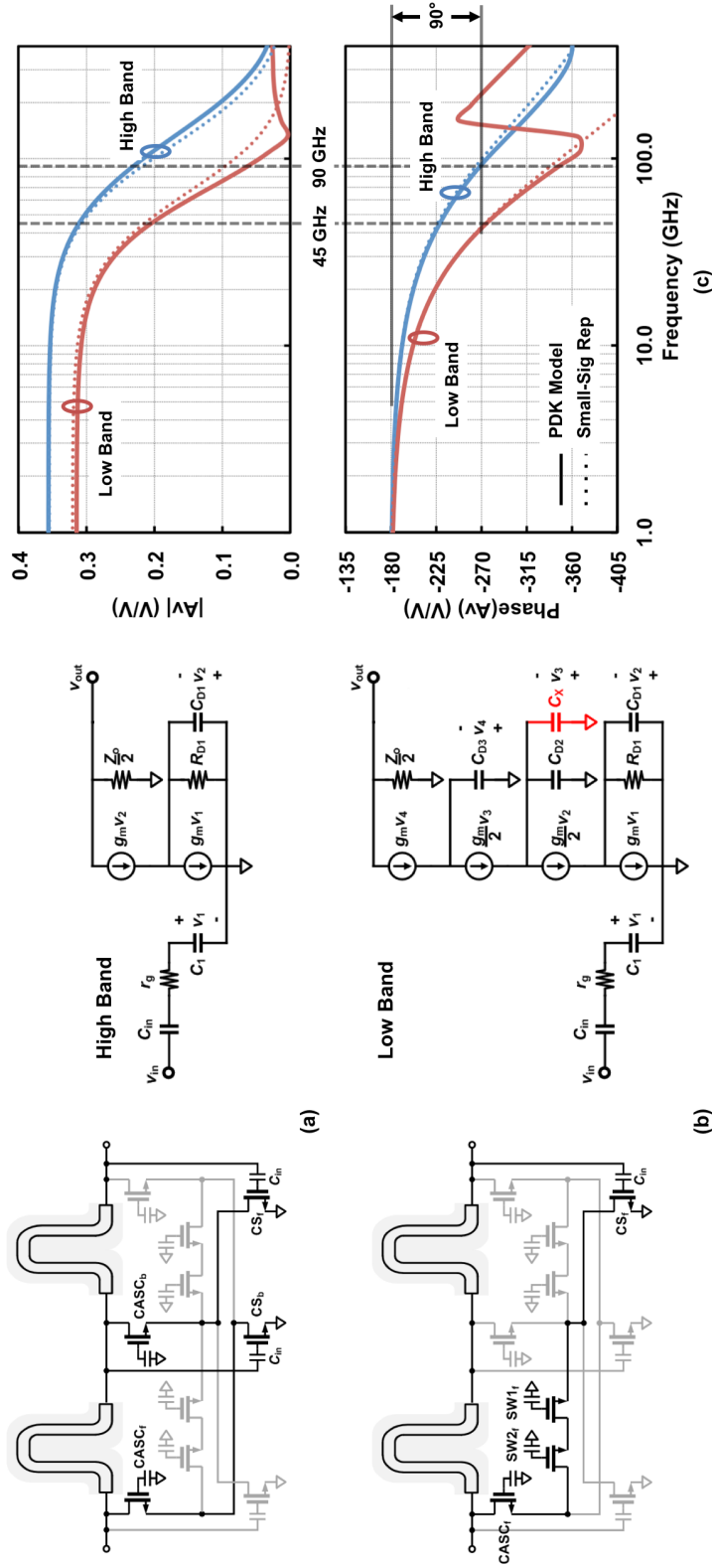
Figure 3.5: Unilateral small-signal representation of the feedback network in the (a) high band and (b) low band mode of operation. (c) Magnitude and phase response of open-loop voltage gain (A_v).

3.3   Device Measurements in 45-nm CMOS SOI

The 45-nm CMOS SOI process has been characterized for this design. One substantial advantage of the CMOS SOI process is that the floating body devices can be stacked without causing breakdown of a body junction. The SOI FETs are partially depleted with a 145-nm buried oxide layer that isolates the devices from a 13.5 Ω·cm silicon substrate. Transistors are also isolated by shallow-trench-isolation between devices. The back-end-of-line contains 10 copper metal layers (three 1X metal M1−M3, two 1.3X metal C1 & C2, three 2X metal B1−B3, and two 10X metal UA & UB) with the 2.2-μm thick aluminum top metal.

Interconnect parasitics must be carefully characterized for mm-Wave circuit design. The design flow proposed in [17] where RC parasitic extraction for 1X metal interconnects (M1−M3) and electromagnetic simulation [50, 51] of the thick copper metal interconnects as well as the transmission lines built with the top aluminum layer is used. A floating-body 256-μm wide NFET is characterized with the simulated and measured unity current gain frequency (f_{t}) as a function of current density shown Fig. 3.6. The effect of the pads are de-embedded using a four-port system calibration with on-chip open, short, and load standards [52]. While the PDK model shows an intrinsic device f_{t} of 350 GHz, the interconnects degrade the f_{t} to ~280 GHz and is confirmed by the measurement.
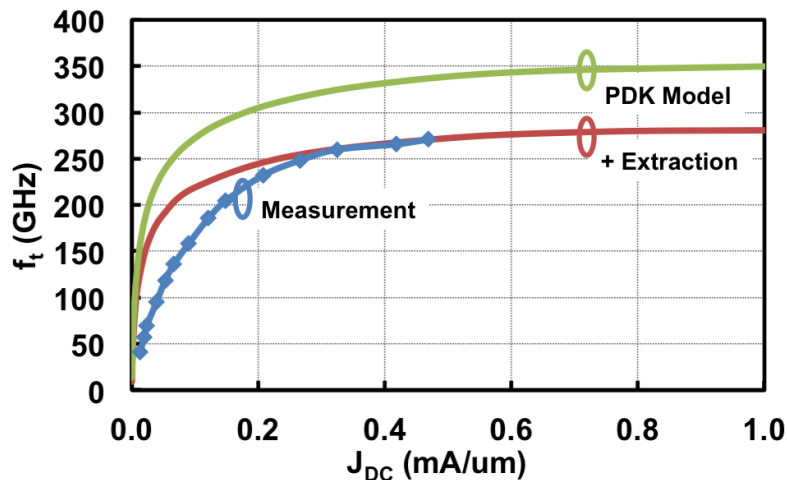
Figure 3.6: Simulated and measured unity current gain frequency (f_{t}).
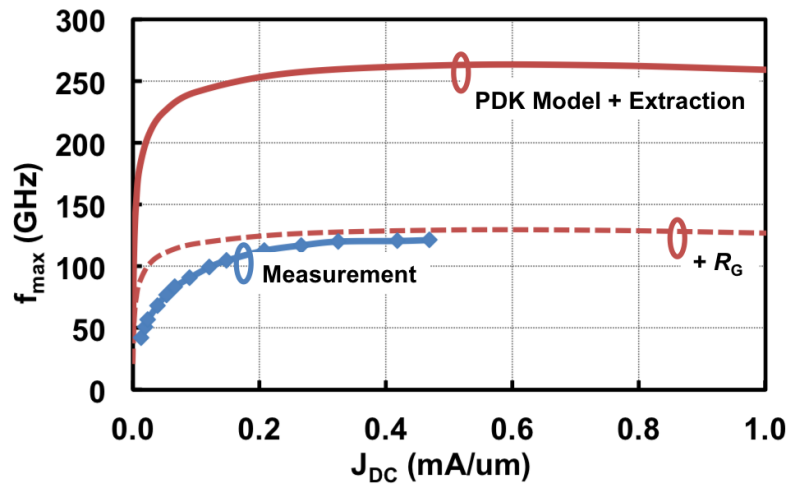
Figure 3.7: Simulated and measured maximum oscillation frequency ($f_{\max}$).
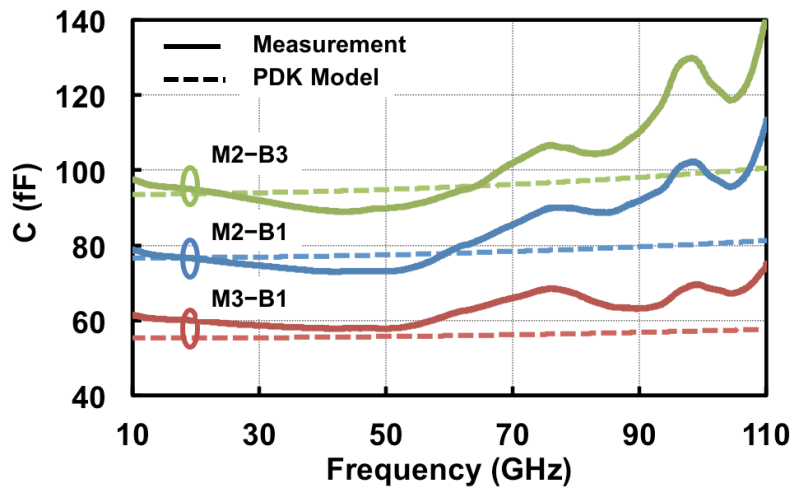
Figure 3.8: Simulated and measured capacitance of three different vertical natural capacitors (VNCAP).

The maximum available gain (MAG) and unilateral gain (U) of a 256-μm NFET are used to measure the maximum oscillation frequency ($f_{\max}$) by extrapolating the U curve. Unlike f_{t}, the measured $f_{\max}$ of 130 GHz is lower than the extracted simulation value of 263 GHz as shown in Fig. 3.7. This suggests that an additional 3.5 Ω resistance exists at the gate of the measured device. The simulated $f_{\max}$ more closely matches the measurement when a discrete resistor R_{G} is added in series with the extracted device.

The interdigitated vertical natural capacitors (VNCAP) are the best candidates for low value mm-Wave capacitances. Fig. 3.8 shows the simulated and measured capacitance of three different capacitors. All capacitors have the dimension of 7 μm $\times$ 8.7 μm but are implemented using different combinations of metal layers between M2 and B3. The PDK model underestimates the capacitors self resonance frequency in all three cases. The input impedance of a 88 fF VNCAP also suggest that the model underestimates the resistive loss of the capacitor.

3.4   Experimental Result

The prototype dual Q- and W-band, bidirectional amplifier is implemented in a 45-nm CMOS SOI process. The chip microphotographs is shown in Fig. 3.9. The amplifier measures 725 μm $\times$ 660 μm with an active area occupies only 460 μm $\times$ 360 μm of die space. The drain bias for the feedback network is provided through external bias tees at both the input and output of the amplifier. The high band is biased with a 2 V supply whereas the low band is biased with a 3 V supply because of the triple cascode feedback structure.

S-parameters is measured using the Agilent E8361A 67 GHz two-port network analyzer, Agilent E5260A mm-Wave extender, and Cascade Microtech ACP 110-LW-GSG-100 probes. A Cascade Microtech 104-783 W-band impedance standard substrate (ISS) is used for calibration up to the probe tips. The reference impedance is 50 Ω for all measurements. The S-parameters measurement for each mode of operation is conducted independently and the results are plotted in Fig. 3.10. Peak S_{21} of at least 4.2 dB is obtained in all modes of operation with
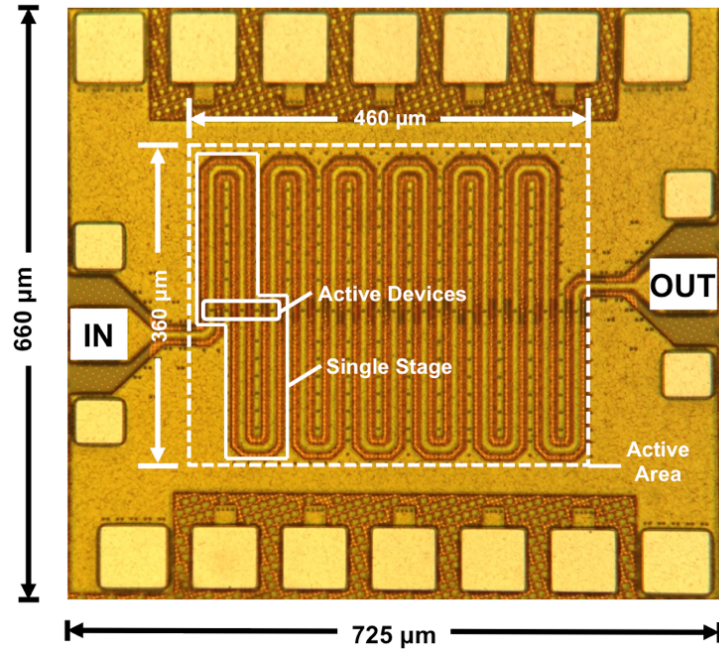
Figure 3.9:   Die microphotograph of the dual Q- and W-band, bidirectional amplifier implemented in a 45-nm CMOS SOI process.

the center frequency around 80 and 40 GHz for the high and low frequency modes, respectively, and represents a 4-dB degradation of the designed value. There are several explanations for this performance degradation:

1.   Additional parasitic resistance R_{G} at the input of the feedback path which is a combination of the underestimation of series loss in the VNCAP and the additional gate resistance associated with the device mentioned in Section 3.3.

2. The two-tiered, RC-EM design flow proposed in [17] neglects the inductance in the 1X metal layer. This method works well in the layout with no long routing in the lower metal. However, the feedback network layout of the BCWA must traverse the width of the transmission line, inevitably requiring long routing in 1X metal layer at the gate of the common-source FETs which introduces an additional gate inductance L_{G}.

3. The feedback network is located directly underneath the transmission line with a ground plane in the B3 metal layer. Because the two-tiered design flow decoupled the lower and upper metal layers, the additional capacitace C_{G} between

Mode	$f_\circ$ [GHz]	Gain [dB]
Low f Forward	40	4.6
Low f Reverse	41	4.5
High f Forward	85	4.2
High f Reverse	81	4.6
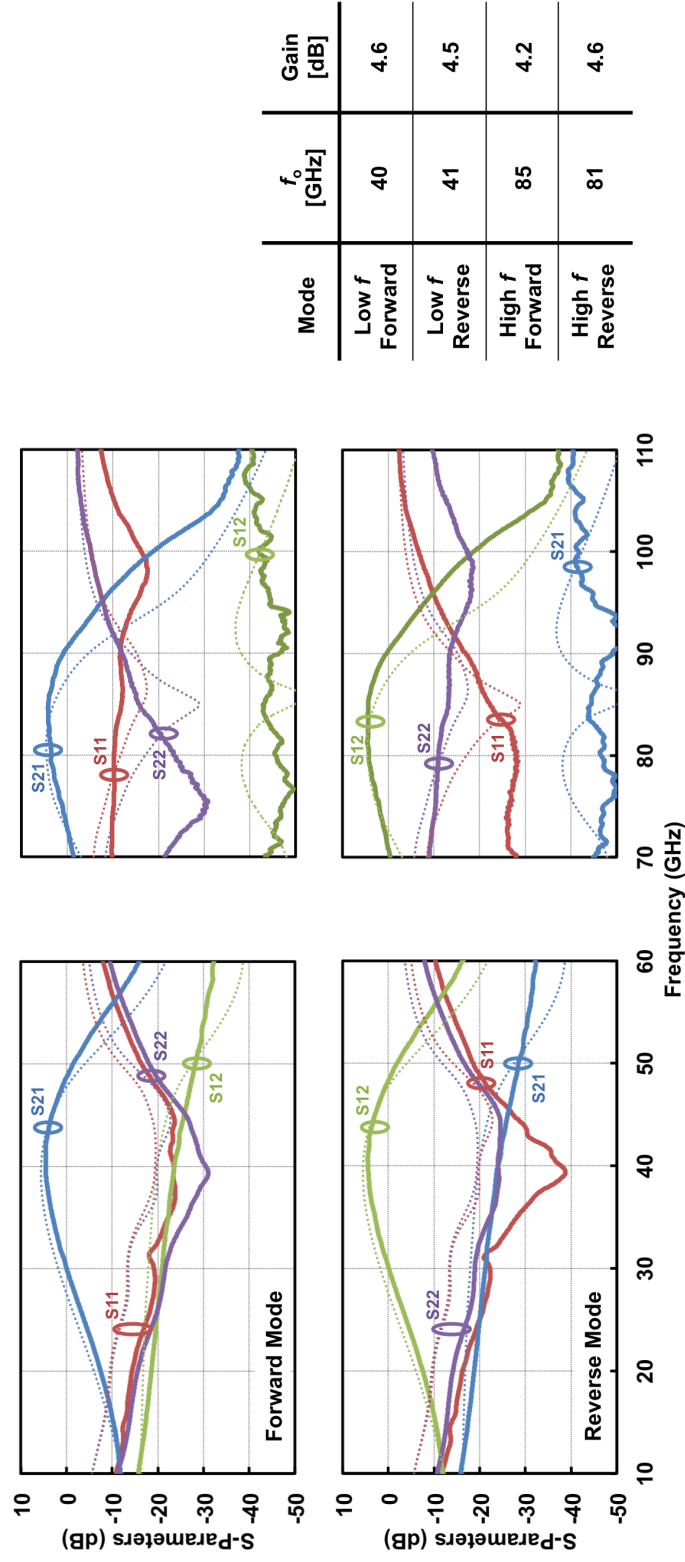
Figure 3.10: Simulated (dotted) and measured (solid) S-parameters of all four modes of operation of the dual-band, bidirectional constructive wave amplifier.

the CS transistor gates and the ground plane was not accounted for.

These additional parasitic components (R_G, L_G, and C_G) are added back in the simulation to yield the results in the dotted lines which are in good agreement with the measurement.
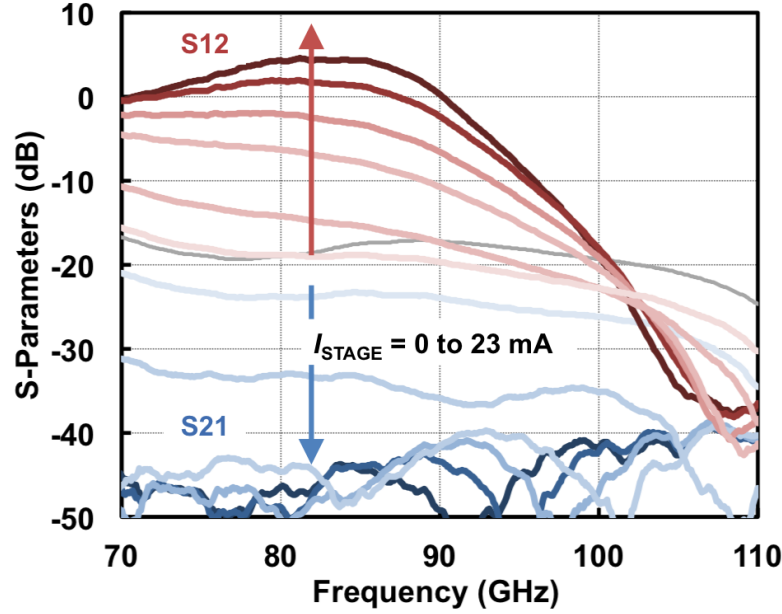
Figure 3.11: Gain (S_{12}) and isolation (S_{21}) responses of the dual-band, bidirectional amplifier operating in the high frequency band and reverse amplification mode.

Fig. 3.11 shows the gain and isolation responses of the amplifier in the high frequency, reverse operation mode as a function of bias current. With the feedback network off, the circuit behaves as a capacitively-loaded lossy transmission line. As the current increases, the open-loop feedback voltage gain increases and the directionality of the amplifier is established. The maximum gain and isolation variation of 20 dB is achieved. Similar gain control also presents in other modes of operation.

Linearity measurements are conducted at 40 GHz (low frequency band), forward amplification mode with the amplifier biased for maximum gain. The measurement results for both the two-tone test and the compression test are shown in Fig. 3.12. The two-tone input signals given by two Agilent E8257D 67 GHz signal
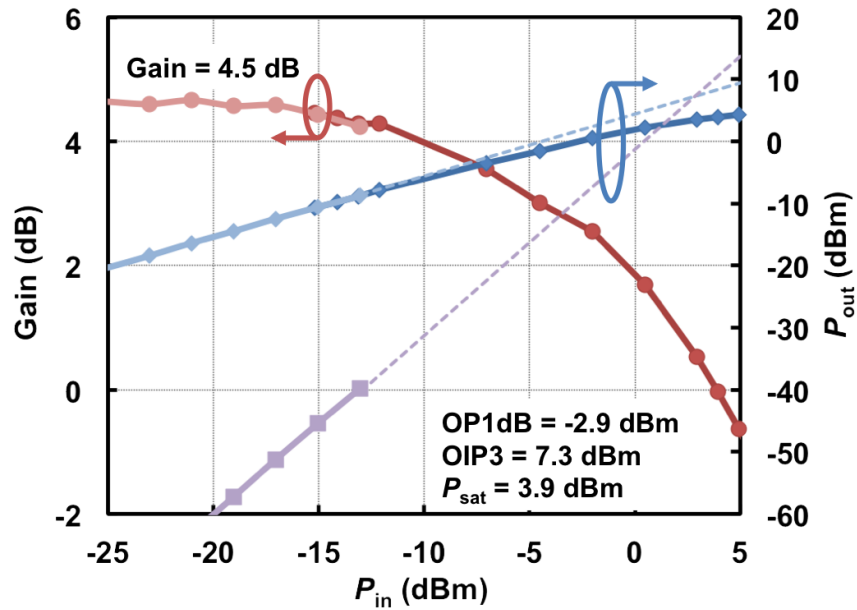
Figure 3.12: Linearity measurements at 40 GHz (low frequency band) and forward amplification mode.
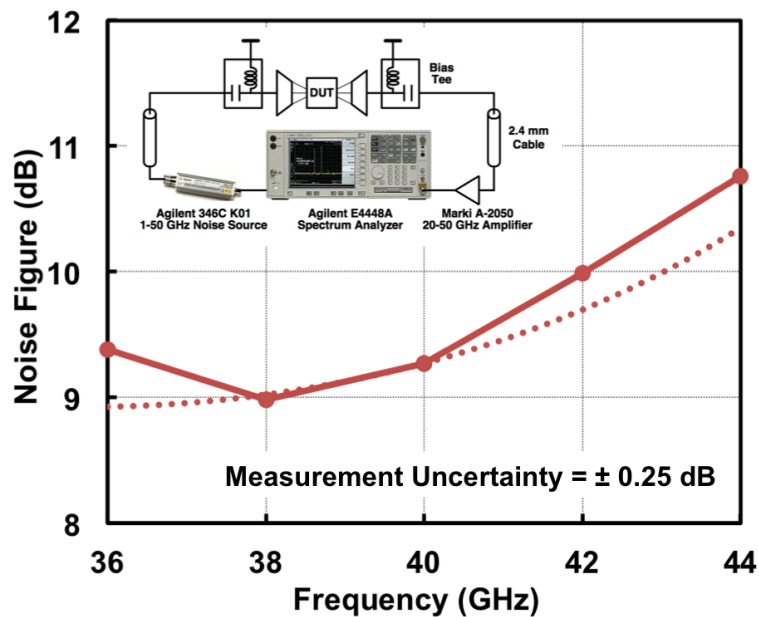
Figure 3.13: Simulated (dotted) and measured (solid) noise figure for the low frequency band and forward amplification mode and the associated test setup.

generators are 20 MHz apart at 40 and 39.98 GHz. The Agilent E4448A spectrum analyzer is used to monitor the output power of the amplifier. The saturation output power measurement (dark traces) shows a peak saturation power (P_{sat}) of 3.9 dBm with an output 1-dB compression point (OP1dB) of -2.9 dBm. The two-tone test (light traces) yields an output third-order intermodulation intercept point (OIP3) of 7.3 dBm.

The noise figure with the associate measurement setup is showed in Fig. 3.13. The circuit is biased in the low band, forward amplification mode. A minimum noise figure of 9 dB is measured at 38 GHz with the measurement uncertainty of ± 0.25 dB according to the uncertainty analysis on the spectrum analyzer.

3.5   Conclusion

A dual-band, bidirectional amplifier was proposed that allows electronic control of signal amplification in either forward or reverse direction at 40 GHz or 81 GHz and is demonstrated in a 45-nm CMOS SOI process. Reconfigurability was achieved by manipulating of traveling wave along the transmission line with a field of FETs feedback circuit, thus eliminating the need for mm-Wave switches. The circuit exhibited a peak gain of more than 4.2 dB in all modes of operation. The gain of amplifier was electronically tunable and the maximum gain and isolation variation of 20 dB was achieved. Linearity measurement at the 40 GHz band showed a peak P_{sat} of 3.9 dBm with an OP1dB of 2.9 dBm and an OIP3 of 7.3 dBm. A minimum noise figure of 9 dB was achieved at 38 GHz.

Acknowledgements

Chapter 4

mm-Wave Reconfigurable Active Circulator

A full duplex transceiver is a transceiver which is capable of simultaneously transmit and receive on a single channel at the same time [53]. Unlike the half duplex system where T/R switch (time-division duplexed) or a diplexer (frequency division duplexed) are required in order to share a single antenna for both transmit and receive, a full duplex system requires a circulator to separate the transmit and receive signals as illustrated in Fig. 4.1.

A circulator is a three-port device that directs energy from one port to a neighboring port in only one direction. The S-parameters for an ideal circulator are

$$
\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}. \tag{4.1}
$$

Because a circulator is a non-reciprocal circuit, it can only be realized using non-reciprocal components such as ferrites or active devices. The rotation of energy between ports in a conventional circulator is produced through the interaction of the traveling wave with a magnetic field. A network of passive, reciprocal couplers can only be used to realized a quasi-circulator as shown in [31]. Active circulators have been shown in [31–34]. However, they do not allow for full circulation or any
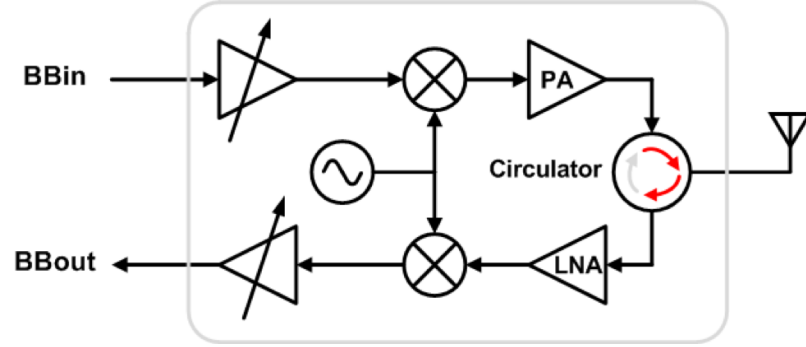
Figure 4.1: Block diagram of a full-duplex transceiver with a circulator.

control over the direction of circulation. The principle of the bidirectional amplifier presented in the previous chapter is applied to the realization of a mm-Wave integrated circulator in this chapter that not only provides complete circulation of the signal, but can also be reconfigured to circulate in both directions.

4.1 Principle of Operation

The block diagram of the active integrated reconfigurable circulator is shown in Fig. 4.2(a). The basic building blocks are three, four-port couplers and three bidirectional amplifiers connecting in a loop. The couplers are implemented as branch line couplers and the bidirectional amplifiers are implemented based on the bidirectional constructive wave amplifier (BCWA). The use of the bidirectional amplifiers is essential to synthesizing the circulator response since the passive couplers cannot realize a non-reciprocal response.

A 2-bit digital controller is used for choosing between 4 modes of operation: clockwise circulation, counter-clockwise circulation, quasi-circulation that allows signal to travel from port 1 to port 3 and from port 3 to port 2 and thru between port 1 and 2 as shown in Fig. 4.2(b). The arrow indicates the amplifying direction of the BCWA whereas the dashed line indicates the BCWA that is "attenuating" the signal. More control bits may be used to provide complete quasi-circulation operation between any two ports.

The operation of the clockwise circulation is explained by the signal flow
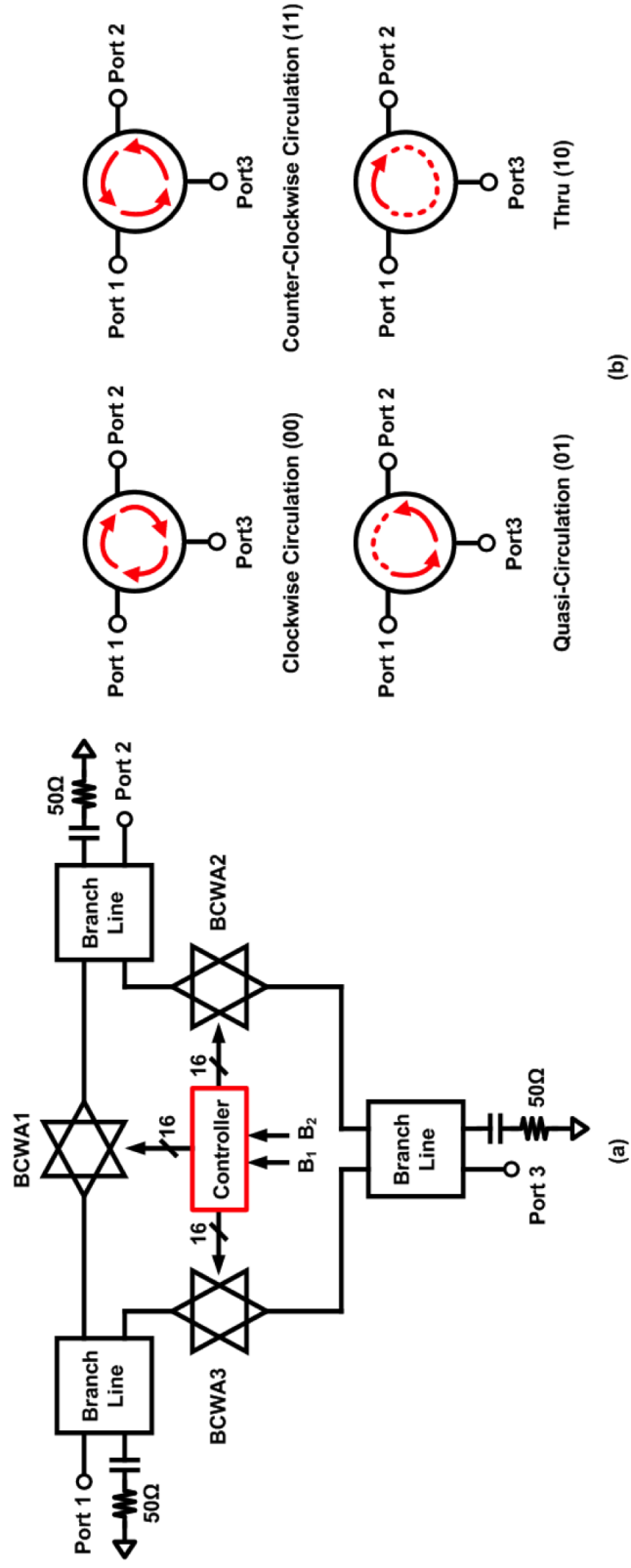
Figure 4.2: (a) Block diagram of the active reconfigurable constructive wave circulator and its (b) four modes of operation: clockwise circulation, counter-clockwise circulation, quasi-circulation, and thru.

from port 1 to port 2. In this mode, all three BCWA are biased for forward amplification. The signal traveling into port 1 is split into quadrature components by the branch line coupler. The signal component that travels to port 2 is a forward traveling signal with respect to the BCWA1 and is amplified to port 2. The signal component traveling to port 3 is seen by BCWA2 as a reverse traveling signal and is attenuated. The branch line coupler in port 2 directs half of the energy to the output and dissipates half of the energy in an on-chip termination resistor. Therefore, a 6 dB power loss due to the two branch line couplers in addition to the insertion loss of the couplers is compensated by the BCWA gain. The signal flow can be analyzed in a similar fashion from port 2 to port 3 and port 3 to port 1. Furthermore, the counter-clockwise circulation can be described by reversing the direction of the bidirectional amplifiers and applying the same reasoning to the signal flow from port 2 to port 1.

The three-port scattering matrix of the active circulator can be derived from the S-parameters of the constituent components. The S-parameters of the branch line coupler at the center frequency are

$$S_{\mathrm{BL}} = \begin{bmatrix} 0 & -j\frac{L}{\sqrt{2}} & \frac{-L}{\sqrt{2}} & 0 \\ -j\frac{L}{\sqrt{2}} & 0 & 0 & \frac{-L}{\sqrt{2}} \\ \frac{-L}{\sqrt{2}} & 0 & 0 & -j\frac{L}{\sqrt{2}} \\ 0 & \frac{-L}{\sqrt{2}} & -j\frac{L}{\sqrt{2}} & 0 \end{bmatrix}. \tag{4.2}$$

where each port is matched and isolated and $L \leq 1$ is the insertion loss of the coupler and is equal in both the through and coupled paths.

The scattering matrix of an N-stage BCWA can be generally written as

$$S_{\mathrm{BCWA}} = \begin{bmatrix} S_{11a} & S_{12a} \\ S_{21a} & S_{22a} \end{bmatrix}. \tag{4.3}$$

By graphing the traveling waves around the circulator, the three-port S-parameters

for the circulator are

$$S_{\text{CW}} =$$

$$\begin{bmatrix} \frac{L^2}{2}\left(S_{11a} - S_{22a}\right) & j\frac{L^2}{2}S_{12a} & j\frac{L^2}{2}S_{21a} \\ j\frac{L^2}{2}S_{21a} & \frac{L^2}{2}\left(S_{11a} - S_{22a}\right) & j\frac{L^2}{2}S_{12a} \\ j\frac{L^2}{2}S_{12a} & j\frac{L^2}{2}S_{21a} & \frac{L^2}{2}\left(S_{11a} - S_{22a}\right) \end{bmatrix}. \tag{4.4}$$

In the following discussion, the circulator is assumed to operate in the clockwise circulation mode where each BCWA is configured to amplify in the forward direction. To simplify the analysis, the constructive wave stage is assumed to be ideal (lossless transmission line, unilateral and no capacitive loading feedback network). The chain (ABCD) matrix in [20] can be simplified to

$$A_{\text{stage}} = \begin{bmatrix} \cos(\theta) & jZ_o\sin(\theta) \\ \frac{j}{Z_o}\sin(\theta) + g_m e^{-j\omega T_d} & \cos(\theta) \end{bmatrix}. \tag{4.5}$$

Since $A = D$ in the ABCD matrix above, it follows that $S_{11a} = S_{22a}$ regardless of the number of cascaded stages. For the phase condition $\theta = \omega T_d = \pi/2$ at the amplifier center frequency, S_{21a} and S_{12a} are functions of the number of stages N and are slightly different for odd and even number of stages

$$S_{21a} = \begin{cases} (-j)^N G_{\text{ss}} G_{\text{cs}}^{(N-1)/2}, & \text{if } N \text{ odd} \\ (-j)^N G_{\text{cs}}^{N/2} & \text{if } N \text{ even} \end{cases} \tag{4.6}$$

$$S_{12a} = \begin{cases} (-j)^N G_{\text{ss}} G_{\text{cs}}^{-(N+1)/2}, & \text{if } N \text{ odd} \\ (-j)^N G_{\text{cs}}^{-N/2} & \text{if } N \text{ even} \end{cases} \tag{4.7}$$

where $G_{\text{ss}} = 1/\left(1 - A_v\right)$ is the single-stage gain and $G_{\text{cs}} = 1/\left(1 - 2A_v\right)$ is the composite gain of two cascade stages. Using (4.6) and (4.7), (4.4) can now be simplified to

$$S_{\text{CW}} =$$

$$(-j)^{N-1} \begin{bmatrix} 0 & \frac{L^2}{2}|S_{12a}| & j\frac{L^2}{2}|S_{21a}| \\ \frac{L^2}{2}|S_{21a}| & 0 & \frac{L^2}{2}|S_{12a}| \\ \frac{L^2}{2}|S_{12a}| & \frac{L^2}{2}|S_{21a}| & 0 \end{bmatrix} \tag{4.8}$$

The S-parameters of the active circulator suggest several interesting features. First, the active circulator provides perfect matching at all ports as long as $S_{11a} = S_{22a}$, which is a property of the BCWA. Second, the directionality of the circulator, defined as the ratio between the forward transmission and reverse isolation between two ports ($D_{xy} = |S_{xy}/S_{yx}|$), is a function of only the composite gain G_{cs}^N and is improved as the number of stage increases. Third, the phase of the forward and reverse waves are dependent on the number of stages and are always a multiple of 90°. It will be shown that the phase of these waves affects the termination value at each port that results in unconditional stability of the circulator.

4.2 Stability Analysis

The stability of the active circulator is examined using the three-port stability analysis method in [54]. Consider port 1 and port 2 with an arbitrary termination in the Γ_3-plane. The expression of the unconditional stability boundary $(\mu(\Gamma_3) = 1)$ is written as

$$\mu(\Gamma_3) = \frac{1 - |S_{12}S_{21}\Gamma_3|^2}{D(\Gamma_3)} = 1 \tag{4.9}$$

where

$$D(\Gamma_3) = \begin{aligned} &|(S_{12}S_{21}\Gamma_3) + [S_{12}S_{21} + (S_{12}^3 + S_{21}^3)\Gamma_3] \\ &+ [(S_{12}S_{21})^* \Gamma_3^*]| + J(\Gamma_3) \end{aligned} \tag{4.10a}$$

$$J(\Gamma_3) = |(S_{12} + S_{21}^2\Gamma_3)(S_{21} + S_{12}^2\Gamma_3)|. \tag{4.10b}$$

Direct substitution of (4.8) into (4.9), (4.10a), and (4.10b) does not yield a simple analytical expression for Γ_3 and instead numerical experiments are leveraged to obtain insights on the stability behavior.

The first experiment is to investigate the relationship between the circulator transmission gain (S_{21}) on stability. $\mu(\Gamma_3)$ for a circulator with 4-stage BCWA is
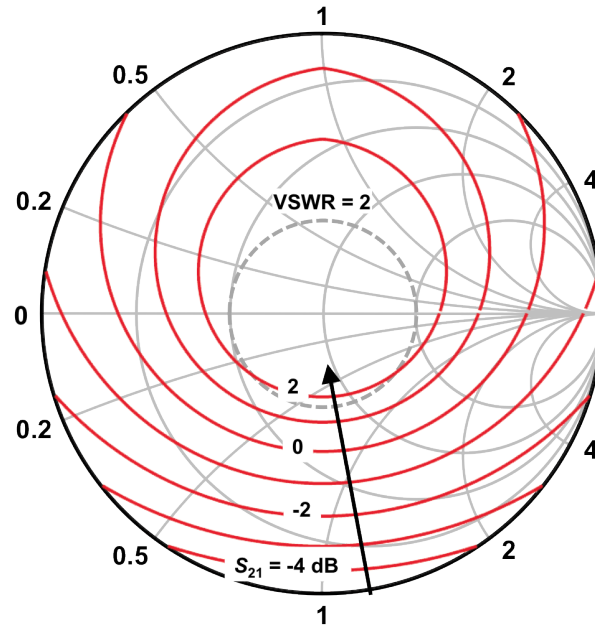
Figure 4.3: Stability boundary at the center frequency of a circulator with 4-stage BCWA viewed in the Γ_3-plane for different transmission gain (S_{21}).
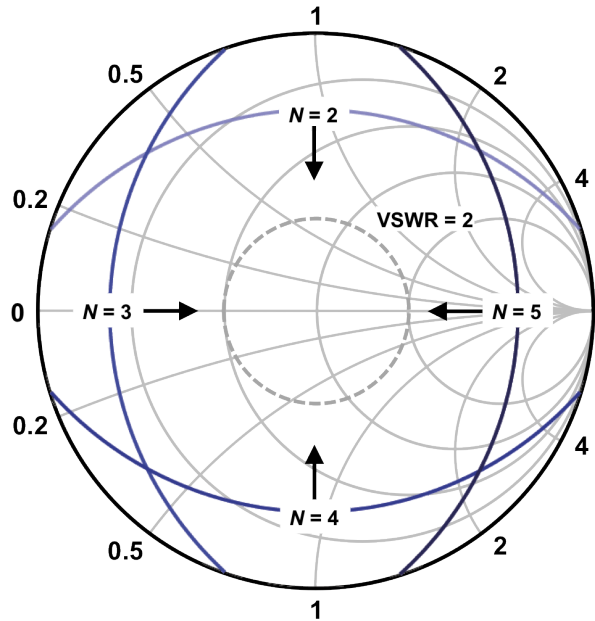
Figure 4.4: Stability boundary at the center frequency of a circulator with fixed transmission gain $(S_{21} = -2 \, \text{dB})$ for BCWA with different number of stages.

plotted in Fig. 4.3. The area inside the arc indicates Γ_3 value that leads to uncon-ditional stability between port 1 and port 2. As the overall transmission gain is varied between -4 to 2 dB or $A_\mathrm{v} = 0.05 - 0.18$, which is within the local uncondi-tional stability limit of the constructive wave stage, the termination region shrinks. This agrees with intuition since as the overall BCWA gain increases, more of the signal from port 2 travels back to port 1 via the reflection from the mismatched load at port 3. Another interesting point to note is that the circulator can pro-vide transmission gain and remains stable. For transmission gain of approximately 1.6 dB, any Γ_3 within VSWR $= 2$ circle will result in stability between port 1 and port 2. Similar results are expected between the other two, two-port pairs due to symmetry of the circuit.

Next, the effect of the number of BCWA stages on the stability boundary is investigated. In this experiment, A_v is varied to maintain forward transmission of -2 dB for circulators with different number of BCWA stages and the stability boundaries are plotted in Fig. 4.4. Observe that the unconditional stability bound-ary rotates as the number of stage increases, since the impedance that causes con-ditional stability is translated across more phase. For example, the circulator with a 4-stage BCWA has a phase lag of $\angle S_{21} = \angle S_{12} = 270°$ (e.g. $-j^3$). Therefore, the impedance Γ_3 at the lower half of the Smith chart causes port 1 and port 2 to be conditionally stable since $D\left(\Gamma_3\right)$ is maximized when $\angle S_{21} = \angle S_{12} = \angle \Gamma_3$.

Fig. 4.5 plots the maximum directionality for stability within VSWR $= 2$ circle. An interesting observation is that as the number of stage increases, the max-imum directionality remains constant for an even number of stages but degrades for an odd number of stages. This is because (4.9) can be written as a function of only G_cs^N in the case of even number of stages and G_cs^N must remain constant for a given limit of $\mu = 1$ at the VSWR $= 2$ circle. The stability analysis suggests that given a desired directionality (or transmission gain) and VSWR, it is desirable to choose the lowest possible number of odd BCWA stages.
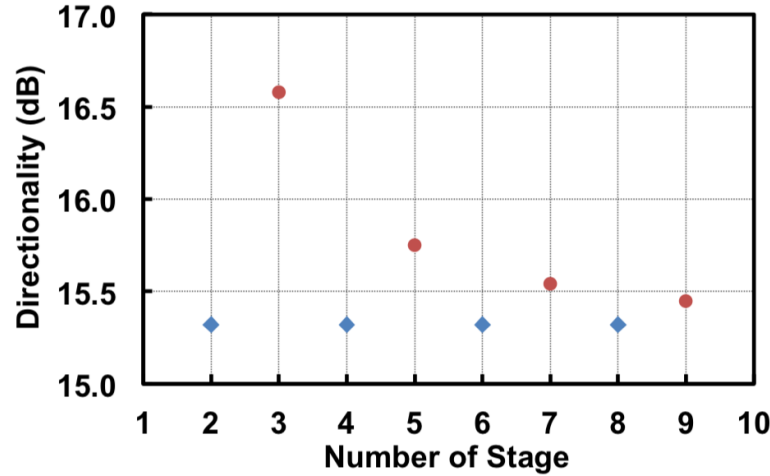
Figure 4.5: Maximum directionality that results in unconditional stability between port 1 and port 2 for all Γ_3 termination within VSWR $= 2$ circle.

4.3 Circuit Design

The branch line couplers are designed using the electromagnetic simulators [50,51]. Floating metal slow-wave structure [55] is used to reduce the physical size of the quarter-wave transmission lines. Electromagnetic simulation shows a 50 Ω, 100 μm slow-wave transmission line exhibits a loss of 0.3 dB with a phase delay of 63 degrees, which translates to an electrical length of approximately 3.5 times longer than a conventional grounded coplanar waveguide tranmission line. Fig. 4.6 shows the simulation result of the branch line coupler. The insertion loss of the thru (S_{21}) and coupled (S_{41}) paths are 1 dB with return loss better than -15 dB from 70 to 85 GHz. The circulator response between all three pairs of ports is relatively insensitive to the gain imbalance of the branch line coupler due to the fact that as the signal travels between two ports, it passes through one thru and one coupled paths of the branch line coupler.

Three bidirectional constructive wave amplifiers are used to control the direction of the signal flow. Each BCWA consists of four bidirectional constructive wave stages as shown in Fig. 4.7. Similar to the dual-band, bidirectional amplifier design, the feedback circuits are shared between each stage to minimize the number of devices loading the transmission line. The forward and reverse mode feedback
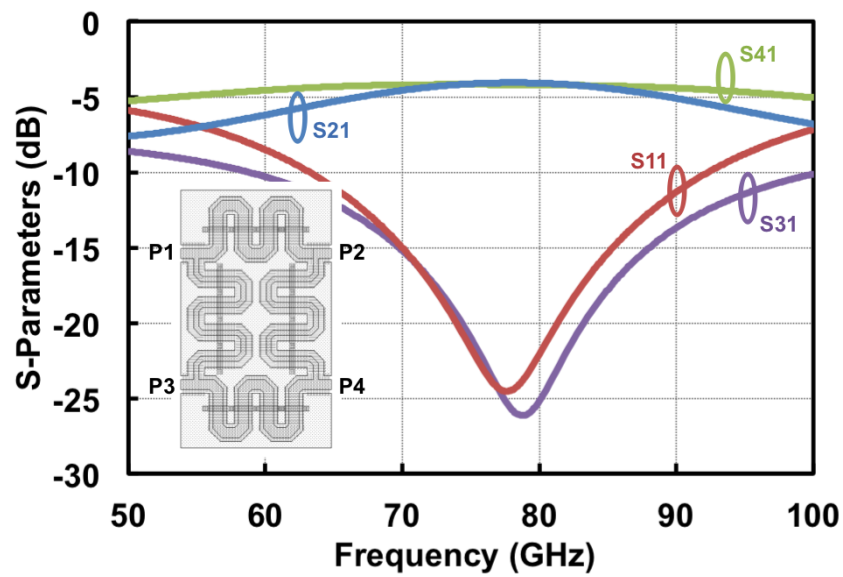
Figure 4.6: *S*-parameters simulation of insertion losses, isolation, and return loss of the slow-wave branch line coupler.
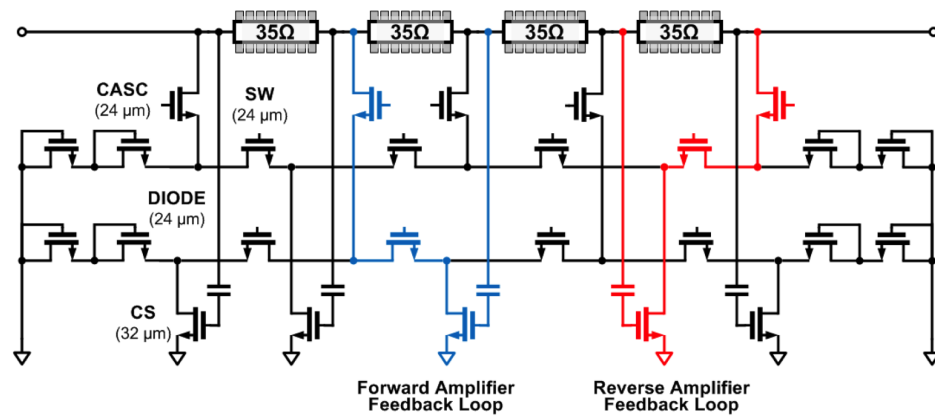
Figure 4.7: Circuit diagram of the 4-stage bidirectional constructive wave amplifier (BCWA) with one of the forward and reverse amplifier feedback loop highlighted in blue and red, respectively.
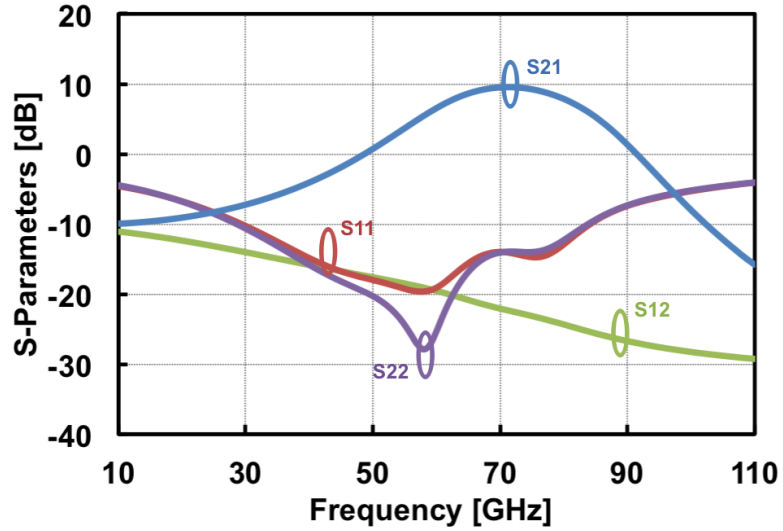
Figure 4.8: Simulated S-parameters of the BCWA in the forward amplification mode.

amplifiers are highlighted in blue and red, respectively. Each of the feedback loops consists of a double cascode amplifier with a series capacitance at the gate of the transconductor. The same unilateral approximation approach is employed when designing these feedback amplifiers as in the dual-band, bidirectional amplifier. Stacks of diode-connected devices are placed on the edge stages to equalized the capacitive loading on the feedback loops to the internal ones. The BCWA has a peak gain of 10 dB at 70 GHz. Fig. 4.8 shows the simulated S-parameters of the BCWA in the forward amplification mode.

In the quasi-circulation mode, BCWA1 performs the attenuation operation between port 1 and port 2 while BCWA2 and 3 are set to amplify signal from port 1 to port 3 and from port 3 to port 2, respectively. The attenuation of the BCWA1 is done by turning on all five transconductors. Although the feedback circuits are on, no phase matching condition is satisfied. The feedback network simply causes heavy capacitive loading on the transmission line, decreasing the line bandwidth and causing higher attenuation. In the thru mode, BCWA1 amplifies signal from port 1 to port 2 while BCWA2 and 3 performs the attenuation operation.

4.4   Experimental Result

The prototype V-band reconfigurable active circulator is implemented in a 45-nm CMOS SOI process. The chip microphotographs is shown in Fig. 4.9. The active circulator measures 1.10 mm $\times$ 1.13 mm. The three ports of the circulator are located in the west, east, and south side of the chip with DC biasing and digital control bits input located in the north side.
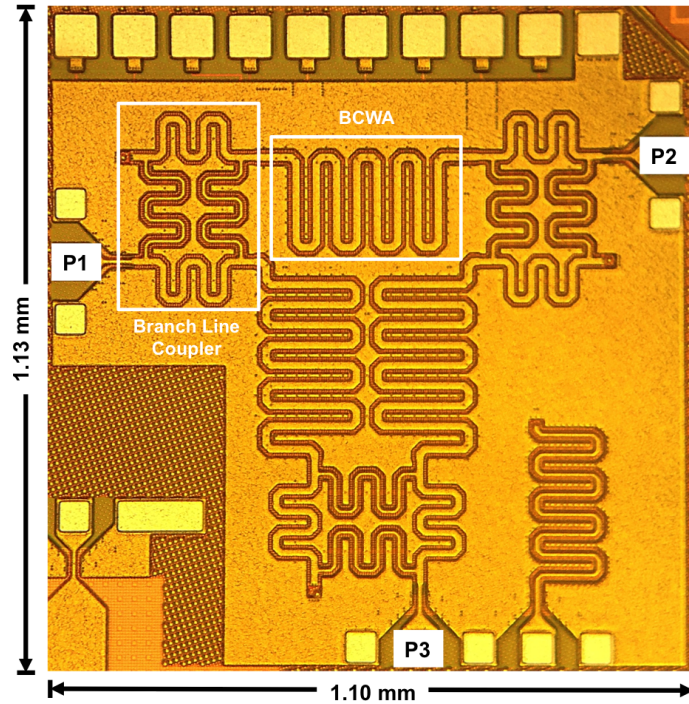
Figure 4.9: Die microphotograph of the V-band reconfigurable active circulator implemented in a 45-nm CMOS SOI process.

S-parameters response is measured using the Agilent E8361A 67 GHz two-port network analyzer, Agilent E5260A mm-Wave extender, and Cascade Microtech ACP110-LW-GSG-100 probes. Fig. 4.10 illustrates the measurement setup between port 2 and port 3. The remaining port (port 1) is terminated with a V-band waveguide termination with the S_{11} within $VSWR = 2$ circle between $44-76$ GHz as shown in Fig. 4.11. Three, two-port measurements are required to fully characterize the circulator in each mode of operation.

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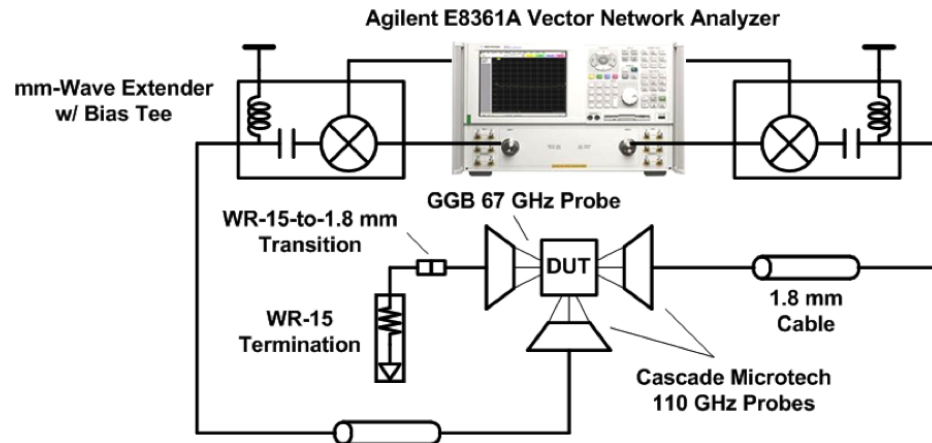
Figure 4.10: S-parameters measurement setup for port 2 and port 3 with port 1 terminated by a V-band waveguide termination.
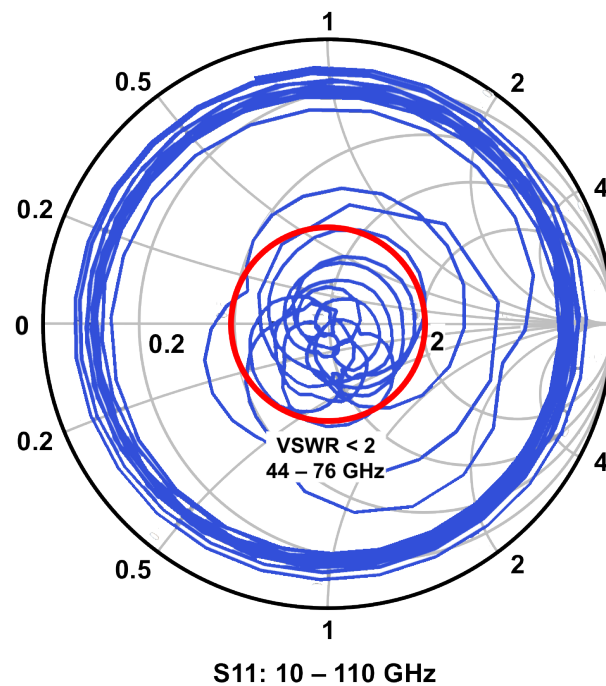
Figure 4.11: S_{11} of the V-band waveguide termination.
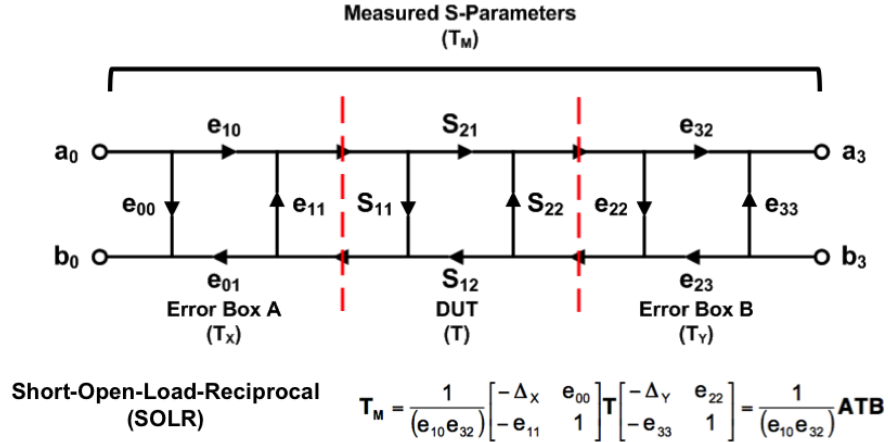
Figure 4.12: 8-term error model for the short-open-load-reciprocal (SOLR) calibration method.

A short-open-load-reciprocal (SOLR) error calibration method [56] is employed in the measurement of the active circulator. It is based on an 8-term error model which represents the measurement system as the cascade of two error boxes between the ideal measurement ports and the DUT reference plane as shown in Fig. 4.12 [57]. Unlike the classical "full two-port" 12-term short-open-load-thru (SOLT) calibration, SOLR does not require the precise knowledge of the delay of the thru structure as long as this fourth calibration standard is a passive reciprocal network. In fact, the accuracy limit of the result at higher frequencies is largely due to the accuracy of the short, open, and load standard that are used for the one-port calibrations. For the circulator measurement, short, open, and load standards on the 104-783 ISS are used for one-port calibrations while the right angle thru from Cascade Microtech 109-531 right angle ISS is used as the reciprocal standard.

Fig. 4.13 shows the S-parameters of the insertion losses and isolations of the circulator. The three separate measurements between port 1 and port 2 (dark traces), port 2 and port 3 (medium traces), and port 3 and port 1 (light traces) with clockwise transmissions (S_{21}, S_{32}, S_{13}) in blue and counter-clockwise transmissions (S_{12}, S_{23}, S_{31}) in red are plotted together. The minimum insertion losses between all pairs of ports is 7.4 dB with 3-dB bandwidth between $60-75$ GHz for both clockwise and counter-clockwise circulation modes. Reverse isolations re-

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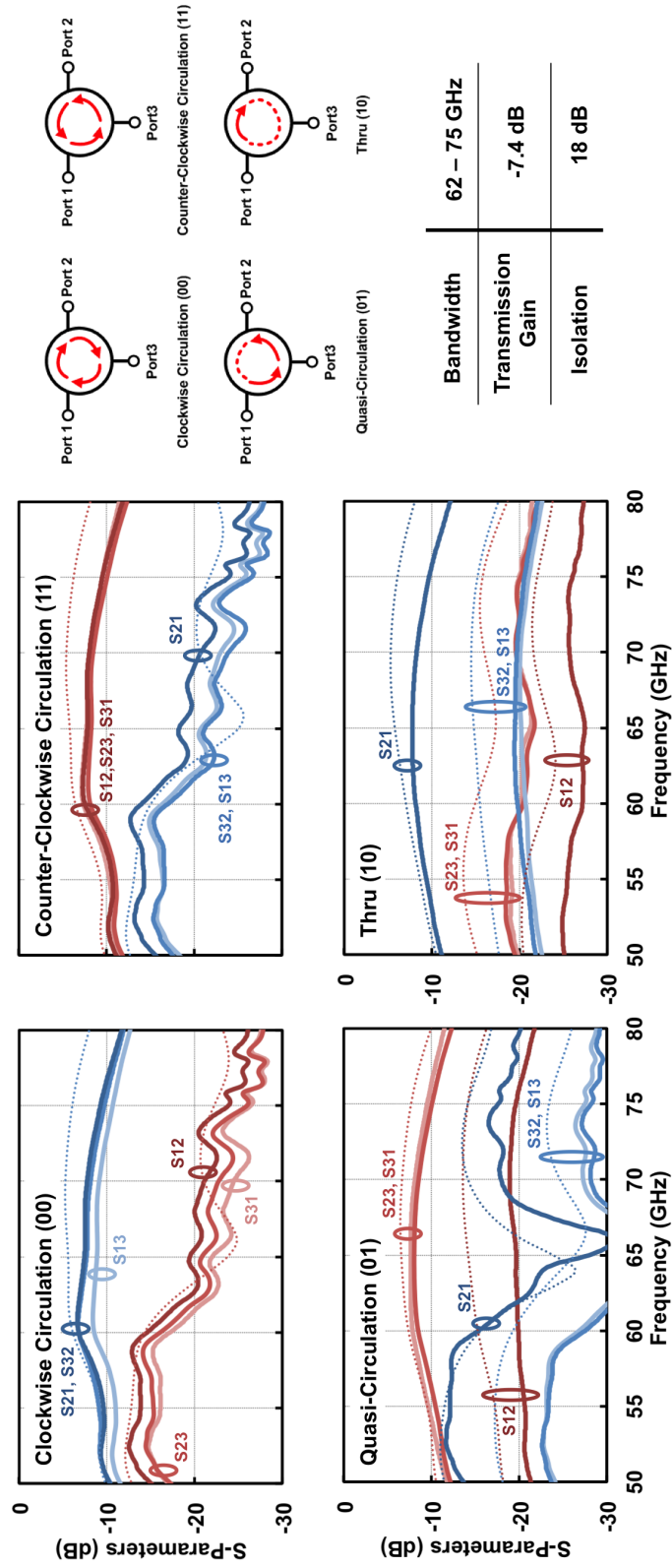
Figure 4.13: Simulated (dotted) and measured (solid) S-parameters of the insertion losses and isolations between the three, two-port pairs in all four modes of operation of the active reconfigurable circulator.
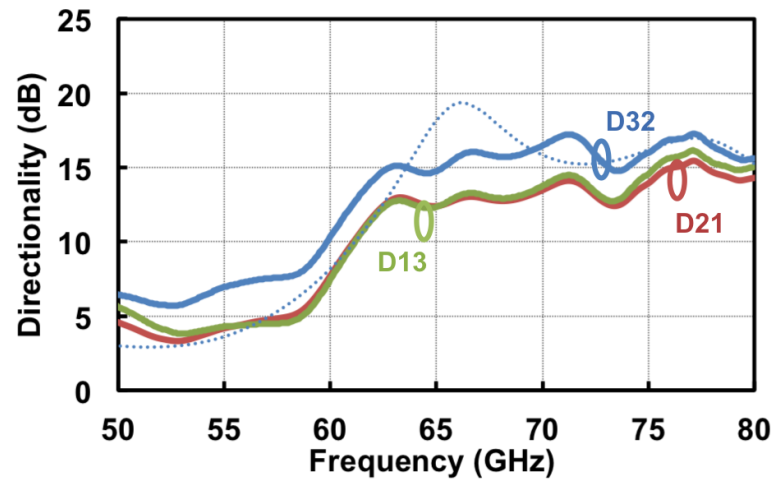
Figure 4.14: Simulated (dotted) and measured (solid) directionality of the circulator in clockwise circulation mode.
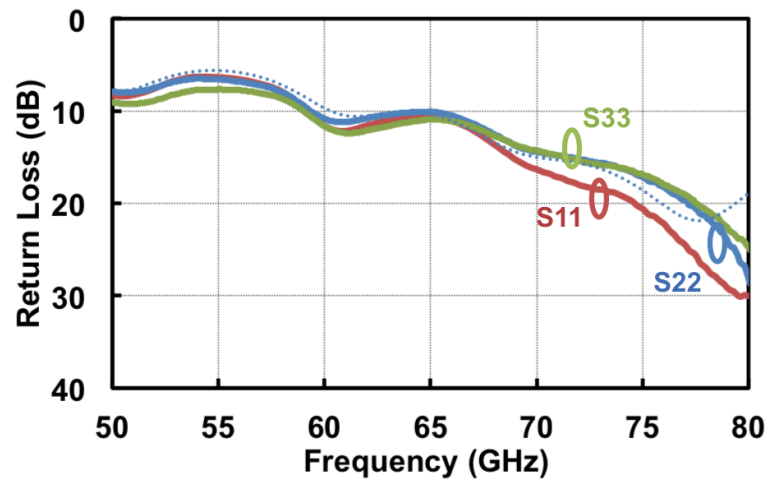
Figure 4.15: Simulated (dotted) and measured (solid) Return loss of the circulator in counter-clockwise circulation mode.

main better than 18 dB between 62−80 GHz. The directionalities are plotted in Fig. 4.14 and remain above 10 dB across the 3-dB bandwidth of the circulator. The circulator in quasi-circulation mode exhibits similar insertion loss response as the full circulation modes but with better reverse isolation between the two pairs of isolated ports because BCWA1 performs the attenuation operation between port 1 and port 2. The significant degradation in gain and frequency downshift from the original designed frequency of 75 GHz is attributed to the same causes mentioned in chapter 3.

Fig. 4.15 shows the return losses at all three ports for the counter-clockwise circulation mode. Unlike the dual-band, bidirectional amplifier in the previous chapter that shows the broadband return loss characteristic of the constructive wave amplifier, the circulator return loss characteristic is narrowband due to the branch line couplers. The return losses remain better than 15 dB between 75−85 GHz, the original design frequency, at all ports. This further affirms that the modeling and design of the branch line coupler and slow-wave transmission line are relatively accurate and it is the feedback networks that cause the overall frequency shift and the performance degradation.

4.5   Conclusion

A *V*-band reconfigurable active circulator was proposed that allows electronic control of signal traveling between 3 ports in four different modes of operation: clockwise, counter-clockwise, quasi-circulation, and as a thru between port 1 and port 2. The stability of the active circulator was analyzed using a three-port stability analysis procedure. The circulator showed a minimum insertion loss of 7.4 dB a 3-dB bandwidth between 60−75 GHz and a reverse isolation of better than 18 dB between all pairs of ports and across all modes of operation.

Acknowledgements

Chapter 5

LO Phase-Shifting, Switchless mm-Wave Bidirectional Front-End Using Linear Coupled Oscillators

As mentioned in the previous chapter, a half duplex system requires a T/R SPDT switch in order to share a single antenna for transmit and receive mode. Similarly, an RF phase shifter is needed in an RF beamforming transceiver in order to create a phase progression between each transceiver element. The performance of the switch and phase shifter will directly affect the link budget as these components are located directly in the signal path. This calls for the design of high performance switch and phase shifter, which remains a challenge at mm-Wave frequency.

This chapter presents an alternative approach in implementing a mm-Wave beamforming transceiver. First, a switchless half-duplex front-end is designed that uses a passive impedance transformation network to create isolation between the PA and the LNA, eliminates the need for a T/R switch. Second, an LO phase-shifting architecture is employed to remove the need for a phase shifter in the signal path. The phase progression in the LO signal is achieved by a two-element linear
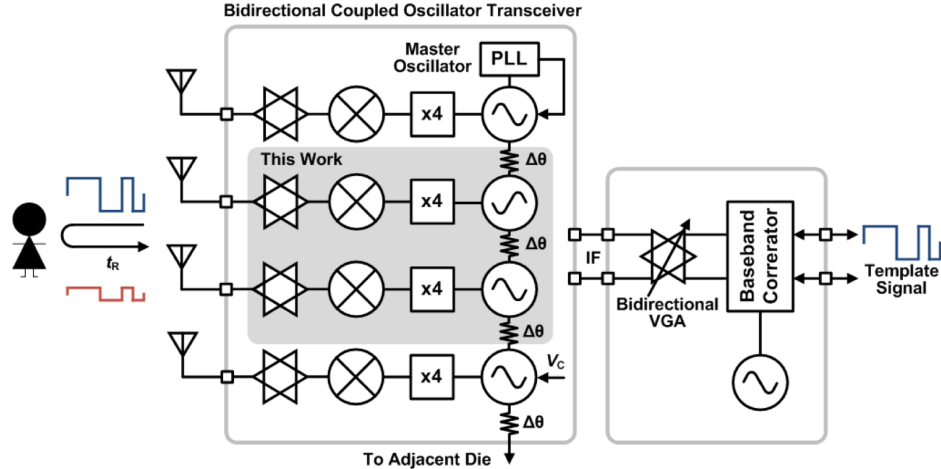
Figure 5.1: An example of a half-duplex pulse compression radar (PCR) system with linear coupled oscillators transceiver for beamforming.

coupled oscillator array and frequency multipliers. This architecture can be used with a TDD baseband signal processor and is easily scalable linearly on-chip or possibly from chip-to-chip. The block diagram of the proposed system is illustrated in Fig. 5.1

5.1   Switchless Bidirectional Front-End

The 70 GHz bidirectional front-end consists of two main circuit blocks; A power amplifier/low-noise amplifier (PALNA) that supports half-duplex bidirectional operation and a double-balanced passive mixer. The circuit is implemented in the 90-nm SiGe BiCMOS process. The back-end-of-line (BEOL) of the process and the associated dimensions shown in Fig. 5.2 include nine copper layers with a top aluminum metal layer. A 4-μm heterojuction bipolar transistor (HBT) with a single emitter, dual collectors, and base fingers (CBEBC) is a unit cell with the device interconnection simulated up to the top copper layer using EMX [51]. Including the interconnection parasitics, the HBT device exhibits peak f_t and f_{max} of 280 and 320 GHz at the current density of 2.4 mA/μm as plotted in Fig. 5.3. Minimum NF_{min} of 2.4 dB at 74 GHz is achieved at 0.3 mA/μm. A 50 Ω ground-shielded coplanar waveguide (G-CPW) transmission line designed on the OL cop-
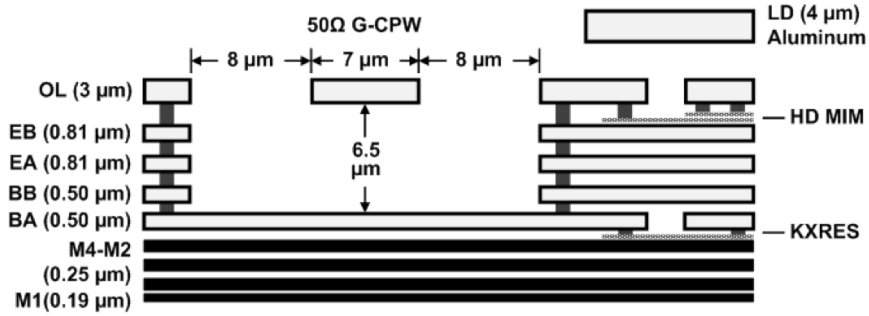
Figure 5.2: Back-end-of-line of the 90-nm SiGe BiCMOS process.

per layer with the ground shield in the BA layer and shows a simulated loss of 0.6 dB/mm at 74 GHz with Q of 27. This transmission line, along with a high-density metal-insulator-metal (HD-MIM) capacitor $(2.72 \text{ fF}/\mu m^2)$ are used in the implementation of the matching and resonance networks throughout the design. The frequency response of the G-CPW and HD-MIM are plotted Fig. 5.3. EM simulation of the HD-MIM capacitor at 74 GHz shows approximately four times higher Q than the compact model in the process design kit.
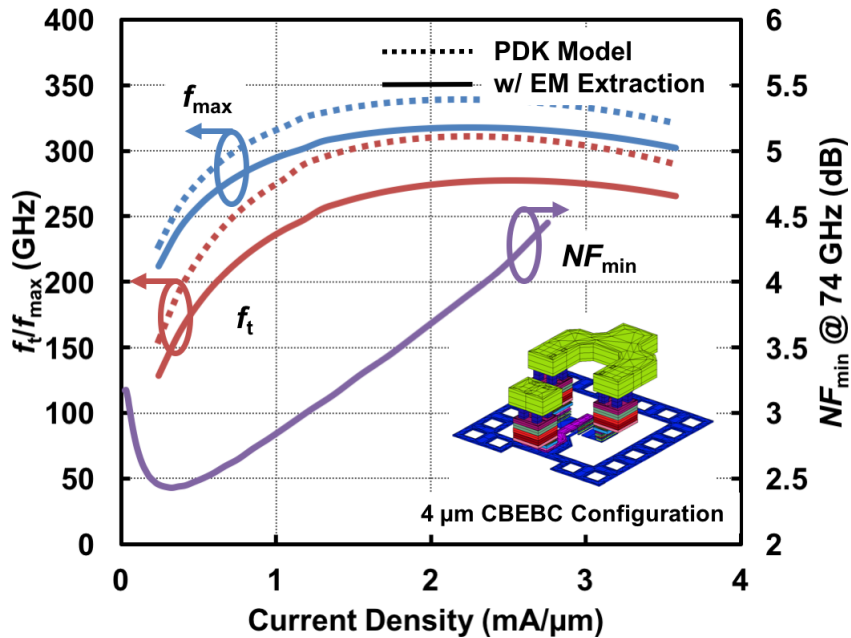
Figure 5.3: Simulated f_t, f_{max} and NF_{min} at 74 GHz of a 4-μm CBEBC HBT device as a function of current density.
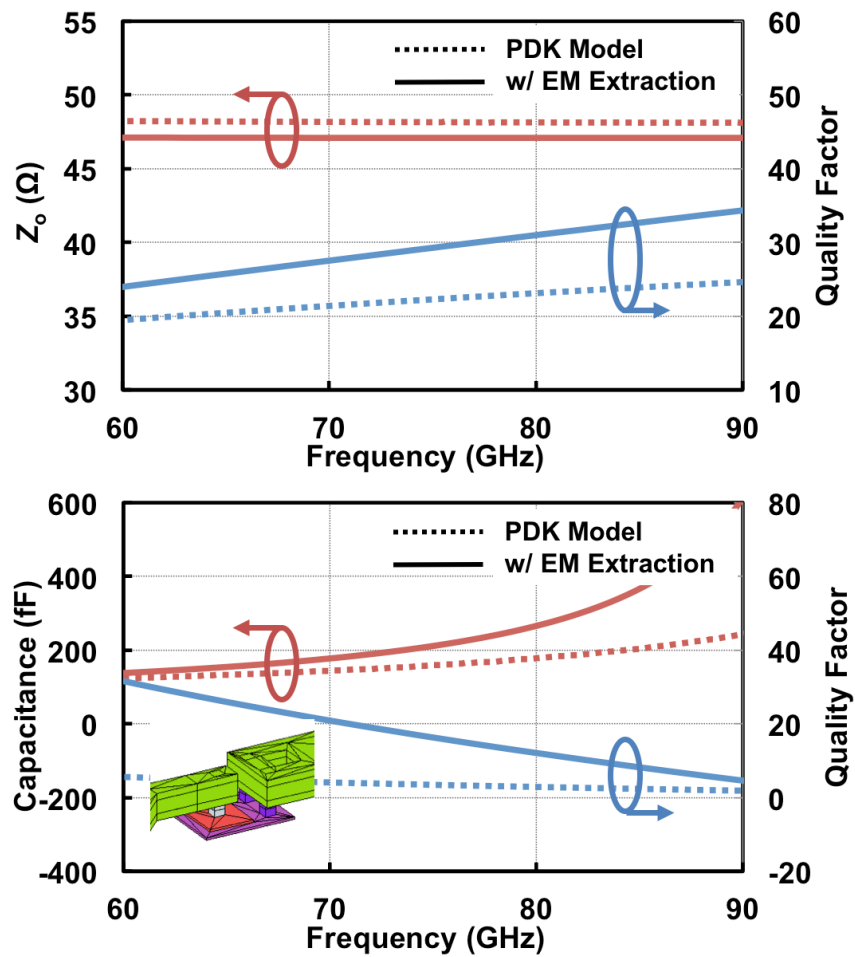
Figure 5.4: Frequency response of a 100 μm G-CPW transmission line and a 140 fF HD-MIM capacitor.

5.1.1 Power Amplifier/Low-Noise Amplifier (PALNA)

The power amplifier/low-noise amplifier (PALNA) consists of a 3-stage PA and 3-stage LNA connected through an isolation network at both the RF and mixer ports. The mode of operation is chosen by enabling the base biasing circuitry of either the PA or the LNA. There are several advantages in using the proposed output matching and isolation network instead of a T/R switch at the RF output. First, it will be shown that the loss of this output network is relatively low compare to mm-Wave T/R switches [30, 58], thus improving the overall output power of the PA and minimize the noise figure of the LNA. Second, the output network consists of only passive components and therefore is not a bottleneck of the linearity performance. The schematic of the PALNA is shown in Fig. 5.5.

LNA Design

The LNA consists of three amplifier stages. The first stage is a common-emitter with inductive degeneration provided by transmission line T_1 and is biased at the current density of 0.3 mA/μm for minimum noise. Q_1 is designed with a length of 10 μm to make the optimum source impedance R_{opt} close to 50 Ω for simultaneous noise and power matching and to minimize the base resistance r_b. The second and third stages of the LNA are common-emitter stages and are optimized for maximum gain. The interstage complex conjugate matching for the first and second LNA stages are implemented by the transmission line T_3 and capacitor C_2 and T_4 and C_3, respectively.

The input impedance seen looking into the LNA can be expressed as

$$
\begin{aligned}
Z_{\text{IN}} &= sL_1 \| Z_{PA,OFF} \| \\
&\quad (r_{b1} + r_{C1}) + \frac{g_{m1}L_2}{C_{be1}} + \frac{1}{s\left(C_{be1} \parallel C_1\right)} + sL_2 \\
&\approx sL_1 \| \left(r_{b1} + r_{C1}\right) + \frac{g_{m1}L_2}{C_{be1}} + \frac{1}{s\left(C_{be1} \parallel C_1\right)}.
\end{aligned}
\tag{5.1}
$$

L_1 and L_2 are inductors implemented using transmission lines T_1 and T_2. The inductance L_1 is chosen to resonate with $C_{be1} \parallel C_1$ at the operating frequency. At

	L (μm)
Q_1	10
$Q_{2,3,4}$	4
Q_5	2x4
Q_6	2x8

	fF
C_1	176
$C_{2,3}$	234
C_4	109
C_5	234
$C_{6,7,8}$	117

	L (μm)
T_1	160
T_2	40
T_3	70
T_4	70
T_5	200
T_6	160
T_7	40
T_8	60
T_9	50
T_{10}	180
T_{11}	180

	Tx	Rx
$V_{CC,LNA}$		1.5 V
I_{Q1}		2 mA
I_{Q2+Q3}		12 mA
$V_{CC,PA}$	1.8 V	
I_{Q4+Q5}	28 mA	
I_{Q6}	14 mA	
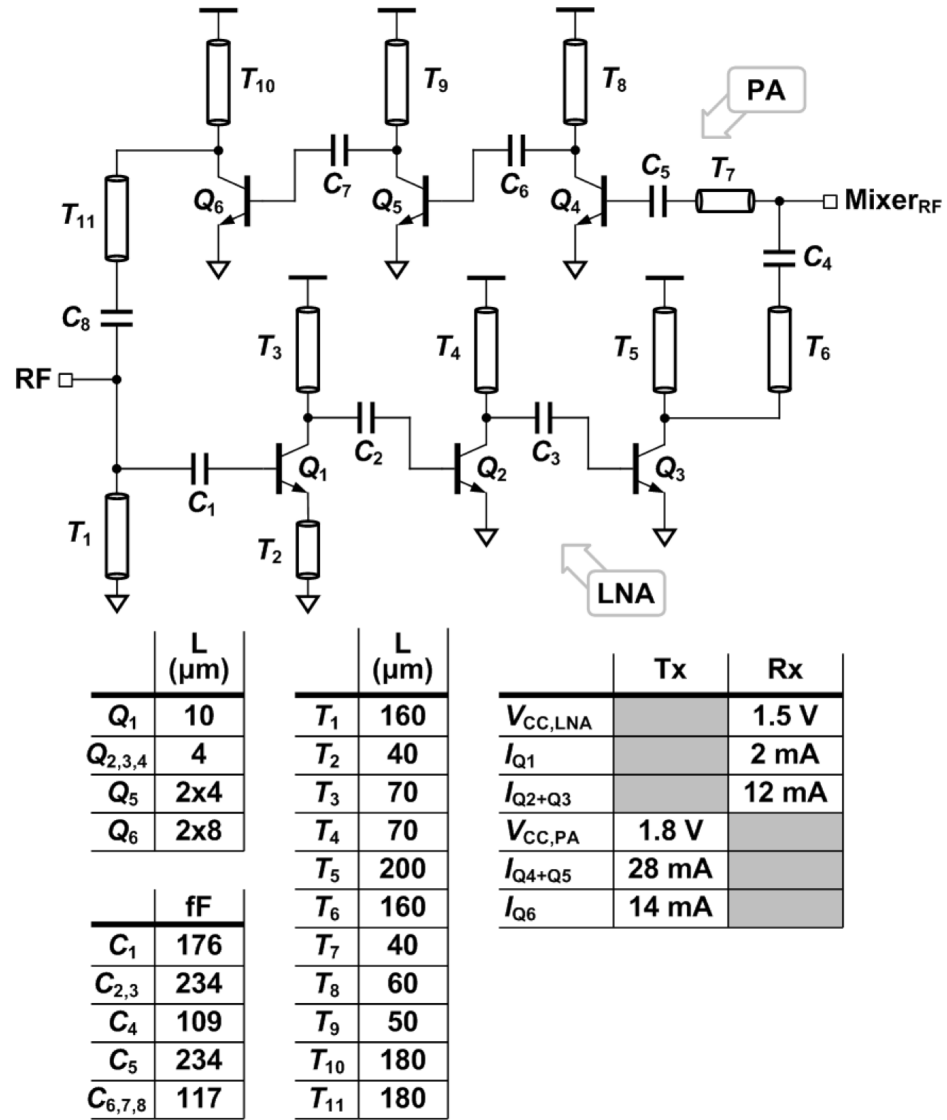
Figure 5.5: Schematic of the PALNA with associated device sizing and bias conditions (bias circuitry omitted).
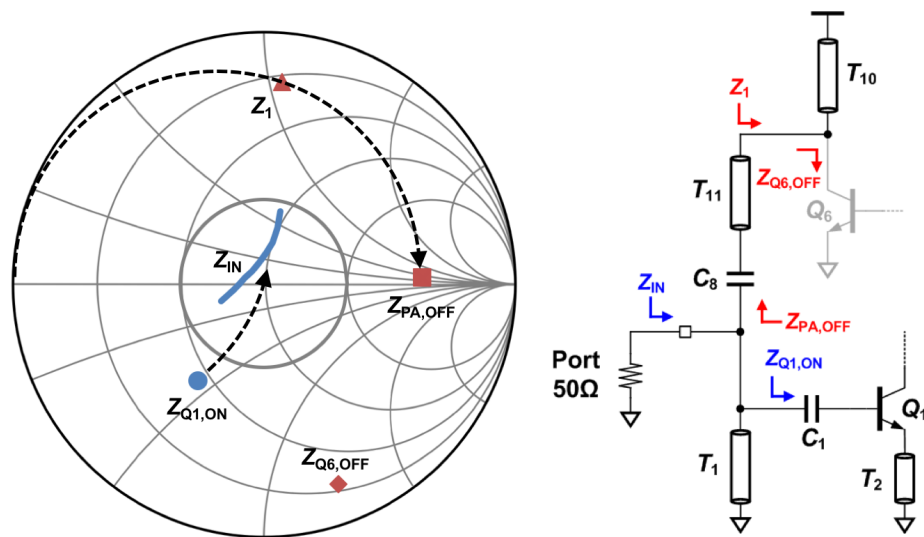
Figure 5.6: Impedance transformation in the receive mode.
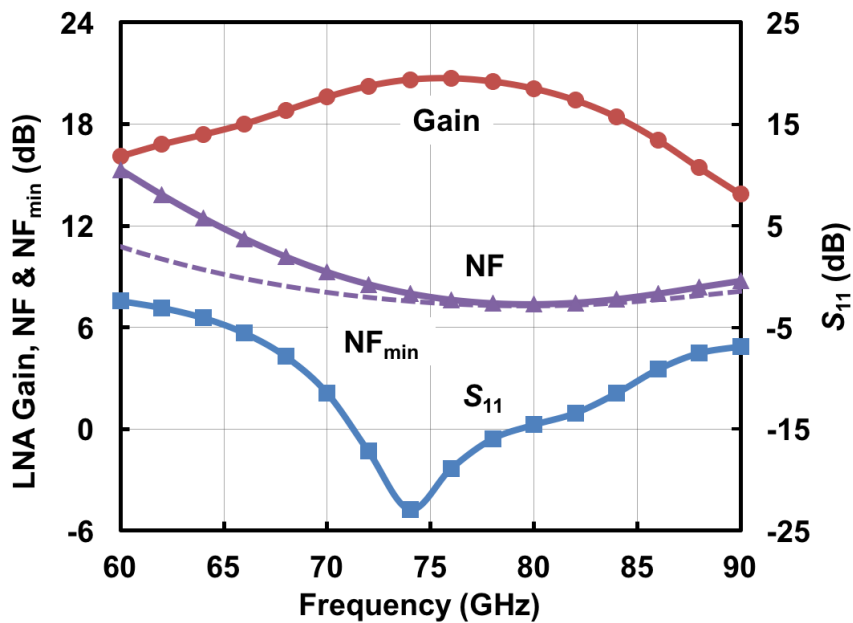
Figure 5.7: Simulated gain, NF and S_{11} of the LNA as a function of frequency.
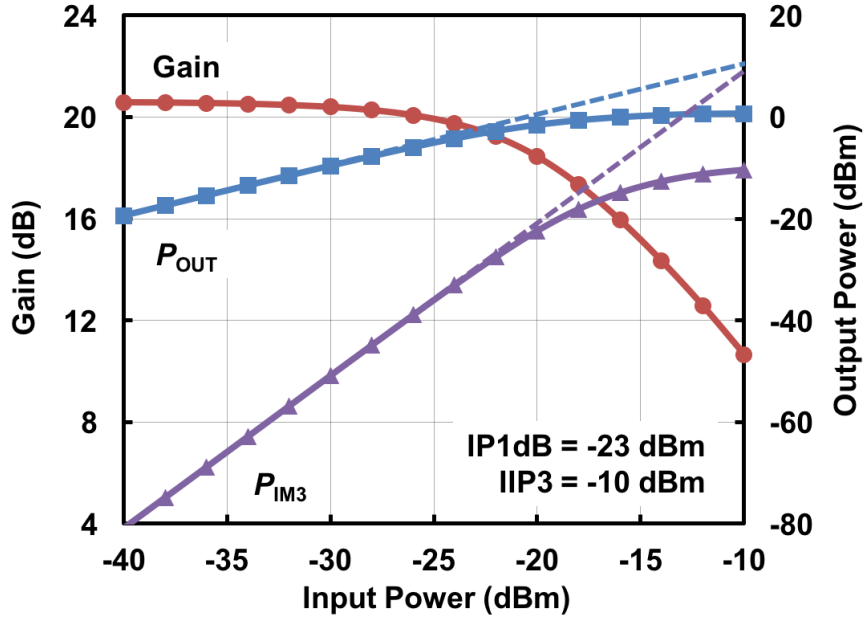
Figure 5.8: Simulated gain, output power, third order intermodulation power at 74 GHz of the LNA.

resonance, Z_{IN} can be rewritten as

$$
\begin{aligned}
Z_{\text{IN}} &= Q^2 (r_{b1} + r_{C1} + \frac{g_{m1} L_2}{C_{be1}}) \\[2mm]
&= \frac{1}{\omega_{\text{o}}^2 \left(C_{be1} \parallel C_1 \right)^2 \left(r_{b1} + r_{C1} + \dfrac{g_{m1} L_2}{C_{be1}} \right)} \approx 50 \ \Omega
\end{aligned}
\tag{5.2}
$$

where ω_{o} is the resonance frequency. With fixed device sizing and current density, this equation guides the choice of L_2. For the approximation in (5.1) to be valid and to prevent the input signal from being absorbed into the PA, the impedance of the PA in the off state ($Z_{\text{PA,OFF}}$) must be high. The device Q_6 in the off state provides an effective collector capacitance C_{c6} on the transmission line T_{10} and T_{11}.

The impedance seen looking into the PA network can be expressed as

$$
\begin{aligned}
Z_{\mathrm{PA,OFF}} &= Z_{\mathrm{o}} \frac{\dfrac{1}{sC_{\mathrm{c6}}} \parallel jZ_{\mathrm{o}} \tan\left(\beta l_{\mathrm{T10}}\right) + jZ_{\mathrm{o}} \tan\left(\beta l_{\mathrm{T11}}\right)}{Z_{\mathrm{o}} + j\left(\dfrac{1}{sC_{\mathrm{c6}}} \parallel jZ_{\mathrm{o}} \tan\left(\beta l_{\mathrm{T10}}\right)\right) \tan\left(\beta l_{\mathrm{T11}}\right)} \\[2mm]
&= jZ_{\mathrm{o}} \frac{\tan\left(\beta l_{\mathrm{T10}}\right) + \tan\left(\beta l_{\mathrm{T11}}\right)\left(1 - \omega_{\mathrm{o}} C_{\mathrm{c6}} Z_{\mathrm{o}} \tan\left(\beta l_{\mathrm{T10}}\right)\right)}{1 - \tan\left(\beta l_{\mathrm{T10}}\right)\left(\tan\left(\beta l_{\mathrm{T11}}\right) - \omega_{\mathrm{o}} C_{\mathrm{c6}} Z_{\mathrm{o}}\right)}
\end{aligned}
\tag{5.3}
$$

where a lossless transmission line is assumed and β is the propagation constant. For an ideal case where $C_{\mathrm{c6}} = 0$, (5.3) reduces to $jZ_o \tan\left(\beta\left(l_{\mathrm{T10}} + l_{\mathrm{T11}}\right)\right)$ which suggests that the total length of the transmission line T_{10} and T_{11} should be $\lambda/4$. However, this effective length is slightly reduced due the finite C_{c6}, and the additional impedance contribution of C_8. The total length of T_{10} and T_{11} are optimized in simulation to ensure high impedance.

Simulation shows $Z_{\mathrm{PA,OFF}} = 210\ \Omega$ which implies a 0.9 dB loss of received power into the PA network. The impedance transformation in receive mode is shown on the Smith chart in Fig. 5.6. The simulated peak LNA gain is 21 dB with a minimum noise figure of 7.5 dB and return loss better than 10 dB between 70 and 84 GHz as shown in Fig. 5.7. A two-tone simulation shows the LNA has an input-referred 1-dB compression point (IP1dB) of -23 dBm and an input-referred third order intercept point (IIP3) of -10 dBm in Fig. 5.8.

PA Design

The PA consists of three common-emitter amplifier stages. The first two stages are biased at approximately 2.4 mA/μm for maximum f_{t} and gain. Similar to the LNA design, T_8 and C_6 and T_9 and C_7 form interstage conjugate matching networks for the first and second stages of the PA. The final stage of the PA is optimized for maximum output power. Load pull simulations indicate the optimum output impedance Z_{opt} of approximately $35 + j15$ for maximum output power of 9 dBm.

To maximize the power delivered to the load, the load impedance of the LNA in the off state ($Z_{\mathrm{LNA,OFF}}$) must also be large. The effective input impedance
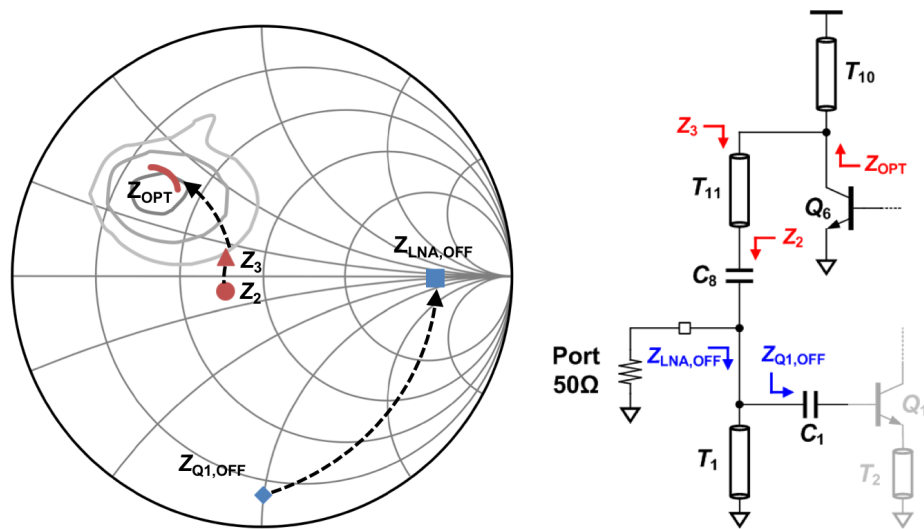
Figure 5.9: Impedance transformation in the transmit mode.
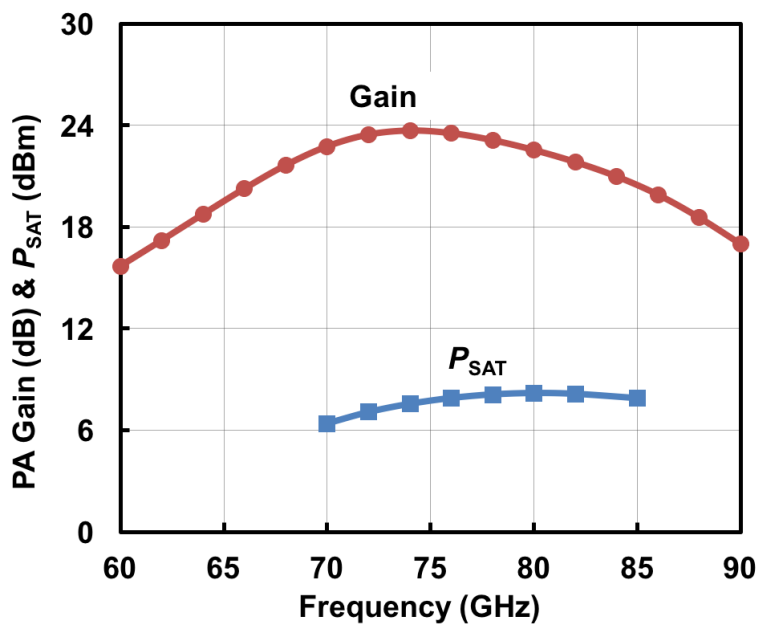
Figure 5.10: Simulated gain and P_{sat} of the PA as a function of frequency.
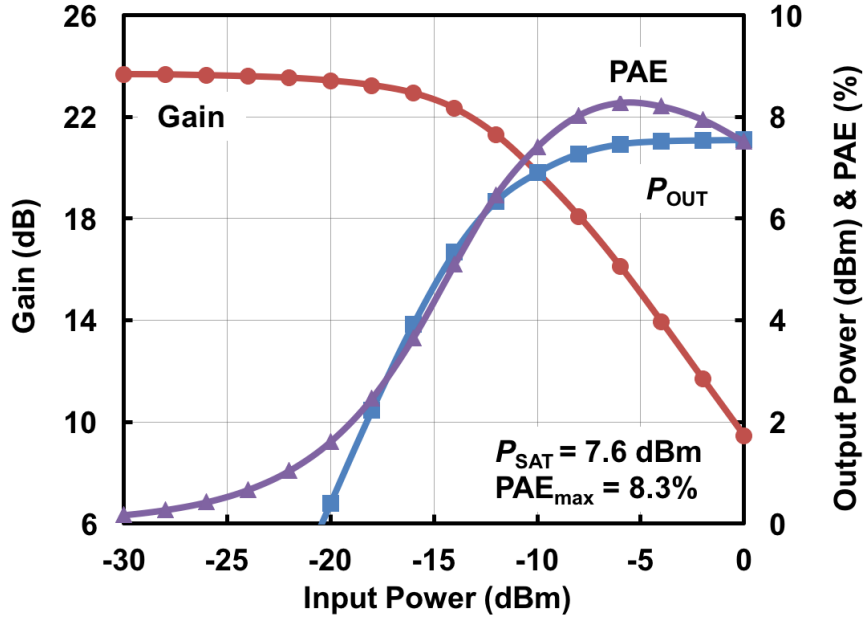
Figure 5.11: Simulated gain, output power, and PAE at 74 GHz of the PA.

seen at the base of Q_1 when the device is off is $Z_{\mathrm{Q1,OFF}} = sL_2 + 1/sC_{be1} + r_{b1} + r_{C1}$ $thickapprox 1/sC_{be1} + r_{b1} + r_{C1}$. Similar to when Q_1 is on, this impedance and the inductance created by transmission line T_1 form a parallel resonance, leaving the effective impedance of the LNA in the off state to be

$$Z_{\mathrm{LNA,OFF}} = Q^2(r_{b1} + r_{C1}) = \frac{1}{\omega_\mathrm{o}^2 \left(C_{be1} \parallel C_1\right)^2 \left(r_{b1} + r_{C1}\right)}. \tag{5.4}$$

Note that unlike in the receive mode, the additional real part created by the inductive degeneration is not present, leaving $Z_{\mathrm{LNA,OFF}}$ to be much higher than 50 Ω. Simulation shows $Z_{\mathrm{LNA,OFF}} = 275$ Ω and the output power loss due to the LNA network is approximately 0.7 dB.

With large $Z_{\mathrm{LNA,OFF}}$, the impedance looking from the output of the PA network Z_2 is close to 50 Ω. The transmission line T_{11} simply extends the 50 Ω reference plane. The shunt inductance L_{10} formed by transmission line T_{10} loads the PA,

$$L_{10} = jZ_o \tan\left(\beta l_{\mathrm{T10}}\right). \tag{5.5}$$

Equations (5.3) and (5.5) guides the selection of the length of T_{10} and T_{11}. This impedance transformation is graphically illustrated on the Smith chart in Fig. 5.9. Simulation result of the PA gain and saturation output power (P_{sat}) is shown in Fig. 5.10 with a peak gain and peak P_{sat} of 24 dB and 8.1 dBm, respectively. The simulated gain, output power, and power-added efficiency (PAE) at 74 GHz is also plotted in Fig. 5.11.

5.1.2 Passive Mixer

A passive mixer is used for both down- and up-conversion since it is inherently bidirectional. The double-balanced topology minimizes LO feedthrough and cancels even-order harmonics. The mixer is a ring of four 90-nm NFETs. The FET gates are biased through bias resistors (not shown). The center tap of the RF balun and two 10 kΩ shunt resistors are used to set DC operating points of the RF and IF port, respectively. The IF port is differential and is interfacing directly with an IF buffer. The interconnection network of the mixer is simulated up to OL metal layer using EMX to capture all parasitic effects. On-chip spiral baluns provide single-ended-to-differential conversion for the mixer RF and LO ports. The RF balun B_1 is realized with a one-turn primary inductor in the OL copper layer and a one-turn secordary inductor in the LD aluminum layer. Capacitors C_9 and C_{10} serve as DC blocking capacitors for the FET gates from the LO driver stage supply as well as provide a conjugate matching for the LO buffer. The schematic of the double-balanced passive mixer with the associate device sizing and dimensions of the RF balun are shown in Fig. 5.12.

The mixer is simulated under the loading of the PALNA in the transmit mode and IF buffer in the receive mode with the LO power of 5 dBm. Simulated results in Fig. 5.13 show the mixer and RF balun have a voltage conversion loss of -10 and -8.5 dB in the transmit and receive mode, respectively. The linearity simulation at 74 GHz of the mixer is shown in Fig. 5.14 and suggests that the mixer linearity is not a bottleneck to the overall linearity.
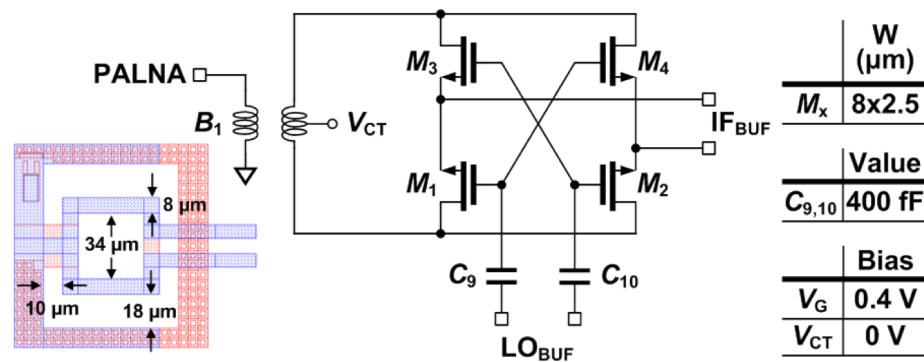
Figure 5.12: Schematic of the double-balanced passive mixer with associated device sizing and balun layout.
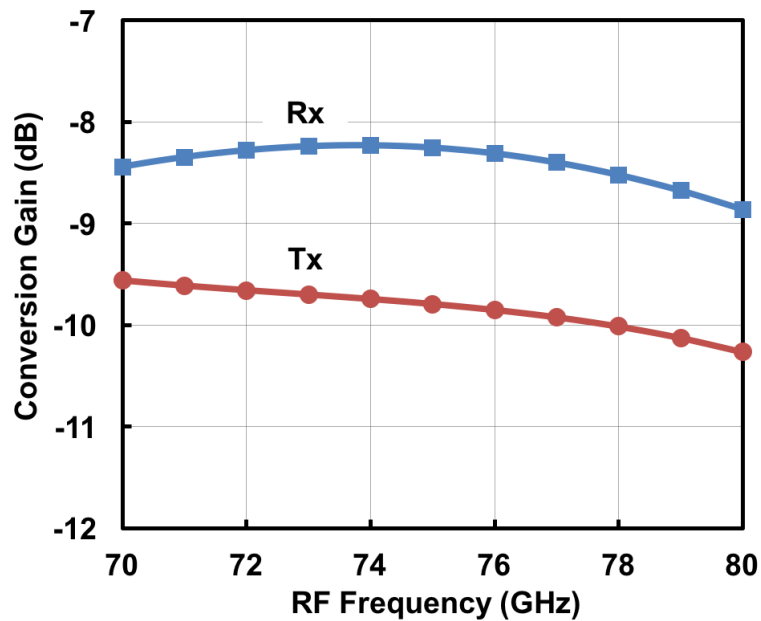
Figure 5.13: Simulated conversion loss of the mixer as a function of frequency.
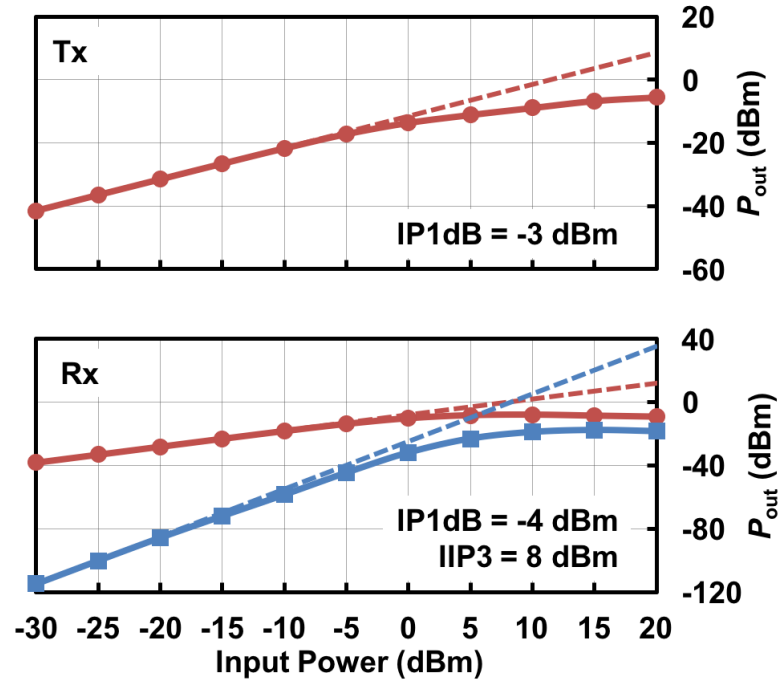
Figure 5.14: Simulated linearity of the passive mixer in transmit and receive mode.

5.2 LO Phase Shifting Using Linear Coupled Oscillators

An LO-based phase shifting architecture can be used in a beamforming transceiver. One way of creating a progressive LO phase shift is by using injection locking oscillator. The phase dynamics of an oscillator with an injection signal close to its natural frequency are described by the Adler's equation as [59]

$$\frac{d\theta}{dt} = \omega_{\mathrm{o}} - \omega_{\mathrm{inj}} + \triangle\omega_{\mathrm{m}} \sin\left(\theta_{\mathrm{inj}} - \theta\right) \tag{5.6}$$

where ω_{o} and ω_{inj} are the natural oscillation frequency of the oscillator and the injection frequency, θ_{inj} and θ are instantaneous phase of the injected signal and the oscillator, and $\Delta\omega_{\mathrm{m}}$ is the locking range determined by the coupling strength ϵ and the quality factor Q of the oscillator $\triangle\omega_{\mathrm{m}} = \epsilon\omega_o/2Q$. Under steady-state condition $\frac{d\theta}{dt} = 0$, the phase difference between the oscillator and the injected signal

is given as

$$\Delta\theta = \arcsin\left(\frac{\omega_{\text{inj}} - \omega_{\text{o}}}{\triangle\omega_{\text{m}}}\right), \tag{5.7}$$

and suggests that the maximum phase difference is $\pm 90°$ at the edge of the injection locking range ($\omega_{\text{inj}} = \omega_{\text{o}} \pm \Delta\omega_{\text{m}}$). This phase tuning can be further enhanced by using frequency multipliers M [43]. With the frequency multiplier, the phase increases proportionally to the multiplication factor, e.g. $\triangle\phi = M\triangle\theta$ where $\triangle\phi$ is the phase difference at the multiplier output.

A linear array of coupled oscillators operates according to a similar principle as injection locked oscillators. The phase dynamics of the ith bilateral coupled oscillators under injection locking are described as [60].

$$\begin{aligned}
\frac{d\theta_i}{dt} &= (\omega_i - \omega_{\text{inj}}) \\
&- \frac{\epsilon\omega_i}{2Q}\left[\sin\left(\Phi - \theta_i - \theta_{i-1}\right) + \sin\left(\Phi - \theta_i - \theta_{i+1}\right)\right] \\
&+ \frac{\rho_i\omega_i}{2Q}\sin\left(\Phi - \psi_i - \theta_i\right)
\end{aligned} \tag{5.8}$$

where ω_i and θ_i are the ith oscillator's natural frequency and instantaneous phase, ρ_i is the injection signal strength at the ith oscillator, Φ is the phase of the coupling network. The terms containing subscripts 0 or $N+1$ are ignored (at the edge of the array). An injection from one side of the array means that $\rho_1 = \rho$ and $\rho_i = 0$ otherwise. Assuming that the injection strength is the same as coupling strength $\rho = \epsilon$, a constant phase progression across the array $\triangle\theta = \theta_i - \theta_{i-1} = \theta_1 - \psi_1$ is a valid steady state solution to (5.8) provided that

$$\omega_{\text{inj}} = \begin{cases} \omega_i - 2\triangle\omega_{\text{m}}\sin\left(\Phi\right)\cos\left(\theta\right) & 1 \leq i < N \\ \omega_i - \triangle\omega_{\text{m}}\sin\left(\Phi - \triangle\theta\right) & i = N. \end{cases} \tag{5.9}$$

Assuming that the coupling network contribute no phase shift $\Phi = 0$, (5.9) can be simplified to

$$\omega_{\text{inj}} = \begin{cases} \omega_i & 1 \leq i < N \\ \omega_i + \triangle\omega_{\text{m}}\sin\left(\triangle\theta\right) & i = N \end{cases} \tag{5.10}$$

which suggests that a constant phase progression through the array is generated by only detuning of the Nth oscillator by $\pm\triangle\omega_{\mathrm{m}}\sin\left(\triangle\theta\right)$ from the injection frequency while maintaining the inner oscillators natural frequency at the injection frequency.

5.2.1   Two-Element Linear Coupled Oscillators

To demonstrate the phase shifting using coupled oscillators, the two element on-chip oscillators are linearly coupled through thin film tantalum nitride (TaN) BEOL resistors (KXRES) at both of the complementary outputs as shown in the block diagram in Fig. 5.15. An external injection signal from off-chip is applied to one end of the chip while the oscillator on the opposite end is detuned. The outputs of each oscillator are applied to the frequency multiplier chains described in the next section to provide the LO signals for the passive mixers in each of the bidirectional front-end.

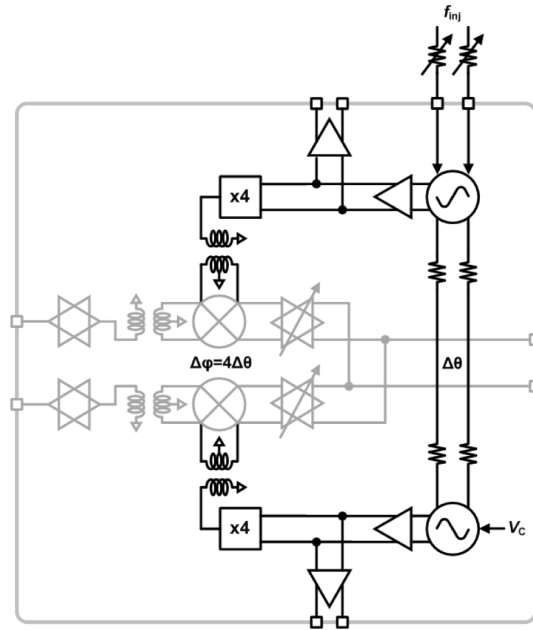**Figure 5.15**: Block diagram of the 2-element linear coupled oscillators with an external injection signal.

The cross-coupled voltage-controlled LC oscillator (VCO) is used in this design as shown in Fig. 5.16. PMOS-type single switch topology is adopted for
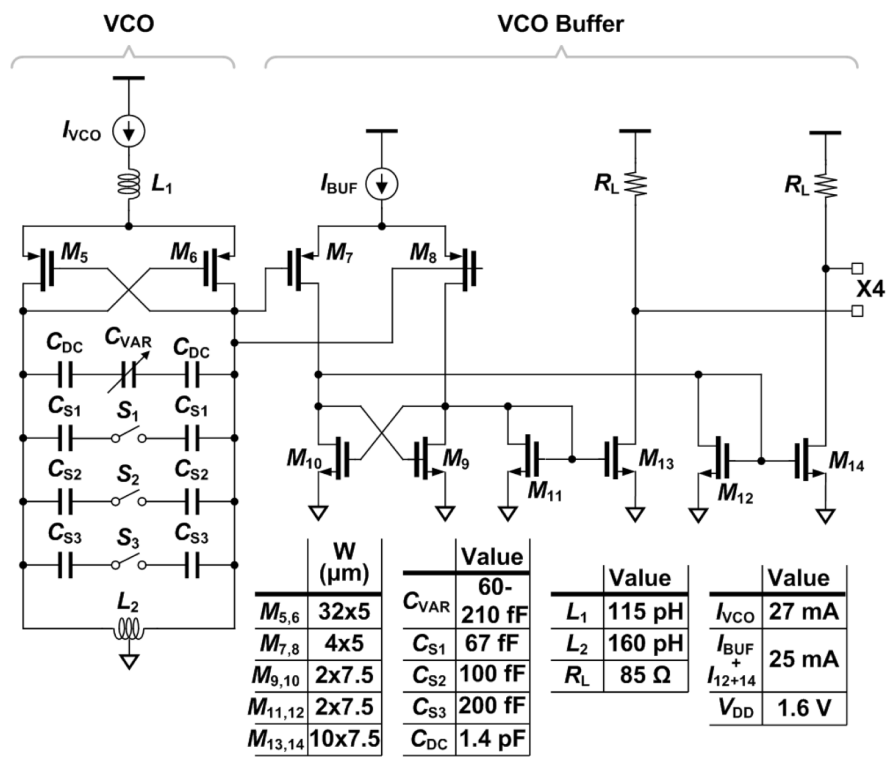
Figure 5.16: Schematic of the LC voltage-controlled oscillator and its output buffer with associated device sizing and bias conditions.

minimum flicker noise. Inductor L_1 is inserted on top of the cross-coupled PMOS pair to minimize the flicker noise contribution of the current source. Inductor L_2, varactor C_{VAR} and a 3-bit digital capacitor banks $C_{\mathrm{S1-S3}}$ form a resonance load. The VCO has a simulated tuning range between 15.5–16.6 GHz and K_{VCO} of 200 MHz/V. A differential amplifier with cross-coupled load is used as VCO output buffer. The simulated differential swing at the output of the buffer is 1.2 V_{pp}.

5.2.2 Frequency Multiplier Chain

The frequency multiplier chain consists of four different circuit blocks as shown in Fig. 5.17. The first block is the differential VCO buffer tuned for the 16 GHz fundamental frequency. The output matching of the buffer is designed using a differential spiral inductor L_3 and HD-MIM capacitors C_{11} and C_{12} . This buffer provides enough swing to compensate for the 6 dB loss of the two-stage RC polyphase filter. The polyphase filter provides differential to quadrature conversion of LO waveform to drive the frequency quadrupler stage. The KXRES is also used in the polyphase filter for good matching and low temperature variation. Simulation of the polyphase filter shows a maximum gain mismatch of 0.4 dB with an operating bandwidth from 9 to 19 GHz.

The frequency quadrupler consists of the transconductor devices Q_{21-24}. When driven with quadrature waveforms, the combined collector current exhibits a fourth harmonic component which is buffered to the output via a cascode amplifier Q_{25}. The inductance created by the transmission line T_{10} resonates with the collector capacitance of the quadrupler and input capacitance of the buffer device at $4f_\mathrm{o}$. The LO output power at $4f_\mathrm{o}$ is amplified using a cascode LO buffer consisting of Q_{26} and Q_{27}. The LO buffer is loaded with the balun B_2 that performs single-ended to differential conversion of the LO signal. The balun has an OL copper as primary inductor and LD aluminum secondary inductor with the dimensions shown in Fig. 5.17.

Fig. 5.18 shows the transient waveforms at each stage of the LO chain. The VCO input is modelled as a 16 GHz sinusoidal source with a 1.2 V_{pp} differential swing. The VCO buffer at node A gives 3 V_{pp} differential swing. Node B shows
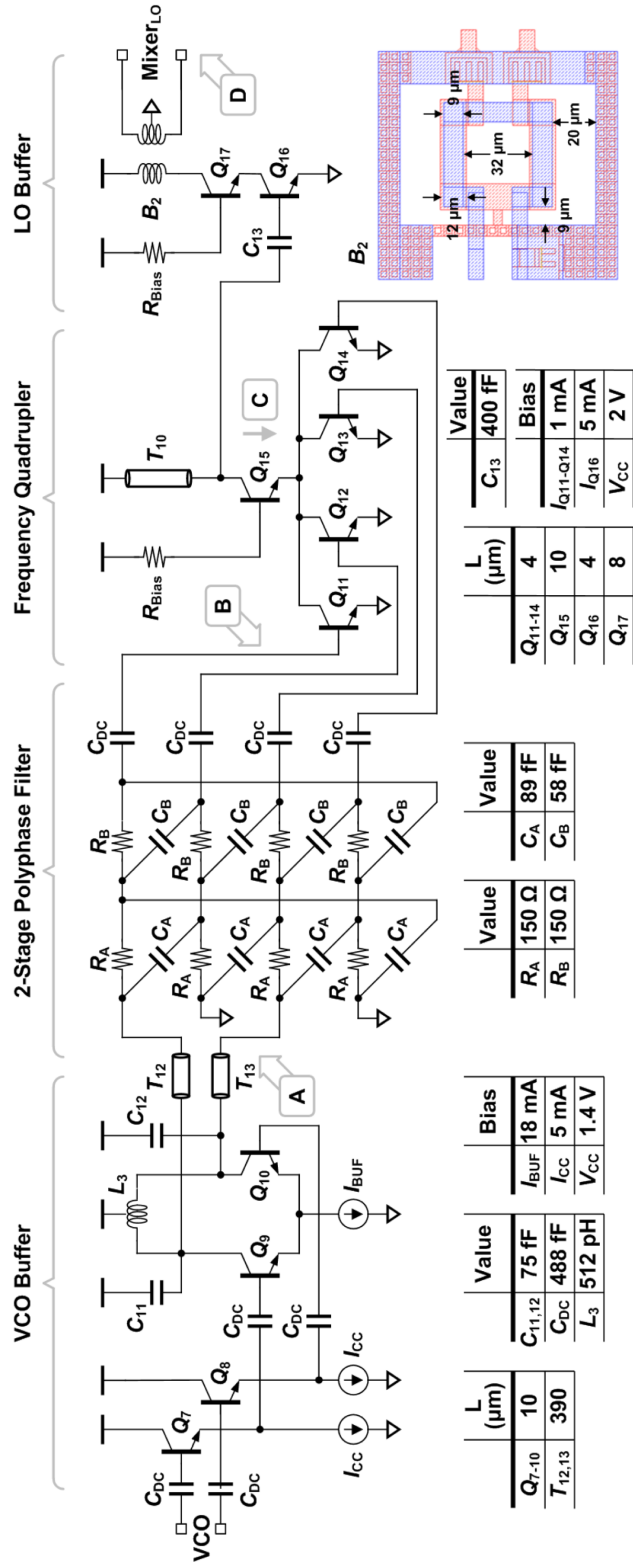
Figure 5.17: Schematic of the LO chain with associated device sizing and bias conditions. The LO chain consists of four blocks: VCO buffer, 2-stage polyphase filter, frequency quadrupler, and LO buffer.

the quadrature signals at the input of the frequency quadrupler with 400 mV$_{\text{pp}}$ swing. The fourth harmonic content can be observed in the quadrupler collector current (C). Finally, the differential voltage swing at the gates of the mixer at node D is shown with a 0.8 V$_{\text{pp}}$ swing.

Figure 5.18: Transient waveform at each node of the LO chain.

5.2.3 IF Buffer

A bidirectional IF buffer is added to each of the channels for IF power combining/splitting. The buffer consists of a differential receive and transmit amplifier connected in an anti-parallel loop as shown in Fig. 5.19. The mode of operation

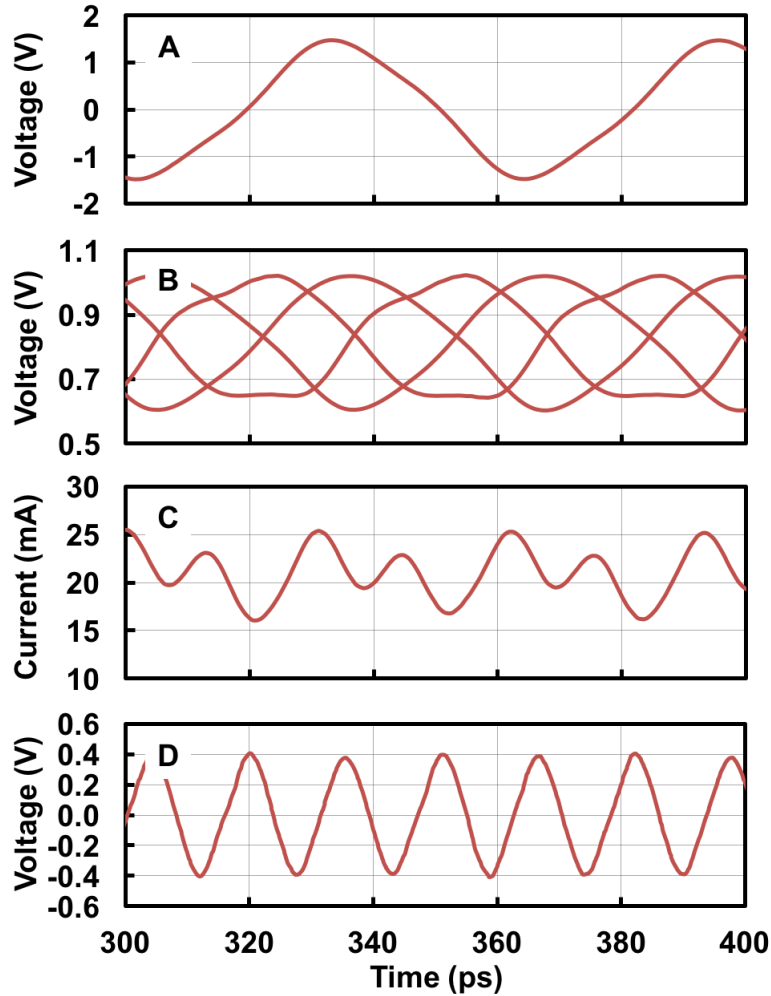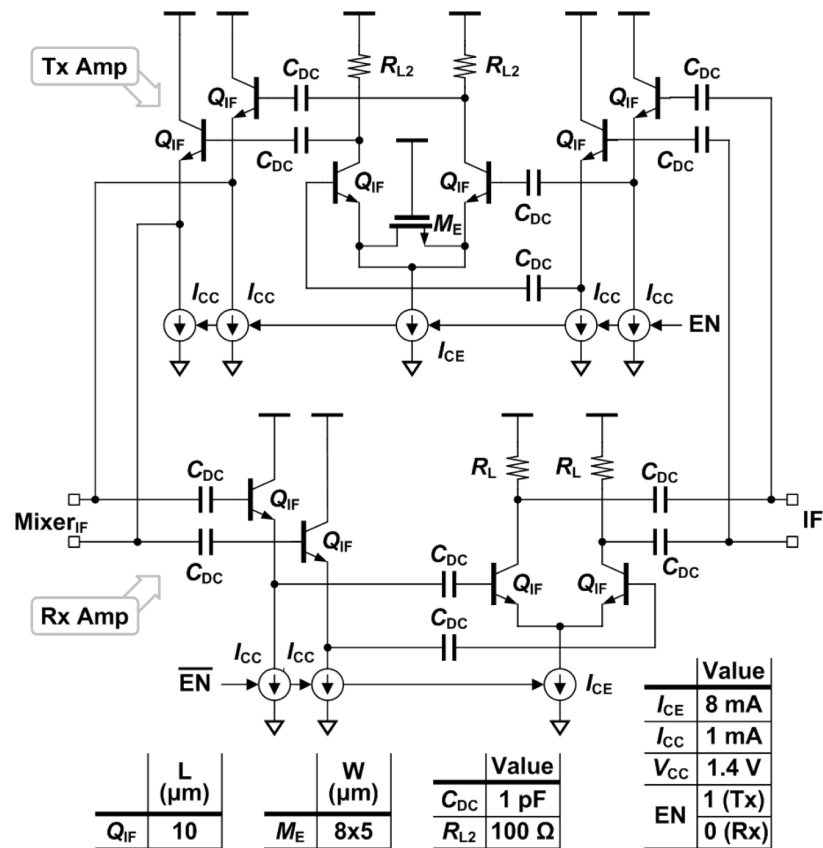**Figure 5.19**: Schematic of the IF buffer with associated device sizing and bias conditions.

of the IF amplifier is chosen with an enable bit that turns on and off the current biasing network of the respective amplifier. The differential receive buffer consists of a two-stage cascaded emitter follower (EF) and a common-emitter (CE) stage. The EF stage is used to reduced the effective resistance seen at the input node of the CE stage to help improve the bandwidth. The transmit buffer is similar with the addition of a EF stage at the output. The CE stage is degenerated with a MOS transistor operating in triode region in order to improve linearity performance in the transmit mode. The additional EF output stage is used to isolate the noise contribution of the load resistances of the CE stage from the input of the receive buffer. Simulation results of the IF buffer show peak gain of 8.7 and 8 dB in the transmit and receive mode, respectively, with 3-dB bandwidth of approximately 15 GHz. The transmit IF buffer has simulated P_{sat} of -6 dBm while the receive IF buffer has a simulated noise figure of 6.5 dB.

5.3   Experimental Result

The prototype two-element, 70-GHz bidirectional front-end is fabricated in a 90-nm BiCMOS process ($f_{\text{t}}/f_{\text{max}}$ of 280/320 GHz). The die microphotograph is shown in Fig. 5.20. The circuit measures 2.4 mm $\times$ 1.47 mm. The front-end consumes 42 mA from a 1.8 V supply in the transmit mode and 14 mA from a 1.5 V in the receive mode. The VCO, frequency multiplier chain, and buffers for each of the chain nominally consume 117 mW from 1.4 V and 2 V supplies.

5.3.1   Bidirectional Front-End Measurement

The bidirectional PALNA and mixer are evaluated using on-chip probing at RF, LO and IF. The return loss of the RF and LO are measured using the Agilent E8361A two-port network analyzer, Agilent E5260A mm-Wave extender, and Picoprobe 110 GHz GSG probe and plotted in Fig. 5.21. The measured RF input return loss is better than 10 dB from 68−80 GHz. The minimum LO return loss is slightly shifted from the designed 64 GHz to 70 GHz partly due to the focused ion beam (FIB) modification at the LO port.
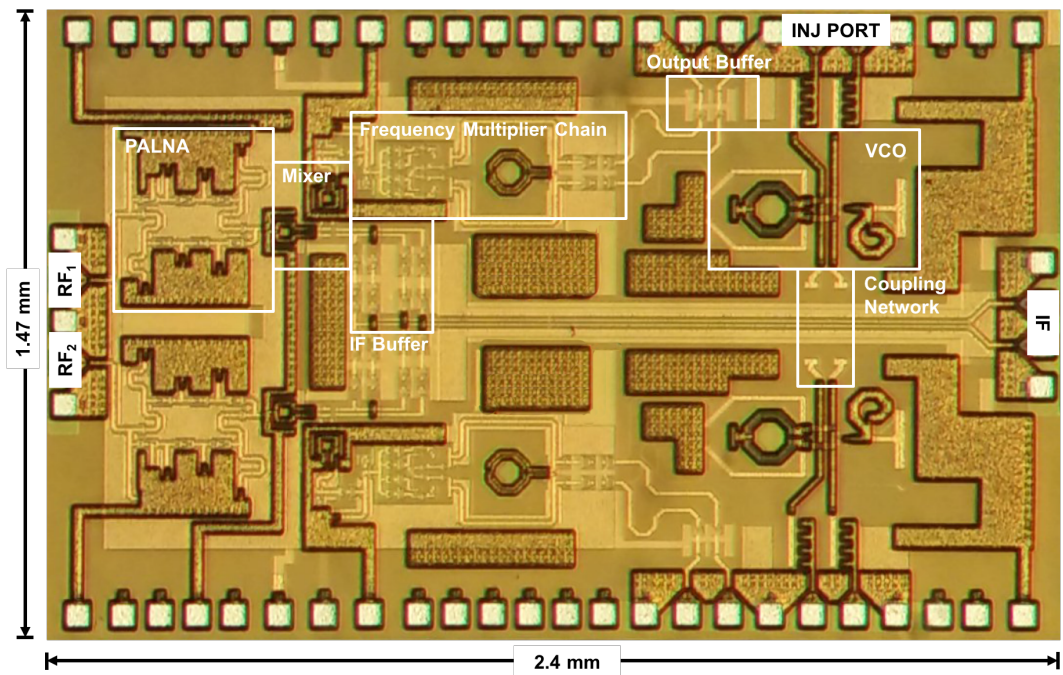
Figure 5.20: Die microphotograph of the two-element, 70-GHz bidirectional front-ends with linear coupled oscillators in 90-nm BiCMOS technology.
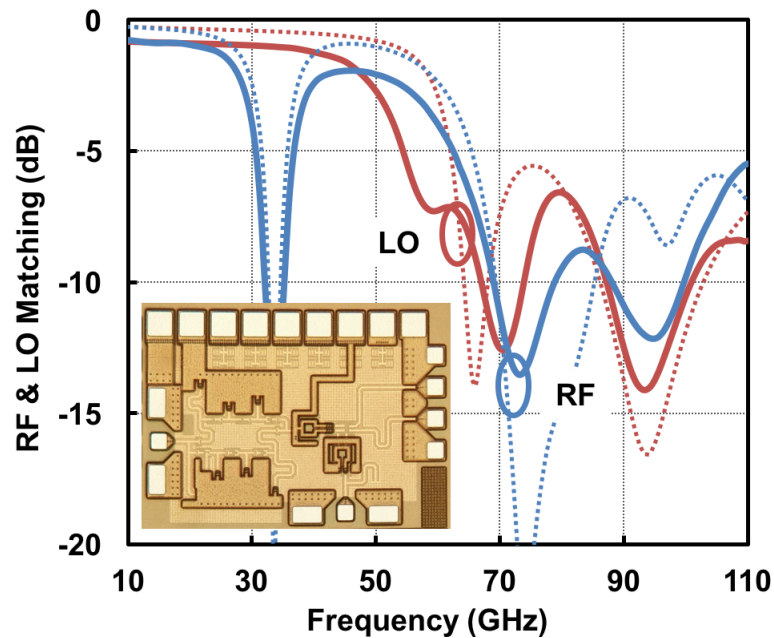
Figure 5.21: Measured (solid) and simulated (dotted) RF and LO port matching of the bidirectional PALNA and mixer front-end (pictured).
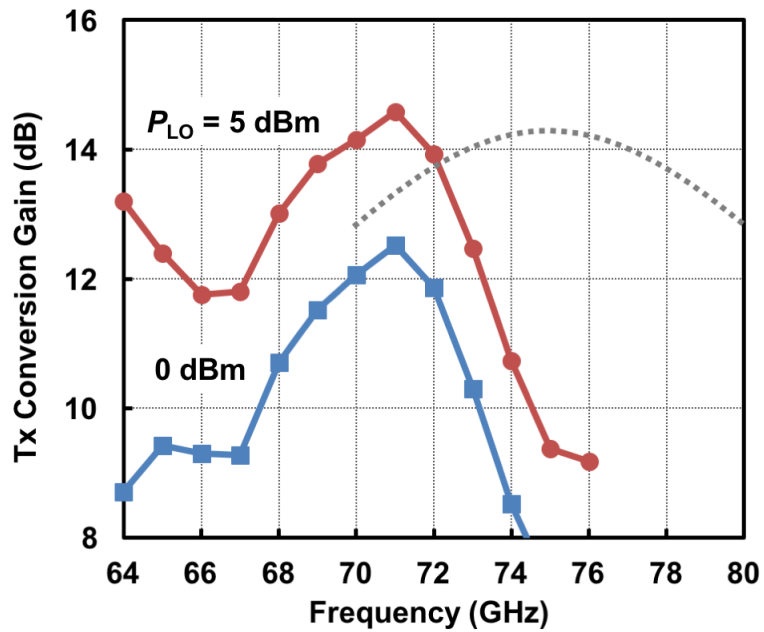
Figure 5.22: Measured conversion gain in the transmit mode for LO power of 0 and 5 dBm (solid) and simulated conversion gain (dotted).
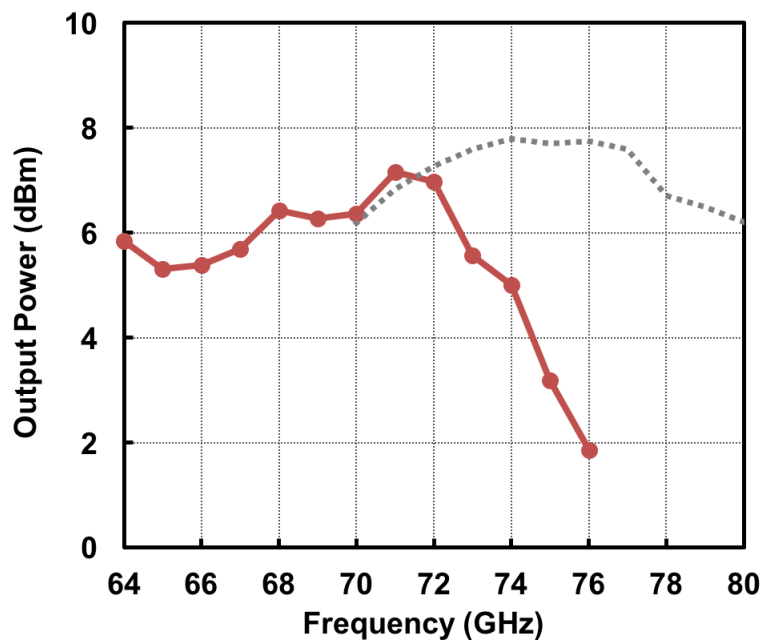
Figure 5.23: Measured (solid) and simulated (dotted) saturated output power as a function of frequency of the transmit mode.

Conversion gain and output saturation power are characterized in the transmit mode. The Anritsu 68269A/NV 40 GHz signal generator and a 180° hybrid provides a differential IF input from $4-16$ GHz. The IF input loss is characterized to the probe tip across the frequency range. The LO signal is provided by the Agilent E8257D 67 GHz signal generator. The RF port is probed using a WR-10 waveguide probe and the Agilent W8486A power meter is used for the power measurement. Although WR-10 waveguide is recommended for measurements at W-band (75–110 GHz), it can be characterized down to 64 GHz. Fig. 5.22 shows the measured transmitter conversion gain for LO power of 0 and 5 dBm. The transmitter has a peak conversion gain of 14.5 dB with a 3-dB bandwidth between 66–73 GHz. Peak P_{sat} of 7.1 dBm is measured at 71 GHz and remains above 5 dBm across the 3-dB bandwidth as shown in Fig. 5.23.

In the receive mode, the Agilent E8257D 67 GHz signal generator and the Pacific Millimeter Products E3 E-band frequency tripler provide the 64–76 GHz RF input signal. A 10-dB coupler is used for power monitoring with the Agilent W8486A power meter connected to the direct path and the RF probe connected to the coupled path, providing the receiver with a small-signal input. LO signal is distributed in the same manner as in the transmit mode. The differential IF outputs are combined off-chip through a 180° hybrid and the output power is monitored by the Agilent E4448A spectrum analyzer. Fig. 5.24 shows the receive mode conversion gain of 9.9 dB with a 3-dB bandwidth approximately between 66–73 GHz.

Two input tones at 70 and 69.95 GHz are generated using the Pacific Millimeter E3 and W3 frequency triplers and combined through a W-band magic tee. The receiver linearity is plotted in Fig. 5.25 with a IP1dB of -23 dBm and an IIP3 of -15 dBm.

Gain method is used for the receiver noise figure measurement as illustrated in Fig. 5.25. In order to observe the change in the noise floor, an IF amplifier with 30 dB gain and 3 dB NF is inserted between the 180° hybrid and the spectrum

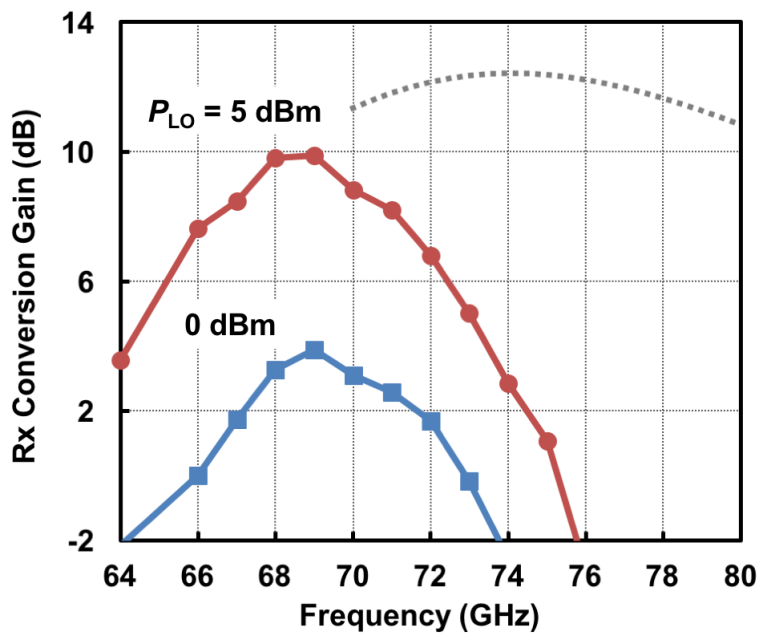**Figure 5.24**: Measured conversion gain in the receive mode for LO power of 0 and 5 dBm (solid) and simulated conversion gain (dotted).
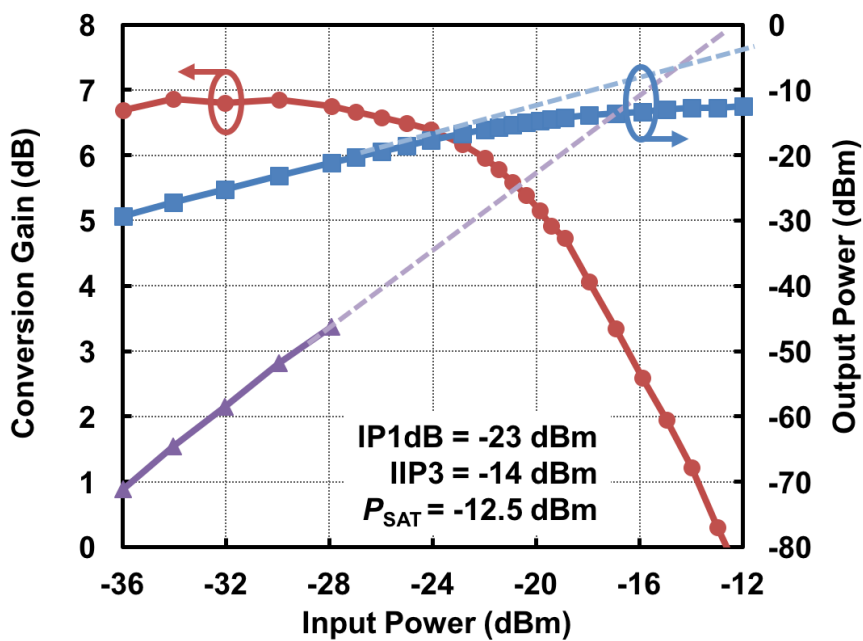

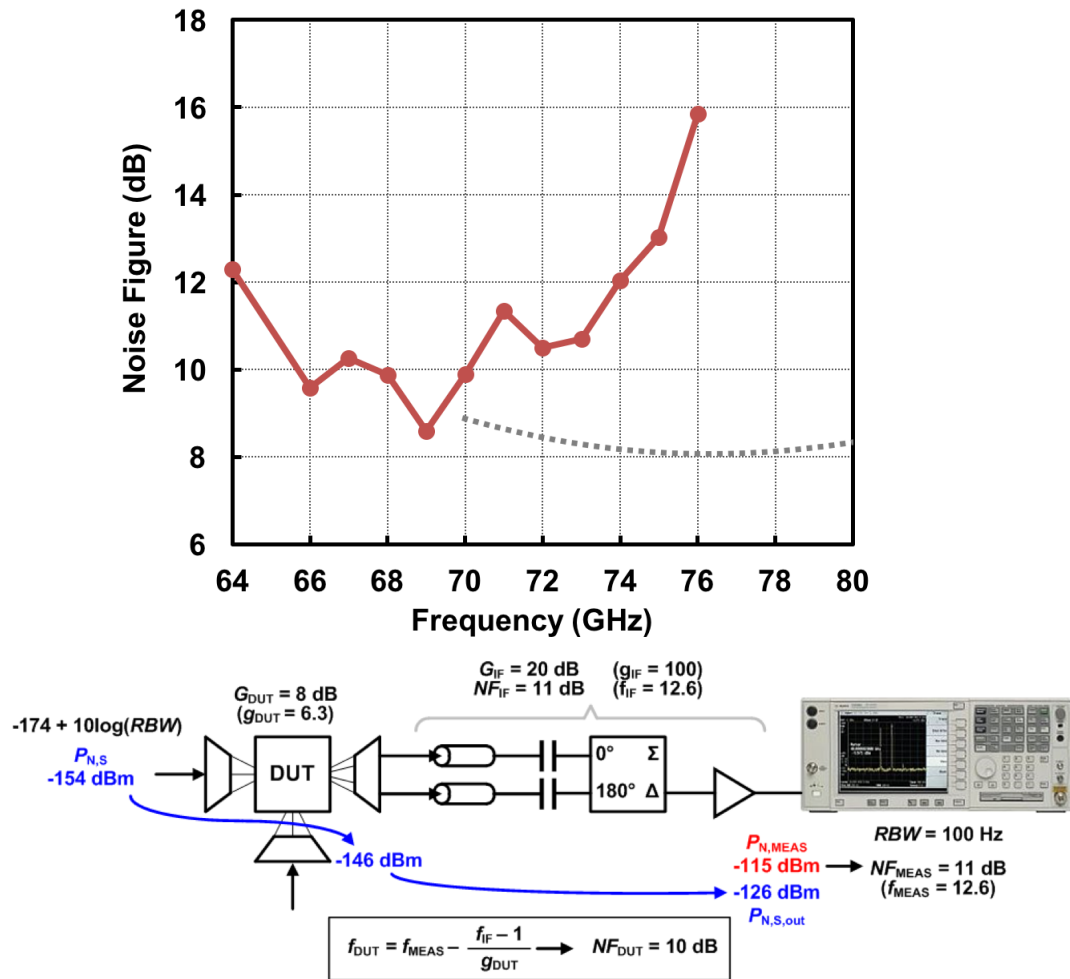**Figure 5.25**: Two-tone linearity measurement of the receive mode.

Figure 5.26: Measured noise figure (solid) and simulated noise figure (dotted) of the receiver with the associate measurement setup and example calculation at 70 GHz.

analyzer. The noise figure of the receiver is then calculated using the Friis formula,

$$f_{\text{DUT}} = f_{\text{MEAS}} - \frac{f_{\text{IF}} - 1}{g_{\text{DUT}}} = 10^{\left(\frac{P_{\text{N,MEAS}} - P_{\text{N,S,out}}}{10}\right)} - \frac{f_{\text{IF}} - 1}{g_{\text{DUT}}}. \qquad (5.11)$$

Fig. 5.26 shows the receiver noise figure as a function of frequency as well as an example of noise figure calculation at 70 GHz. The receiver has a minimum noise figure of 8.6 dB at 69 GHz.

The slight shift in the center frequency of the front-end is attributed to the use of HD-MIM capacitor in the signal path. The HD-MIM indicated approximately four times higher Q in EM simulation when compared to the design kit model. The overall lower Q of the HD-MIM capacitor suggests the use of vertical-natural capacitor (VNCap) or a custom metal-oxide-metal (MOM) capacitor.

5.3.2   VCO and LO Beamforming

The two-element array is evaluated with the chip bonded to the printed circuit board. A differential buffer is designed for VCO output measurement. The differential injection signal is provided by the Agilent E8257D 67 GHz signal generator and an external $8-26.5$ GHz hybrid coupler. The Agilent E4448A spectrum analyzer is used to monitored the output oscillation frequency and for the phase noise measurement.

The tuning curves of the VCO are plotted in Fig. 5.27. The VCO is tunable from $14.3-15.35$ GHz across 8 digital states or 8.75% tuning range with K_{VCO} of 220 MHz/V. This tuning range is approximately 1 GHz downshifted from the simulated value. The LO tuning range shown in Fig. 5.28 is characterized by giving a fixed 7 GHz IF tone and observing the RF output frequency in the transmit mode as the VCO is tuned. A V-band external harmonic mixer is used in conjunction with the Agilent E4448A spectrum analyzer to monitor the RF spectrum. The LO tuning range is from $58.25-61.4$ GHz. The last digital state of the oscillator is not usable because the oscillation frequency has fallen outside of the operating bandwidth of the frequency multiplier chain.

Fig. 5.29 shows the phase noise of a free-running and locked phase noise of the VCO at 15 GHz. The free-running VCO shows a phase noise of -109 dBc/Hz at
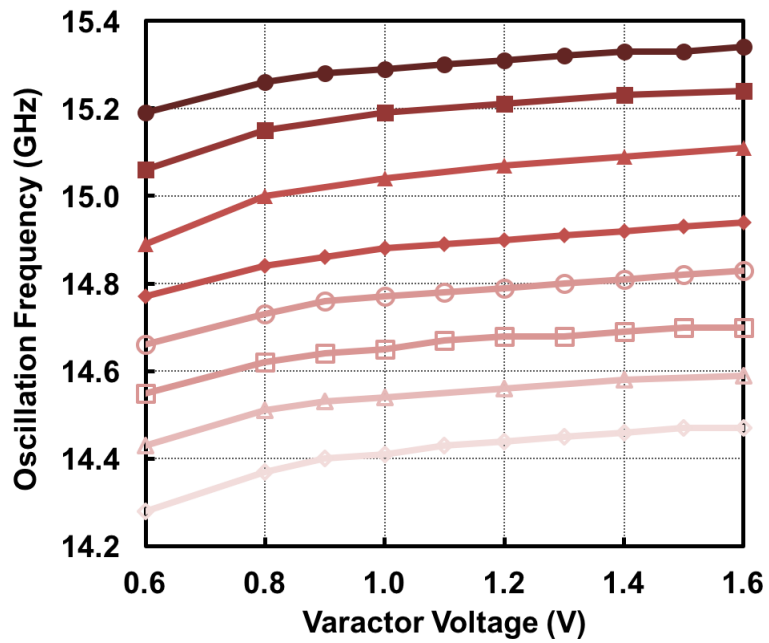
Figure 5.27: Measured tuning curves of the VCO as a function of varactor bias voltage.
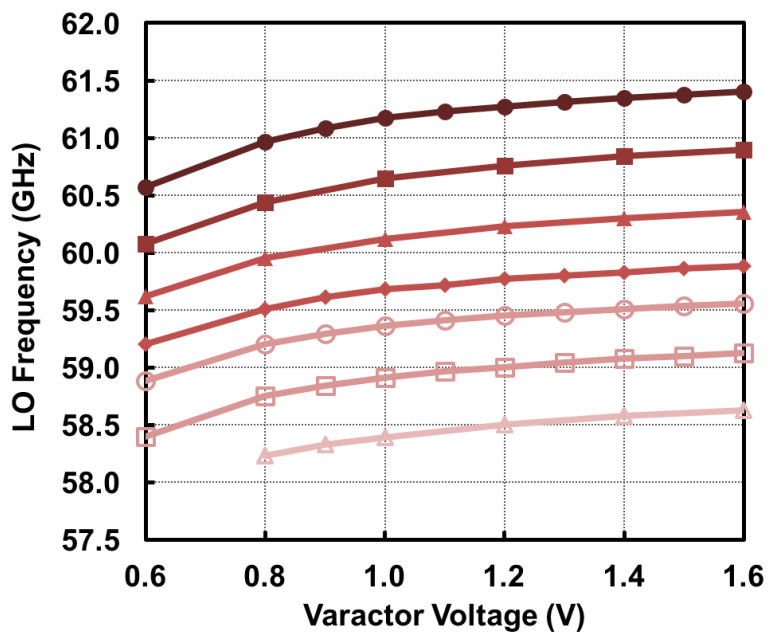

Figure 5.28: Measured tuning curves of the LO signal as a function of varactor bias voltage.
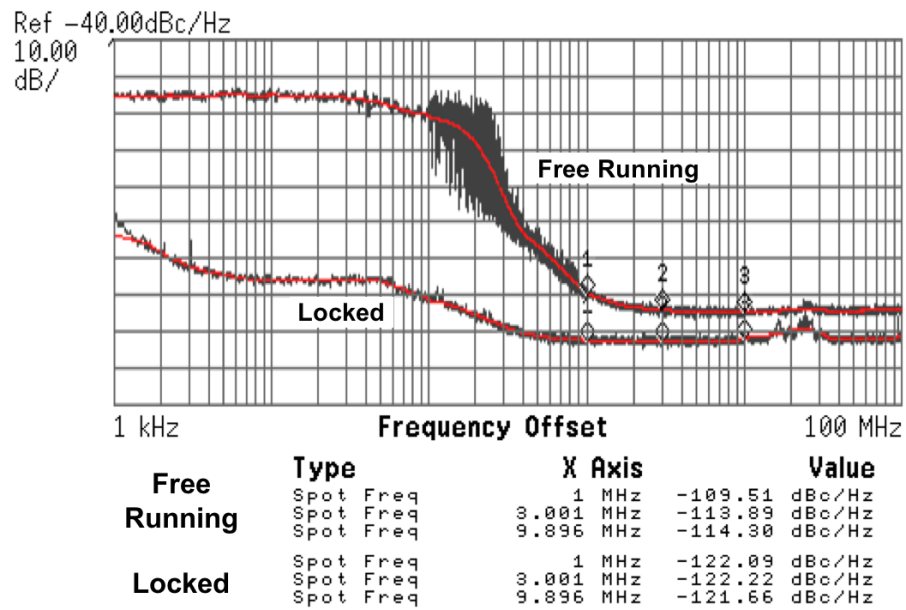
Figure 5.29: Measured free-running and injection locked oscillator phase noise.
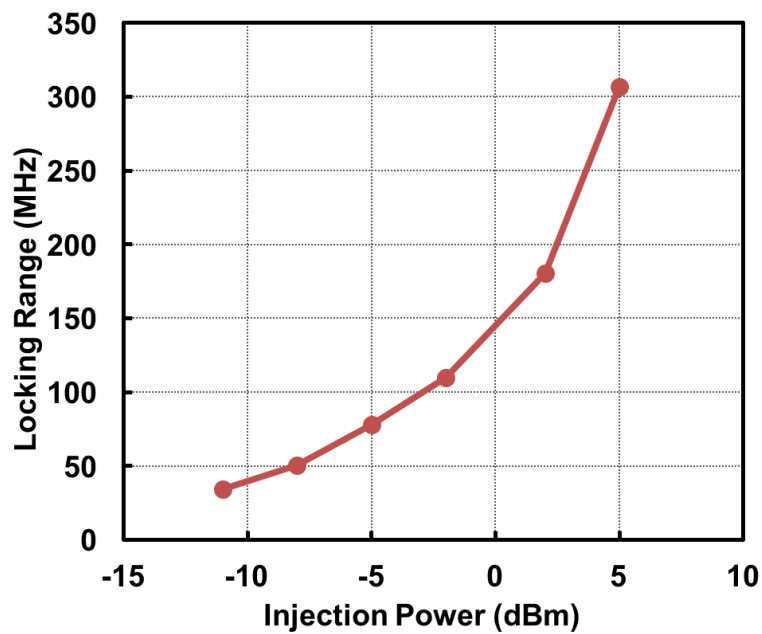
Figure 5.30: Measured injection locking range as a function of injection power.

1 MHz offset. The locked oscillator has a phase noise of -122 dBc/Hz at 1 MHz off-set. The locking range as a function of injection power is plotted in Fig. 5.30. The array exhibits a locking range of 305 MHz with an injection power (de-embedded to the edge of the printed circuit board) of 5 dBm.
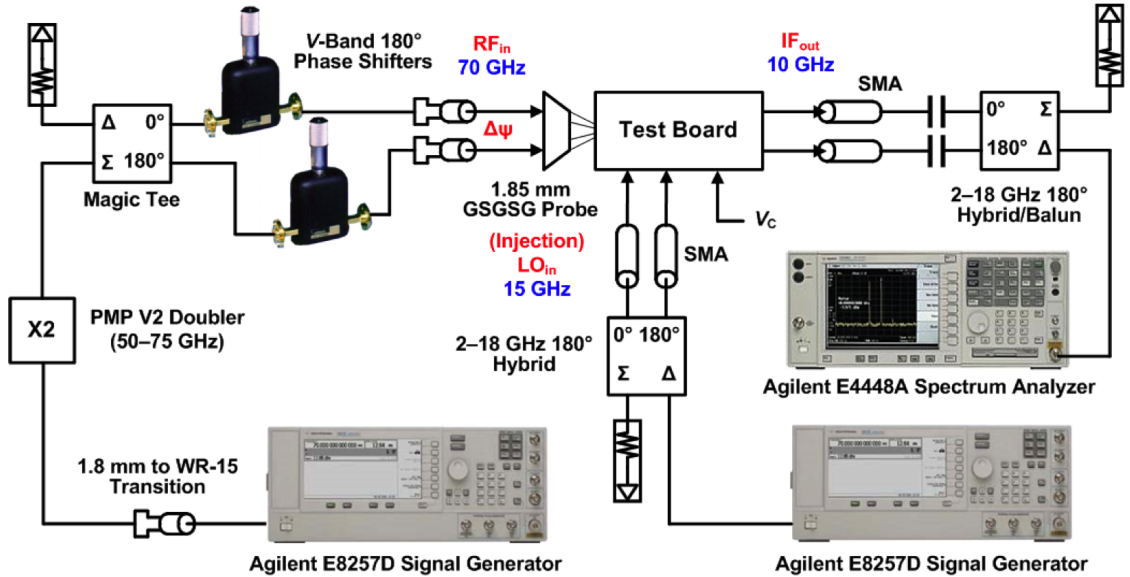
Figure 5.31: LO phase shifting measurement setup.

LO phase shifting is measured by observing the change in the downcon-verted IF power in the receive mode. The measurement setup is shown in Fig 5.31. A 35-GHz RF signal provided by the Agilent E8257D 67 GHz signal generator drives the Pacific Millimeter V2 V-band frequency doubler to give a 70-GHz RF signal. A V-band magic tee splits the RF signal and two V-band phase shifters emulate the incident angle of the RF input. A 50 GHz GSGSG probe is used to deliver the small-signal RF inputs to both of the receivers. The differential IF outputs are combined off-chip through the 180° hybrid and the output power is monitored by the Agilent E4448A spectrum analyzer.

To determine the relative phase difference between the two LO signals, the RF phase shifters are first set to locate a notch in the IF power ($\Delta\psi = 180°$) when the two VCOs are locked and tuned at the same frequency ($\Delta\phi = 0°$). Next, the edge VCO is detuned and one of the RF phase shifter is tuned to locate a new notch location. The new angle of the RF phase shifter indicates the phase difference
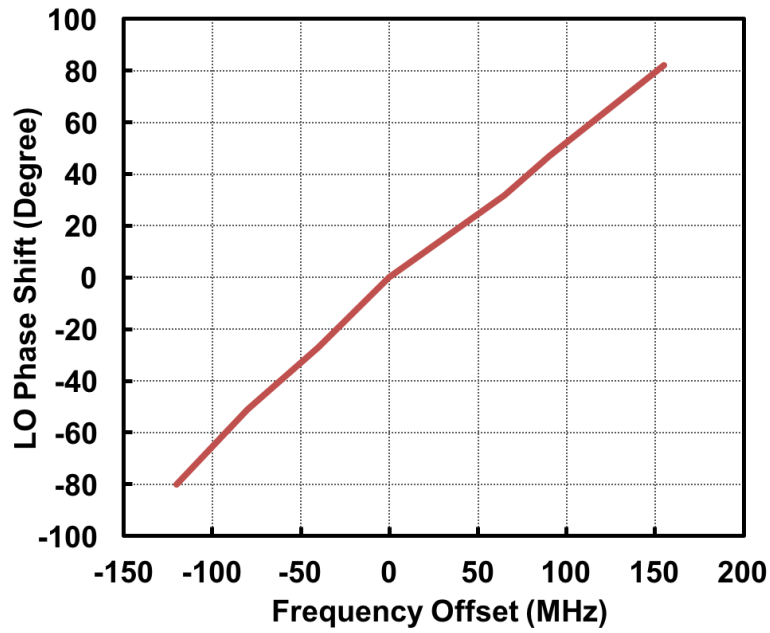
Figure 5.32: Measured LO phase shifting as a function of frequency offset.
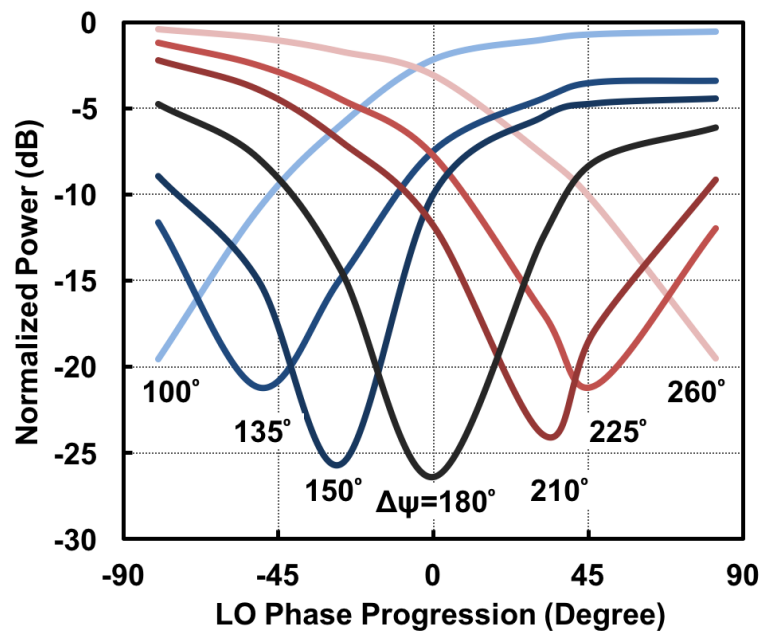
Figure 5.33: Measured normalized IF power as a function of LO progressive phase ($\Delta\phi$) for different RF input angles ($\Delta\psi$).

between the LO signals. This process is repeated for different VCO tuning voltages and the relative LO phase as a function of frequency offset is plotted in Fig. 5.32. The measurement shows a maximum LO progressive phase shift of $\Delta\phi = \pm80°$ which translates to a $\Delta\theta = \pm20°$ phase progression between the two oscillators. Fig. 5.33 plots the normalized IF power as a function of LO progressive phase for different RF input angles. Although the measurement is limited by the resolution and the accuracy in the characterization of RF phase shifters, it can be observed that the LO progressive phase is continuously tunable to locate a notch at different RF angles.

5.4   Conclusion

A 70-GHz bidirectional front-end was demonstrated for half-duplex systems in a 90-nm SiGe BiCMOS process. A passive impedance transformation network isolated the PA and LNA, eliminating a mm-Wave transmit/receive switch. The circuit achieved a saturated output power of 7.2 dBm and conversion gain of 14.5 dB and 9.9 dB in transmit and receive mode, respectively, and a minimum noise figure of 8.6 dB. The front-end was integrated with a two-element linear coupled oscillators and the maximum phase progression in the LO signal of $\pm80°$ was demonstrated by the detuning of the edge oscillator. This architecture allowed for the array to be easily scaled linearly either on-chip or possibly from chip-to-chip.

Acknowledgements

Chapter 6

SiGe High-Speed Track-and-Hold Amplifier

Geometry scaling in silicon processes has enabled CMOS and SiGe HBT technologies to be used in the design of high-speed mm-Wave circuits and systems. Here, a high-speed track-and-hold (THA) is presented to demonstrate the capability of the SiGe BiCMOS process. The performance of the THA serves as a benchmark for the technology and illustrates its competitiveness with the state-of-the-art III-V InP processes for high-speed mm-Wave designs.

6.1   Track-and-Hold Amplifier Design

Like its name suggests, a track-and-hold amplifier is a sampling circuit that passes the input signal to the output during the track mode and maintains the last input value during the hold mode. The THA consists of, in the simplest form, a sampling switch driven by a clock signal followed by a capacitor. During the track mode, the switch is closed and the input voltage signal is transferred to the capacitor and the output. The capacitor retains the previous input value when the switch is open during the hold mode. The waveforms of an ideal track-and-hold is illustrated in Fig. 6.1.

In a bipolar technology, a sampling switch is implemented using a switched emitter follower (SEF) architecture shown in Fig. 6.2. The SEF consists of two
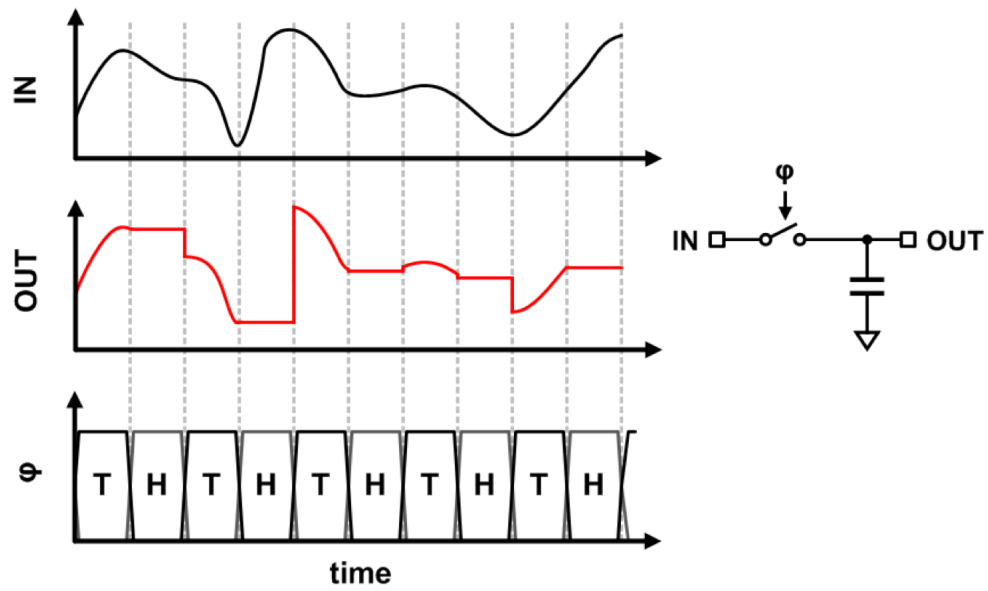
Figure 6.1: Operation of a track-and-hold circuit.
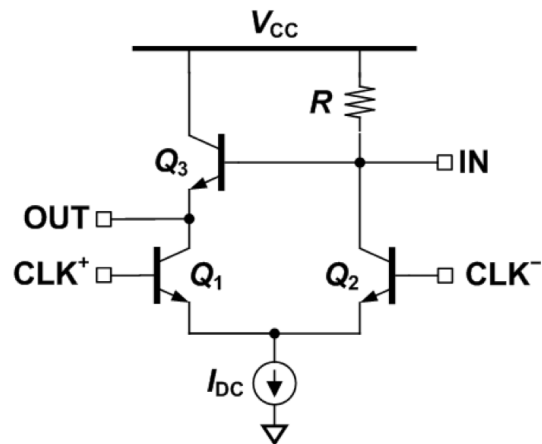
Figure 6.2: The switched emitter follower architecture.

switching transistors Q_1 and Q_2 and an emitter follower device Q_3 [61]. During the track mode shown in Fig. 6.3(a), the device Q_1 is on and Q_3 forms an emitter follower that buffers the input to the output. In the hold mode (Fig. 6.3(b)), Q_2 is on and the current is drawn through the resistor R. The voltage drop across R must be large enough to turn off Q_1.

(a)

(b)
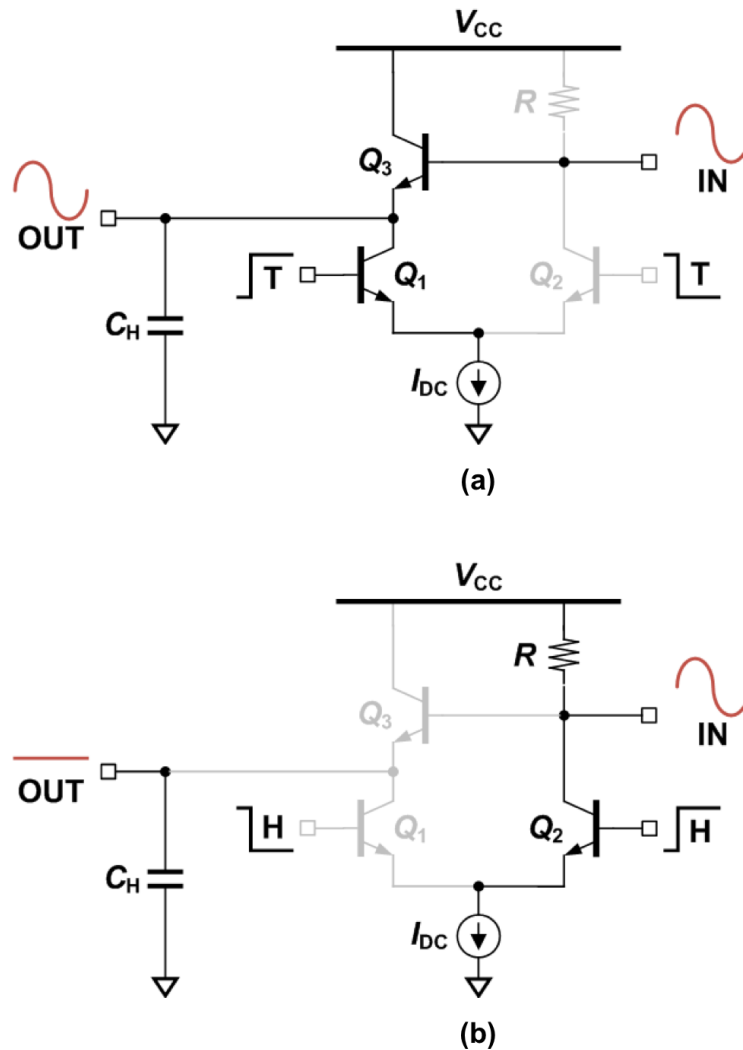
Figure 6.3: SEF in (a) track and (b) hold mode.

6.2 A 50 GS/s Track-and-Hold Amplifier in 90-nm SiGe BiCMOS Circuit Design
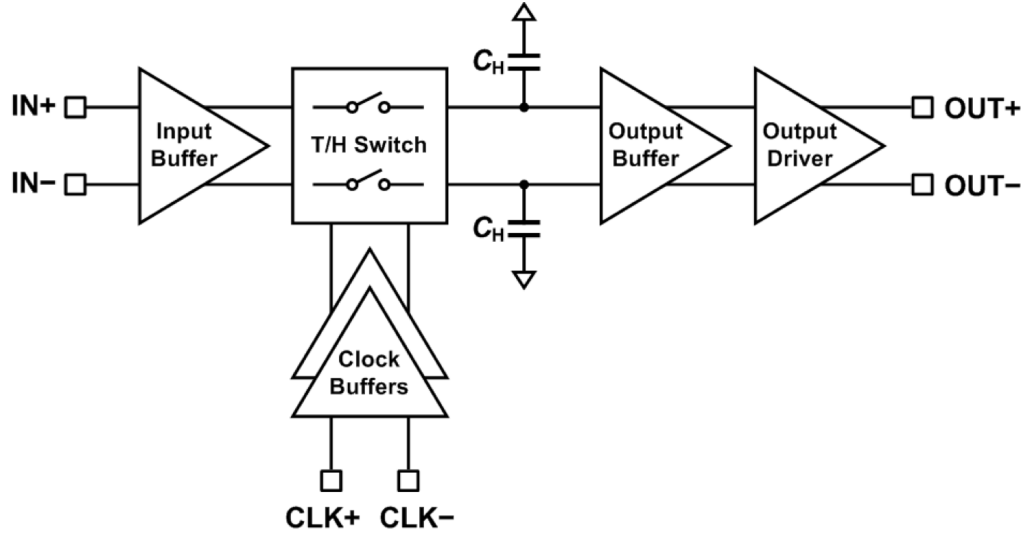
Figure 6.4: Block diagram of the proposed 50 GS/s track-and-hold amplifier.

Fig. 6.4 shows a block diagram of the proposed 50 GS/s THA. The THA is fully differential where the track-and-hold switches are driven by an external differential clock signal. At the input is a buffer that provides a single-ended impedance match to 50 Ω. The buffer is a two-stage emitter follower (EF) followed by a differential cascode common-emitter amplifier (CE). The CE amplifier is heavily degenerated to ensure that the buffer is not the bottleneck of the overall THA linearity. The schematic of the input buffer and its bias condition is shown at the center of Fig. 6.5

The input buffer is followed by two switched emitter followers utilizing switched cascode current sources to drive the hold capacitors C_H. Fig. 6.5 shows the bias condition of the SEFs when operating in the track mode (left side) and hold mode (right side). Note that in actual operation, these two switches will always be in the same mode. In the track mode, Q_8 and Q_{10} are conducting and Q_7 forms an emitter follower that buffers the input to the output. In the hold mode, Q_{14} and Q_{16} are on and the voltage drop across R_L shuts off Q_{12}. Two cross-coupled capacitors C_F are used to offset the signal which feeds through the
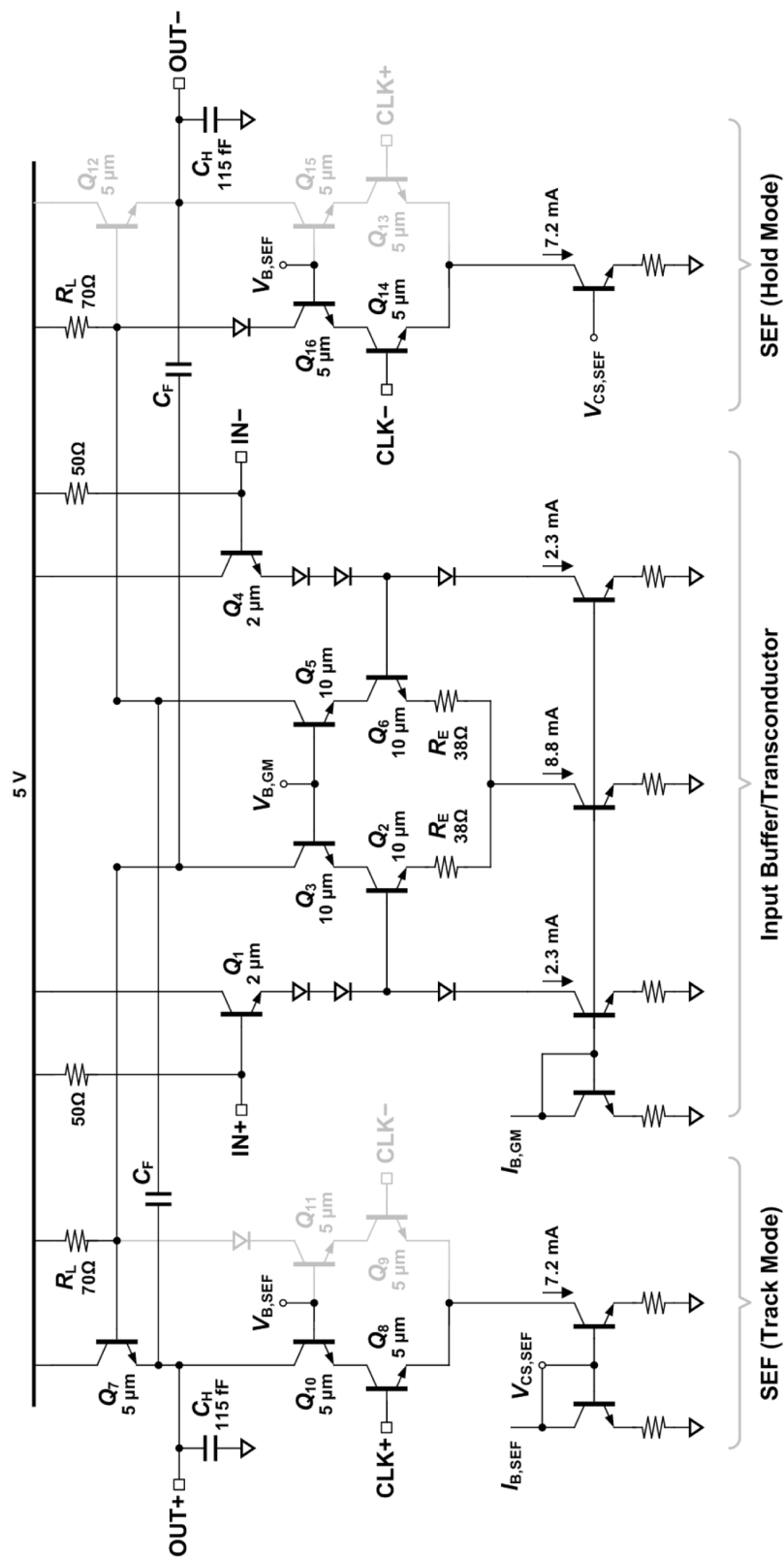
Figure 6.5: Schematic of the input buffer and the switched emitter followers with associated device sizing and bias condition.
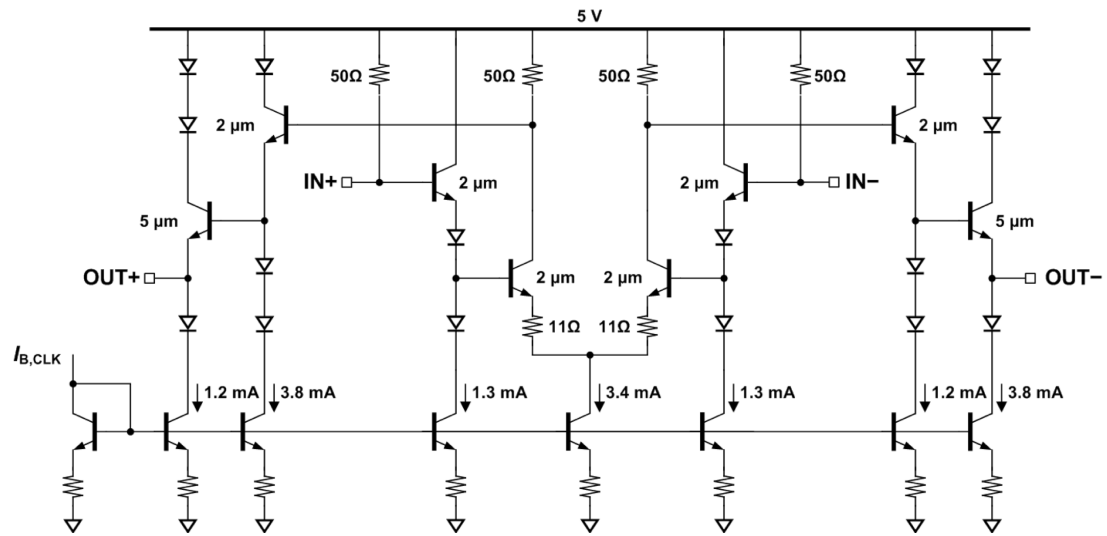
Figure 6.6: Schematic of the clock buffer chain with associated device sizing and bias condition.
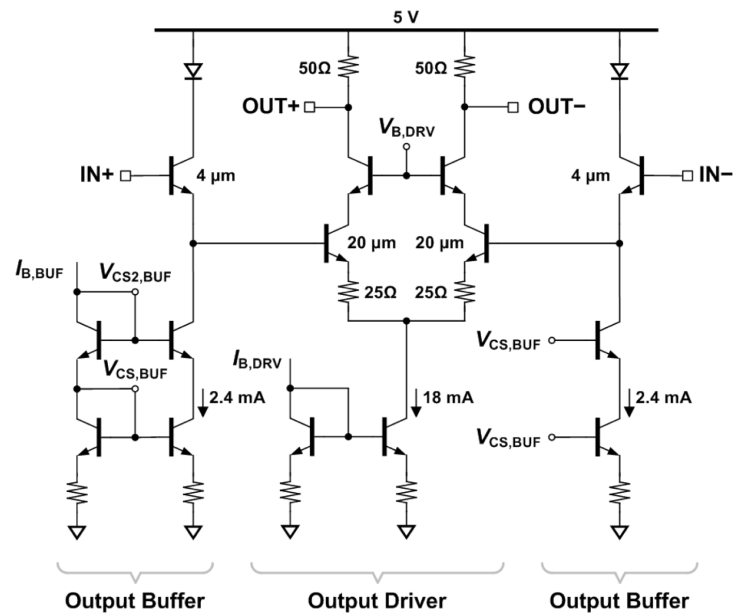
Figure 6.7: Schematic of the output buffer with associated device sizing and bias condition.
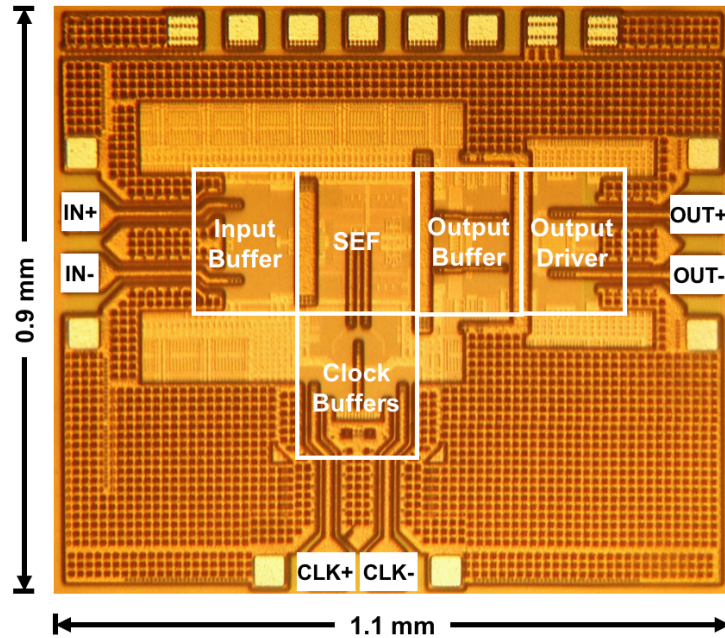
Figure 6.8: Die microphotograph of the 50 GS/s track-and-hold amplifier implemented in a 90-nm SiGe BiCMOS process.

C_{be} of Q_7 and Q_{12} in the hold mode [61, 62]. These capacitors are implemented with two series diodes in order to track the parasitic C_{be} of the switches across process. Nominally, the differential SEF consumes 72 mW.

A 4-stage differential clock buffer shown in Fig. 6.6 is driven by an external differential clock signal with with 0.6 V_{pp} swing. The first EF stage is matched to 50 Ω by a resistor from the base of the device to the supply. This is followed by a differential CE amplifier and two EF stages to provide the correct DC level and low output impedance to the switches. The clock buffer nominally consumes 80 mW and has a simulated small-signal 3-dB bandwidth of 64 GHz.

The differential CE output driver is designed to drive an external 50 Ω load. Matching is provided by a 50 Ω thin film tantalum nitride back-end-of-line (BEOL) load resistor which has a low temperature coefficient and minimal parasitics. Heavy resistive degeneration (25 Ω) is added to enhance the linearity of the output stage. Preceding the driver is a EF output buffer that isolates the SEF from the output driver. The schematic and bias conditions of the output buffer

and driver are depicted in Fig. 6.7. The output buffer and the 50 Ω output driver nominally consume 24 mW and 90 mW, respectively. The complete THA in track mode has a simulated small-signal 3-dB bandwidth of 25 GHz.

6.3   Experimental Result

The 50 GS/s THA is implemented in a 90-nm SiGe BiCMOS process with a simulated peak f_t of 280 GHz. The die microphotograph is shown in Fig. 6.8. The THA measures 0.9 mm × 1.1 mm and consumes 108 mA from a 5 V supply. All tests are conducted on a probe station.

Single-ended S-parameters are measured using the Agilent N5242A 26.5 GHz 4-port network analyzer. The complimentary input and output are terminated with 50 Ω loads. The THA is forced into a track mode by applying a 5 V and 4.5 V DC signals through external bias tees to the CLK+ and CLK- ports, respectively. These voltages are switched for the hold mode measurement. The simulated and measured S-parameters are shown in Fig. 6.9 . The 3-dB bandwidth of the THA in the track mode is 25 GHz while the hold mode input to output isolation is better than 40 dB over the entire band. The input (S_{11}) and output (S_{22}) return losses remains better than 10 dB over the 3-dB bandwidth.

Time domain measurement is conducted using the test setup shown in Fig. 6.10. The two outputs of the THA are displayed on channel 1 and 2 of the oscilloscope and the differential waveform is obtained by subtracting the two outputs using the internal mathematical function. To ensure proper alignment of the single-ended outputs, the input signal is turned off and the two outputs are aligned by minimizing the common-mode feedthrough of the clock. Fig. 6.11(a) shows the single-ended and differential time domain waveforms of a 12.5 GHz signal sampled at 50 GS/s. The differential waveform is superimposed on a 12.5 GHz reference in Fig. 6.11(b).

Harmonic distortions are characterized for the single-ended output. The differential input signal is provided by the Agilent E8257D signal generator with a 5 kHz−11 GHz balun for measurement up to 5 GHz and a 6−26.5 GHz 180° hybrid
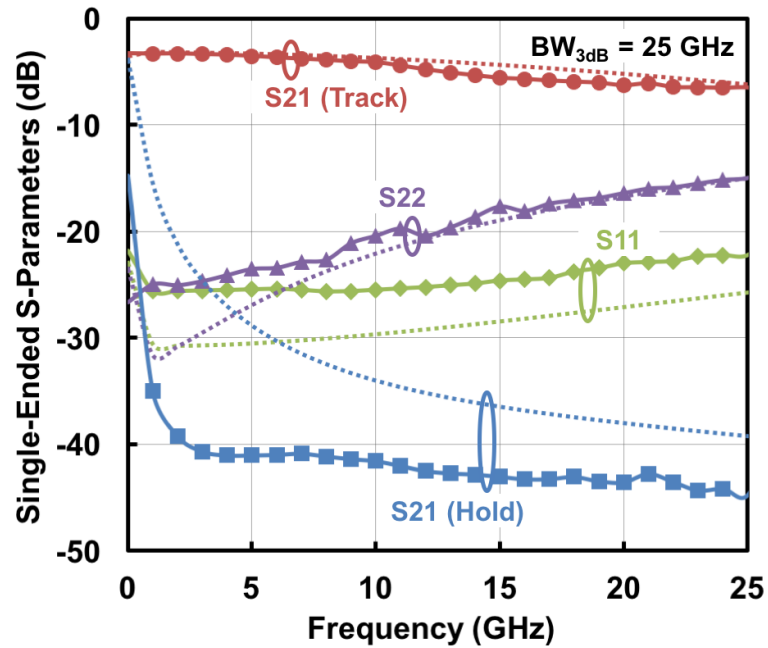
Figure 6.9: Measured (solid) and simulated (dotted) single-ended S-parameters of the 50 GS/s THA.
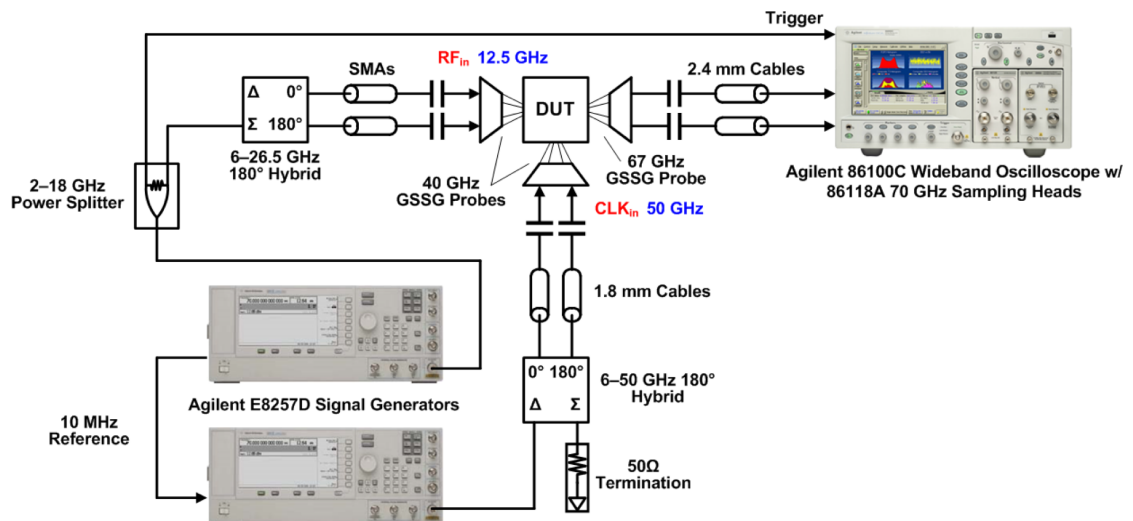
Figure 6.10: Measurement setup for capturing the transient waveforms.

Number Averages = 16

50 mV/div, 20 ps/div
25 mV/div (Single-Ended waveforms)

	current	mean	std dev	minimum	maximum	
V p-p(f3)	180.65 mV	175.68 mV	13.562 mV	116.65 mV	209.09 mV	Setup & Info
Frequency(f3)	12.51 GHz	12.51 GHz	0.0 Hz	12.51 GHz	12.51 GHz	

(a)

Number Averages = 16

50 mV/div, 20 ps/div

	current	mean	std dev	minimum	maximum	
V p-p(f3)	180.65 mV	175.68 mV	13.562 mV	116.65 mV	209.09 mV	Setup & Info
Frequency(f3)	12.51 GHz	12.51 GHz	0.0 Hz	12.51 GHz	12.51 GHz	

(b)

Figure 6.11: Measured (a) single-ended and differential outputs and (b) differential output superimposed on unassembled output of a 12.5 GHz sinusoid sampled at 50 GS/s.
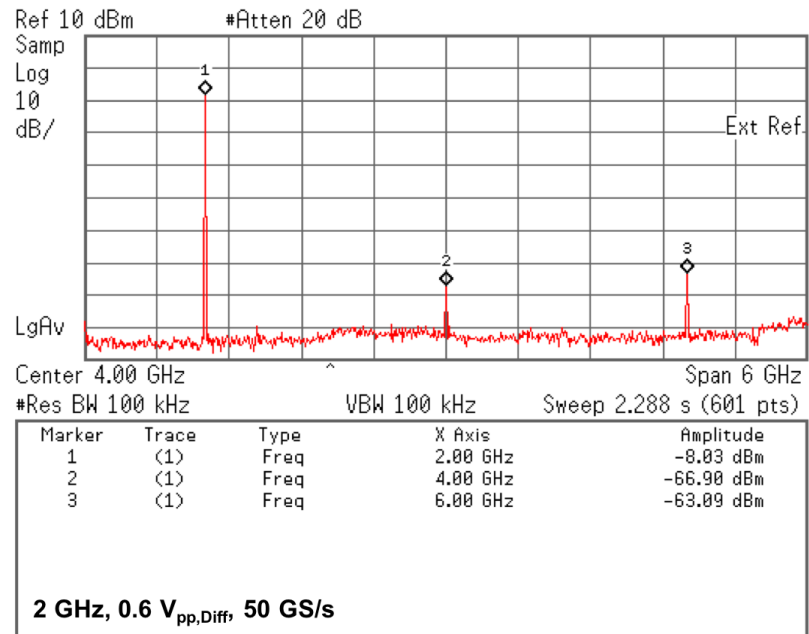
Figure 6.12: Spectrum of a 0.6 V_{pp} differential, 2 GHz sinusoid sampled at 50 GS/s.
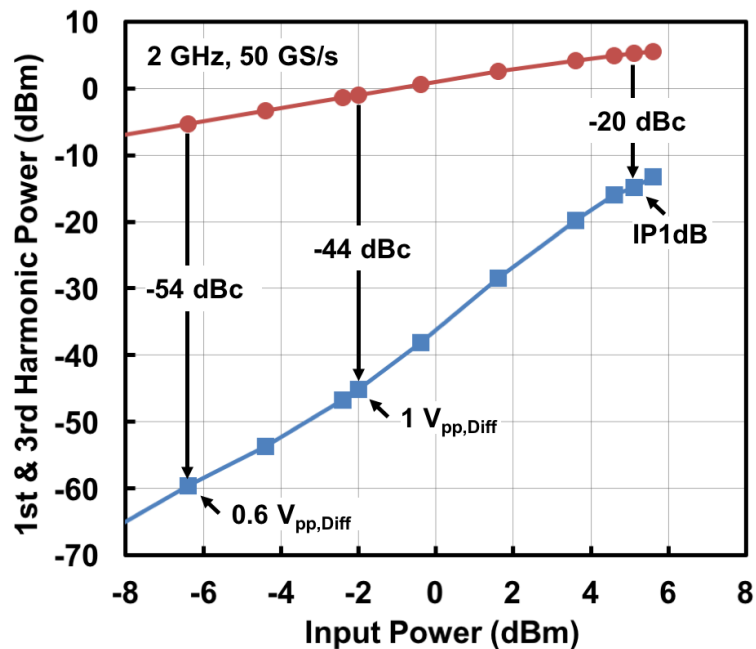
Figure 6.13: Measured HD3 as a function of input power of a 2 GHz sinusoid sampled at 50 GS/s.
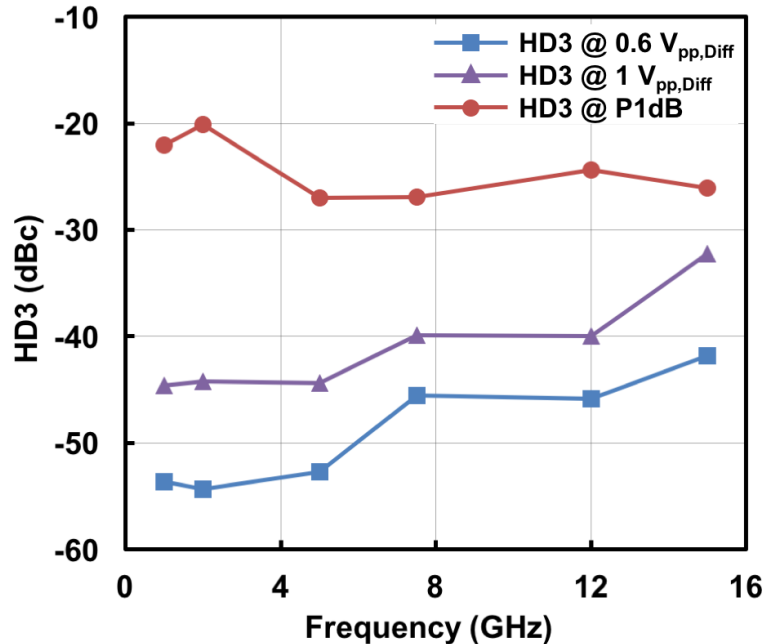
Figure 6.14: Measured HD3 as a function of frequency for 0.6 V_{pp}, 1 V_{pp} and P1dB input levels.

for input signal up to 25 GHz. The output spectrum is observed using an Agilent E4448A 50 GHz spectrum analyzer. Fig. 6.12 shows the spectral contents of a 0.6 V_{pp} differential 2 GHz signal sampled at 50 GS/s. The fundamental and third harmonic powers are plotted for different input power in Fig. 6.13. The measured third harmonic distortion (HD3) are -54 dBc, -44 dBc, and -20 dBc at 0.6 V_{pp} differential, 1 V_{pp} differential, and 1-dB compression point (P1dB) input levels, respectively. HD3 is also characterized across frequency at 50 GS/s clock rate for 0.6 V_{pp} differential, 1 V_{pp} differential and IP1dB inputs from 1$-$15 GHz as shown in Fig. 6.14. The HD3 is better than -40 dBc for a 1 V_{pp} differential input range.

A two-tone test is performed by first combining and then separating the input signals with 100 MHz offset from two signal generators with back-to-back 180° hybrids. The fundamental signal powers and their corresponding third-order intermodulation (IM3) products are observed single-ended using the Agilent E4448A 50 GHz spectrum analyzer. The spectrum of the two-tone test at 12 GHz is shown in Fig. 6.15. Fig. 6.16 shows the fundamental and output IM3 powers as a function
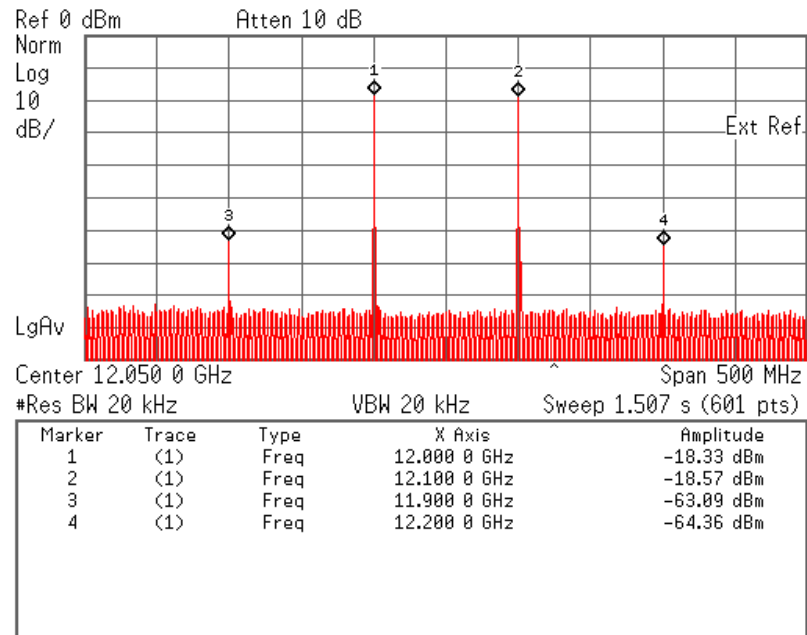
Figure 6.15: Spectrum of a two-tone test at 12 GHz and 50 GS/s.
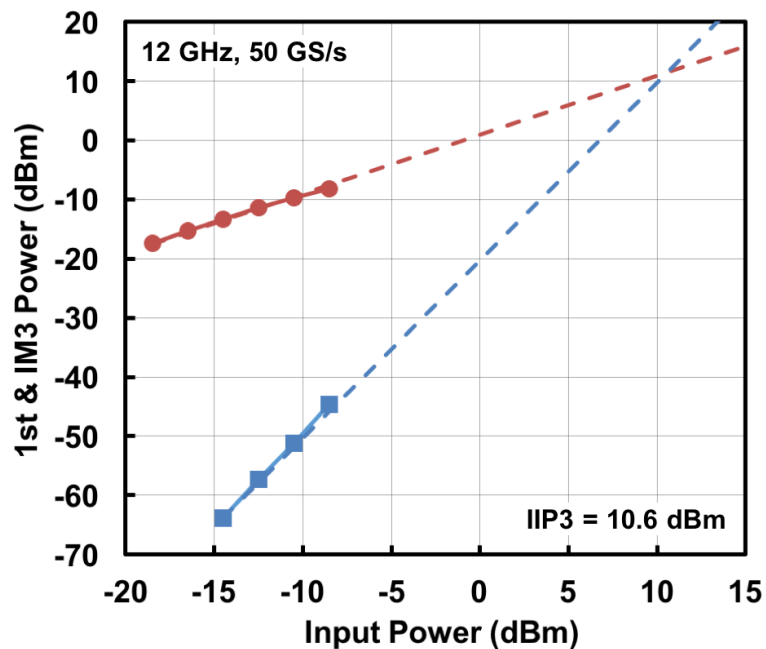
Figure 6.16: Measured fundamental and IM3 power as a function of input power.
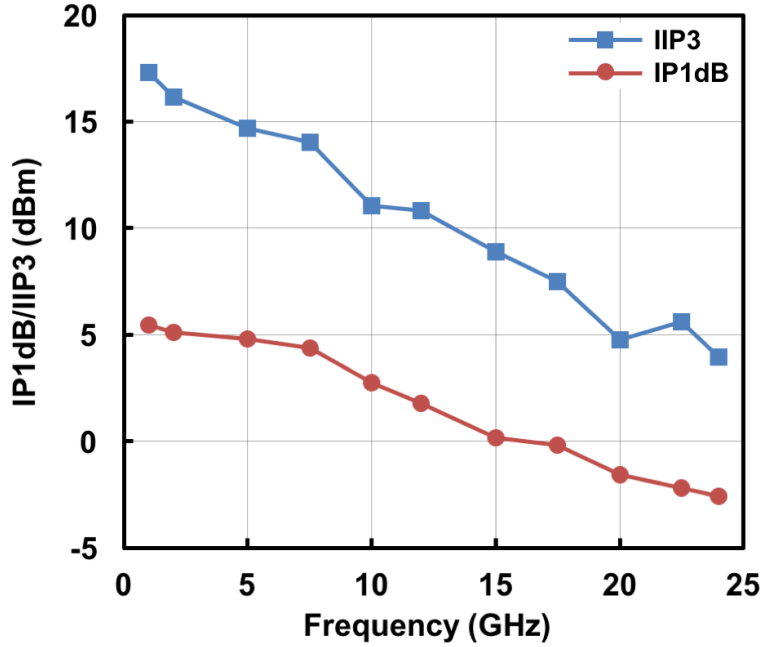
Figure 6.17: Measured IP1dB and IIP3 as a function of frequency.

of input power at 12 GHz. The input-referred 1-dB compression point (IP1dB) and third order input intercept point (IIP3) as a function of input frequency at 50 GS/s are plotted in Fig. 6.17. The THA shows a maximum IP1dB and IIP3 of 5 dBm and 17.5 dBm with the IIP3 remains above 4 dBm at the Nyquist frequency.

The 50 GS/s sampling is confirmed by beat frequency test. The single-ended spectrum for the 50.001 and 51 GHz input are shown in Fig. 6.18. The difference between the fundamental and the second and third harmonics are 26 dB and 41 dB, respectively for the 50.001 GHz input and 25 dB and 46 dB for the 51 GHz input. It is expected that the second harmonic will be lower when the circuit is operated and measured differentially.

Table 1 compares this work with the current state-of-the-art THAs in SiGe BiCMOS and InP technologies. This work demonstrates the highest sampling frequency among the SiGe BiCMOS THAs. It also consumes approximately 2.5 times less power than the InP THAs of similar performance, suggesting that a higher sampling rate can possibly be achieved in this process with additional power consumption.
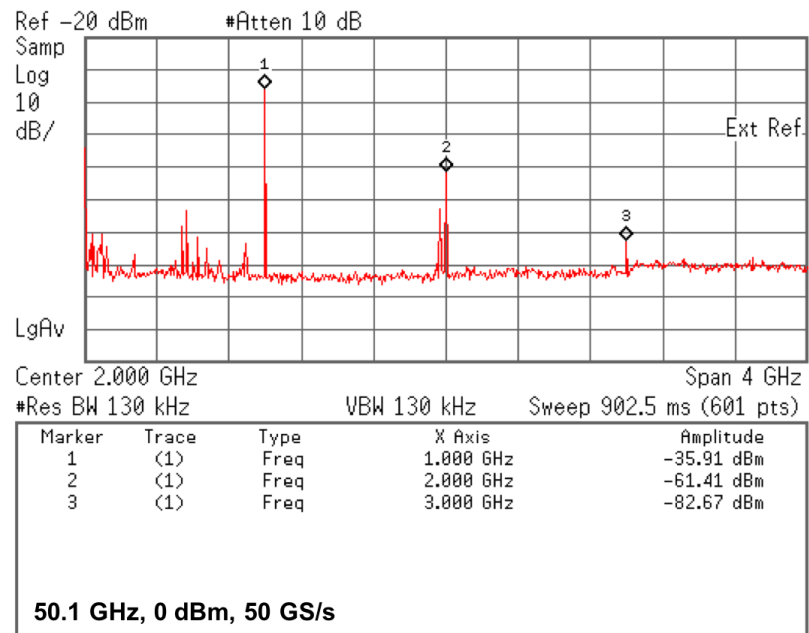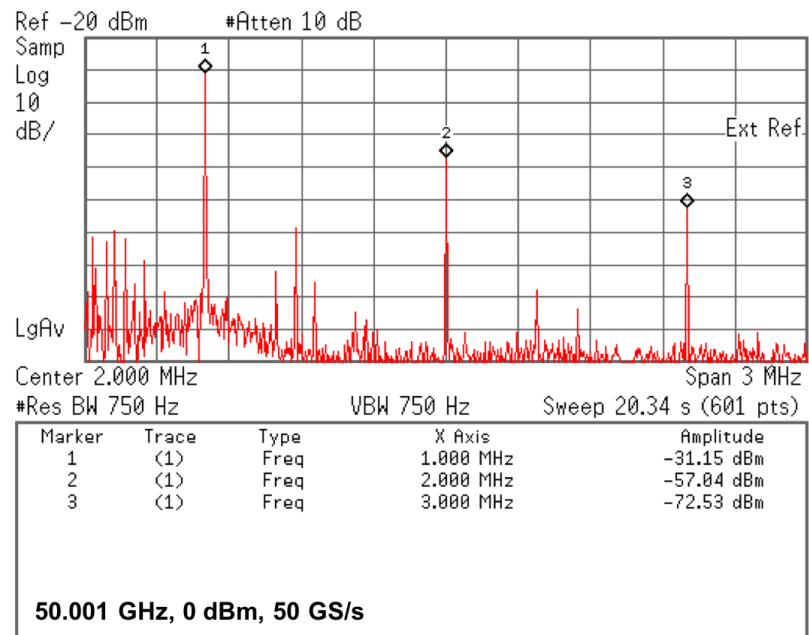
Figure 6.18: Beat frequency tests with 50.001 GHz and 50.1 GHz input frequencies.

6.4 Conclusion

A 50 GS/s track-and-hold amplifier was designed and fabricated in a 90-nm SiGe BiCMOS process. The THA demonstrated the highest sampling speed among the current state-of-the-art SiGe THAs and consumed approximately 2.5 times less power than reported InP THA of similar performance. This work illustrated the competitiveness of SiGe BiCMOS processes with III-V InP processes for high-speed mm-Wave designs.

Acknowledgements

Table 6.1: Performance Comparison of Track-and-Hold Amplifiers

	f_s (GS/s)	BW (GHz)	Input Range (V_{pp})	HD3@f_{RF}/f_s (dBc@GHz/GHz)	IIP3@f_{RF}/f_s (dBm@GHz/GHz)	Power (mW)	Supply (V)	Die Size (mm^2)	Process
[62]	40	43	-8 dBm	-29@10/40 -27@19/40	8@6/40 0@19/40	540	3.6	1.0 × 1.1	SiGe HBT f_t = 160 GHz
[63]	40	16	1	-32.4@10/40 -44.2@3/18 -50.5@2/12	15.6@10/40	560	5.5	1.8 × 1.0	SiGe HBT f_t = 160 GHz
[64]	50*	42	0 dBm	—	21@30/50	640	4, 3.3	1.3 × 1.2	SiGe BiCMOS
[65]	30	—	0.6	-59@1/30 -50.5@31/30	19@1/30	420	5.5	1.1 × 0.7	InP BiCMOS f_t = 300 GHz
[66]	50	27	9 dBm	-29.5@15/50	20.7@6/50 17.4@18/50 16.7@22/50	1200	-5, -2.5	0.7 × 1.1	InP DHBT f_t = 300 GHz
[67]	50	50	1	-56.3@3/50 -36.5@25/50	—	1850	-6.2	1.5 × 1.2	InP DHBT f_t = 320 GHz
This Work	50	25	1	-45@1/50 -32@15/50	17.3@1/50 5.6@22.5/50	540	5	0.9 × 1.1	SiGe HBT f_t = 280 GHz

* No transient waveform

Chapter 7

Conclusions

This dissertation presented the analyses, designs and implementations of mm-Wave electronically reconfigurable circuit blocks that operate bidirectionally and at multiple frequencies. The general overview of the mm-Wave frequency band, the high frequency characteristics of active devices, and the needs for mm-Wave reconfigurable circuit blocks in silicon technology were discussed in Chapter 1.

Three mm-Wave reconfigurable circuit blocks realized using the constructive wave amplification technique (CCWA) in both SiGe BiCMOS and CMOS SOI processes were shown in the first part of the dissertation. In Chapter 2, a 60 GHz constructive wave power amplifier was realized in a 0.12-μm SiGe BiCMOS process. The BiFET active feedback network was optimized for high power handling and the amplifier achieved a peak gain of 10.7 dB and a peak P_{sat} and PAE of 16.4 dBm and 15.3%, respectively. Chapter 3 presented a dual Q- and W-band, bidirectional amplifier in 45-nm CMOS SOI process where operations at different bands and directions were realized by electronically reconfiguring the feedback "field of FETs". The amplifier achieved a peak gain of more than 4.2 dB in all modes of operation. The gain can also be electronically controlled with the maximum gain and isolation variation of 20 dB. The bidirectional concept was extended to the implementation of the V-band reconfigurable active circulator in a 45-nm CMOS SOI process in Chapter 4. The active circulator was reconfigurable to operate in four different modes of operation: counter-clockwise, quasi-circulation, and as a thru between port 1 and port 2. The circuit showed an insertion loss of 7.4 dB with 18 dB

isolation in the reverse direction between adjacent pairs of ports.

Chapter 5 discussed a 70 GHz, LO phase shifting switchless bidirectional front-end using linear coupled oscillators in a 90-nm SiGe BiCMOS process. The isolation between the PA and LNA was achieved by the passive impedance transformation network with a passive mixer for the bidirectional frequency conversion. The proposed architecture enabled a TDD operation without the need for T/R switch. The circuit achieved the conversion gain of 14.5 dB and 9.9 dB in transmit and receive mode, respectively, and a minimum noise figure of 8.6 dB. The front-end was integrated with a two-element linear coupled oscillators and the maximum phase progression in the LO signal of $\pm80°$. is demonstrated by the detuning of the edge oscillator. This architecture allows for the array to be easily scaled linearly either on-chip or possibly from chip-to-chip.

Finally, a 50 GS/s track-and-hold amplifier (THA) was presented in Chapter 6 with a small-signal bandwidth of 25 GHz and measured HD3 of better than -40 dB up to 15 GHz input. The THA demonstrated the highest sampling speed among the current state-of-the-art SiGe THA and consumed approximately 2.5 times less power than the InP THAs of similar performance.

The work presented in this dissertation demonstrated the practicality of using silicon-based technology for high-speed, mm-Wave applications. The circuit technique showed can easily be applied to design in other mm-Wave frequency bands and beyond.

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