

# Lawrence Berkeley National Laboratory

## Recent Work

### Title

Development of a Customized SSC Pixel Detector Readout for Vertex Tracking

### Permalink

<https://escholarship.org/uc/item/9jg191gd>

### Authors

Barkan, O.

Atlas, E.L.

Marking, W.L.

et al.

### Publication Date

1990-10-01



# Lawrence Berkeley Laboratory

UNIVERSITY OF CALIFORNIA

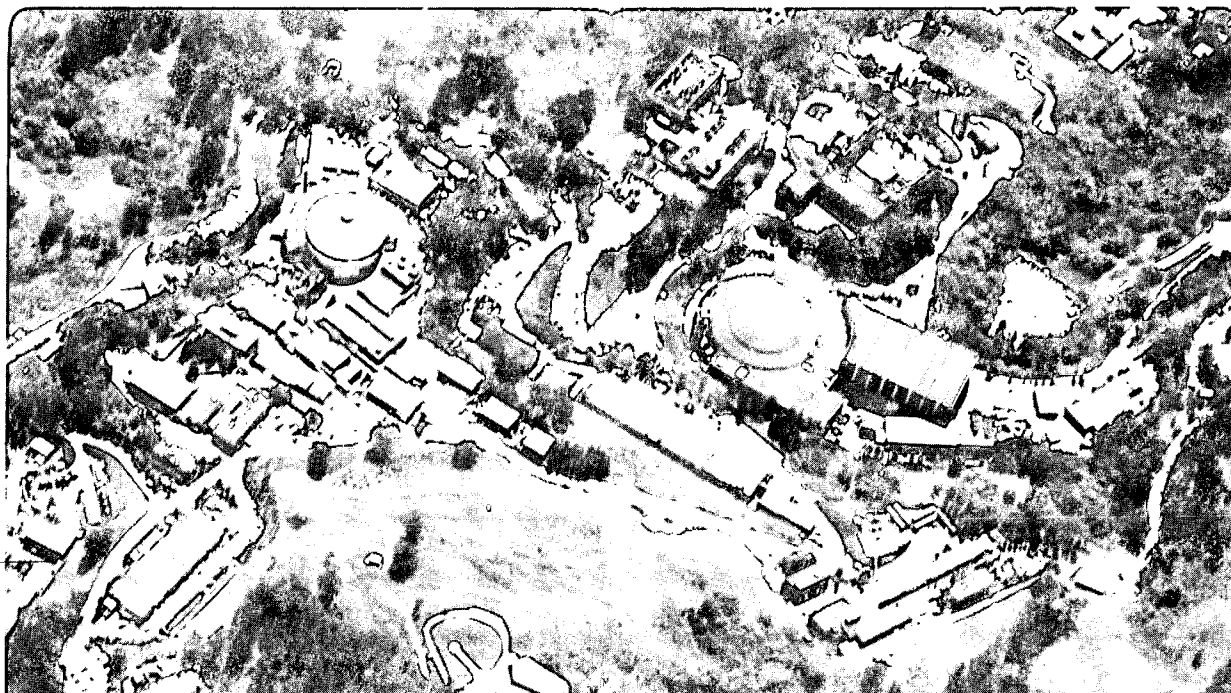
## Physics Division

Presented at the Symposium on Detector Research and Development for the Superconducting Super Collider, Fort Worth, TX, October 15-18, 1990, and to be published in the Proceedings

### Development of a Customized SSC Pixel Detector Readout for Vertex Tracking

O. Barkan, E.L. Atlas, W.L. Marking, S. Worley, G.Y. Yacoub, G. Kramer, J.F. Arens, J.G. Jernigan, S.L. Shapiro, D. Nygren, H. Spieler, and M. Wright

October 1990



Prepared for the U.S. Department of Energy under Contract Number DE-AC03-76SF00098.

1 LOAN COPY 1  
1 Circulates 1  
1 for 2 weeks 1

Bldg. 50 Library  
Copy 2

LBL-29792

## **DISCLAIMER**

This document was prepared as an account of work sponsored by the United States Government. While this document is believed to contain correct information, neither the United States Government nor any agency thereof, nor the Regents of the University of California, nor any of their employees, makes any warranty, express or implied, or assumes any legal responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by its trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof, or the Regents of the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof or the Regents of the University of California.

**DEVELOPMENT OF A CUSTOMIZED SSC PIXEL DETECTOR READOUT  
FOR VERTEX TRACKING<sup>1</sup>**

Ozdal Barkan, Eugene L. Atlas, Wayne L. Marking, Stuart Worley, Ghassan Y. Yacoub  
Hughes Aircraft Company, Carlsbad, CA 92009

Gordon Kramer  
Hughes Aircraft Company, El Segundo, CA 90245

John F. Arens, J. Garrett Jernigan  
Space Sciences Laboratory, University of California,  
Berkeley, CA 94720

Stephen L. Shapiro  
Stanford Linear Accelerator Center,  
Stanford University, Stanford, CA 94309

David Nygren, Helmuth Spieler, Michael Wright  
Lawrence Berkeley Laboratory  
University of California  
Berkeley, CA 94720

October 1990

---

<sup>1</sup>This work was supported in part by the Director, Office of Energy Research, Office of High Energy and Nuclear Physics, Division of High Energy Physics, of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

## DEVELOPMENT OF A CUSTOMIZED SSC PIXEL DETECTOR READOUT FOR VERTEX TRACKING\*

Ozdal Barkan, Eugene L. Atlas, Wayne L. Marking, Stuart Worley, Ghassan Y. Yacoub  
Hughes Aircraft Company, Carlsbad, CA 92009

Gordon Kramer  
Hughes Aircraft Company, El Segundo, CA 90245

John F. Arens, J. Garrett Jernigan  
Space Sciences Laboratory, University of California,  
Berkeley, CA 94720

Stephen L. Shapiro  
Stanford Linear Accelerator Center,  
Stanford University, Stanford, CA 94309

David Nygren, Helmuth Spieler, Michael Wright  
Lawrence Berkeley Laboratory, Berkeley, CA 94720

### Abstract

We describe the readout architecture and progress to date in the development of hybrid PIN diode arrays for use as vertex detectors in the SSC environment. The architecture supports a self-timed mechanism for time stamping hit pixels, storing their xy coordinates and later selectively reading out only those pixels containing interesting data along with their coordinates. The peripheral logic resolves ambiguous pixel ghost locations and controls pixel neighbor readout to achieve high spatial resolution.

A test lot containing 64 X 32 pixel arrays has been processed and is currently being tested. Each pixel contains 23 transistors and six capacitors consuming an area of 50  $\mu\text{m}$  by 150  $\mu\text{m}$  and dissipating about 20  $\mu\text{W}$  of power.

### Introduction

Pixel arrays (2-dimensional array of small semiconductor detector elements) provide significant technical advantages for use as vertex detectors [1,2]. These include good track resolution, small capacitance, high signal-to-noise ratio, increased radiation resistance [3,4]. High interaction rates and the increased quantity of data ( $10^8$  data channels for a typical vertex detector [3]) necessitate sparse readout circuitry within the detector chips. We have developed a pixel array chip architecture that supports a self-activated mechanism for time stamping hit pixels, storing their xy coordinates and later selectively reading out only those pixels containing interesting data along with their coordinates. Test chips that contain a 64 x 32 array of pixels (50  $\mu\text{m}$  x 150  $\mu\text{m}$  each) have been processed.

### Requirements/Assumptions Concerning SSC Detectors

Our chip architecture was developed with the goal of being able to handle the worst case assumptions about SSC interaction rates and background radiation. Pixels and the periphery architecture can be simplified if less demanding assumptions are made.

It is assumed that every 16 ns there is a beam crossing. On the average there are 1.5 events/beam crossing and only 1 percent of them will be interesting. A 1  $\text{cm}^2$  chip at a radius of 3 cm from the beam axis will be hit during 30

different beam crossings while waiting for the Trigger level 1 signal. (A Trigger level 1 signal is externally generated, signals the occurrence of an interesting event and has a delay of 1-2  $\mu\text{s}$  from the beam crossing. This delay will be fixed once the calorimeter design is completed.) For each beam crossing when the array is hit, up to 25 pixels will be hit or will be a neighbor of such a hit pixel. (It is desirable to read neighbors of hit pixels to determine the centroid of a particle track). It is also assumed that these 25 pixel locations will not be hit again until the data is read or discarded.

Requirements/specification for the chip include [5,6] quiescent power dissipation of 0.1 - 1.0  $\text{W}/\text{cm}^2$ , dynamic range of 500 (determined by 100,000 holes maximum input charge and 200 electron rms noise), time stamping with 16 ns time resolution, readout of the charge stored and xy addresses in about 1  $\mu\text{s}$ , radiation hardness to 10 MRad, and testability.

### Prototype Architecture and Block Diagrams

A first prototype array for the final SSC vertex detector has been designed and will be going into fabrication in December 1990. Figure 1 shows the periphery architecture and Figure 2 shows the pixel architecture. A number of prototyping steps are envisioned to reach the final radiation hard version of the SSC array.

\*Work supported by the U.S. Department of Energy, contract number DE-AC03-76SF00098(LBL) and DE-AC03-76SF00515(SLAC)

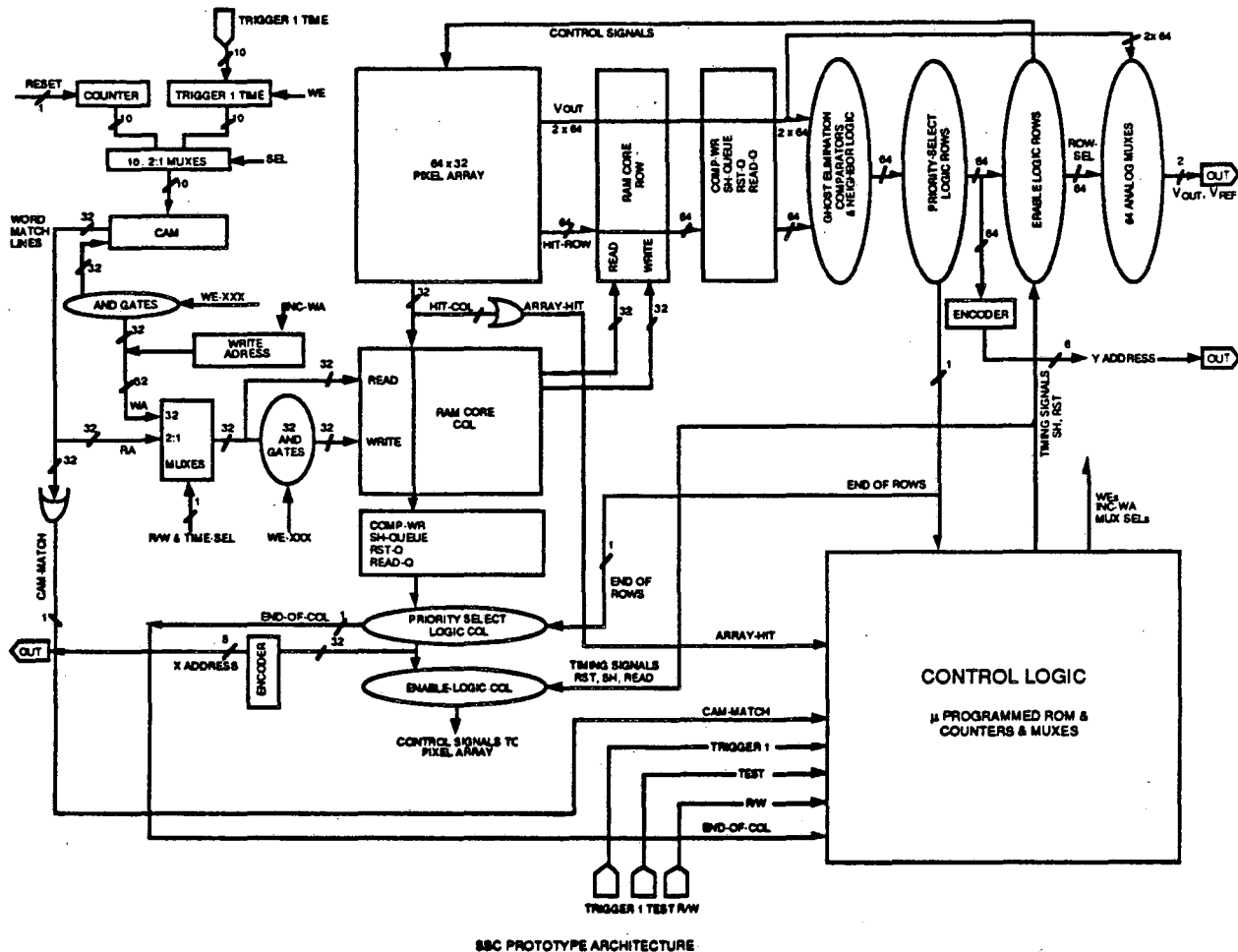


Figure 1. Pixel Detector SSC Prototype Architecture.

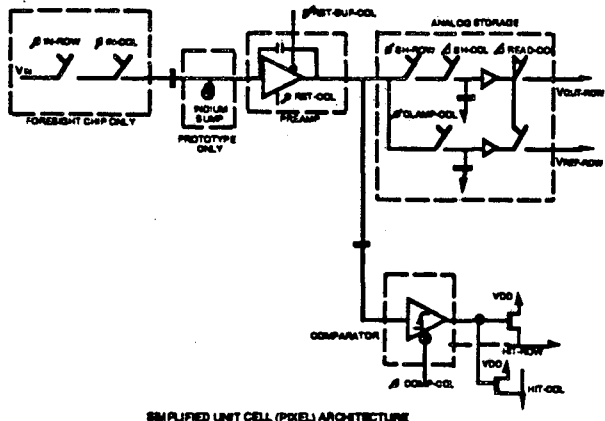


Figure 2. Simplified Unit Cell (Pixel) Architecture.

A brief overview of chip operation is as follows:  
 If the array is hit, the time of the hit is stored in the content addressable memory (CAM), along with the hit pixel locations that are stored in the random access memory

(RAM). The array keeps storing new hit information until the arrival of a Trigger level 1 signal. At that time the chip searches the CAM for a hit at the time of interest indicated by the Trigger level 1 signal. If a hit exists, it reads those hit locations one at a time and sends the stored charge information and address to be processed. Hit data that does not correspond to the time of interest is not read out and pixels are reset to receive future hits.

This architecture resolves ambiguous hit locations (due to multiple pixels hit at one time) and does not require continuous clocking of pixels or periphery logic, eliminating switching noise and power dissipation. All control signals are generated internal to the chip using  $\mu$ -programmed control logic. The CAM and the RAM do not require encoding and decoding. Dynamic storage with no refresh circuitry could also be used since, typically, we are no longer interested in data after a few microseconds. These characteristics result in a smaller periphery and an improved fill factor (> 90%). The chip has a test mode of operation for production testing, as well as an inside-SSC test mode to disconnect bad pixels from the logic.

The unit cell has within it a transimpedance amplifier, charge storage and analog buffering, and a fast comparator to signal hits to the row and column circuitry.

The pixel has both digital and analog parts in close proximity due to the density required. Great care has been taken to minimize the coupling of the digital signals to the sensitive analog portion of the circuit. Separate analog and digital supply rails are provided in the unit cell to isolate the analog circuitry from any spikes resulting from digital switching. DC bias lines are used at the cell edges to prevent cell-to-cell crosstalk.

Several capacitor types are used; PS1 to Metal 1 and Metal 1 to Metal 2 for low value capacitors (2.5 - 10 fF) and PS1-Pwell for higher values (50 - 300 fF).

In the near future we expect advances in both scaling and silicon-on-insulator (SOI) multilevel technologies to allow the unit cell size to shrink to 50  $\mu\text{m}$  X 50  $\mu\text{m}$  or smaller with current circuit complexity. We also expect the advances to result in a faster, better performing unit cell.

#### Preprototyping Arrays

Before committing to full prototype production we have decided to process test chips to verify the pixel functionality and the speed of time stamping and analog readout. We have used an  $L_{\text{eff}} = 1.2 \mu\text{m}$  single poly, double metal (pitch  $\sim 3.5 \mu\text{m}$ ) CMOS process which guarantees 100 MHz operation at room temperature for worst case process conditions. We are also going to layout and process a single pixel at Hughes Aircraft using a Hughes radiation hard SOS technology to evaluate the radiation hardness of the design. None of these test chips contains detectors. Instead, electrical voltage inputs to pixels are used for test and verification of operation. The prototype will contain PIN detectors to be built by LBL.

#### Test Data

The test arrays have arrived and are under test.

#### FY91 Plans

We plan to process our current prototype design in early 1991. A 6 design with AC coupled detectors (to eliminate dark current buildup due to radiation damage induced leakage) will be processed during the second half of FY91. A rad hard SOS version of this second design will also be processed after verification of the non-rad hard version.

#### References:

- [1] S. Shapiro, W. Dunwoodie, J. Arens, and S. Gaalema, "Silicon PIN Diode Array Hybrids for Charged Particle Detection," Nucl. Instrum. Methods A275: 580 (1989).
- [2] J. G. Jernigan, J.F. Arens, G. Kramer, T. Collins, J. Herring, S.L. Shapiro, and C. Wilburn, "Performance Measurements of Hybrid PIN Diode Arrays," Presented to the 1990 Int. Industrial Symposium on the Supercollider, Miami Beach, FL (1990) SLAC-PUB 5211.
- [3] H. Spieler, "Integrated Microsystems as a Driving Force in Modern Detector Designs," Proceedings of the International Conference on the Impact of Digital Microelectronics and Microprocessors on Particle Physics, Trieste, Italy, March 28-30, 1988.
- [4] D. R. Nygren, "Silicon Tracking Devices for the SSC," Proceedings of the Summer Study on High Energy Physics in the 1990s, pp 754-761, Snowmass, Colorado, June 27 - July 15, 1988.
- [5] G. Kramer, et al, Memorandum of Understanding SSCPC-025 "Proposed Plan for Pixel Array Development for the SSC," (1989) as modified by O. Barkan, Preliminary Design Review HTC, Carlsbad, CA, May 2, 1990.
- [6] G. Kramer, et al, "The Pixel Detector Development Collaboration," Summary Report for FY'90 and Proposed Effort for FY'91, Presented to the SSC Laboratory, September 1, 1990.

LAWRENCE BERKELEY LABORATORY  
UNIVERSITY OF CALIFORNIA  
INFORMATION RESOURCES DEPARTMENT  
BERKELEY, CALIFORNIA 94720