Title
Developing Through-Wafer Via (TWV) and Plasma Dicing Process for Silicon Interconnect Fabric (Si-IF)

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Developing Through-Wafer Via (TWV) and Plasma Dicing Process for Silicon Interconnect Fabric (Si-IF)

A thesis submitted in partial satisfaction

of the requirements for the degree Master of Science

in Electrical Engineering

by

Yandong Luo

2018

ABSTRACT OF THE THESIS

Developing Through-Wafer Via (TWV) and Plasma Dicing Process for Silicon Interconnect Fabric (Si-IF)

by

Yandong Luo

Master of Science in Electrical Engineering
University of California, Los Angeles, 2018
Professor Subramanian Srikantes Iyer, Chair

In this thesis, the through-wafer via (TWV) technology is developed for signal and power delivery on silicon interconnect fabric (Si-IF). The electrical performance of through-wafer via is simulated by ANSYS HFSS with different design parameters. Low insertion loss is obtained when it is operating at the low-frequency range (<1GHz). The electrical reliability issues such as electromigration are examined and verified. The thermal reliability issues related to TWV during Si-IF fabrication are analyzed by simulation. It is observed that interfacial delamination can be induced at the interface between Cu via and SiO_2 liner due to the CTE mismatch between the materials. The TWV is fabricated in UCLA Nanolab on a 300μm thick wafer. Plasma dicing technology is also developed based on deep silicon etch to obtain smooth die edge after dicing, which enables compact die assembly on Si-IF.

The thesis of Yandong Luo is approved.

Chandra J Joshi

Mark S Goorsky

Subramanian Srikantes Iyer, Committee Chair

University of California, Los Angeles

2018

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Acknowledgments

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At last, I would like to thank my parents for their constant support and help.

CHAPTER 1

Introduction

1.1 The Demand for New Packaging Technology

Nowadays, device scaling is slowing down due to the high cost of development and manufacturing **[1]**. New approaches to continue system scaling and improve computing performance have become the focus of research.

New packaging technology is a potential candidate for system scaling and performance improvement. First, packaging scaling lags far behind that of device level scaling. In fact, packaging size has only been scaled by 5 times over the past 50 years while the transistor size has been scaled down by over 1000 times **[2]**. Besides, present packaging technology is limiting the system performance.

In a packaging system, interconnect between packaged dies, laminate and PCB is typically achieved by solder-based interconnect, such as micro bumps, C4 bumps (about 100μm pitch) and BGA (about 400μm pitch) [3]. It is challenging to scale down the pitch of the bumps due to solder protrusions and substrate warpage. Large interconnect pitch limits the number of I/O ports and thus the chip bandwidth. To meet the increasing demand for high chip bandwidth, serial links with high operating frequency are applied for inter-chip communication. It leads to high power consumption and complexity in the design of serialization and deserialization (SerDes) circuit **[4]**. To accommodate more I/O ports, the chip-level packaging is enlarged.

However, the die space is increased with larger packaging size, which leads to a longer data link and higher communication latency.

System on chip (SoC) technology can shorten the length of the data links by fabricating all functional modules into a single die. However, increasing complexity in design flow and low yield are two issues for large-scale SoC systems. Besides, heterogeneous integration is not applicable in SoC systems.

3D integration technology has been proposed to improve the system performance **[5], [6]**. However, the relatively high cost and the thermal management issues can limit its application.

1.2 Si Interconnect Fabric (Si-IF) Technology

As discussed above, the two significant drawbacks of present packaging technology are the limited number of I/O ports and long data link. To solve these problems, a novel system level packaging scheme—silicon interconnect fabric (Si-IF) technology is proposed **[2],[3], [7],[8]**. Figure 1.1 shows the interconnect scheme on Si-IF and PCB. The basic idea of Si-IF is to build fine-pitch interconnect levels (<10μm pitch) on a silicon board for inter-die communication. The silicon dies are diced by plasma dicing and then bare dies are bonded onto Si-IF by thermal compression bonding (TCB) **[7]**. The key technological features of Si-IF are listed as below.

- Fine-pitch interconnect built on silicon board (<10μm pitch).
- The elimination of die-level packaging and compact die assembly.
- Thermal compression bonding to enable heterogeneous integration scheme.

- Through-wafer vias (TWVs) on full thickness Si wafer for signal and power delivery.

These features of Si-IF eliminate the drawbacks of current packaging system and improve the overall system performance. By using fine pitch interconnect, more I/O ports can be placed at the die edge and parallel data transfer is enabled for inter-die communication, which improves the chip bandwidth with less power consumption. By removing die-level packaging, die space is reduced by compact die assembly on the Si-IF, resulting in shorter data link length (50-500μm) compared with that on PCB (typically a few centimeters). The shortened data link leads to lower data latency and the elimination of transceivers and transmitters in data links. As a result, faster inter-die communication with less power consumption can be achieved on Si-IF. According to S. Jangam *et.al* **[8]**, the energy consumption for data transfer is significantly reduced to 0.4pJ/bit on the Si-IF, while it is 23pJ/bit on PCB with SerDes circuit. By thermal compression bonding, heterogeneous integration can be realized on Si-IF. It enables better system performance by fabricating each functional module with the manufacturing process that yields its best performance.

Better thermal-mechanical performance is also obtained on Si-IF. For packaging system with an organic substrate, the CTE mismatch between organic materials, the solder bumps, and silicon dies can cause severe reliability issues by CPI. However, on Si-IF, CPI is eliminated because both the dies and the board are made of Si. Si-IF also enables higher heat dissipation efficiency because Si has much higher thermal conductivity

(149W/K·m) than organic materials (typically <1W/K·m), which is important for systems with high integration density.

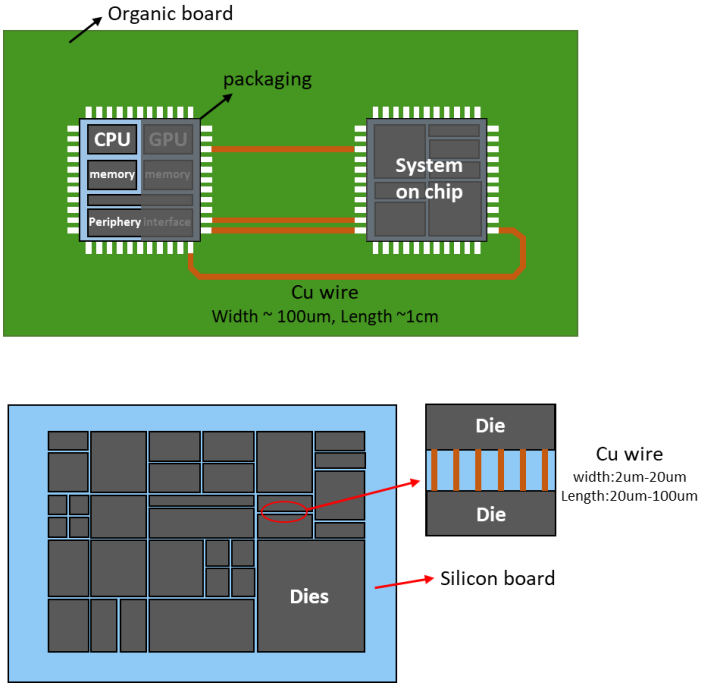


Figure 1.1 The interconnect scheme on PCB (top) and on Si-IF (bottom)

1. 3 Contribution of this Work

The primary objectives of this work are to develop two technological enablers for the Si-IF: the through-wafer vias (TWVs) and plasma dicing (PD), both of which involves high aspect ratio Si etch. The contributions of this work are as follows.

(1). Design and verify the electrical performance of TWVs

(2). Examine the thermal reliability issues related to TWVs during the Si-IF fabrication

(3). Fabricate TWVs on 300μm thick Si wafer.

(4). Develop plasma dicing process to enable compact die assembly on Si-IF.

1.4 Organization of this Thesis

The organization of the thesis is as follows. In Chapter 2, the electrical performance of TWV is simulated in ANSYS HFSS with different design parameters. Chapter 3 presents the interconnect design and electrical reliability analysis for the TWV based power links. The thermal reliability issues related to TWV during the Si-IF process is analyzed in Chapter 4. Chapter 5 demonstrates the fabrication process of TWV in UCLA Nanolab. The process flow of plasma dicing and the characterization results are presented in Chapter 6. The conclusions are drawn in Chapter 7.

CHAPTER 2

The Design and Electrical Simulation of Through-Wafer Vias (TWV)

In the silicon interconnect fabric (Si-IF) technology, the communication between dies on the two opposite sides can be achieved by building vias on Si-IF. More importantly, power modules are attached to the backside of Si-IF. Therefore, vias are needed to connect Si-IF and the power modules for power delivery. A similar concept named through silicon via (TSV) has been practiced for 3D integration technology, which provides vertical connect among the stacked Si dies **[9], [10].** In the TSV process, the Si dies are usually thinned to about 50μm thick for the ease of making high aspect ratio via. However, the Si-IF is fabricated on a thick Si wafer (300-500μm) to provide enough mechanical support for the dies bonded. Therefore, the vias built on this thick Si-IF are called through-wafer vias (TWV). Two types of TWVs, the signal vias, and power vias are designed for low-frequency signal (<1GHz) transfer and power supply, respectively, as shown in Figure 2.1. In this chapter, we mainly focus on the design and electrical simulation of the signal vias.

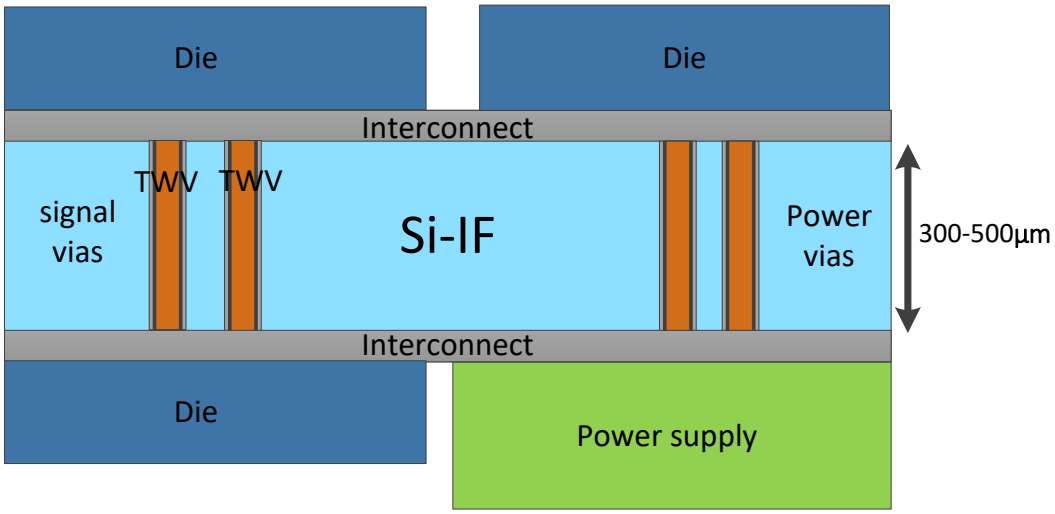


Figure 2.1 The TWVs in silicon interconnect fabric (Si-IF)

Two types of vias geometry, the cylindrical via and co-axial via are considered [11], [12]. The former is designed for both the signal via and power vias, while the latter is used only for the signal via due to its relatively high resistance. The top view of via cross-section is shown in Figure 2.2. For the cylindrical via, the diameter of the Cu core is 50µm and 100µm for the signal via and power via, respectively. The Cu core is surrounded by 2µm thick SiO_2 dielectrics for electrical insulation. A 20nm TiN diffusion barrier is deposited by ALD to prevent Cu atom diffusion into SiO_2 dielectrics. The depth of a TWV is about 300-500µm, depending on the thickness of the Si-IF. The geometry of a co-axial TWV is shown in Figure 2.2(b). The signal is conducted by the Cu core with 50µm diameter. The 5µm thick copper shell is grounded to prevent coupling noise between the core and the Si substrate. A 25µm-thick dielectric is filled between the Cu core and grounded Cu shell. SiO_2 or benzocyclobutene (BCB) can be used as the filling dielectrics **[12]**. SiO_2 dielectrics are deposited between the Cu shell

and Si substrate. The detail information about fabricating co-axial vias can be found in **[11]**.

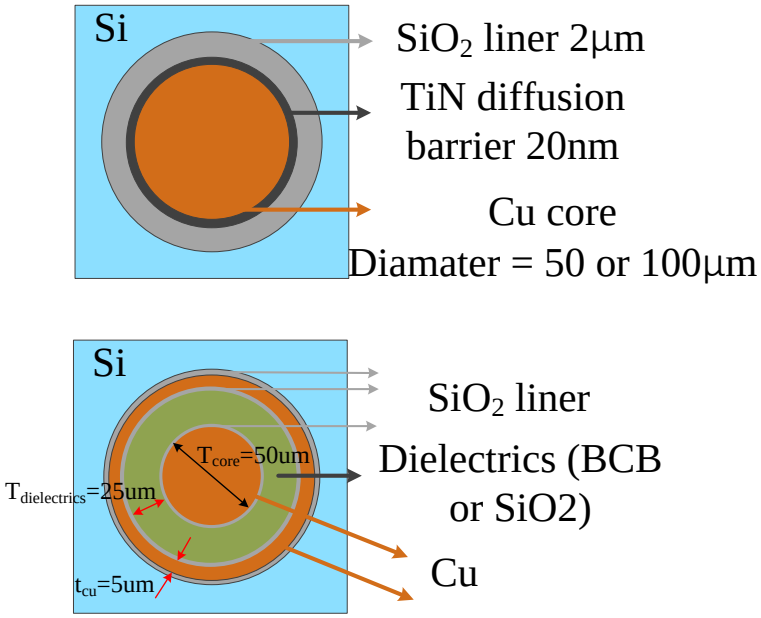


Figure 2.2 The cross-section of the cylindrical TWV (b) the cross-section of the coaxial TWV

2.1. Transmission Property of TWV

To study the transmission property of TWV, the insertion loss of signal TWV is calculated by ANSYS HFSS. For cylindrical via, a signal-ground (S-G) TWV pair is simulated **[12], [13]**. The diameter of the Cu core is 50μm and the height is 500μm. The thin TiN barrier layer is not considered for the ease of simulation. A 20μm SiO_2 layer is built at the top and bottom surfaces of the Si substrate to consider the effect of redistribution layer dielectrics. The silicon substrate is assumed to be lightly doped with a resistivity of 10Ω·cm. The lumped ports are applied at the top and bottom surface of the via. For the coaxial TWV, the diameter and height of the Cu core are the same as the cylindrical TWV. The thickness of the filling dielectrics and the Cu shell are 25μm

and 5μm, respectively. Two types of filling dielectrics, SiO_2 and BCB are considered. The insertion loss is characterized by the transmission coefficient S_{21} with a frequency sweep from 10MHz to 20GHz. All the materials parameters and geometrical parameters used in the simulation are listed in TABLE 2.1.

Table 2.1 Parameters for TWV Electrical Simulation

Parameter	Value	Parameter	Value
The dielectric constant of Silicon	11.7	The thickness of Cu shell (coaxial TWV)	5μm
The dielectric constant of SiO_2	3.9	The thickness of the filling dielectrics (coaxial TWV)	25μm
The dielectric constant of BCB	2.6	TWV height	500μm
Si Substrate resistivity	10Ω·cm	TWV pitch (for the S-G pair)	100μm
The diameter of Cu core	50 μm	The thickness of the SiO_2 liner	2μm

The simulated S_{21} is plotted in Figure 2.3. The insertion loss rises as the signal frequency is increased due to the leakage from Cu core to Si substrate through the SiO_2 dielectrics **[14]**. At high-frequency range (>5GHz), insertion loss of the co-axial TWV is 0.6dB~1.3dB smaller than the cylindrical TWV because the Cu shell effectively prevents the signal from coupling into Si substrate. The transmission property of the coaxial TWV also depends on the property of its filling dielectrics. The insertion loss is smaller when filling dielectrics with smaller dielectric constant and less loss tangent is used. Though coaxial TWV shows less insertion loss at a higher frequency, the signal TWV is designed to operate at the frequency <1GHz, where both types of TWV show insertion loss <0.25dB. Therefore, only the cylindrical TWV is studied in this thesis because of its less complicated fabrication process.

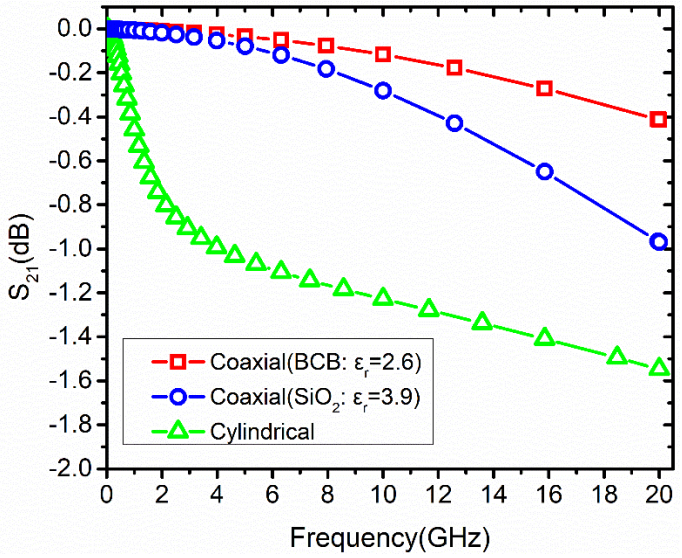


Figure 2.3 The insertion loss of cylindrical TWV and coaxial TWV

The impact of TWV design parameters on its transmission property is studied by varying one parameter while keeping the other parameters unchanged. First, the TWV pitch is changed from 75μm, 100μm to 200μm. From the results in Figure 2.4, the transmission property with different TWV pitches is similar at the low-frequency range (<1GHz), where the insertion loss is about 0.25dB at 1GHz. For high-frequency range (>5GHz), the insertion loss increases with a smaller TWV pitch. As the TWV pitch decreases, the conductance and capacitance of the Si substrate between the signal via and ground via is increased, which leads to larger insertion loss **[14]**.

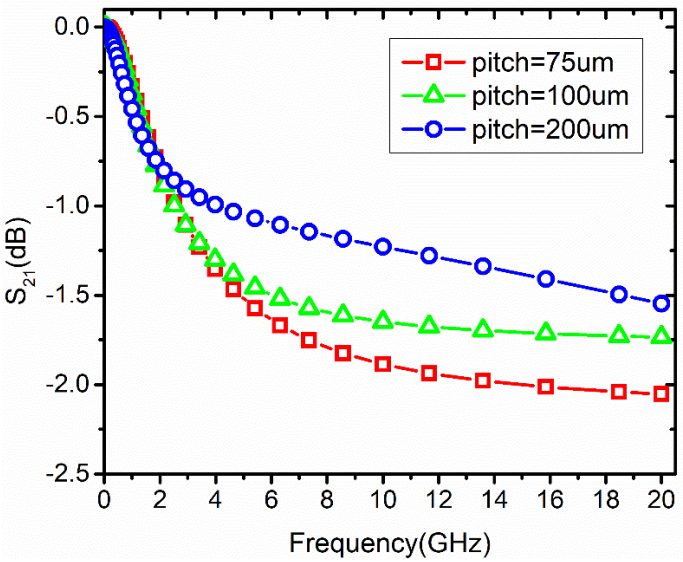


Figure 2.4 Insertion loss S21 vs. TWV pitch

The insertion loss S_{21} vs the thickness of SiO_2 liner is plotted in Figure 2.5. It is observed that the insertion loss is reduced with thicker SiO_2 dielectrics. It can be explained by the leakage loss between TWV and Si substrate through SiO_2. Since the capacitance of the SiO_2 liner is inversely proportional to its thickness, thicker oxide liner has a larger impedance ($Z = 1/j\omega C_{SiO2}$), which leads to less leakage and therefore lower insertion loss. To ensure the insertion loss is less than 1dB at 1GHz, the SiO_2 thickness should be larger than 1μm. However, thicker SiO_2 requires longer oxidation time, especially for thermal oxidation where the non-linear deposition rate makes it time-consuming to grow thick SiO_2. Therefore, the SiO_2 is chosen to be 1μm-2μm for the fabrication process.

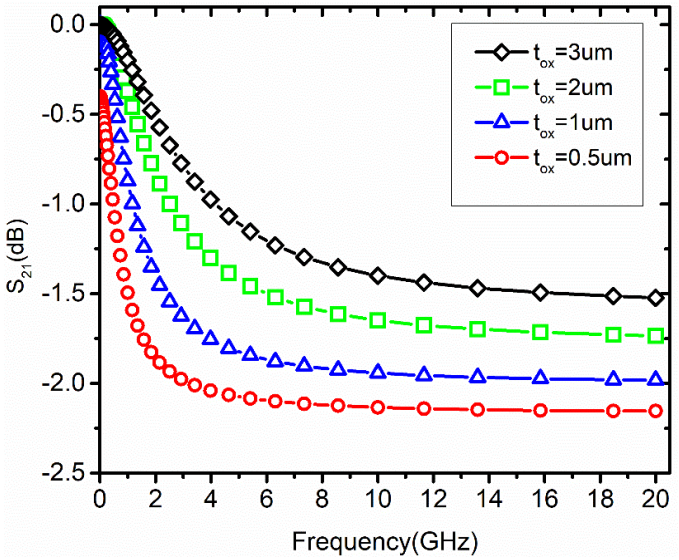


Figure 2.5 S_{21} vs. the thickness of the SiO_2 liner

Figure 2.6 shows the relation between TWV diameter and insertion loss. The via space is fixed at 50μm. It is observed that insertion loss is reduced for smaller via diameters, which can be explained by the decreased capacitance of the SiO_2 liner due to a smaller surface area. Therefore, the diameter of the signal via is chosen to be 50μm (aspect ratio = 10 for 500μm thick Si wafer) considering the difficulty in high aspect ratio via etching.

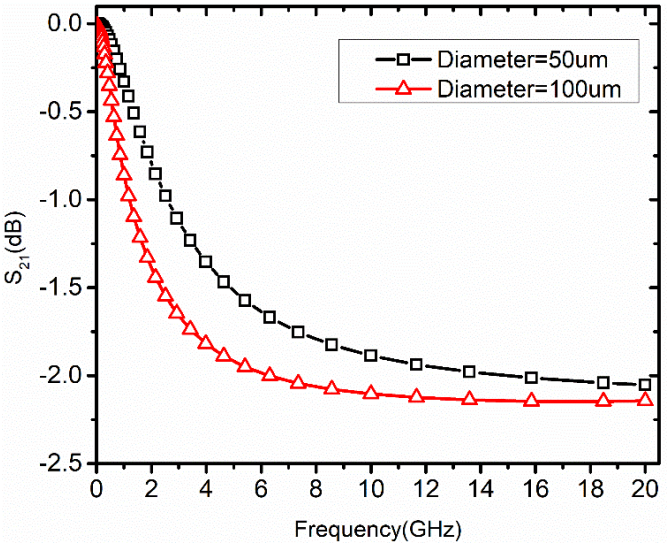


Figure 2.6 S_{21} vs. TWV diameter

2.2 Transmission Property of a Signal Path

For inter-die communication across the Si-IF, a complete data link consists of 4-layer Cu wiring levels on both sides of the Si-IF, the interconnect between Cu wiring levels and dies, and the TWV, as shown in Figure 2.7.

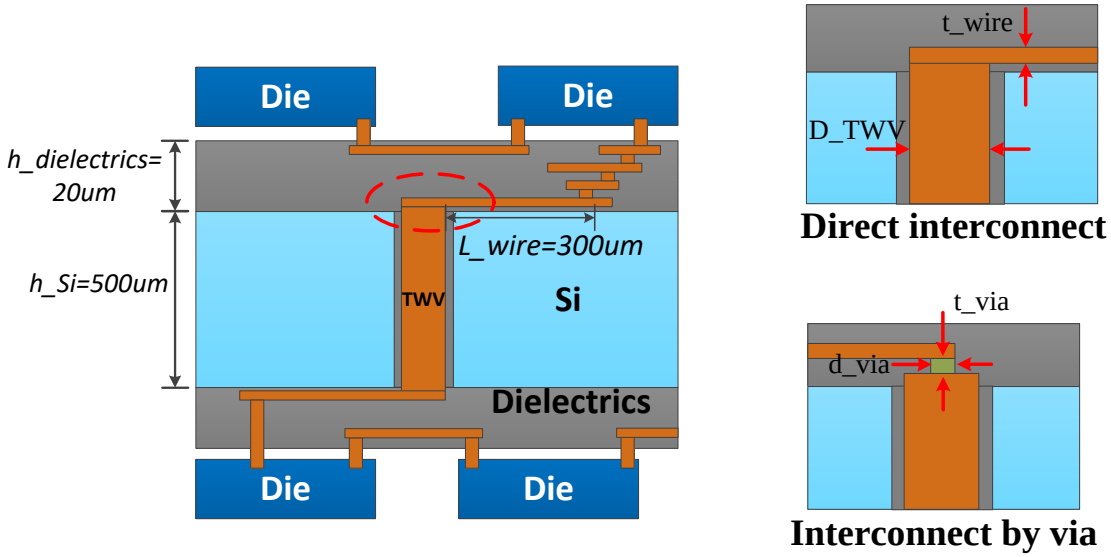


Figure 2.7 A data link with TWV (left) Two interconnect scheme between the Cu wires and TWV (right).

For the TSVs, the interconnect between via and Cu wiring levels are achieved by building micro bumps above the vias **[14]**. However, for TWVs, it is difficult to fabricate micro bumps with uniform thickness because of dishing effect in CMP. Therefore, two interconnect schemes without micro bumps are proposed: the direct connect scheme (scheme 1) and via-connect scheme (scheme 2), as shown in Figure 2.7. In scheme 1, Cu wires are fabricated directly on the TWV with a single damascene process. In scheme 2, the Cu wires are connected to TWV by a via. The dual damascene

process is used for this scheme.

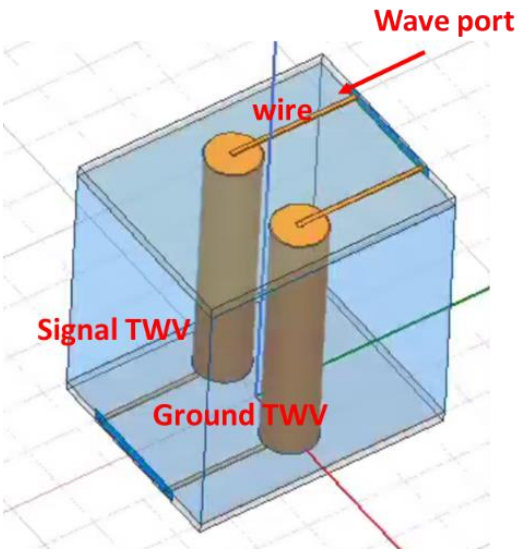


Figure 2.8 The simulation model of a data link with TWV in ANSYS HFSS

The transmission property of a data link with TWV is studied in ANSYS HFSS with a signal-ground (S-G) model, as shown in Figure 2.8. The Si-IF is modeled as a Si substrate with 20μm thick SiO_2 dielectrics on its top and bottom surfaces. Although there are four wiring levels on Si-IF, only the bottom wiring level is considered to reduce the complexity of the simulation. The pitch of Cu wire is 10μm and the thickness is 2μm **[3]**. The wire length is 300μm in the simulation model, which is a reasonable value for compact die assembly with less than 100μm die space. Therefore, the total length of the data link is about 1100μm. The EM wave excitations are applied at the end of the Cu wires. All the parameters in the simulation are listed in TABLE 2.2.

TABLE 2.2 Parameters for Electrical Simulation

Parameter	Value	Parameter	Value
The dielectric constant of Silicon	11.7	The thickness of SiO_2 liner	2μm
The dielectric constant of the SiO_2	3.9	Cu wire pitch	10μm
Si Substrate resistivity	10Ω·cm.	Cu wire width	5μm
The diameter of Cu core	50 μm	Cu wire thickness	2μm
TWV height	500μm	Cu wire length	300μm
TWV pitch	100μm		

The simulated insertion loss S_{21} is plotted in Figure 2.9. Low insertion loss is obtained at both low-frequency range (less than 0.6dB at 1GHz) and high-frequency range (less than 3dB at 10GHz). It is also observed that scheme 2 shows 0.2dB lower loss than scheme 1 for signals with 0-10 GHz frequency. It can be attributed to lower insertion loss at the TWV/Cu wire interface.

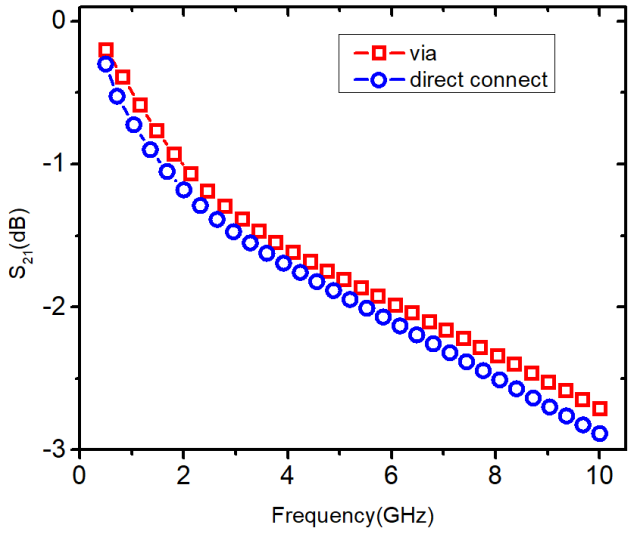


Figure 2.9 The insertion loss S_{21} for a data link with TWV

CHAPTER 3

Through-Wafer Vias for Power Delivery

The power delivery on Si-IF is achieved by TWV based power delivery network (PDN), where each TWV carriers 1A current from the power modules to the densely packed Si dies on Si-IF. The geometry of the TWVs for power delivery is similar to the cylindrical signal TWVs except that the diameter is increased to 100μm to reduce the resistance. In this chapter, we mainly focus on designing the interconnect schemes between power TWV and Cu wiring levels for the PDNs. Reliability issues such as current crowding at the interface of via and Cu wires, IR drops in the PDNs and current uniformity in the Cu wires are modeled and analyzed.

3.1 Simulation Model

Three interconnect schemes are compared in this chapter, as shown in Figure 3.1. In Scheme 1, the Cu wires are directly connected to TWV with a single damascene process. In Scheme 2, the Cu wires are connected to TWV by an array of vias, where 4×8=32 wires are fanned out for each TWV. In Scheme 3, the vias are fabricated at the periphery of TWV only and each Cu wire is then connected to one via, where 4×6 =24 wires are fanned out from each TWV. Both Scheme 2 and 3 can be fabricated by the dual damascene process.

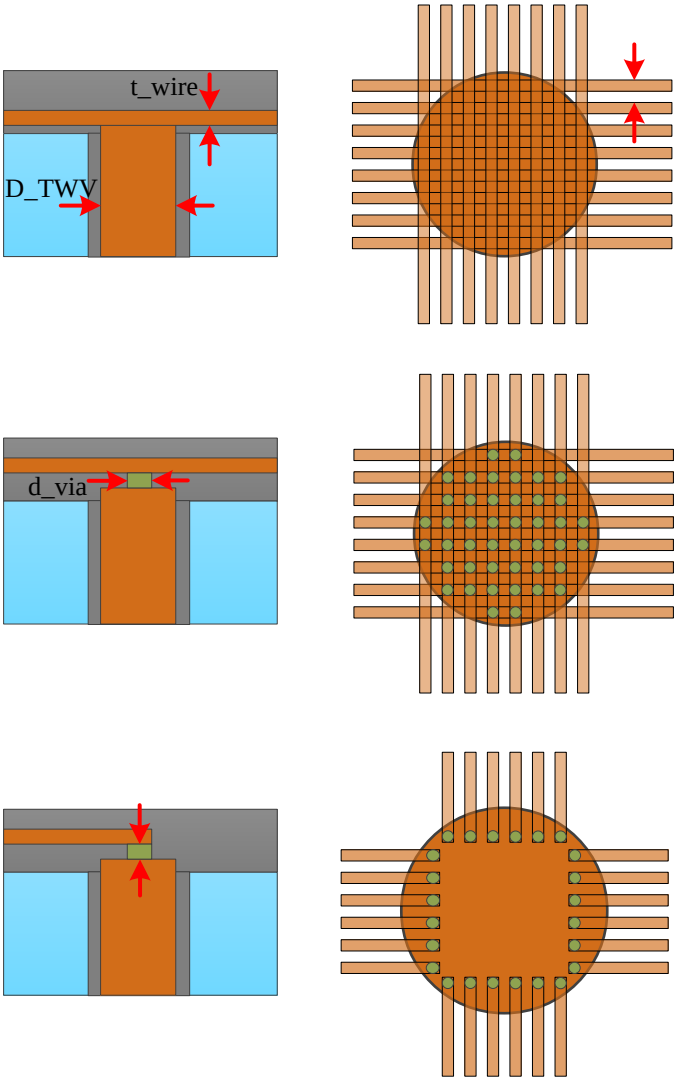


Figure 3.1 Three interconnect schemes between the power TWV and wiring levels

3.2 Modeling of Current Crowding Effect

For Cu wiring levels, electro-migration is induced by the “electron wind force”, where the electron flux drives Cu atom to a vacancy nearby and leaves behind a new vacancy at the original Cu atom position. The Cu atom flux is in the direction of current while the vacancy flux is in the opposite direction, which leads to void formation near the cathode. The void can increase wire resistance and even lead to interconnect functional failure. More information about the electro-migration can be found in **[15]-[17]**.

The locally enhanced current density, termed current crowding, is the primary cause of electromigration **[15]**. It occurs at the turning point of current flow due to resistance mismatch. The current density distribution in TWV and Cu wiring levels are examined by FEM simulation, where 1A current is carried by each TWV. Figure 3.2 plots the current density at the intersection plane of the via and Cu wire. For Scheme 1, current crowding occurs at the periphery of the TWV. For Scheme 2 and 3, current crowding occurs at the interface of the via and Cu wire. The maximum current density is 1.1×10^{10} A/m^2, 8.73×10^{9} A/m^2 and 7.4×10^{9} A/m^2 for the three interconnect schemes, respectively. These values are below the threshold for electromigration, which is 5.7×10^{10}A/m^2 for Cu **[3]**. Therefore, it is indicated that interface between TWV and Cu wiring levels are resistant to electromigration due to low current crowding.

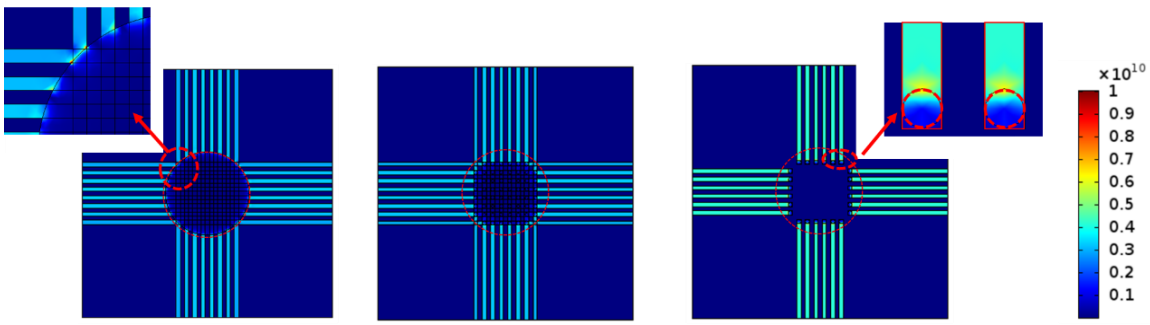


Figure 3.2 The current density distribution at the via/wire interface

3.3 Current Uniformity Analysis

The current enters each Cu wire can be different due to the non-uniform current density distribution at the TWV/Cu wire interface. Figure 3.3 shows the current in each Cu wire, which is normalized by the current in the ideal case. The Current non-uniformity ΔI is

defined as the difference between the maximum and minimum current. Scheme 1 shows poor current uniformity where ΔI is as high as 20%. In scheme 2, good current uniformity is observed for the Cu wires in the middle. However, for the two wires near the boundary, the current drops rapidly, resulting in ΔI = 8%. Good current uniformity is obtained in scheme 3 with less than 0.2% ΔI.

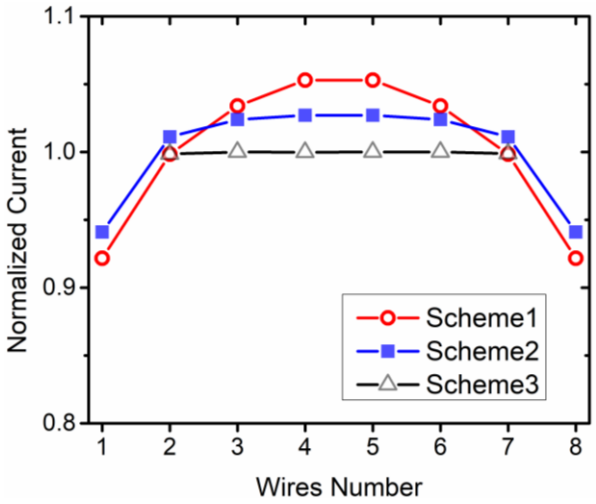


Figure 3.3 Current uniformity in different Cu wires

3.4 IR Drops in Power Link

The IR drop in a TWV based power link is evaluated with different Cu wire lengths, as plotted in Figure 3.4. It is observed that the IR drop varies linearly with the wire length. Scheme 1 and 2 show similar IR drops while Scheme 3 shows slightly higher IR drop since each wire carries higher current. If the maximum IR drop allowed is 2% V_{dd}, then the maximum length of Cu wire is about 200-250μm in this power link. It is also observed that the voltage drop rises if the via diameter is reduced to 50μm (the dashed line) because of higher via resistance.

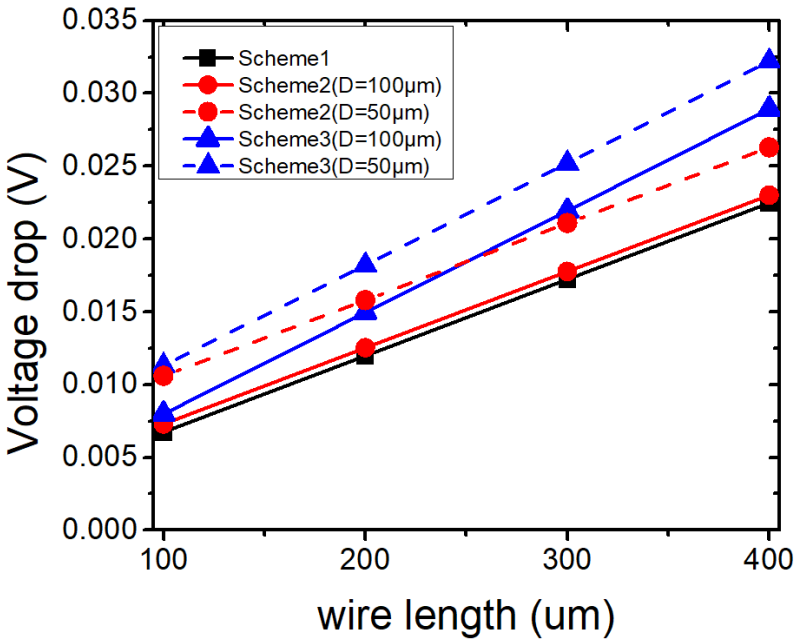


Figure 3.4 IR drop vs the length of wires

CHAPTER 4

Thermo-mechanical Reliability Analysis

Thermal excursions are applied to TWV when building the four-layer Cu wiring levels above it with the dual damascene process, as shown in Figure 4.1. The maximum temperature occurs during PECVD SiO_2 deposition. Under high thermal load, Cu via extrudes out of surrounding Si due to its higher coefficient of thermal expansion (CTE) **[18]**, resulting in non-uniform dielectrics deposition. The Cu wires built above the local extrusion will be thinned down after the CMP process, which leads to higher wire resistance **[19]**. Besides, high thermal stress can induce interfacial delamination at the Cu/SiO_2 interface and cohesive cracks in Si substrate due to the CTE mismatch between Cu, Si and SiO_2 **[20]-[23]**. It degrades the reliability and electrical performance of TWV and Si-IF. In this chapter, the thermal-mechanical reliability issues are analyzed to study the impact of process temperature on TWV reliability.

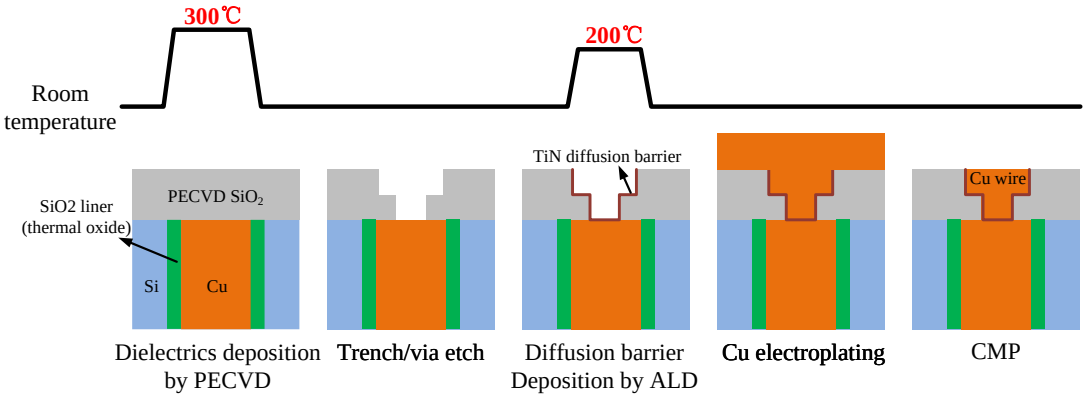


Figure 4.1 Thermal load applied to TWVs during the fabrication of Cu wiring levels

4.1 Simulation Model

The simulation model is shown in Figure 4.2. The Cu via is surrounded by a 2μm thick SiO_2 liner and the Si substrate. The bottom wiring level with 10μm pitch Cu wires is built above the TWV. The TiN diffusion barrier is neglected in this model because it is only 20nm thick. Anisotropic material property of Si is considered and its stiffness matrix is expressed as Eq. (4.1) **[19]**, which is a symmetrical matrix. Cu is treated as an orthotropic material and its Young's modulus and shear modulus are adopted from Ref. **[24]**. A non-linear material model is applied here to consider Cu hardening under plastic deformation, as listed in TABLE 4.2 **[21]**. The yield strength of Cu is 240MPa and its stress-free temperature is set to be 25℃. All the materials parameters used in the simulation are listed in TABLE 4.1. The symmetrical boundary condition is applied at the lateral surfaces to simulate a periodic TWV array on the Si-IF.

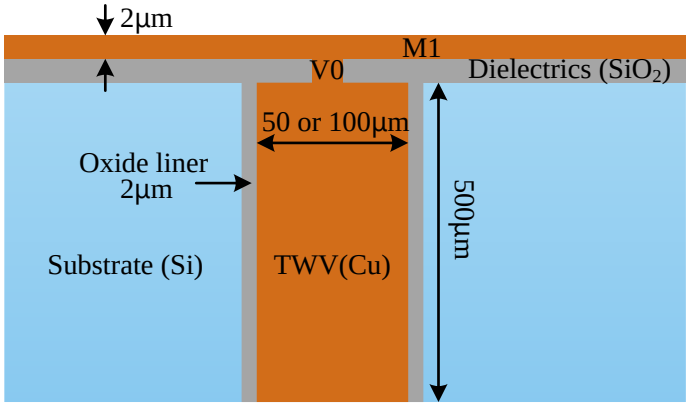


Figure 4.2 The cross-section view of the simulation model

TABLE 4.1 Materials Parameters in Thermal Mechanical Simulation

Materials	Young's modulus	Poisson's ratio	CTE (ppm)
Si	See Eq. (4.1)	0.21	2.6
Cu	E_1=156GPa E_2=68GPa E_3=68GPa G_{12}=G_{23}=G_{13}=60.96GPa	0.36	17

SiO_2	70GPa	0.17	0.5

TABLE 4.2 Hardening Function of Copper

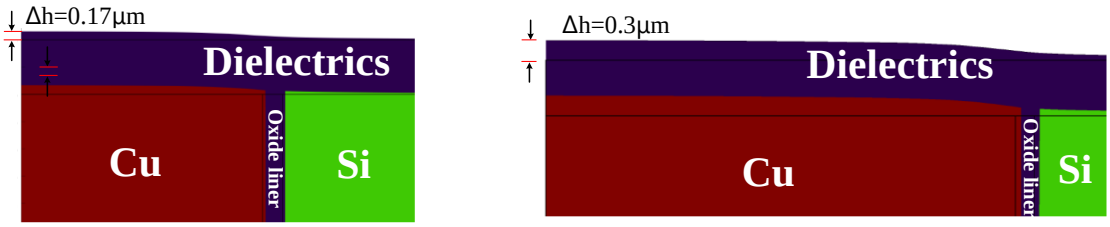
Stress(MPa)	Plastic Strain
240	0
250	0.003
255	0.007
255	0.009
250	0.007

$$S=\begin{bmatrix} C_{11} & C_{12} & C_{33} & 0 & 0 & 0 \\ C_{12} & C_{22} & C_{23} & 0 & 0 & 0 \\ C_{33} & C_{23} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{66} \end{bmatrix} \qquad \begin{aligned} C_{11} &= C_{22} = C_{33} = 165.7\,GPa \\ C_{12} &= C_{23} = C_{13} = 63.9\,GPa \\ C_{44} &= C_{55} = C_{66} = 79.6\,GPa \end{aligned} \tag{4.1}$$

4.2 Results and Discussion

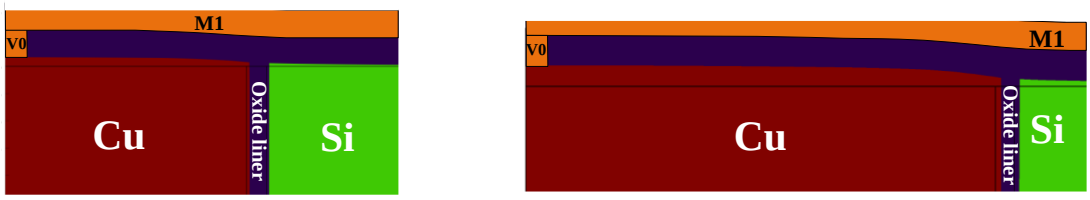
The effect of Cu extrusion is first analyzed. 300℃ thermal load is applied to TWV to simulate the situation during PECVD SiO_2 dielectrics deposition. Under this temperature, Cu via extrudes out of the Si substrate and induces non-uniform dielectrics deposition due to plastic deformation. As shown in Figure 4.3(a), the height variation Δh of the dielectrics is 0.17μm and 0.3μm for 50μm and 100μm diameter vias, respectively. The deformation is exaggerated when plotting the figure to make it more visible. The Cu wire on the local extrusion is thinned down after CMP process, which increases the local wire resistance, as shown in Figure 4.3(b). To solve this problem, the TWV is annealed and Cu extrusions are planarized by CMP before fabricating the

Cu wiring levels **[18]**.



D=50μm D=100μm

(a). Cu via pumping after PECVD oxide deposition



D=50μm D=100μm

(b). Deformed wire structure after M1 thining

Figure 4.3 (a). Cu via extrusion after PECVD oxide deposition. (b) The deformed wire after planarization by CMP.

The thermal stress distribution at 300°C is obtained by FEM simulator. In general, the thermal stress is higher for TWVs with 100μm diameter than 50μm, as shown in Figure 4.4 (a) and (c). High compressive stress is induced in the Cu via and Si substrate because of lateral Cu expansion, which can cause cohesive cracks **[22]**. High shear stress σ_{yz} is induced at the top of via because of Cu extrusion, as shown in Figure 4.4 (b) and (d). It induces plastic deformation and peels the Cu via off the SiO_2 liner, which is the driven force of interfacial delamination.

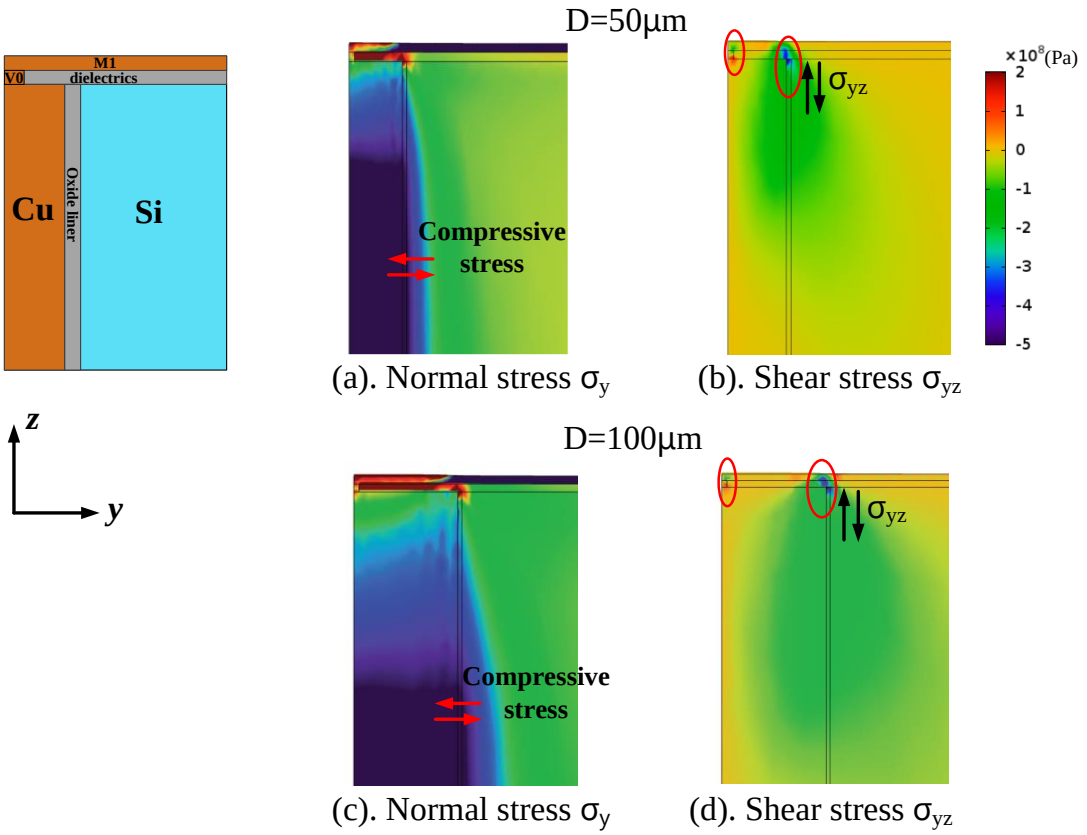


Figure 4.4(a) The normal stress σ_y (b) the shear stress σ_{yz} for via with a 50μm diameter (c) The normal stress σ_y (d) the shear stress σ_{yz} for via with a 100μm diameter. The temperature in the simulation is 300℃.

Under thermal stress, interfacial delamination initiates at defects such as micro-cracks or voids, which is introduced during the TWV process**.** Energy release rate (ERR) based fracture mechanical analysis is conducted to evaluate the potential risk of interfacial delamination under thermal load **[20]**. A pre-existing defect of length *a* is assumed at the Cu/SiO_2 interface and the total strain energy is *U*, as shown in Figure 4.5(a). When the crack length is increased by *da*, the materials along the crack is freed and the stored strain energy is released to break the atomic bond and extend the crack, resulting in strain energy change *dU* **[25]**. The energy release rate is calculated as ERR = -*dU*/*dA*, where *dA* is the surface area change of the crack.

The ERR is calculated under different process temperature for 50μm and 100μm diameter vias, as shown in Figure 4.5(b). Generally, the ERR is increased as the crack extends. If the ERR becomes larger than the fracture energy of the Cu/SiO_2 interface ($9J/m^2$ **[20]**), the crack will propagate catastrophically and induces delamination. Under process temperature of 200℃, ERR is smaller than the fracture energy of Cu/SiO_2 interface over a large range of crack length (0-30μm), which indicates that the delamination of Cu/SiO_2 interface can be avoided under 200℃. When the process temperature rises to 300℃, the ERR exceeds the fracture energy if the crack length is longer than 20μm, which indicates that delamination can be initiated by long cracks. Besides, it is also observed that higher ERR is induced by Cu via with larger diameter. The reliability issues can be alleviated by lowering the process temperature and increasing the process reliability in the TWV fabrication to reduce the number of defects.

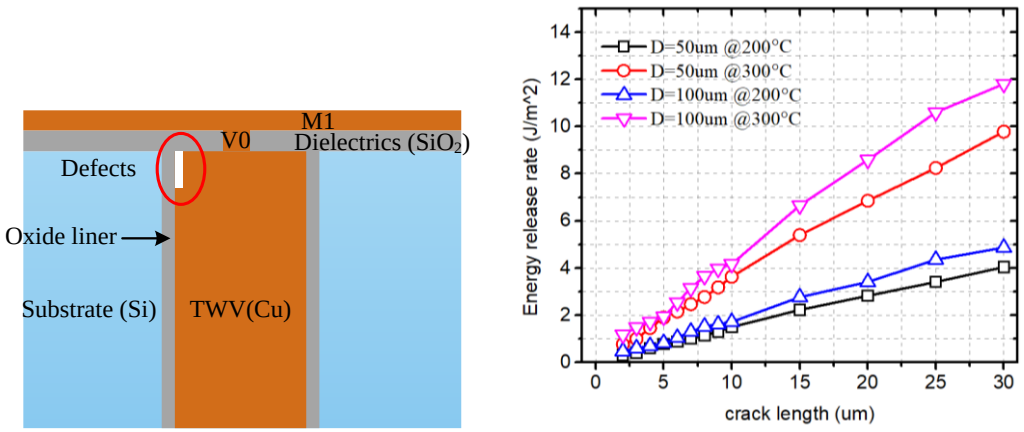


Figure 4.5 (a) the model to calculate ERR (b) The simulated ERR vs crack length

CHAPTER 5

Experiment Demonstration of Through-Wafer Vias

5.1 Fabrication Process of TWV

The fabrication process of TWVs is shown in Figure 5.1. The via is etched by Bosch etch process with 2μm thick Si oxide as hard mask. The photoresist cannot be used as the etch mask because of its high consumption rate during Bosch etch. A 1μm oxide liner layer is grown by wet oxidation for electrical insulation, which provides good film uniformity and step coverage in high aspect ratio via. TEOS based PECVD can also be used for oxide deposition **[26]**. A 20nm TiN diffusion barrier is deposited by ALD to prevent Cu diffusion into SiO_2. The via is filled by Cu electroplating after sputtering seed layer (600nm Cu/50nm Ti). Three challenges exist in the process because of the high aspect ratio of vias: 1). Obtaining desired via profile with acceptable etch rate. 2). step coverage of the deposition and sputtering steps. 3). void free Cu electroplating with an acceptable rate.

5.2 Via Etch by Bosch Process

The high aspect ratio vias on the Si wafer is created by Bosch etch process, which is featured of high etch rate, high selectivity and controllable profile **[27]**.

The Bosch etch is a multi-cycle plasma etch process that each cycle consists of passivation, polymer etch and silicon etch, as shown in Figure 5.2. The typical reactant

gases are SF_6, C_4F_8, and Ar. The glow charge of Ar helps with plasma formation. The high energy electrons in the plasma dissociate SF_6 and C_4F_8, which forms fluorine radical, SF_5^+ ions, and CF_2 monomer **[28]**.

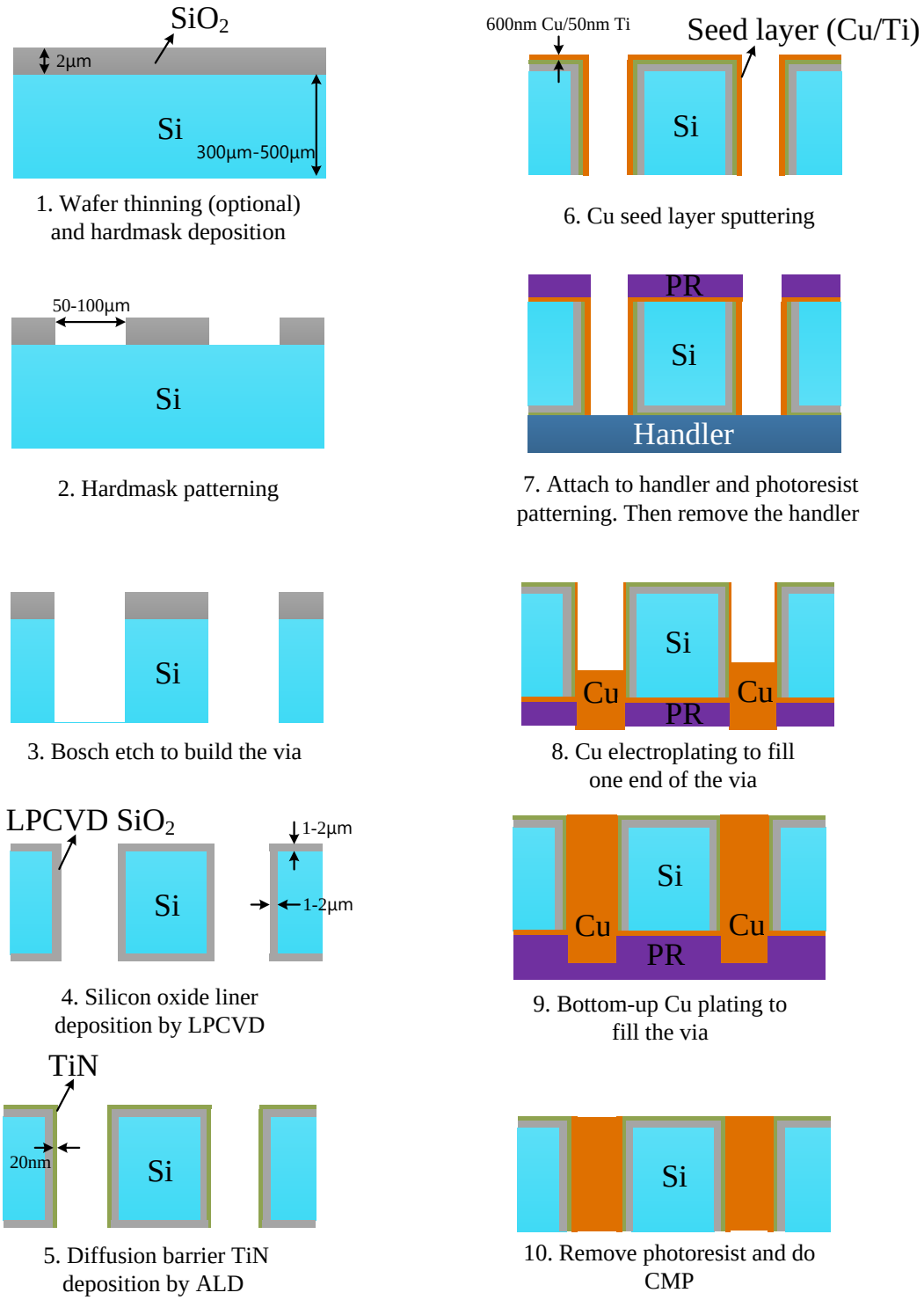


Figure 5.1 The fabrication process of TWV

In the passivation phase, the CF_2 monomer polymerizes on the sidewall and the bottom of the vias. The polymer passivates the Si surface and prevents it from chemical etch in the later etch phase. In the polymer etch phase, the SF_5^+ ions are accelerated under the high electric field in the plasma sheath and bombard the Si surface vertically, which selectively removes the polymer at the bottom and expose the Si surface. Then, in the Si etch phase, ion bombardment breaks the Si-Si bond at the surface and creates highly active dangling bonds. The fluorine radicals diffuse to Si surface and form volatile SiF_4. Si is removed when the SiF_4 is desorbed from the surface.

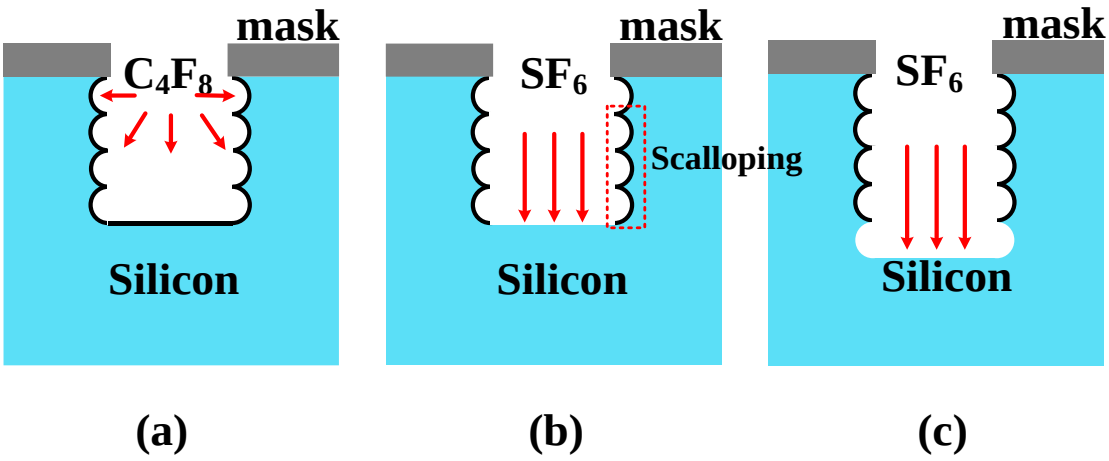


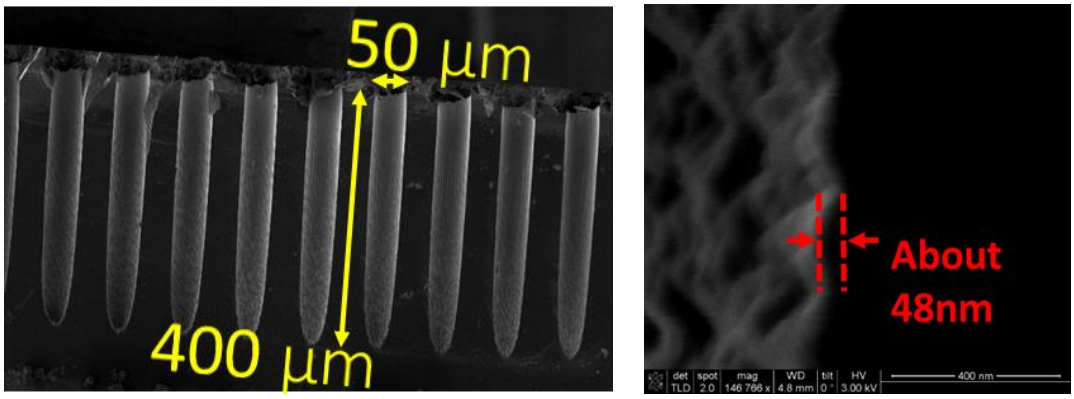
Figure 5.2 the three phases of a Bosch etch cycle (a) polymerization (b) polymer etch (c) silicon etch

5.3 Via Profile Characterization

Figure 5.3(a) shows the SEM images of the TWV cross-section with 50μm diameter after 100min Bosch etch. The sidewall profile is straight while it gets narrower and stops at about 400μm depth. It can be attributed to the impact of aspect ratio dependent etch, where the limited gas transport and less ion bombardment at the bottom of the via

makes it gets narrow and finally stops at the critical aspect ratio **[29]**. The impact of aspect ratio dependent etch can be reduced by increasing the bias power, reducing chamber pressure or using a ramped parameter process **[27]**.

The average etch rate is 6μm/min in the first 50min. Higher etch rate can be obtained by reducing polymerization time. However, the etch anisotropy is reduced at the same time and scalloping is increased because of thinner polymer on the sidewall. An optimal point of the etching rate and anisotropy should be achieved by balancing the duration of polymerization and etch steps.



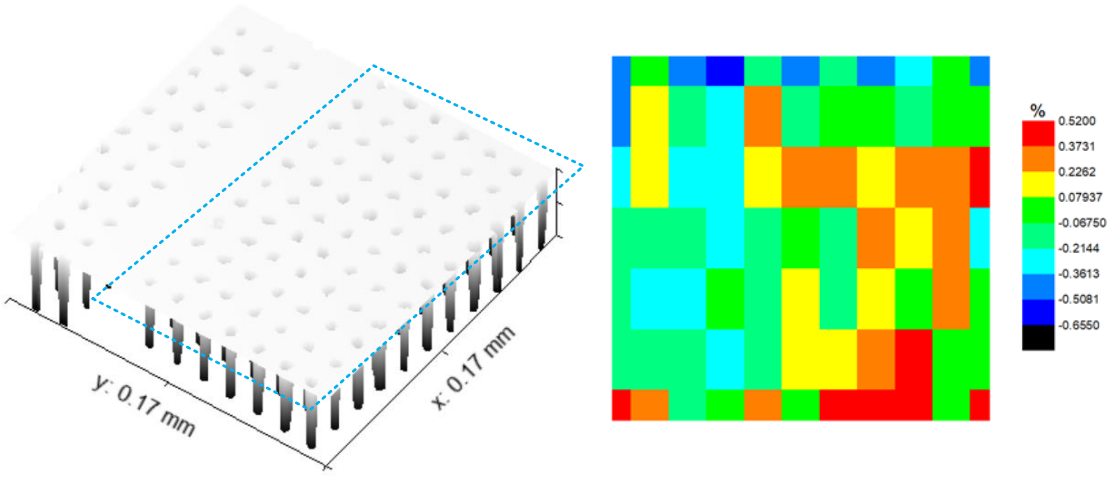
(a) (b)

Figure 5.3 (a) The cross-section view of 50μm diameter TWV under SEM after 100min Bosch etch (b) A zoom-in picture of the sidewall

Ideally, the etch process is anisotropic because of the sidewall passivation. However, since the passivation and etch steps are alternative, the freshly exposed sidewall is not covered by polymer and lateral etch occurs, which leads to scalloping at the sidewalls **[30]-[33].** Figure 5.3(b) shows a zoom-in picture of the via sidewall, where the amplitude of the sidewall is about 48nm. The scalloping on sidewall will impact the

step coverage and conformity of the dielectrics in the subsequent deposition process **[31]**. For vias with thin oxide liner, a large leakage current is also observed due to the poor dielectrics step coverage and cohesive crack induced by stress concentration at the scalloping protrusions **[32]**. Continuous gas flow can help reduce the scalloping. Thick SiO_2 liner (>1μm) also helps smoothen the scalloping.

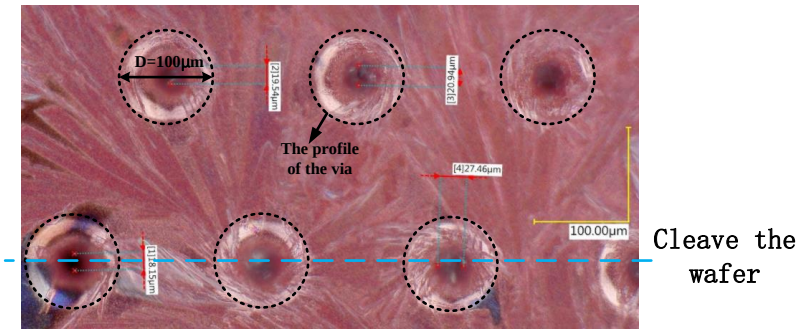
Optical profiler is used for non-destructive characterization of the 3D via profile, which provides a large field of view, as shown in Figure 5.4(a). Based on this measurement, the etch rate uniformity is calculated to estimate the etch time to etch through each via. Figure 5.4(b) shows the etch rate difference in the region marked by the dashed line in Figure 5.4(a). The etch rate of each via is normalized by the average etch rate. Only 1.2% etch rate difference is observed. The etch uniformity TWV density is also impacted by the local via density through micro-loading effect **[27]**, which should be considered during the layout design to get a uniform etch rate.



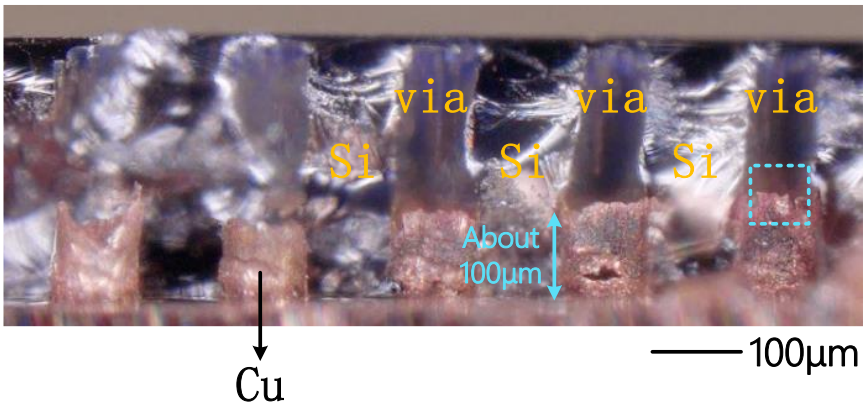
(a) (b)

Figure 5.4 (a) the via profile under an optical profiler. (b) The etch rate of different vias in the dash line box in Figure (a)

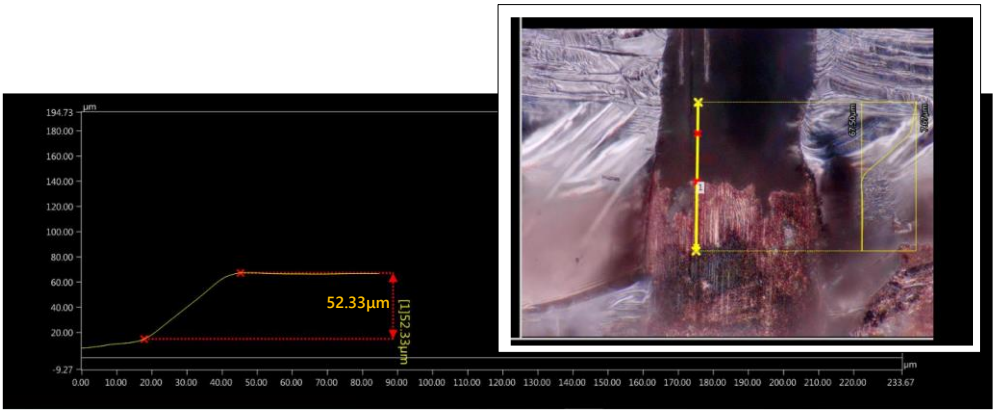
The top view of the vias after 3h Cu plating is shown in Figure 5.5 (a). The wafer is cleaved along the blue dash line to get cross-section image of the via, as shown in Figure 5.5 (b). Due to high via aspect ratio, only part of the via is covered by seed layer. Therefore, Cu is plated near one end of the via. The via sidewall profile in the blue dash line region is characterized by Keyence microscope. The sidewall profile along the yellow line is shown in Figure 5.5(c). The Cu thickness on the sidewall is about 52μm, which indicates that one end of the via is filled. With this Cu plug, a bottom-up Cu plating can be used to fill the via. Further improvement of the plating tool and chemicals should be conducted to obtain acceptable plating rate.



(a)



(b)



(c)

Figure 5.5 (a) top view of the vias after 3h plating. (b). the cross-section image of the vias (c) the profile of the sidewall in the blue dash line region in Figure (b).

CHAPTER 6

Plasma Dicing for Si-IF

6.1 Dicing Technology Requirement For Si-IF

On Si-IF, compact die assembly is conducted to reduce data latency. 20-40μm die space is achieved by advanced bonding tool with precise overlay control. However, with a rough die edge, the minimum die space and the distance from the metal pad to die edge are increased, which leads to longer data links, as shown in Figure 6.1. Therefore, smooth die edge is needed to get short data link. The mechanical strength of silicon die is also important because there is no die-level packaging on Si-IF, which requires less chipping and micro-cracks induced during dicing. Besides, polygonal die shape is preferred to increase the flexibility for die assembly.

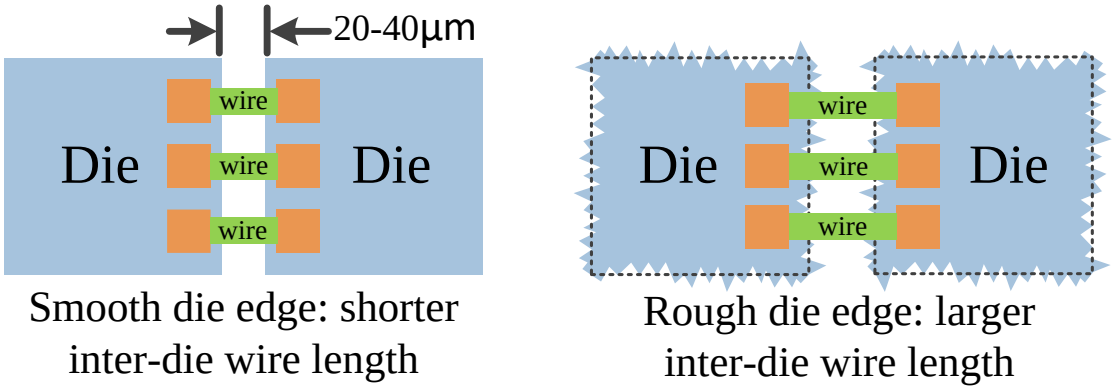


Figure 6.1 The data link between two dies with smooth and rough die edges

As discussed above, the requirement for dicing technology is summarized as follows.

- Smooth die edge

- No chipping and micro-cracks after dicing
- Flexible die shapes

6.2 Challenges in State-of-the-art Dicing Technologies

Saw dicing and laser dicing are the two common ways for Si die singulation. But unfortunately, none of them satisfies the above requirements. The drawbacks of saw dicing are listed as follows **[33]-[35]**.

- Rough die edge. Irregular fracture occurs under the high pressure induced by the blade, which is more significant for thinner wafers.
- Large dicing street (typically > 60μm) is needed to accommodate the blade. It reduces the total die area on one wafer, especially for wafers with small dies (1×1mm).
- Micro-cracks and delamination are introduced. Catastrophic die fracture can be induced by the cracks and die malfunction also occurs when the cracks propagate into the fragile low-k dielectrics. Keep out zone (KOZ) and crack stops are usually designed at the die edge to prevent the crack propagation, which further increases the length of the data links.
- Inefficient for thin dies. As the wafer becomes thinner, the blade feed speed needs to slow down to reduce chipping.

Laser dicing creates dicing street by the local high temperature induced by laser. The drawbacks of laser dicing are seen as follows **[36]**.

- Heat affected zones (HAZ) created by high local temperature. Neither active device nor interconnect can be put near the HAZ, which increases the length of the data

links.

- Multilayer delamination. Since multiple different materials are stacked on the wafer surface, multilayer delamination occurs at high temperature due to the CTE mismatch.
- Low throughput because the laser beam is scanned linearly.

6.3 Plasma Dicing Process

To overcome the drawbacks of current dicing technology, plasma dicing technology is developed. In plasma dicing, dies are diced by plasma assisted chemical etch instead of mechanical dicing. In this work, plasma dicing process for 300μm thick Si wafer is developed with acceptable etch rate.

A dummy dicing process is conducted to characterize the etch rate, dicing street profile and die edge roughness, as shown in Figure 6.2. The wafer is first thinned to 300μm by polish and CMP, which is a reasonable value that balances die strength and the etching time. Then 2μm PECVD SiO_2 is deposited as hard mask. Thermal oxidation cannot be used here because the active devices on a real wafer will be damaged by high temperature (>1000℃).The dicing street is then patterned on the hard mask by lithography and reactive ion etch. The width of the dicing street are 10μm, 20 μm, 30 μm and 40μm in this experiment. The wafer is attached to a handler after the photoresist is removed. Finally, the dicing street is etched by Bosch etch process to get the silicon dies.

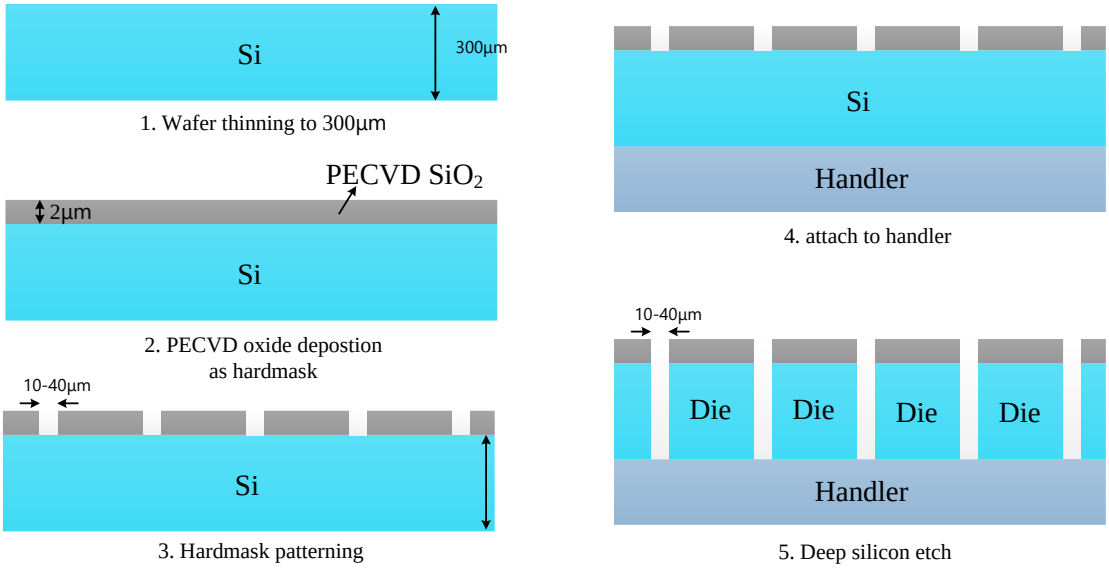


Figure 6.2 The process flow of plasma dicing (dummy dicing)

6.4 Profile Characterization

The 40μm width dicing street after Bosch etch is shown in Figure 6.3, where a smooth die edge is obtained. The width at the top of the dicing street is enlarged to 45μm, which can be attributed to the undercut effect during the Bosch process **[27]**.

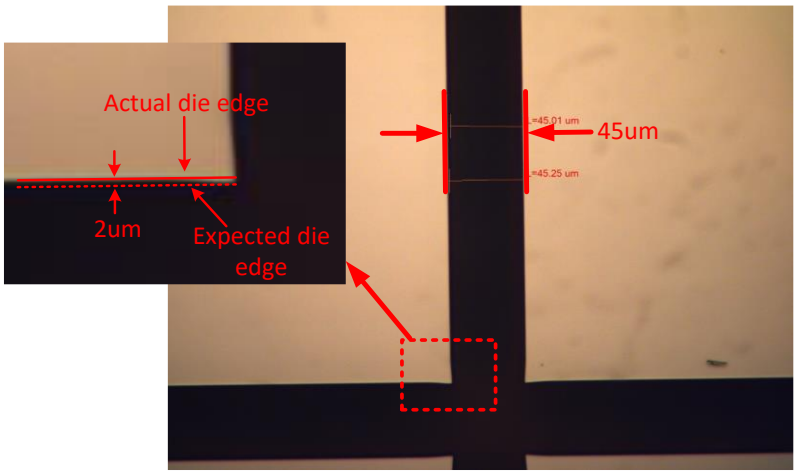


Figure 6.3 the dicing street of the die after plasma dicing

The etch rate for 10μm wide dicing street is about 6μm/min while it is about 6.5μm/min for the other three. It can be attributed to the lower etchant transport rate when the

aspect ratio is increased.

6.5 Throughput Benefits of Plasma Dicing

The time consumption to dice a 300mm wafer is compared with different dicing technology, including plasma dicing, saw dicing and laser dicing. For plasma dicing, the time consumption is calculated by dividing wafer thickness with etch rate. Two typical etch rate, 6μm/min (in UCLA Nanolab) and 15μm/min (state-of-the-art commercial tool) are used here. For saw dicing and laser dicing, the time consumption is calculated by dividing total dicing street length by dicing speed. The dicing speed of saw dicing depends on wafer thickness and the values are adopted from **[36]**. Figure 6.4 shows the calculated results. To dice $1cm^2$ square die on a 300μm thick wafer, saw dicing shows significantly higher efficiency than the other methods. However, when the wafer thickness is reduced to 100μm, plasma dicing becomes the most time-efficient method because the speed of saw dicing is slowed down from 120mm/s to 20mm/s to reduce chipping **[36]**. For smaller dies of $1mm^2$, plasma dicing provides quick wafer singulation while the dicing time of saw dicing and laser dicing is increased linearly as the dicing street length increases. Therefore, plasma dicing is beneficial for the situations where thin and small dies are required.

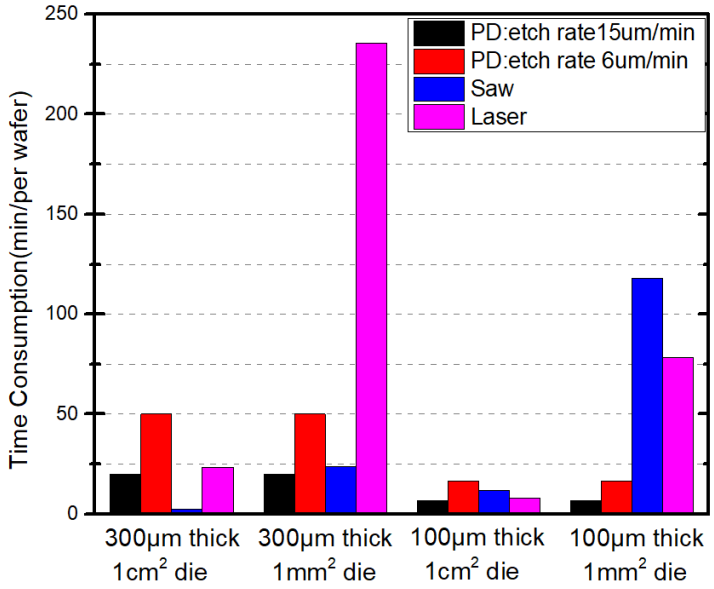


Figure 6.4 A comparison of the time consumption for 300mm Si wafer singulation with plasma dicing (PD), saw dicing and laser dicing.

CHAPTER 7

Conclusions and Future Work

In this thesis, the through-wafer via (TWV) technology is developed for signal and power delivery on silicon interconnect fabric (Si-IF). The electrical performance of through-wafer via is simulated by ANSYS HFSS width different design parameters. Low insertion loss is obtained when it is operating at the low-frequency range (<1GHz). The electrical reliability issues such as electromigration are examined and verified. The thermal reliability issues related to TWV during Si-IF fabrication are analyzed by simulation. It is observed that interfacial delamination can be induced at the interface between Cu via and SiO_2 liner due to the CTE mismatch between the materials. The TWV is fabricated in UCLA nanolab on a 300μm thick wafer. Plasma dicing technology is also developed based on deep silicon etch to obtain smooth die edge after dicing, which enables compact die assembly on Si-IF.

In the future, a novel electroplating method is to be developed for void-free copper plating with an acceptable rate. The electrical test is to be conducted to measure the via resistance and transmission property. Electromigration test is also to be conducted to examine the reliability issues when carrying high current.

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