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High Efficiency Power Amplifier Design Techniques for Advanced Transmitters

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by

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The dissertation of Bagher Rabet is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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LIST OF ABBREVIATIONS

AC	Alternating Current
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
AM-AM	Amplitude-to-Amplitude Modulation
AM-PM	Amplitude-to-Phase Modulation
Balun	Balanced-to-Unbalanced
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BW	Bandwidth
CM	Common Mode
CMOS	Complementary Metal-Oxide-Semiconductor
CW	Continuous Wave
DC	Direct Current
DM	Differential Mode
DPD	Digital Predistortion
DUT	Device Under Test
EVM	Error Vector Magnitude
FET	Field Effect Transistor
GND	Ground
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IM3	3rd Order Intermodulation
IQ	In-phase / Quadrature
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LDMOS	Laterally-Diffused Metal-Oxide-Semiconductor
LINC	Linear Amplification with Nonlinear Components
mm-Wave	Millimeter Wave
NMSE	Normalized Mean Squared Error
OFDM	Orthogonal Frequency-Division Multiplexing
OPA	Outphasing Power Amplifier

P_{1dB}	1-dB Compression Power
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PF	Power Factor
pHEMT	Pseudomorphic High-Electron-Mobility Transistor
Psat	Saturated Output Power
PSD	Power Spectral Density
Q	Quality Factor
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
SiGe	Silicon-Germanium
SILC	Single-Input Linear Chireix
SOI	Silicon-on-Insulator
TDDB	Time-Dependent Dielectric Breakdown
VCCS	Voltage-Controlled Current Source
VSWR	Voltage Standing Wave Ratio

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ABSTRACT OF THE DISSERTATION

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The emerging 5G and mm-wave high data rate wireless communication applications have exacerbated the challenges of the PA design, especially for the commercial Si-based ICs. The complex wideband OFDM signals in these applications, with high PAPR, demand stringent PA requirements of linearity, and efficiency at both peak and backoff power levels. This dissertation addresses the design challenges for sub-6GHz and 28GHz CMOS and SiGe integrated PAs, by introducing novel techniques and presenting them with proper

mathematical framework and modeling, alongside the hardware implementations that achieve record results.

Active load modulation, employed in Doherty and Chireix outphasing architectures, is one of the well-known techniques to improve the backoff efficiency of PAs. In theory, outphasing offers a better efficiency profile than Doherty, but it was traditionally believed that it works well only with voltage-mode PAs. However, recently it has been shown that for outphasing with current-mode PAs, if the input drive power reduced at backoff, good results can be achieved. In this dissertation a detailed mathematical analysis for current-mode outphasing is presented, and then the implemented 5.5GHz 45nm CMOS-SOI dual-input outphasing PA is discussed that achieves record average PAE of 30.9% while generating a 40MHz 64-QAM OFDM modulated signal with 7.9dB PAPR and 14dBm average output power.

At 28GHz band, the loss due to the integrated passive elements is one of the bottlenecks to achieve high efficiency. To address this issue a novel Chiriex combiner based on a “triaxial balun” is presented. An equivalent circuit model of the balun is introduced for the first time to make the analysis and design more straight forward. The implemented chip in 130nm SiGe BiCMOS process shows balun loss of only 0.5dB at 28GHz, and the dual-input outphasing PA achieves a record average PAE of 25.3% for an 8.1dB PAPR, 80MHz 64-QAM OFDM signal with average output power of 14.3dBm.

In phased array systems, it is not practical to employ individual digital predistortion (DPD) for each PA unit, and they must be inherently linear. A novel architecture named Single Input Linear Chireix (SILC) PA is introduced that not only has a high backoff efficiency but also has a linear response achieved by correcting the transistor related

distortions using the systematic AM-AM and AM-PM variations. The implemented PA in 130nm SiGe process demonstrates 19dBm saturated output power with 34.4% peak PAE and 6-dB backoff PAE of >23% at 27.5GHz. The modulated signal performance using a 100MHz 64-QAM OFDM signal shows average output power of 11.9dBm with PAE >20%, EVM <5%, and ACLR<-33dBc without using predistortion.

For 28GHz applications that require small footprint, the 2-stack CMOS PAs can offer enough output power with high peak efficiency. In order to improve the linearity, it is desirable to design for a "sweet spot" in the 3rd order intermodulation (IM3) at a critical power, where the distortion is significantly decreased. By adding a large resistor with a proper value at the gate of the transistor, the power dependent leakage current is used to create a dynamic bias that results in a slight amount of gain expansion that counters the gain compression due to the saturation of the PA. Experimental result using a 2-stack 28GHz PA implemented with 45nm CMOS-SOI shows peak output power of 19dBm and 43% PAE, and can attain high linearity without predistortion. Two-tone measurements show the formation of sweet spots at which IM3 decreases on order of 5-10dB at output power levels of order of 5dB backed off from P_{1dB}.

Chapter 1

Introduction

1.1 Background and Motivation

One of the important enablers of our present highly-interconnected society is the broad availability of wireless communication systems that allow the transmission of high data rates using compact devices with low power consumption. To support the further advancement of the wireless system capabilities, including higher data rates and wider signal bandwidths, there is an on-going research effort to move to higher frequencies ranges like the mm-wave regime, and to employ high-order QAM / OFDM signals with high peak-to-average power ratios (PAPR). One of the most significant challenges for the implementation of such systems is the design of the power amplifiers, which are responsible for accurately generating the required high frequency signals to be delivered to the transmitter antennas. The efficiency of power amplifiers typically decreases with increasing frequency, and with backoff from the maximum output power of the amplifier as required for modern complex modulations (whose peak-to-average power ratios are typically in the range of 7 to 10dB). The development of

power amplifier designs which improve efficiency is an important task for the future widespread deployment of 5G wireless systems, both at sub-6GHz frequencies and at mm-wave frequencies (particularly 24, 28 and 39 GHz).

In order to improve efficiency at power backoff, there are a number of architectures that have been exploited in existing 3G and 4G systems. Of these, envelope tracking, outphasing and Doherty amplifiers are the most popular power amplifier designs. Virtually every base-station amplifier in use today employs one of these variants in order to improve the overall transmitter efficiency. One common feature of these techniques, however, is the need for predistortion processing of the input signal in order to obtain a sufficiently accurate output signal (which must linearly replicate the desired signal in order to minimize transmission errors and to avoid producing spurious outputs in neighboring spectral bands). The predistortion in current systems is typically done using digital techniques (Digital Predistortion, DPD). This entails significant costs in power consumption and complexity, which increase as the signal bandwidth increases. For large base-station amplifiers, with output power in the range of 10's of Watts, the cost of the DPD can be absorbed. For future 5G systems, transmitters will be based on antenna arrays, using a multiplicity of power amplifiers (typically 16 to 256), each of which will have correspondingly lower output power than for 4G amplifiers; and each will have wider bandwidths than in use today. As a result, the use of DPD in the future will be significantly constrained, and there is a major effort to develop power amplifiers which do not require external predistortion in order to meet linearity objectives, while at the same time providing high efficiency for signals with high peak-to-average power backoff.

Another consequence of the fact that the overall power of the transmitter is shared by many power amplifiers, is that the power required of each power amplifier can be relatively modest (often in the range of 10's to 100's of mWs). This allows silicon-based technologies to be potentially used to meet the power amplifier needs. With the dimensional scaling of Si transistors, primarily driven in the past by digital circuit requirements, the speeds of the transistors have increased to the point where they have ample gain in the mm-wave regime. A key remaining concern is the need to improve their output power and efficiency to the point where they can meet 5G transmitter goals.

1.2 Dissertation Objective and Contributions

This dissertation addresses the design challenges for sub-6GHz and 28GHz CMOS and SiGe integrated PAs, by introducing novel techniques and presenting them with proper mathematical framework and modeling, alongside hardware implementations that achieve record results.

One of the novel techniques is a derivative of the outphasing amplifier architecture, in which the "voltage-mode" building block amplifiers employed in the conventional outphasing theory are replaced by more realistic current-mode amplifiers. The associated system is analyzed in detail, and an optimal control strategy for the current-mode amplifier inputs is derived, which provides high efficiency and at the same time minimizes input bandwidth requirements. The technique is demonstrated with a 5.5GHz 45nm CMOS-SOI dual-input outphasing PA that achieves record average PAE of 30.9% while generating a 40MHz 64-QAM OFDM modulated signal with 7.9dB PAPR and 14dBm average output power.

Another technique, also a derivative of the outphasing architecture, employs the current-mode outphasing method at mm-wave frequencies, along with a novel Chiriex power combiner based on a triaxial balun, which significantly reduces the losses compared with conventional combiners. The technique is demonstrated with a 28GHz PA in a 130nm SiGe BiCMOS process, which shows a balun loss of only 0.5dB; the dual-input outphasing PA achieves a record average PAE of 25.3% for an 8.1dB PAPR, 80MHz 64-QAM OFDM signal with average output power of 14.3dBm.

In order to avoid the need for DPD, a novel architecture named Single Input Linear Chireix (SILC) PA is introduced that not only has a high backoff efficiency but also has a linear response achieved by correcting the transistor-related distortions using the systematic AM-AM and AM-PM variations from the architecture itself. The implemented PA in 130nm SiGe process demonstrates 19dBm Psat with 34.4% peak PAE and 6-dB backoff PAE of >23% at 27.5GHz. The modulated signal performance using a 100MHz 64-QAM OFDM signal shows average output power of 11.9dBm with PAE >20%, EVM <5%, and ACLR<-33dBc without using predistortion.

An additional technique for linearity improvement is introduced in a 28GHz CMOS PAs using silicon-on-insulator (SOI) technology. It is desirable to design for a "sweet spot" in the 3rd order intermodulation (IM3) at a critical power, where the distortion is significantly decreased. It was shown that by adding a large resistor with a proper value at the gate of the transistor, the power-dependent leakage current can create a dynamic bias that results in a slight amount of gain expansion that counters the gain compression due to the saturation of the PA. With a 2-stack 28GHz PA, peak output power of 19dBm and 43% PAE was obtained; at the same time, two-tone measurements show the formation of sweet spots at

which IM3 decreases on order of 5-10dB at output power levels backed off from P_{1dB}, as desired for high efficiency high PAPR applications.

1.3 Dissertation Organization

This dissertation is organized as follows.

In Chapter 2, after a brief background, a detailed mathematical framework for the outphasing technique is presented. Then the rationale for and analysis of the outphasing architecture using current-mode building block amplifiers and its associated optimal control strategy is presented. The technique is demonstrated with a 5.5GHz 45nm CMOS-SOI dual-input outphasing PA.

Chapter 3 follows the same current-mode outphasing design principle for mm-wave frequencies, where the high insertions loss of the passive networks is a big challenge for achieving high efficiencies. To address this issue, a novel Chireix combiner based on a "triaxial balun" is presented. An equivalent circuit model of the balun is introduced for the first time to make the analysis and design more straight-forward. An implemented chip in 130nm SiGe BiCMOS process is described, which achieves record PAE in backoff.

The linearity aspects of the mm-wave PAs, while maintaining high efficiencies, are addressed in Chapter 4. The Single Input Linear Chireix (SILC) PA architecture is introduced that not only has a high backoff efficiency but also has a linear response achieved by correcting the transistor-related distortions using the systematic AM-AM and AM-PM variations. The technique is demonstrated with a PA implemented in 130nm SiGe technology which demonstrates record PAE for 64-QAM OFDM signals without the use of DPD.

A 2-stack CMOS PA is introduced in Chapter 5 that can offer enough output power with high peak efficiency for the mm-wave applications that require small footprint. In order to improve the linearity, the power-dependent gate leakage current is used to create a dynamic bias that results in a slight amount of gain expansion, forming a “sweet spot” in the 3rd order intermodulation response. Experimental two-tone results using a 28GHz 2-stack PA implemented with 45nm CMOS-SOI demonstrate the formation of sweet spots at which IM3 decreases on order of 5-10dB at output power backoff levels.

Chapter 2

Outphasing with Current-Mode Power Amplifiers

2.1 Introduction / Background

Outphasing was invented by Henri Chireix around 1935 as an efficiency improvement technique for the AM radio station power amplifiers (PAs) [1], and was employed in RCA's commercially successful *Ampliphase* transmitters from mid-1950s to 1970s [2]. A similar technique was introduced by D. C. Cox in 1974 for a different purpose; Linear Amplification with Nonlinear Components (LINC) [3]. Both methods work based on the same principle; the relative phase between two identical and constant-envelope unit PAs is varied in order to construct the desired signal that is obtained by combining the individual outputs. The difference, however, is in the type of the combiners that are required for each method.

For LINC applications, isolating combiners, like standard Wilkinson, are needed, so that there will be no load-pulling effects between the unit PAs and a highly linear overall

response can be obtained. Unfortunately, isolation comes at a cost; all the power that is not sent to the load gets wasted on the isolating resistor, because the unit PAs always generate a constant amount of power. This feature results in a Class-A like efficiency profile, meaning that the efficiency and output power drop with the same rate as the PA goes to backoff. Also, compared to a Class-A (or any other linear mode) PA, the required input signals for a LINC transmitter are subject to a severe bandwidth expansion that is cumbersome. Nevertheless, there are still some advantages in terms of efficiency and linearity to use a LINC architecture instead of a Class-A PA. The first advantage is that LINC makes it possible to modulate signals using highly efficient switching mode PAs (e.g., Class-E, Class-D) that are otherwise hard to backoff. This choice for unit PAs will improve the overall peak efficiency because for instance an ideal Class-D PA is twice as efficient as an ideal Class-A PA. It is also possible to restore some of the power sent to the isolating node, by using a rectifier, in order to further improve the efficiency [4]. The second advantage is more subtle and is related to heating. Class-A PAs get cooler at their peak output power and get hotter at backoff, but in LINC the unit PAs always remain at the same temperature. Therefore, the related memory effects that can degrade the linearity are not present.

For Chireix outphasing, on the other hand, the combiners are non-isolating, and the two unit PAs load-pull each other such that the efficiency improves at backoff. An in-depth analysis of the Chireix outphasing is provided in the next section.

2.2 Mathematical Analysis

Analysis of the Chireix outphasing scheme is usually done by replacing the unit PA cells with ideal voltage sources [5, 6], as shown in Fig. 2.1.

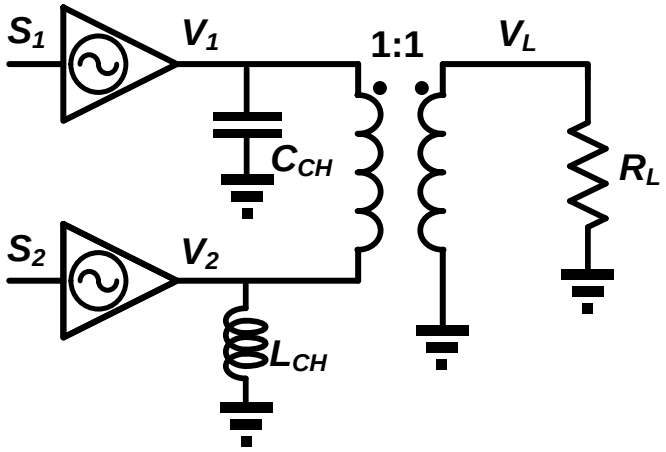


Figure 2.1: Voltage-mode Chireix outphasing.

The constant-envelope signals generated by these two voltage sources have equal amplitudes and opposite phases ($V_1 = Ae^{-j\varphi}$ and $V_2 = Ae^{+j\varphi}$), and the load power is controlled by varying φ (outphasing angle) from 90° to 0°, since $|V_L| = 2A\sin\varphi$. To find the impedance seen by each PA cell, the "Common Mode (CM) / Differential Mode (DM)" analysis method can be used.

$$V_{CM} = \frac{1}{2}(V_2 + V_1) = A\cos\varphi \tag{2.1a}$$

$$V_{DM} = \frac{1}{2}(V_2 - V_1) = jA\sin\varphi \tag{2.1b}$$

$$V_1 = V_{CM} - V_{DM} \tag{2.1c}$$

$$V_2 = V_{CM} + V_{DM} \tag{2.1d}$$

For CM excitation, the balun appears as an "open", therefore the CM current flowing into it is zero. For DM excitation, on the other hand, this current is $2V_{DM}/R_L$. Thus, the overall impedance at each port, presented by the balun itself (without considering L_{CH} and C_{CH}), can be derived.

$$Z_1 = \frac{V_1}{I_1} = \frac{V_{CM} - V_{DM}}{-\frac{2V_{DM}}{R_L}} = \frac{R_L}{2}\left(1 - \left(\frac{V_{CM}}{V_{DM}}\right)\right) = \frac{R_L}{2}(1 + j\cot\varphi) \tag{2.2a}$$

$$Z_2 = Z_1^* = \frac{R_L}{2}(1 - j\cot\varphi) \tag{2.2b}$$

In order to include the effect of Chireix compensating elements, it is easier to first convert the impedances (Z_1 and Z_2) to admittances (Y_1 and Y_2).

$$Y_1 = \frac{1}{Z_1} = \frac{2}{R_L}[\sin^2\varphi - j\sin\varphi\cos\varphi] \tag{2.3a}$$

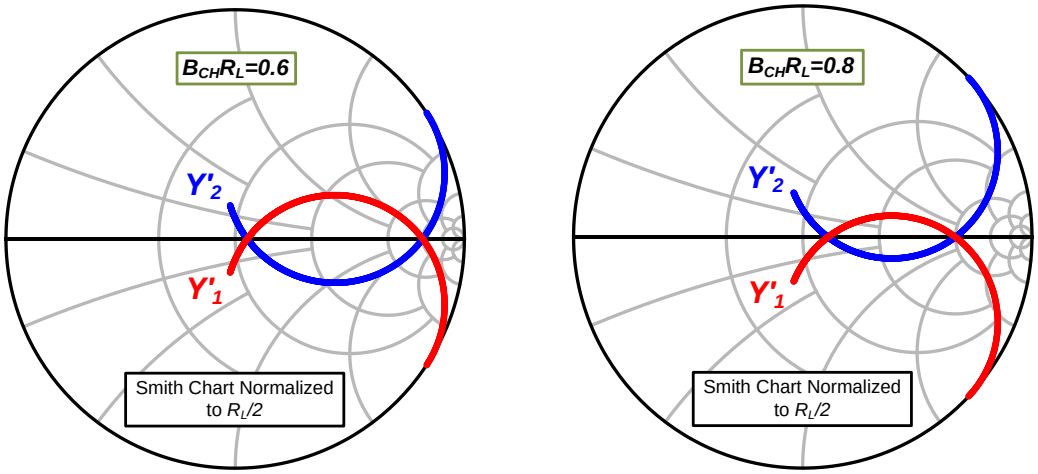
$$Y_2 = Y_1^* = \frac{2}{R_L}[\sin^2\varphi + j\sin\varphi\cos\varphi] \tag{2.3b}$$

Then, by adding $+jB_{CH}$ to Y_1 and $-jB_{CH}$ to Y_2, C_{CH} and L_{CH} are taken into account, and the overall admittances seen by the unit PAs (Y_1' and Y_2') are calculated.

$$Y_1' = Y_1 + jB_{CH} = \frac{2}{R_L}\left[\sin^2\varphi - j\left(\sin\varphi\cos\varphi - \frac{B_{CH}R_L}{2}\right)\right] \tag{2.4a}$$

$$Y_2' = Y_1'^* = \frac{2}{R_L}\left[sin^2\varphi + j\left(\sin\varphi\cos\varphi - \frac{B_{CH}R_L}{2}\right)\right] \tag{2.4b}$$

$B_{CH}R_L$ is the design parameter which determines the impedance profile seen by the unit PAs at power backoff. Figure 2.2 shows Y_1' and Y_2' on the smith chart for two different $B_{CH}R_L$ values.



(a) (b)

Figure 2.2: Admittances seen by the unit PAs in conventional Chireix outphasing designs for $B_{CH}R_L$ of (a) 0.6, and (b) 0.8.

The two points where the admittance curves on Fig. 2.2 cross each other are associated with the φ values that result in purely resistive load impedances seen by the unit PAs. These values can be found by setting the imaginary part of Eq. 2.4a to zero.

$$\sin\varphi\cos\varphi = \frac{B_{CH}R_L}{2} \;\Rightarrow\; \sin 2\varphi = B_{CH}R_L \tag{2.5a}$$

$$\varphi_1 = \frac{1}{2}\sin^{-1} B_{CH}R_L \quad , \quad \varphi_2 = 90° - \varphi_1 \tag{2.5b}$$

The real power generated by each unit PA (P_{PA}) can be calculated based on the assumptions made so far. Having a constant voltage amplitude at the outputs of the unit PAs means that P_{PA} varies only as a function of $Real\{Y'_{1,2}\}$.

$$P_{PA} = \frac{1}{2}\times\left|V_{1,2}\right|^2 \times Real\{Y'_{1,2}\} = \frac{A^2}{R_L}\sin^2\varphi = P_{PA,MAX}\sin^2\varphi \tag{2.6}$$

Similarly, η for an ideal Class-B PA with constant output amplitude, is only a function of $Real\{Y'_{1,2}\}$ / $|Y'_{1,2}|$ which is also known as *Power Factor* (PF)[1].

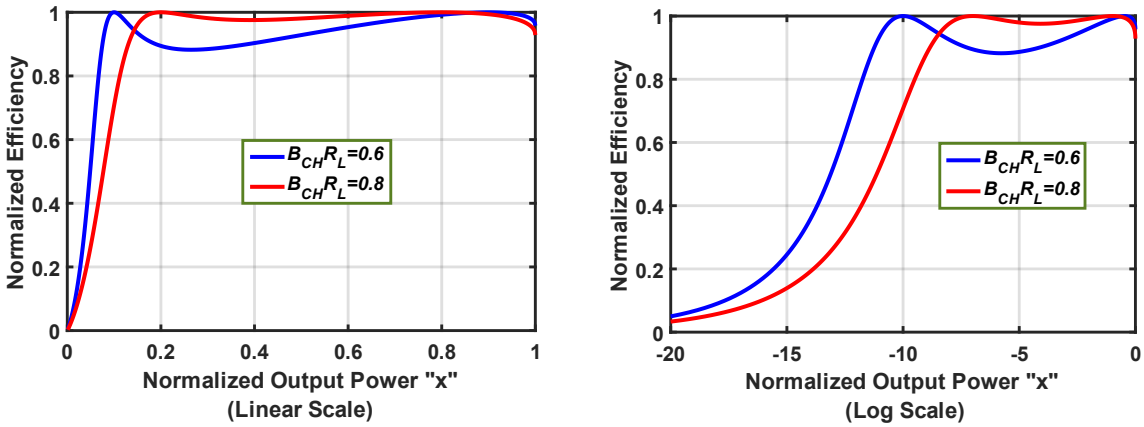
$$\eta = \eta_{MAX}\frac{Real\{Y'_{1,2}\}}{|Y'_{1,2}|} = \eta_{MAX}\frac{\sin^2\varphi}{\sqrt{(\sin^2\varphi)^2 + \left(\sin\varphi\cos\varphi - \frac{B_{CH}R_L}{2}\right)^2}} \tag{2.7}$$

The relation between η and P_{PA} is obtained by combining Equations 2.6 and 2.7. As a shorthand notation, we replace " $\sin^2\varphi$ " with "x".

$$\frac{P_{PA}}{P_{PA,MAX}} = \sin^2\varphi \triangleq x \tag{2.8}$$

$$\eta_{norm} = \frac{\eta}{\eta_{MAX}} = \frac{x}{\sqrt{x^2 + \left(\sqrt{x - x^2} - \frac{B_{CH}R_L}{2}\right)^2}} \tag{2.9}$$

Fig. 2.3 shows η_{norm} plotted vs. x for two different $B_{CH}R_L$ values.



(a) (b)

Figure 2.3: Efficiency vs. output power for classical Chireix outphasing in (a) linear scale and (b) log scale.

1- With a small approximation, this statement is also correct for an ideal Class-C PA.

The two peak efficiency points on each curve are associated with the two crossing points of Y_1' and Y_2' trajectories on the smith chart (Fig. 2.2).

It is important to note that a class-B PA, even a saturated one, does not resemble a voltage source [7], because for a current-mode PA when the load impedance has a varying reactive part (as is the case here), the phase of the output voltage does not follow the input signal. In order to satisfy this condition, voltage-mode PAs (e.g., Class-D) are needed, although they are not available at high frequencies.

The other disadvantages of this approach become apparent at deep backoff power levels where the two full-swing signals at the outputs of the unit PAs need to cancel out each other. Any mismatch between the two paths results in an unwanted signal to leak to the output and cause nonlinearity. Besides, since the input signals (S_1 and S_2 in Fig. 2.1) are also constant envelope, for low output power levels the overall gain is low and the power-added-efficiency (PAE) is degraded.

In order to address these issues, "outphasing with current-mode PAs" is proposed. In fact, an ideal Class-B PA can be modeled as a voltage-controlled current source (Gm), and is considered as a current-mode PA. A question arises, however, regarding how the condition of constant voltage envelope should be maintained at the outputs of the unit PA cells such that the outphasing operation is intact. To find the answer, we need to first look at the output currents of the unit PA cells under the ideal outphasing operation condition. I_1 and I_2, shown in Fig. 2.4, can be calculated by multiplying the required output voltages of the unit PAs (V_1 and V_2) by the admittances they see (Y_1' and Y_2').

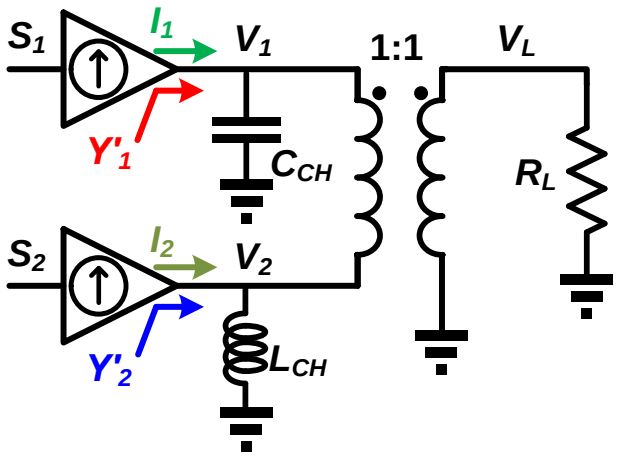
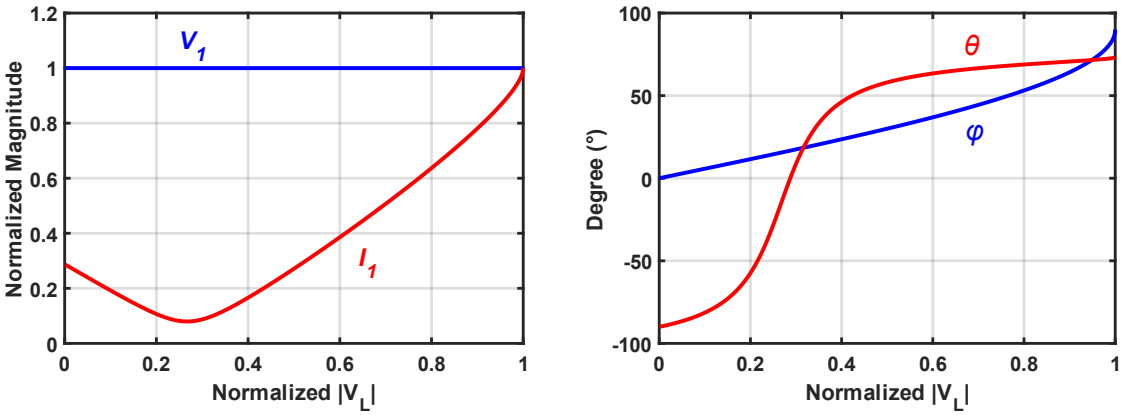


Figure 2.4: Current-mode Chireix outphasing.

$$I_1 = V_1 \times Y_1' = \frac{A}{R_L}[B_{CH}R_L \sin\varphi - j(2\sin\varphi - B_{CH}R_L\cos\varphi)] = |I_1|e^{-j\theta} \quad (2.10a)$$

$$I_2 = V_2 \times Y_2' = V_1^* \times Y_1'^* = I_1^* = |I_1|e^{j\theta} \quad (2.10b)$$

In Fig. 2.5, the normalized magnitudes of I_1 and V_1 and their phases (θ and φ) are plotted vs. normalized V_L, for a design with $B_{CH}R_L = 0.6$.



(a) (b)

Figure 2.5: (a) Magnitude and (b) phase variations of the output voltage and current of a unit PA in conventional Chireix outphasing with $B_{CH}R_L$ = 0.6.

From these plots it is clear that the magnitude of I_1 (and I_2) is not constant, and θ is not equal to φ (except at the two crossing points where the impedances seen by the unit PA cells become purely resistive). These details are important because for a Gm cell, it is the output current (not the voltage) that is controlled by the input. Therefore, *the PA input signals, S_1 and S_2, should be chosen based on the required I_1 and I_2*, so that the outphasing condition will be maintained. In an ideal case, S_1 and S_2 would simply be equal to I_1 and I_2 divided by a constant real Gm. In practice however, the nonidealities of the PA cells should be taken into account, meaning that the Gm will no longer be a constant real number.

The relationship between φ and θ can be calculated using Eq. 2.10a.

$$-\theta = \tan^{-1}\left(\frac{-2\sin\varphi + B_{CH}R_L\cos\varphi}{B_{CH}R_L\sin\varphi}\right) \tag{2.11a}$$

$$-\tan\theta = \frac{-2}{B_{CH}R_L} + \cot\varphi \tag{2.11b}$$

$$\tan\theta + \cot\varphi = \frac{2}{B_{CH}R_L} \tag{2.11c}$$

It is interesting to note that, as shown in Fig. 2.5, the required variation for θ in order to go from full power down to around 8dB backoff (0.4 normalized V_L) is much less than the variation required for φ (27° instead of 67°). This reduction in the required phase variation can be advantageous if analog circuitry is to be used to generate the input signals [8, 9].

Another issue with the canonical outphasing is that Y_1' and Y_2', as depicted in Fig. 2.2, become highly susceptive (reactive) after the second crossing point near the edge of the smith chart, resulting in low PF and thus low efficiency. The fast drop in η at deep power backoff is evident in the plots shown in Fig. 2.3. Also, the unusual increase of $|I_1|$ (and hence I_{DC})

toward low V_L values (Fig. 2.5) indicates the same fact. Fortunately, this problem can be resolved by employing the current-mode nature of the unit PAs when they are no longer forced to have a constant voltage envelope. To proceed with this idea, it will be useful to include the effect of the output voltage amplitude ($|V_{1,2}|$) in the equations of the efficiency (η) and power (P_{PA}) for the unit PAs.

$$\eta_{norm} = \frac{|V_{1,2}|}{|V_{1,2}|_{max}} \times PF = |V_{1,2}|_{norm} \frac{x}{\sqrt{x^2 + \left(\sqrt{x - x^2} - \frac{B_{CH} R_L}{2}\right)^2}} \tag{2.12}$$

$$P_{PA,norm} = \frac{P_{PA}}{P_{PA,MAX}} = \left(\frac{|V_{1,2}|}{|V_{1,2}|_{max}}\right)^2 \sin^2 \varphi = |V_{1,2}|_{norm}{}^2 x \tag{2.13}$$

Equation 2.13 shows that in addition to outphasing (varying x), reducing the voltage magnitude ($|V_{1,2}|$) can also be used to decrease the output power. Therefore, to avoid the fast drop in PF and η at deep backoff, it is better to stop doing outphasing below a certain power level and instead reduce the voltage magnitude, similar to the way that a standard class-B PA works ("mixed-mode" operation [10-12]). Doing so, the efficiency will drop with a rate proportional to the square root of the output power. To determine the optimal point for switching to "class-B mode", we first re-arrange Eq. 2.13 as $|V_{1,2}|_{norm} = \sqrt{P_{PA,norm}/x}$, and accordingly substitute $|V_{1,2}|_{norm}$ in Eq. 2.12.

$$\eta_{norm} = \sqrt{\frac{P_{PA,norm}}{x}} \times \frac{x}{\sqrt{x^2 + \left(\sqrt{x - x^2} - \frac{B_{CH} R_L}{2}\right)^2}} \tag{2.14a}$$

$$\eta_{norm} = \sqrt{P_{PA,norm}} \times \sqrt{\frac{x}{x^2 + \left(\sqrt{x - x^2} - \frac{B_{CH} R_L}{2}\right)^2}} \qquad (2.14b)$$

Equation 2.14b shows that, as the output power is reduced from its peak value, no matter by decreasing x (outphasing) or decreasing the voltage magnitude (class-B mode), the $\sqrt{P_{PA,norm}}$ term pulls down the efficiency with a square root rate. The improvement due to the Chireix outphasing, however, comes from the other term that is a function of x only ($f(x)$). To have a better understanding, $f(x)$ is plotted in Fig. 2.6, for $B_{CH}R_L$ of 0.6.

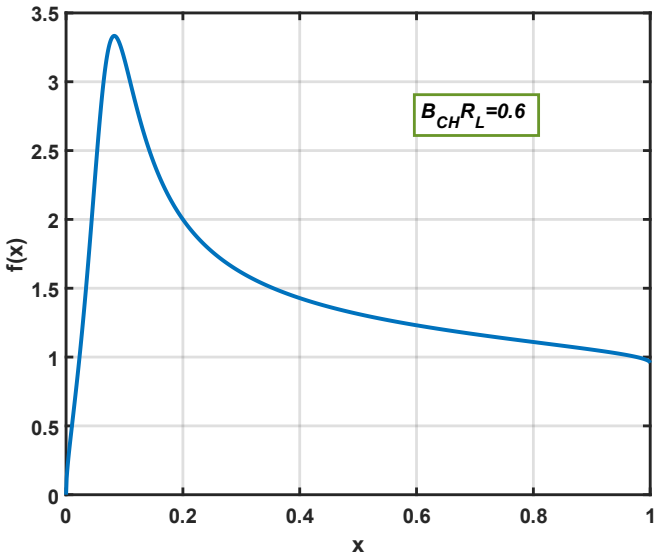


Figure 2.6: *f(x)* (the second term in Eq. 2.13b) vs *x* for $B_{CH}R_L$ = 0.6.

It is shown in this plot that as x decreases from 1 toward 0, $f(x)$ increases up to its maximum point, therefore the reduction in η (Eq. 2.14b) due to the first term ($\sqrt{P_{PA,norm}}$) gets compensated and the efficiency remains high. After its maximum point however, $f(x)$ also

starts decreasing in addition to the first term, causing the efficiency to drop fast. Thus, the optimal point to switch to Class-B mode is where $f(x)$ is maximum. This point can be found by setting the derivative of $f(x)$ equal to 0 and solving it for x.

$$\frac{df}{dx} = 0 \;\Rightarrow\; x_{switch} = \frac{(B_{CH}R_L/2)^2}{1 + (B_{CH}R_L/2)^2} \tag{2.15}$$

x_{switch} is slightly below the x value associated with the backoff peak efficiency point. For instance, in a case with $B_{CH}R_L$ of 0.6, the x value of the backoff peak point is equal to $\sin^2 \varphi_1$= 0.1 (where φ_1 is obtained by Eq. 2.5b), but the x_{switch} is equal to ~ 0.08. Also, it is interesting to note that x_{switch} corresponds to θ = 0°, which is obtained by finding $\cot \varphi_{switch}$ with respect to x_{switch} and plugging it in Eq. 2.11c.

$$\cot \varphi_{switch} = \sqrt{\frac{1}{\sin^2 \varphi_{switch}} - 1} = \sqrt{\frac{1}{x_{switch}} - 1} = \frac{2}{B_{CH}R_L} \tag{2.16}$$

$$\tan \theta_{switch} + \cot \varphi_{switch} = \frac{2}{B_{CH}R_L} \;\Rightarrow\; \tan \theta_{switch} = 0 \;\Rightarrow \theta_{switch} = 0° \tag{2.17}$$

Thus, for optimal control, θ needs to be varied from $\tan^{-1} 2/B_{CH}R_L$, that is related to the maximum load power (φ = 90° in Eq. 2.5b), down to 0° which is the switching point to Class-B mode. Figure 2.7 shows the impedance variations, efficiency enhancement and the voltage and current changes under the optimal control condition and compares it to the standard method.

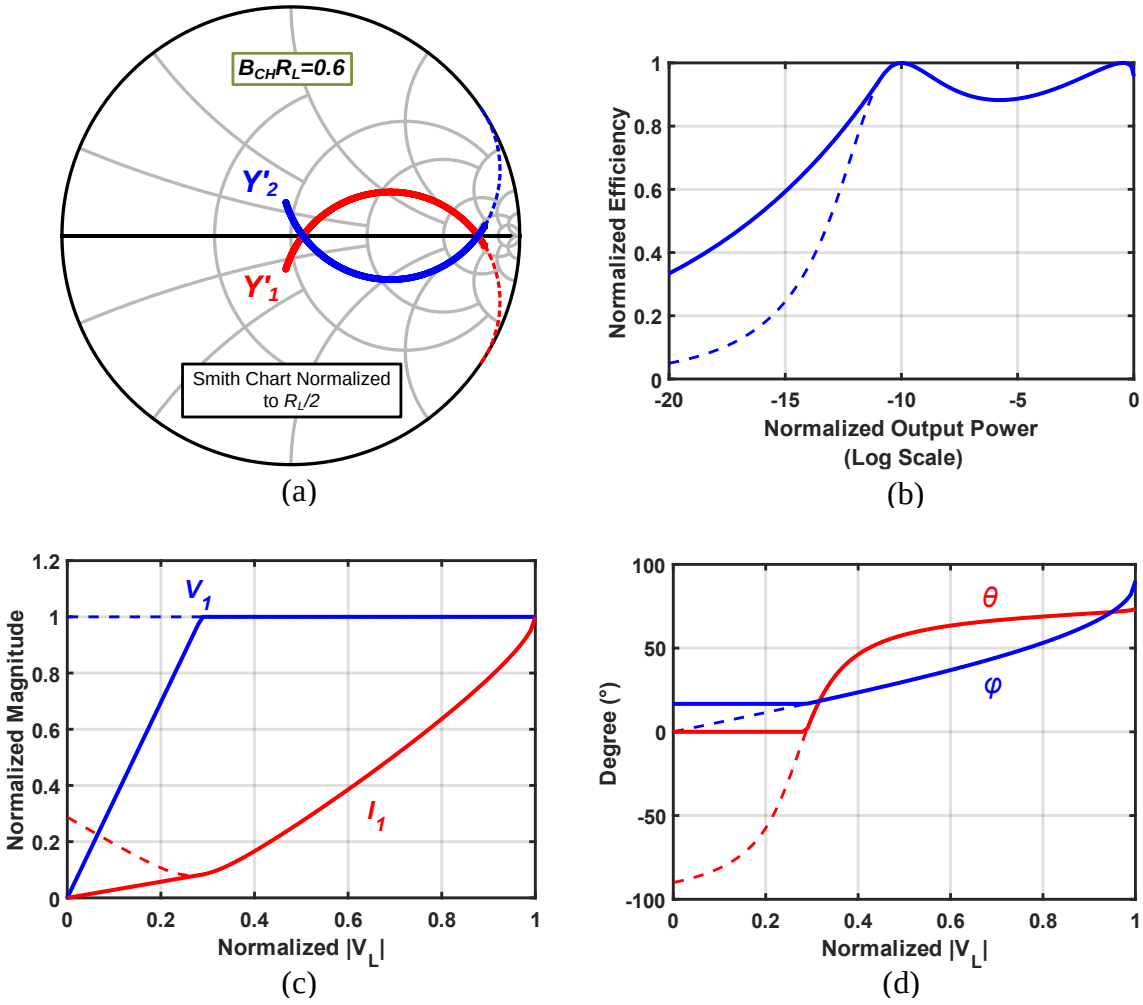


Figure 2.7: Comparison of the outphasing method with standard (dashed lines) and optimal (solid line) control functions for $B_{CH}R_L$ of 0.6; (a) impedance variations seen by the unit PAs, (b) normalized efficiency, (c) magnitude and (d) phase variations of the output voltage and current of a unit PA.

The last and one of the most important issues to discuss about outphasing, is the bandwidth expansion experienced by the input signals due to the required non-linear function of $\varphi = \sin^{-1}|V_L|_{norm}$. This problem is usually a major discouragement for the PA designers, preventing them from pursuing outphasing-based designs, especially for the modern applications with wide bandwidth signals. Here, with a simulation-based experiment, we show that for the current-mode outphasing with optimal control the bandwidth expansion is

greatly alleviated compared to the standard method. Figure 2.8 shows the normalized power spectral density (PSD) of a 100MHz 64-QAM OFDM signal with 9dB PAPR and compares it to the spectra of the input signals required in the standard and optimally controlled approaches.

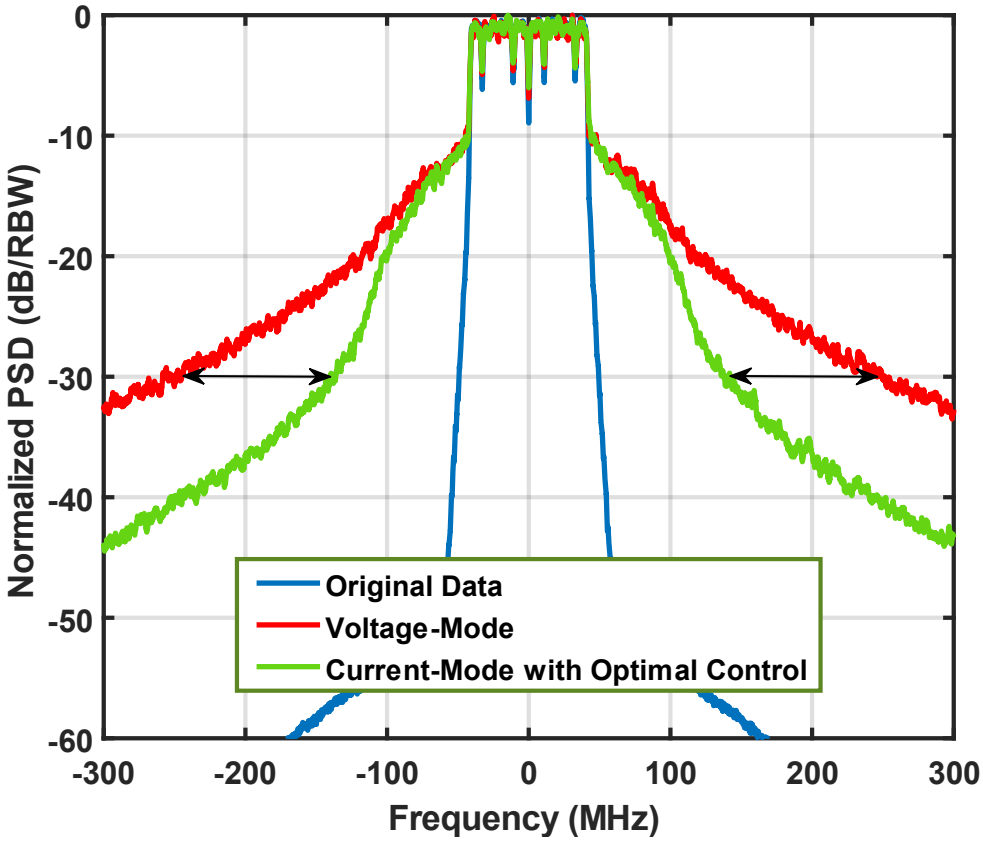


Figure 2.8: Normalized PSD for a 100MHz 64-QAM OFDM signal with 9dB PAPR and the related input signals required for the standard voltage-mode and the optimally controlled current-mode outphasing methods.

If we take the -30dB spectrum level as the reference, Fig. 2.8 shows that, compared to the standard outphasing, the bandwidth expansion in the optimally controlled current-mode approach is reduced by more than a factor of 2.

In this section, we reviewed the mathematical framework describing the Chireix outphasing operation for current-mode PAs, and showed that by optimally controlling the input signals, the problems associated with the standard voltage-mode outphasing (e.g., low efficiency, gain, and PAE at deep backoff, sensitivity to path mismatches, operation at high frequencies, and the bandwidth expansion of the input signals) can be resolved. Although similar analyses and conclusions have been published by other authors [11, 12], to the best of our knowledge, the equation describing the relation between the input and output outphasing angles (θ and φ in Eq. 2.11c), and the equations showing the optimal point to switch to class-B mode (Eq. 2.15 and 2.17) have been introduced here for the first time. In the next section we will explore a practical implementation of this technique using a CMOS IC process.

2.3 Design and Implementation

As a proof of concept, and in order to show the applicability of this technique in IC implementations, we designed a 5.5GHz dual-input current-mode outphasing PA, using a high-resistivity substrate 45nm CMOS-SOI process. Figure 2.9 shows the schematic of this design.

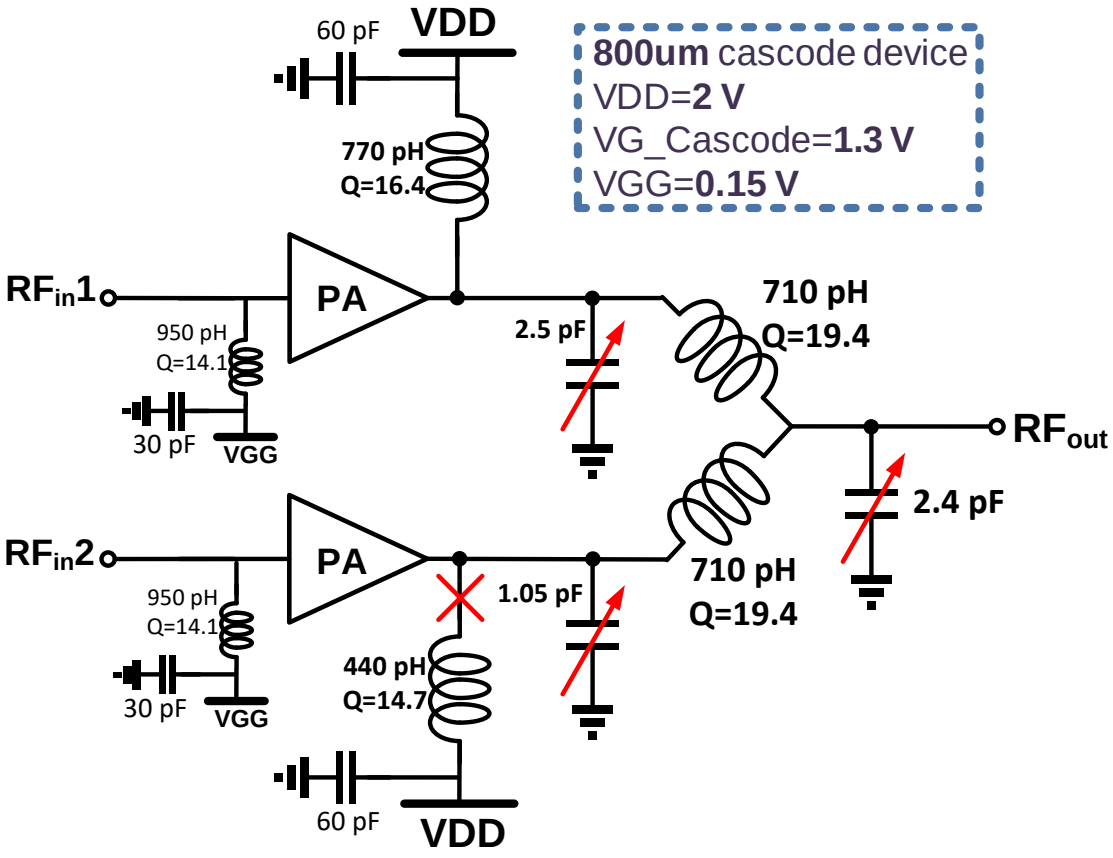


Figure 2.9: Schematic of the 5.5GHz dual-input current-mode outphasing PA implemented in 45nm high-resistivity substrate CMOS-SOI process. The red marks annotate the elements that are laser trimmed after the fabrication to achieve best tuning.

Note that we have implemented a common-mode combiner rather than a differential one that was described in the previous section. Two identical cascode cells with gate widths of 800um, Vdd of 2V, top gate bias voltages of 1.3V, and gate bias voltages of 0.15V (class-C) were used as the unit PAs. The high-resistivity substrate option was chosen to achieve a lower insertion loss in the passive elements of the output combiner. It is known that the loss caused by the electric and magnetic couplings from the inductors to the substrate, reduces considerably when it has a high resistivity. However, since this process was new at the time (offered for the first time), and the device models were premature for accurate simulations, we

designed the passive network such that we could tune it post process by laser trimming. This strategy included having segmented capacitive banks that are easy to laser trim, and two inductor options for the DC feed. As shown in Fig. 2.9, eventually the smaller inductor was trimmed out and the Vdd was supplied through the bigger inductor for both unit PAs. Figure 2.10 shows the die photo after the final tunings. The chip measures 1.2mm x 1mm including the RF and DC pads.

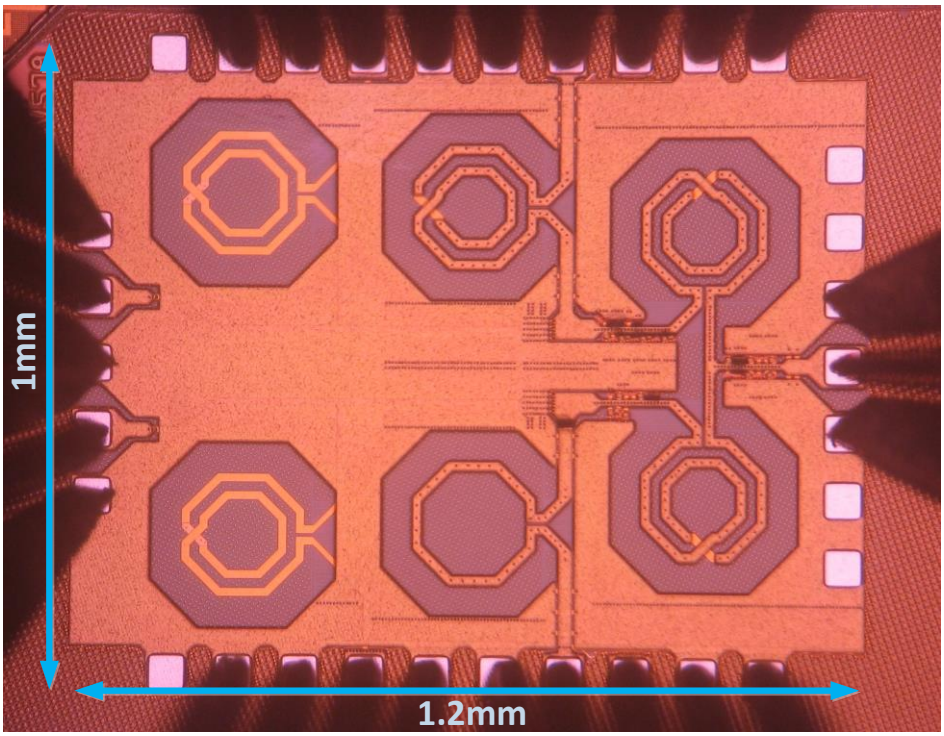


Figure 2.10: Die photo of the 5.5GHz dual-input outphasing PA after laser trimming.

2.4 Test Results

The unit PAs were biased in the class-C region, which results in a high efficiency as well as in a nonlinear gain (G_m) profile. Thus, the exact theoretical control functions, derived in section 2.2 by assuming a constant gm, are not directly applicable here, although the basics of that analysis hold thoroughly. The best strategy, therefore, is to sweep the two input signals, with equal amplitudes and opposite phases to each other, in order to find the best control function for the highest efficiency. Figure 2.11 shows the results of such a sweep.

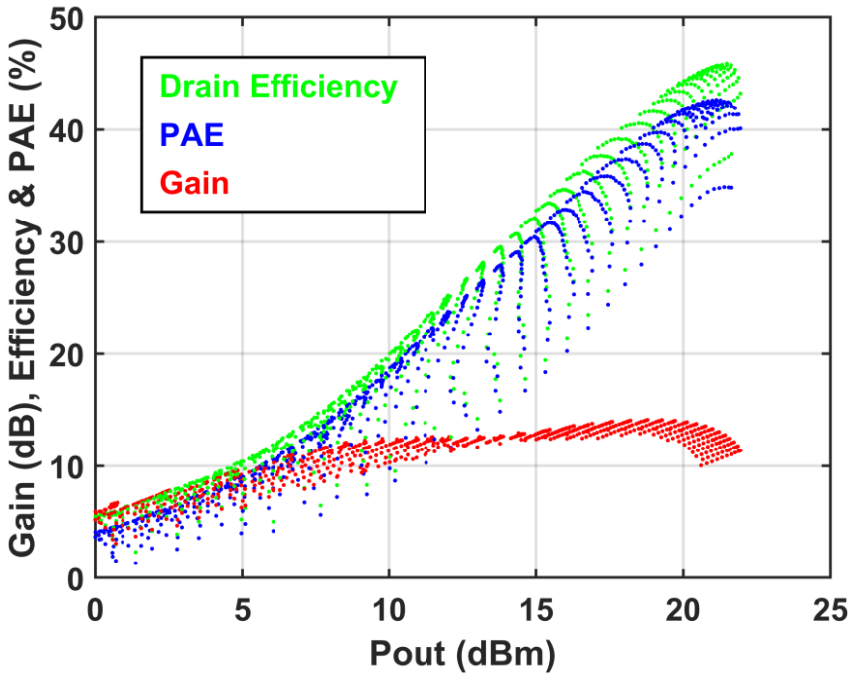


Figure 2.11: Measurement results of a simultaneous sweep of the input amplitude and outphasing angle (θ) to find the best control function for the highest efficiency.

By choosing the highest PAE points for each output power in the plot of Fig. 2.11, the optimal control functions for the input amplitude and phase are obtained. Figure 2.12 shows these functions.

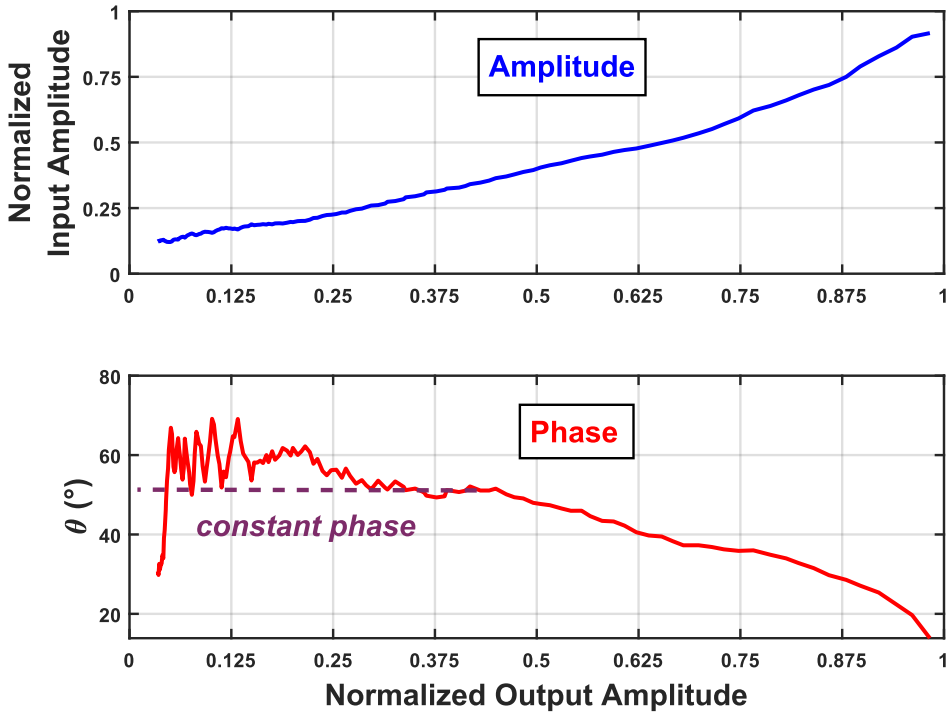


Figure 2.12: Optimal control functions for the input amplitude and outphasing angle (θ), obtained by the sweep measurement. The noisy part of the phase function at the low power region is replaced by a constant value as shown by the dotted line.

Note that since we have implemented a common-mode combiner in this design, the curve of θ is flipped vertically compared to what was shown in Fig. 2.7. Following the optimal control functions, the static performance of the PA is evaluated be measuring the continuous wave (CW) response, that is shown Fig. 2.13.

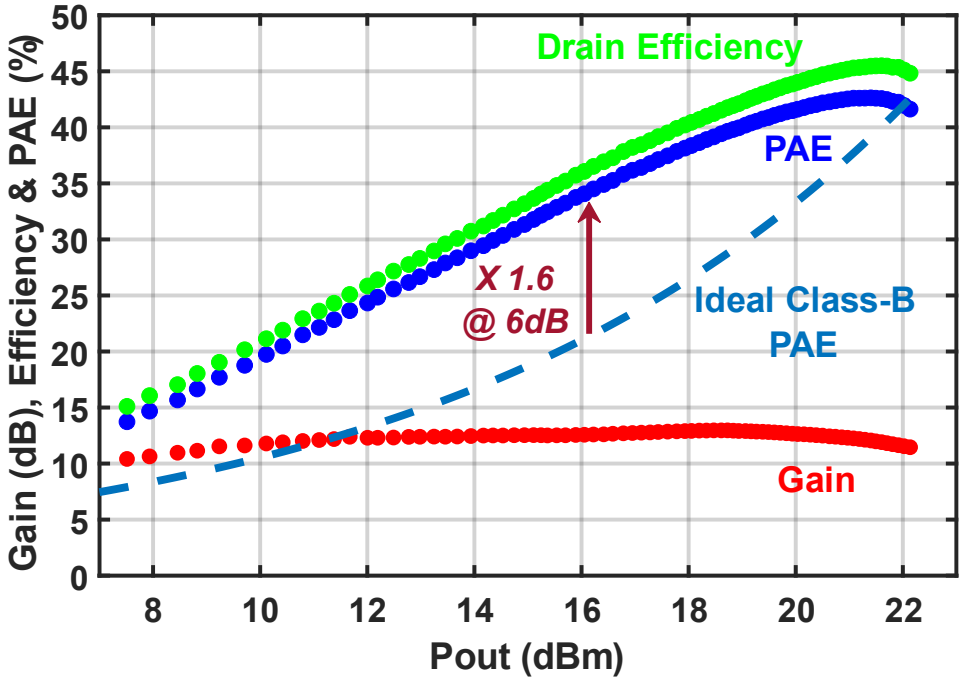


Figure 2.13: CW performance measured at 5.5GHz. The gain is defined by P_{out} /(P_{in1}+P_{in2}). At 6-dB power backoff the PAE is improved by 1.6 times compared to an ideal class-B PAE.

At 5.5GHz, the PA achieves 22.1dBm P_{sat}, 42.6% peak PAE, and 6-dB backoff PAE of 34% that is 1.6 times improvement over the ideal class-B case. The gain for dual input is defined as $P_{out}/(P_{in1} + P_{in2})$.

In order to evaluate the dynamic performance of the PA, a 40MHz 64-QAM OFDM signal with 7.9dB PAPR is used. The response was linearized by utilizing a simple memoryless DPD. Also, the whole measurement setup including the PA was equalized. The results are depicted in Fig. 2.14.

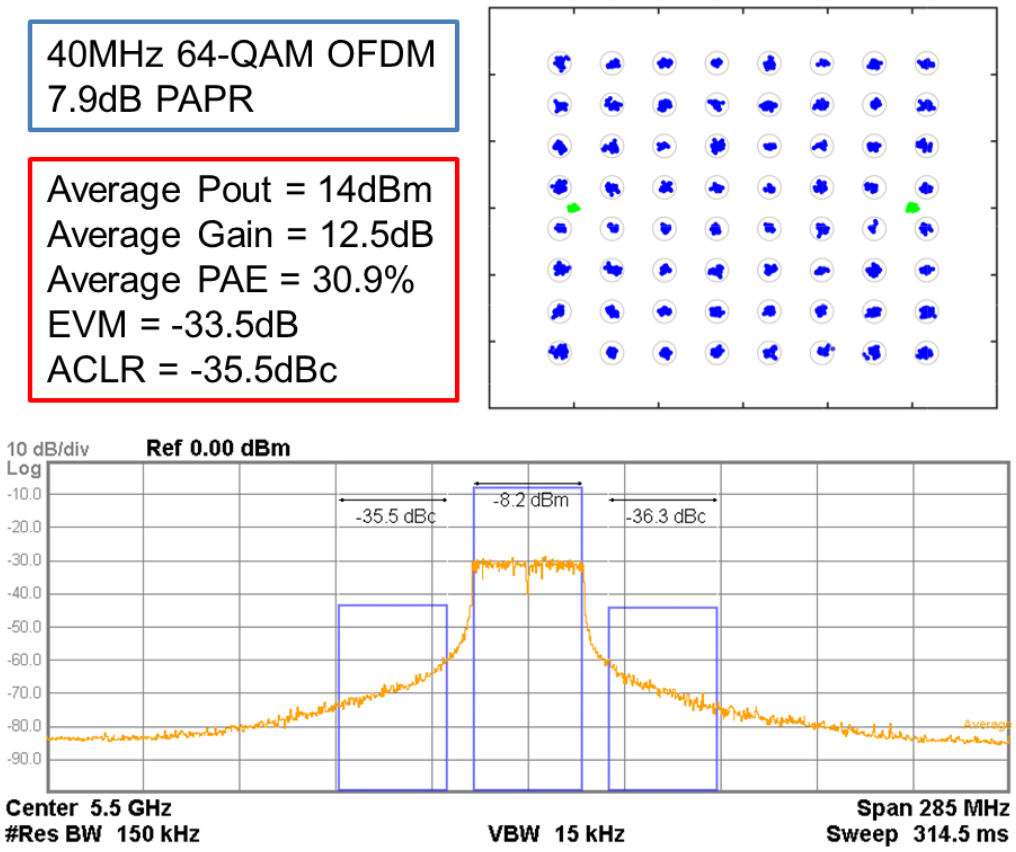


Figure 2.14: Modulated signal performance of the PA for a 40MHz 64-QAM OFDM signal with 7.9dB PAPR centered at 5.5GHz.

The PA achieves 30.9% average PAE and 14dBm average output power with the EVM better than -33.5dB and ACLR better than -35dBc. Another modulated signal test was run using an 80MHz 64-QAM OFDM signal with 8.1dB PAPR. Similar to the previous test, memoryless DPD and equalization of the setup were utilized. Figure 2.15 shows the results.

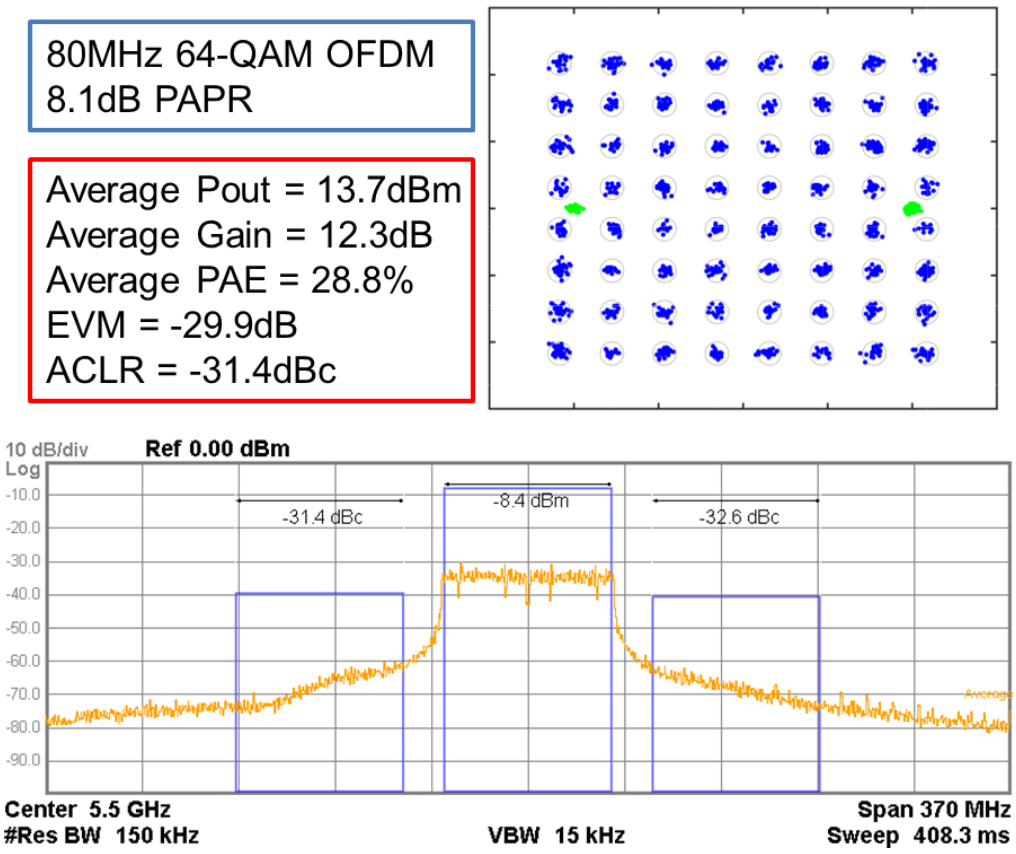


Figure 2.15: Modulated signal performance of the PA for an 80MHz 64-QAM OFDM signal with 8.1dB PAPR centered at 5.5GHz.

For the 80MHz signal, the PA demonstrates 28.8% average PAE with average P_{out} of 13.7dBm. The EVM is -29.9dB and the ACLR is better than -31dBc. Table 2.1 summarizes the performance of the PA and compares it to the state of the art.

Table 2.1: Comparison to state of the art.

	This work	[13] RFIC'16	[14] ISSCC'15	[15] JSSC'17
Frequency (GHz)	5.5	5.9	3.7	3.5
Technology	45nm CMOS	40nm CMOS	65nm CMOS	45nm CMOS
Architecture	Outphasing	Outphasing	Class-G / Doh.	Class-G / Doh.
PA Cell	Class-C	RFDAC / E	RFDAC / D^{-1}	SC / D
P_{SAT}(dBm)	22.1	22.2	26.7	25.3
Peak PAE (%)	**42.6**	34.9	40.2*	30.4
6-dB PBO PAE (%)	**34**	19	37*	25.3
Modulation Type	64-QAM OFDM	64-QAM Single Carrier	16-QAM Single Carrier	256-QAM OFDM
Signal BW (MHz)	**40 / 80**	20	1	10 / 40
Pre-distortion	Mem-less DPD	Mem-less DPD	Mem-less Dyn.	Mem-less DPD
Average Pout (dBm)	14 / 13.7	16.4	20.8	17.1 / 15.6
EVM (dB)	-33.5 / -29.9	--	-24	-40.1 / 35.8
Average PAE (%)	**30.9 / 28.8**	16.1	28.8*	21.4 / 19.2

* Drain Efficiency

To the best of our knowledge, this work demonstrates the highest reported average efficiency for a CMOS PA in the 5GHz band.

2.5 Conclusion

An in-depth mathematical analysis of the outphasing technique for power amplifier efficiency improvement was presented in this chapter. The short-comings of the standard voltage-mode outphasing were discussed and it was shown that by utilizing current-mode PA cells and optimally controlling them, the backoff gain, efficiency and PAE can be improved, the bandwidth expansion of the input signal can be reduced, and the operating frequency can be extended to the range where voltage-mode PAs cannot be realized. We introduced new

equations describing the relation between the input and output outphasing angles, as well as equations describing the optimal control functions. Next, we demonstrated a CMOS IC implementation of this method for sub-6GHz band with an exceptional performance. The PA achieved 22.1dBm P_{sat} at 5.5GHz, with 42.6% peak PAE, and 6-dB backoff PAE of 34%. The modulated signal performance showed average efficiencies as high as 30.9% and 28.8% for 64-QAM OFDM signals with 40MHz and 80MHz bandwidth, 7.9dB and 8.1dB PAPR, average output powers of 14dBm and 13.7dBm, and EVMs of -33.5dB and -29.9dB, respectively. To the best of our knowledge, these numbers are record results for a CMOS PA at this frequency band.

Acknowledgement

This chapter is co-authored with H. Gheidi and P. Asbeck. The dissertation author was the primary investigator and author of this chapter.

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Chapter 3

mm-Wave Outphasing Power Amplifier Design Using the Triaxial Balun

3.1 Introduction

Gigabit-per-second millimeter-wave (mm-wave) access and backhaul networks at 28GHz demand high-order QAM, OFDM, and/or carrier-aggregated waveforms that force the PA to operate under high peak-to-average power ratio (PAPR) [1]. High PAPR requirements aggravate the design of mm-wave Si CMOS and SiGe BiCMOS PAs since a linear response and high efficiency are simultaneously desired. Recent work has demonstrated mm-wave PAs with peak efficiency exceeding 30% at 28GHz for output powers above 20dBm [1-5]. However, high average efficiency associated with high-PAPR waveforms remains elusive. To improve average efficiency, circuit techniques based on Doherty [3] and outphasing [6] have been demonstrated in mm-wave bands. Earlier work using these techniques showed average efficiency with QAM waveforms that is well under 20%.

In this chapter, we present a SiGe BiCMOS outphasing power amplifier (OPA) with substantially better performance due to an extremely low-loss power combiner that realizes both excellent peak power-added-efficiency (PAE) of 41% and average PAE of 25.3% for an 8.1dB-PAPR signal at 28GHz. The power combiner is based on a compact triaxial balun structure that simultaneously generates the Chireix compensating reactances at the output ports of the PAs for load modulation and combines the RF power with low loss.

In the conventional Chireix OPA, as discussed in the previous chapter, the PAs drive the combiner with constant-envelope signals separated by an outphasing angle ($\pm\varphi$). The load seen by each PA is modulated through a non-isolating power combiner, along with the opposite-signed Chireix reactances ($\pm jX_{CH}$) at each of the combiner ports. Previous work investigated the Chireix OPA in mm-wave bands with limited success to realize high average efficiency [6]. Two significant challenges exist for CMOS/BiCMOS PAs in mm-wave bands. First, high losses in the on-chip power combiners significantly reduce the gain, output power, and any theoretical average efficiency improvement. Second, the typical OPA requires a voltage-mode PA that is difficult to realize at mm-wave frequencies due to the relative admittance presented by device parasitics.

3.2 Triaxial Balun as the Chireix Combiner

The triaxial balun is conceptually illustrated in Fig. 3.1.

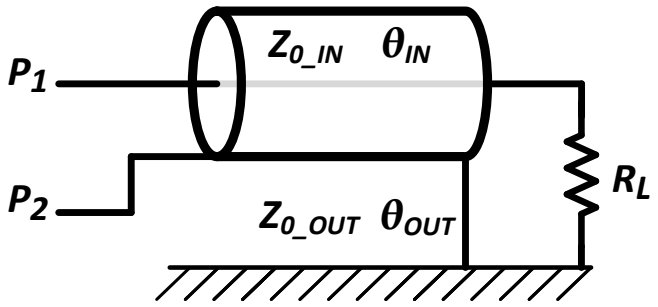


Figure 3.1: Triaxial (or coaxial) balun.

This passive structure, originally known as the coaxial balun, consists of two conductors connected to the input ports (P_1 and P_2) and a ground plane that serves as a return path for the load current. In our design, since we explicitly implement the ground plane with a third conductor, we refer to the structure as the triaxial balun. There are two transmission lines in this balun, one formed between the conductors of P_1 and P_2 with the characteristics of Z_{0_IN} and θ_{IN}, and the other one formed between the conductor of P_2 and the ground plane with the characteristics of Z_{0_OUT} and θ_{OUT}, although the conductor connected to P_1 is shielded from the ground plane and there is no transmission line formed between them. Figure 3.2a shows the proposed equivalent RF model of the triaxial balun.

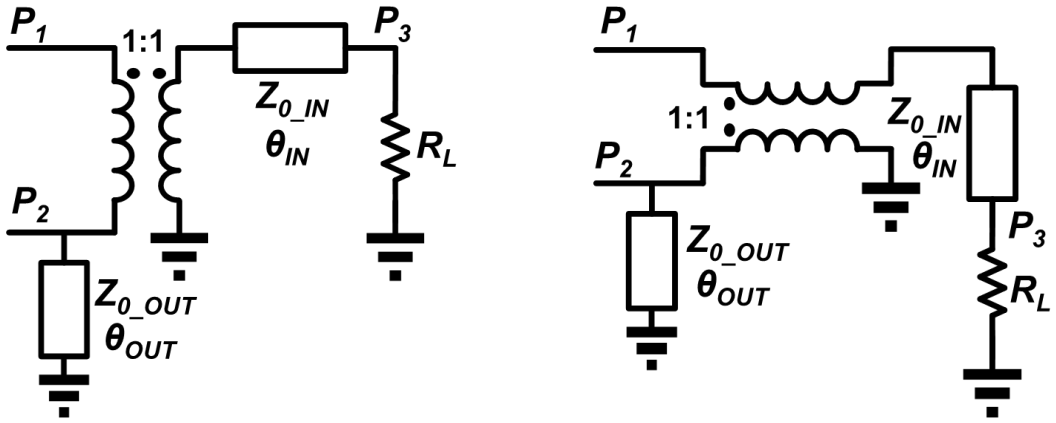


Figure 3.2: (a) Equivalent RF model of the triaxial balun, (b) equivalent RF and DC model of the triaxial balun.

This model captures the RF behavior precisely, but slight adjustments are needed to capture the DC behavior. Alternately, the model shown in Fig 3.2b captures both the DC and RF behaviors; for simplicity however we continue to use the first model throughout this chapter.

In a standard application [7] the inner transmission line needs to provide matching to the load impedance ($Z_{0\_IN} = R_L$), while the outer transmission line, which appears as a shorted stub on P_2, needs to provide a high impedance in order to not create imbalance between the ports. Therefore, the length of the balun should be $\lambda/4$, so that the outer shorted stub provides an open. In our application the situation is different, we inherently need the imbalance in order to make a Chireix combiner, thus the balun can be shorter than $\lambda/4$.

The proposed OPA is shown in Fig. 3.3.

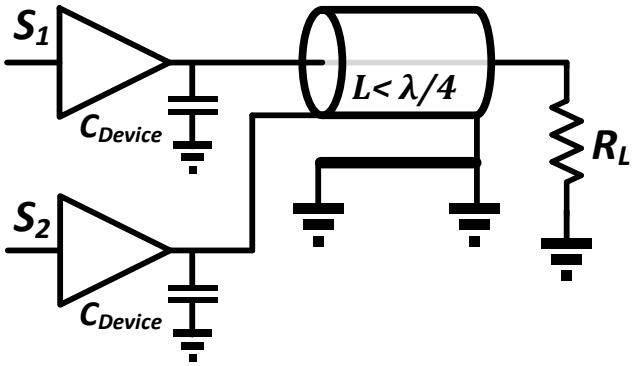


Figure 3.3: Proposed triaxial balun outphasing PA.

It replaces the conventional Chireix combiner with a triaxial balun that combines the outputs of the two PAs while inherently producing the compensating reactances and providing impedance match to the load with low loss. The impedances produced by the triaxial balun can be related to the design of the Chireix outphasing scheme as shown in Fig. 3.4.

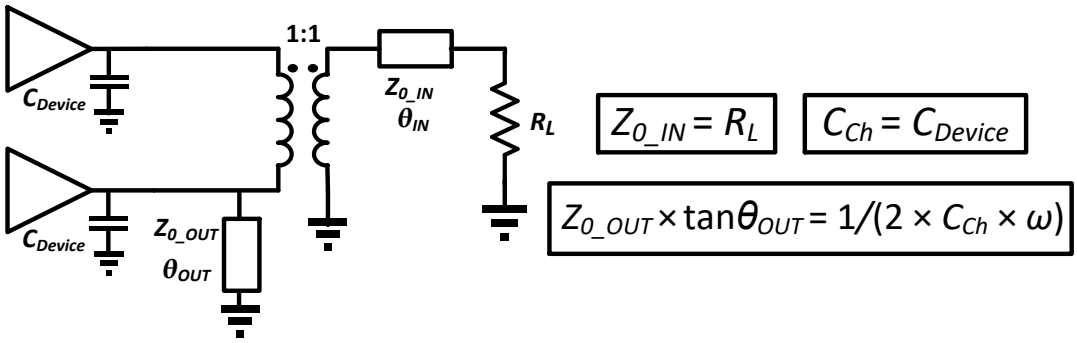


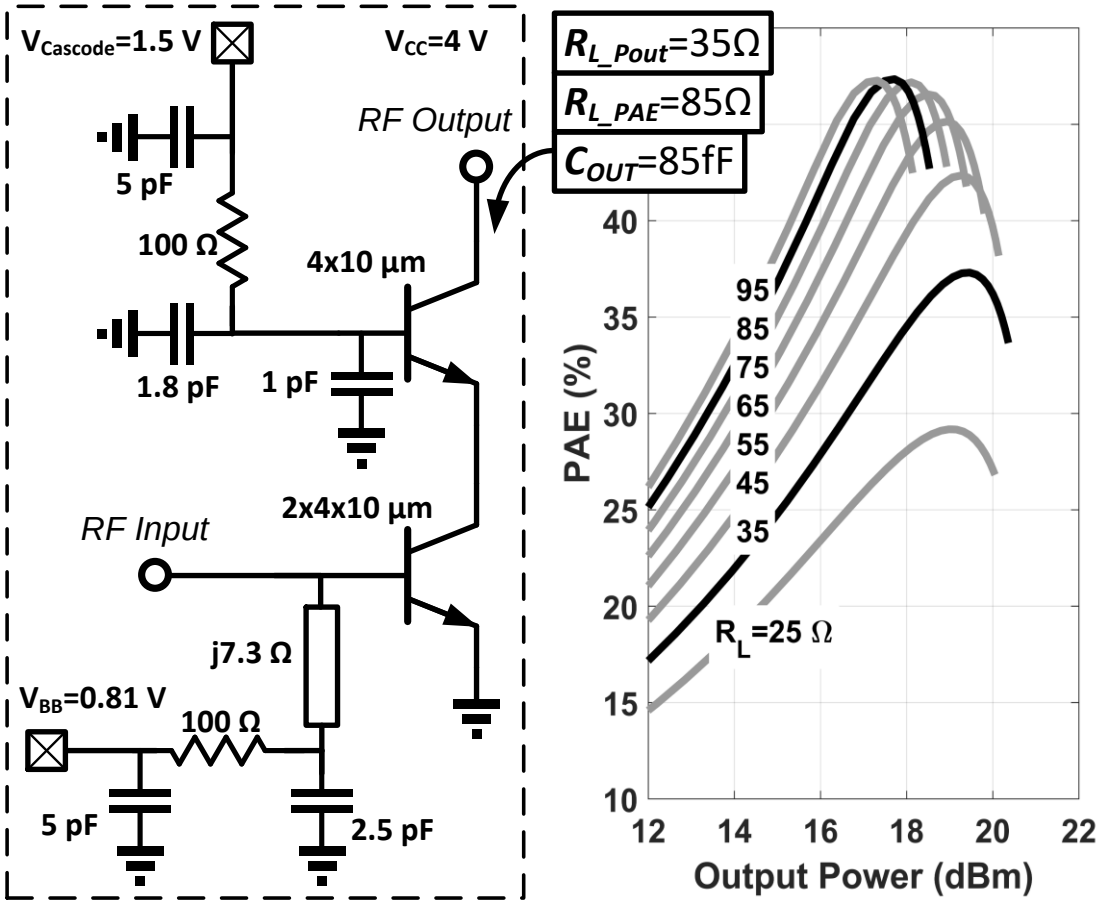
Figure 3.4: The equivalent model and design criteria for the proposed outphasing PA shown in Fig. 3.3.

The PA cell's output capacitance (C_{Device}) is absorbed into the Chireix network while the length of the balun is chosen to produce the desired shunt inductance on one of the PA

outputs. Thus, a relatively short length, e.g. $l \approx \lambda/15$, transmission line is required for the outphasing combiner, resulting in low loss.

3.3 Design and Implementation

The PA cell is illustrated in Fig. 3.5a based on a 0.13µm SiGe HBT cascode where the output capacitance is roughly 85fF.



(a) (b)

Figure 3.5: (a) Schematic of the HBT PA cell, and (b) post-layout simulation of PAE for R_L sweep.

The cascode base is biased with low impedance to sweep out the carriers generated from impact ionization, thereby improving the breakdown for increased output power. The transistor emitter lengths are sized to create a loadline impedance that optimizes the efficiency and output power over the range of impedances seen by the triaxial balun (Fig. 3.5b). The PA cell produces 20.5dBm and a maximum PAE of 47% based on post-layout simulation.

In Fig. 3.6, the triaxial balun, as implemented in a planar integrated circuit process, is shown.

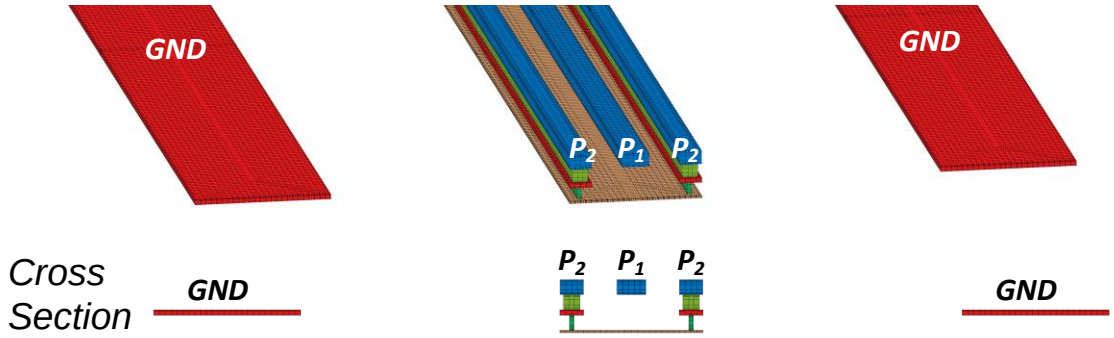
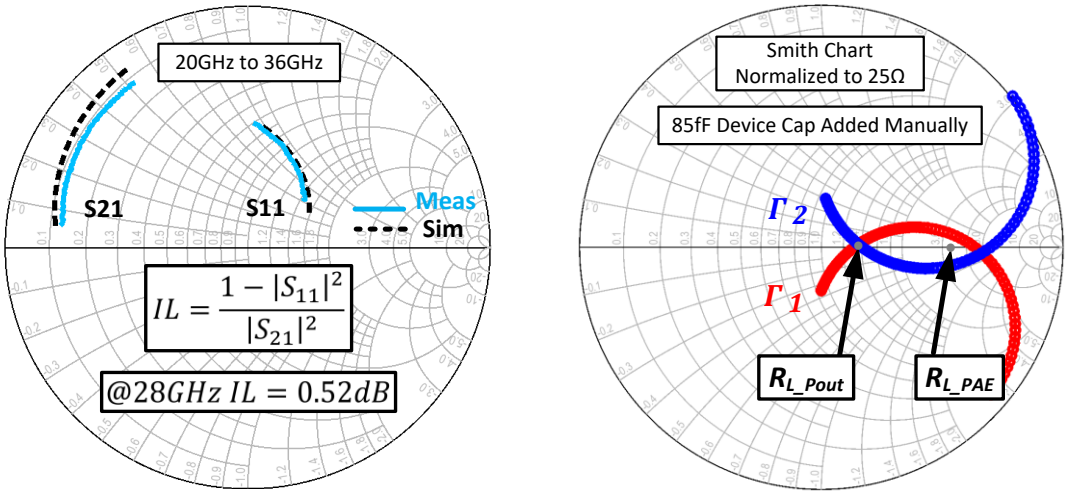


Figure 3.6: The implemented triaxial balun in a SiGe IC process.

P_1 is the central conductor while P_2 is the shield around P_1 to form a microstrip structure, and the return path is through the ground conductor on either side of P_2. A fabricated back-to-back test structure indicates that the measured insertion loss of the combiner is 0.52dB and is close to the simulated value of 0.35dB around 28GHz (Fig 3.7a).



(a) (b)

Figure 3.7: (a) Measured and simulated S-parameters of the fabricated back-to-back balun, and (b) simulation of the resulting load modulation on the PA cells.

Furthermore, Fig. 3.7b shows the impedances seen at P_1 and P_2 as a function of outphasing angle, which matches the canonical outphasing load modulation. The loads corresponding to the PA cell's peak output power and efficiency, denoted R_{L_Pout} and R_{L_PAE}, are traversed by the outphasing impedance trajectories.

Each PA cell has a DC voltage supply provided through the triaxial balun. The cell connected to P_2 is fed directly from the alternate end of the conductor with AC short provided by local bypass capacitors (not shown in the schematic). The cell connected to P_1 can be fed via a DC-feed inductor at any point along the inner conductor. In this work, a wirebond connecting one of the DC pads to the output RF pad provides this inductor. The die micrograph is shown in Fig. 3.8. The PA area, including pads and input routing, is 700um x 800um and the chip operates from a 4V supply.

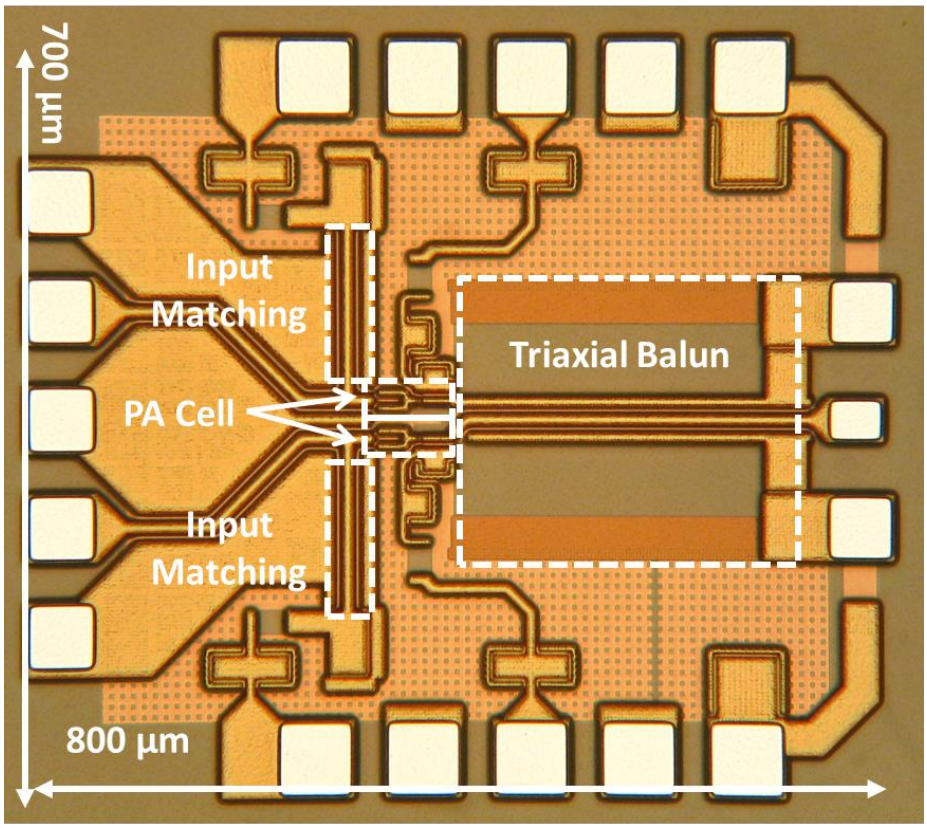


Figure 3.8: Die photo.

3.4 Test Results

While the PA cells present a large output impedance to the combiner compared to the canonical voltage source in a general outphasing approach, the amplitude and phase difference of the input signals (S_1 and S_2) are modified (as described in Chapter 2) to maintain high efficiency over a range of output powers. The input signals for testing are equi-amplitude with opposite phase. An initial sweep is performed to determine the optimal amplitude and phase for maximum efficiency.

The simulated and measured gain, collector efficiency (η), and PAE are plotted in Fig. 3.9.

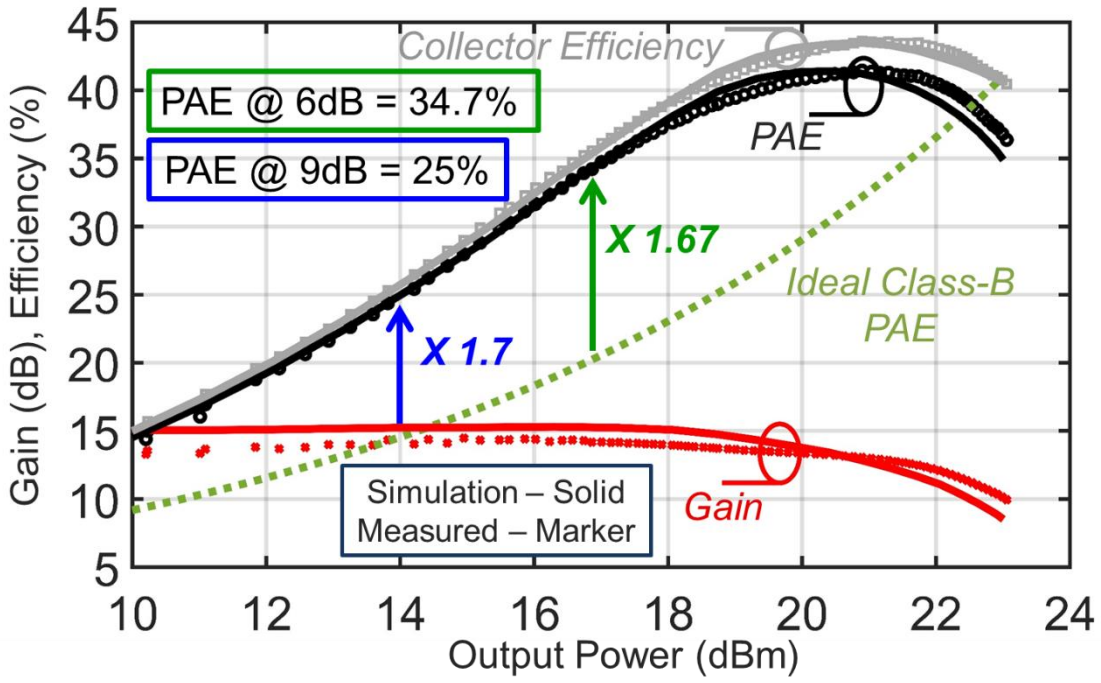


Figure 3.9: CW performance measured at 28GHz. At 6-dB and 9-dB power backoff the PAE is improved by 1.67 and 1.7 times respectively, compared to an ideal class-B PAE.

The measured small-signal gain is 14dB. The peak output power is 23dBm with corresponding PAE of 35.5%. The peak PAE of 41% is reached at 21dBm while the collector efficiency reaches 44%. The PAE measured at 6-dB backoff relative to the maximum power of 23dBm is 34.7%. Additionally, corroboration between simulation and measurement is excellent over the entire range of output power.

The OPA was tested with an 80MHz 64-QAM OFDM signal with PAPR of 8.1dB at 28 GHz as shown in Fig. 3.10.

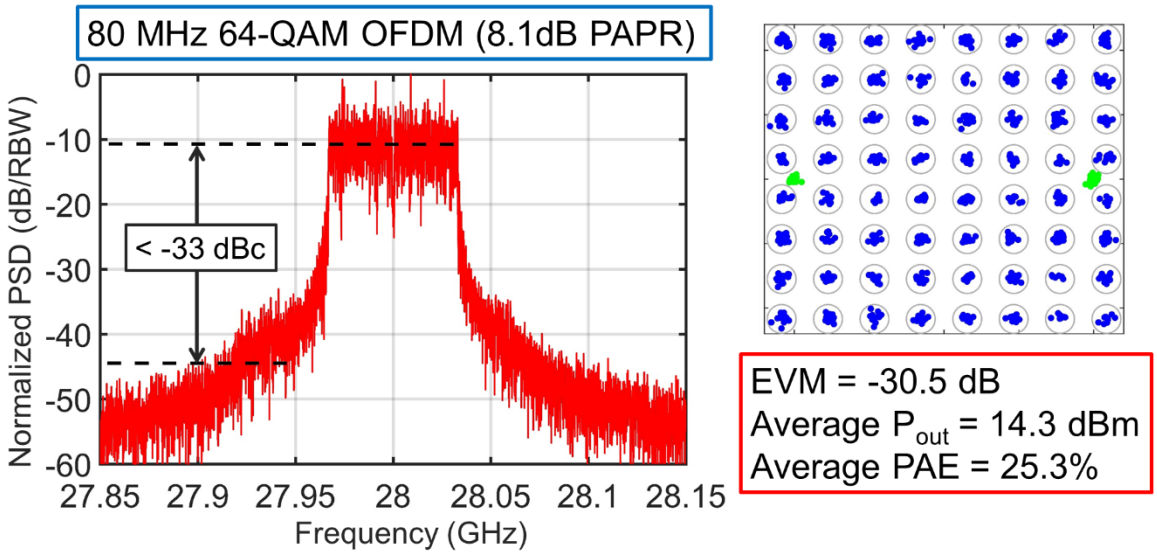


Figure 3.10: Modulated signal performance of the PA for an 80MHz 64-QAM OFDM signal with 8.1dB PAPR centered at 28GHz.

Equalization is applied to the entire test setup including the PA. The average output power with modulation is 14.3dBm and the RMS EVM of 3% is achieved with the use of a memoryless DPD algorithm. The average PAE for the OFDM signal is 25.3%. The adjacent-channel power leakage, also shown in Fig. 3.10, indicates that the relative power 60MHz away from the band edge is less than -33dBc.

3.5 Conclusion

Table 3.1 compares the proposed OPA with state-of-the-art PA performance at 28GHz.

Table 3.1: Comparison to state of the art.

	This work	[4] ISSCC'16	[1] ISSCC'17	[3] ISSCC'17
Frequency (GHz)	28	30	27	28
Technology	130nm SiGe	28nm CMOS	40nm CMOS	130nm SiGe
P_{SAT}(dBm)	**23**	15.3	15.1	16.8
Peak PAE (%)	**41.4**	36.6	33.7	20.3
PAE @ 6dB from P_{SAT}	**34.7**	NA	15.1	13.9
Modulation Type	64-QAM OFDM	64-QAM OFDM	64-QAM OFDM	64-QAM Single Carrier
Signal BW (MHz)	80	250	800	500 / 1000
Pre-distortion	Mem-less DPD	No	No	No
Average Pout (dBm)	**14 .3**	5.3	6.7	9.2 / 7.2
EVM (dB)	-30.5	-25	-25	-27 / -26.6
Average PAE (%)	**25.3**	9.6	11	18.5* / 14.4*

* Collector Efficiency

This work achieves high output power, peak efficiency, and most notably, the highest 6-dB power backoff PAE at 34.7% compared to prior work. Furthermore, the modulation measurement demonstrates that the PA can achieve excellent EVM at a high average output power with the assistance of memoryless DPD. Additionally, the average PAE for the QAM OFDM waveform is the highest average efficiency for any silicon-based mm-wave PA and demonstrates the potential for fully integrated PAs that can efficiently support high-PAPR waveforms at 28GHz.

Acknowledgement

This chapter is mostly a reprint of the material as it appears in IEEE International Solid-State Circuits Conference Digest of Technical Papers, 2018, Rabet, Bagher;

Buckwalter, James. The dissertation author was the primary investigator and author of this material.

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Chapter 4

The Single-Input Linear Chireix (SILC) Power Amplifier

4.1 Introduction

As discussed in the previous chapters, the low distortion levels required for spectrally efficient complex modern communication signals with high peak-to-average power ratio (PAPR) put strict requirements on the linearity of wireless transmitters. Average efficiency, mostly determined by the PA performance at peak and backoff power levels, is another significant criterion, particularly for battery powered devices. For emerging 5G applications employing mm-wave phased-arrays with multiple PA units on the same die, the importance of linearity and efficiency escalate further, since implementing individual digital predistortion (DPD) for each unit is not practical and heating of the PAs, densely placed next to each other, can be a problem. Therefore, the PA units must be inherently linear and efficient.

Chireix outphasing [1] and Doherty [2], the two popular active load modulation techniques used at RF frequencies for PA efficiency enhancement, are currently being

investigated for mm-wave applications. Both methods, in their original forms, utilize two PA cells connected to a non-isolating three port passive network, which serves as a power combiner and provides the desired load modulation during operation.

In theory, outphasing offers a better efficiency profile than Doherty [3], and in practice there are a variety of creative ways to implement the Chireix combiner with low loss (e.g., two-element L-C [4], offset transmission lines [5], on-antenna outphasing [6]-[7], and triaxial balun [8]). Also, in contrast to most Doherty implementations, the PA cells in outphasing have the same size, are biased similarly, and see the same magnitude of fundamental load modulation. These features make the dual-input implementations of outphasing [8] more advantageous than the dual-input implementations of Doherty (with analog [9]-[10] or digitally assisted mixed- signal [11] PAs) in that the two inputs for outphasing are symmetric (they have the same amplitude with opposite phases, i.e., complex conjugate in base-band signal domain).

On the other hand, a major advantage of the Doherty architecture, which has historically made it a more common choice than outphasing, is the simplicity of implementing its input signal splitter that feeds the two PA cells from a single RF input source, without the need for an extra IQ modulator and the bandwidth expansion problem associated with dual-input realizations.

In recent years, there have been successful proposals for novel architectures within the Doherty-outphasing continuum, in order to garner the best advantages of both methods in one circuit [12]-[13]. The primary emphasis in these works has been placed on efficiency improvement for single RF input amplifiers, leaving the linearity to be addressed with DPD. This chapter presents a method that not only improves backoff efficiency while requiring a

single RF input, but also corrects the nonlinearity of the PA cells, eliminating the need for predistortion. It relies on use of the Chireix combiner and is termed here the Single Input Linear Chireix (SILC) PA. In the following, the design principles of the SILC PA are first discussed, and an experimental implementation with SiGe HBTs is then described. Measurement results with a 64-QAM OFDM signal appropriate for 5G applications are reported, showing an average output power of 11.9dBm and PAE>20%, which to the authors' best knowledge is among the highest PAE reported to date for an OFDM signal without DPD (or other forms of digital enhancement) at power levels of interest for 5G transmitters.

4.2 Proposed Architecture

4.2.1 Schematic

Figure 4.1 shows the proposed topology that consists of a standard Chireix PA with Doherty-like biases, and a simple input network providing a constant phase shift (θ_0) to the main path.

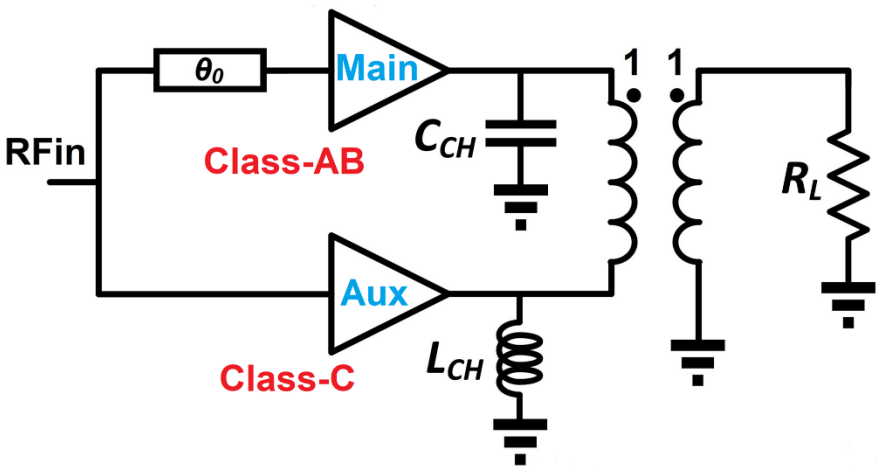


Figure 4.1: Proposed PA architecture with the main and auxiliary PA cells biased in class-AB and Class-C respectively.

Depending on the type of the Chireix combiner and characteristics of the PA cells, the delay line can be placed at the input of either amplifier for proper operation. Here, the unit PA cells are regarded as current sources, and the shunt compensating elements with susceptances of $\pm B_{CH}$ (C_{CH} and L_{CH}) are chosen in accordance with outphasing principles [14]. Analysis of the circuit is carried out by splitting the operation into low power and high power regions.

4.2.2 Operation at Low Power Region

At low input power levels, the auxiliary amplifier is off, and the main amplifier works as a standalone class-AB PA. The equivalent circuit for this mode of operation is depicted in Fig. 4.2a.

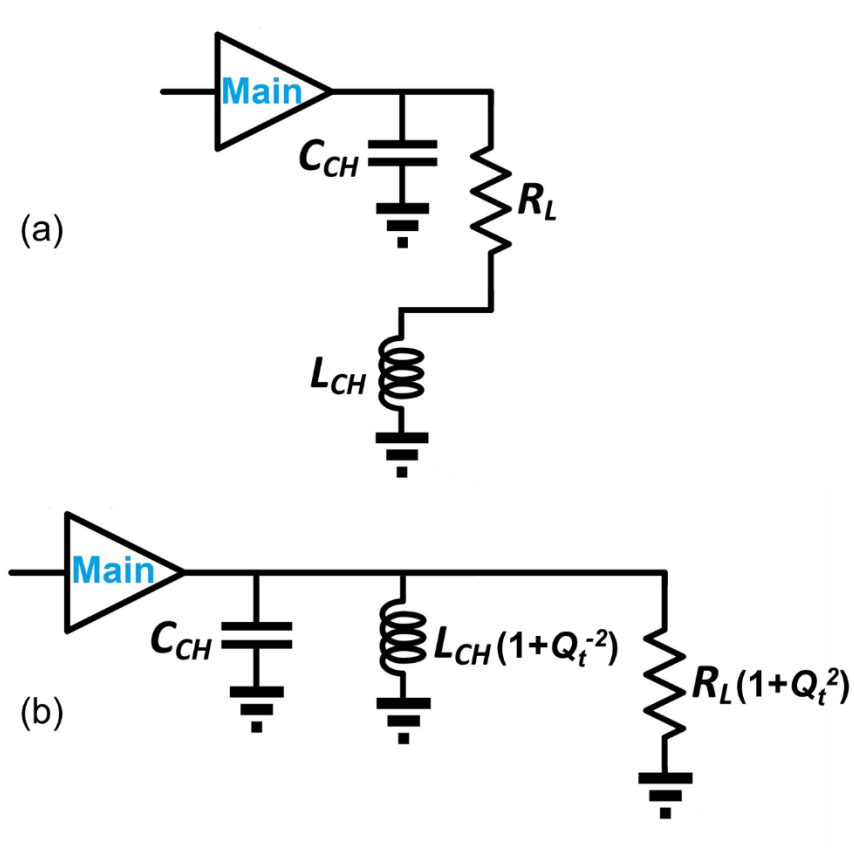


Figure 4.2: Equivalent circuit at low power when the auxiliary amplifier is off: (a) R_L moved to the primary side of the transformer and (b) series to parallel impedance transformation applied.

The load impedance seen by the main PA at low power (Z_A) can be calculated by performing a series-to-parallel impedance transformation, as shown in Fig. 4.2b. The quality factor of this transformation (Q_t) is equal to inverse of $B_{CH}R_L$, which is a design parameter for Chireix combiners determining the back-off efficiency profile of the outphasing PAs. For example, $B_{CH}R_L$ equal to 0.6 and 0.86 result in backoff peak efficiency points at 10dB and 6dB respectively, therefore Q_t is typically a value in the 1.16-1.66 range. Additionally, C_{CH} is tuned out, although not completely, by the resulting parallel inductance, keeping the reactive part of the load impedance low for high efficiency. The residual capacitance, $C_{CH}/(1+Q_t^2)$,

causes modest efficiency and gain reduction due to a non-unity power factor (PF_A) ranging between 0.75 and 0.85. Equation 4.1 shows the relation between the PF_A and Q_t.

$$PF_A = \frac{Real\{Y_A\}}{|Y_A|} = \frac{\frac{1}{R_L(1+Q_t^2)}}{\sqrt{\left(\frac{1}{R_L(1+Q_t^2)}\right)^2 + \left(\frac{B_{CH}}{1+Q_t^2}\right)^2}} = \frac{Q_t}{\sqrt{1+Q_t^2}} \tag{4.1}$$

One can design a modified Chireix combiner to avoid any excess reactance [13]; however, the degraded symmetry of the circuit is not desirable for the high power mode of operation described in the next sub-section.

The PA should be designed such that the auxiliary amplifier remains off up to the input power where the main amplifier starts saturating and exhibits nonlinear behaviors including gain compression and AM-PM distortion. In principle, the efficiency should reach its maximum class-AB value scaled by PF_A (0.75 - 0.85), and the gain should be lower than the class-AB gain by $PF_A/2$ (3.7 - 4.25dB). The extra 1/2 for the gain ratio is due to the fact that in this mode of operation the input power going to the auxiliary amplifier is wasted.

4.2.3 Operation at High Power Region

As the auxiliary amplifier turns on and begins providing power, a variety of mechanisms influence the output, of which some are due to the topology itself (i.e., load modulation, systematic AM-AM and AM-PM variations), some are due to the device non-idealities (i.e., gain compression and AM-PM distortion), and some result from combination of both topology and device non-idealities (i.e., self-outphasing), as discussed below.

The end point of this region, where the PA provides its highest output power, is considered first. Both amplifiers work with their full power at this point, with a constant phase shift (θ) between them, resulting from the delay line at the input network (θ_0), as well as phase imbalance (θ_1) coming from the non-equal input impedances of the PA cells due to their bias difference ($\theta = \theta_0 + \theta_1$). If a standard combiner is used, this operation point can be designed to lie in a high-efficiency area (PF=1) of the impedance trajectories provided by the Chireix method [5] shown in the Smith chart of Fig. 4.3.

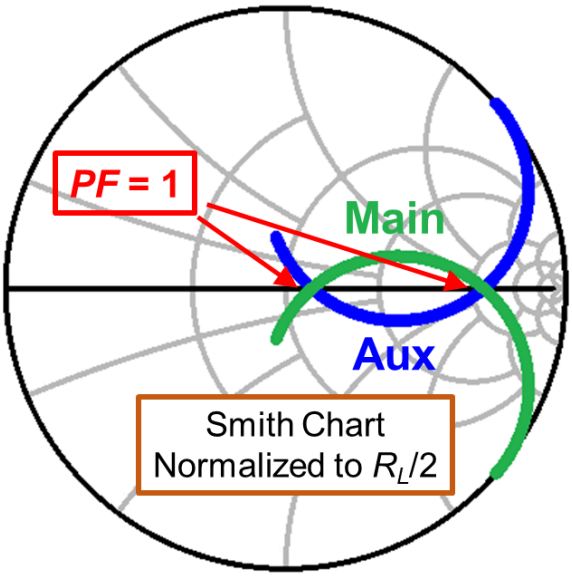


Figure 4.3: Impedance trajectories provided by the Chireix combiner in standard outphasing operation. The high-efficiency points with unity *PF* are marked.

There are two candidates for this point, one close to the center of the Smith chart with a lower impedance value associated with higher output power, and the other one at "outphasing backoff", providing higher load impedance appropriate for low power operation. The design parameter that determines the impedance of choice is the phase shift θ between the two amplifiers.

Note that for standard outphasing operation, equal fundamental voltage amplitudes are required at the ports of the Chireix combiner. This approach is also followed here at full power; since the auxiliary amplifier is biased in class-C and has lower gain, it is set to have a higher supply voltage than the main amplifier in order to match the voltage swings at maximum power.

To further investigate the different possible design approaches, simulations with an idealized transistor model (nonlinear voltage-controlled current source (VCCS) that includes a knee voltage contribution, described in Appendix I) and an ideal balun have been done. Figure 4.4a shows the impedance trajectories seen by the main and auxiliary amplifiers for an example design, where the end point impedance at maximum power is chosen to be the lower value of the two options mentioned above.

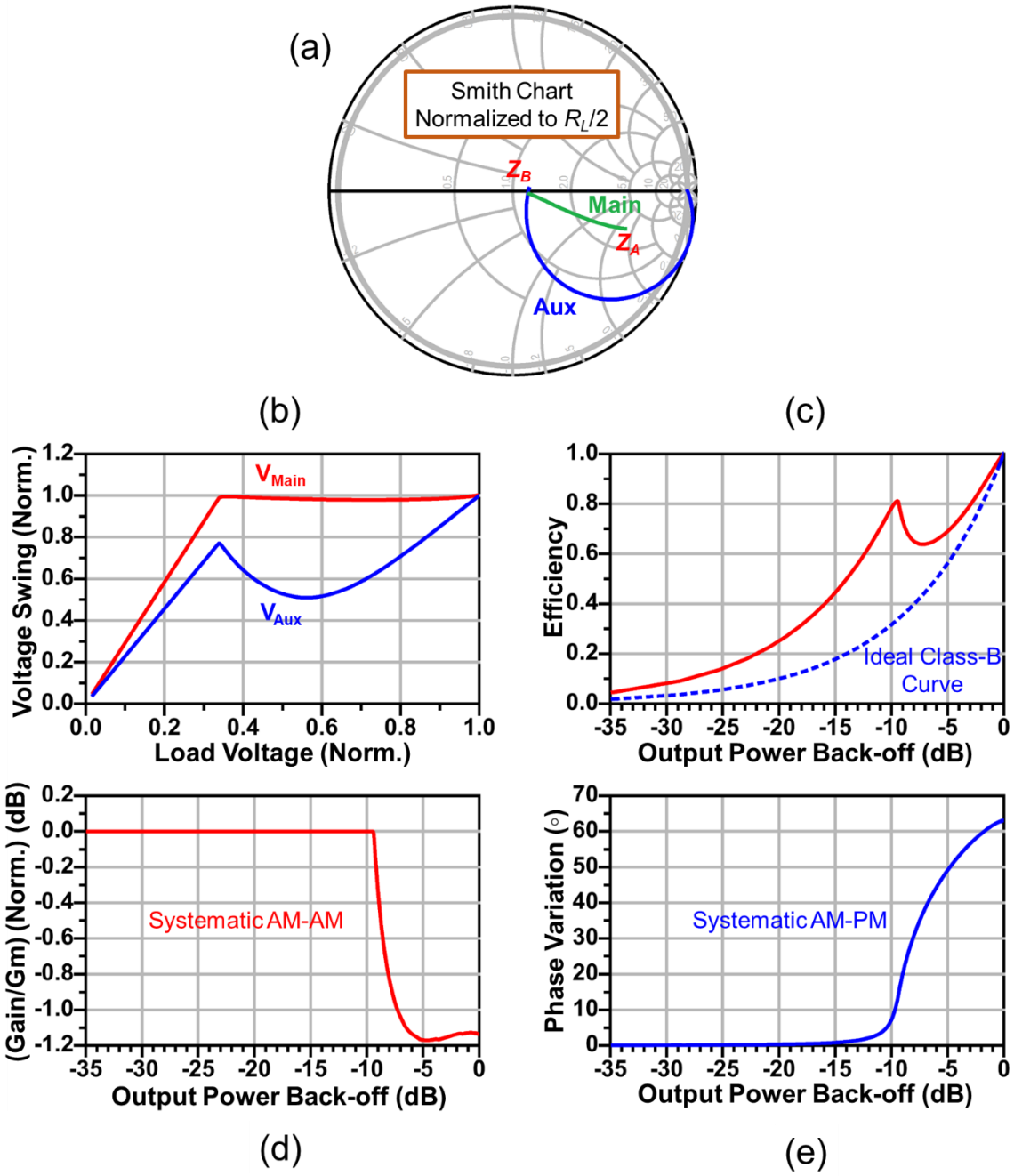


Figure 4.4: Simulation of an example design with a low, purely resistive impedance at peak power, using the idealized transistor model (nonlinear VCCS with knee voltage): (a) impedance trajectories seen by the amplifiers, (b) output voltage magnitudes of the amplifiers normalized to the main supply voltage, (c) normalized overall efficiency, (d) systematic AM-AM, and (e) systematic AM-PM.

With $B_{CH}R_L$ of 0.8 (Q_t =1.25), the fixed phase shift between the amplifiers is calculated accordingly based on the standard Chireix equations [5] ($\theta = \sin^{-1} B_{CH}R_L = \sin^{-1} Q_t^{-1} = 126.9°$). Theory predicts that the trajectory of impedance seen by the main amplifier starts at

$$Z_A = [R_L(1+Q_t^2)] \,||\, \left[\frac{1+Q_t^2}{jB_{CH}}\right] = R_L(Q_t^2 - jQ_t^2) \tag{4.2}$$

and ends at

$$Z_B = R_L Q_t^2 \left(1 - \sqrt{1-Q_t^2}\right) = \frac{R_L}{2\cos^2\frac{\theta}{2}} \quad . \tag{4.3}$$

These values are supported by the simulation results shown in Fig. 4.4a. The output power variation due to load modulation (LMR) for the main amplifier is

$$LMR_{Main} = \frac{Real\left\{\frac{1}{Z_B}\right\}}{Real\left\{\frac{1}{Z_A}\right\}} = (1+Q_t^2)\left(1+\sqrt{1-Q_t^{-2}}\right) \tag{4.4}$$

which corresponds to 4.1 (6.1dB) in this design. For the overall output power, the contribution of the auxiliary amplifier is then taken into account, by doubling the value for the main amplifier (adding 3dB), since at the maximum power both amplifiers see the same impedance (Fig. 4.4a) and have the same output voltage swing (Fig. 4.4b). The back-off peak efficiency is therefore expected to be at a power level 9.1dB below the maximum power with a value reduced by PF_A (0.78) relative to the peak efficiency. These numbers are in good agreement with the simulations shown in Fig. 4.4c. The slight difference between the theory and simulation is due to the presence of knee voltage and saturation of the PA cells. Note that in Fig. 4.4a, the impedance seen by the auxiliary amplifier goes outside of the smith chart for a small region at the beginning of its operation. This condition is not an indicator of instability;

it only shows that a small portion of the power generated by the main amplifier is consumed by the auxiliary amplifier.

These results are favorable in terms of efficiency, but the linearity aspects of the PA need to be addressed as well in order to achieve a design that does not require DPD. The goal is to have systematic AM-AM and AM-PM changes that are in the opposite direction of the gain compression and AM-PM variation caused by the device non-idealities, so that the overall response is distortion free. For an overdriven amplifier, the gain compression characteristics and resultant AM-AM distortion are in general dependent on the choice of power transistor (SiGe HBT, CMOS, LDMOS, pHEMT) and bias conditions. The corresponding AM-PM distortion, associated with the change of device input and output capacitance as well as the impedance matchings, is often a critical determinant of the overall amplifier linearity in this regime.

4.2.4 Systematic AM-AM and AM-PM Variations

The net amount of systematic AM-AM results from two features. The first one is the $PF_A/2$ ratio that was mentioned above. In contrast to the low power mode of operation, at high power the power factor rises to unity and the input power going to the auxiliary amplifier is not wasted, therefore the gain increases by $2/PF_A$. The second feature is that the load modulation decreases the gain, if the gm is considered to be constant for the PA cells. This gain variation is captured by looking at the change in the magnitude of impedance seen by the main amplifier ($|Z_A|/|Z_B|$), thus the overall systematic AM-AM can be calculated as shown below.

$$Systematic\ AM-AM = \frac{2}{PF_A} \times \frac{|Z_B|}{|Z_A|} = 2 \times \left(1 - \sqrt{1 - Q_t^{-2}}\right) = 4\sin^2\frac{\theta}{2} \qquad (4.5)$$

Equation 4.5 in this example, results in ~ -1dB, meaning that for a design with low value impedance at peak power, the systematic AM-AM aggravates the device gain compression problem rather than fixing it. In order to capture the systematic AM-AM in simulation, the variation of large signal transconductance (Gm) is de-embedded from overall gain variation, as shown in Fig. 4.4d.

Next, the systematic AM-PM and the mechanism that causes it are described by looking at the combiner port voltages. Figure 4.5 shows a simplified phasor diagram illustrating the output voltages of the main (V_{Main}) and auxiliary (V_{Aux}) amplifiers as well as the load voltage (V_{Out}).

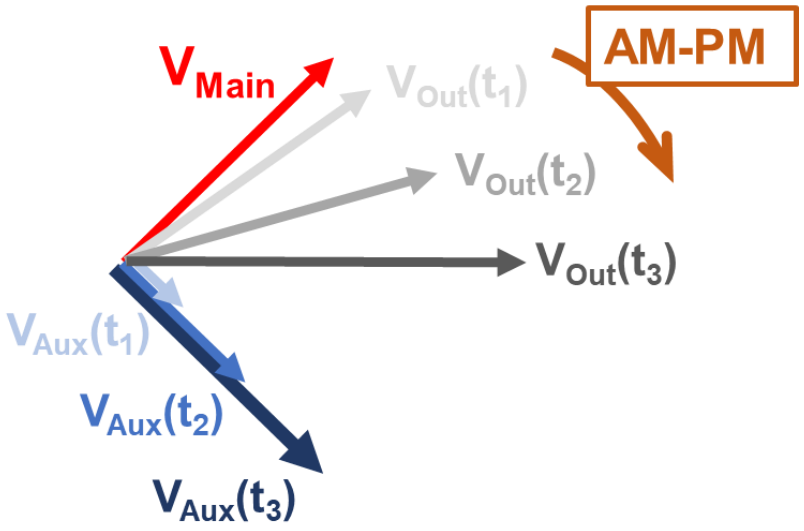


Figure 4.5: Simplified phasor diagram describing the systematic AM-PM of the load voltage in the high power mode of operation.

A vector sum (instead of subtraction) is depicted here for the sake of convenience, even though the actual combiner is differential. We use the simplifying assumptions that V_{Main} and

the phase difference between the two vectors (θ) stay constant in this region. As V_{Aux} increases, the magnitude and phase of V_{Out} vary simultaneously, and it is clear from the figure that the overall amount of this systematic AM-PM is equal to half of θ, because eventually V_{Aux} approaches the same magnitude as V_{Main}. In practice, the assumptions made here are not accurate, because the main and auxiliary amplifiers see reactive loads in the middle points (Fig. 4.4a). However, since at the end point both of them see a purely resistive impedance, the overall systematic AM-PM change captured by this analysis, as given by Eq. 4.6, remains a very good approximation. A more detailed calculation, that takes into account the differential nature of the combiner and the effects of C_{CH} and L_{CH}, is presented in Appendix II.

$$Systematic\ AM-PM \cong \frac{total\ input\ phase\ shift\ (\theta)}{2} = \frac{\sin^{-1} Q_t^{-1}}{2} \qquad (4.6)$$

The simulation result shown in Fig. 4.4e verifies this analytical approach. The AM-PM obtained in this example is not particularly favorable for an overall linear amplifier, because the relatively large amount (~50 degrees over a 5dB power variation and ~63 degrees in total) is significantly greater than typical device-related phase distortions.

In this example design, it was seen that a remarkable backoff efficiency profile is achievable with a simple outphasing PA topology that has an asymmetric bias and a constant phase shift between the two input RF signals feeding the PA cells. The phase shift was chosen such that the load impedance at maximum power was relatively low, and therefore the efficiency had a second peak at a deep backoff, but the linearity in terms of AM-AM and AM-PM was not good. As a result, this design can be a strong candidate for applications where predistortion is available. Modifications are needed, however, for applications where inherent linearity is required.

A similar design is now examined that at peak power has the higher impedance with unity power factor

$$Z_B = R_L Q_t^2 \left(1 + \sqrt{1 - Q_t^{-2}}\right) = \frac{R_L}{2\sin^2\frac{\theta}{2}} \tag{4.7}$$

achieved by changing the input phase shift to the other answer of the trigonometric equation $\theta = \sin^{-1} Q_t^{-1}$, which is 53.12° (for $B_{CH}R_L = 0.8$). The simulation results, obtained by using the same transistor model, are shown in Fig. 4.6.

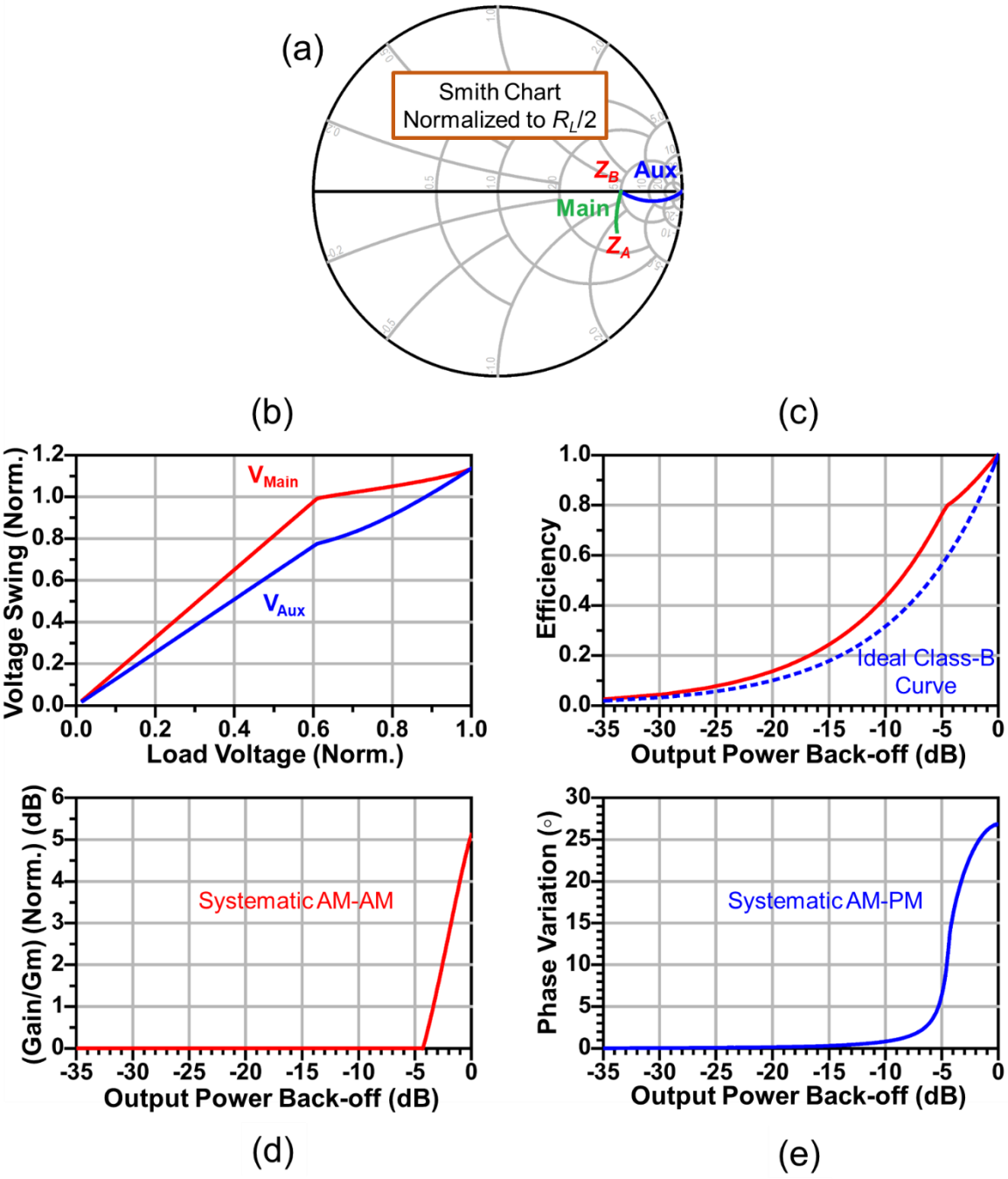


Figure 4.6: Simulation of an example design with a high, purely resistive impedance at peak power, using the idealized transistor model (nonlinear VCCS with knee voltage): (a) impedance trajectories seen by the amplifiers, (b) output voltage magnitudes of the amplifiers normalized to the main supply voltage, (c) normalized overall efficiency, (d) systematic AM-AM, and (e) systematic AM-PM.

Compared to the previous example, here the amount of load modulation for the main amplifier is minor (Fig. 4.6a) and

$$LMR_{Main} = \frac{Real\left\{\frac{1}{Z_B}\right\}}{Real\left\{\frac{1}{Z_A}\right\}} = (1 + Q_t^2)\left(1 - \sqrt{1 - Q_t^{-2}}\right) \tag{4.8}$$

is only 0.11dB. Also, the output voltage of the main amplifier continues to increase (deep saturation) even after the auxiliary amplifier turns on (Fig. 4.6b). The efficiency profile, shown in Fig. 4.6c is not as good as the previous example, but it is still better than an ideal class-B and has a back-off peak at ~4.4dB, with a value that is lower than the peak efficiency by PF_A (0.78) as found for the previous case. Note that if the efficiency curve was plotted vs absolute power (rather than normalized power), the backoff efficiency peak would be at the exact same output power in both example designs, but the peak power would be different. The systematic AM-AM expression needs to be modified too, since Z_B has increased. The new expression is

$$Systematic\ AM - AM = \frac{2}{PF_A} \times \frac{|Z_B|}{|Z_A|} = 2 \times \left(1 + \sqrt{1 - Q_t^{-2}}\right) = 4\cos^2\frac{\theta}{2} \tag{4.9}$$

that results in ~5dB (Fig. 4.6d), which can compensate the device related gain compression coming from the considerable amount of effective Gm reduction due to the deep saturation experienced by the main amplifier. (As it will be discussed later, the deep saturation of the main amplifier can be avoided in a practical design by adjusting the bias condition of the auxiliary amplifier.) The equation for the systematic AM-PM is same as Eq. 4.6 and results in ~ 26.6°. The simulation result shown in Fig. 4.6e is in good agreement with the calculation.

It is also possible to have an intermediate design between the two previous examples. As shown in Fig. 4.3, if a phase shift other than the two values suggested by $\theta = \sin^{-1} Q_t^{-1}$ is

applied to the input signals, the peak power impedances seen by the main and auxiliary amplifiers will be complex conjugates of each other and not purely resistive (Z_B and Z_B^*). As a result, the peak efficiency will drop slightly due to the non-unity power factor of Z_B (PF_B), but other than that the PA will work in a manner similar to the previous examples. Fig. 4.7 shows the simulation results for a case with phase shift of 90° applied at the input.

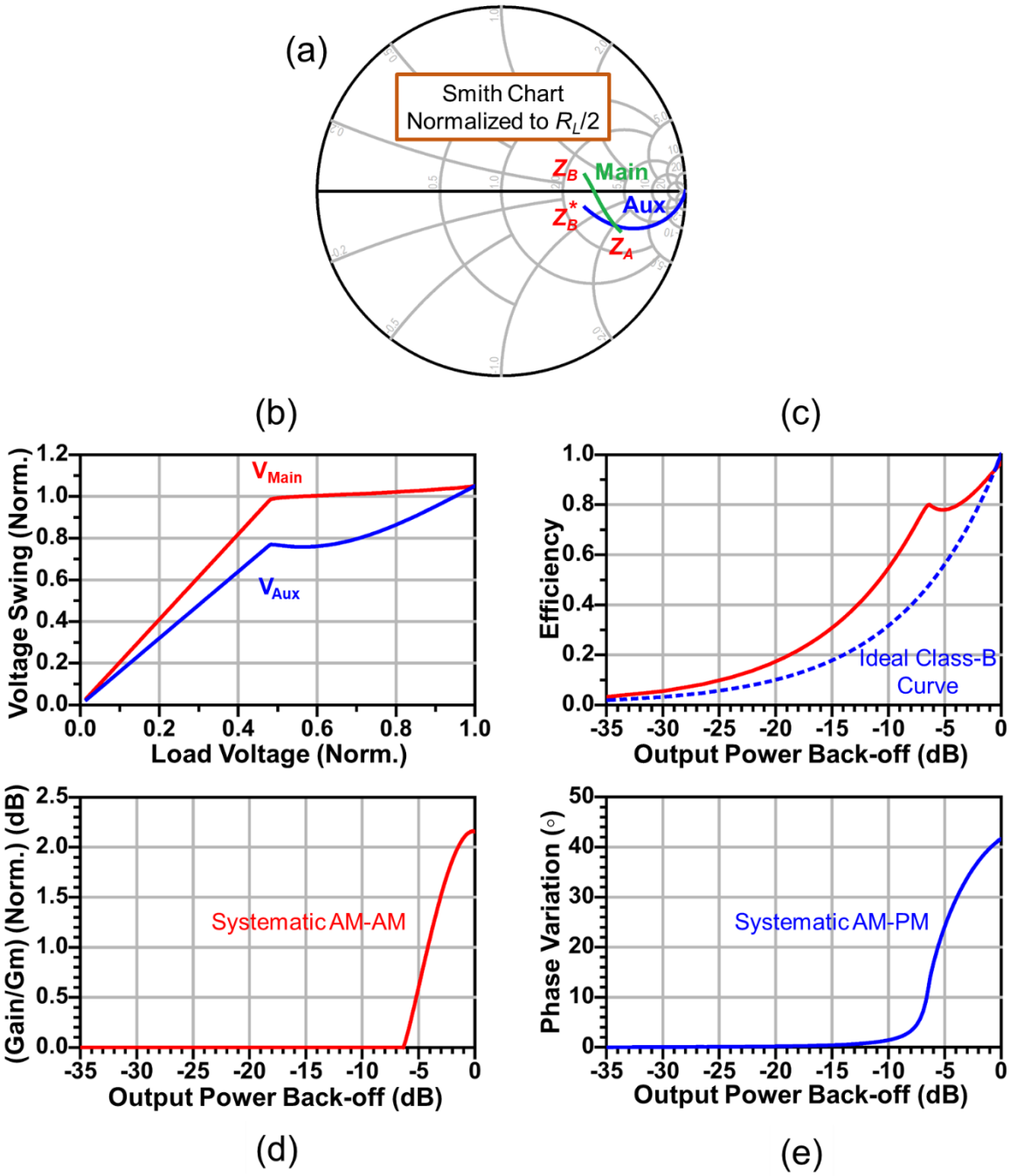


Figure 4.7: Simulation of an example design with 90° phase shift at the input, using the idealized transistor model (nonlinear VCCS with knee voltage): (a) impedance trajectories seen by the amplifiers, (b) output voltage magnitudes of the amplifiers normalized to the main supply voltage, (c) normalized overall efficiency, (d) systematic AM-AM, and (e) systematic AM-PM.

There is an appreciable amount of load modulation for both PA cells (Fig .4.7a), and the main amplifier is less driven into deep saturation (Fig. 4.7b). The efficiency peaks at a back-off power of 6.2dB (Fig. 4.7c), and the systematic AM-AM, captured by the simulation, is ~2.1dB (Fig. 4.7d). A more general form of the equations can be applied in this case

$$Systematic\ AM-AM = 2\times\frac{Real\{Z_B\}}{Real\{Z_A\}} = 2\times\frac{PF_B}{PF_A}\times\frac{|Z_B|}{|Z_A|} \tag{4.10}$$

$$LMR_{Main} = \frac{Real\left\{\frac{1}{Z_B}\right\}}{Real\left\{\frac{1}{Z_A}\right\}} = \frac{PF_B}{PF_A}\times\frac{|Z_A|}{|Z_B|} \tag{4.11}$$

Note that since the PA cells operate in current mode and at the maximum power, they see different reactive loads and experience different amounts of saturation, the actual voltage phase shift at the combiner ports is not 90°, therefore the systematic AM-PM shown in Fig. 4.7e is slightly lower than the expected value of ~45° suggested by the first line of Eq. 4.6.

The above-mentioned behavioral characteristics of this intermediate design are in between those of the two previous ones; therefore by changing the input phase shift, a certain design goal (e.g., a required amount of systematic AM-PM) can be achieved, although the other specifications (e.g., the systematic AM-AM) will vary as well, in a manner that may result in an undesirable outcome. An additional control knob, with a somewhat independent influence, is useful to make the PA work in a more favorable fashion. The bias condition of the PA cells, especially the auxiliary amplifier, can provide such a control parameter. Since in practical devices the gm is usually bias dependent, as the bias voltage of the auxiliary amplifier is varied, both the turn-on input power level and the gm change, affecting the overall AM-AM behavior as well as the backoff efficiency profile of the PA (similar to what happens in the Doherty architecture). For example, if the auxiliary amplifier is set to have a

low bias voltage (deep class-C) it will turn on at a higher input power level and even after that, it will have a low gm (soft turn-on). This condition will lead the main amplifier to go to deep saturation which is beneficial in terms of backoff efficiency, but it is problematic in terms of linearity since the reduced Gm at saturation drops the gain. In contrast, a higher bias for the auxiliary amplifier will result in a higher overall gain and a lower efficiency peak at backoff.

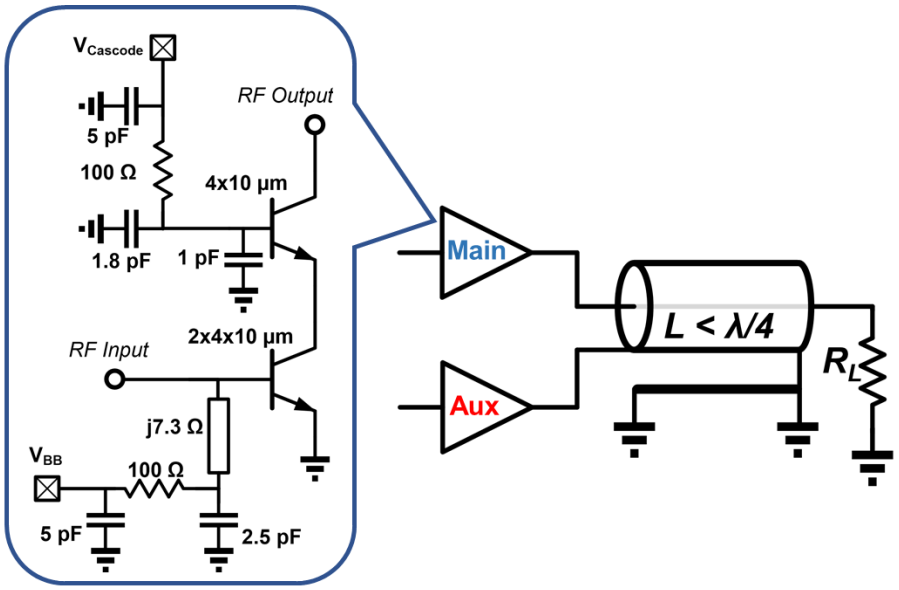
An additional feature of this architecture results indirectly from the AM-PM variation caused by the device nonideality and impacts the impedance trajectories seen by the unit PA cells. As noted above, the device related AM-PM arises mostly from the voltage dependent capacitance variation at the input and output nodes. The onsets of this phenomenon for the individual main and auxiliary PA cells are at different power levels, due to their bias and supply voltage differences. As a result, there is a power-dependent phase variation between the individual PAs, which together with the Chireix combiner result in "self-outphasing" that slightly changes the impedance trajectories at the intermediate power levels. To capture this effect in simulation a realistic device model is needed; the effect is shown in the simulated results for the experimental SiGe PA discussed in the next section.

The design methodology for the SILC PA adopted in this work is to linearize the overall PA response by appropriately choosing the input phase shift θ_0 and the auxiliary bias condition, such that the best AM-AM and AM-PM are obtained.

4.3 Implementation

The 28GHz high-efficiency dual-input ouphasing PA, described in Chapter 3, which was implemented in 130nm SiGe BiCMOS (GF 8HP) process [8], is used here as the core PA (Fig. 4.8a).

(a)



(b)

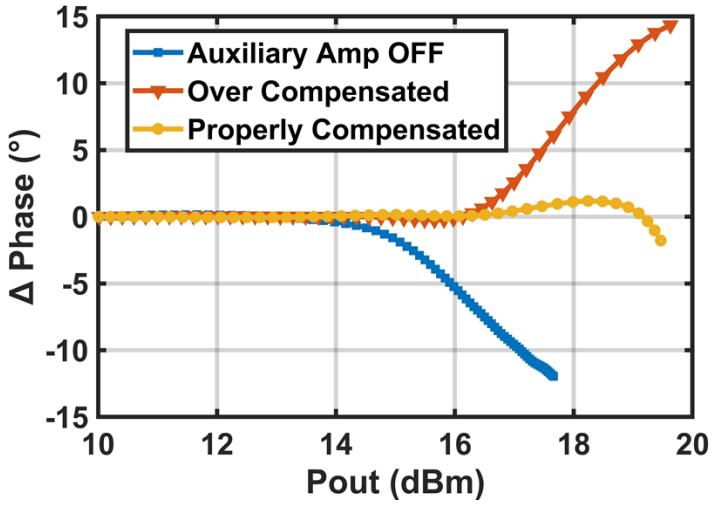


Figure 4.8: (a) Schematic of the core PA (b) Post-layout simulation of the overall AM- PM response at 28GHz.

The combiner is implemented as a "triaxial balun" with electrical length of ~λ/15 using the top 3 metal layers of the process, achieving an exceptionally low loss of ~0.5dB at 28GHz (determined in a back-to-back balun measurement). The unit amplifiers employ a cascode cell with a smaller size top device to achieve the low output capacitance needed for the Chireix operation. The bias voltages have been modified in accordance with the desired mode of operation described in the previous section (i.e., class-C bias and higher V_{CC} for the auxiliary amplifier). Base biases were provided through 100Ω on-chip resistors and the transistors drew 33.4mA and 38.8mA, measured at maximum power, from supply voltages of 3.7V and 4.3V for the main and auxiliary PA cells, respectively.

Post-layout simulation of this PA, fed by a pair of phase-shifted RF signal sources, confirms the predicted behavior in terms of efficiency and linearity. As shown in Fig. 4.8b, if the auxiliary amplifier is completely turned off, the main amplifier by itself introduces a noticeable amount of AM-PM distortion toward its saturation. A proper bias of the auxiliary amplifier together with appropriate phase shift, result in a flat AM-PM response (Over-compensation is also possible and must be avoided).

Based on the simulations, in this design, the signal phase shift due to the input impedance difference of the PA cells is sufficient for the desired operation ($\theta = \theta_1$) and there is no need for an explicit delay line at the input ($\theta_0 = 0°$). Therefore, the same RF signal is fed to both inputs of the core PA, via DC blocking caps that are necessary because of the difference in the base bias of the PA cells. A back-to-back triaxial balun (fabricated to be tested separately) is used for this purpose. The core PA and the input signal splitter chips are attached next to each other on a board and connected via very short wirebonds, forming the

overall PA (Fig. 4.9). The effect of the wirebonds is included in the simulations by using series inductors.

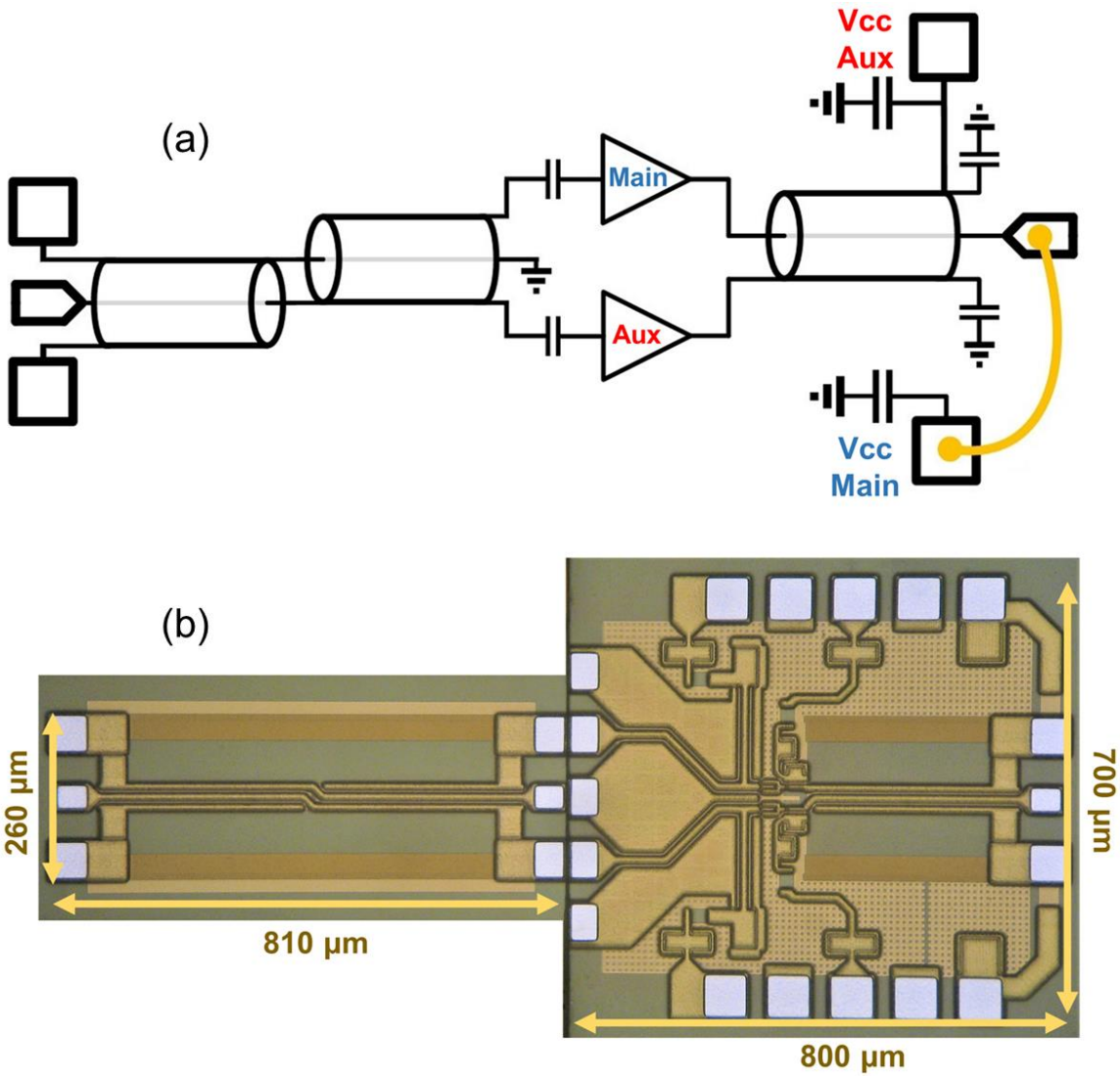


Figure 4.9: (a) Schematic of the overall PA. (b) Die photo (before wirebonding).

The post-layout simulation results of the overall PA, while being driven from a single 28GHz RF source, are shown in Fig. 4.10.

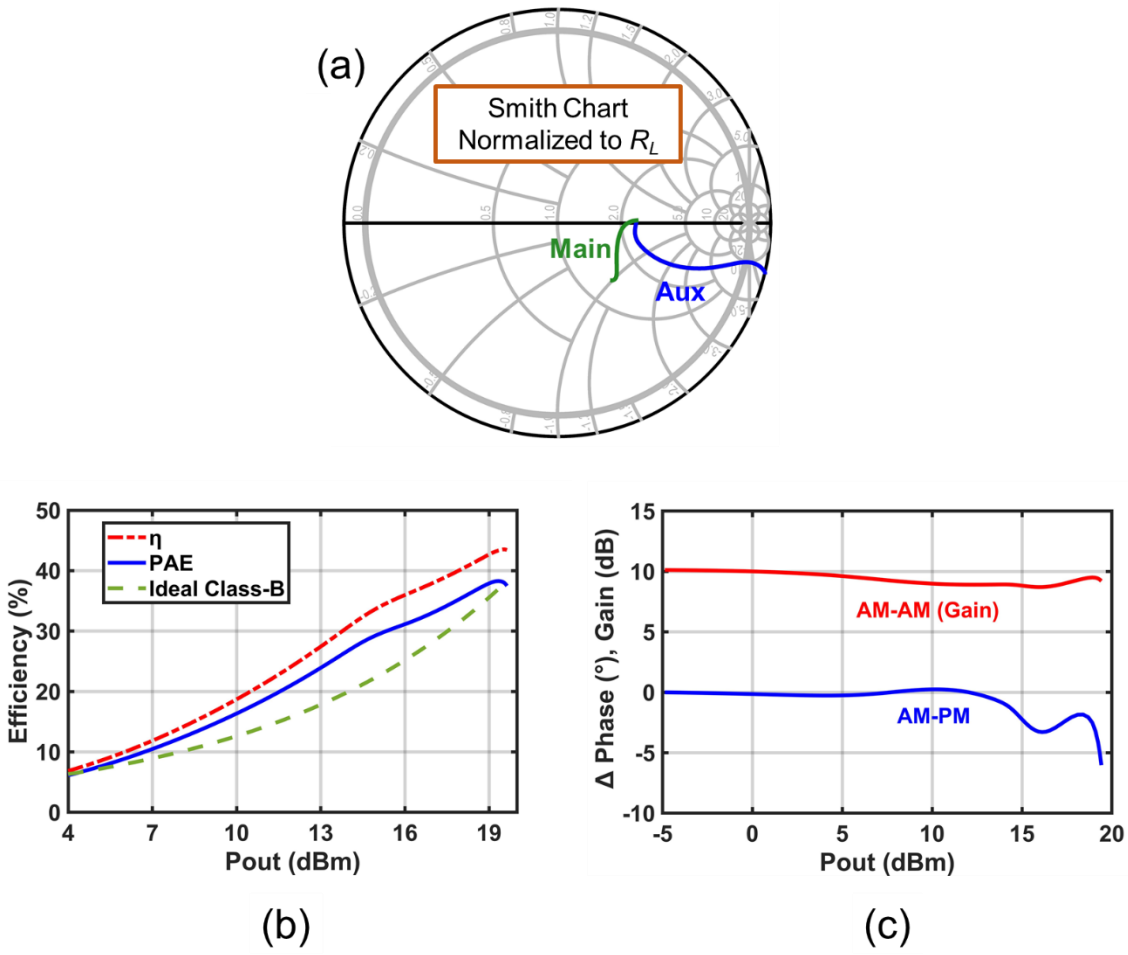


Figure 4.10: Full PA post-layout simulation at 28GHz: (a) Trajectories of impedance seen by the internal current sources of the main and auxiliary amplifiers (b) Efficiency, (c) Gain and AM-PM.

By manually de-embedding the 85fF device output capacitance, the impedance variations seen by the internal current sources of the main and auxiliary amplifiers are captured (Fig. 4.10a). The trajectories shown here (with the Smith chart normalized to R_L) are slightly more curved than those in the idealized simulations of Fig. 4.6 and Fig. 4.7, due to the "self-outphasing" phenomenon mentioned in the previous section. The insertion loss of the output balun is the expected value of 0.5dB and stays constant with respect to the output power.

Figure 4.10b shows that the PAE at 6-dB backoff is improved by 34% compared to an ideal Class-B, while Fig. 4.10c shows the gain is flat to within 1dB and the phase variation is below 5 degrees up to 19dBm output power. The AM-AM and AM-PM variations remain in these ranges at least for 1GHz of bandwidth, under the nominal bias condition.

4.4 Measurement Results

Measurements are carried out at 27.5GHz (instead of 28GHz) due to the presence of a slight mistuning in the circuit. Figure 4.11a shows the continuous wave (CW) test result demonstrating more than 19dBm Psat with peak PAE of 34.4% and 6-dB backoff PAE of greater than 23% that corresponds to 34% improvement over ideal Class-B backoff behavior.

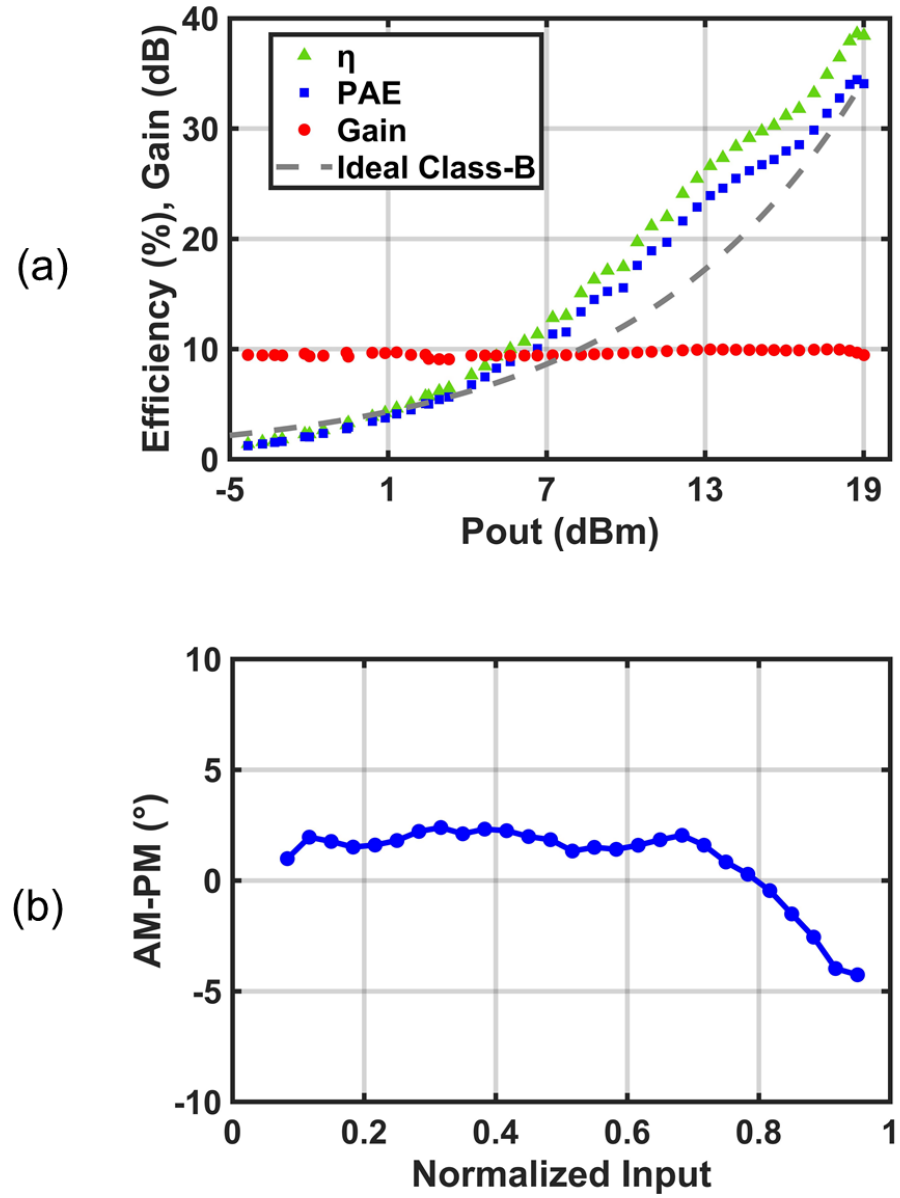


Figure 4.11: (a) CW measurement at 27.5GHz showing efficiency and gain (b)AM-PM obtained from the modulated signal measurement under the same bias condition.

The gain is also shown on the same plot; it is flat to within ±0.3dB of 9.7dB. The AM-PM shown in Fig. 4.11b is obtained from the modulated signal measurement under the same bias condition and has ±3.3 degrees variation.

A 100MHz 64-QAM OFDM signal (generated with Keysight M8195A Arbitrary Waveform Generator and up-converted to 27.5GHz) is used to evaluate the dynamic performance of the PA (with output signal captured using Agilent DSO80604B 6GHz 40GS/s real time oscilloscope after down-conversion to 2.5GHz). Average collector efficiency of 22.9% and average PAE of 20.2% is obtained for 11.9dBm output power. Linear equalization has been applied to the complete setup including the DUT (using Keysight VSA software), and with no DPD, EVM of 4.9% and ACLR better than -33dBc (at 100MHz offset from the carrier frequency) are achieved. Figure 4.12 shows the resulting constellation and spectrum of the output signal.

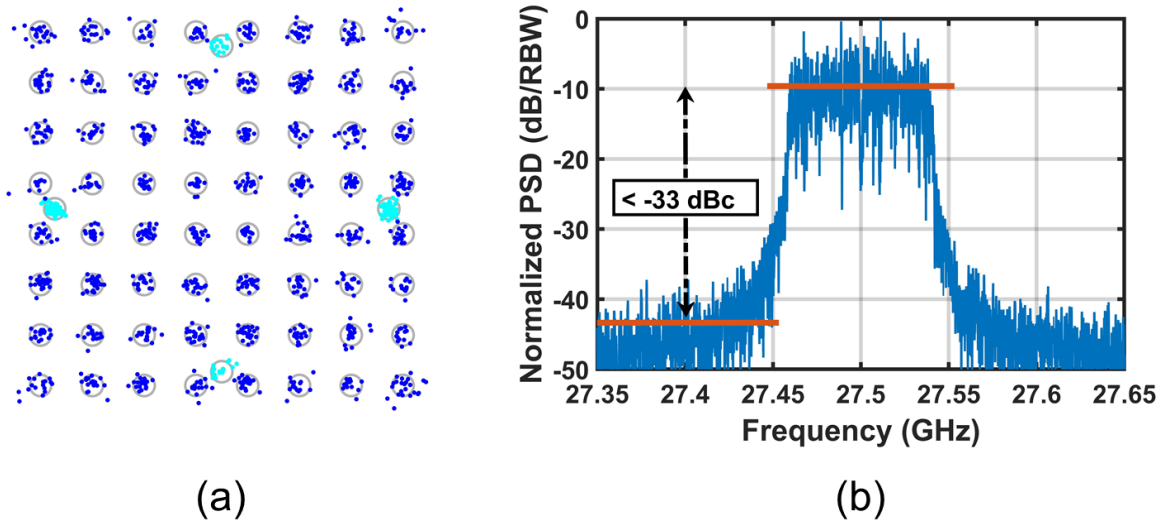


Figure 4.12: (a) constellation and (b) spectrum of the PA output for a 100MHz 64-QAM OFDM signal cantered at 27.5GHz with no DPD.

Table 4.1 summarizes the SILC PA performance and compares it to the recently published state-of-the-art power amplifiers that modulate OFDM signals without employing digital enhancement.

Table 4.1: Comparison to state of the art.

	This Work	[15]	[16]	[17]/[19]	[18]/[19]	[20]	[21]
Frequency (GHz)	27.5	28	26.75	27	26	30	27
Technology	130nm SiGe	45nm CMOS-SOI	45nm CMOS-SOI	45nm CMOS-SOI	45nm CMOS-SOI	28nm CMOS	40nm CMOS
Topology	SILC	Doherty	2-stack	2-stack	4-stack	2-stage Diff.	3-stage Diff.
Psat (dBm)	19	22.4	18.9	19.5	23.6	15.3	15.1
Peak PAE (%)	34.4	40	40.5	46.7	32	36.6	33.7
6-dB PBO PAE (%)	23.9	28	23	24	17	18	15.1
Gain (dB)	9.7	10	12	10*	11.5	16.3	22.4
Modulation Type	64-QAM OFDM	64-QAM OFDM	64-QAM OFDM	64-QAM OFDM	64-QAM OFDM	64-QAM OFDM	64-QAM OFDM
Signal BW (MHz)	100	800	800	800	800	250	800
Predistortion	No	No	No	No	No	No	No
Average Pout (dBm)	11.9	13	9.8	9.2	15	5.3	6.7
EVM (%)	**4.9**	5.5	5.5	5.5	5.5	5.6	5.6
Average PAE (%)	**20.2**	16.8	14.8	17	14	9.6	11

* Gain at maximum PAE

Given these constraints, this work presents the highest reported average efficiency for a silicon-based integrated PA.

4.5 Conclusion

SILC, a new method for simultaneously improving backoff efficiency and linearity of PAs, is presented. The circuit consists of a Chireix outphasing topology with asymmetric biases for the PA cells and a simple input signal splitter creating a phase shift between them. The implemented mm-wave integrated circuit achieves an average PAE greater than 20% while modulating a 64-QAM OFDM signal with 100MHz bandwidth and 11.9dBm average output power at 27.5GHz. Without using DPD, EVM less than 5% and ACLR better than -33dBc are obtained, demonstrating the potential for emerging 5G applications. Additional

improvements may be possible in future work by using different device sizes for the two branches.

Acknowledgement

This chapter, in full, has been submitted for publication of the material as it may appear in IEEE Journal of Solid-State Circuits, 2019, Rabet, Bagher; Asbeck, Peter. The dissertation author was the primary investigator and author of this paper.

Appendices

I- The Idealized Transistor Model

A mathematically defined two-port network (Fig. 4.13a) is used to create the transistor model as a nonlinear voltage-controlled current source (VCCS) that includes a knee voltage contribution.

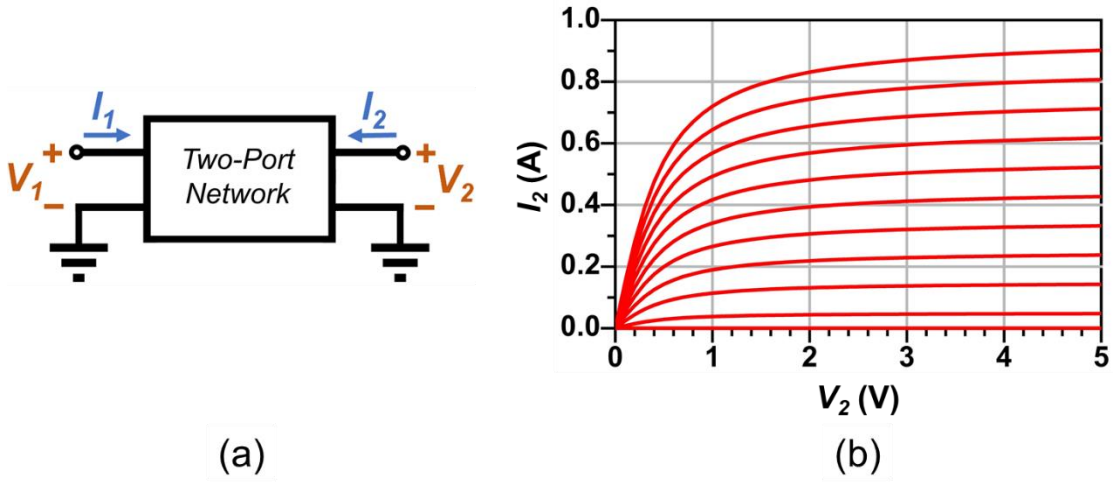


Figure 4.13: (a) A generic two port network that is used to create the VCCS transistor model, (b) I-V curves of the model described by (12) with V_{th}=0.5, gm=0.1, and α=2.5 while V_1 is swept from 0 to 10V with 1V steps.

The set of conditions and equations that are used to define the transistor-like behavior are given below.

$$\begin{cases} I_1 = 0 \\ if\ [(V_1 - V_{th}) \leq 0]\ or\ [V_2 \leq 0]\ then\ I_2 = 0 \\ else\ I_2 = gm \times (V_1 - V_{th}) \times \dfrac{\tan^{-1}(V_2/\alpha)}{\pi/2} \end{cases} \tag{4.12}$$

V_{th} and gm model the transistor's threshold voltage and forward conductance respectively, while α sets the value of the knee voltage. Figure 4.13b shows a set of I-V curves obtained by using this transistor model with V_{th}=0.5, gm=0.1, and α=2.5. In this simulation V_1 is swept from 0 to 10V with 1V steps.

II- Derivation of the Systematic AM-PM Equation

In order to calculate the systematic AM-PM, the phase of the load voltage at low power (V_{L1}) and at peak power (V_{L2}) are subtracted from each other. Figure 4.14a shows the equivalent circuit at low power when the auxiliary amplifier is off, with the corresponding currents annotated.

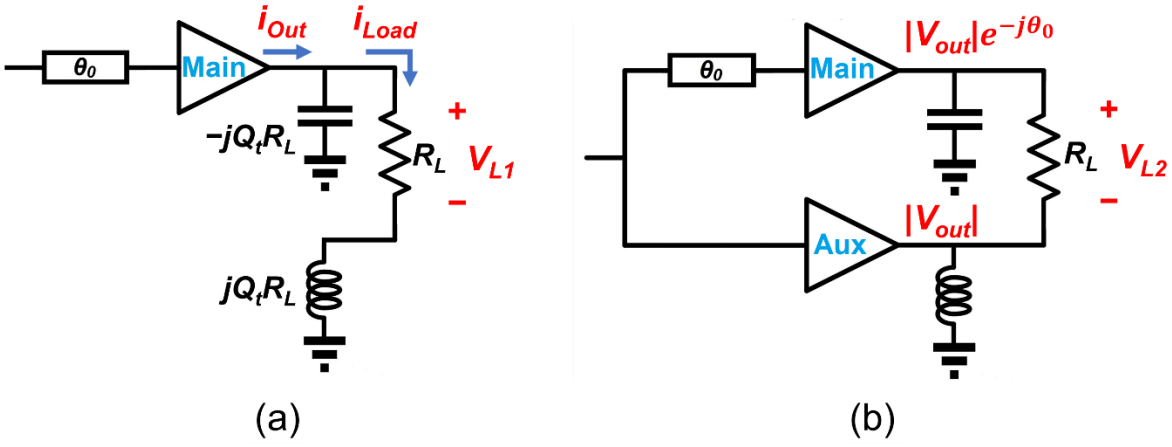


Figure 4.14: Equivalent circuits to calculate the phase of the load voltage at (a) low power, and (b) peak power.

It is obvious that the phase of V_{L1} is the same as the phase of i_{Load} in this mode of operation. By writing KVL and KCL at the output node of the main amplifier, it can be shown that $i_{Load} = i_{Out} \times (-jQ_t)$, and since i_{Out} itself has θ_0 degrees delay, the phase of V_{L1} is calculated to be $-(\theta_0 + 90°)$.

Figure 4.14b shows the equivalent circuit at peak power. If the PA is designed such that at this point the main and auxiliary amplifiers see a purely resistive (PF=1) impedance and have the same voltage swing ($|V_{Out}|$), V_{L2} would be equal to $|V_{Out}| \times [\exp(-j\theta_0) - 1]$. In that case, it can be shown that the phase of V_{L2} is equal to $-(\theta_0/2 + 90°)$.

The overall phase variation from low power to peak power is equal to phase of V_{L2} minus phase of V_{L1}, that results in $\theta_0/2$, as it was suggested by Eq. 4.6.

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Chapter 5

Gate Leakage Current Effects on the Linearity of CMOS Power Amplifiers

5.1 Introduction

The inherent linearity of the mm-wave PAs is of prime concern for the 5G systems which typically incorporate many individual power amplifiers driving large antenna arrays with wide signal bandwidths. In the previous chapter we introduced the SILC PA that achieves good linearity while maintain high efficiency. However, for applications with area constrains, small footprint class-AB PAs with inherent linearity are desirable. To optimize linearity in cellular band handsets, a widely used approach is to engineer the AM-AM and AM-PM distortion characteristics and harmonic terminations of the PAs, in order to develop "sweet spots" in their intermodulation response [1-3]. At these spots the 3rd order intermodulation products (IM3) decrease by 5 to 10dB from the general extrapolated values as a function of power. The sweet spots of IM3 observed in two-tone tests are replicated in the ACPR found with broadband modulated signals, and are also evident in the EVM measured

within the signal band. A common scenario for the appearance of sweet spots is to have gain expansion at power levels slightly lower than the gain compression experienced when the PAs saturate. As a result, there can be cancellation between contributions from 3rd order and 5th order nonlinearity terms. Similar linearity behaviors are found for mm-wave PAs [4,5]. Figure 5.1 shows gain vs input power for a representative mm-wave PA (fitted to measured results from the circuit described below) exhibiting gain expansion and compression, and computed results from a two-tone test, as well as ACPR and normalized mean square error (NMSE) for an OFDM signal with 8.5dB PAPR, which all display "sweet spot" behavior.

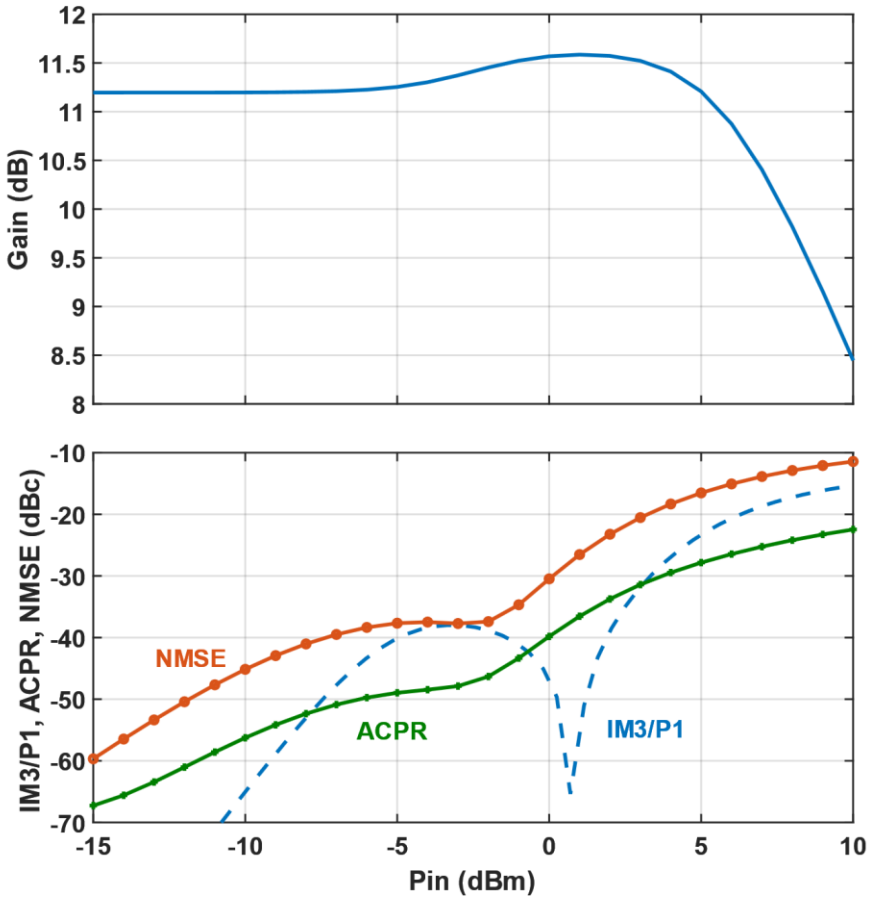

Figure 5.1: Gain vs Pin (CW measurements) and simulated IM3/P1(two-tone), ACPR and NMSE (OFDM) vs Pin average.

AM-PM and memory effects are neglected in the simulations. With strict EVM requirements it is necessary to limit the amount of gain expansion attained (to values of order 0.5 to 1dB), which is principally used to balance out the gain compression, thereby delaying its onset to higher power levels. In order to produce the gain expansion in cellular band PAs, a variety of strategies are employed. HBTs with input base voltage bias inherently produce strong gain expansion with increasing power level. Numerous input bias circuits that control the degree of gain expansion have been reported for both HBTs and FETs [2-5]. For scaled CMOS devices, the behavior of transconductance vs input voltage generally leads to decreasing gain as a function of input power, for Class-A and Class-AB bias conditions, and so the inherent device characteristics do not favor the gain expansion and sweet spot behavior, although it is observed in deep Class-AB [6]. Adaptive bias circuits to control gain have been reported for CMOS mm-wave amplifier [4,5], although they are not yet widely used. In this chapter we demonstrate that PAs with scaled CMOS devices also exhibit small amounts of gate leakage currents that are a function of output power. If large value resistors are used in the bias circuits, the gate leakage currents lead to variable gate voltage vs output power, and impact the overall linearity of the amplifier. The effects of gate leakage and its influence on linearity are demonstrated experimentally using a previously reported 28GHz PA implemented with 45nm CMOS-SOI [7], which exhibits near state-of-the-art combination of output power, efficiency and linearity. Two-tone tests confirm the presence of sweet spots in IM3 and the influence of the gate leakage current is demonstrated by varying the gate bias resistance.

5.2 Experimental Circuit

The 28GHz power amplifier employs the 2-stack structure shown in Fig 5.2; a corresponding microphotograph is also shown [7].

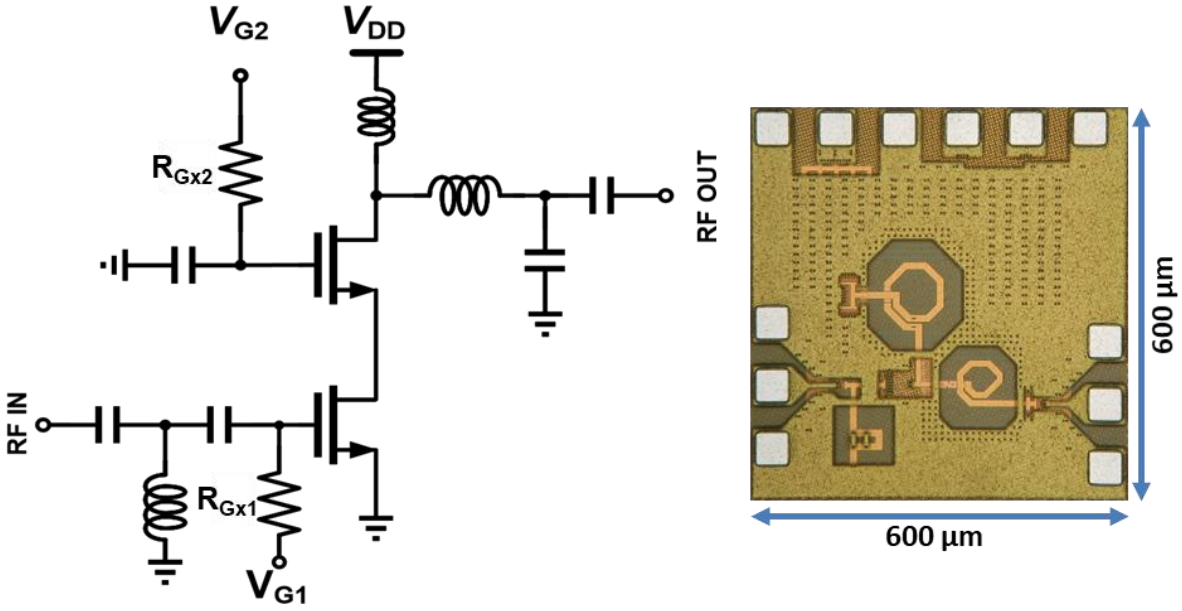

Figure 5.2: Circuit diagram of a 2-stack 28GHz PA, along with chip microphotograph.

The overall gate width is 307um for each of the transistors. The voltage swing at the top gate is controlled by the inclusion of an appropriately size capacitor at the gate and its dc bias is such that the overall V_{DS} swings of the two transistors are approximately equal. The power supply voltage is 2.2V corresponding to approximately 1.1V V_{DS} per device**.**

Gate voltages V_{G1} and V_{G2} are applied through on-chip resistors set to a high value (R_{G1x}=R_{G2x}=14KΩ) so that there is no loss of RF signal in the bias path. With CW signal inputs at 28GHz, the measured PAE and gain vs output power are shown in Fig. 5.3 (bias conditions V_{DD}=2.2V, V_{G1}=0.175V, V_{G2}=1.7V, corresponding to deep Class AB), which illustrate Psat=19dBm, and peak PAE=43.

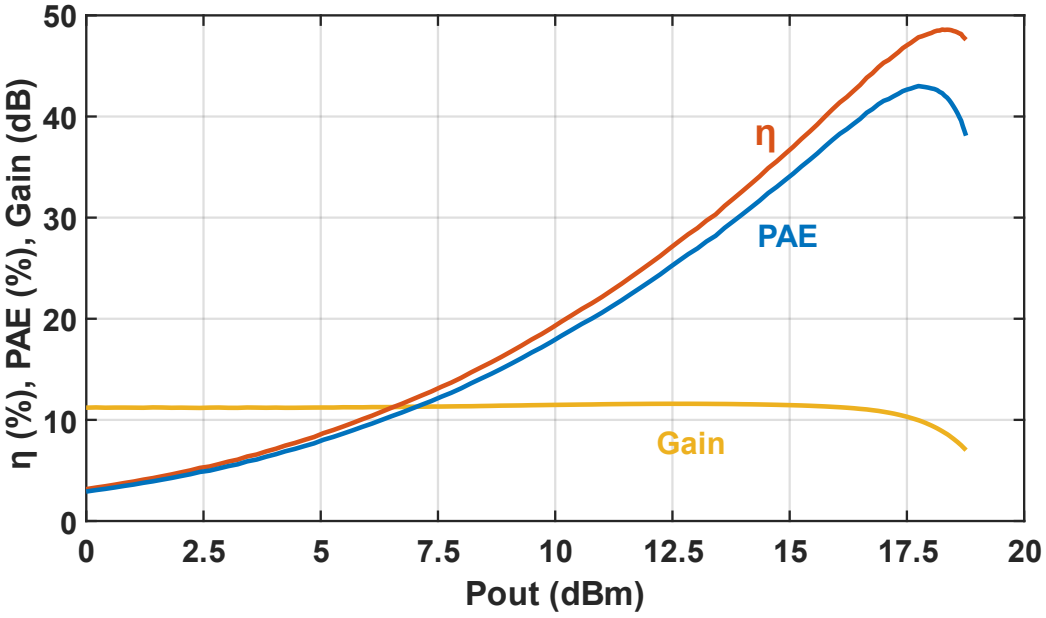

Figure 5.3: Measured drain efficiency, PAE and gain vs output power at 28GHz.

In modulation experiments with 800MHz 64-QAM OFDM signals, 5.5% EVM is maintained with PAs of this design up to output power of 9.8dBm and PAE= 14.8% without DPD [7].

5.3 Gate Leakage and Bias Effects

For thin gate oxides, the presence of gate leakage currents due to Fowler-Nordheim tunneling is well-established, and typically captured in foundry models. The leakage current can be in opposite directions for regions of the channel near the source and near the drain, with a net direction that depends on the value of V_{ds}. Figure 5.4 depicts representative band diagrams including gate oxide and channel, illustrating the tunneling paths.

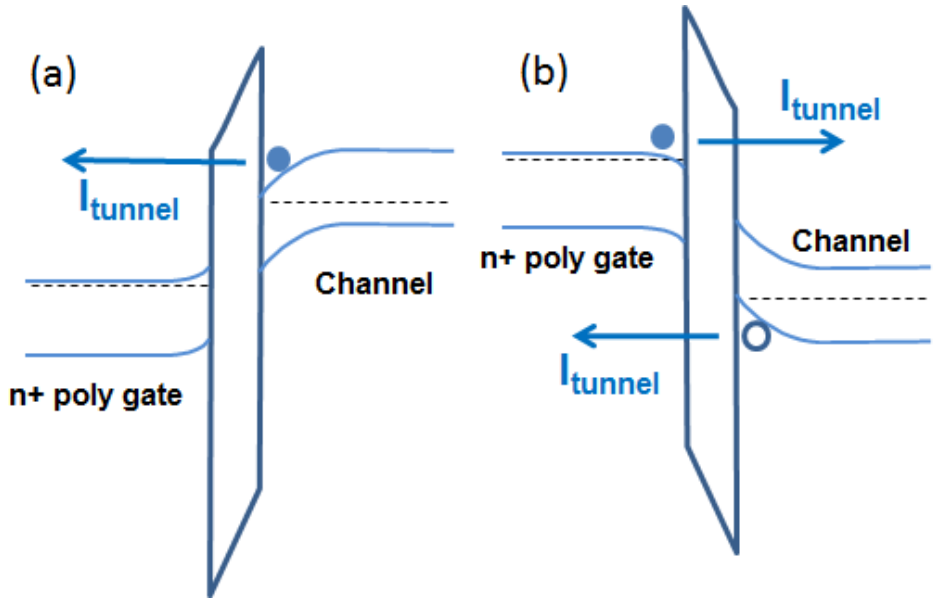

Figure 5.4: Band diagram of FET gate, oxide and channel showing gate leakage paths: (a) near source, for Vgs>0; (b) near drain, for Vgs<0 and Vds>0.

Near the source, for a Vgs>0 bias condition, electron tunnel current can flow from channel to gate (Fig. 5.4a). Near the drain, for Vgs<0 and Vds>0, the oxide electric field reverses as shown in Fig. 5.4b. This last bias condition occurs in Class-AB power amplifiers during a portion of the cycle when the drain current is off. Figure 5.5 presents measurements of the gate leakage current for the experimental circuit, showing that the gate leakage changes direction when the output power level exceeds 14dBm, and the net variation reaches 4.5uA (~15nA/um) when the output power is maximum (drain voltage for the bottom transistor reaches 2V and the gate voltage is at its minimum level of -0.8 to -1V.

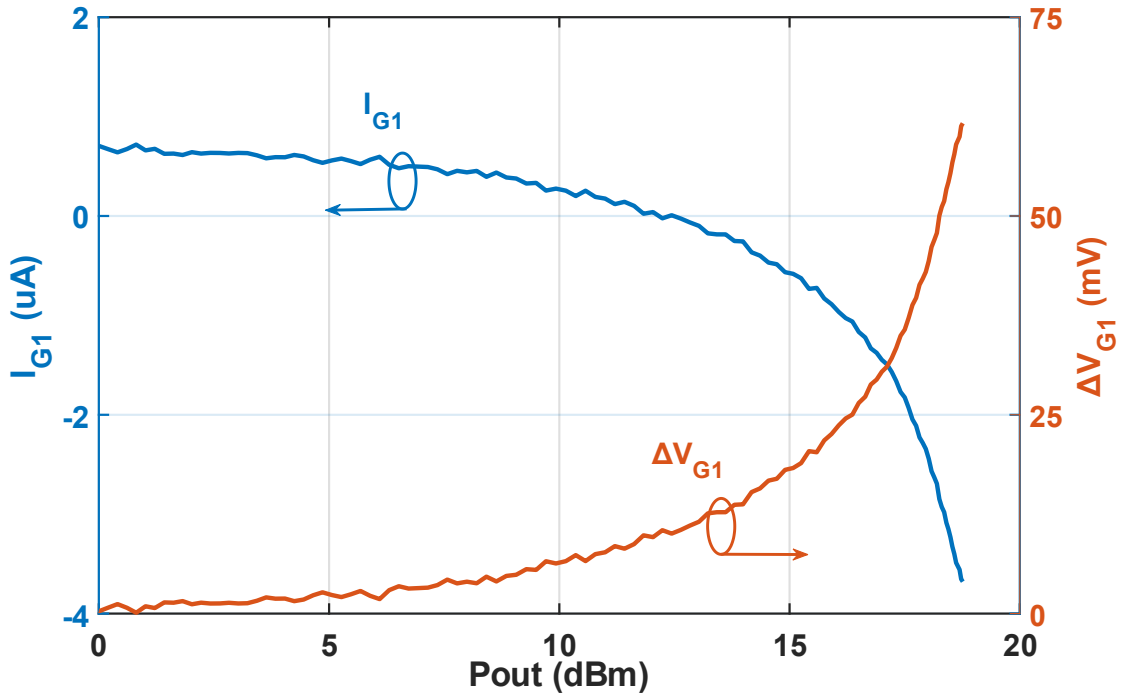

Figure 5.5: Measured gate leakage current I_{G1} vs output power, and calculated V_{G1} bias variation (R_{Gx1}=14KΩ).

At high power levels the net gate leakage I_{g1} is out of the gate of the FET, and thus there is voltage drop ($I_{G1}R_{Gx1}$) which increases the value of internal gate voltage as shown in Fig. 5.5. This tends to produce gain expansion as the power increases.

It is necessary to keep the gate tunneling currents within bounds, in order to not incur reliability problems from time-dependent dielectric breakdown (TDDB). The time-to-breakdown for TDDB is known to be dependent on the aggregate charge due to tunnel currents [8], and is a very strong function of voltage drop between gate and drain. The use of high value resistors to bias the gate helps to limit this voltage drop by self-adjusting the dc gate voltage.

5.4 Linearity Measurements

To quantify the effect of leakage current on the linearity of the PA, probe-based measurements were made of gain vs output power under CW excitation, and two-tone measurements with variable tone separation centered at 28GHz. Measurements were made with two different values of R_{Gx1}, in order to induce different amounts of voltage drop $I_{G1}R_{Gx1}$ due to the gate leakage. In one case, the on-chip bias resistor of 14KΩ was used alone. In the second case, an off-chip resistor of 39KΩ was used in addition to the on-chip resistor. This increased the overall value of power-dependent voltage drop (although only by a factor of 2.1x since the gate leakage current I_{G1} was dependent on the R_{Gx1} value). Gain and two-tone response are compared for the two R_{Gx1} values after adjusting the externally applied gate voltage V_{G1} so that the drain current with input power set to zero are equal. Figure 5.6 compares the CW gain vs output power for the two cases, illustrating an increase in gain expansion with the larger value of R_{Gx1}.

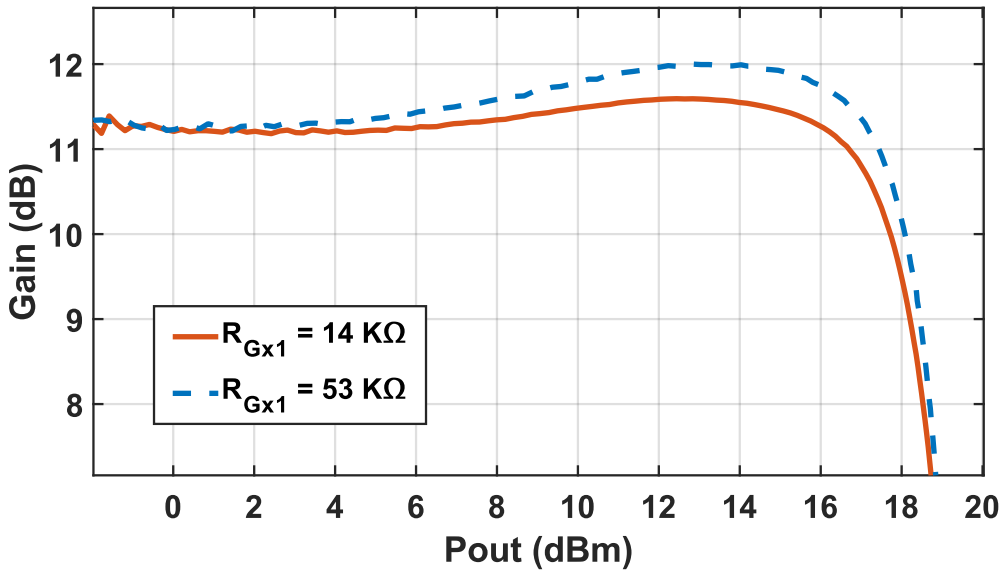

Figure 5.6: Measured gain vs output power using R_{Gx1}=14 (solid line) and 53KΩ (dashed line).

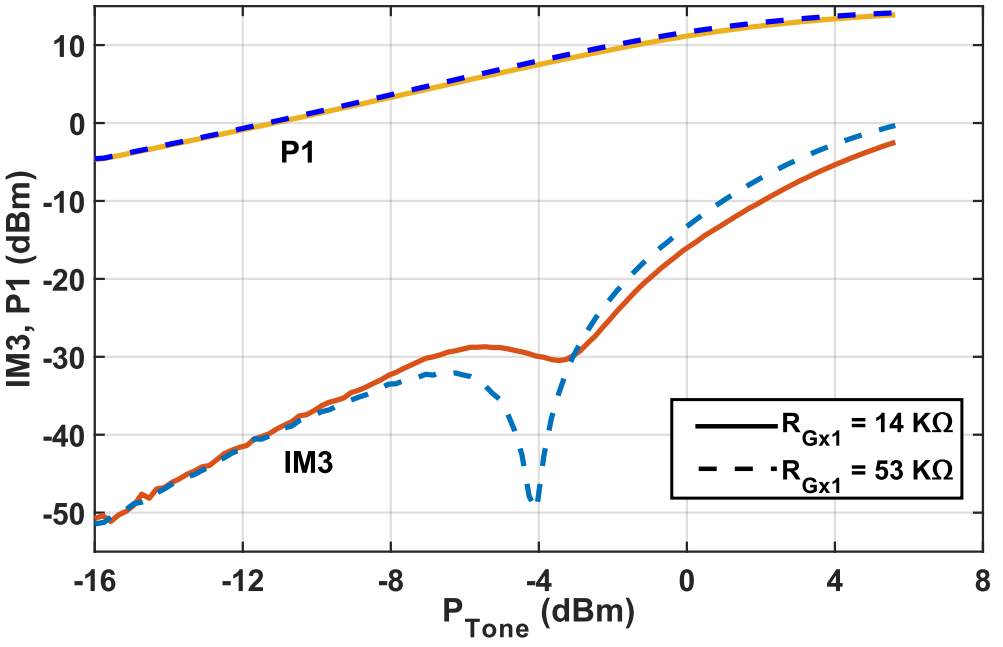

Figure 5.7: Measured IM3 and fundamental output (P1) vs input tone power, using R_{Gx1}=14KΩ (solid line).

Figure 5.7 depicts the IM3 values in two-tone measurements showing more pronounced sweet spots for the high R_{Gx1} bias resistors. Only lower sideband intermodulation is shown; results for the upper sideband are roughly similar. For Fig. 5.7, a tone spacing of 0.2MHz was used. Measurements of IM3 carried out with various tone separations are shown in Fig. 5.8 for the on-chip R_{Gx1}=14KΩ case.

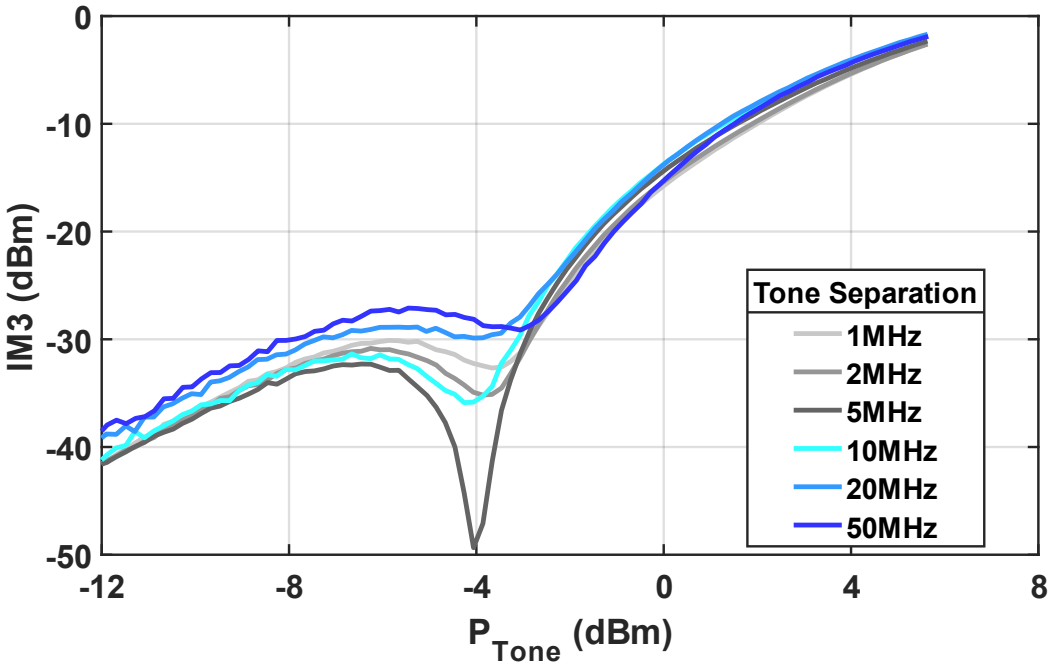

Figure 5.8: IM3 vs input power for tone spacings of 1MHz, 2MHz, 5MHz, 10MHz, 20MHz and 50MHz (R_{Gx1}=14KΩ).

With tone separation of 50MHz, the depth of the notch is decreased, although it is still present. The varying depth and location of the notch vs tone spacing indicates presence of memory effects (possibly self-heating and $R_{Gx1}C_{gs}$ time constant) which can affect the amount of gain expansion.

5.5 Discussion and Conclusion

Calculations (Fig. 5.1) based on the gain curves of Fig. 5.6 indicate sweet spot behavior in rough accord with experiment, despite the omission of AM-PM distortion and self-heating. The agreement is in keeping with earlier observations that AM-PM effects are small in these amplifiers [9]. The desirable amount of gain expansion tolerable depends on signal criteria. Excessive gain expansion produces higher IM3 at lower power levels and could worsen BER even if average EVM is improved.

In summary, it is shown that linearity performance measures such as IM3, ACPR and EVM can be improved in mm-wave CMOS-SOI PAs by incorporation of a small amount of gain expansion, and that gain vs power is influenced by FET gate leakage currents. Further control over gain expansion and AM-AM characteristics is expected from active bias networks.

Acknowledgement

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Chapter 6

Summary and Future Work

6.1 Summary

The advanced high data rate wireless transmitters with MIMO capability that employ phased array architectures and modulate wide band complex signals, require high efficiency and linearity from the power amplifier blocks. Among the well-known ways to improve the efficiency, the supply modulation methods like envelope tracking do not work well when the signal bandwidth is wide. Therefore, the Doherty architecture, which is an active load modulation technique, has been widely used due to its simplicity. In this dissertation, alternative architectures were demonstrated that are potential candidates for future wireless systems. It was shown that the dual-input current-mode outphasing PAs can achieve exceptionally high average efficiency values if implemented and controlled properly. Another challenge, particularly for the mm-wave realizations, is the insertion loss of the passive structures in the commercial silicon IC processes. A novel Chireix power combiner was presented that exploits the inherent asymmetry of the triaxial balun, captured by its model, as an advantage to achieve low loss, enabling high efficiency results at 28GHz. Some

applications may not be able to afford dual-inputs and DPD. For these cases, the SILC PA was introduced to address the backoff efficiency and linearity requirements while using a single input with no DPD. In this technique the nonlinearities caused by the transistor devices get compensated by the systematic AM-AM and AM-PM variations that result from the architecture of the circuit. Finally, it was shown that introducing dynamic bias to the class-AB PAs, which in the case demonstrated was produced by the gate leakage current, can be an effective way to enhance their linearity performance.

6.2 Future Work

There are still more challenges to be addressed for the current and future wireless transmit and receive systems. If the fully digital phased arrays, for which every PA has a dedicated baseband unit, become commercially feasible, the presented high efficiency dual-input current-mode outphasing PAs, that rely on DPD, can be employed to achieve high performances. The symmetry involved in the outphasing approach reduces the overhead of implementing two inputs per PA. For the more realistic analog and hybrid beamforming phased arrays, however, the inherent linearity of the unit PAs is still of a great importance. To continue the work presented in Chapter 5 that utilized the leakage current of the device itself to improve the AM-AM response, explicit analog circuitry can be used to provide dynamic biasing with better control. The AM-PM response is also equally important and needs to be analyzed and addressed by utilizing adjustable predistorters.

Another solution to linearize the response of a phased array transmitter in which one baseband unit serves multiple PAs, is to use a single DPD to correct the collective response of

the array. Unfortunately, the effectiveness of this approach reduces when the PAs exhibit different nonlinearity characteristics, that can be due to the impedance variations introduced by the antenna elements during the operation. This impedance variation causes greater than unity VSWR, and is a major challenge, not just for the linearity concerns but also for reliability and power handling issues. The variations can be deterministic, e.g., because of the coupling of the antenna elements during beam steering, or random, e.g., due to a foreign object in the proximity of the antenna array. Adaptively-controlled tunable matching networks can be explored as solution a for this problem.