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Authors

Burmeister, E F

Bowers, J E

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Integrated Gate Matrix Switch for Optical Packet Buffering

Emily F. Burmeister, *Student Member, IEEE*, and John E. Bowers, *Fellow, IEEE*

Abstract—An integrated 2×2 semiconductor optical amplifier gate matrix switch is characterized for use in an optical packet buffer. Error-free performance for all port configurations is demonstrated for 40 Gb/s with less than 1-dB power penalty and an input power dynamic range of greater than 15 dB. Switching times are measured for decreasing optical input power to show an upper limit of 1-ns rise time (20%–80%). The factors limiting the maximum number of recirculations are explored toward optimizing future designs. It is concluded that the amplifier gate matrix switch is suitable for optical packet buffering.

Index Terms—Optical buffers, optical memories, optical switches, photonic integrated circuits, semiconductor optical amplifiers (SOAs).

I. INTRODUCTION

THE research drive to translate switching to the optical layer is being actively pursued. Optical packet switching presents a solution for future optical communication networking that uses capacity more efficiently, increases throughput, and provides greater flexibility than pure wavelength-division multiplexing [1]. However, buffering is a challenge that has yet to find a compact, scalable, high bit-rate solution. The majority of optical buffering approaches can be generalized as either feed-back or feed-forward buffers. Two-by-two and one-by-two switches have been investigated as the core of both feed-back [2] and feed-forward [3], [4] approaches. However, these approaches have not achieved great acceptance, primarily due to switch performance limitations. In order to overcome the limitations, an integrated semiconductor optical amplifier (SOA) gate matrix switch is evaluated in this letter. A recirculating buffer approach is chosen because it is a promising feed-back buffering approach [5]–[7]. A schematic of a recirculating buffer with a buffer depth of three is shown in Fig. 1.

Recirculating buffers place significant performance requirements on the 2×2 switch. Minimally, the switch must be bit-rate scalable up to 40 Gb/s, have low crosstalk (< -40 dB) and high extinction ratios (>40 dB) for cascadability [8], and be able to switch within packet guard bands (1–5 ns). Faster switches to allow shorter guard bands are desirable in order to increase the maximum link utilization. In addition, amplified spontaneous emission (ASE) must be kept low over many recirculations to maintain acceptable signal-to-noise ratios. Lastly, it is desirable

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The authors are with the Electrical and Computer Engineering Department, University of California at Santa Barbara, CA 93106 USA (e-mail: emily@ece.ucsb.edu).

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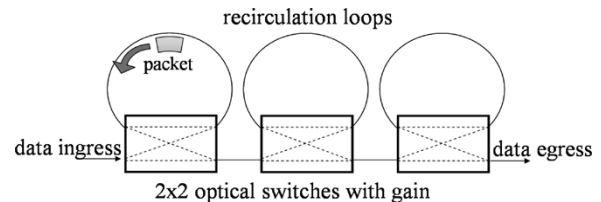


Fig. 1. Schematic of a recirculating buffer approach.

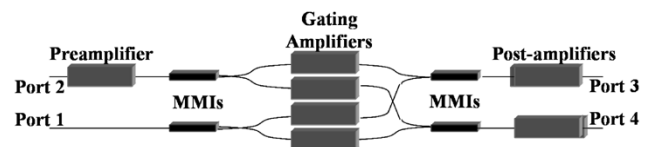
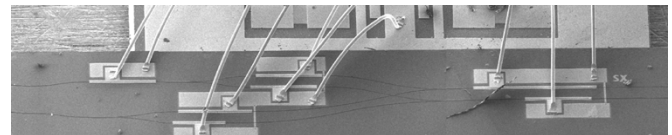


Fig. 2. SEM and schematic of a fabricated SOA gate matrix switch wirebonded to an aluminum nitride submount.

that the dynamic range be large in order to provide flexibility both for system implementation and to allow for recirculating loop power fluctuations. The SOA gate matrix switch is the most promising switch choice for recirculating buffers primarily because other switch types can not reach the crosstalk requirement. In the past, gate matrix switch designs have been studied for fast switching [9], developed for high gain [10], and measurements have been performed up to 1 [11] and 10 Gb/s [12]. To the best of the authors' knowledge, this letter is the first to evaluate gate matrix performance up to 40 Gb/s.

II. DEVICE DESIGN

In-Ga-As-P/In-P amplifier gate matrices were fabricated to perform 2×2 switching at a wavelength of $1.55 \mu\text{m}$ with low insertion loss. A scanning electron microscope (SEM) showing the switch design is pictured in Fig. 2. The switch uses an offset quantum-well platform for ease of fabrication, to allow for the possibility of future integration with other standard photonic integrated circuits, and to provide a lower confinement factor for linear performance at higher output powers [13]. Three amplifiers in addition to the four gating amplifiers were utilized to further compensate for losses from fiber-chip coupling, 3-dB 1×2 MMI coupler loss, 3-dB gating loss, as well as passive waveguide loss of approximately 2 dB/mm. The amplifiers range in length from 300 to 800 μm ; chosen such that the output powers of each stay below saturation levels for the largest range of input

power. The four port configurations were designed to provide different levels of gain in order to determine the optimized combination for a recirculating loop switch. The impact of a preamplifier at Port 2 is specifically investigated.

III. MEASUREMENTS

A. Measurement Setup

All experiments are performed on devices that are soldered and wirebonded to aluminum nitride submounts and affixed using thermal compound to a thermoelectric cooler. The submounts are cooled to approximately 15 °C. The optical signal (1556.5 nm) is modulated using a super high frequency (SHF) 50-Gb/s bit-error-rate tester (BERT) with return-to-zero (RZ) $2^7 - 1$ pseudorandom bit sequence (PRBS) data at 40 Gb/s. At 40 Gb/s, the BERT is limited to a PRBS length of $2^7 - 1$, however, 10-Gb/s measurements are taken for up to $2^{31} - 1$. An erbium-doped fiber amplifier, 1.2-nm thin film bandpass filter, and a variable optical attenuator are used to control the input light. A polarization controller is also used to maintain a transverse-electric-polarized input since the quantum-well SOAs are polarization dependent. Lensed fiber arrays are mounted on translation stages for coupling to and from the devices. Switching times are measured using continuous-wave light and by modulating the injection current of the gating amplifiers using a 3-GHz HP pattern generator.

B. Measurement Results

Static measurements were performed for initial characterization of the device. The highest crosstalk is -42 dB and the extinguished signal was buried in ASE at -45 dB below the signal, yielding an extinction ratio greater than 40 dB. The insertion loss of the port configurations including fiber-to-chip coupling ranges from 4 to 26.5 dB. The least loss is found for transmission from Port 2 to Port 3 which includes a preamplifier and the longest SOAs in the design. Increasing the wavelength to the gain peak of 1575 nm provides 3 dB of extra gain. The gain peak is higher than desired due to heating, but this can be reduced in subsequent chips with better contact metal resistance.

The sensitivity degradation for the four port configurations at 40 Gb/s is shown in Fig. 3. The back-to-back measurement is taken as a reference for the system by bypassing the device under test with a fiber patch cord. As can be seen in Fig. 3, all power penalties are below 1 dB. The primary limitation of sensitivity is the ASE that builds up in the amplifiers. The same measurements were repeated again at 10 Gb/s with NRZ $2^7 - 1$ and $2^{31} - 1$ PRBS data to show the influence of word length. Longer word lengths are expected to add extra power penalty because of pattern effects due to the presence of longer strings of zero or one bits. The power penalty for $2^{31} - 1$ PRBS data is 1 dB, only 0.25 dB above that found for measurements using $2^7 - 1$ PRBS data. The measurements are shown in Fig. 4.

The dynamic range of an optical switch is defined here as the range of optical input powers that are error-free (10^{-9}) while providing less than a 2-dB power penalty for a preamplified receiver. Nonlinear gain saturation in SOAs results in pattern effects which become more limiting with higher bit rates such as 10 and 40 Gb/s.

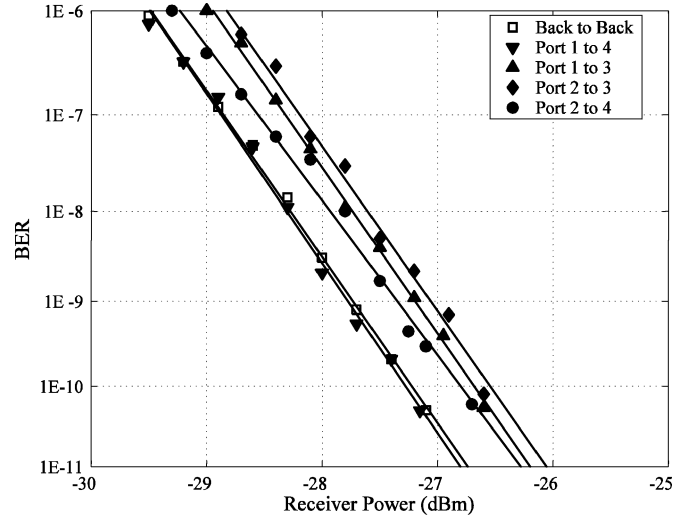


Fig. 3. BER versus optical receiver power for all port configurations at 40-Gb/s RZ $2^7 - 1$.

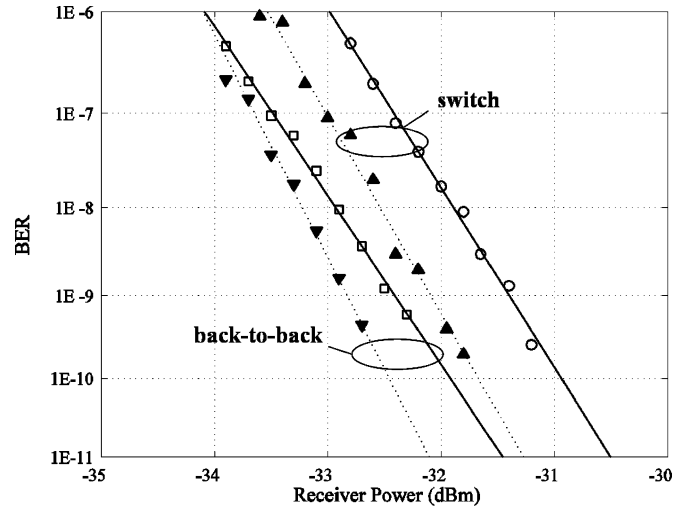


Fig. 4. BER versus optical receiver power for transmission from Port 2 to 3 at 10 Gb/s with $2^7 - 1$ (dotted line) and $2^{31} - 1$ (solid line) NRZ PRBS.

Power penalty for a BER of 10^{-9} is shown in Fig. 5 for two port configurations at varying optical input powers. The curves for the two transmission paths are similar for lower powers, but as expected, the influence on the upper power limit from gain saturation is more significant for the path with the preamplifier.

As previously noted in the introduction, recirculating buffer switching must occur in the guard bands between packets. Switching times versus optical input power are shown in Fig. 6 for varying gating currents. Higher input powers and gating currents both yield faster rise times since the photon density levels are closer to that needed for stimulated emission [9], [14]. However, for this application, there is no input power in the switch while switching between packets. Therefore, switching times will occur on the curve at the limit found for decreasing input powers. The rise times shown in Fig. 6 are from 20% to 80% of one level to provide more stability to the measurements at lower powers. Fall times were also measured and were consistently less than the rise times. This is expected

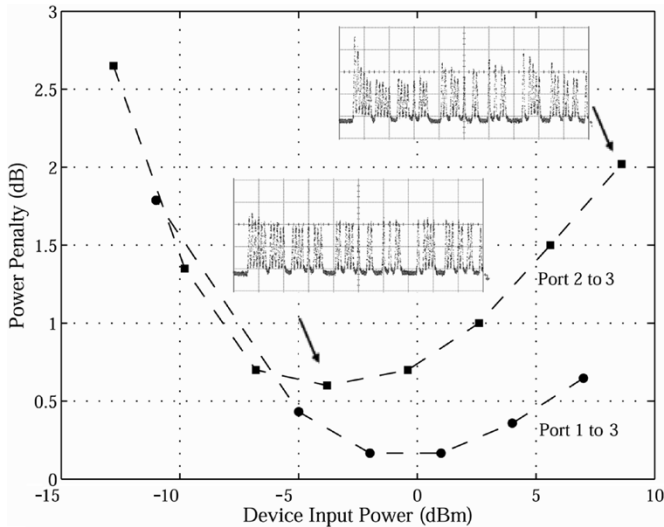


Fig. 5. Power penalty curves with corresponding scope traces are shown for transmission from Port 2 to 3 and Port 1 to 3 for 40-Gb/s RZ $2^7 - 1$.

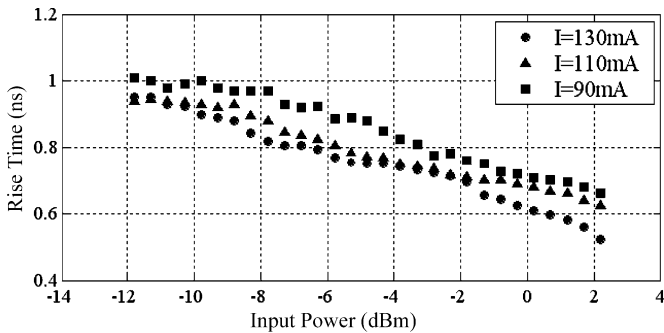


Fig. 6. Switching rise times as a function of the optical input power to the device and the injected current.

due to short carrier lifetimes while carrier densities are still high during the switching off of the SOA [9].

IV. CONCLUSION

Semiconductor amplifier gate matrix switches provide a solution for high performance switches needed for recirculation optical buffers. The switch studied in this letter demonstrates all of the requirements including low power penalty and high dynamic range at 40 Gb/s, low crosstalk, high extinction ratio, and fast switching. The challenge of a switch design for a recirculating buffer is to provide enough gain to compensate for delay line propagation, coupling, and chip losses while keeping pattern effects low. Future designs will include preamplifiers as it is found that the dynamic range remains above 15 dB and adds

only 0.5 dB of excess power penalty for input powers at 0 dBm. In conclusion, an SOA gate matrix switch was fabricated and used to demonstrate that there exists a viable integrated solution for switch design for recirculation buffers at high bit rates.

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