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Heterogeneous Integration at Fine Pitch (≤ 10 µm) using Thermal Compression Bonding

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***Abstract*—The scaling of package and circuit board dimensions is central to heterogeneous system integration. We describe our solderless direct metal-to-metal low pressure (< 70 MPa) and low temperature (< 250 °C) thermal compression bonding (TCB) technique and present preliminary results of dielet (4 – 25 mm^2 area) attach to a rigid Silicon Interconnect Fabric (Si-IF) with up to two levels of wiring (2 – 10 µm pitch). Dielets were attached at a pitch ≤ 10 µm with an inter-dielet spacing of ≤ 100 µm. We show an effective specific contact resistance of < 1 Ω-µm^2 and shear strength of > 20 MPa. The combined reduction of dielet interconnect pitch, dielet-to-dielet spacing and trace pitch will enable a Moore's law for packaging.**

Keywords- Siclicon Interconnect Fabric (Si-IF), interconnect pitch, dielet-to-dielet spacing, thermal compression bonding (TCB), heterogeneous integrations

I. MOTIVATION

Scaling of circuit board is related to the pitch at which dies are connected to the board and today's technology is based on Ball Grid Array (BGA Pitch). While advanced packaging techniques such as Si-Interposers have shown pitches in the 50 µm regime, they constitute an additional packaging level and do not necessarily overcome this BGA pitch limitation [1]. The leading edge solder bump flip chip technology has a bump pitch down to 40 µm [2] in production. Recently, Soussan *et al.* have reported on tin (Sn)-based micro-bump interconnects, with an interconnect pitch of 10 µm [3]. Compared to other type of substrates such as FR4, a Si-based substrate can provide excellent planarity, fine wiring pitch and matched coefficient of thermal expansion (CTE) for Si-based chips [4] though with potentially increased RF losses. These RF losses can be minimized using small inter-dielet spacing. Our approach is to connect dielets directly to a silicon substrate, with a few levels of wiring, at fine pitches.

The conventional bumps and BGA technology use solder materials. The major drawbacks at fine pitch, depicted in figure 1 & 2, are the solder extrusion during thermal compression bonding [5] and the formation of brittle intermetallic compounds [6] at the joints, which pose a reliability problem. During cyclic loading these joints are subjected to high thermal mechanical stresses, which cause joint failures due to fatigue cracking [7]. Replacing the soldered contact with a metal-metal contact would certainly circumvent these issues. However, it is very challenging to obtain a reliable metal-metal bond. From a material perspective Cu is an ideal candidate for direct metal-metal bonding as it exhibits excellent electrical and thermal properties. At the same time, Cu is very prone to oxidation which makes it difficult to bond. Xie et al. have demonstrated 6 µm direct Cu-Cu thermal compression bonding with in-situ formic acid treatment for oxide removal [8]. Finally, molten solder provides self-alignment due to surface tension. We lose this advantage when we eliminate solder and have to rely on accurate placement.

In this work we will present our investigations on metal-metal (Au-capped Cu) direct bonding with contacts at 10 µm pitch along with their electrical and mechanical performance. We will also provide a comparison with the existing interconnect technologies.

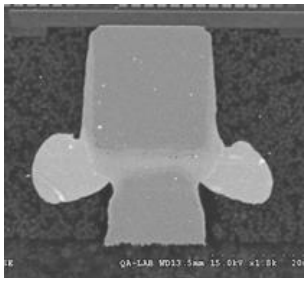

Figure 1. Solder extrusion druing TCB of micro-bumps [5]

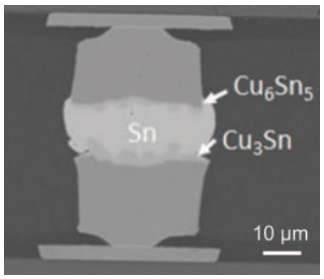

Figure 2. Formation of brittle intermetallics during soldering [6]

II. FINE PITCH INTEGRATION SCHEME

A. *Silicon Interconnect Fabric (Si-IF)*

In order to achieve these goals we introduced a silicon based platform/substrate called the "Silicon Interconnect Fabric (Si-IF)" which allows us to interconnect dies at fine pitch. The Si-IF is fabricated using conventional Si-based BEOL processing with up to four levels of conventional Cu-damascene interconnects with wire pitches in the range of 1 – 10 µm and is terminated with Cu pillars of 2 – 5 µm height & diameter also using a damascene process. The Si-IF replaces both the packaging laminate and the PCB used in the conventional packaging schemes [4] and provides following key advantages:

- Enables fine pitch traces (1 – 5 µm) and fine pitch interconnects (2 – 10 µm).
- Is agnostic to the individual dielet fabrication technology node or semiconductor base i.e. Si, SiC, GaN etc.

- ❖ Can accommodate dielets of various sizes (Edge length: 1 – 5 mm) and thickness (50 – 750 µm)
- ❖ May be enabled with built-in passive and active components
- ❖ Exhibits rigidity and mechanical robustness.
- ❖ Minimizes global thermomechanical mismatch between chips and substrate.
- ❖ Provides good heat dissipation as silicon has good thermal conductivity

A schematic of a Si-IF with mounted dielets is shown in figure 3.

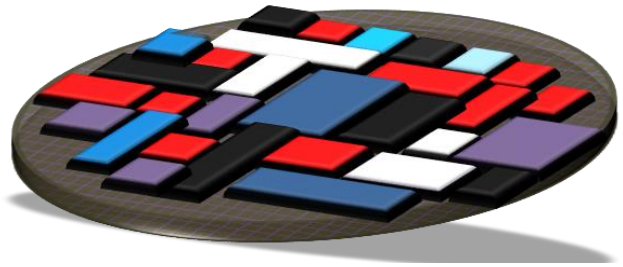

Figure 3. Schematic of a Si-IF with mounted dielets.

B. Fabrication Process and Interconnection Technology in Si-IF

The fabrication process steps of the Si-IF are indicated in figure 4. The test dielets were also prepared in similar fashion but terminated with copper pads (Stop at step 5). The mechanical assembly and electrical interconnection of the dielets to the Si-IF is realized through direct metal-metal thermal compression bonding between Cu-pillar on the SiIF and the Cu-pad on the dielet. We chose this scheme to allow standardization of the pillars on the SIF and this allows us to accommodate heterogeneous dielets from diverse sources. For a successful TCB, the following conditions must be met. The mating surfaces have to be pristine i.e. they must be free of native oxides and other contamination. Furthermore, they have to be atomically flat. Very often moderately rough surfaces come into contact only at their asperities and therefore the ratio of contacting area to total area is very low [9]. While native oxides, contaminations and surface roughness are difficult to modify beyond certain limits, the deformation of the materials can be achieved over wide range by applying external pressure and temperature. At room temperature, limited plastic deformation at surface asperities requires very high bonding pressures. The pressure conditions can be relaxed at higher temperature, where the yield point of the material decreases with increasing temperature [10]. With a suitable combination of pressure and temperature, the material first breaks through any brittle native oxide and deforms plastically at the bonding interface and moves along the surface to fill voids. This helps to bring the two surfaces in the range of interatomic distance. Furthermore, the materials on either side of interface diffuse across the mating surfaces causing grain growth across the interface.

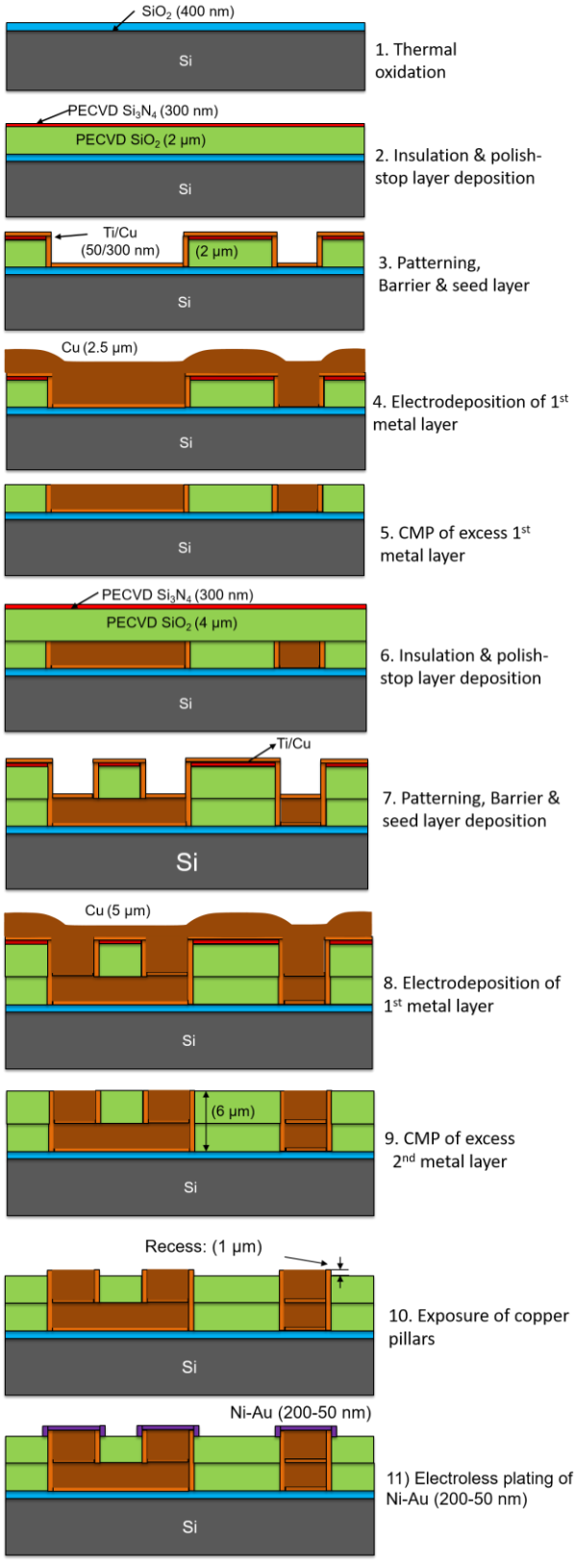

Figure 4. Fabrication process of Si-IF

III. TEST VEHICLES FOR FINE PITCH INTERCONNECTS

The Si-IF in this work, was fabricated using Si-based BEOL processing, as shown in figure 6, with two levels of conventional Cu-Damascene interconnects with wire pitches 2 – 10 µm and is terminated with Cu-pillars (Ø = 5 µm & Pitch = 10 µm) also using a damascene process. The dummy dielets in this study are similarly prepared and contain only one level of wiring, which is terminated with Cu pads. The Cu pillars and pads were capped with Ni-Au to prevent oxidation. Both Si-IF and dielets were designed to form daisy chain to test the electrical continuity. Figure 5 shows the complete fabricated Si-IF. The test Si-IF was designed to accommodate 4 dielets of size (4 mm X 4 mm) with an interconnect pitch of 10 µm and with a total of 640,000 connections. Figure 6 & figure 7 show the micrographs of 1st and 2nd layer of Si-IF respectively. The micrographs of the dielet are depicted in figure 8.

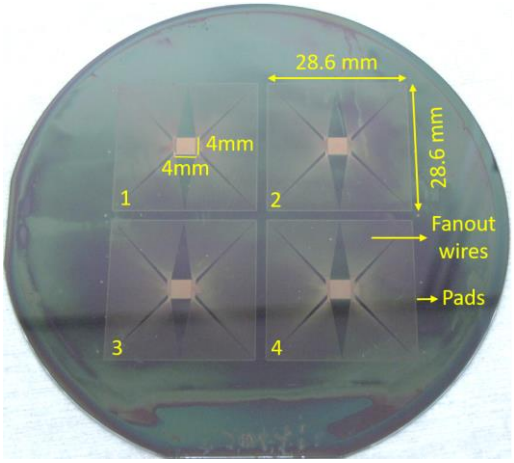

Figure 5. Planer view of fabricated Si-IF with Cu-pillars to accommodate 4 dielets.

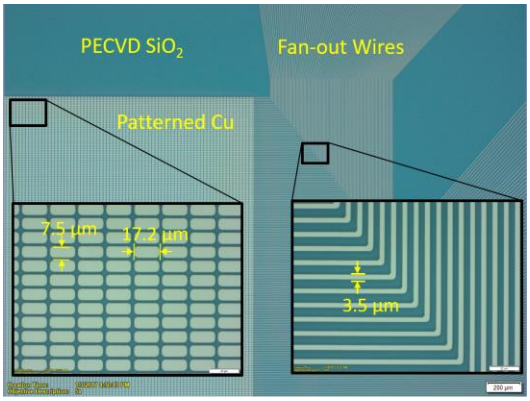

Figure 6. Micrograph of 1st layer of Si-IF showing fine wiring and connecting pads for Cu-pillars

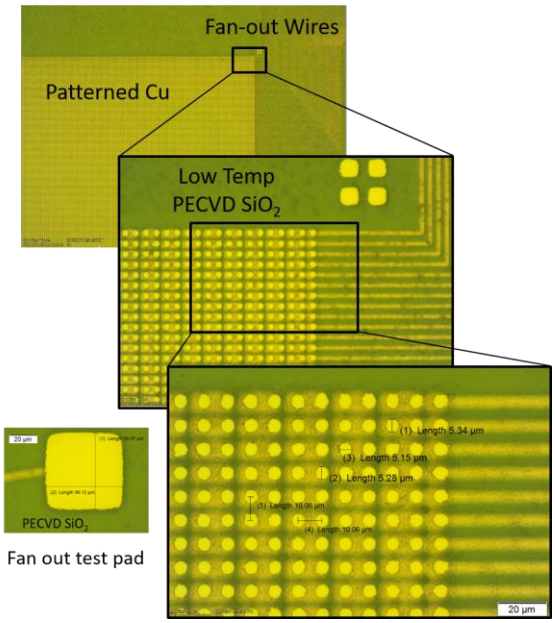

Figure 7. Micrograph of the 2-layer test Si-IF with Cu-pillars (Ø = 5 µm & Pitch = 10 µm). Test pad size is 50X50 µm

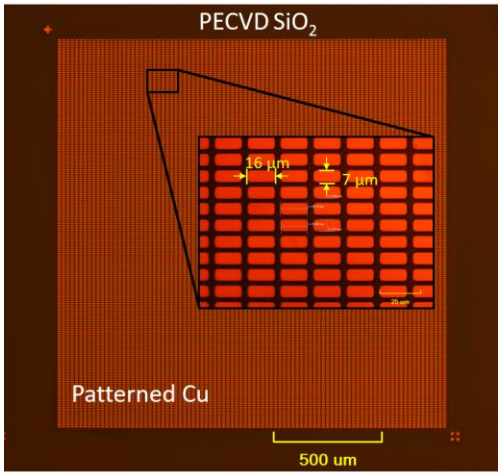

Figure 8. Micrograph of a fabricated test Si-Dielet with die size of 2X2 mm and 10 µm interconnect pitch.

IV. THERMAL COMPRESSION BONDING (TCB)

The thermal compression boding of the test sites was carried out using an optimized *dielet-to-wafer* bonder from K&S, with a potential pillar to pad alignment accuracy of ±1 µm (3-σ) during TCB using alignment marks on both dielet and Si-IF. The schematic of the setup is shown in figure 9 and process parameters are given in table 1.

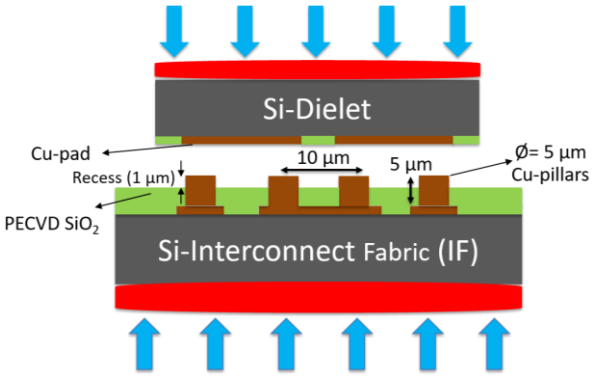

Figure 9. Direct metal-metal bonding between test Si-IF and Si-dielets. Both are bonded in a daisy chain fashion

TABLE I. MATERIALS AND SIZES OF TYPICAL INTERCONNECTS

Process parameters	Value
Bond-head temperature	350 °C
Bottom chuck temperature	120 °C
Bonding pressure	64 MPa
Tacking & Annealing time	20 sec & 8 min
Chamber environment	Air

V. RESULTS AND CHARCTERIZATIONS

A. *Surface Rouhness of CMP Planarized Copper Surfaces*

We described earlier that atomically flat and pristine surfaces with high topographic uniformity is the key to the formation of reliable contact [9] and high throughput. During fabrication of both test Si-IF and dielet wafers, a Chemical Mechanical Planarization (CMP) process was used to achieve surface smoothness on both the Cu-pillars and Cu-pads.

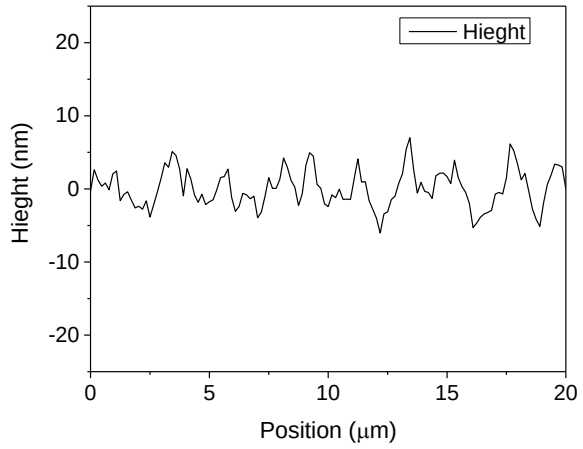

Figure 10. Surface roughness on the Cu surface after CMP process.

The surface roughness was measured using an Atomic Force Microscope (AFM). Figure 10 shows a 1D-scan of the roughness on a 20 µm scan length on the polished copper surface. Here, the average root mean square (rms) roughness was 2.6 nm. This number can be brought down by a factor of 2 with CMP process optimization. The average rms roughness on a non-planarized copper surface after electroplating was found to be 27.3 (±15) nm. After CMP process the average rms surface roughness improved by a factor of 9 i.e. 3.0 (±1.9) nm.

B. *Effect of Native Oxides*

For thermal compression bonding, it is essential to remove the surface contamination and native oxide layer because it can affect the adhesion of mating surfaces. The copper surface is very prone to the formation of surface oxides (e.g. Cu_2O, CuO, etc.) even under normal atmospheric conditions. Furthermore, the rate of oxidation increases with the increase of temperature and time as shown in figure 11. The trends are modelled based on the empirical data taken from [11]–[13]. It indicates that at room temperature (300 K), a 1 nm thick layer of surface oxide forms on bare copper surface within one hour.

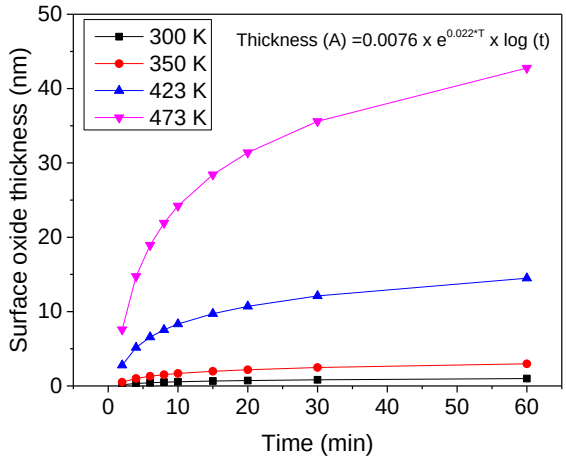

Figure 11. Modelled oxidation rate of copper under combinec influence of temepratuer and time based on impirical data in [11]–[13].

The surface oxidation phenomenon was confirmed by an XRD scan of a bare copper sample before and after acetic acid swabbing. Data indicates that oxide peak intensities are significantly reduced after the swab and but increase with the passage of time even under room temperature conditions. If we extrapolate the trend towards zero minutes after swab, the peak intensities for all oxides peaks will fall to zero as shown in figure 12. In our initial experiments, copper surfaces were cleaned using acetic acid dip for 30 sec prior to the TCB process. Since, the Si-IF remains on the heated chuck (120 °C) at all times, the formation of oxide layer is unavoidable even after the acetic acid swab. This necessitates an in-situ oxide removal technique, such as localized formic acid vapor treatment, which bleeds the

vapor on the copper surfaces on both (Dielet & IF) sides just prior to the TCB.

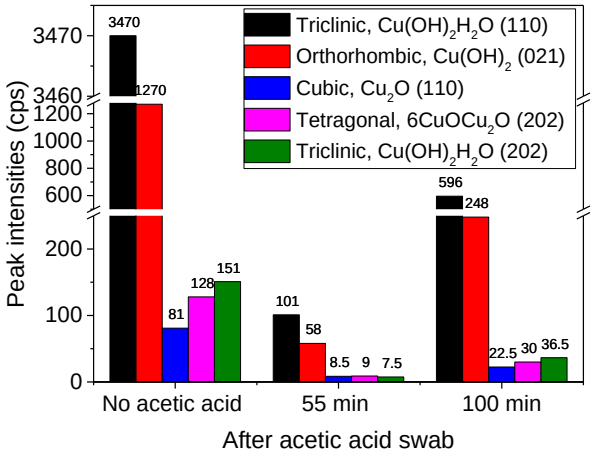

Figure 12. Effect of acetic acid dip on oxide formation on copper at room tempeature. The full widh at half maximum (FWHM) of all the peaks in every case was of the same order.

C. *Electroless Nickel Gold (ENiG) Plating*

Due to difficulties in preventing the oxidation of copper surface, both pillars (Si-IF) and pads (dielet) were capped with thin layers of Ni/Au (200/50 nm). The Ni acts as a diffusion barrier while Au serves as the surface finish layer. Gold is an inert metal and it is free of any native oxides. Both nickel and gold were deposited using electroless plating process.

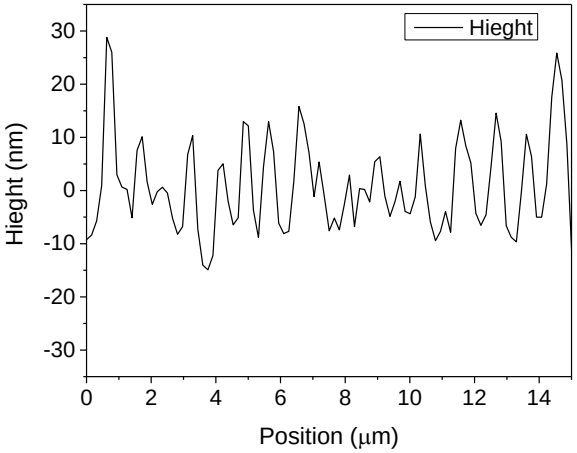

Figure 13. Surface roughness on the Cu surface after CMP process.

The surface roughness of the Au plated on planarized copper surface was measured. The average rms roughness was found to be 9 (±1.5) nm as depicted in figure 13, which was approximately 3 times higher than the polished copper surface. Snugovsky *et al.* have described that under galvanic cell conditions, the electroless Ni deposition process is not properly controlled. A defective Ni microstructure forms inside the nodules, providing channels for the Au plating solution to accumulate. This leads to accelerated corrosion of the Ni and to excessive Au deposition. This phenomenon is called as "Black Pad Formation" [14]. This unfortunately leads to a rough surface and affects the Au-Au effective contact area during TCB.

D. *Shear Strenght of the Bonded Contacts*

While keeping the bonding pressure and bonding temperature constant the shear strength of the bonded samples was measured with different annealing durations. The average shear strength increased with increasing the annealing time as shown in figure 13. The contact area is expected to increase with increasing time as material continues to deform plastically and fills the interfacial gaps. The creep may take place as we continue to apply pressure and temperature simultaneously for long duration [15]. Au-capped copper pillars (Ø = 5 μm) in comparison with solder (Sn) capped copper Cu pillars [16] (Ø = 4 μm) exhibited higher shear strength after annealing for 8 min. The solder bumps in conventional packages are usually surrounded by the underfill material [17], which provides additional mechanical support to the bumps and further increases the shear strength of the dielet. In our case, the Au-capped pillars were not surrounded by any underfill material.

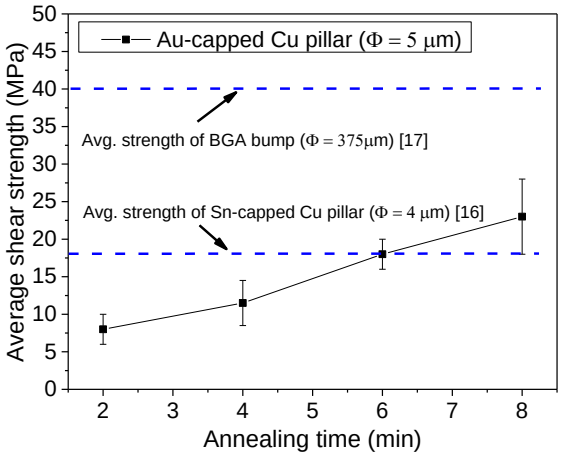

Figure 14. Effect of annealing time on shear strength of bonded interconnect

E. *Alignemnt Accuray*

Alignment accuracy is the key requirement for the bonding of fine pitch interconnects. We were able to achieve ±1 μm alignment overlay accuracy under the bonding conditions in table 1. To optimize the alignment process, both Si-IF and dielets wafers were fabricated with only the top most layers (pillars for Si-IF & pads for Dielets) with alignment marks using thin evaporated layers of Ti/Au (50-200 nm) in a lift-off process. These special test dielets were mounted onto the Si-IF with a short duration of 20 sec while other process parameters were kept the similar. The figure 18 shows a

micrograph of a dielet mounted on Si-If. The dielet was then sheared off the Si-IF and checked for the overlay alignment accuracy as shown in figure 15.

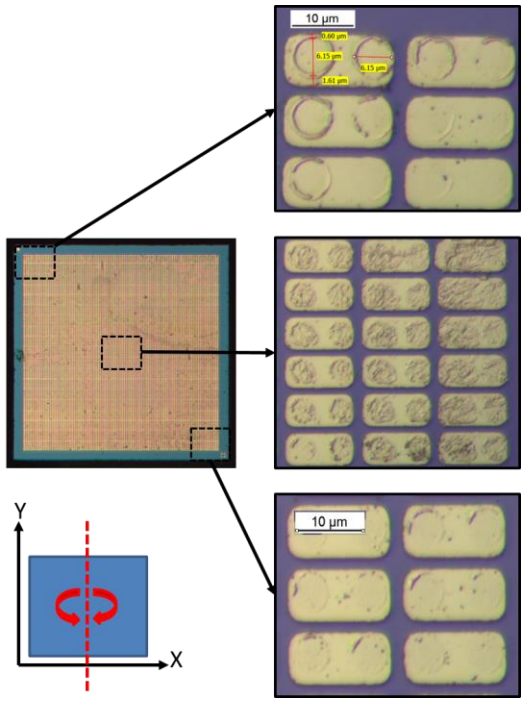

Figure 15. Dielet after shearing off the test Si-IF. An overaly of +1 µm is in x-direction, +0.5 µm in y-direction. Here, rotation of dielet plane around z-axis is about 0.003 deg

F. 100 microns Inter-dielet Distance

In addition to interconnects, we also demonstrated an inter-dielet spacing of 100 µm. This may be reduced to 30 – 50 µm inter dielet spacing. The limiting factors in this case can be the roughness, waviness and chipping of the dielet edges. This can be overcome using sophisticated state-of-the-art dicing techniques such as plasma dicing. The figure 16 shows the complete silicon interconnect fabric with 112 dielets (2 X 2 mm) mounted on Si-IF with an inter-dielet distance of 100 microns, shown in figure 17.

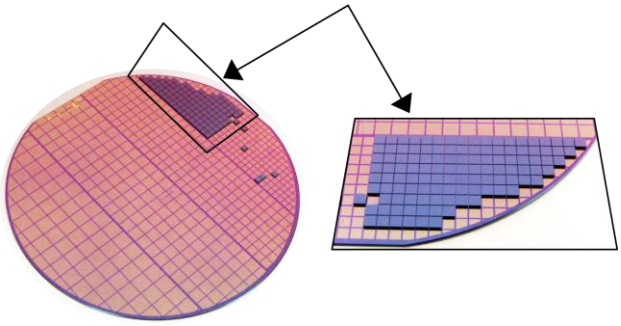

Figure 16. Si-dielets bonded on to Si-IF with 100 µm inter-dielet distance

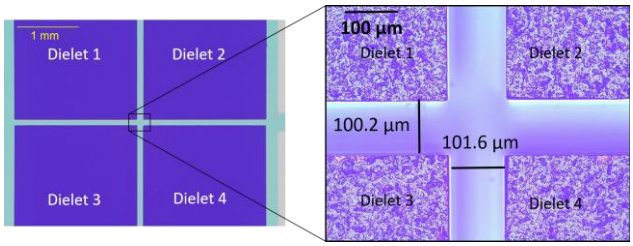

Figure 17. Micrograph of the mounted dielets with 100 µm interdielet distance.

G. Electrical Continuity Tests

Electrical continuity tests were performed after mounting the test dielets on Si-IF to form daisy chains. Each daisy chain is comprised of 400 interconnects as shown schematically in figure 18. The IV-characteristics were measured for daisy chains and the average contact resistance per interconnect (Pillar-to-pad) was found to be a 42 mΩ as shown in figure 19.

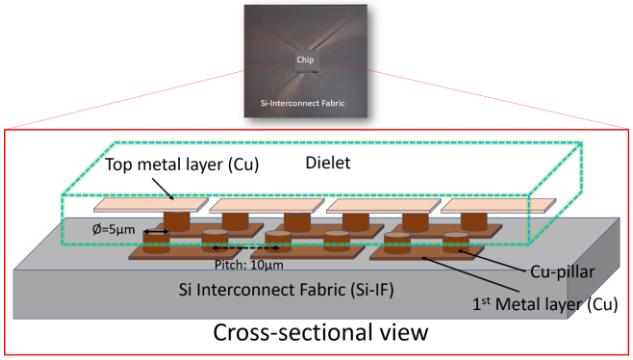

Figure 18. 3D view of a test Si-dielet thermal compression bonded on Si-IF in form of daisy chains. The pillars (Si-IF) & pads (Dielet) are capped with Au.

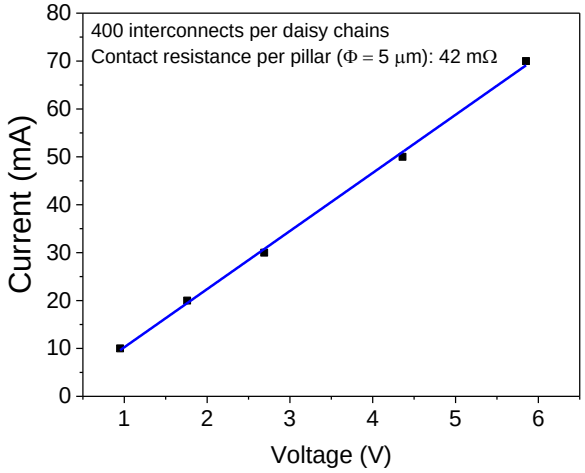

Figure 19. IV-characteristics of a single daisy chain. It includes the resistance of interconnects, pads (Si-IF & Dielet) and the fanout wires.

VI. Discussion & Conclusions

Based on our Fine Pitch Integration (FPI) scheme, we have successfully demonstrated the interconnect pitch of 10 µm and an inter-dielet spacing of 100 µm on a Silicon Interconnect Fabric (Si-IF) using direct metal-metal thermal compression bonding. The dielet-to-interconnect fabric contacts were realized through a state-of-the-art dielet-to-wafer K&S bonder, which can achieve ±1 µm alignment accuracy. We can confidently state that both interconnect pitch and inter-dielet spacing can be further reduced to 2 – 5 µm and 30 – 50 µm respectively. The combined reduction of interconnect pitch, dielet-to-dielet spacing and trace pitch will not only enable a Moore's law for packaging but will also help to improve the overall electrical, thermal, and thermo-mechanical performance on the system level [4].

Our investigations show that for a successful thermal compression bond, mating surfaces should be pristine i.e. free of native oxides and other contaminations and atomically flat. Bare copper surfaces get readily oxidized at even at temperature. In our initial experiments, we swabbed the bare copper surface with acetic acid before the start of bonding process, which leads to the formation of copper acetate. However, prolonged exposure (several minutes) on heated chuck (120 °C) decomposes the copper acetate and copper gets oxidized before the bonding process. This necessitates the inclusion of an in-situ surface cleaning process, such as formic acid vapor bleed just prior to thermal compression bonding. To circumvent the copper oxidation problem, we placed thin capping layers of electrolessly plated Ni-Au. The surface roughness on polished Cu surface (Avg. rms: 3 nm) changed by a factor of 3 i.e. 10 nm after Ni-Au plating. However, under our process conditions [64 MPa, 20 sec (tacking), 8 min (annealing), 350 °C (Bond head), 120 °C (Chuck)], interconnects with contact resistance of 42 mΩ were achieved.

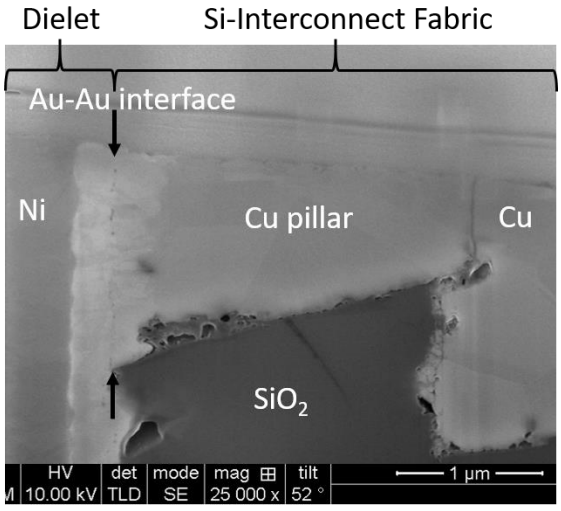

Figure 20. SEM/FIB cross section of a single Si-IF-to-Dielet contact.

Figure 20 shows the cross section of a single contact (Si-IF-to-Dielet). The Au-Au interface has nano-scaled voids present at the interface, which can be reduced by improving the surface roughness and with further annealing. A comparison of interconnect geometries, electrical and material properties with the existing interconnects in state-of-the-art packaging schemes is presented in table II and III.

TABLE II. Geometric and Electrical Properties [18], [19], [20]

Interconnect type	Ø [µm]	Contact pad area [µm^2]	Contact resistance [mΩ]	Effective specific contact resistance [Ω-µm^2]	Material
C4 bump [18]	100	~7800	10	78	PbSn
C4 bump [18]	50	~1950	25	48.7	PbSn,
µ-bump [19]	23	~415	47	19.5	CuSn
µ-bump [19]	16	~201	43	8.64	CuSn
Cu pillar [20]	11.2	~100	12	1.2	Cu
Cu-Pillars	***5***	***~19.5***	***42***	***0.820***	***Au-capped Cu***

TC: Thermal Compression, RS: Reflow Soldering

TABLE III. Key Materail Properties of Interconnect Materails

Interconnect type	Material	Thermal conductivity [W/cmK]	Electrical resistivity [µΩ-cm]	CTE [ppm]
µ-bump	PbSn	57	11	24
	CuSn	34-70	13	20
This work				
Cu-Pillars	***5***	***400***	***1.7***	***16***

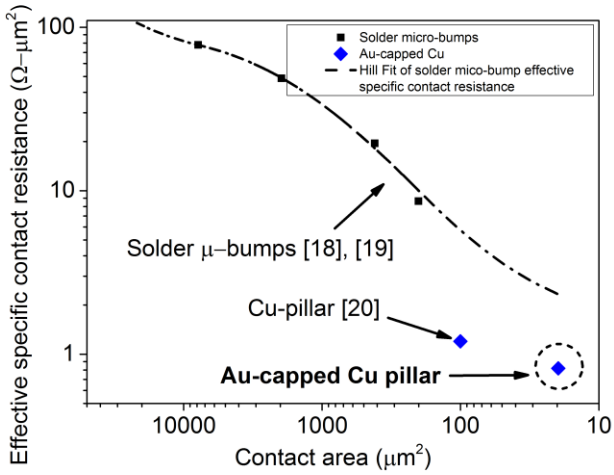

Figure 21. Comparison of effective contact resistacne of solder micro-bumps and Au-capped Cu-pillar

Figure 20 gives a comparison of effective specific contact resistance of solder micro-bumps and Cu-pillars. It can be seen that effective contact resistance of Au-capped copper pillar is 4X smaller than the solder micro-bumps. We ascribe this to current crowding in the larger bumps where

only the perimeter of the large bumps contributes to electrical conduction. In our case, the entire pillar contributes. Compared to solder materials, Cu shows a factor of $6-8$ increment in terms of thermal conductivity while it shows a factor of 7X decrement in electrical resistivity. In our scheme, copper pillars are capped with very thin layer of Ni-Au. According to test standard MIL-STD-883, method 2019.9, all die contact areas larger than $4\ mm^2$ shall withstand a minimum force of 25 N (or 6.25 MPa). In our case, the total contact area under chip was $3.14\ mm^2$. The interconnects exhibited a shear strength of 22 MPa using optimized process parameters as described in table 1. The contacts successfully passed the shear tests and they showed higher shear strength compared to Sn-capped solder joints under optimized process conditions.

VII. Outlook

After successfully demonstrating interconnects at 10 µm pitch using FPI scheme, we are further assessing the electrical, mechanical, thermal properties of these contacts. Focus will be given to the reliability of these contacts and we will develop a model to predict the life time of these metal-metal joints.

VIII. Acknowledgement

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IX. References

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