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DPLL and Energy Harvesting Circuit for Low-Power and Miniaturized System Applications

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DPLL and Energy Harvesting Circuit for Low-Power and Miniaturized System Applications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical & Computer Engineering

by

Chien-Heng Wong

2018

ABSTRACT OF THE DISSERTATION

DPLL and Energy Harvesting Circuit for Low-Power and Miniaturized System Applications

by
Chien-Heng Wong

Doctor of Philosophy in Electrical & Computer Engineering
University of California, Los Angeles, 2018
Professor Mau-Chung Frank Chang, Chair

As fabrication technology improves, computation ability has increased accordingly and enables new applications such as biomedical and health monitoring systems, internet of things (IoT) and home security surveillance. To satisfy stringent requirements such as limited supply, power and area for these new specs of emerging applications, critical circuit blocks must operate under low supply voltage and, if possible, generate power from ambient environments. These new applications can be further popularized if costly off-chip passive components which occupies large PCB footprint can be avoided.

This thesis firstly introduces fundamentals of phase locked loop (PLL) which provides clock to all analog and digital circuits in systems. Then a 0.75V 0.014mm2 2.6GHz digital bang-bang PLL with dynamic double-tail phase detector and supply-noise-tolerant g_m-controlled DCO is proposed. Lastly, this thesis introduces a fully integrated CMOS dual source adaptive thermoelectric and RF energy harvesting circuit with 110mV startup voltage. Both circuits adopt no off-chip devices and can operate under low voltage or harvest energy from ambient environments. The prototype DBBPLL has been implemented in a mainstream 28nm CMOS process and consumes 2.9mW, while achieving low in-band phase noise of -105dBc/Hz. The energy harvester is implemented in 28nm CMOS; it achieves a self-startup voltage of 110mV without RF input and 85mV at -16dBm input. The boost converter power conversion efficiency (PCE) is 25% and the harvester overall PCE is 10%.

The dissertation of Chien-Heng Wong is approved.

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2018

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Chapter 1

Introduction

1.1 MOTIVATION

A compact low-supply-voltage yet low-noise digital bang-bang PLL (DBBPLL) is proposed. The bang-bang phase detector (BBPD) in this work is based on a dynamic double-tail latch which enables high time-to-voltage gain and low input-referred noise under tight power supply headroom. The ring-based digitally-controlled oscillator (DCO) is made of multiple g_m-controlled delay units and a constant-g_m-biased current digital-to-analog converter (DAC). By combining these two blocks, the DCO can now better tolerate supply noise and process variations. A prototype DBBPLL has been implemented in a mainstream 28nm CMOS process with compact die area of 0.014mm^2. When operating at 2.6GHz, it consumes 2.9mW with 0.75V supply and achieves low in-band phase noise of -105dBc/Hz.

Besides, a fully integrated dual source adaptive thermoelectric and RF energy

harvesting circuit is presented. Its boost oscillator, rectifier and boost converter all operate at RF frequency to make inductor and capacitor integration feasible. The oscillator G_m adaptive bias reduces current consumption at higher voltage while assists startup at lower voltage. The RF input signal further reduces startup voltage through Q-enhanced amplification and super-regenerative mode. Implemented in 28nm CMOS, it achieved a self-startup voltage of 110mV without RF input and 85mV at -16dBm input. The boost converter power conversion efficiency (PCE) is 25% and the harvester overall PCE is 10%.

1.2 THESIS OVERVIEW

This thesis is divided into four chapters. In Chapter 2, an overview of phase-locked loop is introduced, including the linear model and considerations of parameter decision. Further, the noise analysis of PLL is discussed for acquiring more insight of PLL design. The design and analysis of a 0.75V 0.014mm^2 2.6GHz digital bang-bang PLL with dynamic double-tail phase detector and supply-noise-tolerant g_m-controlled DCO is presented in Chapter 3. A fully integrated 28nm CMOS dual source adaptive thermoelectric and RF energy harvesting circuit with 110mV startup voltage is presented in Chapter 4.

Chapter 2

Elements of Phase-Locked Loop

2.1 INTRODUCTION

Many digital and analog systems use phase-locked loops (PLLs) as a general mixed-signal block to generate clock. In wireless communication systems such as WiFi or bluetooth, PLL is used to synthesize associated carrier frequency. They are used to select different channels for both sides of modulator/demodulator (MODEM). In wireline system such as DDR or PCIE, PLLs are used for generating precise edge to sample transmitted data. As a result, PLLs are enabling building blocks for many electronic devices nowadays like wearable devices or biomedical applications. This chapter introduces an overview of PLLs. Basic concept is introduced firstly, then mathematical derivation. At last we derive analysis of noise response, giving an insight to the elementary design of PLLs.

2.2 PHASE-LOCKED LOOP

2.2.1 Simple PLL topology

From [1], [2] and [3], PLLs uses a given frequency or phase information to track its output which may be from VCO or DCO to synthesize a specific frequency in a feedback way. PLL will act to alter frequency or phase of VCO or DCO to keep it align to input reference clock and decrease phase error. The input phase error between VCO's or DCO's output signal and the input reference clock approaches to zero, or stays constant after PLL act to correct them. Under such situation, the phase of VCO's or DCO's output signal are actually locked to the phase of the reference signal, so as to the frequency or its associated harmonic tones.

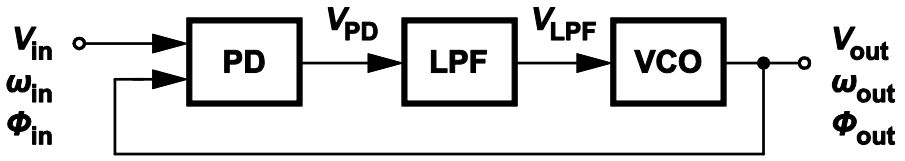

Fig. 2.1 Simple PLL topology.

A simple PLL is made up of a phase frequency detector (PD), a low pass filter (LPF), and a voltage-control oscillator (VCO) which is shown in Fig. 2.1. As the phase difference between the inputs varies, so does the value of the output of the PD,

and provides a dc level proportional to the phase difference. The operation of PD is similar to that of differential amplifiers in that both sense the difference between the two inputs, generating a proportional output to the low-pass filter. The LPF suppresses the high-frequency components of the PD output, generating the dc value to control the VCO frequency. The VCO then oscillates at a frequency equal to the input frequency with a constant phase difference.

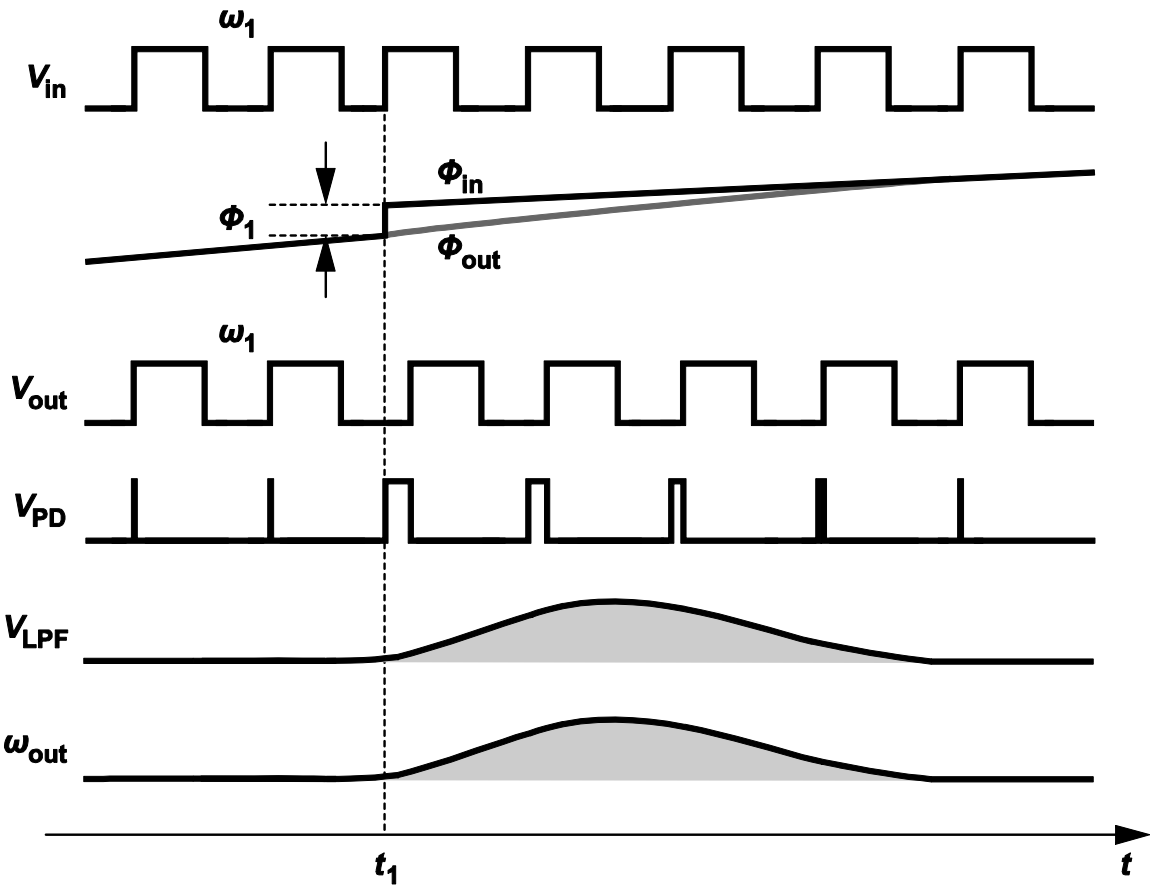

Fig. 2.2 Response to a PLL to a phase step.

According to [1], [2] and [3], Let us now analyze the response facing small phase transients at the input when a PLL is in locked condition. Consider a PLL in the locked condition and both the input and output frequencies are ω1. Suppose, as shown in Fig. 2.2, according to [2] and [3], the input experiences a phase step of ϕ_1 at $t = t_1$. Since the output of the LPF does not change instantaneously, the VCO initially continues to oscillate at ω_1. The growing phase difference between the input and output then creates wide pulses at the output of the PD, forcing V_{LPF} to rise gradually. As a result, the VCO frequency begins to change, attempting to minimize the phase error. When the loop returns to lock, ω_{out} goes back to ω_1, requiring that V_{LPF} and hence $\phi_{out} - \phi_{in}$ also return to their original values. The exact settling behavior of PLLs depends on the various loop parameters and will be quantified in next section.

2.2.2 Linear model of PLL

Although PLLs are highly nonlinear systems, it has been observed that when they are in lock, their transient behavior can be reasonably well approximated by linear differential equations. Indeed, analysis methods similar to those first developed to describe PLLs have now been applied to other important nonlinear systems such as adaptive filters and switching power supplies. Thus, understanding the small-signal

modeling of PLLs can be very useful in understanding many important signal-processing systems.

A typical PLL controls the loop dynamic and generates an output signal synchronous with the reference signal by negative feedback. As shown in Fig. 2.1, the PLL is composed of PFD, CP, LPF, VCO, and a frequency divider. Assuming that the PLL is in locked condition, it means that the two inputs of the PFD have the same frequency and phase under ideal condition. As a result, the frequency of output of the VCO is N times to the reference signal. N is the divide ratio of the frequency divider. To construct the linear model from Fig. 2.1, the function of the building blocks in the PLL will be discussed below.

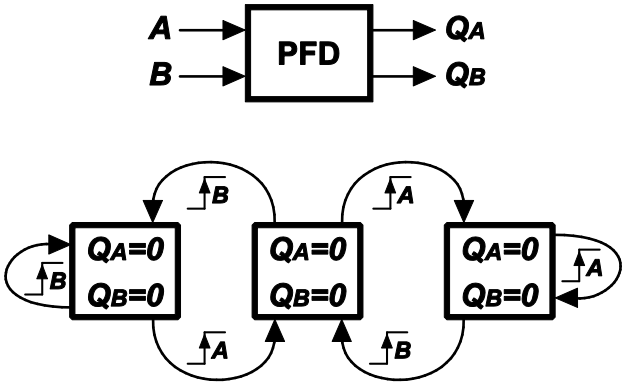

Fig. 2.3 PFD and its state function figure.

The PFD is extensively used in the PLL to detect the phase and frequency

difference of the reference and feedback signals. Fig. 2.3 illustrates state machine figure of a PFD with two periodical inputs and it is similar to a tri-state machine. When the PFD senses a rising edge at A, the state moves from state 2 to state 0 or from state 0 to state 1. When the state is state 1, a rising edge at A cannot alter the state anymore. At this moment, when a rising edge of B arrives, it moves state 1 to state 0. Fig. 2.4(a) shows the timing chart stated above and it can be found that the phase difference between A and B can be detected. Besides, Fig. 2.4(b) shows the timing chart when the frequency of the two inputs are different. The PFD stay in the state 0 and state 1 more than in state 2 Assuming that the frequency of A is higher than B. Consequently, the mean level of Q_A is higher than Q_B and the frequency difference can be detected, too. Fig. 2.5 shows the characteristic figure of the PFD.

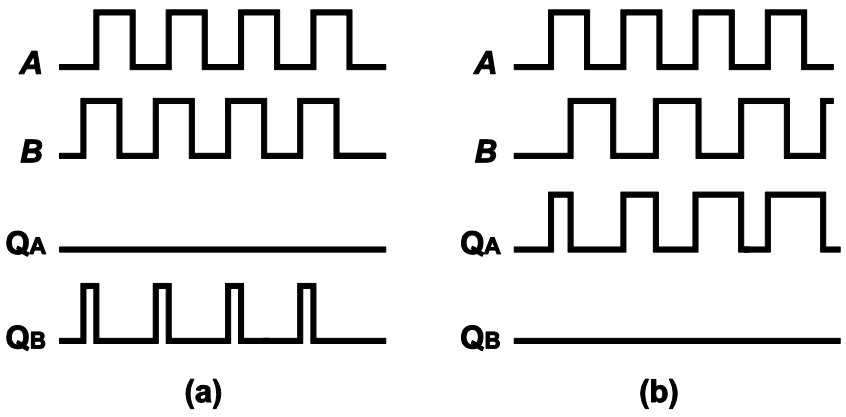

Fig. 2.4(a) Timing chart of PFD while A lags to B. (b) Timing chart while $\omega_A > \omega_B$.

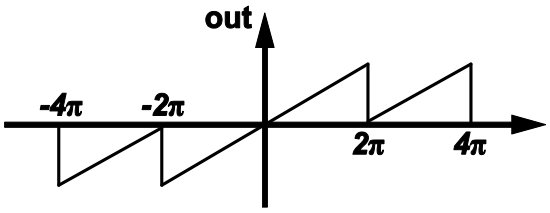

Fig. 2.5 Characteristic of PFD.

The PFD cannot offer a precise signal proportional to the phase difference because the output of PFD is in the form of pulse width. For this reason, CP is added to transform the pulse width into the current signal. Fig. 2.6(a) shows a circuit composed of a PFD and a CP and Fig. 2.6(b) shows its timing chart. When A leads B, the CP generates a constant periodically and charges the C_p making a constant increasing in voltage. Therefore, the relation between PFD and CP can be derived as

$$I_{pump} = I \cdot \frac{\phi_e}{2\pi}. \tag{2.1}$$

I_{pump} is the output of CP, is the phase difference between A and B, and I is the CP current source. Because of that the combination of the PFD and the CP is a discrete-time system; it can be approximated to a linear system only if the loop bandwidth is low enough compared to the reference frequency.

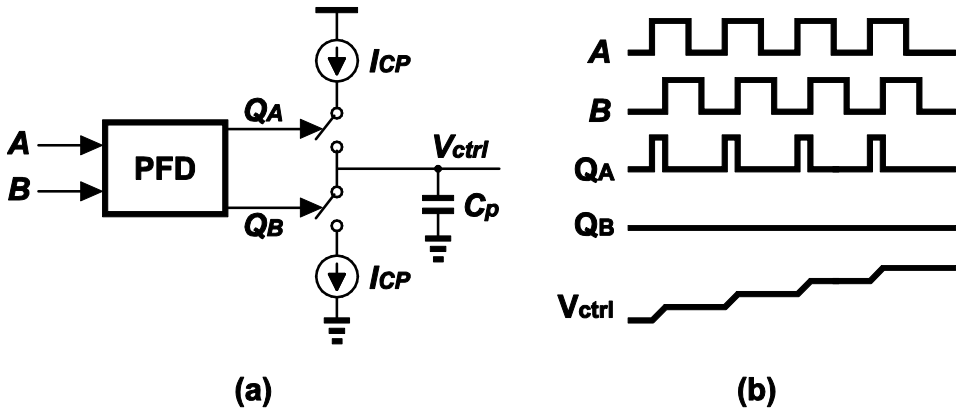

Fig. 2.6(a) PFD, CP, and filter. (b) Timing chart when A leads to B.

A passive filter is needed to add after the CP to transform the current signal to the voltage signal and filter out high-frequency noise. If a capacitor is simply adopted, it will cause close-loop unstable. To solve this problem, add a resistor R_p in series with the capacitor C_p can generate a left-side zero shown in Fig. 2.7(a). However, it may still face the unstable problem due to the nonideal effect. Besides, the output of the filter has serious ripple problem because of the uncontinuous changing in voltage illustrated in Fig. 2.7(b). The PLL system may fail to lock if the ripple caused by I_pR_p drop over the operating range of VCO or frequency divider. To relieve the issue, add a smaller capacitance in parallel with the original filter and turn it into a 2^{nd} order loop filter shown in Fig. 2.8.

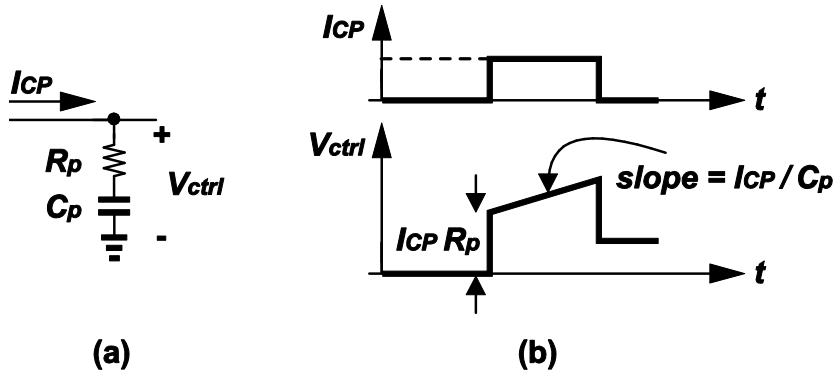

Fig. 2.7(a) First order filter. (b) Transient response of first order filter.

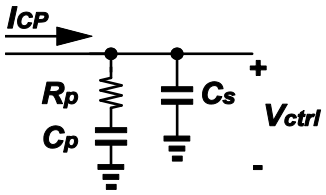

Fig. 2.8 Second order filter.

For an ideal VCO, its relation between input and output frequency can be represented in the following equation:

$$\omega_{VCO} = \omega_{FR} + 2\pi \cdot K_{VCO} \cdot V_{ctrl}. \tag{2.2}$$

In the (2.2), ω_{FR} represents the frequency of VCO when input voltage is 0; K_{VCO} represents the gain of the VCO. Due to that the phase can be acquired by the integration of frequency, the phase output of the VCO can be denoted as

$$\phi(t) = \phi_0 + \int_{-\infty}^{t} \omega(t) \tag{2.3}$$
$$\omega(t) = \frac{d\phi(t)}{dt}$$

In the (2.3), $\phi(t)$ corresponding to the phase of the signal; ϕ_0 represents the initial phase; $\omega(t)$ is the frequency in radius. Therefore, the output of an ideal VCO can be expressed as

$$y(t) = A \cdot \cos[\omega_{FR} t + 2\pi \cdot K_{VCO} \int_{-\infty}^{t} V_{ctrl}(t) dt]. \tag{2.4}$$

By the (2.4), it can be observed that the VCO is actually an integrator. Consequently, the transfer function of the VCO in phase can be represented as

$$\frac{\phi_{out}}{V_{ctrl}}(s) = \frac{2\pi \cdot K_{VCO}}{s}. \tag{2.5}$$

2.2.3 Dynamics of PLL

After analyzing every blocks used in the PLL, a phase-domain linear model of PLL can be constructed. The PFD can be seen as a subtractor subtracting the reference signal from the feedback signal. The CP can be taken as a constant gain. The VCO can be taken as a integrator with a constant gain. And divider is seen as a constant gain. By the statement above, the linear model of PLL is shown in Fig. 2.9.

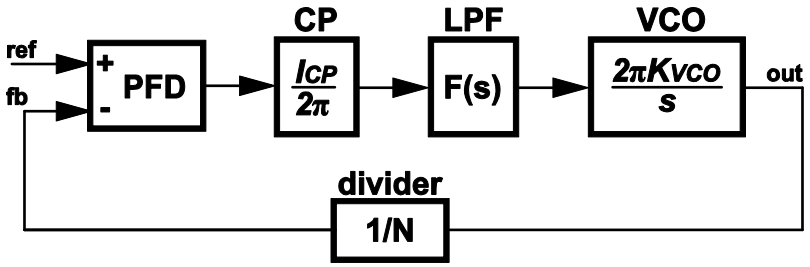

Fig. 2.9 Linear model of PLL.

The unit in Fig. 2.9 is rad/s, ϕ_e represents the difference between reference phase ϕ_{ref} and feedback phase ϕ_{fb} ,and The CP converts the ϕ_e into current. Consequently, the gain of PFD and CP is $K_{\mathrm{PD}}(I_{\mathrm{CP}}/2\pi)$. The output of CP is then converted into the voltage signal for the VCO generating the output signal. The VCO can output a stable frequency signal by the feedback mechanism of the control system. Besides, the (1/s) in the VCO means the integration from frequency to phase. As a result, the open loop transfer function of the Fig. 2.9 can be derived as

$$G(s) = K_{PD} \cdot F(s) \cdot \frac{2\pi \cdot K_{VCO}}{s} \cdot \frac{1}{N} = \frac{I_{CP} \cdot F(s) \cdot K_{VCO}}{s} \cdot \frac{1}{N}. \tag{2.6}$$

If the filter shown in Fig. 2.7(a) is adopted, (2.6) can be altered into

$$G(s) = \frac{I_{CP} \cdot K_{VCO}(1 + s \cdot R_p C_p)}{s^2 \cdot N \cdot C_p} = \frac{I_{CP} \cdot K_{VCO} \cdot R_p}{N} \cdot \frac{s + \omega_z}{s^2}. \tag{2.7}$$

ω_z in (2.7) is $1/R_{\mathrm{p}}C_{\mathrm{p}}$. Furthermore, the unity gain bandwidth K can be defined as the frequency where the open loop gain is 1. Because of that the K is usually much bigger than ω_z, K can be derived as bellows,

$$G(s) = \frac{I_{CP} \cdot K_{VCO} \cdot R_p}{N} \cdot \frac{s + \omega_z}{s^2} \approx \frac{I_{CP} \cdot K_{VCO} \cdot R_p}{N} \cdot \frac{1}{s} = 1 \quad (2.8)$$
$$\Rightarrow K \approx \frac{I_{CP} \cdot K_{VCO} \cdot R_p}{N}$$

As a result, the open loop transfer function can be simplified as

$$G(s) = K \cdot \frac{s + \omega_z}{s^2}. \quad (2.9)$$

The frequency response is shown in Fig. 2.10. The x-axis is normalized to *K*, and the zero is put on the one-tenth of *K*. If the zero is not low enough, it may cause unstable condition. Consequently, the position of zero is usually low enough or increasing unity gain bandwidth for better phase margin.

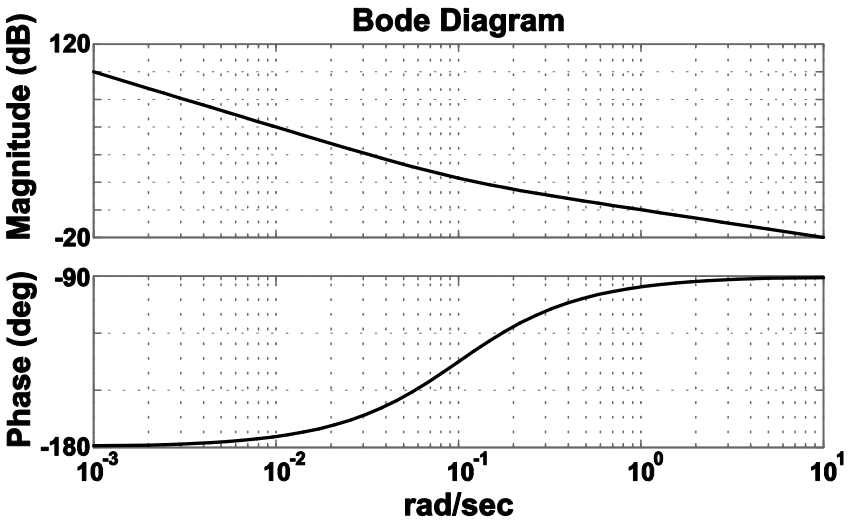

Fig. 2.10 Frequency response of first-order PLL.

2.2.4 Noise Response of PLL

Indicated in Fig. 2.11, there are several noise sources in a PLL based frequency synthesizers such like divider/reference jitter, $\Phi_{jit}[k]$ corresponding to noise-induced variations in the transition time of the input reference clock or divider output signal. Periodic reference spur, $E_{spur}(t)$ caused by current mismatch in charge pump or other affect such as charge injection and charge sharing. Charge pump noise, $I_{cp}(t)$ induced by the transistors that construct the charge pump circuit. Finally, VCO noise, $\Phi_{vn}(t)$ caused by the intrinsic noise of the VCO and voltage noise at the output of the loop filter. Besides, from (2.6) the closed-loop transfer function H(s) can be written as

$$H(s) = \frac{\phi_{out}}{\phi_{ref}} = \frac{A(s)}{1 + A(s)}. \tag{2.10}$$

H(f) equals to 1 at dc and approximates 0 as frequency increase infinitely, this implies that H(f) is a low-pass filter.

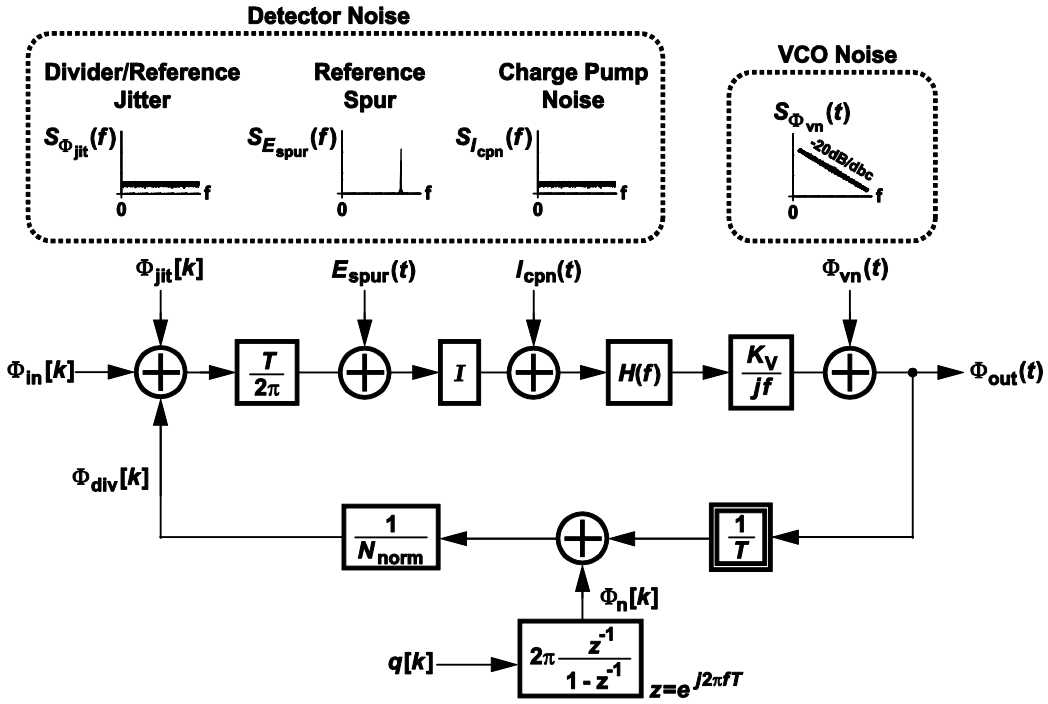

Fig. 2.11 A linear model of PLL-based frequency synthesizers including various noise sources.

As shown in Fig. 2.11, the noise sources have been classified into two categories, VCO noise and detector noise. This comes from the reason that divider/reference jitter, reference spur and charge pump noise all interacts with a low pass filter to the frequency synthesizer output. On the contrary VCO noise interacts with a high pass filter to the frequency synthesizer output.

From (2.10), Fig. 2.11, and [?], the detector noise, VCO noise and their effect on the frequency synthesizer output can be derived as follow

$$S_{\Phi_{out}}(f)\Big|_{\text{Detector Noise}} = S_{\Phi_{out}}(f)\Big|_{\text{Divider/Reference jitter}} + S_{\Phi_{out}}(f)\Big|_{\text{Reference Spurs}} + S_{\Phi_{out}}(f)\Big|_{\text{Charge Pump}}, \tag{2.11}$$

Where

$$\begin{cases} S_{\Phi_{out}}(f)\Big|_{\text{Divider/Reference Jitter}} = \left|T \cdot N_{\text{nom}} \cdot G(f)\right|^2 S_{\Phi_{jit}}(f) \\ S_{\Phi_{out}}(f)\Big|_{\text{Reference Spurs}} = \left|2\pi \cdot N_{\text{nom}} \cdot G(f)\right|^2 S_{E_{spur}}(f) \\ S_{\Phi_{out}}(f)\Big|_{\text{Charge Pump}} = \left|\frac{2\pi N_{\text{nom}}}{I} \cdot G(f)\right|^2 S_{I_{cpn}}(f) \end{cases}, \tag{2.12}$$

and

$$S_{\Phi_{out}}(f)\Big|_{\text{VCP Noise}} = \left|1-G(f)\right|^2 S_{\Phi_{vn}}(f). \tag{2.13}$$

Furthermore, from (2.10) and Fig. 2.11, the effect of sigma-delta modulator output quantization noise on the frequency synthesizer output can be derived as

$$\begin{aligned} S_{\Phi_{out}}(f)\Big|_{\text{Quantization Noise}} &= \frac{1}{T} \cdot \left|T \cdot G(f)\right|^2 \left|2\pi \frac{e^{-j2\pi fT}}{1-e^{-j2\pi fT}}\right|^2 S_q(f) \\ &= \frac{1}{T} \cdot \left|T \cdot G(f)\right|^2 \cdot (2\pi)^2 \cdot \left(2\sin(\pi fT)\right)^{2(L-1)} S_{e_L}(f) \end{aligned}. \tag{2.14}$$

Shown in (2.14), the effect of output quantization noise of an L^{th}-order sigma-delta modulator on the synthesizer output reduces in order by one. This comes from the integrating operation of divider. Finally, the total output noise can be derived by summing up (2.11), (2.13) and (2.14),

$$S_{\Phi_{out}}(f)\Big|_{\text{Total Noise}} = S_{\Phi_{out}}(f)\Big|_{\text{Detector Noise}} + S_{\Phi_{out}}(f)\Big|_{\text{VCO Noise}} + S_{\Phi_{out}}(f)\Big|_{\text{Quantization Noise}}. \tag{2.18}$$

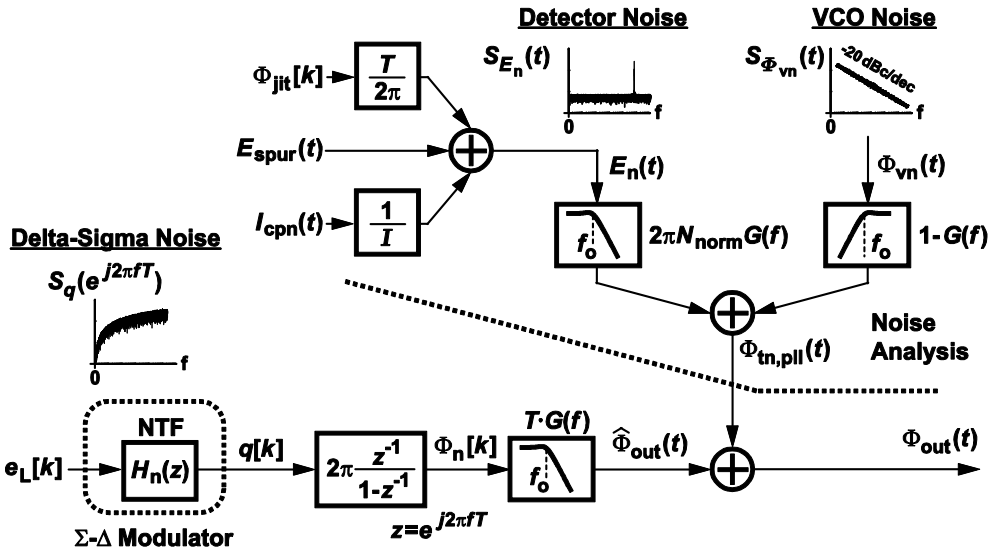

Fig. 2.12 A parameterized model of a PLL-based frequency synthesizer.

Fig. 2.12 shows a parameterized model of sigma-delta fractional-*N* frequency synthesizers, including quantization noise, VCO phase noise and detector noise and their effect on the frequency synthesizer phase noise performance. With the aid of various noise spectrum derived earlier, Fig. 2.13 shows an example of a frequency synthesizer output phase noise diagram. A frequency synthesizer with 400 kHz bandwidth and 20 MHz input reference clock is examined. In Fig. 2.13, the blue line represents the impact of VCO noise at the synthesizer output, by modeling VCO noise as a -20 dB/decade slope curve with a spot noise of -120 dBc/Hz at 1 MHz offset frequency. The actual VCO deviates from the -20 dB/decade rolloff at low frequencies due to 1/f noise, and at high frequencies due to a finite noise source. The green line represents the detector noises, in this example reference spurs is neglected and the

detector noise is modeled as a -90 dBc/Hz white noise. As mentioned before the detector noise interacts with a low pass filter before reaching the synthesizer output. Shown in Fig. 2.13, the influence of detector noises dominates at low offset frequencies, and the influence of VCO and quantization noise dominates at high offset frequencies. Fig. 2.14 shows phase noise result for PLL without delta-sigma modulator and considering noise variation of 5% for both detector and VCO noise, assuming that PD contribute -110dBc/Hz in-band noise and VCO has -90dBc/Hz at 1MHz offset frequency.

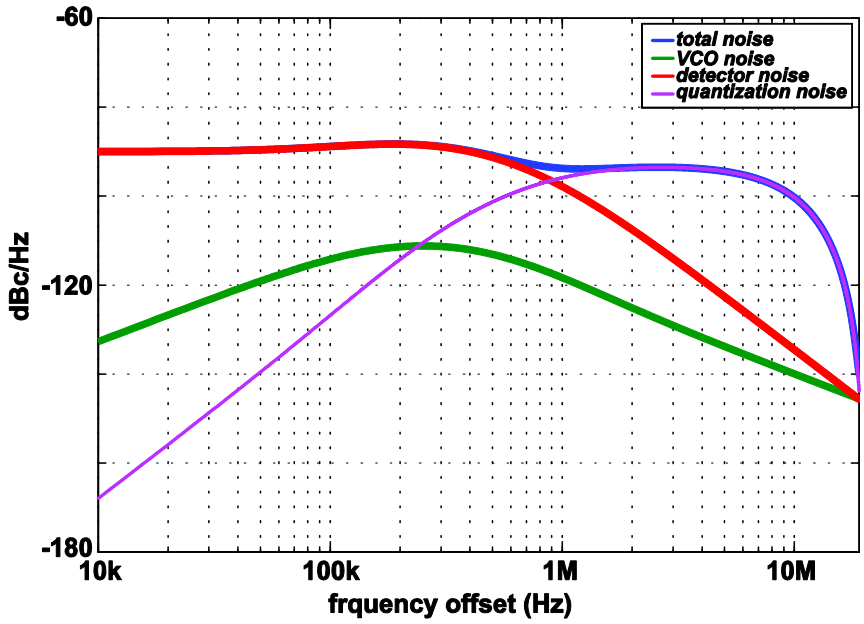

Fig. 2.13 Output phase noise of the frequency synthesizer.

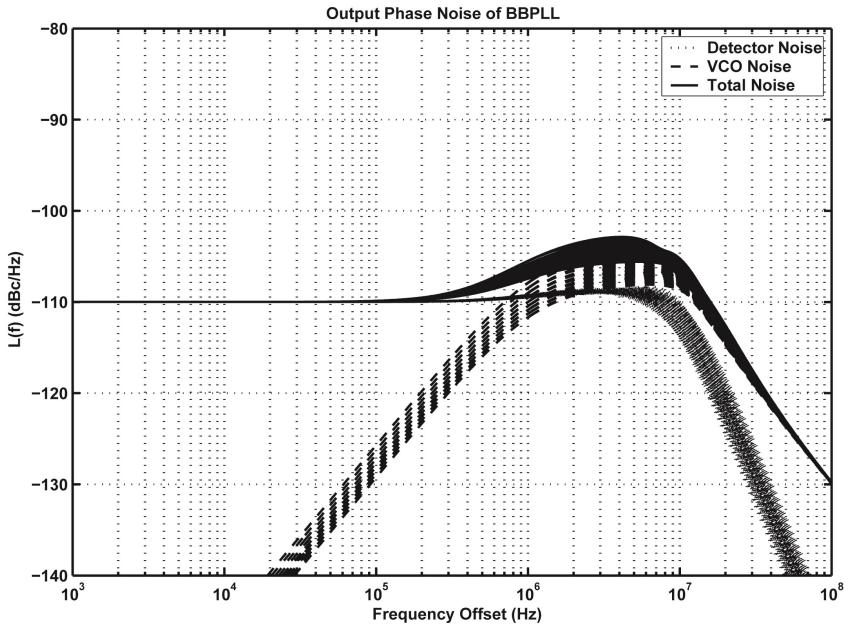

Fig. 2.14 Output phase noise of -110dBc/Hz in-band noise and -90dBc/Hz at 1MHz offset frequency VCO noise with 5% variation.

2.2 BEHAVIORAL MODLE

To verify the viability of PLL with specific parameters, a behavioral model needs to be established to reconstruct transient response. Especially when a new architecture is adopted such as digital filter, time-to-digital converter or bang-bang phase detector (BBPD). To begin with, each sub block in PLL is emulated in C code through the mathematical derivation obtained from previous sections. Fig. 2.15 shows a schematic of a PLL. It uses a BBPD as its phase detector. A proportional and an integral path combined as a digital low pass filter. With arbitrary selected initial condition, we can

start to run transient simulation and get phase noise results by doing Fourier transform of output signal as Fig. 2.16. By adding an 8-bit digital-to-time converter to cancel quantization noise, a fractional-N frequency synthesizer behavioral model can be implemented and its phase noise result is shown as Fig. 2.17.

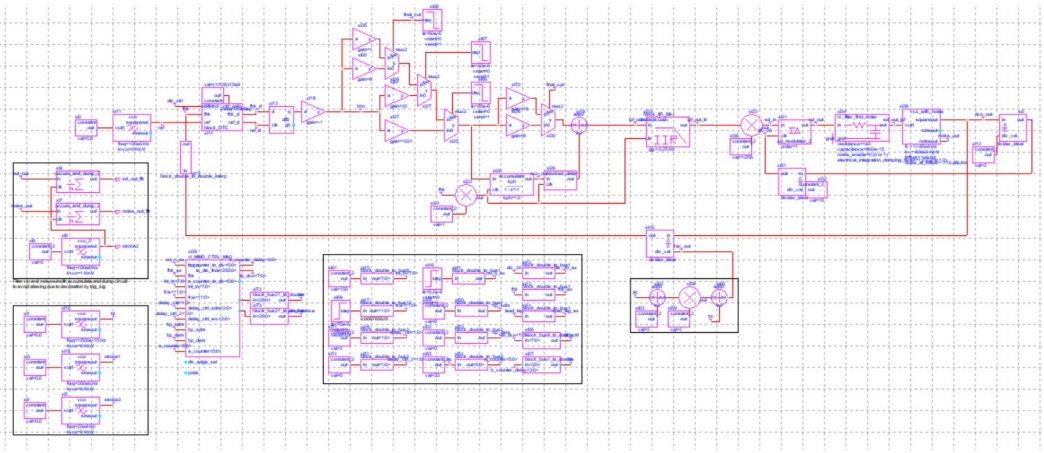

Fig. 2.15 Behavioral model of PLL with bang-bang phase detector.

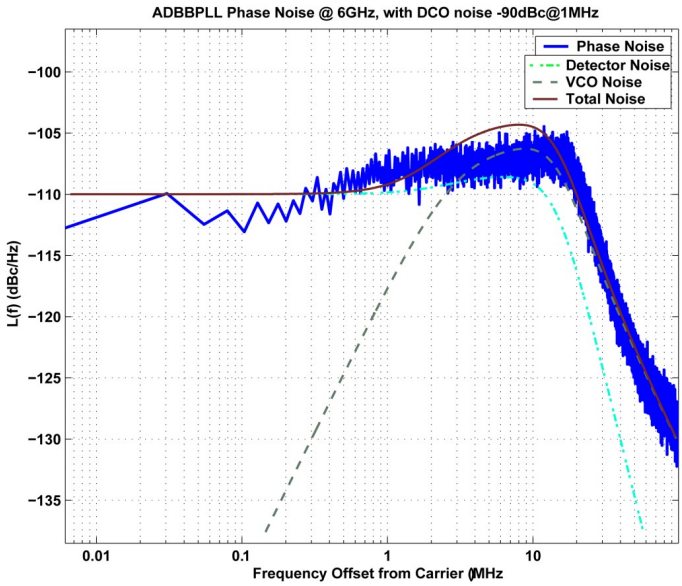

Fig. 2.16 Phase noise result from behavioral model based on Fig. 2.14 parameters.

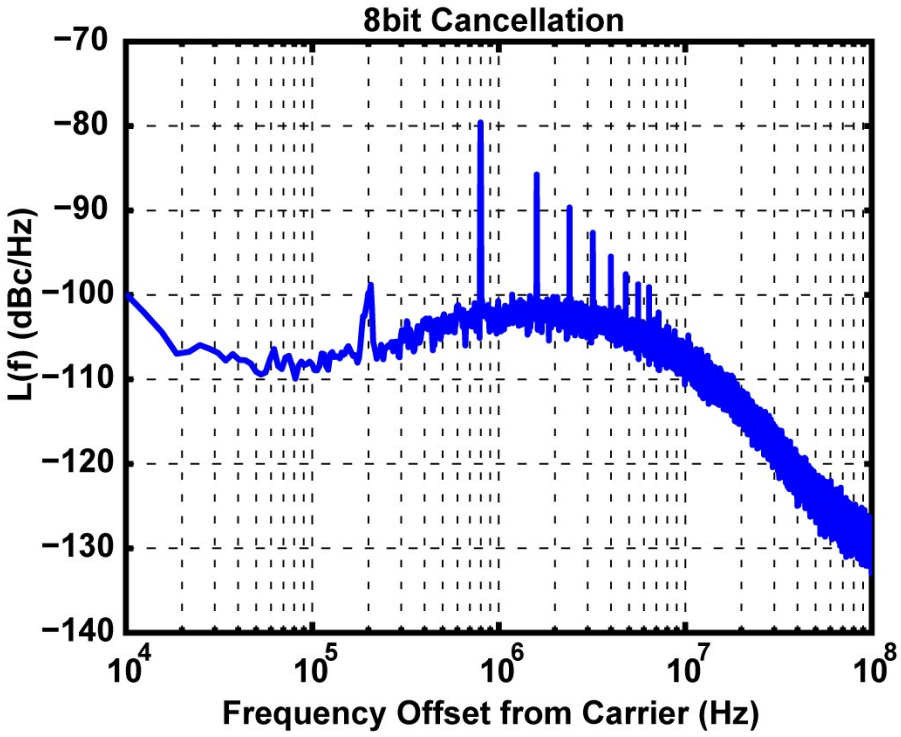

Fig. 2.17 Phase noise of fractional-N PLL with 8-bit DTC quantization noise cancellation.

Chapter 3

A 0.75V 0.014mm^2 2.6GHz Digital Bang-Bang PLL with Dynamic Double-Tail Phase Detector and Supply-Noise-Tolerant g_m-Controlled DCO

3.1 INTRODUCTION

Conventional charge-pump-based PLL utilize passive components for low pass filter which occupies large area as can be seen in Fig. 3.1. The BW is difficult to be tuned under such architecture and it needs higher supply for charge pump which needs cascade to boost output impedance. Digital phase-locked loops (DPLL) have drawn increasing attention recently due to advantages in employing area/energy-efficient digital cells. DPLLs' non-idealities can also be calibrated more effectively in the digital domain. As a result, the DPLLs are preferred choices in realizing modern chip-to-chip communications [12], wearable devices, internet of things (IoT) and biomedical systems for low-power, small-area, and PVT-tolerant operations. DPLL

can be used in both wireline and wireless system as can be seen in Fig. 3.2 and Fig. 3.3. Nevertheless, the interface that converts between analog and digital signals in DPLL, such as time-to-digital converters (TDCs) and DCOs, have become the primary bottleneck for achieving high performance DPLL.

Many techniques have been proposed to achieve high resolution in the TDC, such as Vernier comparison [4], time amplification [5], and gated ring oscillator [6], but at the cost of excessive power/area consumption and design complexity. Consequently, the bang-bang phase detector (BBPD), which has a simpler architecture and less power consumption, is a more practical way to overcome these limitations. However, the D flip-flop (DFF) typically used as the BBPD may often be meta-stable when both input clock edges are in close proximity and greatly degrades the in-band noise of the digital PLL.

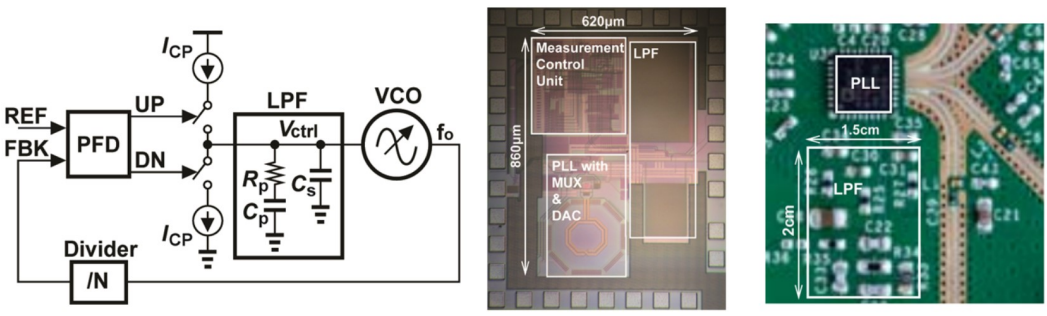

Fig. 3.1 Conventional analog PLL with passive components.

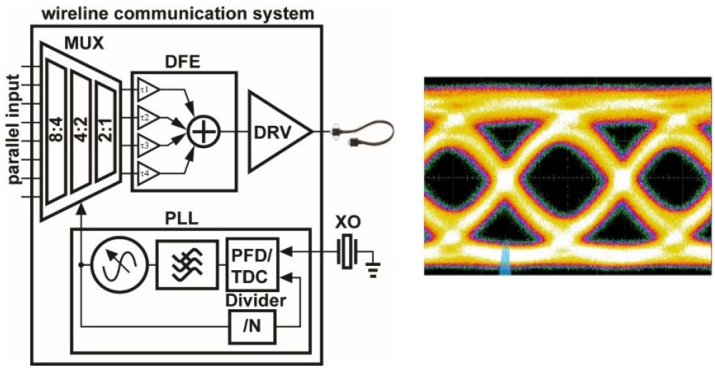

Fig. 3.2 PLL in wireline system.

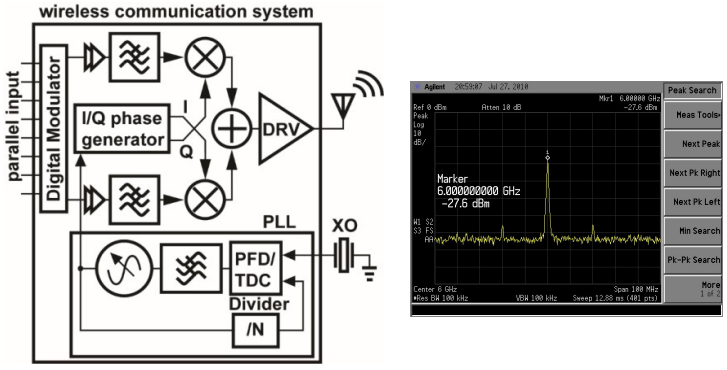

Fig. 3.3 PLL in wireless system

The design of DPLL's key building block DCO imposes a further challenge. Although the ring oscillator may be more cost/area-effective and thus the preferred choice for many future applications, a few design and performance issues must be resolved first for practical system insertions. For instance, when capacitor arrays are implemented for DCO's frequency tuning, they inevitably add extra parasitic capacitance. Also, the tuning range of the ring-oscillator based DCO must be

sufficient to tolerate PVT variations. Consequently, the number of LSB tuning steps will be hard to reduce. Keeping KDCO constant is another prerequisite for PLL's stability, which is critically vital for DBBPLL owing to its large nonlinear operations. Moreover, since the ring-oscillator based DCO especially for the single-ended one also has a relatively low power-supply-rejection ratio (PSRR), it can be easily interfered by neighboring circuits. Adding low-drop-out regulator (LDO) can enhance its PSRR, however may degrade its phase noise, occupy more area caused by necessary stabling capacitors, and lose its voltage headroom.

To address the aforementioned issues, a low input-referred-noise low-voltage BBPD based on the dynamic double-tail phase detector, is proposed to mitigate the meta-stability problem of the conventional DFF-based BBPD and improve the in-band phase noise of the digital BBPLL. A ring-oscillator-based constant-g_m-biased DCO, which can avoid the fine-tuning capacitor array, better tolerate PVT variations and supply noise, is also proposed in this work.

The chapter is arranged as follows: Section II-A describes the BBPD and derives its input-referred noise. Section II-B describes the DCO and its characteristic. Section II-C introduces the architecture of the PLL and shows simulation results on phase

noise. Section III demonstrates the testing results.

3.2 BUILDING BLOCKS OF THE ADBBPLL

3.2.1 Dynamic BBPD

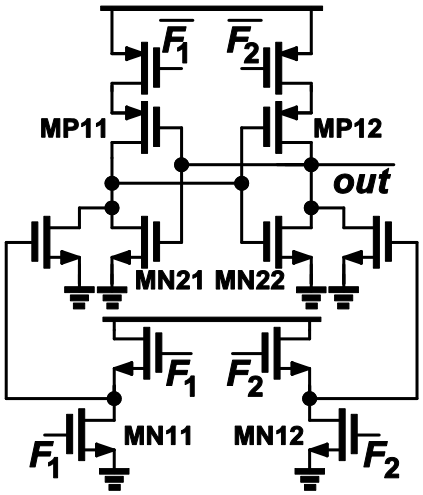

Fig. 3.4 Schematic of the proposed BBPD

Fig. 3.4 shows the schematic of the proposed BBPD. It is Fig. 3.4 Schematic of the proposed BBPD

modified by using a dynamic double-tail comparator [7], taking advantage of its ability to perform under low supply voltage. At first, the PD is operated in sampling phase. MN11 and MN12 will sense the time difference and build up a voltage difference on V_{out} when clock edges arrive. Afterwards, the regeneration amplifier will start to convert the relatively small voltage difference into the rail-to-rail signal that captures lead/lag relation between two input clock edges. Fig. 3.5(a) shows the

detailed transient operation of the BBPD. The g_m of MN11 and MN21 then specify the duration of the sampling phase and regeneration phase, respectively.

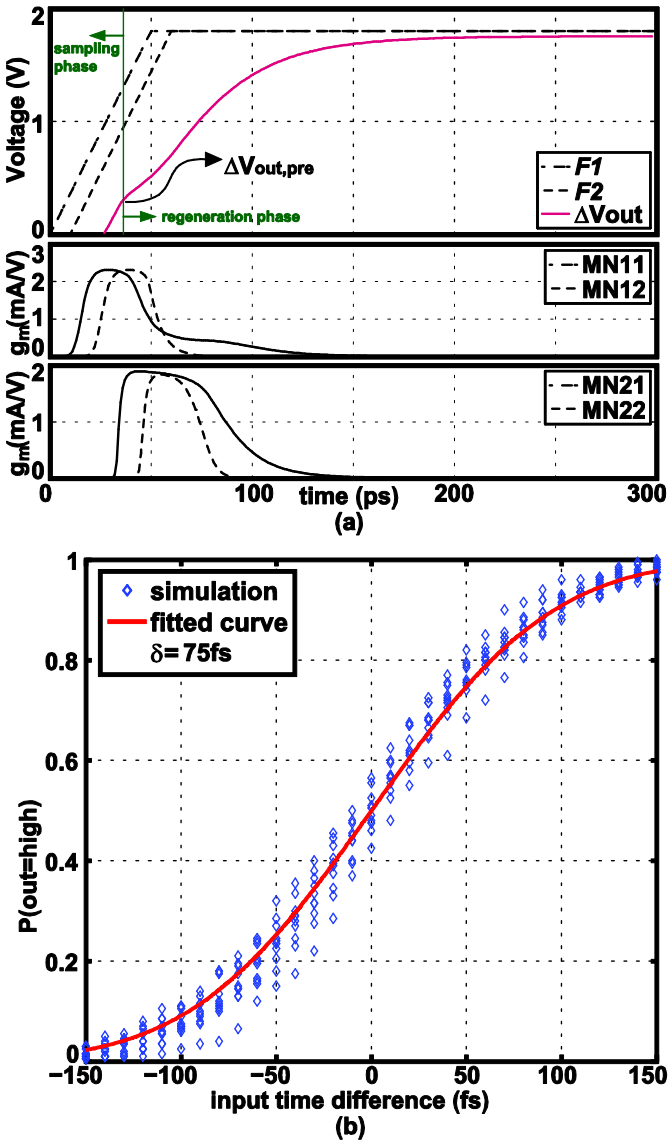

Fig. 3.5 (a) Transient simulation of the BBPD. (b) Cumulative distribution function of the BBPD.

To analyze the noise performance of this PD, we first derive the output thermal noise in voltage, v_n. Assuming that the PD is a linear periodically time-varying system due to its nature of clock-triggering operation, the output thermal noise can be derived in the methodology introduced by [8]. At first, the small signal model of the PD under sampling phase is shown in Fig. 3.6 and we can see that the noise transfer functions of MN11,12 and MN21,22 are similar to the classic strong-arm dynamic comparator. Second, we need to determine the sampling duration, tsample, during which the cross-coupled regeneration amplifier is not turned on:

$$t_{\text{sample}} = \frac{C_{\text{out}} \cdot V_{\text{th}}}{I_{\text{MP}}}, \tag{1}$$

where IMP is the current which go through the MP11,12. Afterwards, v_n can be obtained from integrating the impulse sensitivity function (ISF) and then multiplying the noise source (in1 and in2):

$$v_{\text{n}}^2 = \frac{4kT\gamma}{3C_{\text{x}}} \cdot \frac{t_{\text{sample}}^3}{\tau_{\text{s1}} \cdot \tau_{\text{s2}}^2} + \frac{4kT\gamma}{C_{\text{out}}} \cdot \frac{t_{\text{sample}}}{\tau_{\text{s2}}}, \tag{2}$$

where γ is the excess noise factor of short-channel MOS transistors and two time

constant $\tau_{s2}= C_x/g_{m11}$ and $\tau_{s2}= C_{out1}/g_{m21}$ are defined. We only include the noise generated during the sampling phase here because the regeneration phase will not affect the SNR of the sampled voltage too much and herein can be neglected.

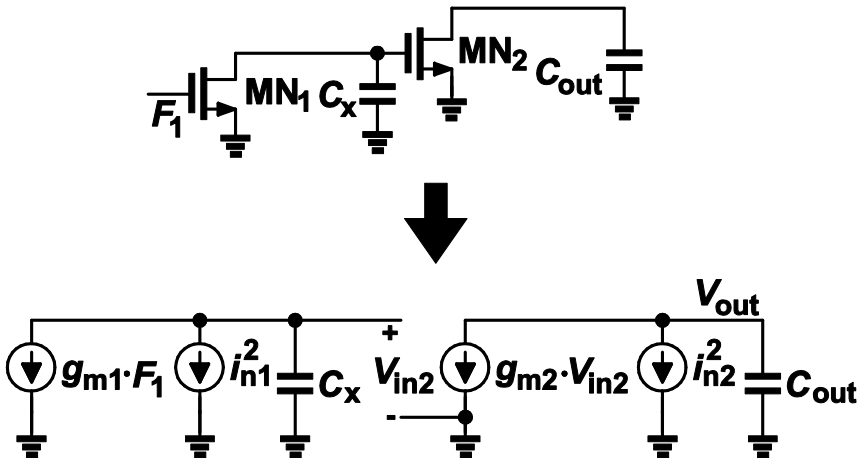

Fig. 3.6 Small signal model of the PD in sampling phase.

To get the input-referred jitter (J_{ref}), we then need to derive the time-to-voltage gain, GTV, of the PD. The current of the PD input transistors MN11,32 is

$$I_{\mathrm{MN}_{11,12}} = \frac{1}{2}\beta(V_{\mathrm{gs}} - V_{\mathrm{thn}})^2, \tag{3}$$

where β represent $\mu_n C_{ox}$(W/L)11,12, and V_{th} is the threshold voltage of NMOS. After the edges, the $\Delta V_{out2\text{-}pre}$ is built on the output of the PD:

$$\begin{aligned}\Delta V_{\text{out2-pre}} &= \int_0^{\Delta t} \frac{1}{2}\cdot\frac{1}{C_{\text{out}}}\cdot k\cdot(\frac{V_{\text{DD}}}{t_{\text{R}}}\cdot t - V_{\text{thn}})^2\cdot dt \\ &= \frac{k}{2\cdot C_{\text{out}}}\int_0^{\Delta t}(\frac{V_{\text{DD}}^2}{t_{\text{R}}^2}\cdot t^2 - \frac{2\cdot V_{\text{DD}}}{t_{\text{R}}}\cdot V_{\text{thn}}\cdot t + V_{\text{thn}}^2)\cdot dt \\ &\cong \frac{k}{2\cdot C_{\text{out}}}\cdot V_{\text{thn}}^2\cdot\Delta t\end{aligned} \quad (4)$$

.

Consequently, the GTV is expressed as

$$G_{\text{TV}} = \frac{\Delta V_{\text{out2-pre}}}{\Delta t} = \frac{\beta\cdot V_{\text{thn}}^2}{2\cdot C_{\text{out}}} \quad (5)$$

.

To obtain the J_{ref}, we divide (2) by (5):

$$\begin{aligned}J_{\text{ref}}^2 &= \frac{v_{\text{n}}^2}{G_{\text{TV}}^2} \\ &= \frac{16kT\gamma}{3C_{\text{x}}^2}\cdot\frac{g_{\text{m11}}\cdot g_{\text{m21}}^2}{I_{\text{MP}}^3}\cdot\frac{C_{\text{out}}^3}{\beta^2\cdot V_{\text{th}}} + \frac{16kT\gamma}{\beta^2\cdot V_{\text{th}}^3}\cdot\frac{g_{\text{m21}}}{I_{\text{MP}}},\end{aligned} \quad (6)$$

The proposed BBPD can be taken as a 1-bit TDC that is capable of detecting tiny time differences between two inputs. To quantify the input-referred jitter, we simulate the bit error rate of the BBPD under different input time differences. Fig. 3.5(b) shows its

cumulative distribution function based on the transistor-level simulation with transient noise: the y axis signifies the probability of BBPD's output becoming logic high and x axis signifies input time differences. The RMS input-referred jitter is about 75 femtosecond. Under locking condition, the input-referred jitter will further decrease the overall gain of the BBPD and thus increase PLL's in-band noise.

3.2.2 Supply-noise-tolerant DCO

Ring-based oscillators often suffer from supply perturbation owing to its frequency being determined by active devices. The problem is much more serious when the ring contains single-ended inverter-based delay units. Instead of using an LDO, a differential topology is adopted in this work for better PSRR compared to the single-ended counterparts. The current of the DCO is provided by a self-biased block that keeps gm in constant rather than the use of diode-connected MOS current source. Fig. 3.7 shows the architecture of the proposed DCO. The g_m-controlled cross-coupled delay unit is used and its effective loading, Z_{out}, on the oscillating node is derived as:

$$Z_{\text{out}} = \frac{R_{\text{p}}}{1 - g_m R_{\text{p}}}. \tag{7}$$

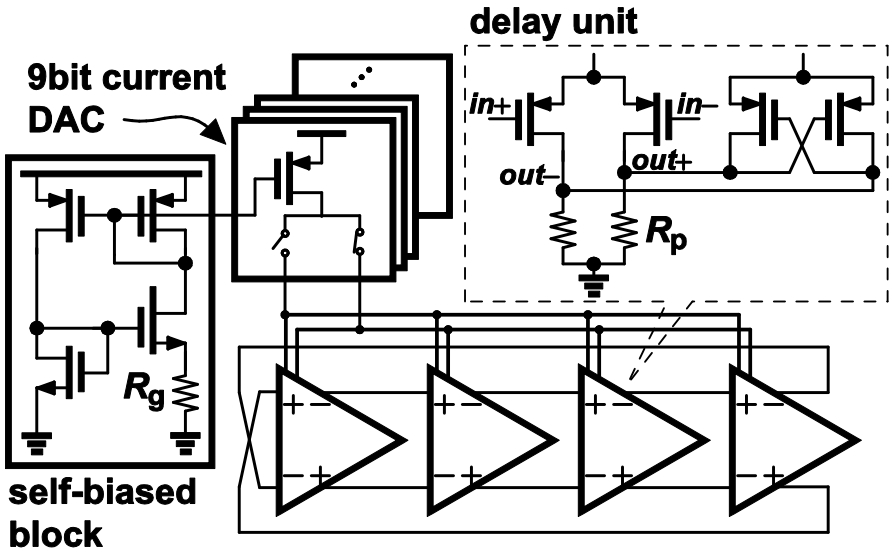

Fig. 3.7 Proposed architecture of constant-g_m-based ring DCO.

It appears from (7) that the delay is determined mainly by R_p, g_m and parasitic capacitors. Because the g_m is the only dynamic parameter, it must be carefully controlled to minimize the variation caused from PVT. For this reason, delay units with mirrored self-biased currents are implemented to immune g_m from PVT intrusions. As a result, a supply-noise-tolerant, ring-based constant-g_m DCO (CGDCO) can be realized by combining the self-biased block and the cross-coupled delay units. Fig. 3.8 shows the simulated VCO supply sensitivity. With an carefully chosen R_g value, the DCO can achieve sensitivity of 0.03. The sensitivity can be further improved if the PSRR of the self-biased block is increased by adding a feedback regulated amplifier. Fig. 6(a) shows the simulation results that the KDCO varies from 300kHz/step to 550kHz/step when the supply voltage encounters 10% deviation,

temperature varies from -30 degree Celsius to 90 degree Celsius and three different corners (TT, SS and FF). It can be seen from Fig. 3.9(a) that the KDCO is grouped into three corner clusters due to the process variation from R_p. However, such KDCO values can be foreground calibrated by slightly altering the value of R_g without changing the topology of delay units directly. Fig. 3.9(b) shows the layout for CGDCO in which a 9-bit current steering DAC is implemented for fine frequency tuning. The DCO consumes less than 2mW and occupies only 0.008mm^2.

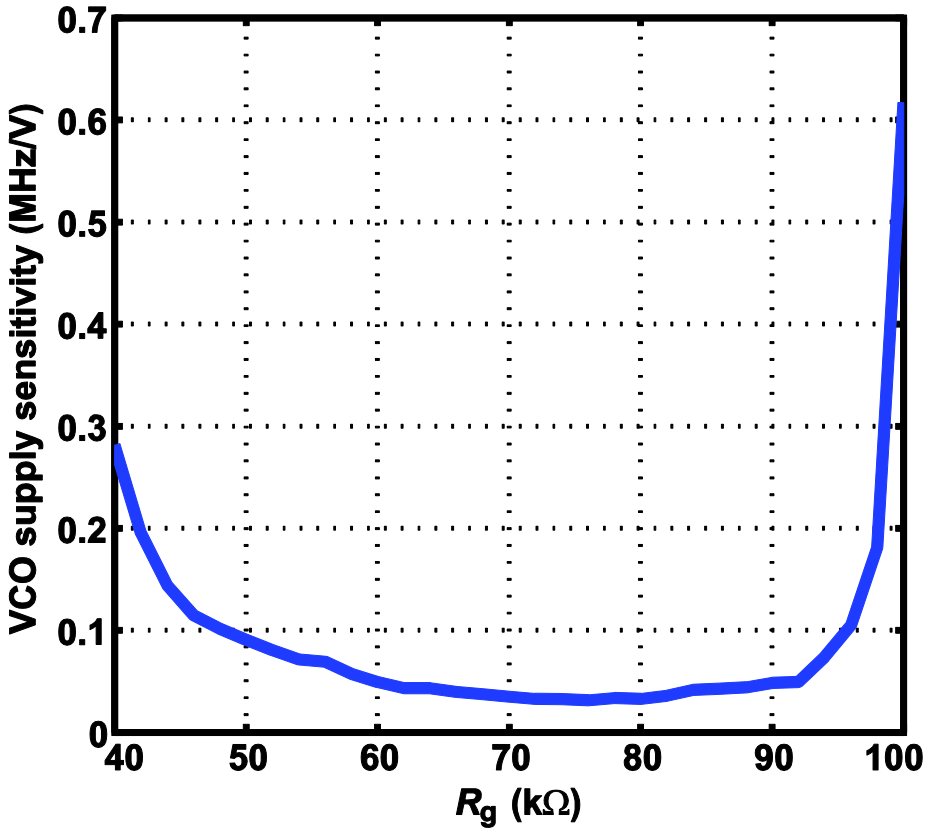

Fig. 3.8 VCO supply sensitivity to different R_g.

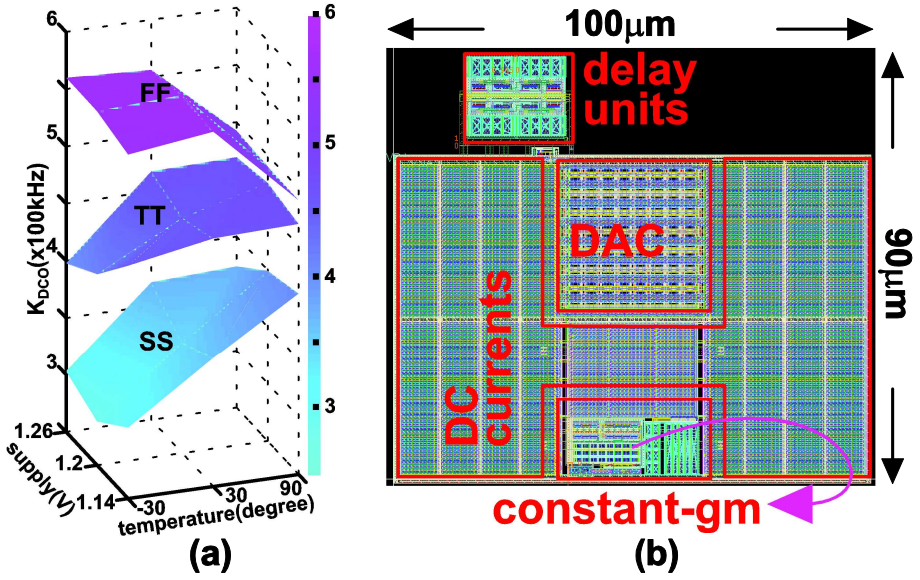

Fig. 3.9 (a) Distribution for KDCO of the DCO under different PVT conditions. (b) Layout of the CGDCO.

3.2.3 Dynamics of PLL

Fig. 3.10 shows the proposed DBBPLL architecture. A retimed pulse swallow divider is used to optimize the duty cycle for decreasing the latency. The duty cycle of the divider output is not set to 50% as usual. The pulse width intentionally shrinks here for decreasing the digital domain latency because the BBPD detects input lead/lag when falling edges of REF or FBK occurs. A proportion and accumulation path following a 1st-order sigma-delta modulator serves as the digital low pass filter which is synthesized and automatically placed and routed.

A 50MHz crystal is adopted as the reference source and the divide ratio is adjustable from 44 to 52, rendering the PLL output frequency range from 2.2GHz to 2.6GHz. Fig. 3.11 shows the simulated phase noise of the BBPLL with different . With carefully managed noise performance of all blocks and digital filter parameters, an optimized bandwidth can be achieved.

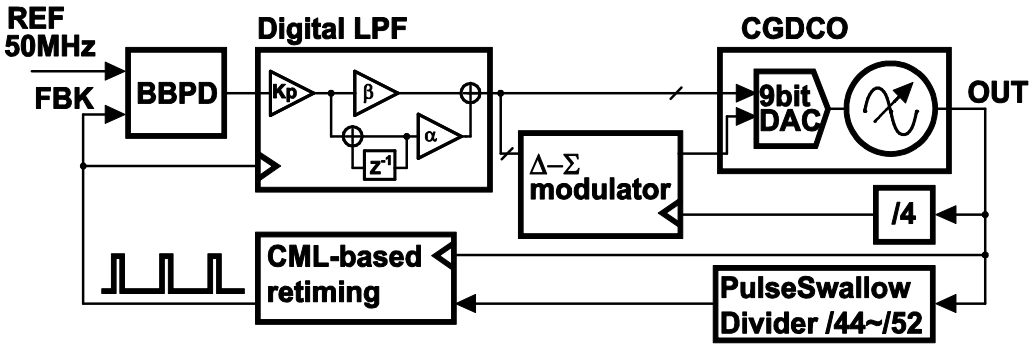

Fig. 3.10 Proposed Architecture of the digital BBPLL.

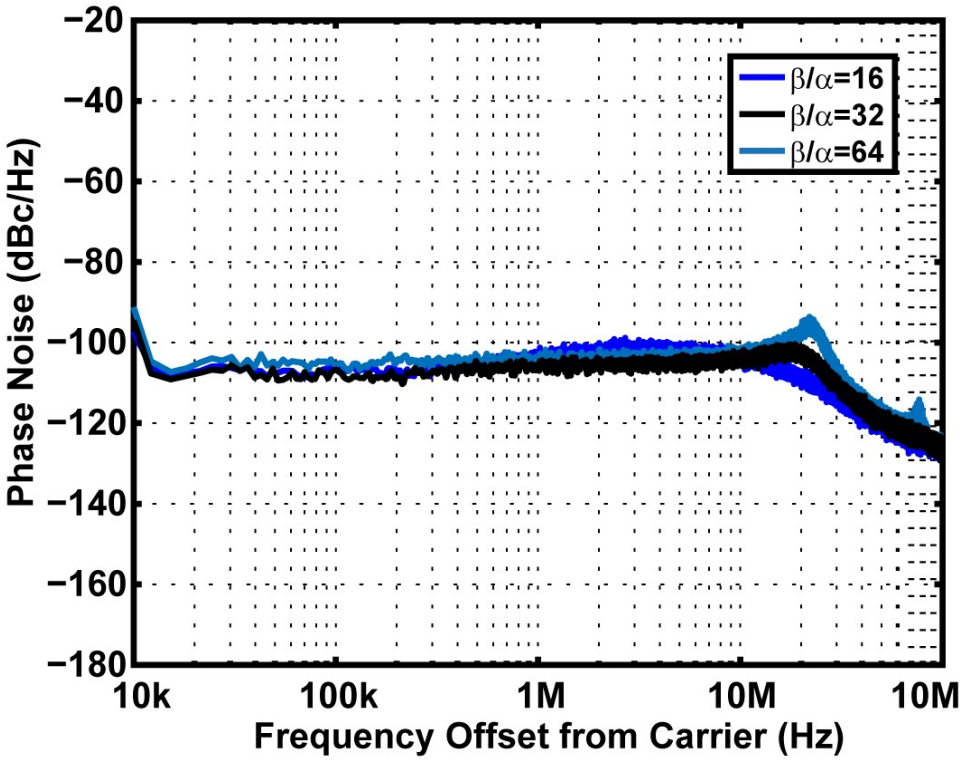

Fig. 3.11 simulated phase noise.

3.3 MEASUREMENT RESULTS & CONCLUSION

A prototype DBBPLL is implemented in 28nm CMOS technology. It consumes 2.9mW under 0.75V supply voltage – the analog part consumes 2.1mW and digital part consumes 0.8mW while excluding output buffer which is added for testing purposes only.

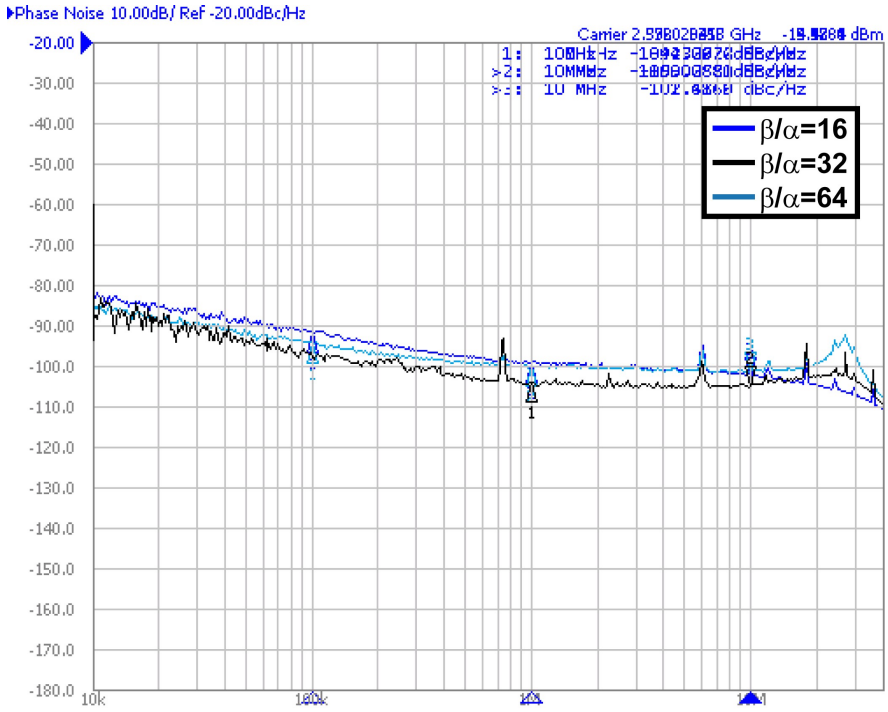

Fig. 3.12 Phase noise at 2.6GHz with different β.

Fig. 3.12 shows the phase noise measured by Agilent E5052A with different at 2.6GHz. The phase noise results match the behavioral simulation in the Fig. 3.11. The minimum in-band phase noise is -105dBc/Hz. The integrated RMS jitter from

20kHz to 40MHz is 3.8ps. Fig. 3.13 shows the phase noise when the power supply is clean and when the power supply is coupled to a 1MHz sinusoidal wave with 200mV peak-to-peak voltage (Vpp). Even with such levels of supply noise, the BBPLL can still be locked and kept stable. Added noise inevitably affects overall output jitter, slightly altering BBPD's gain and hence PLL's dynamic. As noted from Fig. 3.13, -88dBc/Hz tone is incurred by added noise at 1MHz. Fig. 3.14(a) and 3.14(b) show output peak-to-peak jitter in time domain without/with added sinusoidal supply noise of 1MHz 50mV Vpp. They are 30.7ps and 32.2ps, respectively, and are measured through a self-triggered averaged sampling scope (Agilent 86100D). Fig. 3.14(c) shows peak-to-peak jitter under 50mV Vpp supply noise of different frequencies. The added noise appears not to affect the jitter performance due to the supply-noise-tolerant CGDCO and high-bandwidth PLL dynamic that keeps in-band phase noise low.

Fig. 3.15 shows the die photo of this prototype. It occupies 0.014mm^2. Table-3.1 compares our DBBPLL's performance favorably over those of prior arts by achieving the best ring-based DPLL in-band phase noise (-105dBc/Hz) based on 28nm digital CMOS technology.

In summary, we have successfully realized a high performance DBBPLL in 28nm CMOS technology with FoM of -223dB, which is suitable for mobile system, biomedical and wearable applications that are not only area/cost sensitive but also with low supply headroom and noise tolerance.

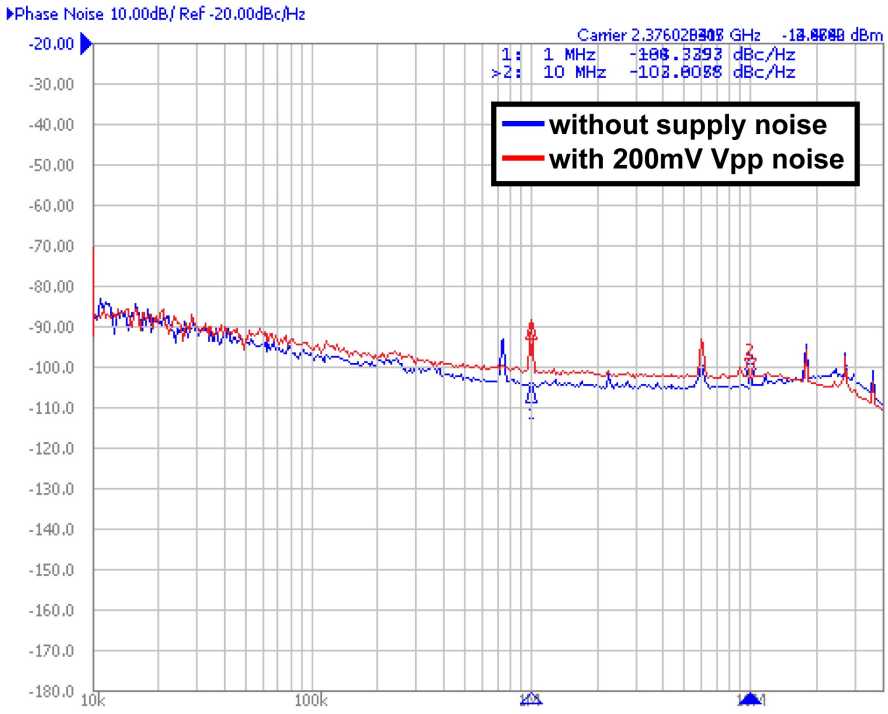

Fig. 3.13 Phase noise with 200mV-Vpp sinusoidal wave added on power supply.

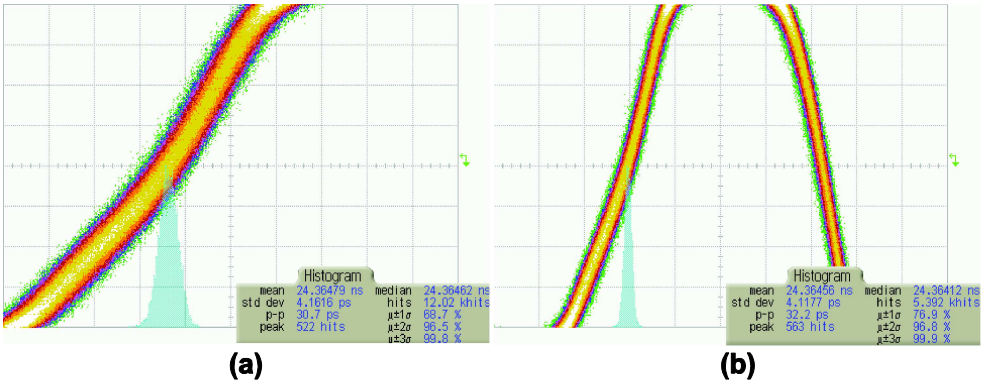

Fig. 3.14 (a) Jitter histogram with clean supply. (b) Jitter histogram with 50mV-Vpp

sinusoidal wave added on power supply.

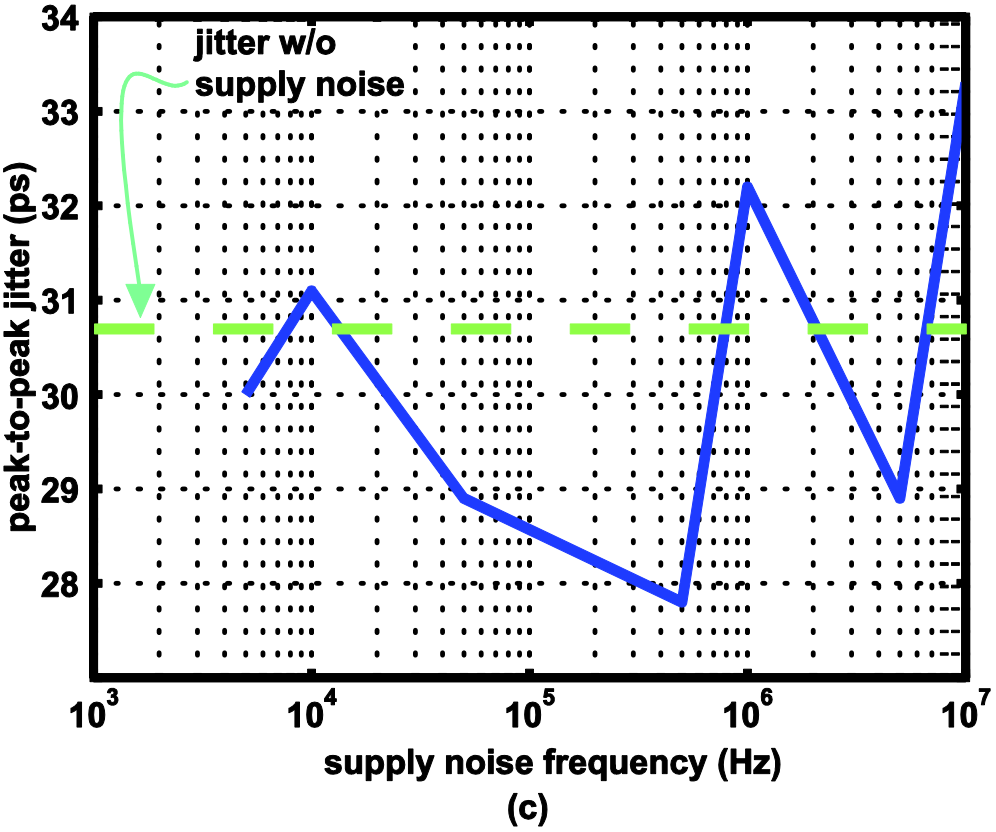

Fig. 3.14 (c) Peak-to-peak jitter vs different frequencies of 50mV-Vpp supply noise.

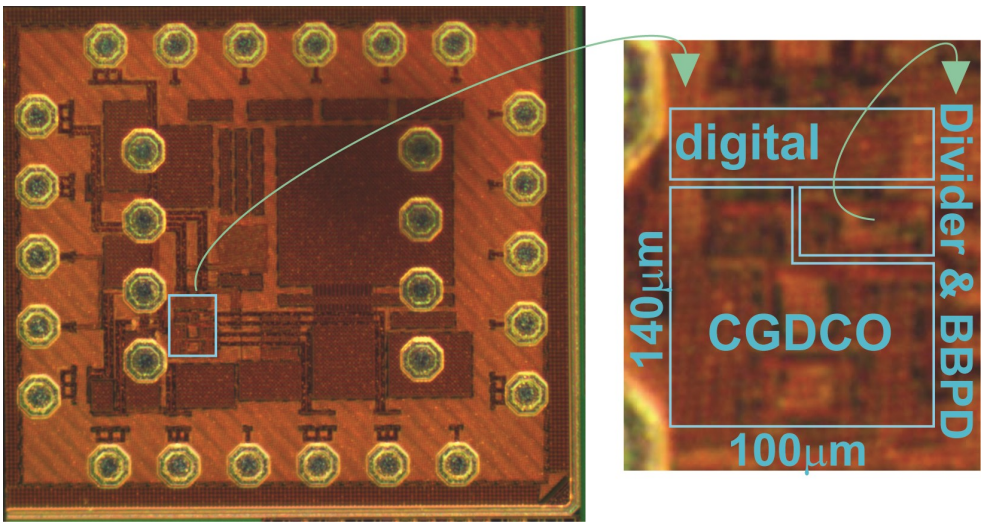

Fig. 3.15 Die photo.

Table 3.1: Comparison with state-of-the-art digital PLLs.

Performance Summary

Metric	ISSCC'15 [9]	JSSC'14 [10]	VLSI'15 [11]	This Work
Architecture	BBPLL	TDCPLL	BBPLL	BBPLL
Technology	14nm(Fin)	28nm	65nm	28nm
Area (mm^2)	0.009	0.032	0.019	0.014
Supply (V)	0.8	1.0	1.2	0.75
Frequency (Hz)	2G	0.63G	1.6G	2.6G
Power (mW)	2.06	3.1	2.7	2.9
Power/Freq (mW/GHz)	1.03	4.92	1.68	1.12
In-band phase noise (dBc/Hz)	-91	-100	-97	-105
Integrated RMS jitter (ps)	18.8	15	2.8	3.8
FoM (dB)*	-211	-211	-227	-223

*FoM is $10\log_{10}[(d/1s)^2 / (Power/1mW)]$, where d is integrated jitter

Chapter 4

A Fully Integrated 28nm CMOS Dual Source Adaptive Thermoelectric and RF Energy Harvesting Circuit with 110mV Startup Voltage

4.1 INTRODUCTION

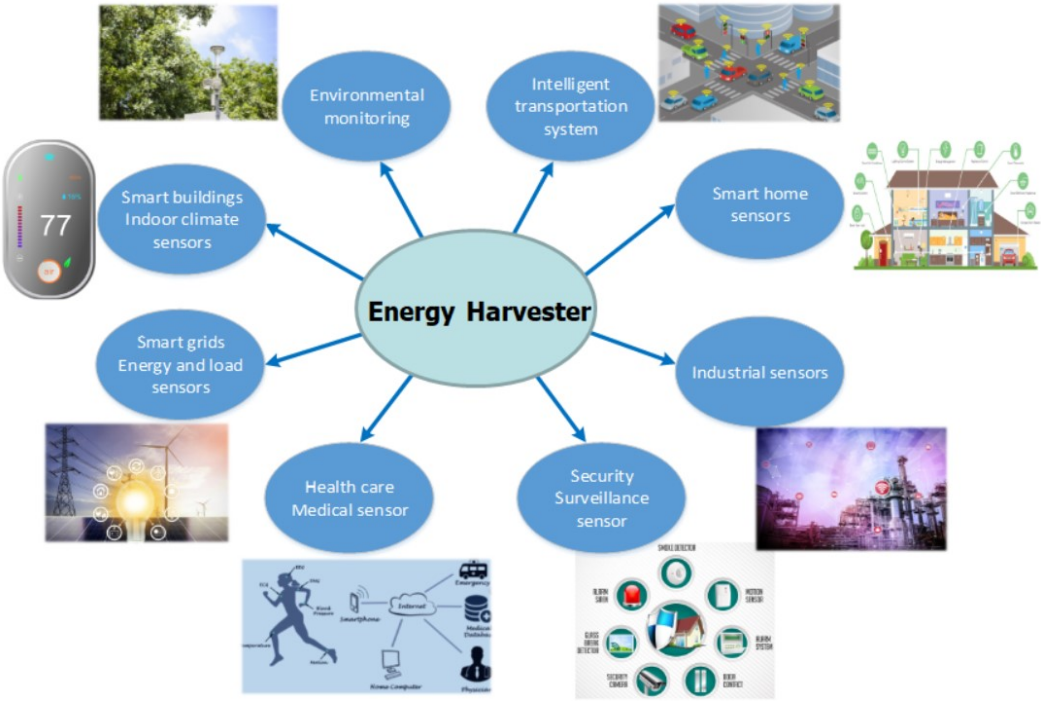

Fig. 4.1. Potential applications of energy harvester.

As wireless sensor networks and internet of gain traction in industrial, medical and consumer applications, self-powered, energy harvesting circuits become a key enabling technology where direct power is impractical or battery replacement is difficult. As shown in Fig. 4.1, energy harvester can be used in many areas such as biomedical health device, wearable appliances, home security systems and industrial sensors.

One energy harvesting challenge is the ultra-low available ambient power. A battery-less energy harvesting system thus requires low input DC voltage or RF power for robust startup performance. Because multiple potential energy sources may be available, such as thermoelectric energy from temperature gradients or RF power from various transmitters, multi-source energy harvesters would utilizing multiple power sources in combination. Many dual-source harvesters are source type agnostic, such as thermoelectric, piezoelectric or photovoltaic DC sources [12], or multi-frequency band RF sources [13]. Other dual-source systems [14, 15] combine two harvesting circuits that work independently. A more efficient approach is proposed to allow the dual sources to interact with each other, lowering the input startup voltage when both are available.

Another challenge is the miniature form factor dictated by certain applications such as implant medical devices, or by cost considerations. A fully integrated solution implies the absence of startup options, such as those relying on an external battery, mechanical switch [16], or large μH or mH transformer/inductor [17, 18], or large μF capacitor [19, 20]. Fig. 4.2 shows conventional energy harvester that utilizes off-chip passive components such as capacitors, inductors and transformers. These components need extra PCB footprint to accommodate and usually are larger than energy harvester itself.

This paper presents a fully integrated energy harvesting system consisting of a boost oscillator startup circuit, a RF rectifier and a boost converter that operate at RF frequency and that completely eliminate off chip components and PCB. To improve energy efficiency, a proposed adaptive bias scheme for the boost oscillator G_m reduces current consumption at higher voltage, while assisting startup at lower voltage.

This chapter is organized as follows: Section 4.2 describes the energy harvesting system, its building blocks and operation theory. Measurement results are summarized and conclusions are drawn in section 4.3.

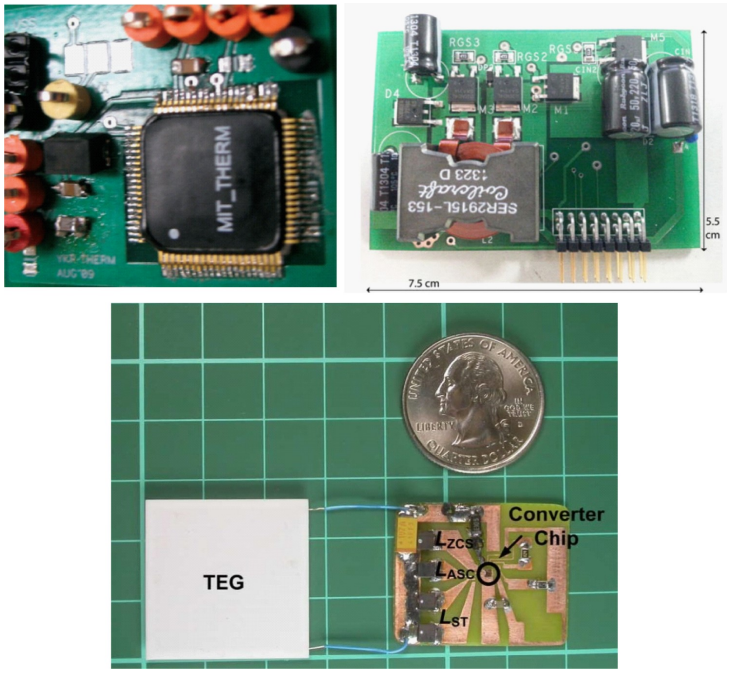

Fig. 4.2 Conventional energy harvester with off-chip passive components.

4.2 Building Blocks Of The ADBBPLL

4.2.1 Dual source thermoelectric and RF energy harvester

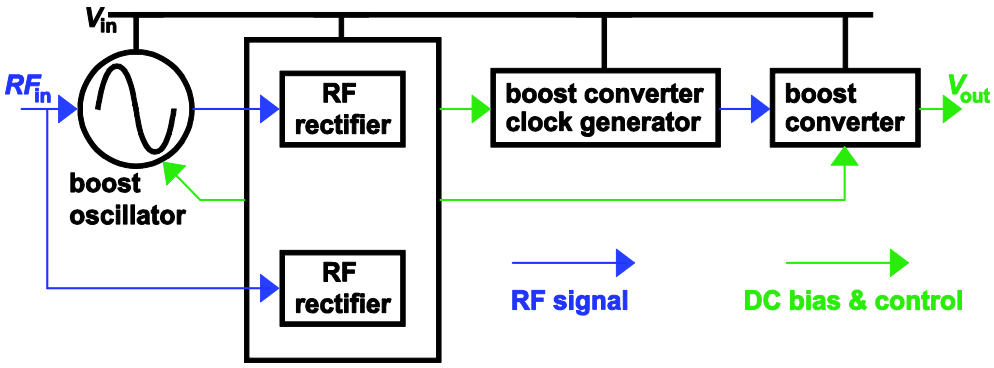

Fig. 4.3. Block diagram of the proposed dual source thermoelectric and RF energy harvester.

Fig. 4.3 shows the proposed energy harvester block diagram that takes a DC input source and a RF injection signal. It consists of a boost oscillator startup circuit, a RF rectifier, a boost converter and its clock generator. The boost oscillator takes V_{IN} as DC power and RF_{in} as an optional RF input signal to generate oscillation at GHz frequency. Either the oscillator output or the RF input drives the RF rectifier, generating DC output voltages that bias and control the boost oscillator adaptive G_m, boost converter and converter driver. The boost converter provides output voltage to the load. All four blocks run at RF frequencies, while the bias and control voltages generated by the rectifier are DC signals.

4.2.2 Adaptive boost oscillator

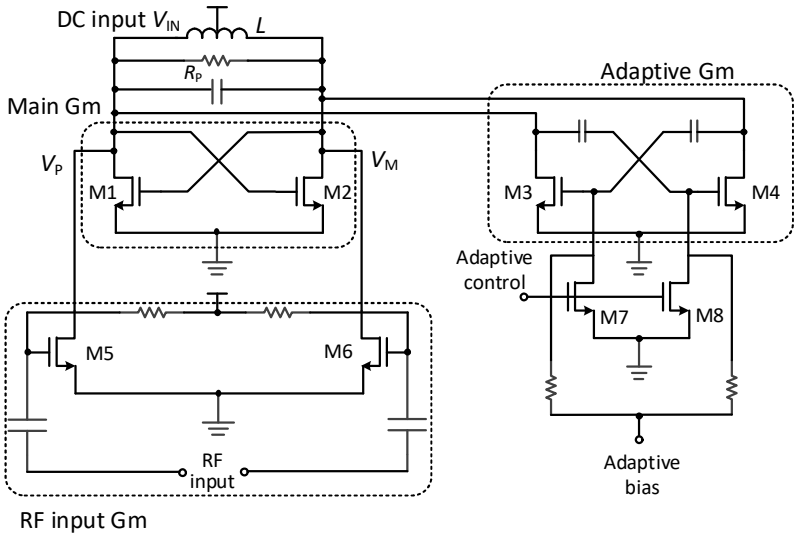

Fig. 4.4. Adaptive boost oscillator

As one of the most challenging blocks of an energy harvester, the startup circuitry works at extremely low input voltage (V_{IN}) to enable other harvester circuits that would not function otherwise. Achieving full integration without any off-chip components, the startup circuit is a negative G_m NMOS LC boost oscillator shown in Fig. 4.4 .It requires lower headroom and imposes less tank parasitic capacitance than its CMOS counterpart. The startup condition is given by $g_m > 2/R_P$, where g_m is the trans conductance of the core devices M1 and M2, and R_P is the oscillator tank equivalent resistance.

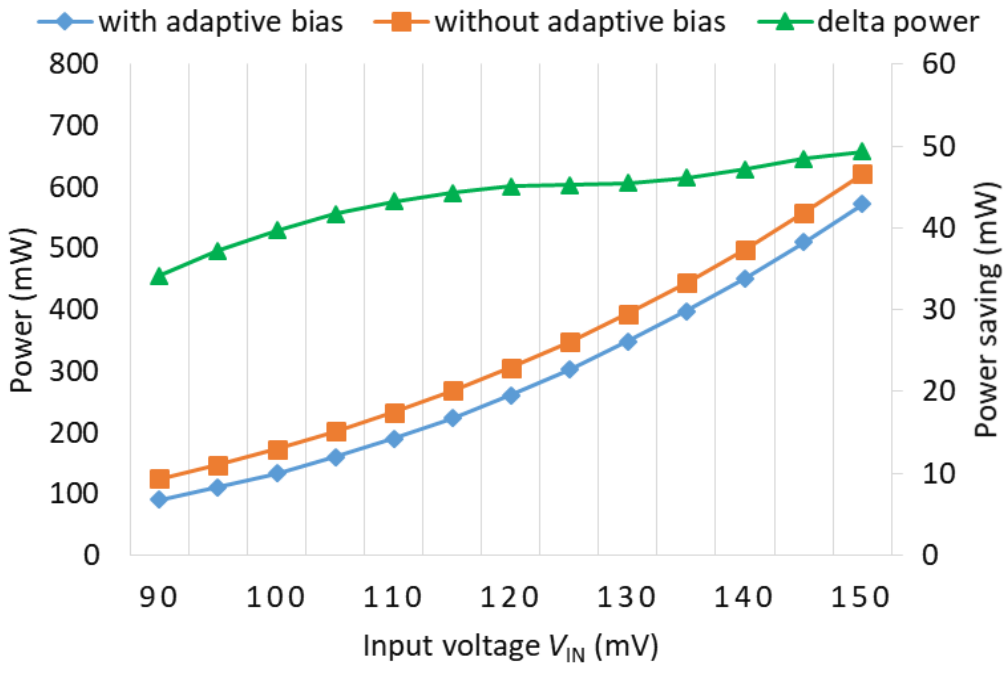

Fig. 4.5. Boost converter power consumption with and without adaptive bias control.

To ensure oscillation startup at low input voltage, the circuit needs to generate sufficient g_m and maximize R_P. To obtain sufficient g_m at low supply voltage, a low threshold voltage native NMOS device is used with large W/L ratio. To maximize R_P, which is usually dominated by the tank inductor $R_{PL}=Q_L*\omega_{osc}*L$, [19] using an off chip inductor with large inductance L (2μH) and high quality factor Q_L while operating at ~30MHz. However, the oscillation frequency ω_{osc} is an important factor that can boost on-chip tank inductor impedance of merely a few nH and moderate Q_L. If the boost oscillator runs at 1.5GHz, a R_{PL} of 200 Ohm is achievable for a 2nH inductor with a Q_L of 10. Although this is still one order of magnitude smaller than the off-chip inductor case, a comparable low startup voltage is feasible with properly designed G_m.

A small tank impedance mandates large g_m for oscillation startup, leading to large core device size needed at low V_{IN}. At higher V_{IN}, the large core devices consume more current than necessary and reduce power efficiency. A proposed adaptive G_m core solves this problem by partitioning the G_m into the main G_m devices (M1 and M2) and adaptive G_m devices (M3 and M4). The main devices are DC coupled with gates biased at V_{IN}, while the adaptive devices are AC coupled with gate

bias controlled by V_{ctrl}, the output of the RF rectifier in the following stage. The rectifier output voltage increases as the oscillation amplitude builds up. When V_{ctrl} is sufficiently high, M7 and M8 will turn on to reduce M3 and M4 gate bias voltages, thus reducing their current consumption. Fig. 4.5 shows the boost oscillator power saving with adaptive control compared with the case when M3 and M4 are constantly biased at V_{IN}.

G_m core adjustment has been applied to wide tuning the VCO, minimizing tank parasitic capacitance at higher frequency when the tank R_P is larger and a smaller g_m is needed for oscillation startup and swing [21]. Part of the G_m core size is switched off. Depending on the pre-programed frequency, not supply voltage. For adaptive boost oscillator in Fig. 2, without prior knowledge of VIN, the G_m core is configured to generate maximum g_m initially to ensure startup and adaptively reduce its power control by the rectifier output that indicates oscillation amplitude.

4.2.3 Super-regenerative operation

Super-regeneration has been used in ultra-low power receivers for startup of an oscillator [22]. The oscillation startup time and amplitude depend on the strength of

the injected signal. When the DC voltage from thermoelectric energy is not sufficient for reliable startup by itself or requires long startup time, the harvester in super-regenerative mode can utilize the RF input power to enhance the startup condition and reduce the startup voltage.

Applying KCL to the oscillator tank in Fig. 4.6, we have

$$C\frac{dV}{dt}+\left(\frac{1}{R_P}-G_m\right)V+\frac{1}{L}\int V dt = I_{inj}\sin(\omega t). \quad (1)$$

The tank voltage V can be solved as

$$V = e^{-\alpha t}e^{j\omega_d t}+\frac{I_{inj}\sin(\omega t+\varphi)}{\sqrt{\left(\frac{1}{R_P}-G_m\right)^2+\left(\omega C-\frac{1}{\omega L}\right)^2}}, \quad (2)$$

where $\alpha=((1/(R_P-G_m)))/2C$ and $\omega_d=\sqrt{((1/LC)-\alpha^2)}$. In Eqn. (2), the first term represents the free running oscillation, while the second is the forced response to the injected signal.

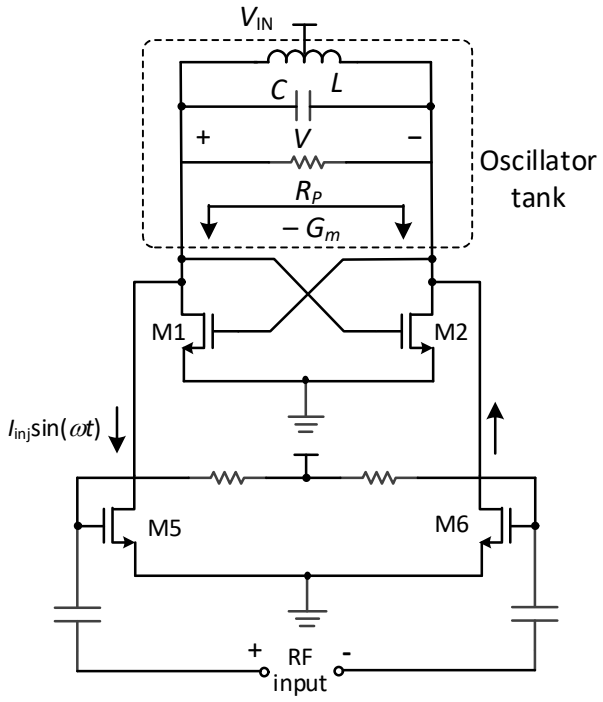

Fig. 4.6. Super regenerative oscillator with RF injection signal.

When G_m is not sufficient at low VIN, and the total tank impedance is positive ($\alpha > 0$), the oscillation cannot start. Negative G_m offsets the tank parasitic resistance RP and enhances the tank Q. The oscillator operates in the Q-enhanced amplification mode for the injection signal and builds up tank swing for harvester startup. When G_m is borderline sufficient to set α negative, the oscillation will take a long startup time. In super-regenerative mode, the injection signal provides the initial tank voltage, speeds up startup and enhances oscillation amplitude, as shown in Fig. 4.7. When G_m is large enough at higher V_{IN}, the oscillator enters free oscillation mode and generate sufficient tank swing.

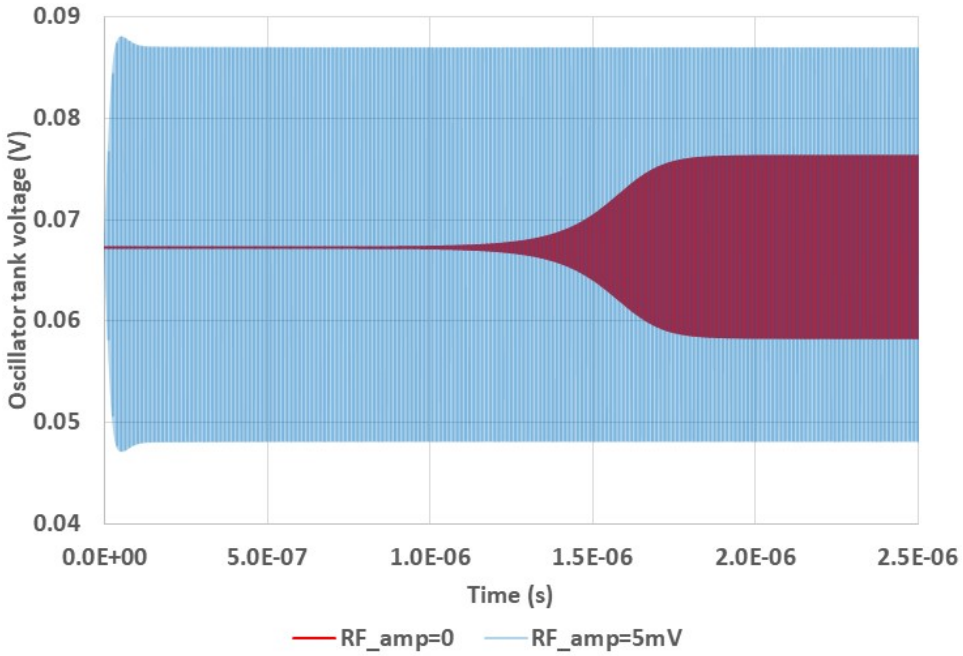

Fig. 4.7 Boost oscillator startup transient waveforms with and without RF injection signal.

Fig. 4.8 shows the oscillation amplitude at different input voltage and injection signal amplitude. The injection signal lowers the threshold V_{IN} voltage for the oscillator to start and increases oscillation amplitude. With the help of ambient RF power, boost oscillator can be easier to start up and therefor the overall system will require less input voltage or power to work.

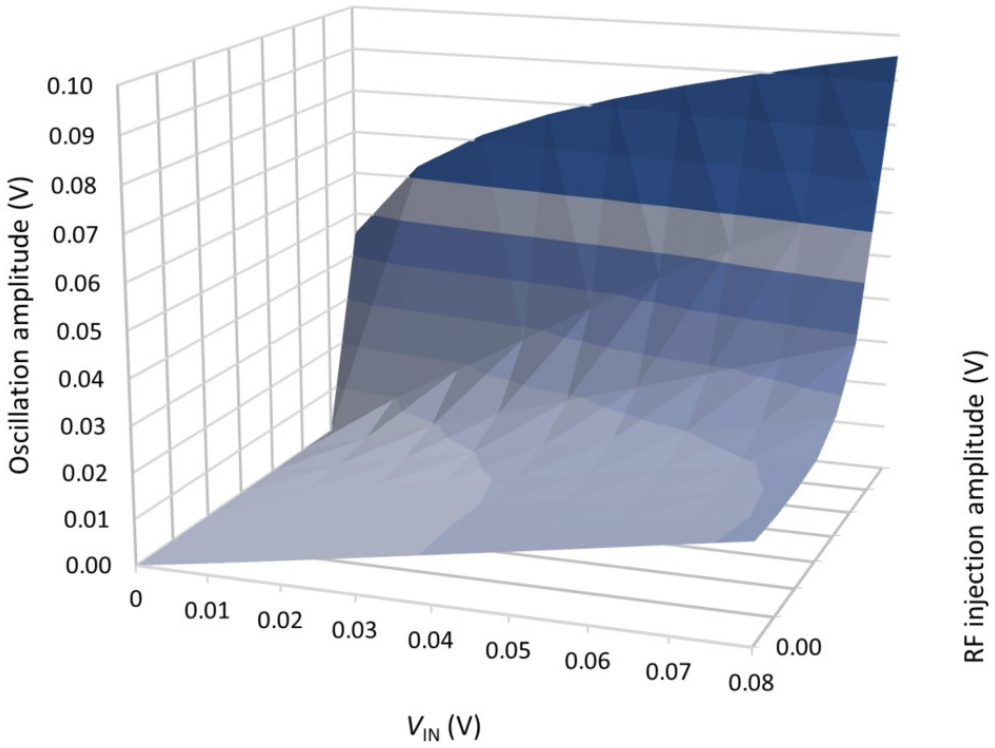

Fig. 4.8. Oscillation amplitude at different VIN and injection signal strength

4.2.4 RF rectifier

A Pelliconi differential charge pump is used as an RF rectifier [23] to generate DC bias and control voltages driven by RF inputs, which are dual sources from the boost oscillator or the RF injection signal. Shown in Fig. 4.9, the rectifier consists of 6 stages with differential RF inputs. The output voltage at the N^{th} stage is given by

$$V_N = V_{IN} + 2N\left(V_{amp} - |V_{th}|\right) - I_{out}R_{out}, \quad (3)$$

where V_{amp} is the RF input amplitude, V_{th} is the transistor threshold voltage, I_{out} is the output loading current, and Rout is the rectifier output impedance. Large RF swing, low device threshold voltage and small load current are desired for high output voltage.

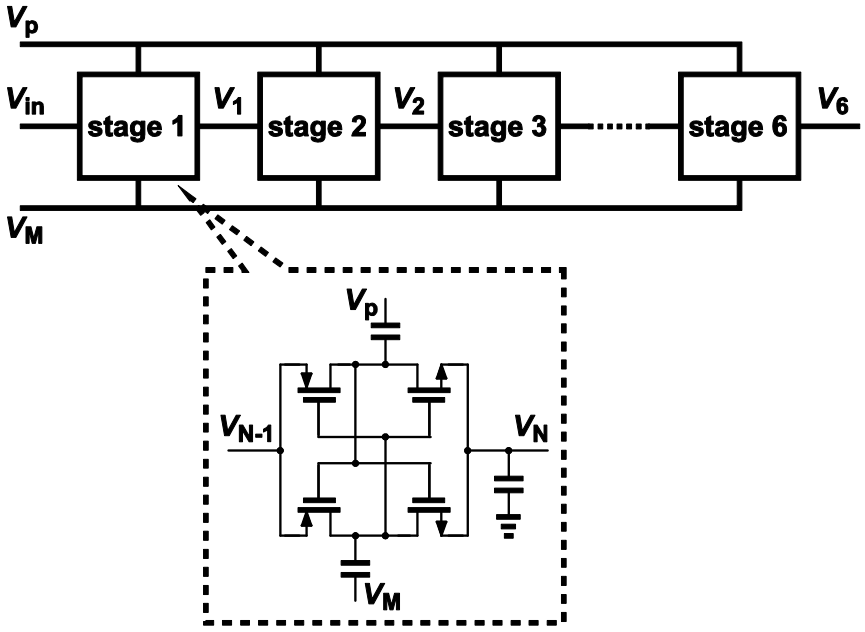

Fig. 4.9 Multi-stage RF rectifier for DC bias voltage generation.

Fig. 4.10 shows the simulated transient waveform at the output of each stage. The outputs reach the steady state in less than 10μs with a voltage gain from 1.9 at the 1st stage to 6.4 at the 6th stage. The RF rectifier can achieve high voltage gain and high PCE. However, it has limited output power at tens of microwatts and usually drives only large load impedance. We take the rectifier output mainly as DC bias and control

voltages with low output current, therefore high voltage gain can be obtained with I_{out} close to zero in Eqn. (3).

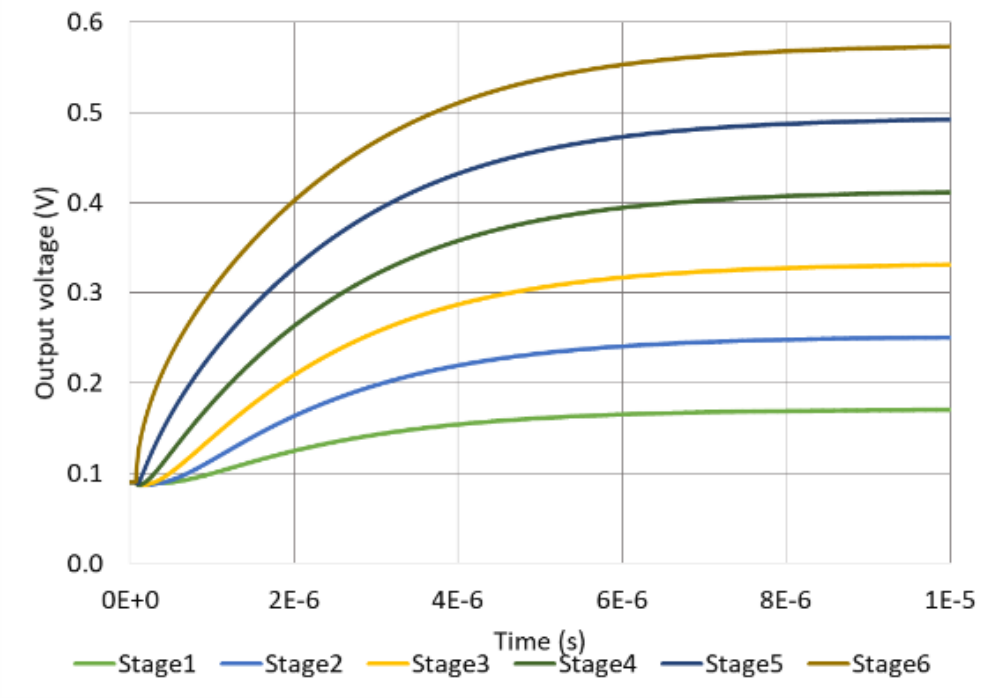

Fig. 4.10 RF rectifier output voltage of each stage.

There are two rectifiers implemented, one driven by oscillator tank voltage and the other by the RF injection signal. When V_{IN} is not large enough to start oscillation, sufficient RF input would be able to generate higher DC voltage to bias up the adaptive G_m devices, leading to RF input assisted oscillation at a lower startup voltage.

4.2.5 Boost Converter

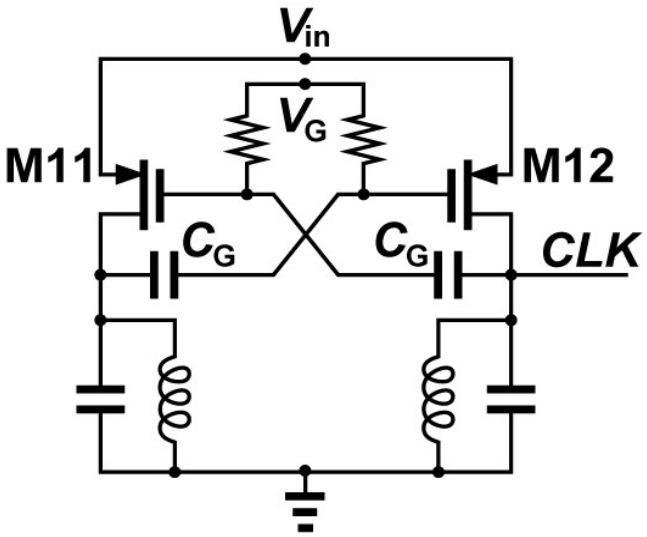

Fig. 4.11 Boost converter clock generator

Boost converters in conventional energy harvesting circuits usually operate at tens of kHz [18] to tens of MHz [19], which require large off-chip capacitor and inductor. Fig. 4.11 and Fig. 4.12 show the schematics of the proposed boost converter and its clock generator. The output capacitor C_L is determined by the output voltage ripple (ΔV) requirement

$$C_L = I_{OUT}/(\Delta V \cdot f) \quad (4)$$

where I_{OUT} is the output current and f is the boost converter clock frequency. For I_{OUT} of 100μA, ΔV of 5mV, a clock frequency of 2GHz will limit C_L to 10pF, which is feasible to be integrated on chip.

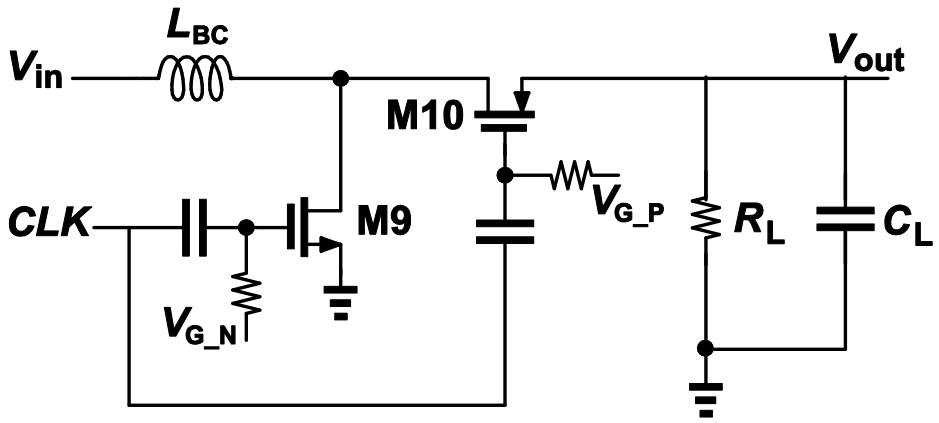

Fig. 4.12 boost converter

It is very challenging to generate the clock signal at GHz frequency while meeting the following requirements: 1) large duty cycle (D) to obtain high voltage boost ratio $V_{OUT}/(V_{IN}=1/((1-D)))$, and 2) large slew rate to minimize simultaneous turn on time of switches M9 and M10 for high PCE. The boost oscillator output cannot drive the boost converter as the clock because of its sinusoidal waveform being near 50% duty cycle and low slew rate. A class-C PMOS LC oscillator is used with the gate of G_m pair M11 and M12 AC coupled to their drain and biased lower than the drain. Because they are PMOS devices, and the class-C operation reduces the turn on time, the drain voltage duty cycle increases and enhances the slew rate. By varying the gate bias VG, the duty cycle and converter boost ratio can be adjusted. Even though the slew rate is ~10GV/s, significantly higher than that of a kHz or MHz clock, the transition phase is not a negligible portion of one period of sub-nanosecond,

during which the switches M9 and M10 inevitably turn on simultaneously, causing current leakage from V_{OUT} to ground, and resulting in a lower PCE than its lower frequency counterpart.

4.3 Measurement Results & Conclusion

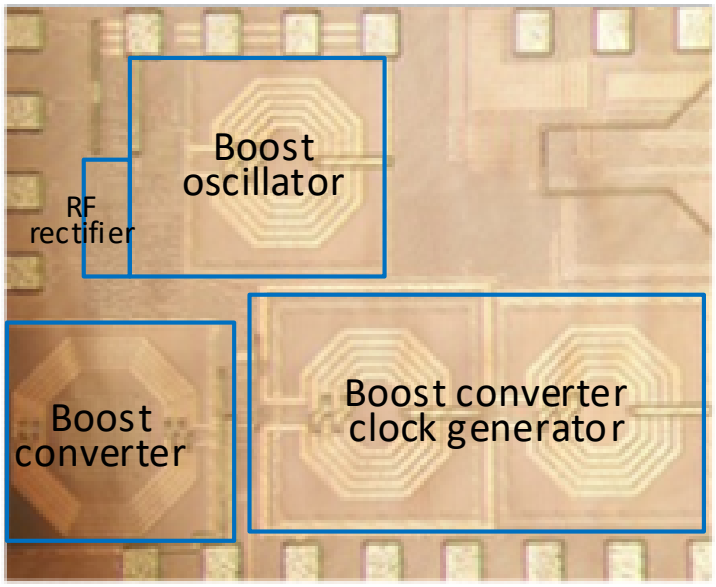

Fig. 4.13 Die photo

The dual source energy harvesting circuit was fabricated in 28nm CMOS process. No off chip components were used. It occupies 0.46mm^2 as shown in Fig. 4.13 including the boost oscillator, the RF rectifier, the boost converter and the converter clock generator. Fig. 4.14 shows the boost oscillator startup voltage over RF input

power. Without RF input, the startup voltage V_{IN} is 110mV with 210μW power consumption. At input power of -16dBm, the startup voltage reduces to 85mV. The boost converter has a peak conversion gain of 2.2, maximum PCE of 25% and maximum output power of 520μW.

Including power consumption of the clock generator and the boost oscillator, the overall peak PCE is 10%. Table 4.1 shows how the design compares with other designs in the literature. Compared to energy harvesters with off-chip inductors and/or capacitors, its PCE is relatively low due to smaller inductance, lower Q, and higher power consumption at RF frequency. Its startup voltage and maximum output power are comparable with most state-of-the-art designs. Future work would focus on further improvement on inductor Q and boost converter switching efficiency.

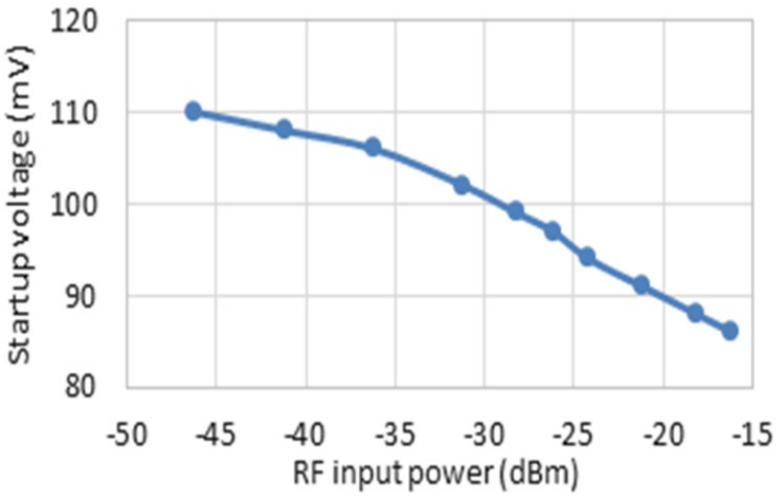

Fig. 4.14 Measured startup voltage at different RF input power levels

This paper presented a fully integrated dual source adaptive thermoelectric and RF energy harvesting circuit. The oscillator G_m adaptive bias reduces current consumption at higher voltage while assisting startup at lower voltage. The RF input signal further reduces startup voltage through Q-enhanced amplification and super-regenerative mode. The boost converter clock is generated by a class-C PMOS LC oscillator for higher duty cycle and slew rate. Implemented in 28nm CMOS, it achieved a self-startup voltage of 110mV without RF input and 85mV at -16dBm input. The boost converter PCE is 25% and the overall PCE is 10%.

Table 4.1 Performance summary and comparison

Metric	JSSC'13 [19]	JSSC'15 [20]	JSSC'14 [17]	JSSC'16 [18]	This Work
Technology	65nm	130nm	130nm	130nm	28nm
Startup Mechanism	LC oscillator	charge pump	XFMR	charge pump	LC oscillator
Off-chip Component	L 2~200mH C 4.7nF, 1mF	C 10nF X 6	XFMR 10mH	L 200mH C 10nF	None
Startup Voltage	50mV	150mV	21mV	70mV	110mV w/o RF 85mV w/ RF
Peak Efficiency	73%	34%, 72.5%	74%	58%	25% converter 10% end-end
Max. Power	282μW	608μW	2mW	17μW	520μW

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