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Low-Cost Gate Drive for Enhancement Mode SiC JFET Devices

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***Abstract*—The main objective of this work is to develop a low cost gate drive circuit for the enhancement mode SiC JFET device with a comparable switching performance as those of commercial ones. To achieve this low cost requirement, the gate drive circuit design needs to use only components which are widely available. In this paper, the proposed SiC JFET gate drive circuit design is described and its switching performance is experimentally verified. The targeted cost per gate drive circuit is made to be less than US$10, which is a sizeable cost reduction in comparison to a commercially available gate drive.**

Keywords— SiC JFET Gate Drive, wide bandgap devices, high temperature Introduction

I. INTRODUCTION

SiC is a wide bandgap semiconductor material which has superior features for power semiconductor devices compared to the current silicon (Si) technology. It can surpass the unipolar limits set by the silicon technology. In particular, SiC has a one magnitude higher breakdown electric field and high temperature thermal capability which translate to higher breakdown voltage for low on-resistance characteristics [1,2] for high temperature applications. This can lead to potential savings in the cooling system.

Although SiC junction field effect transistors (JFET) can be used in applications for voltage ratings of up to 10kV, they are especially competitive in the 1200V category with its low switching losses for the power electronic application on electric traction and photovoltaic inverters. In recent years, SiC JFETs were developed and became popular for the commercial market. The JFET device consists of substantial gate capacitances which are important factors during switchings. A high peak current is needed during the initial turn-on stage to quickly charge the capacitance within the device for a short turn-on transition time. Similarly, a high enough negative peak current is needed during turn-off to discharge the gate capacitance as quick as possible. The parasitic gate-source diode needs to be kept forward biased to ensure good device on-state conduction, such a steady-state positive gate voltage and current will be needed. It is desirable to minimise this steady-state gate loss provided that the device's main conduction current is not affected. The second concern is that, the device has a low gate threshold voltage which does not provide high noise immunity. Thus, a small negative bias is normally necessary to ensure the device does not turn on accidentally by the switching spikes.

In summary, a good SiC gate drive must meet the following requirements: (a) it is able to deliver a quick and substantial amount of charge to the gate capacitances during turn-on process and fast removal of the charge to ensure a fast turn-off process; (b) it is able to maintain the forward bias state of the gate-source diode during the on time but keeping the gate loss to the minimum without affecting the main current conduction; and (c) it is to maintain a small negative voltage at the gate during off state to raise the device's noise immunity. A gate drive chip numbered SGDR600Po [4] was developed by Semi South Laboratories to drive SiC JFET devices. It fulfils the above-mentioned requirements. However, the chip is relatively expensive and not easily available in countries out of the United States. The evaluation board costs about US$180 [5], which is rather expensive to be used for a US$40 SiC JFET SJEPo20Rw--. Thus, it is felt that a much cheaper and equally capable gate Csive circuit need to be developed for SiC JFET devices. Our work has developed such a gate drive with a cost target of US$o 0 and to achieve a comparable gate drive performance.

II. THE GATE DRIVE DESIGN

The proposed hardware circuit for the SiC JFET gate drive is shown in Fig.1. The circuit is made isolated from the control signals through an optocoupler. The optocoupler gives pulse signals ranging from +5V to -15V. To produce a constant conduction current during the on-state, a PNP transistor Q1 is used. The gate current flowing through the JFET device can be controlled by the resistor at the gate. The current is preferably to be around 100mA to 200mA to ensure the device stays on and at the same time it is not over-driven with high losses. A Schottky diode is added at the gate to ensure that the current flows in one direction.

Next, in order to produce sufficient amount of peak current to charge the device capacitance during turn-on, a MOSFET driver chip U1 TC4422CPA is used. However, the input signal will need to be shaped so that the MOSFET driver only produces the pulse current for a short time. A combination of parallel resistor and diode with a capacitor is used to shape the voltage signal.

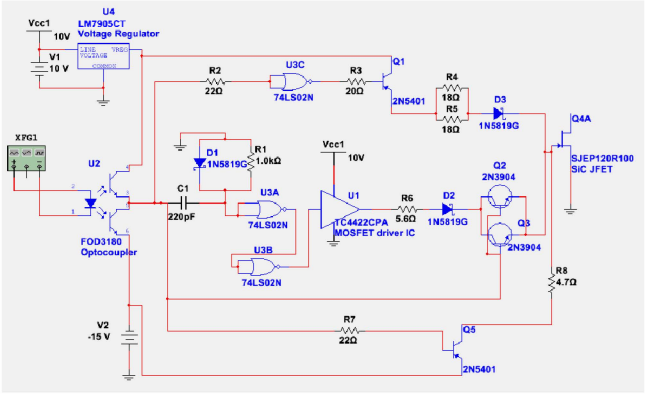

Fig.1 The circuit diagram of the proposed SiC gate drive

The duration of the current pulse to the SiC JFET gate can be controlled by varying the capacitance value. The pulse duration is kept to be less than 300ns to avoid over-driving the device.

For the turn-off part, a PNP BJT transistor Q5 is used to sink the discharging current from the JFET gate capacitance. To make sure that a larger current is sunk, the negative voltage of −15V in the circuitry is decided and it is the maximum negative voltage allowable on the JFET device gate.

The SiC JFET model shown in Fig. 2 is examined. The model can be used in LTSPICE circuit simulation to verify the proposed drive circuit before hardware implementation. The model is not the exact equivalent for the SiC JFET SJEP120R100 in comparison to its characteristics from laboratory measurement. However, it is a satisfactory model to be used. The model has the following important parameters:

Vto=0.9, Beta=16, Lambda=200u, Is=1f, N=3.4, Isr=1n, Nr=6.8, Cgd=1n, Cgs=610p, Rd=45m, Rs=20m, Rg=530m.

These parameters have significant influences on the device threshold voltage, drain and gate terminal characteristics.

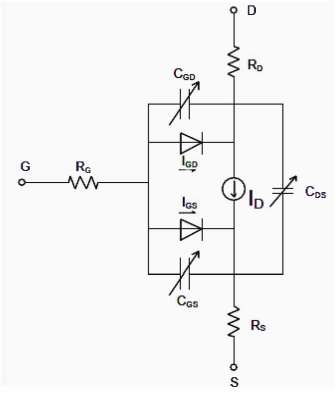

Fig.2 The SiC JFET model used in circuit simulations

Other device models which are close to the input/output characteristics of the real components are used. The HCPL-3150 optocoupler and IXDD409 MOSFET driver IC is used to mimic the actual hardware components respectively. The HCPL-3150 has a similar 20V output swing as the U2 FOD3180 hardware device used in the circuit. Also, the IXDD409 has a similar 9A current peak output rating as the U1 TC4422CPA device used. The rest of the components used in the simulation are the same as the actual hardware components such as 2N5401, 2N3904 and 1N5819 devices. The simulation condition is set at 30V drain side voltage with a 220Ω resistive load.

Fig. 3 shows the simulation results. The device is able to switch appropriately within the gate voltage level of 2.5V to −15V. The gate current has a pulsed peak during turn-on and turn-off period to quickly charge and discharge the gate capacitances.

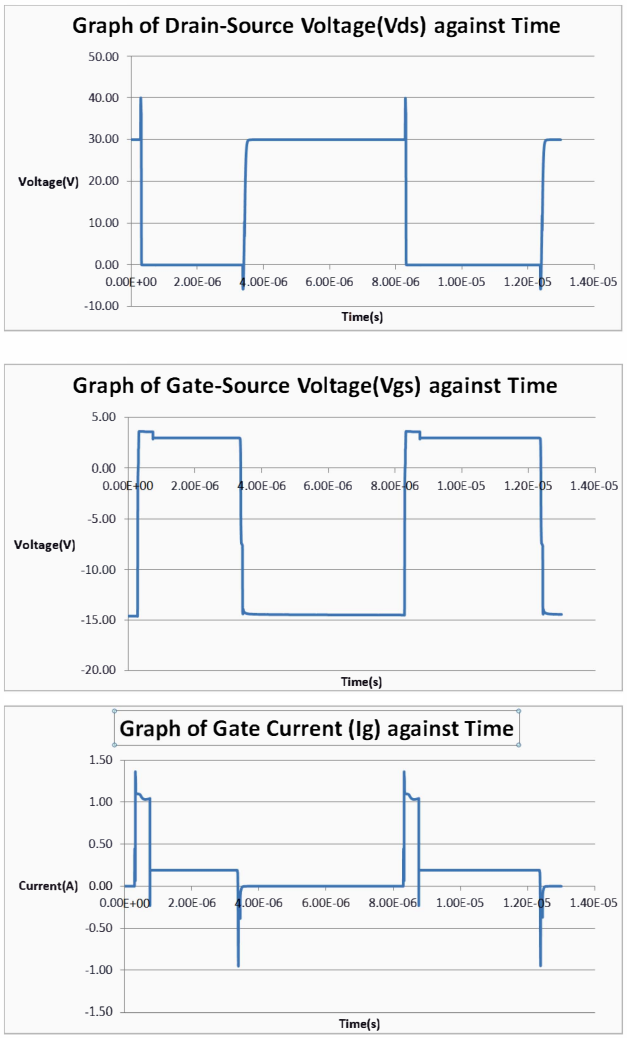

Fig.3 Output waveforms from the LTSPICE simulation on the proposed gate drive circuit during JFET switchings. Top trace: drain-source voltage; middle trace: gate-source voltage and bottom trace: gate current

III. HARDWARE VERIFICATION

Fig.4 shows the hardware circuit implemented. The mesurement waveform is shown in Fig.5. It is observed that the gate to source voltage is at an appropriate level whereby the voltage is maintained at 2.8V during the on-state. This is proper to keep the JFET at on-state during conduction period. Meanwhile, the gate current peaked at a value of around 650mA for about 400ns to quickly turn on the JFET and a negative peak current of around 400mA for about 100ns to quickly discharge the JFET. For the turn-on transition, the rise time is approximately 40ns, while the turn-off fall time is approximately 100ns. The hardware is built with components totaling about Singapore dollar $10.25 (about US dollar $8.20) which is shown in Table I.

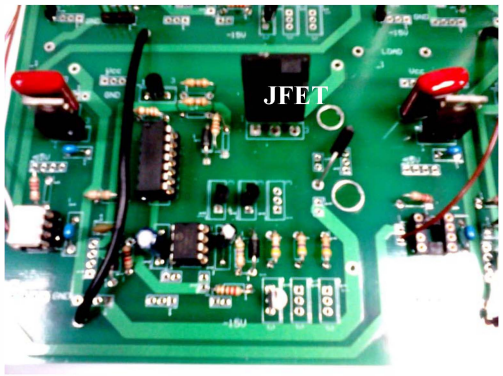

Fig.4 The gate drive circuit on PCB

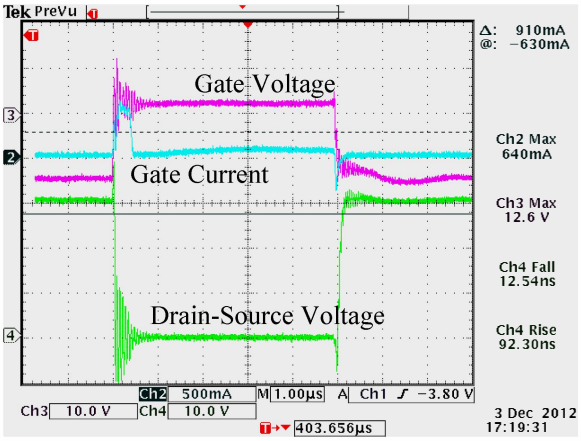

Fig.5 Measurement waveforms: Time scale 1µs/div; Gate voltage 10V/div; Gate current 500 mA/div; Drain-source voltage 10V/div

IV. TEMPERATURE EFFECT

JFET Transistors tend to have different characteristics under higher temperature. In this section, investigations on the characteristics of the SiC JFET at different temperatures were done with the focus on its on-state voltage and switching times. The experimental results are compared with those by LTSPICE simulation.

Table I: List of components and their cost

No.	Component	Quantity	Cost (S$)
1	µ7805 regulator	1	0.40
2	SN74LS02N NOR	1	0.94
3	1N5819 Diode	3	0.45
4	FOD3180 Optocoupler	1	2.50
5	TC4422CPA Driver	1	3.66
6	2N5401 PNP	2	0.48
7	2N3904 NPN	2	0.34
8	0.33µF Cap.	1	0.25
9	0.1µF Cap.	1	0.10
10	68pF Cap.	1	0.03
11	4.7µF Cap.	1	0.30
12	0.25W Resistors	10	0.80
	Overall Cost		**10.25**

Looking into the LTSpice SiC JFET model, there are 3 parameters which contain temperature coefficients. They are *VTO* (the threshold voltage), *Beta* (the β coefficient) and *IS* (the saturation current) of the device. Their respective coefficients are named *VtoTC, BetaTCE* and *XTI*. *VtoTC* affects the threshold voltage, *BetaTCE* affects the drain current level, while *XTI* affects the saturation level. The *VtoTC* parameter can be found in the datasheet, which is −2.0mV/°C. The *BetaTCE* value can be determined using a SPICE modelling formula based on the I_D-V_{DS} curve on the datasheet:

$$\beta(T_2) = \beta(T_1) \cdot 1.01^{BTCE \cdot (T_2 - T_1)} \quad (1)$$

The β value for each temperature can be calculated from the drain current equation:

$$I_D = \frac{1}{2}\beta(V_{GS} - V_T)^2 \quad (2)$$

Meanwhile, *XTI* can be determined from the modelling formula:

$$I_S(T_2) = I_S(T_1) \cdot \left(\frac{T_2}{T_1}\right)^{\frac{XTI}{N}} \cdot e^{\left(-\frac{qE_{G,(300K)}}{NkT_2}\cdot\left(1-\frac{T_2}{T_1}\right)\right)} \quad (3)$$

The *BetaTCE* is found to be −1.15A/V^2 and −120 after some fine-tuning of the values obtained from the equation. With the chosen values of *VtoTC*, *BetaTCE* and *XTI*, the simulated I_D-V_{DS} curves are fitting well to the waveforms found in the datasheet.

From the simulation results at the turn-off stage, it is found that the average increase in the turn-off time for every 25°C is 20.61ns. Meanwhile, for the on-state voltage level, the average increase in the level for every 25°C is 0.0505V.

For the hardware experiment, similarly, the device is heated up from 25°C to 50°C, 75°C and 100°C. The resistive load used for this experiment is 10Ω at a drain voltage of 25V. The experimental data showed much less variation. The turn-off waveforms are shown in Fig.6 for 25°C and 100°C.

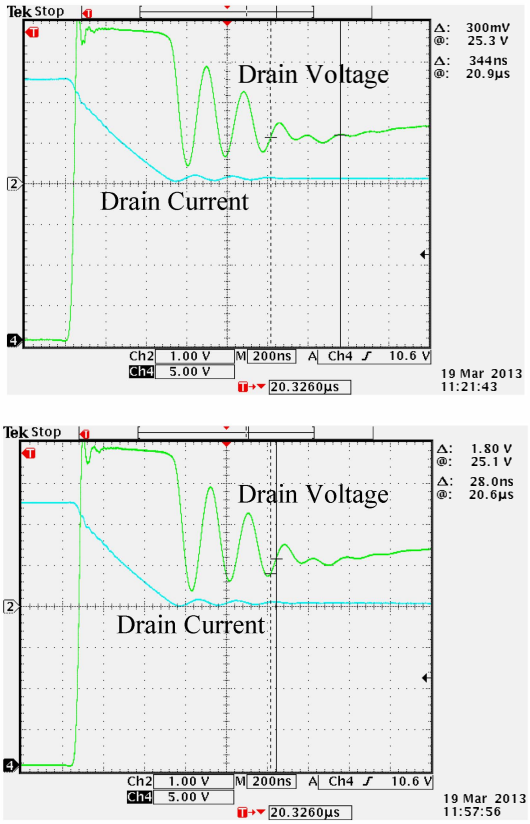

Fig. 6 Turn-off transitions at 25 °C (top) and 100 °C (bottom).

Table II shows comparison between the simulation and the experimental results on the variation of turn-off time and on-state voltage level at different temperatures. The LTSPICE model gives a closer match on the variations of on-state voltage than the turn-off time.

Table II Comparison on the variations of on-state voltage and turn-off time with temperature by using the proposed gate drive circuit

	On-state Voltage Level		Turn-off Time	
	Sim.	Exp.	Sim.	Exp.
Variations	+2.02 mV/°C	+2.4 mV/°C	+0.825 ns/°C	+0.4 ns/°C

V. CONCLUSION

A low-cost design of the gate drive circuit for edhancement mode SiC JFET SJEP120Rw-- has been designed and implemented. The laborator measurement showed that the performance is satisfactory for its switching and on-state performance. Besides that, the effect of temperature on the device is also investigated and compared. The proposed gate drive provides a low-cost solution for the SiC JFET gate drive system.

ACKNOWLEDGMENTS

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