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'Junction-Level' Heterogeneous Integration of III-V Materials with Si CMOS for Novel Asymmetric Field-Effect Transistors

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by

Yoon Jung Chang

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ABSTRACT OF THE DISSERTATION

‘Junction-Level’ Heterogeneous Integration of III-V Materials with Si CMOS for Novel Asymmetric Field-Effect Transistors

by

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Professor Jason C.S. Woo, Chair

Driven by Moore’s law, semiconductor chips have become faster, denser and cheaper through aggressive dimension scaling. The continued scaling not only led to dramatic performance improvements in digital logic applications but also in mixed-mode and/or communication applications. Moreover, size/weight/power (SWAP) restrictions on all high-performance system components have resulted in multi-functional integration of multiple integrated circuits (ICs)/dies in 3D packages/ICs by various system-level approaches. However, these approaches still possess shortcomings and in order to truly benefit from the most advanced digital technologies, the future high-speed/high power devices for communication applications need to be fully integrated into a single CMOS chip. Due to limitations in Si device performance in high-frequency/power applications as well as expensive III-V compound semiconductor devices with low integration density, heterogeneous integration of compound semiconductor materials/devices with Si CMOS platform has emerged as a viable solution to low-cost high-performance ICs.

In this study, we first discuss on channel and drain engineering approaches in the state-of-the-art multiple-gate field-effect transistor to integrate III-V compound semiconductor materials with Si CMOS for improved device performance in mixed-mode and/or communication applications. Then, growth, characterization and electrical analysis on small-area (diameter < 100nm) complete selective-area epitaxy of GaAs/GaN will be demonstrated for achieving 'dislocation-free' III-V compound semiconductor film on a Si(001) substrate. Based on a success in dislocation-free heterogeneous III-V film growth, we propose a novel ultra-scaled 'junction-level' heterogeneous integration onto mainstream Si CMOS platform. Device architecture and its key features to overcome aforementioned challenges will be given to demonstrate the potential to improve the overall system performance with diverse functionality.

The dissertation of Yoon Jung Chang is approved.

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To God the Father, my dearest parents and my younger brother

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CHAPTER 1

Introduction

1.1. Overview

The silicon Complementary Metal-Oxide-Semiconductor (Si CMOS) technologies have been the mainstream in semiconductor IC industry for the past few decades. These transistors act as ideal voltage-controlled switches in digital logic applications and amplifiers in analog/RF applications. In order to achieve improved device performance in terms of speed and functionality with high packaging density at a reduced cost per chip, the physical dimensions of these transistors have been continually shrinking in accordance with Moore's law [1]-[4]. Moreover, size/weight/power (SWAP) restrictions on all high-performance system components have resulted in multi-functional integration of multiple integrated circuits (ICs)/dies in 3D packages/ICs by various system-level approaches such as System-in-Package (SiP) [5] and through-silicon via

(TSV) [6]. However, these approaches still possess shortcomings due to interconnect and power density issues as well as limited level of integration. In order to truly benefit from the most advanced digital technologies, the future high-speed/high power devices for mixed-signal and/or communication applications need to be fully integrated into a single CMOS chip. Such System-on-Chip (SoC) solution can provide diverse functionalities with unprecedented levels of integration. However, Si device performance is inadequate in communication applications where very high frequency and/or power are necessary, and therefore, III-V compound semiconductors have been extensively utilized due to their superior transport and breakdown characteristics. On the other hand, despite III-V compound semiconductor materials performance boost, they are not cost-effective and integration density is low. In this regard, heterogeneous integration of compound semiconductor materials/devices with Si CMOS platform in SoC applications has emerged as a viable solution to low-cost high-performance ICs. Currently, the highest performance SoC system can be achieved via integration of different technologies by integrating high-quality compound semiconductor materials on Si CMOS.

1.2 Motivation and Objectives

Although III-V compound semiconductor materials have a potential to offer excellent analog/RF/mixed-signal device performances owing to higher saturation velocity compared to their Si counterpart, state-of-the-art scaled III-V compound semiconductor channel field-effect transistor [7] resulted in inherently high off-state current (I_{OFF}) due to low density of states and high dielectric constants as well as small bandgap, which compromises the advantage of high performance by degrading device intrinsic gain (A_V), one of important analog/RF/mixed-signal figures-of-merit (FoM). Moreover, due to their small inversion layer capacitance, decrease in on-

state current (I_{ON}) has been observed, which will further worsen device cut-off frequency (f_T). Despite the aforementioned device degradation in III-V-based transistors, heterogeneous integration of these state-of-the-art small-bandgap III-V MOSFETs with Si substrates has been experimentally demonstrated by various approaches such as direct growth [8]-[17], wafer-bonding [18]-[24], top-down etch [25] and thin-layer transfer [26]. On the other hand, analog/RF/mixed-signal high performance devices have utilized state-of-the-art scaled Si CMOS, due to their high frequency performance obtained from aggressive scaling [27], [28]. Power MOSFETs also have been realized with Si utilizing SOI and/or laterally diffused MOSFET (LDMOS) structures [29], [30]. However, because of a trade-off in f_T vs. A_V with scaling as well as insufficient linearity at high frequency and lower breakdown voltage than that of III-V large bandgap compound semiconductor materials, these Si devices are inadequate in communication applications where very high frequency and power are necessary. GaN HEMTs and MOSFETs have recently emerged as state-of-the-art scaled III-V-based devices for the next-generation communication systems, since they possess both high frequency and power capabilities [31]-[36]. Nonetheless, these devices are mostly realized on SiC substrates [33]-[35] limiting cost-effective mass-production manufacturability. Recent achievements in GaN devices on Si substrates are mostly fabricated on Si(111) [31], [32], [36], lacking material/device integration with mainstream Si(100) substrates. Therefore, innovative device architectures and process integration techniques are required for low-cost high-performance ICs in SoC applications, integrating analog/RF/mixed-signal and high voltage/power devices into a single Si chip.

Key figures-of-merit for analog/RF/mixed-signal and high voltage/power applications are illustrated in Table 1-1. For analog/RF/mixed-signal device design, increase in transconductance (g_m) and decrease in gate capacitance (C_{gate}) due channel length scaling result in enhanced cutoff-

frequency (f_T). However, for deeply scaled MOSFETs, decrease in C_{gate} is limited by source/drain to gate overlap capacitances (C_{gs}/C_{gd}), and increase in g_m is limited by velocity saturation as well as source/drain parasitic series resistances. These lead to saturation of further enhancement in f_T. To effectively manage g_m improvement, transistors with long-channel-like behavior and high source injection velocity (and electric field) in the channel for efficient carrier transport are of great help. Moreover, the device intrinsic gain (A_V) can be improved as g_m and output resistance (R_{OUT}) increase. Despite the improvement in g_m as channel length is scaled down, R_{OUT} is degraded due to 2D electric field effects such as channel-length-modulation (CLM) and drain-induced barrier lowering (DIBL). Consequently, due to larger impact of DIBL on the R_{OUT} in the ultra-short-channel regime, the overall A_V is degraded. In addition, enhancement in g_m/I_{DS} ratio requires reduction in the channel length for the same bias condition (i.e. constant V_{DS} and I_{DS}). Moreover, A_V is a strong function of supply voltage (V_{DD}) and when R_{OUT} is small, any nonlinearity in R_{OUT} causes nonlinearity in output signal. V_{DD} also needs to be lowered as the channel length is reduced, which leads to reduced signal swing. For circuits limited by dynamic range, reduced V_{DD} is problematic since input/output headroom is severely restricted. For circuits limited by noise, decrease in V_{DD} results in linear increase in power to maintain the same signal-to-noise ratio (SNR). Threshold voltage, on the other hand, cannot be set high in analog data storage circuits due to limited V_{DD}, which leads to degraded performance due to high off-state leakage current (I_{OFF}). In order to resolve these issues, materials with high breakdown voltage are necessary to be utilized in analog/RF/mixed-signal and high voltage/power applications.

In this study, we adopt both channel and drain engineering approaches to address the aforementioned challenges, and ultra-scaled 'junction-level' heterogeneous integration of III-V materials with Si CMOS for novel asymmetric multiple-gate field-effect transistors is investigated

in detail. In fact, bandgap engineering (i.e. channel/drain engineering) in heterogeneous junction MOSFET structures potentially provides performance improvements in gain and linearity as well as power supply voltage for scaled CMOS in analog/RF/mixed-signal high voltage/power applications. The bandgap engineering parameters are as follow:

(1) Electron affinity (χ_e)

(2) Permittivity (ε)

(3) Bandgap (E_g)

The proposed device with innovations in both materials growth and architecture is expected to realize multi-functional integration of 'defect-free' heterogeneous junction 3D transistors with wide bandgap drain and high mobility channel on ULSI Si CMOS platform. By combining compound semiconductor heterogeneous transistor performance with ULSI level of integration density, transistor option for analog/RF/mixed-signal high voltage/power applications in SoC platform can be effectively realized.

Table 1-1 Key Parameters of Analog/RF/mixed-signal and High Voltage/power Applications

Analog RF Applications	
Key Components	*Definition*
g_m	Transconductance
g_m/I_{DS}	Efficiency of the device
R_{OUT}	Output Resistance
A_V ($=g_mR_{OUT}$)	Intrinsic Gain
f_T	Cutoff Frequency
VIP_3	Linearity
Breakdown Voltage	Breakdown

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}},\ R_{OUT} = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1},\ \text{Av}=g_mR_{OUT}\ \textbf{(Intrinsic Gain)},\ f_T = \frac{g_m}{2\pi C_{gate}} = \frac{g_m}{2\pi (WL)C_{ox}}$$

1.3 Organization

The dissertation is organized as follows:

Chapter 2 introduces various issues and trade-offs in the current state-of-the-art Si and III-V channel MOSFET technologies with aggressive scaling in analog/RF/mixed-signal SoC applications. A detailed numerical simulation analysis on SOI vertical double-gate and planar tri-gate structures is performed to comparatively study their scaling impact on figures-of-merit in analog/RF/mixed-signal applications such as transconductance, initrinsic gain and cutoff frequency. The next section deals with process-induced variation study on the effect of different fin shapes in 14nm-node tri-gate MOSFET on the analog/RF/mixed-signal device performance metrics. Channel engineering approach including electron affinity and permittivity grading in the channel region is proposed to improve the aforementioned trade-offs in analog/RF/mixed-signal SoC applications. The concept as well as its impact on analog/RF/mixed-signal device performance is elaborated and studied in detail utilizing numerical simulations.

Chapter 3 focuses on a detailed simulation study of wide bandgap (i.e. GaAs/GaN) drain heterogeneous MOSFET for high power RF SoC applications to resolve the current problems in Si power devices. The concept and its structure are explained in detail. Optimization study of various device parameters in the proposed wide bandgap drain MOSFET is given throughout the chapter to understand their impact on high power RF device performance metrics.

Chapter 4 deals with experimental realization of feasibility in 'junction-level' heterogeneous integration of III-V materials with Si CMOS. Selective-area molecular-beam epitaxy (MBE) of GaAs/GaN nanostubs on SiO_2-nanopatterned Si(001) substrates utilizing aspect-

ration trapping (ART) technique is demonstrated in detail. The next section highlights the optimization of growth parameters to achieve high quality single-crystalline GaAs/GaN nanostubs with a complete selectivity. A detailed film characterization including defect quantification is performed to study the origins of defects inside GaAs/GaN nanostubs.

Chapter 5 introduces the fabrication of n+GaAs/p+Si(001) heterogeneous vertical PN diodes. Experimental study on different metal contacts to n+GaAs as well as its height variations is performed in detail to understand GaAs/Si(001) heterointerface quality. Current-voltage electrical characteristics of various sizes of n+GaAs nanostubs are shown to assess the feasibility of small-area MBE growth of these nanostubs with the help of ART technique. For realization of this concept, process flow design of wide bandgap drain heterogeneous multiple-gate MOSFET is detailed in the last section of this chapter.

Chapter 6, finally presents the conclusion by summarizing detailed simulation studies on nanoscale MOSFETs with respect to both low power analog/RF/mixed-signal and high power RF SoC applications, followed by MBE-based complete selective-area GaAs/GaN growth on Si(001) substrates with its PN diode current-voltage characteristics. Process flow design of GaAs/GaN drain heterogeneous multiple-gate MOSFET is illustrated utilizing the selective-area GaAs/GaN nanostub as a drain. Possible improvements as well as directions for the future work are briefly discussed in the following section.

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CHAPTER 2

Nanoscale MOSFET for Low-Power Analog/RF SoC Applications

2.1 Introduction

The current trends of continued scaling of transistor physical dimensions driven by Moore's law have gained remarkable breakthrough in its speed improvements. However, the aggressive scaling of Si MOSFETs has faced fundamental challenges: trade-offs in speed vs. power for digital logic applications and cut-off frequency vs. intrinsic gain for analog/RF applications. Decrease in improvement in the on-state current (I_{ON}) and rapid increase in the off-state current (I_{OFF}) resulted in exponential increase in static power dissipation. Moreover, degraded I_{ON} at low supply voltage to minimize the power consumption has limited the overall performance gain in Si devices for digital logic applications. Furthermore, ultra-high transconductance as well

as cut-off frequency are obtained as a result of scaling at the expense of degraded intrinsic gain owing to an exponential decrease in output resistance for analog/RF applications. Therefore, a great number of solutions to the drawbacks of Si MOSFET scaling with novel device processes/structures such as elevated source/drain structures [1], [2], high-k/metal gate stack [3], counter-doping, super halo [4], super steep retrograde channel doping [5], single pocket structure channel engineering techniques [6], Si-on-Insulator (SOI) MOSFETs [7]-[14], and/or double-gate MOSFETs/FinFETs [15]-[18] were experimentally demonstrated. More recently, development in bulk and SOI 3D tri-gate MOSFETs in production [19]-[22] led to a paradigm shift in Si IC industry, resulting in great improvements in device scalability and power dissipation in digital logic applications due to enhanced gate electrostatics compared to their planar counterpart. Moreover, System-on-Chip (SoC) approach has gained great interest for further overall system performance gain in mixed-signal and communication applications [19], [22]. However, regardless of the most advanced technologies, current short-channel ultra-thin SOI MOSFETs and FinFET/tri-gate MOSFETs have difficulty in achieving both ultra-high cut-off frequency (>200GHz) and intrinsic gain (>20) [23]-[26]. Additionally, extensive theoretical study on device physics of these novel architectures is still insufficient in terms of analog/RF/mixed-signal device performances.

Not only novel processes/structures but also high mobility channel materials such as Ge/SiGe [27], [28] and III-V materials [29]-[31] have been widely integrated with Si CMOS platform as a means to overcome the aforementioned limitation in the overall Si device performance for digital logic applications, i.e. degraded I_{ON} at low supply voltage. However, unlike superior analog/RF/mixed-signal device performances [32]-[35], scaled III-V channel MOSFETs have high I_{OFF} [36], [37] that compromises the advantage of their high performance capability.

Nonetheless, these short-channel high mobility channel MOSFETs utilized in thin-body SOI and/or non-planar multiple-gate device architectures [38]-[40] have shown feasibility of integration of III-V materials with Si CMOS for high-performance SoC applications. In this regard, it is imperative to find innovative channel engineering approaches to current scaled III-V channel MOSFETs, in order to gain performance improvements in digital logic and analog/RF/mixed-signal applications. Several methods of channel engineering such as lateral asymmetric doping profiles [41] and work-function engineering in a split gate [42] were reported in the past. These approaches successfully demonstrated device performance improvements in both digital logic (i.e. SS, DIBL, and I_{ON}) and analog/RF/mixed-signal applications (i.e. g_m and R_{OUT}). In this chapter, theoretical analysis on scalability of both vertical double-gate (DG) and planar tri-gate (TG) MOSFET structures for analog/RF/mixed-signal applications is given through numerical simulations. Impact of variations in fin shapes of the state-of-the-art 14 nm-node tri-gate transistor on analog/RF/mixed-signal performance metrics is then discussed to further investigate process variations and optimization strategies to improve analog/RF/mixed-signal figures-of-merit. Finally, the impact of asymmetric channel design solutions such as electron affinity grading as well as permittivity grading on various trade-offs that exist in metrics of analog/RF/mixed-signal applications is examined. This novel channel engineering approach is implemented in a III-V heterojunction thin-body multiple-gate MOSFET structure on a Si CMOS platform.

2.2 Three-dimensional Multiple-Gate Si MOSFET

2.2.1 SOI Vertical DG and Planar TG in Analog/RF/mixed-signal Applications

Sentaurus 2012, Synopsys 3D device simulation tool is utilized to perform comparative studies on the scaling impact of SOI vertical DG and planar TG MISFET structures on analog/RF/mixed-signal performances. A fully-depleted narrow-fin *n*-channel for both of these structures has been implemented in the device simulation, and these structures and their parameters are explicitly given in Figure 2.1 and Table 2-1. The basic structural parameters adopted in this set of simulations are based on Intel's 22 nm-node tri-gate high performance transistor option (L_G=30 nm, W_{fin}=8 nm, H_{fin}=34 nm and t_{ox}=0.9 nm) [43], [44]. The Intel's tri-gate device was designed in a way that resulted in subthreshold swing of 70 mV/dec and DIBL of 40 mV/V with unprecedented on-state characteristics. In the simulations, gap between S/D pads was assumed to be 130 nm (i.e. contacted gate pitch of 90 nm). Moreover, physical gate lengths have been varied from 20 nm to 350 nm in order to study the scaling impact of these devices on analog/RF/mixed-signal metrics. Oxide thickness of 1nm was chosen considering the trade-off between gate tunneling leakage (less than 1 nA/μm) and gate control (SS less than 70 mV/dec at V_{DS}=V_{DD}=0.8 V) in a scaled device of L_G=30 nm. Uniform doping profiles and abrupt junctions are assumed throughout all regions, and dopants are considered to be fully ionized. Moreover, ohmic contacts are assumed to rule out parasitic components such as contact resistance. Therefore, the main difference in the structure of vertical DG device with planar TG transistor is the inclusion of effect of spreading resistance in the device performance, which indeed is quite small in this set of simulations due to a heavily doped source region.

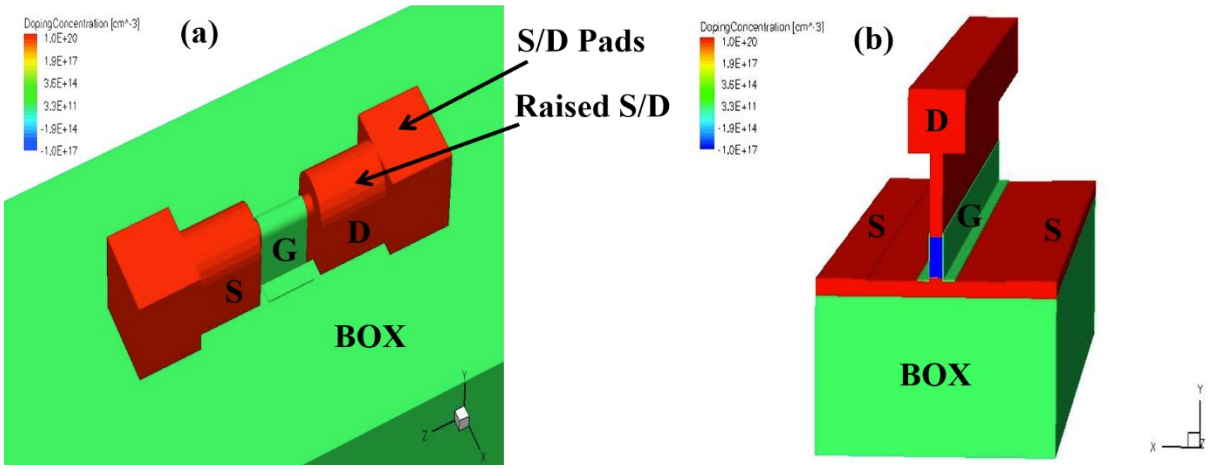

Fig 2.1 Schematic diagrams of fully-depleted SOI *n*-channel (a) TG and (b) DG MISFET structures

Table 2-1 Device Parameter Setup for Vertical DG & TG MISFET Structures

L_{gate} (nm)	20-350
W_{fin}/t_{body} (nm)	10
H_{fin} (nm)	35
W_{gate} (μm)	1
t_{BOX} (nm)	80
t_{ox} (nm)	1
Channel doping (cm^{-3})	$5x10^{18}$
S/D doping (cm^{-3})	$1x10^{20}$
S/D length (nm)	50
Substrate bias (V)	-2(TG)/0(DG)

Regarding the key simulation models, drift-diffusion (DD) transport model has been included in this set of simulations without calibration to the experimental data. This is a comparisons study with variations in the physical gate length and thus, it is more important to capture the difference in physics of vertical double-gate and planar tri-gate transistors than to simulate accurate values of performance metrics. Since hydrodynamic model overestimates the drive current without calibration, and Monte-Carlo (MC) simulation is computationally inefficient,

choosing the DD model is acceptable for the purpose of this set of simulations. Furthermore, Fermi-Dirac statistics model along with Shockley-Read-Hall (SRH) recombination model and Philips Unified mobility model which takes into account electron-hole scattering, screening of ionized impurities by charge carriers, and clustering of impurities have been adopted. Moreover, normal electric field dependent and high field dependent mobilities are considered in the simulation. Thin-body mobility degradation and quantization models are not considered since the channel thicknesses for both structures are kept the same throughout their device performance comparisons. It should be noted that this is a comparative simulation analysis and the actual values of the components in performance metrics can be different depending on the processing conditions, however, the trends are predicted to be the same as these results.

Corner conduction in DG MOSFETs is thought to be the extrinsic part of the device, and thus, it does not cause any degradation in their performance. However, the corner regions present in the TG MOSFETs, are indeed, considered as part of the intrinsic structure, and the current conduction in those regions are known to degrade the subthreshold characteristics of the device due to their early turn-on compared to the main channels. Various research groups have investigated methods to mitigate and/or eliminate this corner conduction in the TG MOSFETs [45]-[47], namely corner implantation and corner rounding. Therefore, for the planar TG transistor structure, corner implantation doping concentration and substrate bias are chosen for its electrostatic potential at virtual cathode point (i.e. position of minimum electrostatic potential along the channel) of top and bottom corners to be lower than that of top/lateral channels by ~5%. In this way, corner conduction is effectively suppressed. In order to ease the control of the complete elimination of the corner conduction in the subthreshold region, quite high channel doping concentration of $5x10^{18}$ cm^{-3} is chosen. This allowed the subthreshold current conduction to be

highly confined to surfaces. The virtual cathode point for each channel is illustrated in Figure 2.2. Moreover, small V_{DS} is chosen to make sure the corner regions turn on later than other channels, since top and lateral channel potentials are greatly affected by V_{DS} variation, compared to that in the corner regions. Figure 2.3 explicitly confirms the position of the current flow at different bias conditions.

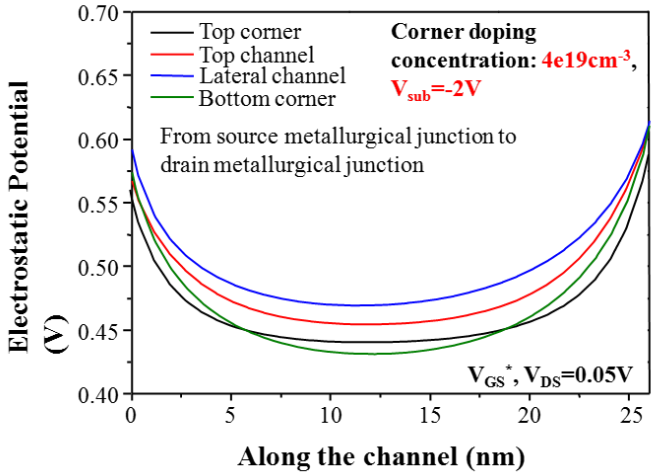

Fig 2.2 Electrostatic potential distribution along the channel at virtual cathode point in fully-depleted SOI *n*-channel planar TG MOSFET

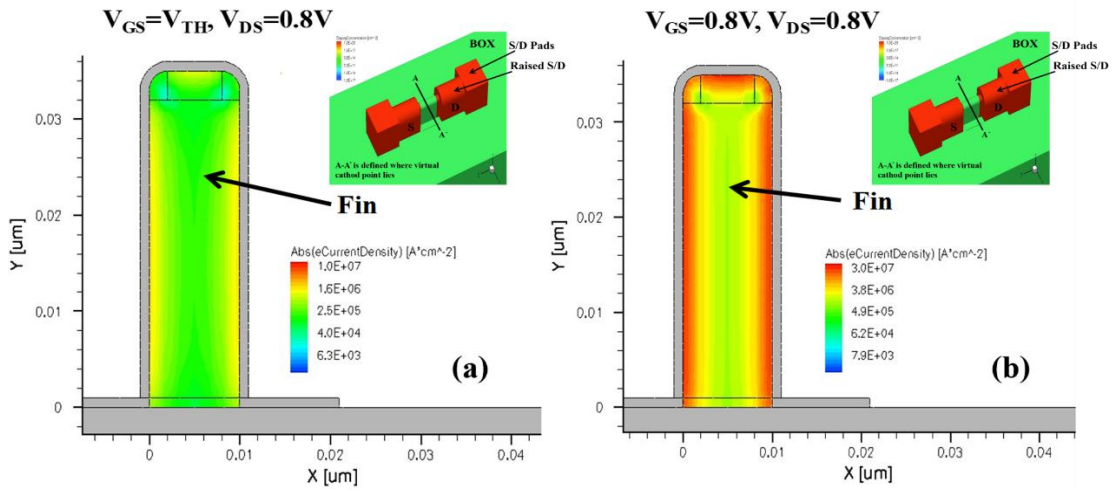

Fig 2.3 Schematic diagrams of electron current density in fully-depleted SOI *n*-channel planar TG MOSFET cut along fin-width direction (A-A') at (a) $V_{GS}=V_{TH}$, $V_{DS}=0.8$ V; (b) $V_{GS}=V_{DD}$, $V_{DS}=0.8$ V

The simulation results of the digital scaling impact on analog/RF/mixed-signal performances of vertical DG and planar TG device structures are illustrated in Fig. 2.4 using analog/RF/mixed-signal metric of transconductance to drain current (g_m/I_{DS}) ratio, intrinsic gain and cut-off frequency as well as their trade-offs. The g_m/I_{DS} ratio represents the efficiency of converting dc power into ac frequency, which is of great importance for low-power analog/RF/mixed-signal applications. At fixed I_{DS}, g_m/I_{DS} ratio improves as the physical gate length decreases due to an increase in g_m as the gate length becomes shorter, given in Figure 2.4(a). There is a degradation in g_m/I_{DS} ratio as the gate length is decreased to 20 nm because the subthreshold swing at this gate length reaches ~100 mV/dec, where as that of longer gate lengths is below 70 mV/dec. This is because initial optimization of device parameters was targeted for the physical gate length of 30 nm. Thus, applying thinner gate oxide and slight adjustment in channel doping concentration is expected for the gate length of 20 nm to follow the same trend previously

discussed. At fixed V_{GT}, g_m/I_{DS} ratio becomes almost constant in the saturation region but is lowered in the subthreshold region as the physical gate length is decreased, shown in Figure 2.4(b). With the given device parameters, no difference of g_m/I_{DS} ratio was observed in vertical DG and planar TG MOSFETs, despite higher g_m values of the planar TG than that of the vertical DG due to the existence of S/D spreading resistances in the vertical DG MOSFET.

Moreover, improvement in intrinsic gain of a planar TG device over a vertical DG MOSFET becomes higher as the physical gate length scales down, shown in Figure 2.4(c). This is mainly due to better DIBL performance of planar TG device over vertical DG one as the physical gate length is decreased owing to its additional top gate. No difference in g_m as well as R_{OUT} between TG and DG devices has been observed at physical gate length at 350 nm and beyond, resulting in no improvement in intrinsic gain. Cutoff-frequency (f_T) of both planar TG and vertical DG structures is enhanced as the physical gate length is decreased as in Figure 2.4(d). Higher f_T of planar TG device over vertical DG is observed within the given physical gate length. This difference between the two devices comes from different g_m and W (i.e. effective transistor width). In fact, f_T values were obtained from its first-order calculation of intrinsic cutoff frequency as $g_m/(WLC_{ox})$. A_V vs. f_T trade-off is shown in Figure 2.5(a). Lower S/D spreading resistances of planar TG device led to its improvement in this trade-off over the vertical DG one as I_{DS} increases at a fixed L_g and as L_g decreases at a fixed I_{DS}. In addition, as the physical gate length is reduced, planar TG device shows better g_m/I_{DS} vs. f_T trade-off (Figure 2.5(b)) than that of vertical DG one at a fixed I_{DS} due to a better g_m performance in the planar TG device. For g_m/I_{DS} vs. f_T trade-off at a fixed V_{GT} (Figure 2.5(c)), the planar TG MOSFET outperforms the vertical DG one as the device operates in the saturation regime. Since the impact of S/D spreading resistances is greater at higher

current level as well as shorter physical gate lengths, planar TG MOSFET architecture is more suitable for future high-performance analog/RF/mixed-signal SoC applications.

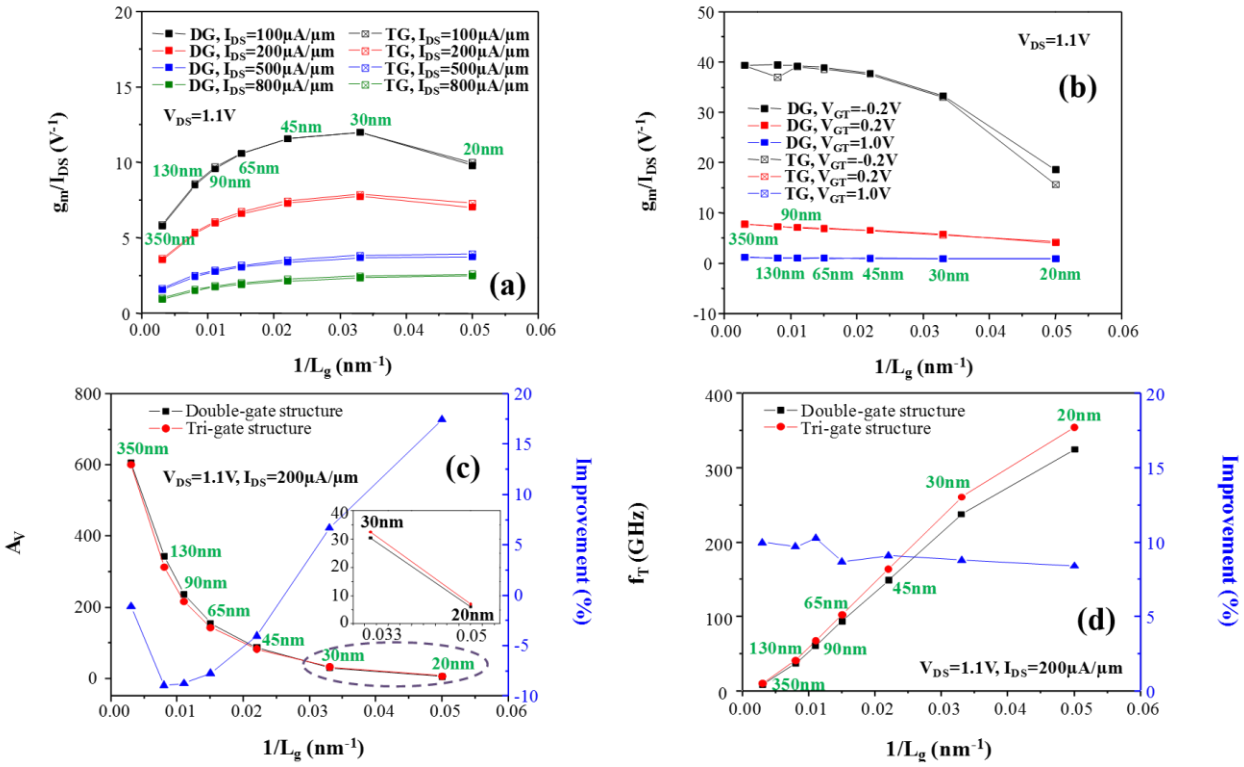

Fig 2.4 Plots of (a) g_m/I_{DS} ratio at fixed I_{DS}; (b) g_m/I_{DS} ratio at fixed V_{GT}; (c) intrinsic gain (A_V) at fixed I_{DS}; (d) cutoff frequency (f_T) at fixed I_{DS} for vertical DG and planar TG device structures

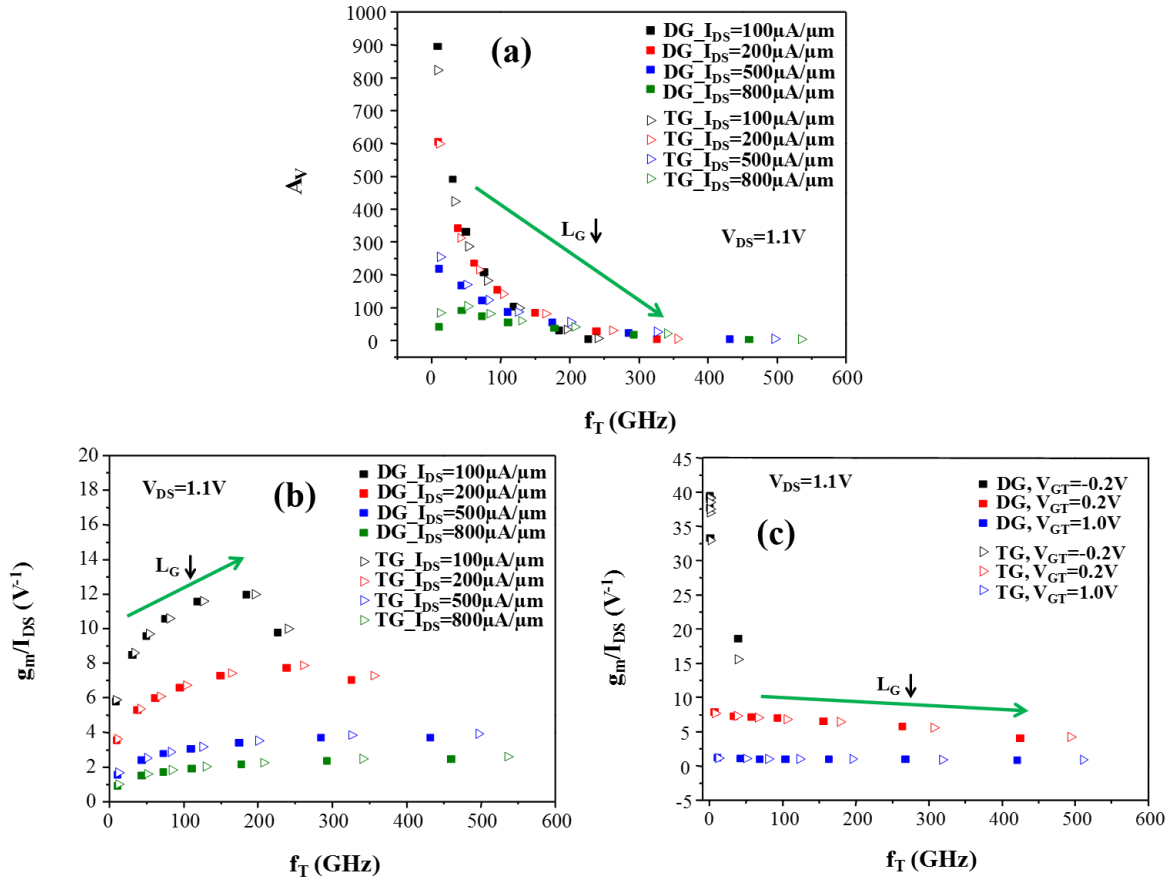

Fig 2.5 Plots of (a) A_V vs. f_T trade-off at fixed I_{DS}; (b) g_m/I_{DS} ratio vs. f_T trade-off at fixed I_{DS}; (c) g_m/I_{DS} ratio vs. f_T trade-off at fixed V_{GT} for vertical DG and planar TG device structures

2.2.2 Impact of Process Variation in Fin Shape on SOI TG Performance

Si tri-gate architecture has shown great digital logic performance improvements towards scaling into sub-20nm regime due to effective suppression of SCEs. However, as device dimension is shrinking, process-induced device variability is of a concern. Main variability sources of tri-gate/FinFETs are random dopant fluctuation (RDF) [48], [49], metal-gate workfunction variation [50]-[52], and dimension variations such as channel length and fin thickness variations [53]-[55]. Compared to RDF, variations in metal-gate workfuction and line-

edge roughness, impact of variations in fin shape on various device performances has not yet been extensively discussed, especially on analog/RF/mixed-signal device performances. Moreover, quantization and stress effects are expected to be different for different shaped fins, which will result in variations in device performances.

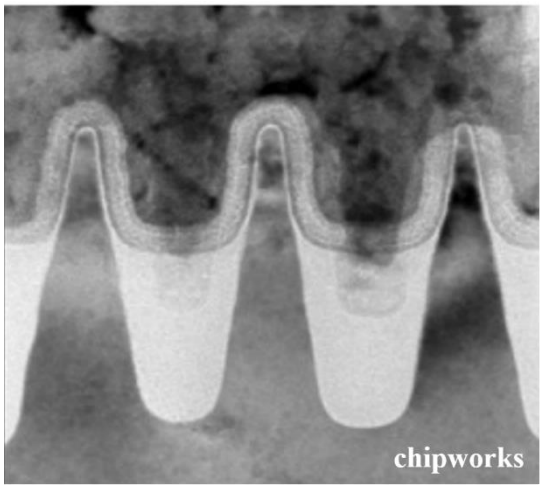

Fig 2.6 TEM image of Intel's 22 nm-node tri-gate NMOS gate and fin structures showing fin thickness variations taken by chipworks

Sentaurus 2012, Synopsys 3D device simulation tool is used to perform extensive analysis on the impact of fin shapes of planar SOI TG MISFET on analog/RF/mixed-signal performances. A fully-depleted narrow-fin *n*-channel Si bulk tri-gate structure in the simulation has been calibrated to Intel's 14 nm-node tri-gate MISFET [22]. Process simulation tool was utilized to generate the device structure with gate-last, high-k-first tri-gate device process flow given in Table 2-2. Due to unknown device parameters such as gate oxide thickness, channel doping concentration/profile, and S/D doping profiles from Intel's data, these parameters including spacer thickness were varied systematically during calibration. Stress components considered in the simulated structure are tensile stress due to SiC S/D, compressive stress due to wrap-around metal-

gate and tensile stress due to STI and contact metals. The simulated structures in different cut-directions and their parameters are explicitly given in Figure 2.7 and Table 2-3.

Multi-valley band structure model which uses analytic bands computed by two-band/6x6 k·p band structure physics model with the parabolic band assumption and Fermi-Dirac statistics applied to each valley is included for stress simulations. Bandgap narrowing and orientation-dependent quantization model (i.e. density-gradient quantum mechanical model) calibrated to both C-V and I-V experimental results are also incorporated. Calibrated drift-diffusion (DD) model has been considered for simulations of transport physics in this set of simulations, since hydrodynamic (HD) model with inclusion of quantization requires more than three fitting parameters due to a dependence of quantization on local temperature (energy) change. This complicates the calibration work compared with adopting DD model which only needs two fitting parameters (i.e. carrier mobility and velocity). Moreover, various mobility models such as orientation- and stress-dependent mobility as well as several degradation models are chosen with calibration. The calibrated overall results are shown in Figure 2.8. Due to various benefits of SOI structure such as low junction leakage and parasitic capacitances as well as ability to withstand high temperature and handle high voltage, it is a good choice for SoC applications, and therefore, SOI tri-gate MISFET structure is utilized in the simulations. After the calibration of bulk tri-gate device, its parameters have been implemented into the SOI counterpart, and the results are given in Figure 2.9.

Table 2-2 Process Flow of Gate-last/High-k-first Tri-Gate

Step	Details
(1)	Si fin formation on SOI substrate
(2)	High-k/SiO_2 deposition
(3)	Dummy poly-gate deposition/patternng
(4)	Spacer formation
(5)	SiC S/D epitaxy
(6)	S/D NiSi formation
(7)	Poly-gate removal
(8)	Metal-gate deposition/patterning
(9)	BEOL

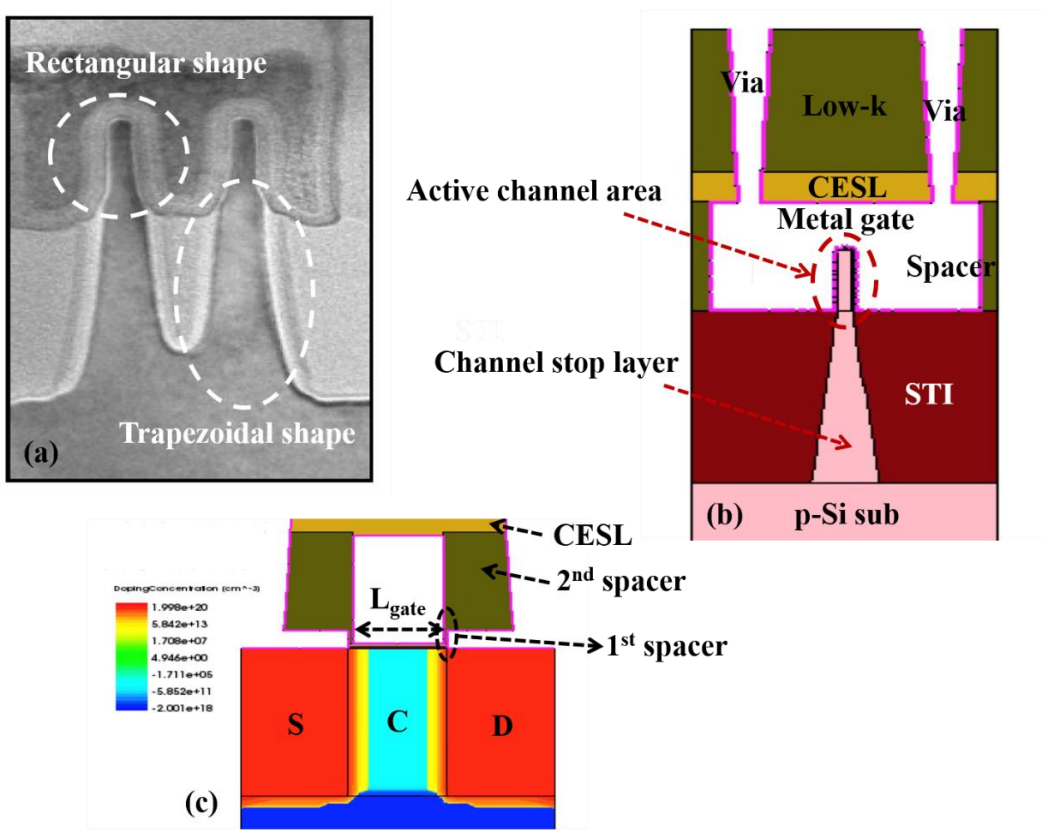

Fig 2.7 (a) XTEM image of Intel's 14 nm-node tri-gate NMOS device [22]; schematic diagrams of simulated 14 nm-node Si tri-gate MISFET structure cut along (b) fin width direction and (c) channel direction

Table 2-3 Simulated Device Parameters for 14nm-node Bulk Tri-Gate MISFET

L_{gate} (nm)	20
W_{fin} (nm)	8
H_{fin} (nm)	42
1st spacer thickness (nm)	1
2nd spacer thickness (nm)	10
STI thickness (nm)	120
Physical t_{gate} (SiO_2/HfO_2) (nm)	1.37 (0.6/0.77)
Gate thickness (nm)	32
Channel doping (cm^{-3})	$1x10^{15}$
Substrate doping (cm^{-3})	$1x10^{15}$
S/D doping (cm^{-3})	$2x10^{20}$
Gate pitch (nm)	70
Fin pitch (nm)	42

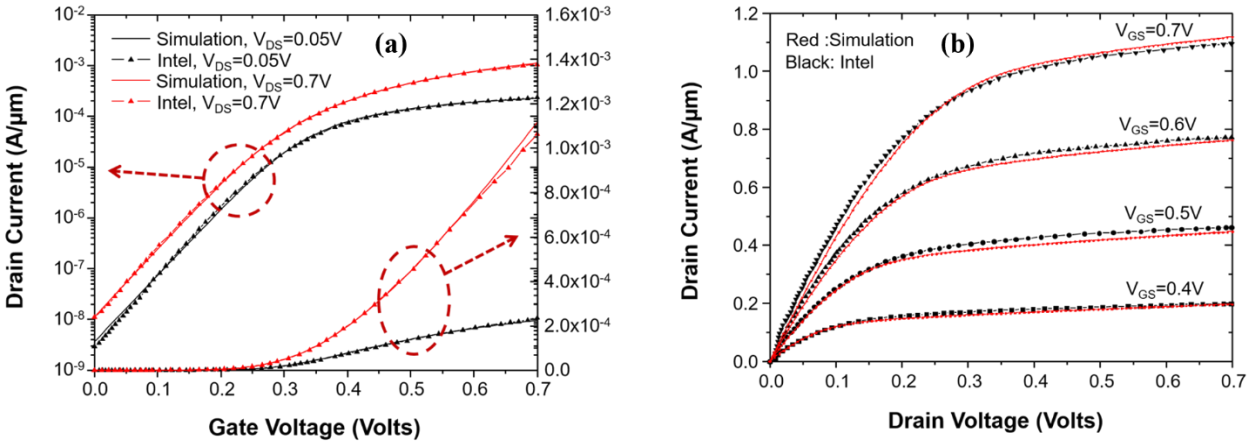

Fig 2.8 Calibrated results of a fully-depleted narrow-fin *n*-channel Si bulk tri-gate structure (a) transfer characteristics and (b) output characteristics

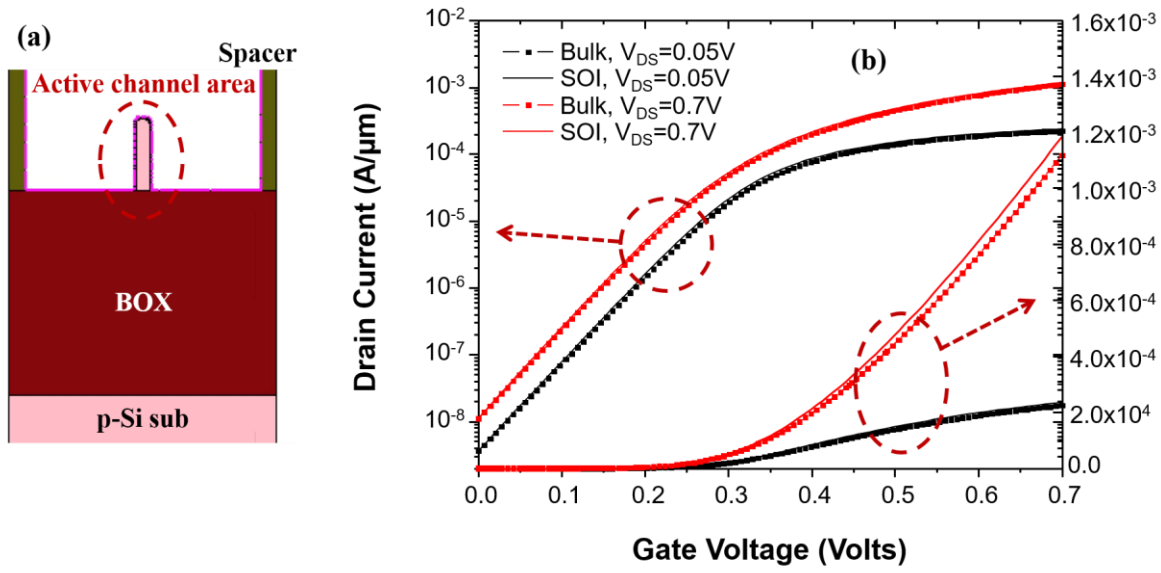

Fig 2.9 (a) Simulated 14 nm-node SOI tri-gate MISFET structure cut along fin width direction; (b) calibrated transfer characteristics of a fully-depleted narrow-fin *n*-channel SOI tri-gate structure

As can be seen from Figure 2.10(a), larger variations of device maximum transconductance with different fin shapes as spacer width is thinned down are observed. This is attributed to impact of variations in channel inversion charge distribution and average electron mobility as well as velocity with different fin shapes on the maximum transconductance given in Figure 2.11 and Figure 2.12. Extracted average tensile longitudinal stress inside the fin channel increases as the top fin width increases. This resulted in enhancement in electron mobility as the top fin width is increased. Electron current flow occurs in the middle of the fin channel even in the on-state due to stress and quantization effects, and thus, mobility and velocity are averaged out along the fin cross-section. However, as the spacer width is increased, impact of external S/D series resistance is pronounced, and therefore, variations in maximum transconductance with different fin shapes become less. On the other hand, drain current efficiency ($g_{m,sat}/I_{DS}$) is increased as the top fin width is decreased given in Figure 2.10(b). This is due to the fact that the drain current efficiency is

inversely proportional to threshold voltage to first-order. As the top fin width is decreased from rectangular shape (i.e. $W_{fin,top}$=8 nm) to triangular shape (i.e. $W_{fin,top}$=2 nm), threshold voltage increases. Thus, gate overdrive (V_{GT}) is decreased at the same V_{GS} as the top fin width is reduced. Moreover, as the spacer thickness is increased, the gate overdrive decreases and therefore, drain current efficiency increases. Since the motivation of this set of simulations is to study the effect of fin shapes on analog/RF/mixed-signal performance metrics, spacer width has been fixed to 1 nm throughout the simulations. In addition, output resistance of the device decreases as the top fin width is increased at various bias currents as in Figure 2.13(a). This is because rectangular fin shape (i.e. $W_{fin,top}$=8 nm) results in greater influence of V_{DS} on channel potential than that of triangular fin shape (i.e. $W_{fin,top}$=2 nm) observed in Figure 2.14. Intrinsic gain also follows the same trend as the output resistance (Figure 2.13(b)). Based on these simulation results, 12% variation in transconductance, 43% variation in output resistance and 22% variation in intrinsic gain at I_{DS}=300 µA/µm were observed. For low-power high-speed applications, it is advantageous to design a transistor with narrower fin widths for improvements in both drain current efficiency and intrinsic gain.

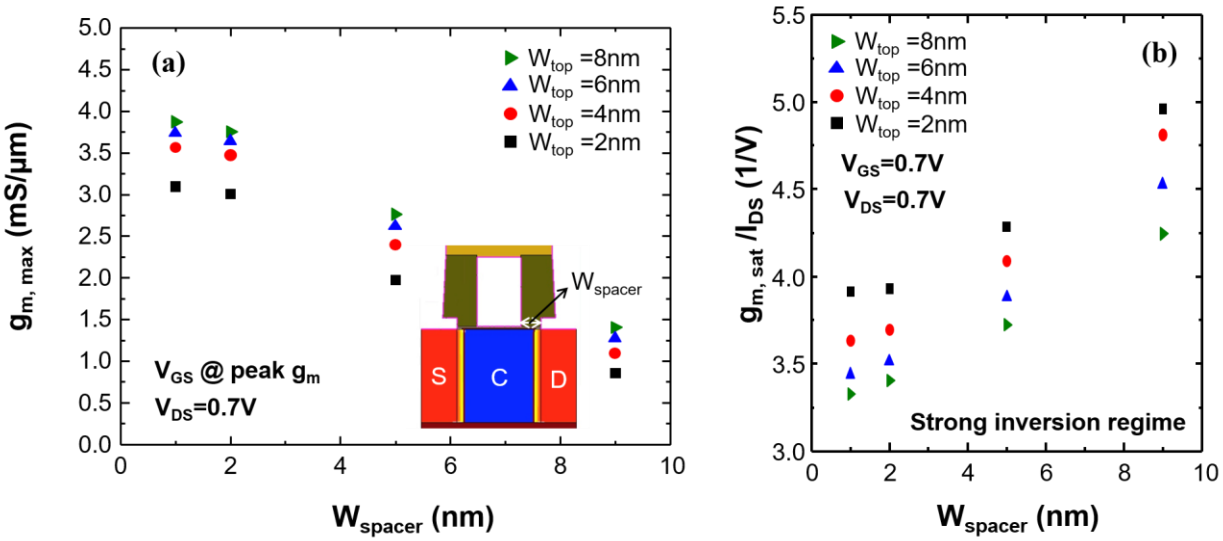

Fig 2.10 (a) Maximum transconductance ($g_{m,max}$) and (b) drain current efficiency ($g_{m,sat}/I_{DS}$) of a fully-depleted narrow-fin *n*-channel SOI tri-gate structure with variations in spacer widths for different top fin widths

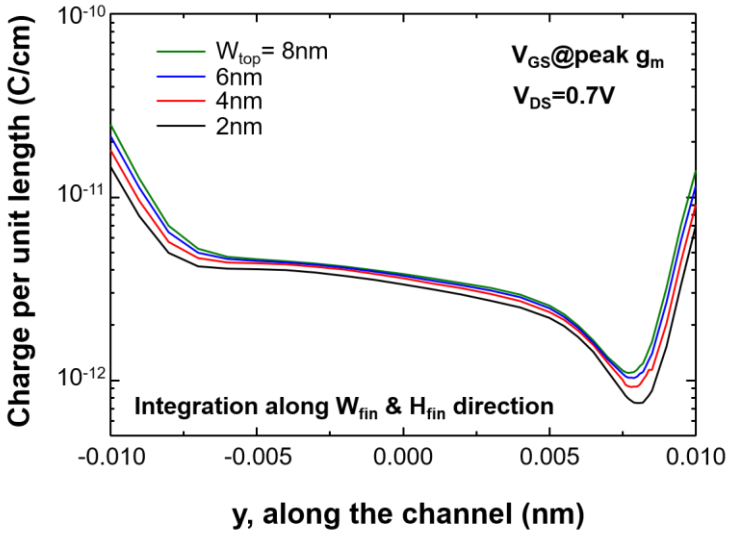

Fig 2.11 Inversion charge distribution along the channel with different top fin widths at V_{GS} @peak g_m and V_{DS}=0.7 V, integrated along fin width and height directions

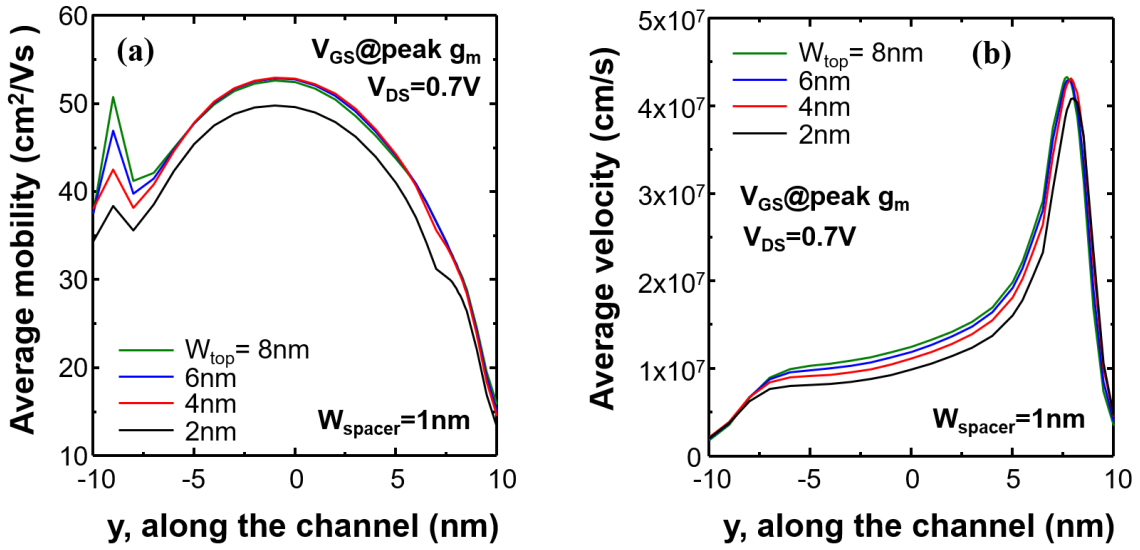

Fig 2.12 (a) Average electron mobility and (b) average electron velocity along the channel with different top fin widths at V_{GS} @peak g_m and V_{DS}=0.7 V

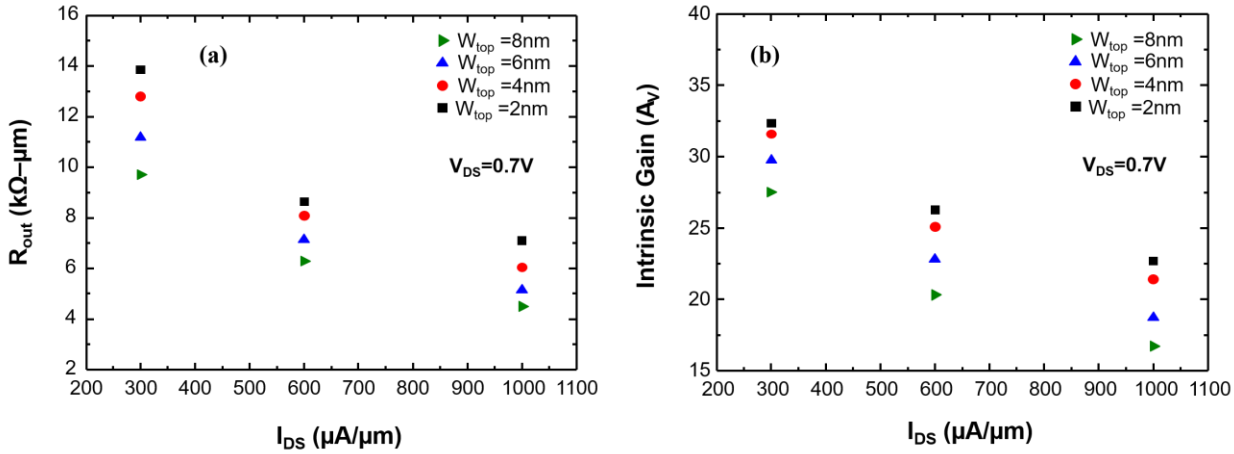

Fig 2.13 (a) Output resistance and (b) device intrinsic gain at various bias currents for different top fin widths with spacer width of 1 nm at V_{DS}=0.7 V

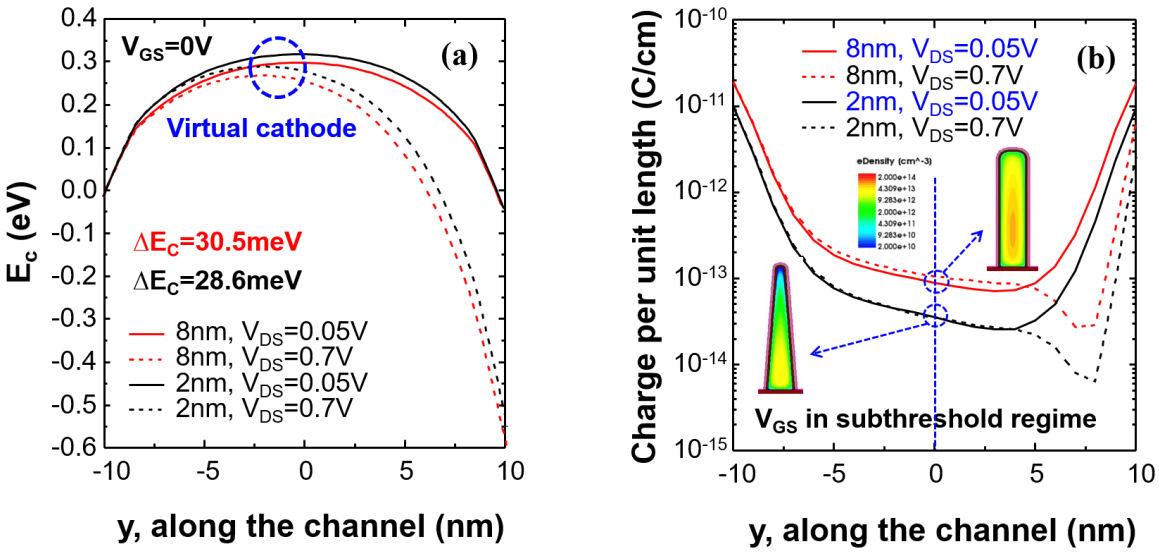

Fig 2.14 (a) Conduction band profile along the channel at V_{GS}=0 V and V_{DS}=0.05/0.7 V and (b) electron charge distribution along the channel at V_{GS} in the subthreshold regime and V_{DS}=0.05/0.7 V for $W_{fin,top}$=2 nm and 8 nm

2.3 Asymmetric Graded-Channel III-V MOSFET

Tailoring the potential profile along the channel by utilizing lower electron affinity near the source than that near the drain region helps improve SCEs such as DIBL and drive current as well as transconductance (g_m), which result in enhanced I_{ON}/I_{OFF} ratio, output resistance (R_{OUT}), intrinsic gain (A_V) and cut-off frequency (f_T). Graded electron affinity profile along the channel is given in Figure 2.15(a). First, lower electron affinity near the source region in the channel increases the source-to-channel diffusion barrier for electrons in weak inversion due to conduction band offset, which decouples the channel and drain, shielding the influence of the drain field penetration into the channel on source/channel potential barrier. Figure 2.15(b) clearly verifies the previous statement. This results in effectively controlled SCEs in terms of DIBL, which gives improved

R_{OUT} and A_V. Moreover, higher magnitude and gradient of lateral electric field compared to a homojunction provide increased average carrier drift velocity in the channel due to enhanced velocity overshoot. In the saturation regime, the drive current can be expressed as $I_{DS}=\upsilon(y)WC_{OX}(V_{GS}-V_{TH}(y)-V(y))$ at any position y where υ (y) is the average carrier drift velocity, V(y) is the channel potential and $C_{OX}(V_{GS}-V_{TH}(y)-V(y))$ is the inversion charge density, and therefore, I_{DS} and g_m as well as f_T can be improved owing to higher average carrier drift velocity near the source end compared with that of the homojunction. Furthermore, non-uniform channel potential profile reduces the peak lateral electric field near the drain region, and it creates local threshold voltage variation along the channel (i.e. higher local threshold voltage near the source compared to that near the drain region). This, in fact, results in a much more uniform inversion charge density along the channel even in the saturation regime of operation where variation in $V_{TH}(y)$ compensates for the increase in V(y) from source to drain. The reduced lateral electric field near the drain and uniform inversion charge density in the channel help minimize the velocity saturated region in the channel, reducing the channel-length-modulation (CLM) which also improves R_{OUT}. 2D device simulation results on inversion charge density and electron velocity profiles along the channel are shown in Figure 2.16. In addition, Figure 2.17 shows the enhanced lateral electric field close to the source region, resulting in improved current drivability, g_m and f_T.

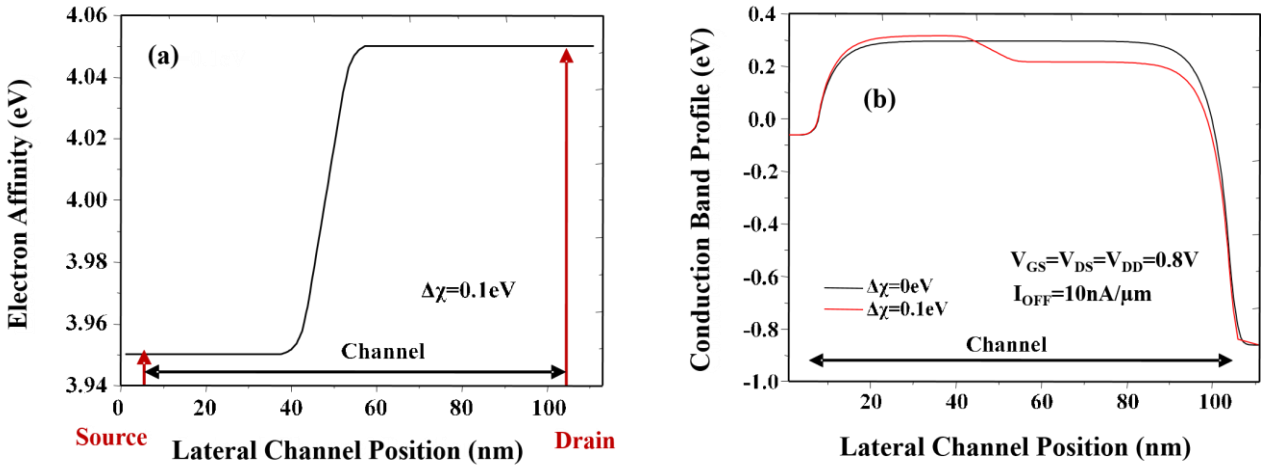

Fig 2.15 (a) Graded electron affinity profile along the channel (20 nm grading distance inside the channel region) and (b) conduction band profiles with and without electron affinity grading in the channel region (L_G=100 nm)

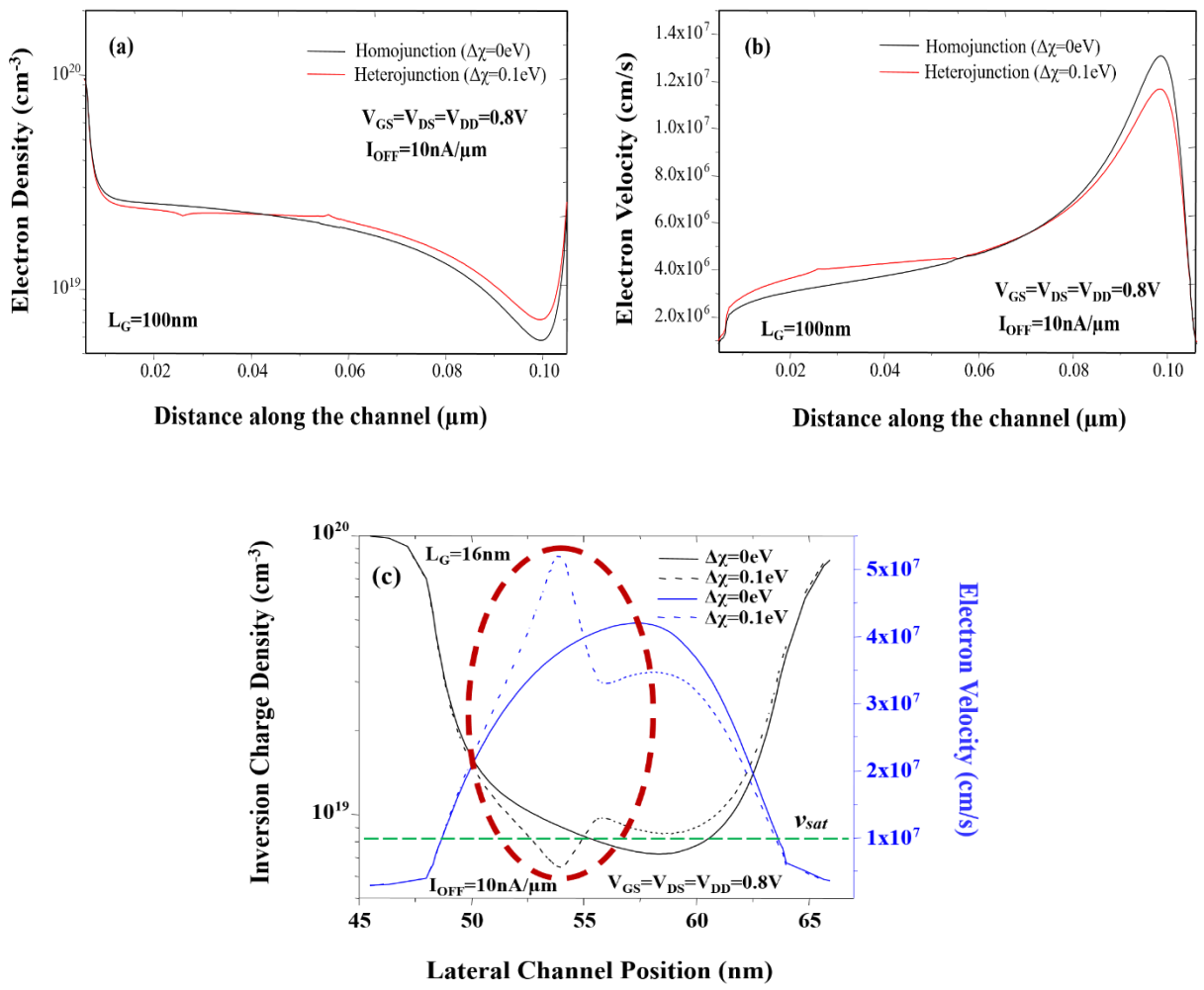

Fig 2.16 (a) Inversion charge density distribution and (b) electron velocity profile along the channel (L_G=100 nm); (c) inversion charge density distribution and electron velocity profile along the channel (L_G=16 nm) (More uniform inversion charge density along the channel and enhanced average carrier drift velocity near the source region for a graded heterojunction device)

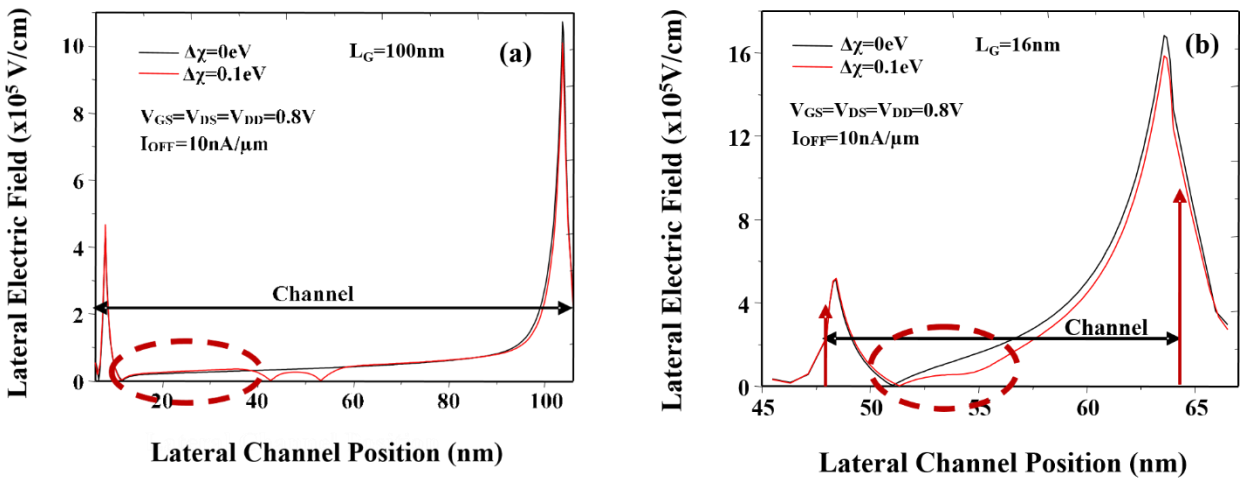

Fig 2.17 Lateral electric field distribution along the channel at (a) L_G=100 nm and (b) L_G=16 nm (increased lateral electric field near the source for a graded heterojunction device)

Since high mobility III-V channel devices suffer from a huge degradation in SCEs such as SS and DIBL due to high permittivity compared to silicon, permittivity grading having a lower value close to the drain compared to that near the source region helps suppress the SCEs, resulting in a better gate control over the channel in ultra-scaled III-V MOSFETs. The permittivity profile along the channel is illustrated in Figure 2.18. This asymmetric profile effectively suppresses the drain field penetration into the channel region and minimizes the drain field impact on the source-to-channel potential barrier. The physical explanation behind is that this scheme provides a steeper electric field near the drain compared to a device with the whole region having high permittivity and therefore, it ensures most of the voltage drop to occur near the drain side. Lateral and vertical electric field distributions are shown in Figure 2.19. The asymmetric permittivity profile gives higher vertical electric field near the source and the field is even higher than the lateral electric field. This results in a much improved gate electrostatics. Figure 2.20 clearly explains why the suppression of SCEs such as DIBL is more pronounced in the asymmetric device. Consequently,

improvements in DIBL and drive current are expected, resulting in further enhancement in R_{OUT} and A_V.

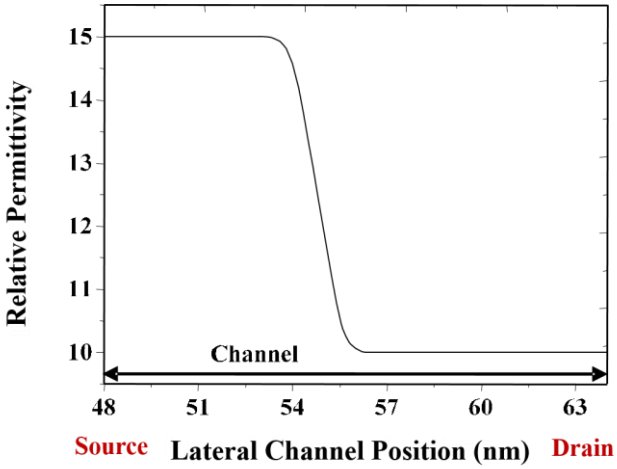

Fig 2.18 Graded relative permittivity profile along the channel (L_G=16 nm) (3 nm grading distance inside the channel region)

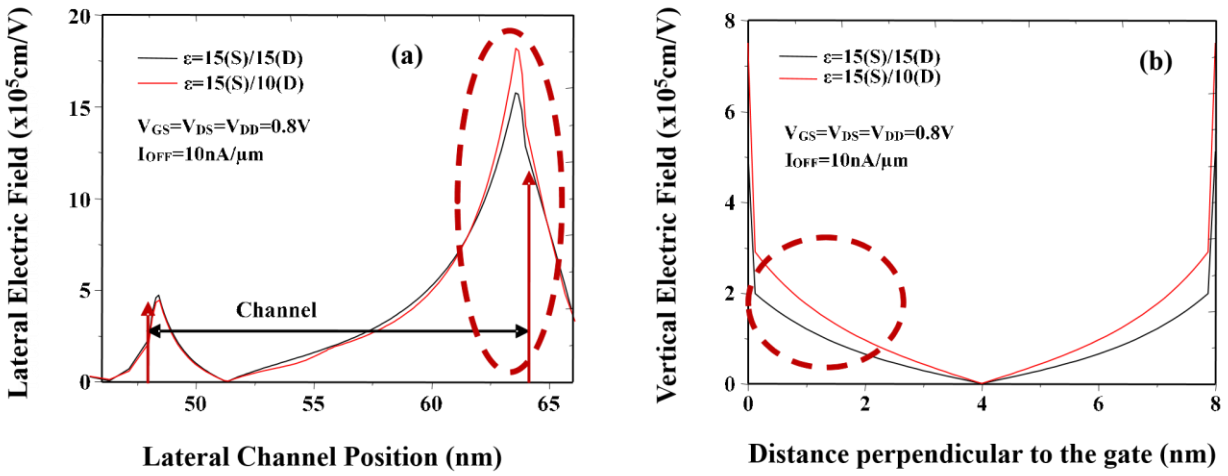

Fig 2.19 (a) Lateral electric field distribution along the channel (voltage drop that occurs in the drain region is increased in the case with ε=15(S)/10(D)); (b) vertical electric field distribution, cut along 1nm into the channel from the top of the source-to-channel barrier (vertical electric field is increased in the case with ε=15(S)/10(D), which translates to a better gate control over the channel) (L_G=16 nm)

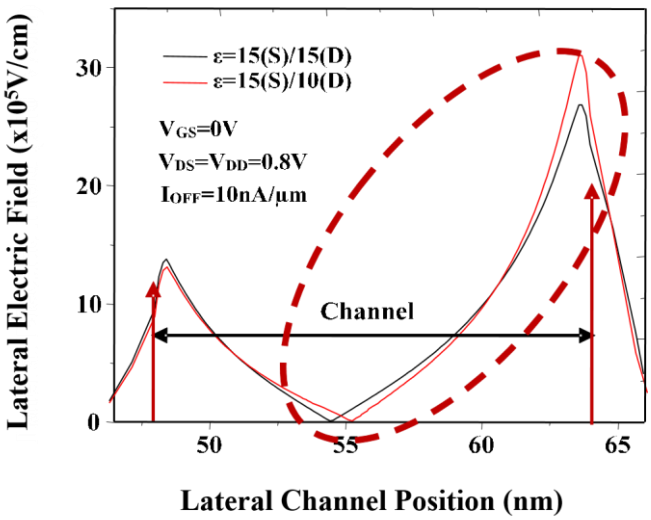

Fig 2.20 Lateral electric field distribution along the channel when V_{GS}=0 V and V_{DS}=V_{DD}=0.8 V (L_G=16 nm) (Less drain field penetration into the channel region in the case with ε=15(S)/10(D))

Sentaurus 2012, Synopsys 2D device simulation tool is used to study the impact of several major parameters of an ultra-scaled III-V heterojunction MOSFET such as electron affinity (i.e conduction band offset) and permittivity on the analog/RF/mixed-signal performance metrics. Moreover, investigation on their trade-offs in order to optimize the device for analog/RF/mixed-signal applications is performed. Double-gate structure with a graded heterojunction is implemented in the device simulation and is explicitly shown in Figure 2.21. Physical gate lengths have been varied from 100 nm to 16 nm, and gate oxide thickness of 1 nm is chosen considering the trade-off between gate tunneling leakage (less than 10 nA/μm) and gate control (SS less than 90 mV/dec at $V_{DS}=V_{DD}=0.8$ V) in a scaled device. With a well-controlled and optimized process, the gate tunneling leakage current can be as small as 10 A/cm^2 which can be translated to $1x10^{-8}$ A/μm and $1.6x10^{-9}$ A/μm for devices with gate length of 100 nm and 16 nm, respectively, assuming a linear dependence of the gate current on the gate length. However, the gate current decreases with a steeper slope as the gate length is decreased. Consequently, the gate tunneling current will have lower values than 10 nA/μm which is smaller than the I_{OFF} set as 10 nA/μm. The body thickness is kept at 8 nm with channel doping of $1x10^{17}$ cm^{-3} and source/drain doping of $1x10^{20}$ cm^{-3} for reasonably suppressed SCEs. Uniform doping profiles and abrupt junctions are assumed throughout all regions. Moreover, ohmic contacts are assumed to rule out parasitic components such as contact resistance. Bulk Si electron mobility of $1.42x10^3$ cm^2/V·s and bulk $In_{0.53}Ga_{0.47}As$ electron mobility of $1.13x10^4$ cm/V·s are used. $1.07x10^7$ cm/s and $3x10^7$ cm/s are also chosen for saturation velocities of Si and $In_{0.53}Ga_{0.47}As$, respectively in the simulations. In order to capture the increased gate capacitance of $In_{0.53}Ga_{0.47}As$ devices due to its quantum capacitance, EOT has been modified to 1.65 nm.

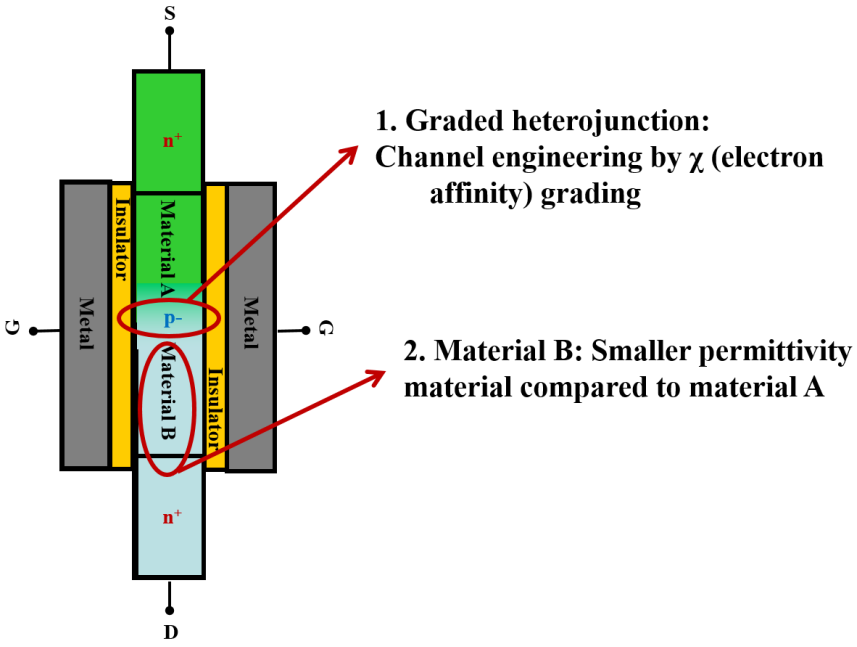

Fig 2.21 Simulated III-V channel double-gate MOSFET with channel engineering approach

Since deeply downsized devices cannot be properly described by conventional drift-diffusion transport physics model due to non-stationary carrier transport effects, hydrodynamic (i.e. energy balance) transport physics model has been included in this set of simulations. This model is based on the full set of transport equations derived from the Boltzmann transport equation (BTE) which takes into account both the momentum and energy relaxation effects. The model also provides carrier velocity dependence on local carrier temperature (energy) through the mobility which decreases as a function of the average energy owing to scattering at high fields. Due to this mobility dependence on the average carrier energy, the carrier velocity in this model is higher than that obtained from the drift-diffusion model. Although this model tends to overestimate the drive current, the model provides simpler means to correction by adjusting the relaxation time to match to the experimental or Monte Carlo simulation results. Since there is very little change in quantization effective mass (i.e. m_z) of both GaAs and InAs with channel thickness above 9 nm,

there is no change in transport effective mass of these channel materials in the scope of this set of simulation. Therefore, quantization model is not included throughout the simulations. Fermi-Dirac statistics model along with Shockley-Read-Hall recombination model and several mobility models including doping dependence, normal electric field dependence and high field dependence mobilities are also considered in the simulation. It should be noted that this is a simulation study and the actual values of the components in performance metrics can be different depending on the processing conditions, however, the trends are predicted to be the same as these results.

Analog/RF/mixed-signal performance of the simulated double-gate asymmetric device with an electron affinity grading is assessed in terms of transconductance, output resistance, cutoff frequency and intrinsic gain for various physical gate lengths as shown in Figure 2.22 through Figure 2.24. Although the improvement in analog/RF/mixed-signal performance decreases as a function of physical gate length, as high as 14 % improvement in intrinsic gain at a fixed I_{DS}=200 μA/μm as well as V_{DS}=0.8 V in a device with L_G=16 nm is achieved. The transconductance improvement in the heterojunction device with the electron affinity grading is due to enhanced source injection velocity which increases the current drivability and hence requires lower overdrive voltage than that of homostructures. Moreover, due to a huge improvement in DIBL, SCEs are effectively suppressed, increasing the gate electrostatics and lowering the overdrive voltage. Increase in transconductance will lead to increased cutoff frequency of the asymmetric heterojunction devices. As discussed in the previous sections, output resistance is further enhanced due to effective suppression of CLM as well as DIBL. Electron affinity grading scheme provides improvement in transconductance of about 3 % and the output resistance about 12 %, resulting in 14 % enhancement in intrinsic gain and 3 % gain in cutoff frequency of the device with L_G=16 nm. Therefore, electron affinity grading strategy is, indeed, effective in improving the intrinsic

gain of sub-100 nm devices since the output resistance significantly degrades as the device dimensions scale down to sub-45 nm.

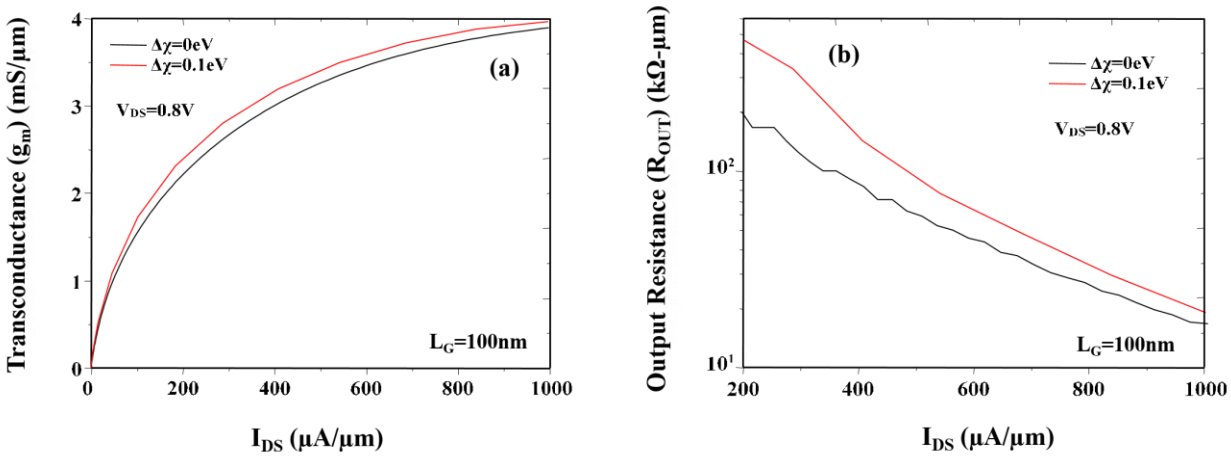

Fig 2.22 (a) Transconductance and (b) output resistance of the simulated double-gate device with electron affinity grading for a gate length of 100 nm at a fixed V_{DS}=0.8 V

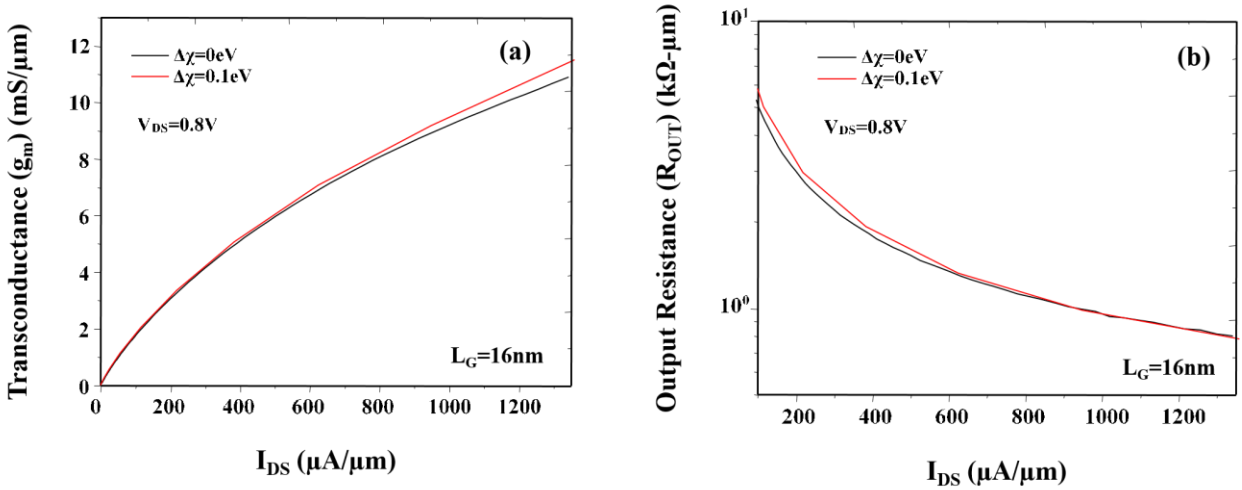

Fig 2.23 (a) Transconductance and (b) output resistance of the simulated double-gate device with electron affinity grading for a gate length of 16 nm at a fixed V_{DS}=0.8 V

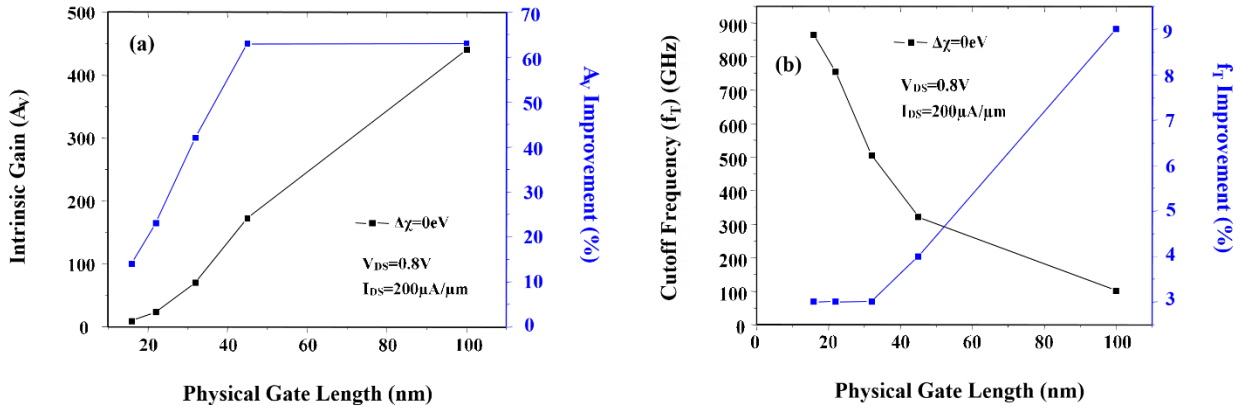

Fig 2.24 (a) Intrinsic gain with its improvement and (b) cutoff frequency with its improvement of the simulated double-gate device with electron affinity grading for various physical gate lengths at a fixed V_{DS}=0.8 V and I_{DS}=200 μA/μm

Furthermore, the effect of permittivity grading along the channel on metrics of the analog/RF/mixed-signal device performance is explicitly shown in Figure 2.25 through Figure 2.27. There is no improvement in transconductance as well as cutoff frequency of heterostructures compared to homostructures with permittivity of both 12 (i.e. Si) and 15 (i.e. InAs) in devices with L_G=32 nm down to 16 nm at a fixed I_{DS}=200 μA/μm and V_{DS}=0.8 V. These performance metrics degrades compared with homostructures with both ε=12 and ε=15 as the physical gate length becomes greater than 45 nm where SCEs are effectively suppressed. This degradation is owing to increased normal electric field at the surface due to smaller permittivity near the drain as discussed in the previous section. However, great enhancement in the output resistance as well as intrinsic gain compared to the homostructures with both ε=12 and ε=15 with the exception of the device with L_G=100 nm is obtained. These results are because of improvements in CLM and DIBL. For 100 nm gate length device, SCEs are effectively suppressed. Hence, this strategy fits in improving the device performance in analog/RF/mixed-signal applications, resulting in better improvements

towards short-channel length devices. Therefore, overall channel engineering strategy (i.e. electron affinity and permittivity grading) results in greater than 20 % and 30 % improvements in intrinsic gain compared to a Si and III-V homostructures, respectively, despite a decrease in device performance improvement with decreasing physical gate length. The channel engineering can realize a ultra-scaled III-V channel MOSFET with an improved trade-off between A_V and f_T.

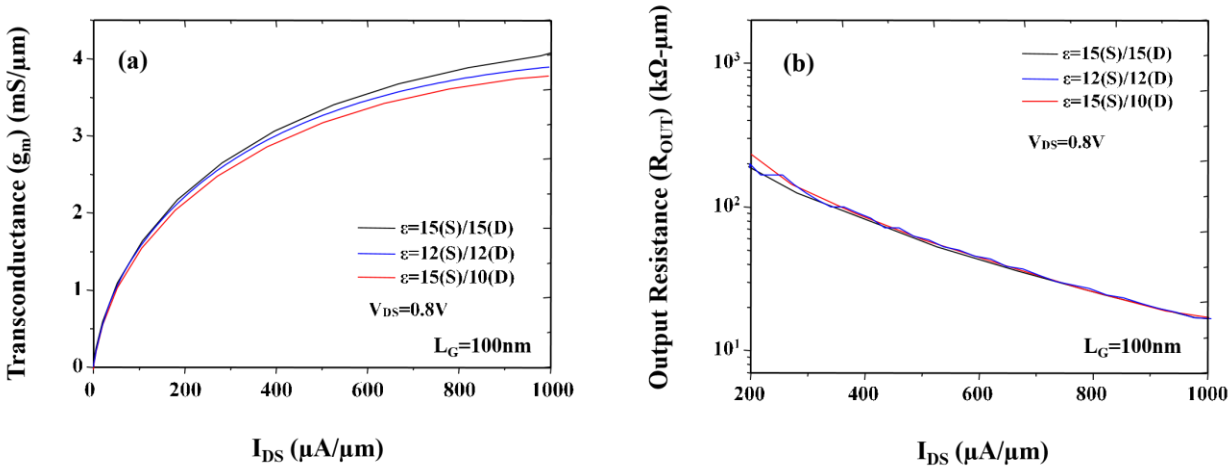

Fig 2.25 (a) Transconductance and (b) output resistance of the simulated double-gate device with permittivity grading for a gate length of 100 nm at a fixed V_{DS}=0.8 V

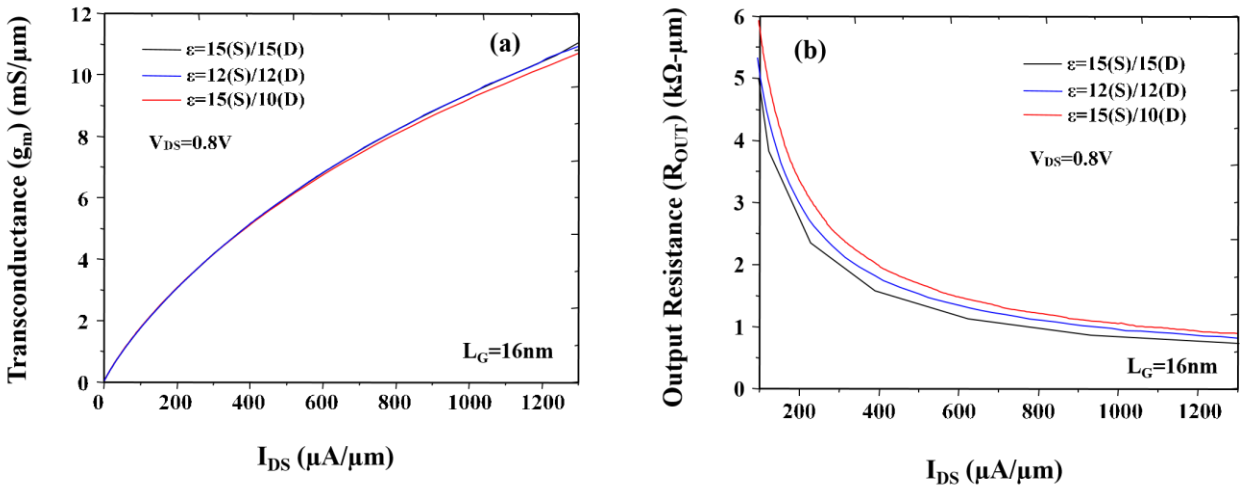

Fig 2.26 (a) Transconductance and (b) output resistance of the simulated double-gate device with permittivity grading for a gate length of 16 nm at a fixed V_{DS}=0.8 V

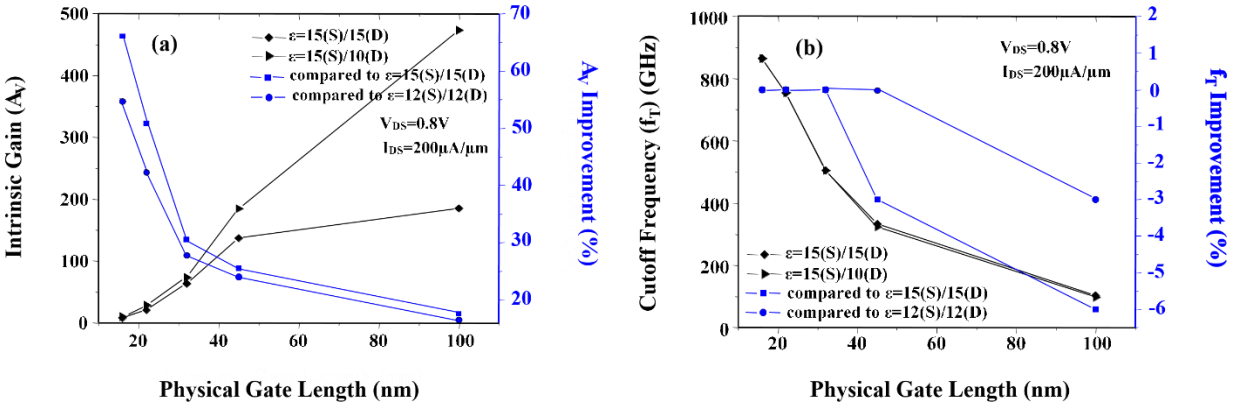

Fig 2.27 (a) Intrinsic gain with its improvement and (b) cutoff frequency with its improvement of the simulated double-gate device with permittivity grading for various physical gate lengths at a fixed V_{DS}=0.8 V and I_{DS}=200 μA/μm

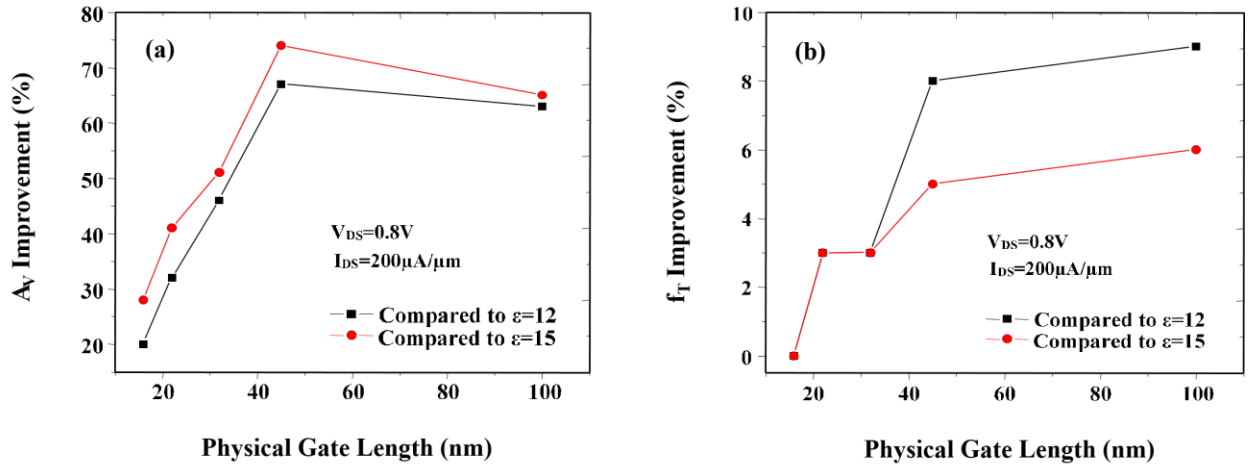

Fig 2.28 Overall analog/RF/mixed-signal performance metrics of asymmetric double-gate MOSFET with channel engineering: (a) intrinsic gain improvements and (b) cutoff frequency improvements for various gate lengths at fixed I_{DS}=200 μA/μm and V_{DS}=0.8 V

Other than the aforementioned analog/RF/mixed-signal metrics, linearity is as important figure-of-merit to assess the device performance. In order to study the improvements in linearity, investigation in the two different terms are necessary. One is third-order intermodulation (IM) intercept point and the other is 1-dB compression point. For a single-stage common-source amplifier, third-order IM intercept point is defined as an input gate bias amplitude at which amplitudes of 1st and 3rd order derivatives of drain current are equal. It can be expressed in the polynomial approximation to the 3rd order as follows:

$$VIP_3 = \sqrt{\frac{4}{3}\left|\frac{c_1}{c_3}\right|} \text{ where } y(t) \approx c_1 x(t) + c_2 x^2(t) + c_3 x^3(t)$$

$y(t)$: output, $x(t)$: input, memoryless and time-variant system

In addition, 1-dB compression point is defined as an input gate bias that causes the small-signal gain to drop by 1 dB and is expressed as the following:

$$P_{1dB} = \sqrt{0.145 \left|\frac{c_1}{c_3}\right|}$$

Performance comparisons of homostructure (i.e. ε=15) and heterostructure with channel engineering (i.e. $\Delta\chi$=0.1 eV and ε=15/10) for L_G=32 nm are made utilizing the two linearity figures-of-merit, given in Table 2-4. I_{DS}-V_{GS} transfer curve is fitted to a 3rd order polynomial (i.e. distortion in g_m) for first-order calculations. 25 % enhancement in linearity is obtained for a III-V channel heterostructure with channel engineering.

Table 2-4 Third-order Intermodulation (IM) Intercept Point/1-dB Compression Point

Device Structure	VIP_3 (V)	P_{1dB} (dBm)
Homostructure	0.684 (-13dBm)	-23
Heterostructure	0.867 (-11dBm)	-20

2.4 Summary

Numerical simulations on the scaling impact of vertical double-gate and planar tri-gate MOSFET structures have been performed by utilizing analog/RF/mixed-signal figures-of-merit. As the physical gate length scales down below 30 nm, planar tri-gate device outperforms the vertical double-gate due to effective suppression of drain field penetration into the channel region. This resulted in 10-20 % improvement in intrinsic gain of the ultra-scaled planar tri-gate structure. Moreover, impact of fin shape variations in state-of-the-art SOI 14 nm-node tri-gate MISFET on analog/RF/mixed-signal performance metrics was studied utilizing the numerical simulation tools.

The observation of 12 % variation in transconductance, 43 % variation in output resistance and 22 % variation in intrinsic gain at I_{DS}=300 µA/µm was made. Scaled SOI tri-gate MISFET with narrower fins is expected to give performance improvements in low-power high-speed SoC applications. Finally, channel engineering approach (i.e. electron affinity and permittivity grading) has been proposed in a scaled III-V MOSFET on a Si CMOS platform to enhance the trade-offs in g_m/I_{DS} vs. f_T and A_V vs. f_T. Despite a reduction in device performance improvement with shorter physical gate lengths, more than 20 % and 30 % overall performance enhancements in intrinsic gain were obtained compared to a Si and III-V homostructures, respectively. By utilizing this channel engineering concept in a planar III-V channel tri-gate architecture can further improve the trade-offs in g_m/I_{DS} vs. f_T and A_V vs. f_T.

2.5 Bibliography

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CHAPTER 3

Wide Bandgap Drain Heterogeneous MOSFET for High-Power RF SoC Applications

3.1 Introduction

Continued scaling of transistor dimensions driven by Moore's law resulted in dramatic performance improvements in digital logic as well as mixed-signal and/or communication applications as discussed in the previous sections. Despite advanced RF Si CMOS platforms, its inherently worse breakdown characteristics compared with III-V-based devices limited its usage in RF/mixed-signal and communication applications. For example, CMOS power amplifiers (PAs) have become the limiting components in RF CMOS transmitter ICs due to theoretical limit in their material properties [1]. Thus, extensive efforts still put into various approaches to heterogeneous IC/die integration in both device- and system-levels for continued high-performance system

development. In this regard, ultra-scaled 'junction-level' heterogeneous integration of 3D Si transistors with GaAs/GaN wide bandgap drain is proposed to resolve the issue of Si CMOS for high power RF SoC applications. The proposed device offers high breakdown voltage of GaAs/GaN and high frequency of scaled Si CMOS with ULSI level of integration density.

Performance of the proposed device has been estimated based on the experimental results of bulk Si and Si LDMOS transistors with L_g=0.18 μm [2], [3]. Minimum gate overlap and constant W with L is assumed. R·W is assumed to be proportional to $1/X_j$ and S/D length is kept the same for devices with different L. g_m is also assumed to be around 1.5 times larger for DG MOSFET compared to single-gate device. Moreover, device/process parameters for both L_g=0.18 μm and 32 nm are from International Technology Roadmap for Semiconductors (ITRS). Since drain current in the saturation regime ($I_{D, sat}$) is linearly proportional to V_{gs}' to first order in short channel devices, external transconductance ($g_{m, ext}$) for L_g=32 nm is twice higher than that of L_g=0.18 μm. Cut-off frequency (f_T) is therefore, 5 times higher for L_g=32 nm than that of L_g=0.18 μm, which gives f_T estimation of ~130 GHz for L_g=32 nm with inclusion of LDMOS structure. For RF PA circuits to achieve output power (P_{out}) of 20 dBm at 150-200 GHz, breakdown voltage of ~30 V is desirable, assuming a general RF block with 50 Ω termination for the input and output. Expected performance gain of the proposed device is summarized in Figure 3.1.

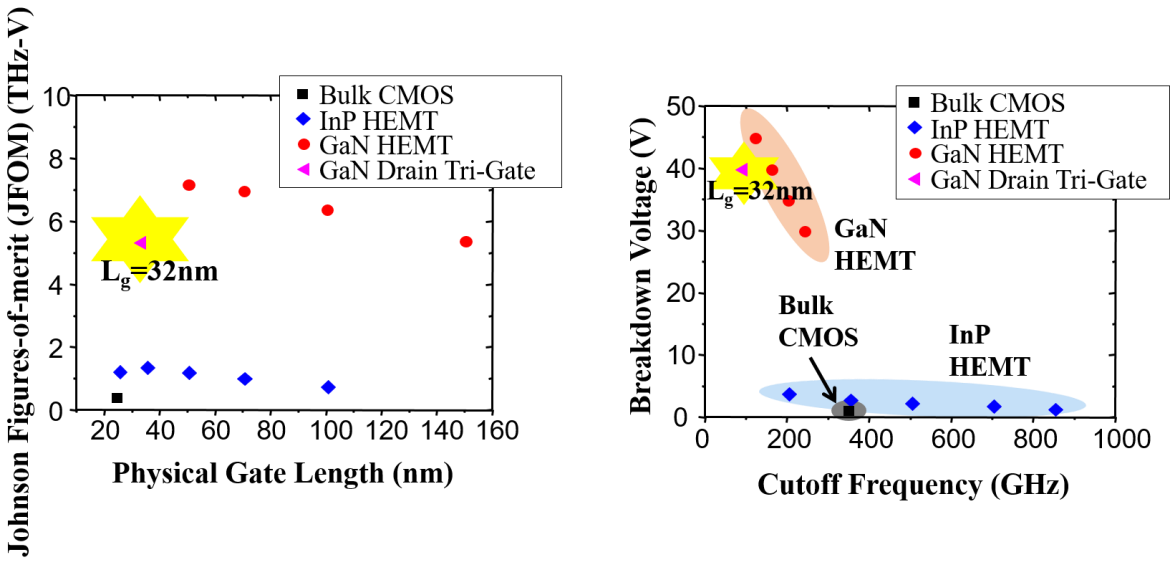


Fig 3.1 Expected performance gain of heterogeneous 3D transistor with GaAs/GaN drain, and its comparison with other state-of-the-art devices in mixed-mode and/or communication applications

3.2 Device Concept and Structure

The proposed device structure, a heterogeneous 3D transistor with wide bandgap GaAs/GaN drain on SOI CMOS platforms, is given in Figure 3.2. It utilizes reduced surface field (RESURF) concept to improve a trade-off in on-resistance (R_{on}) and breakdown voltage (V_{BD}). Having a fully-depleted multiple-gate MISFET architecture improves device scalability and breakdown voltage due to immunity from SCEs. It also helps enhance the current drive capability. Scaled Si channel provides cut-off frequency in the range similar to that of high frequency III-V devices. Additionally, wide bandgap zinc-blende GaN drain offers higher critical breakdown field/saturation velocity, absence of parasitic polarization field, higher doping efficiency and carrier mobility than that of wurtzite-phase GaN materials. In-situ *n*-doped GaN drain leads to reduction in parasitic S/D series resistances and defect reduction due to elimination of ion

implantation. SOI substrate, on the other hand, gives better isolation. Based on the key features of the proposed device, it is well suited for high voltage/power RF SoC applications.

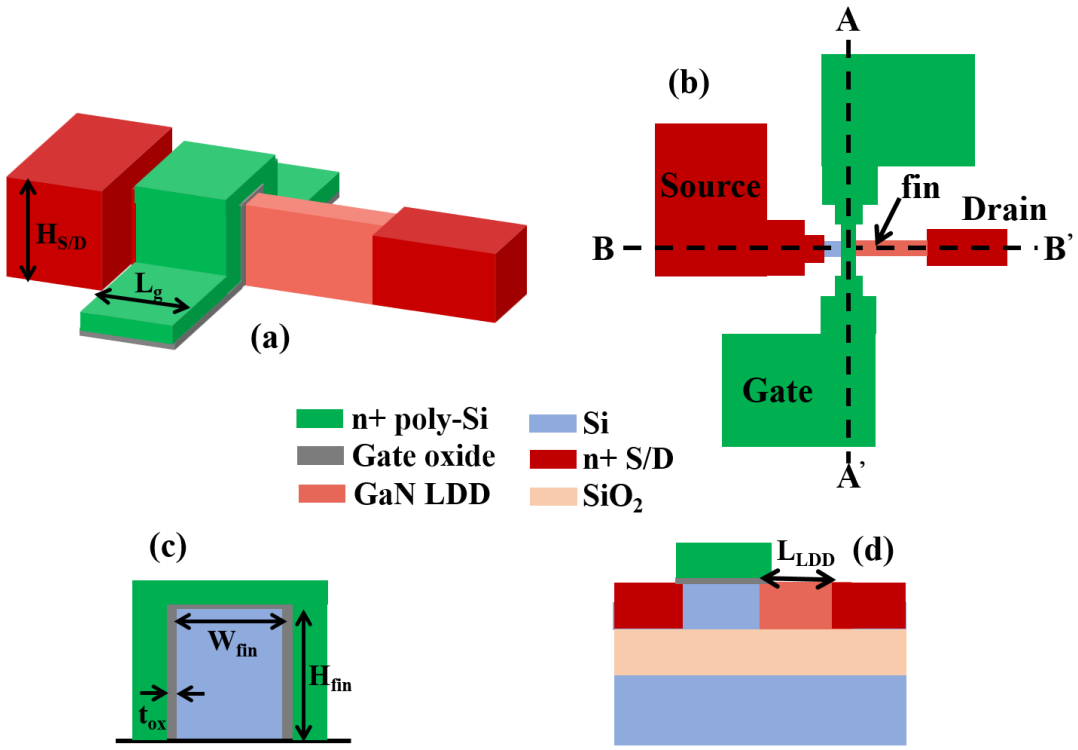


Fig 3.2 Schematic diagrams of heterogeneous 3D MISFET structure with GaAs/GaN drain: (a) overall 3D view; (b) top-view; (c) cross-section cut along fin-width direction; (d) cross-section cut along channel-length direction

3.3 Simulation Setup

Sentaurus 2012, Synopsys 3D device simulation tool is utilized to perform device architecture optimization studies of 3D multiple-gate MISFET in order to investigate the effect of bandgap engineering by incorporating wide bandgap GaAs/GaN drain into the structure. A fully-depleted thin body SOI *n*-channel 3D multiple-gate structure has been implemented in the device

simulation, and the structure and its parameters are explicitly shown in Fig. 3.3 and Table 3-1. These parameters are chosen to meet the criteria of the off-state leakage current of 5 pA/μm at V_{GS}=0 V/V_{DS}=1.1 V, and all other parameters are from ITRS. Most importantly, the given structure has considered the device design for the fabrication to realize selective-area MBE-grown *n*-GaN drain on SOI(100) substrate. Si seed layer required for the selective-area growth of *n*-GaN nanostubs is provided from the SOI Si substrate by etching through the BOX layer. This idea not only gives a better confinement of both threading and misfit dislocations but also gives an advantage of providing a heat sink for this high voltage/power transistor on the SOI platform. Throughout the simulation studies, physical gate length is fixed to 30 nm, and high-k thickness of 4.6 nm (EOT of 2 nm) is chosen considering the trade-off between the cutoff frequency and breakdown voltage. Here, Al_2O_3 dielectric reported in the literature [4] to have a superior interface quality on GaN materials is utilized. Fin aspect ratio of 3.5 is being utilized with various parameters of the RESURF structure such as lightly-doped drain (LDD) length and its doping concentration. This set of simulations assumed uniform doping profiles and abrupt junctions throughout all regions, and dopants are considered to be fully ionized. Moreover, ohmic contacts are assumed to rule out parasitic components, and a midgap metal workfunction of 4.7 eV is assumed.

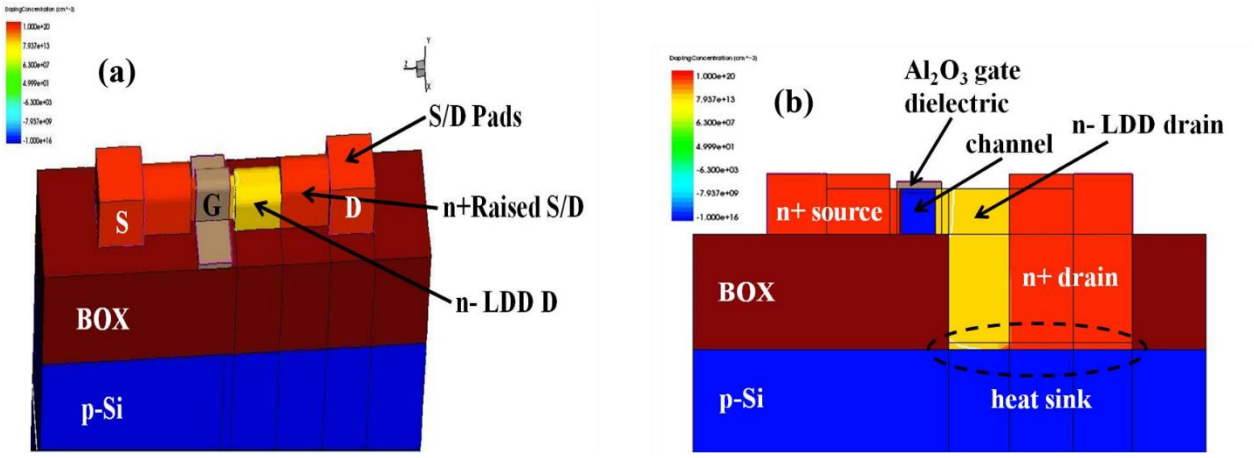


Fig 3.3 Schematic diagrams of simulated fully-depleted SOI *n*-channel tri-gate (a) overall structure and (b) cross-section cut along channel direction

Table 3-1 Device Parameters for 3D Multiple-Gate MISFET Structure with GaN Drain

L_{gate} (nm)	30
W_{fin} (nm)	8
H_{fin} (nm)	34
LDD overlap (nm)	0-13
LDD length (nm)	13-90
LDD doping concentration (cm^{-3})	$1x10^{17}$-$1x10^{19}$
t_{BOX} (nm)	80
$t_{insulator}$ (EOT) (nm)	3.23(1.4)/4.6(2)
Channel doping (cm^{-3})	$1x10^{16}$
Source doping (cm^{-3})	$1x10^{20}$
Drain doping (cm^{-3})	$7x10^{19}$
Fin pitch (nm)	90 (=$3L_g$)

Regarding the key simulation models, drift-diffusion transport model and Fermi-Dirac statistics model have been included in the simulation, along with Shockley-Read-Hall (SRH) recombination model. Several mobility models including Philips Unified, normal electric field dependence and high field dependence mobility are also considered in the simulation. Channel

mobility dependence on different fin orientation is excluded since this set of simulation study is focused on the off-state characteristics. Quantum effects, which have pronounced impact on the device behavior in the on-state, are ignored in this study. In particular, thermionic emission current physics model for capturing the transport across heterojunction interface is taken into account in the simulation. Moreover, band structure parameters such as bandgap, electron affinity (band alignment) and density-of-states effective masses in regard to GaN are fully considered in the set of simulations.

3.4 Optimization of Device Parameters

From the lateral electric field distributions shown in Figure 3.4, peak electric field is highest at the fin corner in the off-state (V_{GS}=0 V/V_{DS}=30 V) even with rounded fin corners and low channel doping. LDD overlap (i.e. gate-to-drain overlap length) is taken to be 4 nm, a reasonable value for a typical length of the drain extension into the channel underneath the gate, because different LDD overlap length made no difference in the field distribution along the channel. Decrease in the lateral E-field with increase in LDD length was observed, in agreement with the well-known high voltage RESURF concept. As can be seen, LDD length greater than 45 nm is necessary in this bias condition for proper field reduction along the channel, especially near the gate edge. Therefore, LDD length of 45 nm is chosen throughout the simulations. Band diagram as well as 2D depletion region and electric field distribution along the channel with LDD doping of $1x10^{17}$ cm^{-3} and 45 nm LDD length are illustrated in Figure 3.5. Due to a small electron affinity difference of 0.05 eV between Si and GaN materials, ΔE_C is negligible at the Si/GaN heterointerface. The fully depleted portion across the top LDD region is clearly observed in this condition. Furthermore, field crowding near the gate edge as well as high field concentration at

the body/BOX interface were observed. These two regions of high fields are the potential bottleneck of the overall breakdown characteristics of the proposed device.

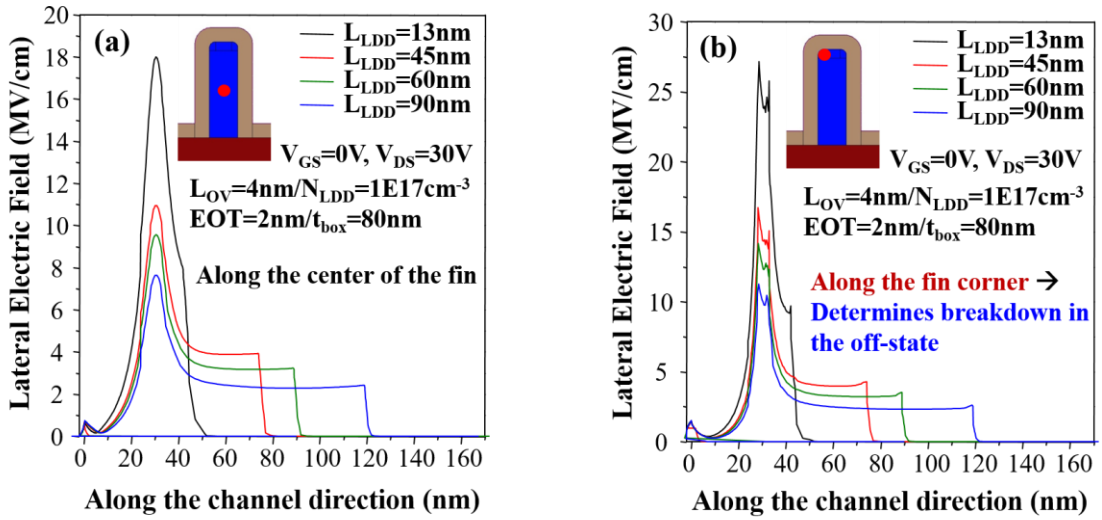


Fig 3.4 Lateral electric field distribution (a) along the center of the fin and (b) along the top fin corner of various *n*-GaN LDD length of 3D device structure

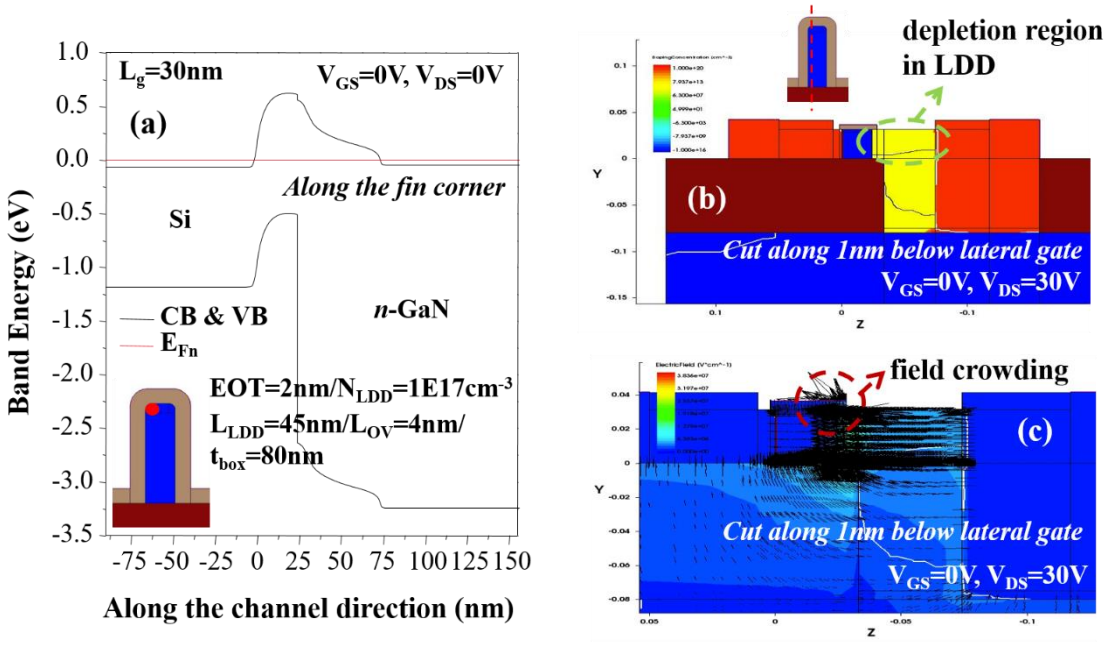


Fig 3.5 (a) Band diagram (b) 2D depletion region contour and (c) 2D E-field distribution along the channel for N_{LDD}=1x10^{17} cm^{-3}, L_{LDD}=45 nm, and L_{OV}=4 nm

Lateral electric field distribution along the channel with different EOT in the top fin corner region with their 2D field distribution is given in Figure 3.6. There is no change in lateral E-field distribution when EOT is varied in the off-state. However, drain field coupling through the BOX layer is reduced for EOT=1.4 nm compared to that of 2nm, shown in Figure 3.6(b) and (c). Moreover, different BOX thickness is known to result in different potential distribution inside the channel, and thus breakdown behavior can be greatly affected by the BOX thickness in conventional SOI devices. Intuitively, thicker BOX results in higher breakdown voltage. The lateral electric field distributions of the proposed device both cut at 1 nm below the top gate and channel/BOX interface showed no difference in their magnitudes with different BOX thickness (t_{box}) in the range between 40 nm and 160 nm, as given in Figure 3.7(a). However, an increase in the drain leakage current was observed as t_{box} was increased (Figure 3.7(b)). The little difference

comes from the thickness of embedded bottom LDD layer, where its thickness is determined by the BOX thickness fixed by the device design. The region at the corner of BOX/channel/LDD region interface is not fully depleted as the BOX thickness is increased at the same drain voltage. As can be seen in Figure 3.8, reduction in the lateral electric field with more uniform distribution was observed as LDD doping concentration is lowered. As a result, LDD doping needs to be lower than $1x10^{18}$ cm^{-3} for proper peak field reduction because non-uniform depletion region along the top LDD region can be observed in such high doping concentration.

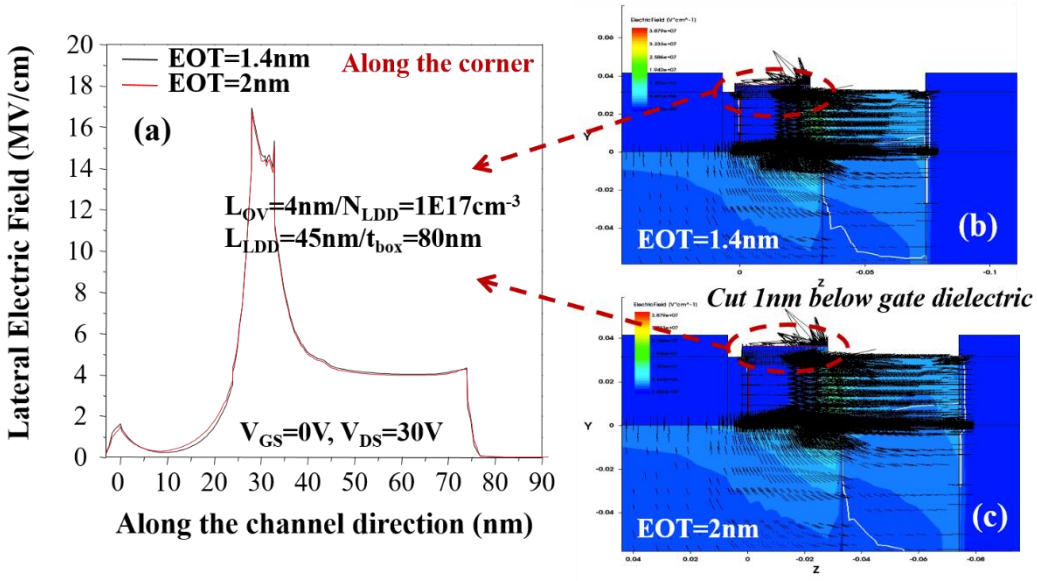


Fig 3.6 (a) Lateral electric field distribution along the channel in the fin corner; 2D E-field distribution of (b) EOT=1.4 nm and (c) EOT=2 nm cut 1 nm below the lateral gate dielectric

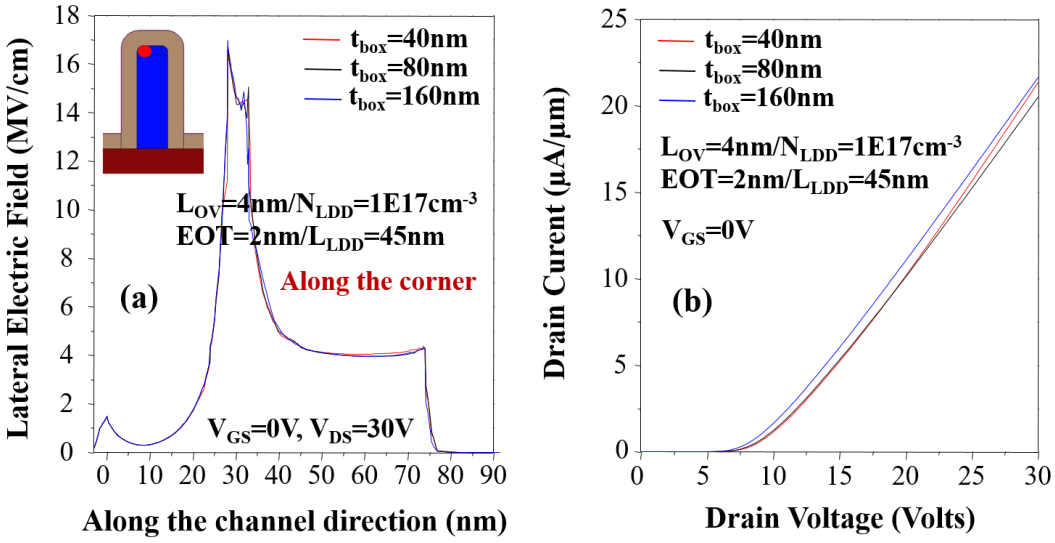


Fig 3.7 (a) Lateral electric field distribution along the top fin corner; (b) output characteristics in the off-state of heterogeneous GaN drain multiple-gate MISFET for different BOX thicknesses

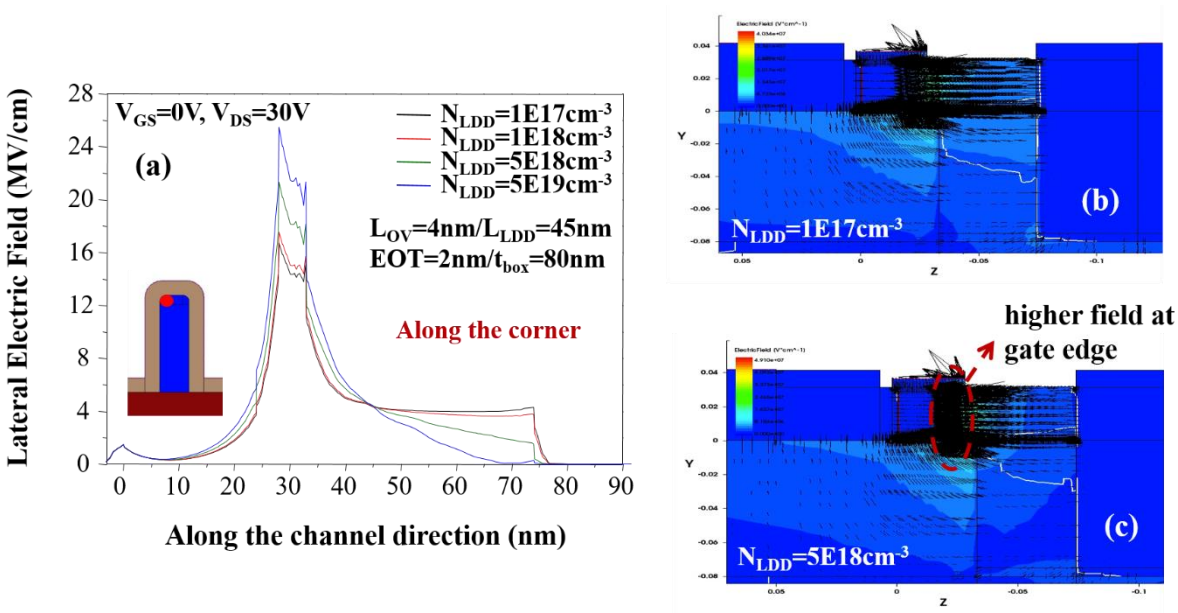


Fig 3.8 (a) Lateral electric field distribution along the channel in the top fin corner with different LDD doping concentrations; 2D E-field distribution of (b) N_{LDD}=1x10^{17} cm^{-3} and (c) N_{LDD}=5x10^{18} cm^{-3}

Breakdown voltage in the off-state is then quantitatively defined as the drain-to-source voltage when the drain current (I_{DS}) at V_{GS}=0 V reaches 1 µA/µm, which gives the surface lateral electric field of approximately 3 MV/cm (critical E-field of c-GaN, 3.2 MV/cm) for devices with EOT of 2 nm. The off-state breakdown voltages of heterogeneous GaN drain 3D multiple-gate MISFET with various device parameters are provided in Table. 3-2. Due to the need of reduction in high peak surface lateral electric field near the gate edge with RESURF structure, a field-plate near the gate edge on top of LDD region (i.e. extension of gate metal into the LDD region with thicker oxide than the gate dielectric for C_{gd} trade-off) has been applied to the device structure. This field-plate structure as well as the lateral electric field distribution along the channel cut along the fin corner with and without the field-plate are illustrated in Figure 3.9. As a result, peak field

position is shifted towards the LDD region, away from the gate edge. Moreover, peak field value is reduced considerably from that of the device structure without the field-plate. These results are schematically illustrated in Figure 3.10 with 2D lateral electric field distribution at the fin corner regions. For a field-plate equipped device with LDD length of 90 nm, LDD doping of $1x10^{17}$ cm^{-3}, EOT of 2 nm and BOX thickness of 80 nm resulted in the off-state breakdown voltage of 14 V, 40 % improvement from the structure without the field-plate.

Table 3-2 Off-State Breakdown Voltages Without Impact Ionization Model

Device Parameters		**Off-State Breakdown Voltage (V_{BD})**
LDD length (nm)	13	4.83
	45	7.18
	60	7.84
	90	9.84
LDD doping concentration (cm^{-3})	$1x10^{17}$	7.18V
	$1x10^{18}$	6.29V
	$1x10^{19}$	4.12V
EOT (nm)	1.4	10.86V
	2.0	7.18V
BOX thickness (nm)	40	7.36V
	80	7.18V
	160	6.69V

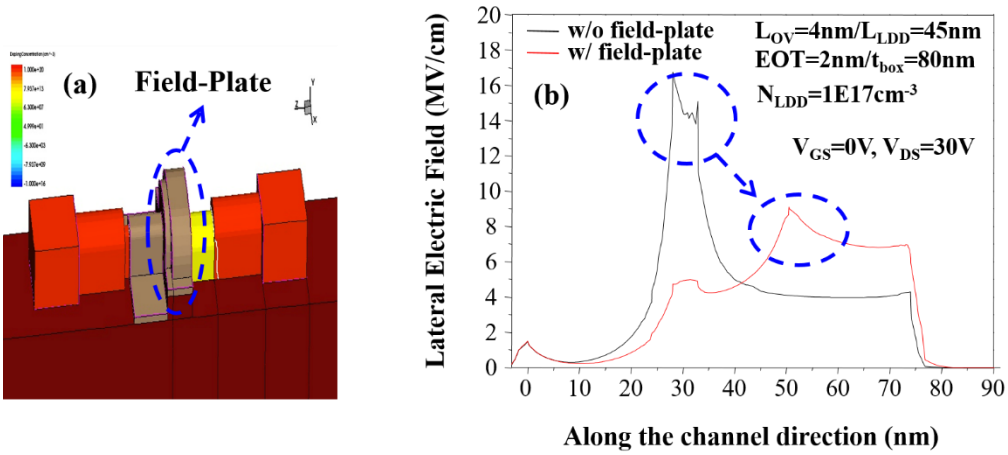


Fig. 3.9 (a) Heterogeneous wide bandgap GaN drain 3D multiple-gate MISFET with a field-plate; (b) lateral electric field distribution along the channel in the top fin corner with and without the field-plate

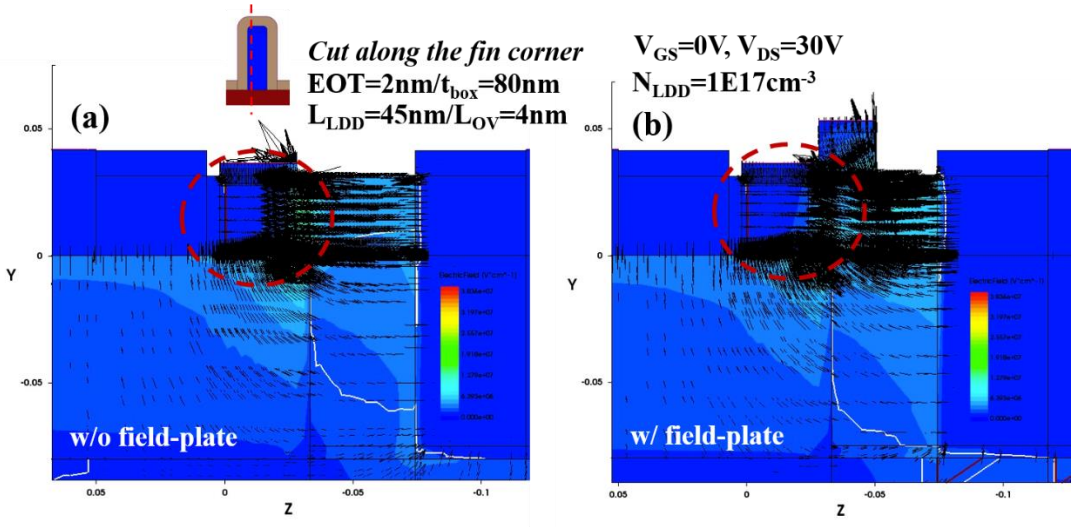


Fig 3.10 2D E-field distribution of heterogeneous wide bandgap GaN drain 3D multiple-gate MISFET (a) without and (b) with a field-plate

For complete physics analysis of off-state breakdown characteristics, impact ionization physics model has been included in the following set of simulations [5], [6]. This physics model takes into account the positive feedback process of Avalanche generation of carriers in the high field regions. This provides better understanding of the breakdown physics of the proposed device architecture. Comparisons are made between the device simulations with and without the impact ionization physics model in order to fully capture the breakdown mechanisms in the proposed device structure. Figure 3.11 and 3.12 show 1D/2D lateral electric field distributions as well as the 2D impact ionization rate along the channel direction. Highest impact ionization rate is observed near the gate edge at the BOX/channel interface (Figure 3.13). Moreover, inclusion of impact ionization physics model modifies both 1D/2D E-field distributions. Thus, it is more convincing to argue out the breakdown physics including this model into the simulation tool. From the breakdown voltage definition mentioned previously, 13 % reduction in the breakdown voltage after inclusion of the impact ionization model is clearly seen.

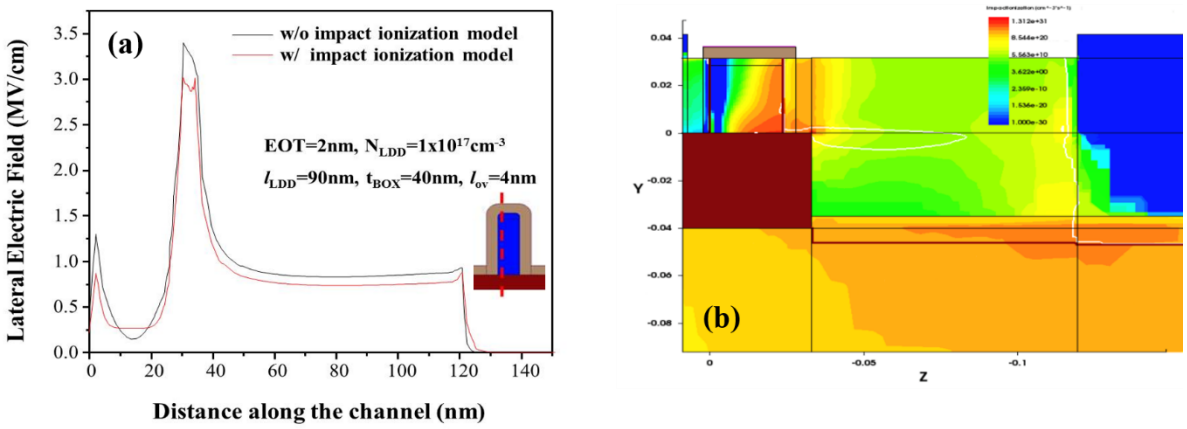


Fig 3.11 (a) Lateral electric field distribution along the channel of heterogeneous wide bandgap GaN drain 3D multiple-gate MISFET with and without impact ionization physics model; (b) 2D distribution of impact ionization rate (i.e. Avalanche generation rate) along the channel direction

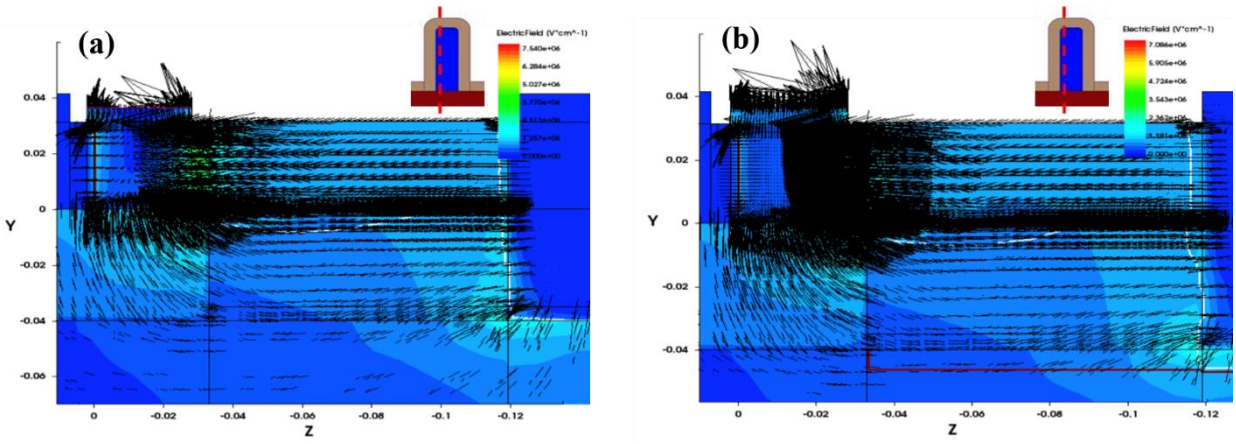


Fig 3.12 Schematic diagrams of 2D E-field distribution along the channel of heterogeneous wide bandgap GaN drain 3D multiple-gate MISFET (a) without and (b) with impact ionization physics model

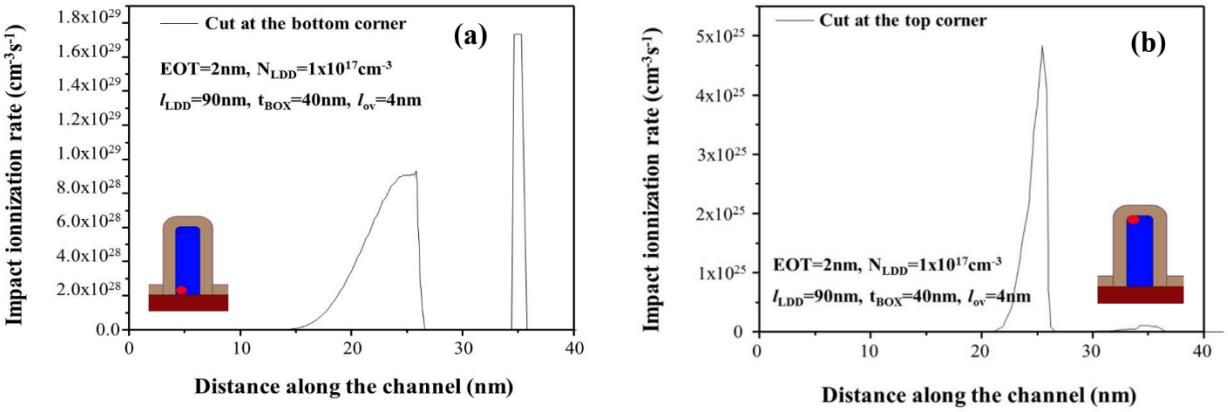
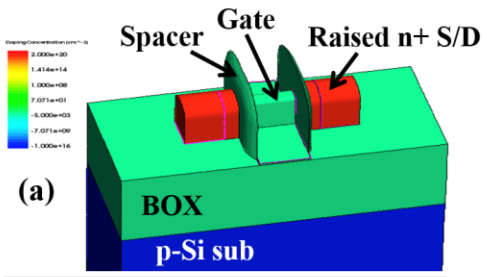


Fig 3.13 Impact ionization rates along the channel of heterogeneous wide bandgap GaN drain 3D multiple-gate MISFET cut (a) at the fin bottom corner (b) at the top fin corner

In order to fully capture the on-state device characteristics of the heterogeneous GaN drain 3D transistor, not only impact ionization physics model but also accurate transport physics based on the calibrated models is important to be considered. Moreover, quantization effect as well as mobility degradation due to a thin layer cannot be neglected in the transport physics in 3D multiple-

gate devices with very narrow fins. In this regard, transport parameters such as constant bulk mobility and saturation velocity in Sentaurus 2012, Synopsys 3D device simulation tool are carefully calibrated to the experimental results from Intel [7] with inclusion of density-gradient (DG) quantum-mechanical (QM) and thin layer mobility models. Due to the importance of non-parabolicity and anisotropy of Si channel under strong quantization effect, none of the QM models in Sentaurus is accurate to produce correct inversion layer density distribution, carrier velocity distribution and carrier effective mobility. Furthermore, given DG QM model has very little effect (i.e. less than 5 % change from classical model) on any transport characteristics such as surface carrier mobility, velocity and electric field distributions. Therefore, direct change in constant bulk mobility and saturation velocity with the inclusion of default DG QM model to fit to the experimental data can provide reasonable estimation of the proposed GaN drain 3D multiple-gate device performance including the effective gate capacitance reduction due to quantization to first-order. Device structure and parameters for the calibration are given in Figure 3.14(a). Accordingly, Figure 3.14(b) shows well-calibrated transfer characteristics. The rest of the device physics models included in this set of simulations are the same as the previous simulation setups. Electron density and its velocity distributions from the calibrated device are demonstrated in Figure 3.15. As can be seen, electron velocity in the channel far exceeds the saturation velocity of Si near the drain. Moreover, lateral electric field distribution along the channel becomes more uniform after calibration shown in Figure 3.16.



L_{gate} (nm)	30
Spacer thickness (nm)	5
$t_{insulator}$ (EOT) (nm)	0.9
t_{BOX} (nm)	80
Extension length (nm)	7
Extension doping (cm^{-3})	$2x10^{19}$
Channel doping (cm^{-3})	$1x10^{15}$
Substrate doping (cm^{-3})	$1x10^{16}$
S/D doping (cm^{-3})	$2x10^{20}$
Gate pitch (nm)	90
Fin pitch (nm)	90 (=$3L_{gate}$)

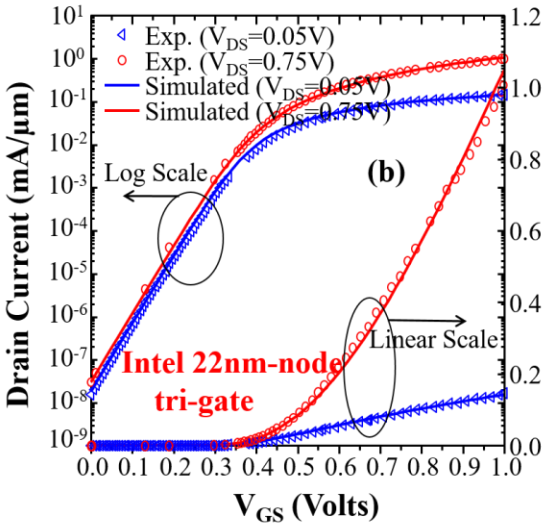


Fig 3.14 (a) Schematic diagram of fully-depleted SOI Si *n*-channel 3D multiple-gate structure (top) and device parameter setup for Si 3D multiple-gate MISFET used in calibration (bottom); (b) I_{DS}-V_{GS} curves of simulated Si 3D multiple-gate MISFET, calibrated to Intel's 22 nm-node tri-gate device with I_{DS} in log-scale (left axis) and I_{DS} in linear-scale (right axis)

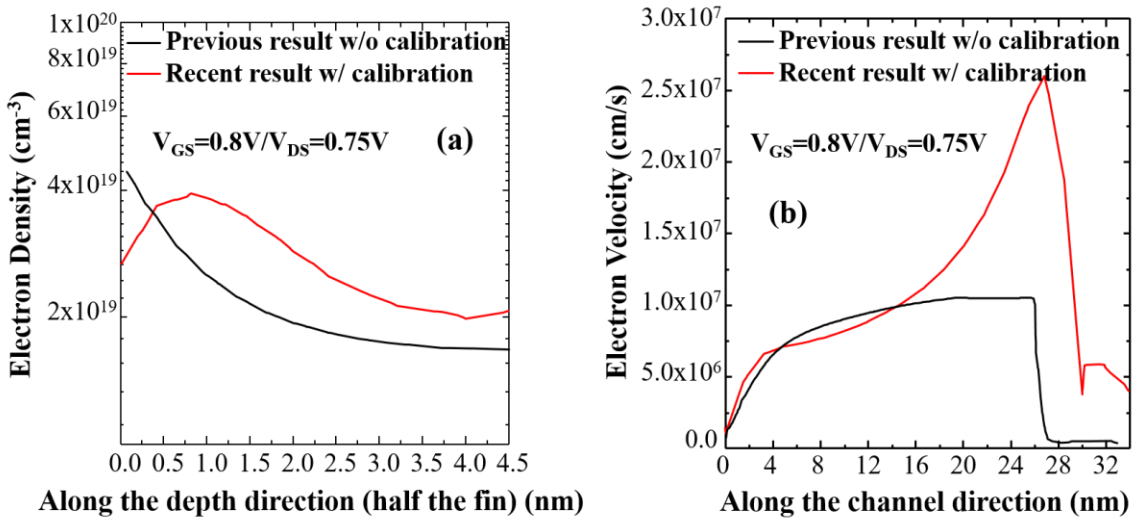


Fig 3.15 (a) Inversion layer electron density along the depth direction from the gate dielectric/channel interface, in the middle of the channel (b) electron velocity distribution along the channel direction, 0.5 nm below the gate dielectric/channel interface

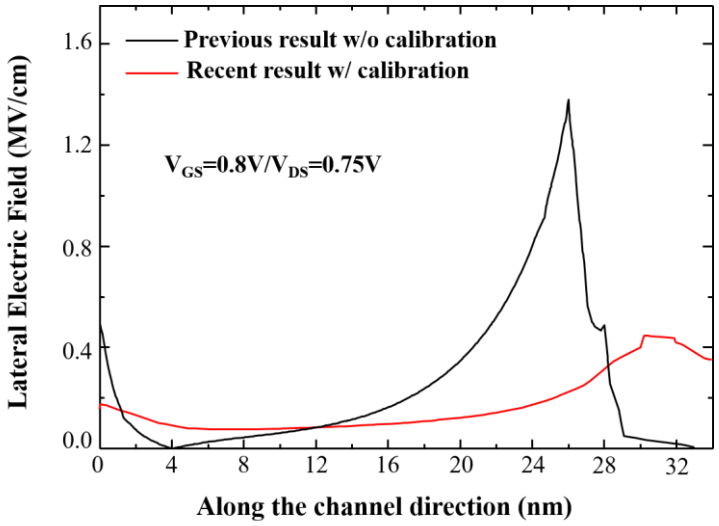


Fig 3.16 Lateral electric field distribution along the channel of fully-depleted SOI *n*-channel 3D transistor with and without calibration to experimental data

The above calibrated Si 3D multiple-gate structure is implemented into the GaN drain 3D MISFET. The simulated structure is illustrated in Figure 3.17(a). The device parameters in regard to GaN drain are the same as the previous simulation setup. Its change in lateral electric field distribution after calibration led to 2X reduction in its peak E-field near the gate/drain region at the top fin corner. The band diagram of the calibrated GaN drain 3D MISFET at V_{GS}=V_{DS}=0 V is plotted out in Figure 3.18(a). Its depletion region contour as well as 2D electric field distribution at the top fin corner is illustrated in Figure 3.18(b) and (c). Unlike the results of the device structure without calibration, lateral electric field as well as impact ionization rate is higher at the fin bottom corner than that of the top corner in the simulated device structure with calibration to experimental data, given in Figure 3.19. The overall off-state breakdown voltages of heterogeneous GaN drain 3D multiple-gate MISFET with various device parameters are shown in Table 3-3. Finally, linear transfer characteristics and output characteristics of the proposed device structure are demonstrated in Figure 3.20(a) and (b), respectively. LDD length of 45 nm, LDD doping concentration of $1x10^{17}$ cm^{-3}, gate/drain overlap distance of 4 nm, EOT of 2 nm and BOX thickness of 80 nm were chosen in this set of simulations. Physical gate length was fixed at 34 nm and its threshold voltage extracted at V_{DS}=0.05 V is 0.347 V in this case. Maximum transconductance of 900 µS/µm was obtained with subthreshold swing of 147 mV/dec and DIBL of 44 mV/V at a constant current of 10 µA/µm. Furthermore, R_{on} of 2 Ω-mm was obtained at V_{GS}=1 V.

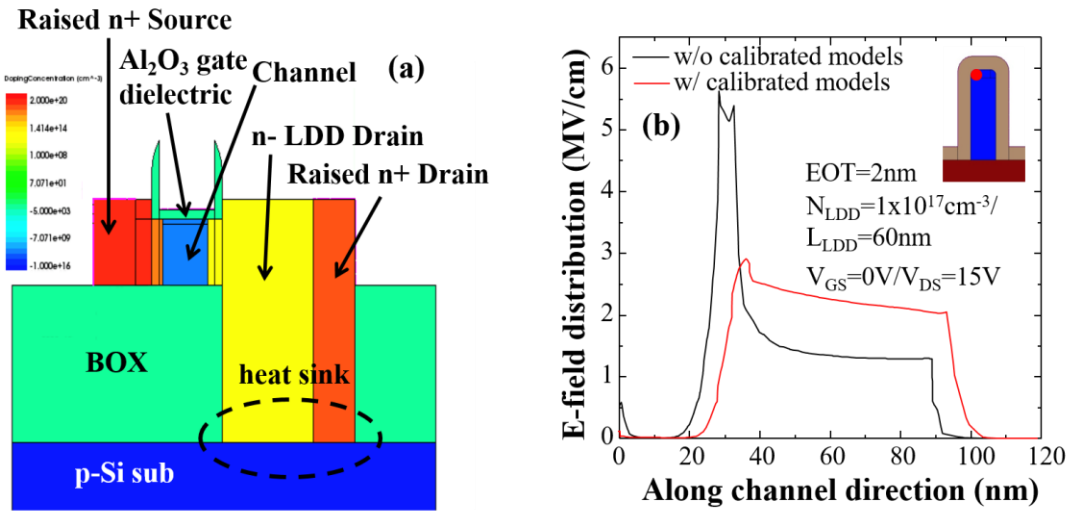


Fig 3.17 (a) Schematic diagram of heterogeneous GaN drain 3D multiple-gate MISFET structure utilizing the calibrated Si 3D transistor architecture including quantum mechanical physics model and thin layer mobility degradation effect; (b) lateral electric field distribution with and without calibration to experimental results

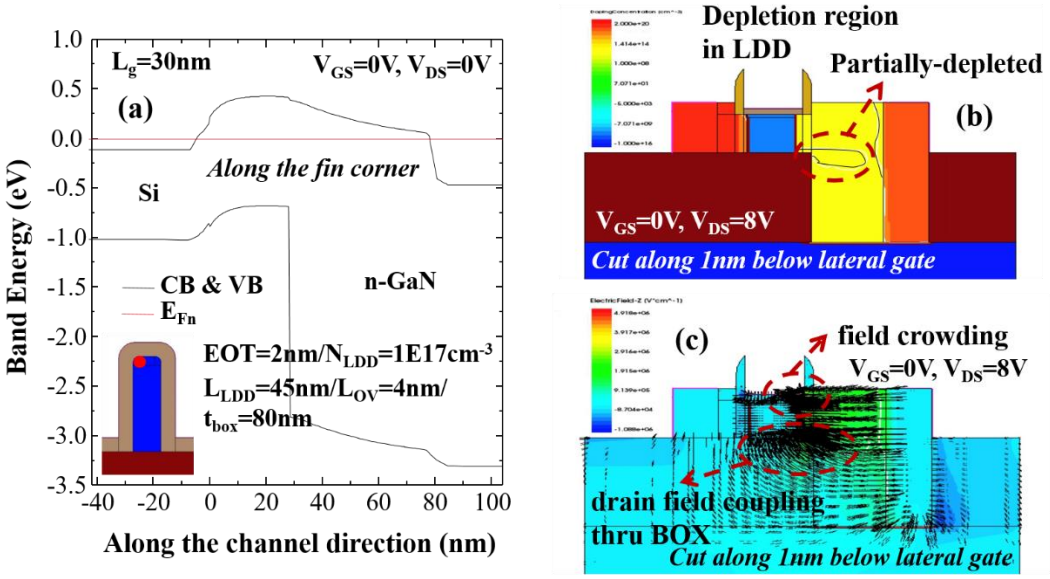


Fig 3.18 (a) Band diagram of heterogeneous GaN drain 3D multiple-gate MISFET structure cut along the top fin corner; (b) cross-section of the device showing the 2D depletion region at the top fin corner; (c) 2D electric field distribution at the top fin corner

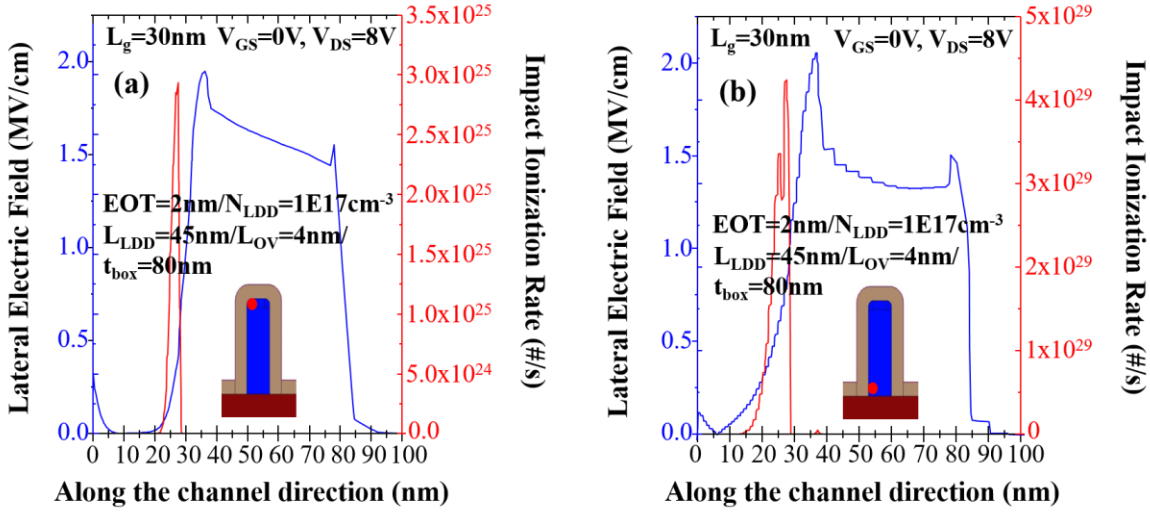


Fig 3.19 Lateral electric field and impact ionization rate distributions of heterogeneous GaN drain 3D multiple-gate MISFET cut along (a) top fin corner and (b) fin bottom corner

Table 3-3 Off-State Breakdown Voltages With Impact Ionization Model

Device Parameters		Off-State Breakdown Voltage (V_{BD})
LDD length (nm)	30	5.98V
	45	7.34V
	60	8.31V
	90	9.95V
	130	13.03V
	180	14.85V
LDD doping concentration (cm^{-3})	$1x10^{17}$	7.34V
	$1x10^{18}$	6.92V
	$1x10^{19}$	3.71V
BOX thickness (nm)	40	7.88V
	80	7.34V
	160	6.65V

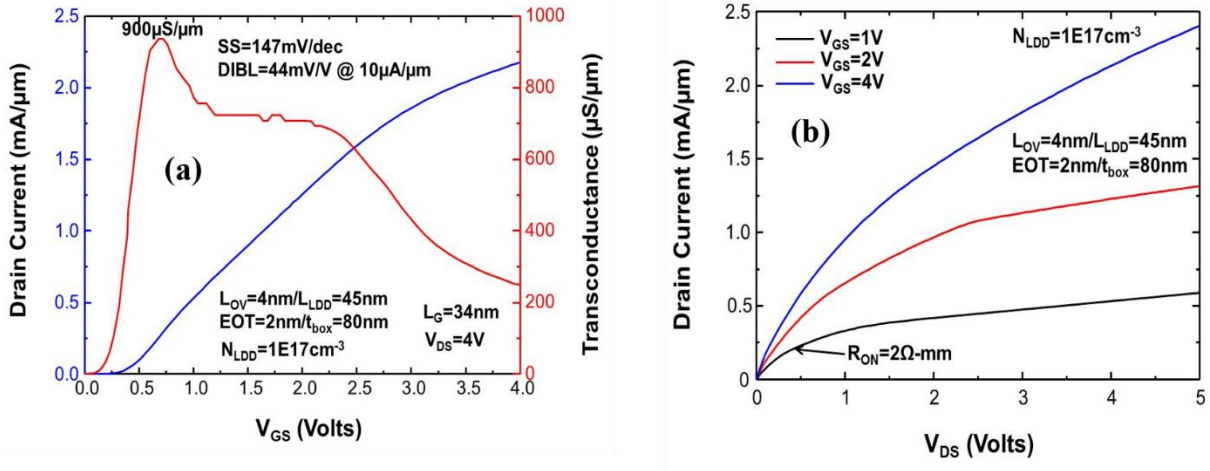


Fig 3.20 (a) Transfer characteristics and (b) output characteristics of the simulated heterogeneous GaN drain 3D multiple-gate MISFET structure

3.5 Summary

Theoretical analysis/simulation studies of the impact of various device parameters on electric field distributions and breakdown characteristics of heterogeneous 3D multiple-gate device architecture based on drain engineering have been performed, utilizing wide bandgap GaN as a drain. Inclusion of appropriate impact ionization physics model as well as well-calibrated carrier transport and mobility models resulted in a 2X reduction in the peak lateral electric field near the gate/drain region, compared to that of the device without calibration. Breakdown characteristics and transport physics were studied in detail to fully understand the physics of heterogeneous GaN drain 3D multiple-gate MISFET structure for optimization of the device in high voltage/power RF SoC applications. The simulated results show that the proposed heterogeneous GaN drain 3D multiple-gate MISFET structure can deliver f_T around 100 GHz with 5X higher breakdown voltage compared with its Si counterpart.

3.6 Bibliography

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CHAPTER 4

Selective-Area MBE Growth of GaAs/GaN Nanostubs

4.1 Introduction

In order to realize heterogeneous integration of III-V wide bandgap semiconductor materials such as GaN with Si CMOS platforms as discussed in the previous chapters, high quality heteroepitaxy of these materials on Si(001) substrates with uniform size, spatial distribution, and doping profiles is necessary. However, significant mismatch exists between the lattices constants and thermal expansion coefficients of Si and GaN. These differences mean that heteroepitaxial growth of GaN on Si typically contains high defect densities, compromising any performance gain. Among various defect reduction schemes, selective-area epitaxy is known to effectively minimize defects in the heteroepitaxial films grown on substrates restricted to sub-micron area which is comparable to the size of transistors with sub-micron physical gate length. This is because strain and defects in the films are restricted in lateral dimensions, and surface energy is further minimized due to confined-geometry. Moreover, it is reported that GaN films directly grown on Si(001) substrates contain a mixture of two phases, wurtzite and zinc-blende, expected to result in further

degradation in device performance. In this regard, GaAs was chosen as a buffer layer for heteroepitaxy of GaN on Si in order to obtain zinc-blende GaN nanostubs. In this chapter, therefore, selective-area molecular beam epitaxy (MBE) of heavily *n*-doped GaAs/GaN nanostubs on Si(001) substrates covered with a nanopatterned SiO_2-mask is demonstrated utilizing aspect-ratio-trapping (ART) technique. The ART method to reduce defects in the heteroepitaxial films is discussed in detail in the next section. In addition, the influence of various MBE parameters including substrate temperature and growth rate on the selective-area epitaxy was investigated, and careful optimization of these growth parameters was performed. Initial nucleation stages of GaAs/GaN nanostubs were specifically studied to understand the origin of defects generated in these nanostubs. Furthermore, the optimal condition where MBE system resulted in complete selective-area growth of GaAs/GaN nanostubs over the SiO_2-mask is explained. This targeted condition was based on the requirement of selective-area epitaxy (SAE): (1) slow growth rate (2) high growth temperature (3) low arrival rate of group-III adatoms. These overall results of MBE film growth and characterization are given throughout this chapter.

4.2 Background

Two main challenges in integrating wide bandgap III-V materials such as GaN with mainstream Si technology arise from mixed zinc-blende-wurtzite GaN phases and high defect density in the grown films. Among the two different phases in GaN, extensive effort had been given to the growth of large-area zinc-blende GaN film on Si(001) substrate due to its interesting properties such as higher doping efficiency and higher bulk mobility compared to the wurtzite GaN film. Unlike wurtzite GaN, polarization-free crystal structure of zinc-blende GaN makes this phase suitable for high quality heavily *n*-doped wide bandgap drain. However, direct growth of

GaN on Si(001) substrate has a possibility of resulting in the mixture of two different phases (i.e. both zinc-blende and wurtzite in the grown film [1], [2] and/or amorphous SiN_x insulating layer formed at the interface [3], which can possibly degrade the overall transistor performance. Based on the experimental results from literatures, it is, thus, inevitable to utilize a very thin buffer layer [4] and/or stable 2x1 reconstructed As-As dimer surface of a patterned bare Si(001) via As_2 flood exposure prior to GaN growth [5] to control the initial stages of its growth to have a single phase, preferably cubic GaN without amorphous film at the interface.

Moreover, numerous approaches to reduce defect density in obtaining high quality III-V films on Si have been demonstrated, including compositional graded buffers [6]-[21], single strained interlayer [22], strained layer superlattices [23]-[27], thermal annealing such as rapid thermal annealing and thermal cyclic annealing [28]-[34], migration-enhanced epitaxy [35]-[37], and two-step growth [38]-[43]. Despite reducing defect densities, these methods are often complex and time-consuming, while thick buffers are unsuitable for Si CMOS integration. Furthermore, many of these approaches involve Si(111) and/or miscut Si(001) substrates, whereas growth on Si(001) is required for CMOS compatibility.

Besides the above-mentioned methods, selective-area growth (SAG) is an alternative approach to minimize defects and to eliminate the need for a thick buffer, mitigating thermal stress and cracking. Most previous reports of III-V materials growth on Si using SAG focused on metalorganic chemical vapor deposition (MOCVD) and chemical beam epitaxy [44]-[47]. These growth techniques use precursor molecules to deliver the III-V species to the sample surface. The fact that pyrolization and reaction rates of the precursors is higher on the Si surface than the SiO_2 mask results in high growth selectivity. An example is template-assisted selective epitaxy, where

MOCVD is used to grow III-V/Si(001) nanowires [48]. However, much research into MOCVD-SAG has focused on trenches where defects still propagate along the channel [49]-[62]. In contrast, molecular beam epitaxy (MBE) is a physical, rather than chemical deposition process in which the III-V species are delivered directly to the surface as pure elemental atoms or dimers. Unless growth conditions are chosen with extreme care, the III-V species are just as likely to stick to the SiO_2 mask as to the exposed Si surface. As a result, obtaining complete selectivity in MBE-based SAG is quite challenging. Despite this difficulty, the advantages of MBE (monolayer thickness control, abrupt doping profiles, and ultrahigh purity growth) mean that successful SAE growth of III-V materials on Si by MBE is of great interest. Because of lower surface/interface energies as well as elimination of antiphase boundaries (APBs), MBE-based SAG research has often focused on Si(111) substrates [63]-[75]. However, integration of III-V materials on Si(001) substrates is necessary due to its importance in semiconductor industry. Furthermore, SAE research on Si(001) substrates using MBE has typically been limited to meso-dimensions in the micron range [76]-[80]. Studies using MBE to achieve SAE of III-V films such as GaAs and cubic GaN in Si regions with nano-dimensions are still lacking, especially those that consider in detail the material quality and its applicability to device applications.

4.3 Aspect-Ratio Trapping (ART)

Aspect-ratio trapping (ART) is a defect reduction technique that has been widely implemented in heteroepitaxy of various III-V materials on Si substrates. This technique provides defect-free heteroepitaxial films above a dislocation-trapping region selectively grown inside dielectric-patterned high aspect-ratio trenches of arbitrary length, by inhibiting the propagation of dislocations generated from the heterointerface. That is, the dislocations terminate at the dielectric

sidewalls. Growth of various IV/III-V materials such as Ge [49]-[55], GaAs/InGaAs [56]-[60], InP [61] and GaN [62] has been extensively studied utilizing the ART technique. These results confirmed its effectiveness in reducing defects. Simple illustration of the technique is given in Figure 4.1. For cubic crystallographic material systems, threading dislocations and/or stacking faults are generated at the heterointerface in [110] directions on {111} planes. This geometry of defects makes a 54.7 $^{\circ}$ angle to the underlying Si substrates, and therefore, heteroepitaxy in trenches with aspect ratio greater than 1.4 on a dielectric-patterned Si substrate can effectively trap dislocations propagating to the top surface.

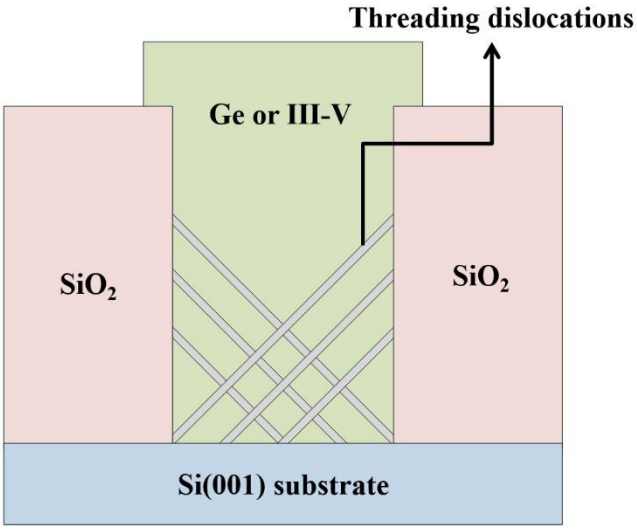


Fig. 4.1 Cross-sectional schematic diagram of ART mechanism in heteroepitaxial films

A remarkable advantage of the ART technique is that it uses a few hundred nanometers thick layer to eliminate defects such as threading dislocations. Even thinner films can be obtained by reducing the width of trenches since the aspect ratio greater than 1.4 can be easily achieved with narrower trench widths. This will, in fact, minimize thermal mismatch and cracking issue between the grown film and substrate. Moreover, since defects have very high energy in small

volumes, nanoscale lithography helps further minimize defect density in the grown films. Owing to its capability in significant reduction of defect density in heteroepitaxial films, selective-area MBE GaN growth with a thin GaAs buffer layer utilizing the ART is chosen in this work to realize junction-level heterogeneous integration of GaN onto mainstream Si technology. This is expected to make further performance improvements in high performance RF/mm-wave high voltage/power device applications.

4.4 Substrate Nano-patterning on Bulk Si(001) Substrate

In order to realize the proposed structure including a small-area (<0.1 μm^2) GaN drain, substrate nano-patterning technique on a bulk Si(001) substrate using e-beam lithography and reactive ion etching (RIE) has been developed, in agreement with aspect-ratio trapping (ART) discussed in the previous section. This technique prevents random positioning and size variation of GaN nanostubs, and thus allows good controllability and reproducibility for the subsequent selective-area MBE growth. The SiO_2-patterned Si substrates with both square and hexagonal arrays of circular/square holes are illustrated in Figure 4.2. Hole diameters and hole-to-hole distances are in the range of 40–300 nm and 100–2000 nm, respectively. Each pattern covered an area of 10000 μm^2. Since nucleation and initial growth are of great interest, the nanoholes with an aspect ratio of 1.2 were designed to simplify the microscopy. Although complete selective-area epitaxy (SAE) of GaN in MBE system has been achieved mostly with SiN_x and Ti mask materials [82], [83] to date, SiO_2 has been chosen as a mask material for MBE-based GaN SAE studies due to the successful demonstration of GaAs SAE utilizing SiO_2 mask rather than SiN_x and Ti masks.

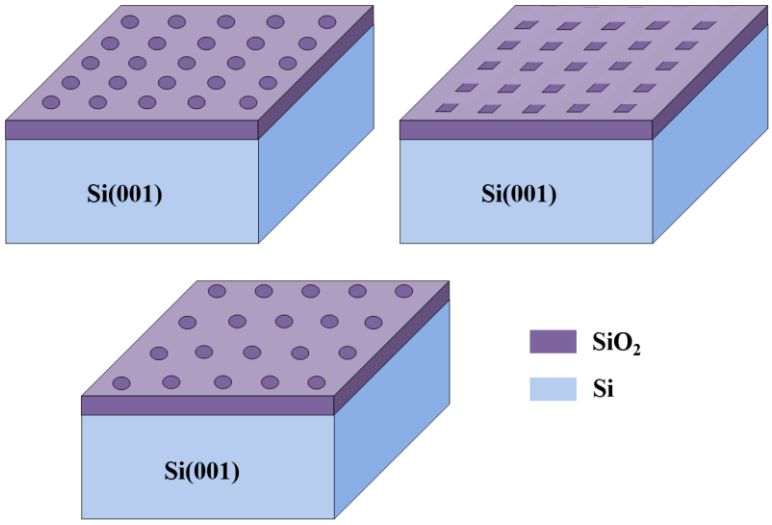


Fig. 4.2 Schematics of SiO_2-patterned bulk Si(001) substrates by e-beam lithography

3" p-type bulk Si(001) substrates of 1–50 Ω–cm resistivity were prepared with standard cleaning processes to remove organics and native oxide. These wafers were then loaded into an oxidation furnace to form atomically-flat 60nm-thick SiO_2 growth masks. Designed hole patterns with different sizes and hole-to-hole distances were transferred from ZEP520A positive resist to the SiO_2 growth masks using e-beam lithography and subsequent RIE etching. The detailed outline of the experimental procedures and its schematics are given in Table 4-1 and Figure 4.3, respectively. These e-beam nano-patterned hole arrays of different dimensions were characterized using scanning electron microscopy (SEM), and the plan-view images of various hole-to-hole distances with 50nm diameter hole arrays are shown in Figure 4.4. Well-ordered holes with less than 10% variation in their diameters across the whole array are observed.

Table 4-1 Process Flow of the SiO_2-mask Nanopatterning

Step	Process	Conditions/Comments
1	Oxide mask growth	Dry oxidation @ 1050°C, 13min
2	Nanopattern mask	E-beam lithography
3	Oxide mask etch	RIE etch (CF_4/CHF_3)
4	Nanopattern mask removal	ZEP520A strip

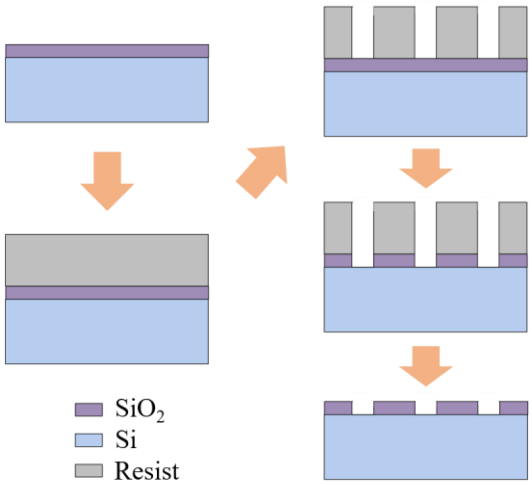
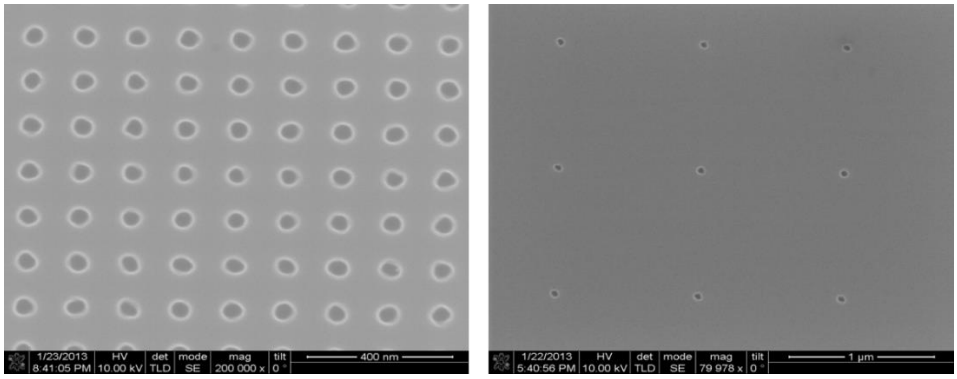


Fig. 4.3 Schematic process flow for e-beam nanopatterning on bulk Si(001) substrate



(a) **(b)**

Fig 4.4 Plan-view SEM images of SiO_2-patterned hole arrays of 50 nm in diameter with a hole-to-hole distance of (a) 100 nm and (b) 1 μm, after SiO_2 dry etching and removal of positive-tone e-beam resist

4.5 MBE Film Growth

4.5.1 Selective-Area *n*-GaAs Buffer Growth

To successfully demonstrate complete selective-area growth of *n*-GaAs buffer layer over mask material, SiO_2, MBE-based SAG requires that: (1) migration length on the SiO_2 mask must be sufficiently large for Ga adatoms to reach the nearest hole (Figure 4.5 (left)); (2) Ga adatom sticking coefficient must be lower on the SiO_2 mask than Si (Figure 4.5 (right)).

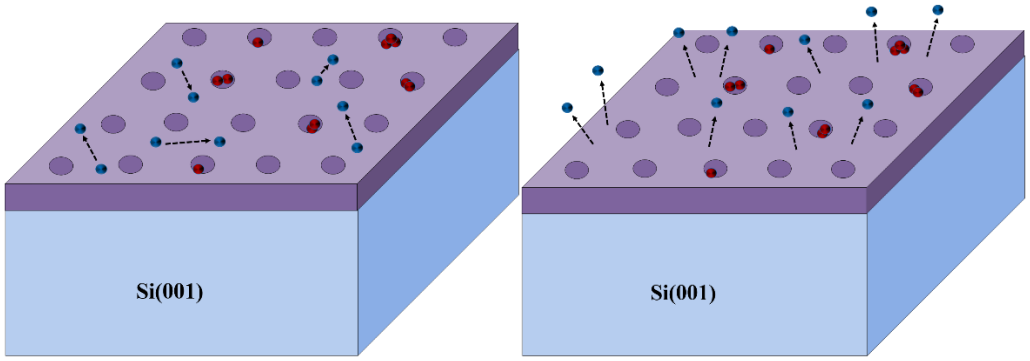


Fig. 4.5 Schematic diagrams of MBE-based SAG mechanisms; blue dots represent Ga adatoms migrating on the SiO_2 mask and getting desorbed from it; red dots symbolize Ga adatoms on the Si surface inside nanoholes

One challenge in growing *n*-GaAs buffer is how to effectively control the film crystallinity. Poly-crystalline *n*-GaAs can be easily grown for SAE compared to blanket growth. This is because native oxide removal inside nano-dimension holes by heating up the substrate to a very high temperature cannot be adequately monitored by in-situ RHEED patterns, and thus, this high temperature step cannot guarantee complete removal of oxide inside the holes. Moreover, low growth temperature is generally favored for GaAs growth with smooth and flat surface since nucleation becomes dominant over surface transport as the temperature decreases, which results

in smaller and denser islands [84]. However, in this case, selectivity will be lowered as well as crystal quality. Since GaAs grown at low temperature is far from equilibrium, the film tends to be poly-crystalline. The poly-crystalline GaAs has top facets in random directions. This can make the subsequent *n*-GaN growth challenging because GaN can easily nucleate on each facet, and if the growth time is not slow enough, those nucleation sites may not coalesce into a bigger one. Therefore, difficulty exists in controlling uniform size of *n*-GaN nanostubs.

Optimization studies with a set of metric for MBE growth parameters: substrate temperature (T_{SUB}), V/III beam-equivalent pressure (BEP) ratio and growth rate were performed. The most important strategy is to alter the sticking coefficients of the SiO_2 mask material as well as Si and the Ga adatom migration lengths on these two different materials. SiO_2-nanopatterned Si(001) substrates were undergone standard cleaning processes prior to loading into the III-As/Sb MBE chamber. These substrates were then heated up to 900 ℃ for a few minutes *in vacuo* to completely remove any residual native oxide formed during substrate transfer/loading. This outgassing step was later found to be the most critical step in achieving complete SAG. The SAG was initiated by the periodic repetition of cycles in which a short deposition of *n*-GaAs was followed by a growth interruption under As_2. This migration-enhanced approach gives Ga adatoms on the SiO_2 mask enough time to migrate into the nanoholes and form a smooth GaAs film on the exposed Si(001) surface. It also allows Ga adatoms that do not reach the holes to effectively desorb from the SiO_2 mask so that complete selectivity as well as a better growth rate controllability is realized with a higher chance of coalescence.

Figure 4.6 shows the optimization study results in detail for complete selectivity with 100 % coverage of *n*-GaAs nanostubs on Si(001) substrates. Planar GaAs growth rates were calibrated with reflection high energy electron diffraction for accurate measurement of Ga flux and V/III

BEP ratio. First, *n*-GaAs/Si nanostubs were grown at different substrate temperature (T_{SUB}) range between 570 and 630 ℃. These substrate temperatures were calibrated using both thermocouple and pyrometer. During this T_{SUB} variation study, V/III BEP ratio was 15 and *n*-GaAs growth rate was ~120 nm/h. At T_{SUB}=570 ℃, there was no growth selectivity: GaAs grows both on the mask and in the nanoholes (Figure 4.6(a)). At this substrate temperature, the Ga sticking coefficient on the SiO_2 mask is too similar to that on the exposed Si. Moreover, the migration length of Ga adatoms on the SiO_2 is shorter than the hole-to-hole distance. Due to the growth on the amorphous SiO_2 mask material, highly defective, polycrystalline *n*-GaAs nanostubs were grown. Increasing T_{SUB} to 590 ℃ (Figure 4.6(b)), complete selective-area single-crystalline *n*-GaAs nanostubs were obtained with four top facets, consistent with (001)-oriented zinc-blende GaAs. Nanostub growth in 100 % of nanoholes with no parasitic growth on the mask was observed. The final height of the *n*-GaAs nanostubs was measured from atomic force microscope (AFM) to be 120 nm. At T_{SUB}=630 ℃ (Figure 4.6(c)), only 2 % of nanoholes contained *n*-GaAs nanostubs. Increased Ga adatom desorption from the SiO_2 mask at higher T_{SUB} means these adatoms have very short amount of time within which the Ga can migrate to the nearest nanohole and form bonds with As [85], [86]. In addition, the V/III BEP ratio of 15 did not supply sufficient As for Ga adatoms to form stoichiometric GaAs nanostubs. This experimental series confirms that under these growth conditions, GaAs SAE is extremely sensitive to substrate temperature. The successful SAE of *n*-GaAs nanostubs on Si(001) occurs only within a relatively small temperature window around 590 ℃.

As a result, 590 ℃ was chosen as the optimized substrate temperature to examine the effect of other growth parameters such as V/III BEP ratio and GaAs growth rate on the *n*-GaAs SAG. A lower growth rate is preferable since the migration length of Ga adatoms increases. However, with

the Ga BEP reduced to $5x10^{-8}$ Torr (Figure 4.6(d)) at a V/III ratio of 15, less than 3 % filling of nanoholes was observed. This phenomenon implies that the migration length of Ga adatoms is too long with this growth rate at the given substrate temperature, and thus, Ga adatoms get desorbed before they form GaAs. Furthermore, this means not enough Ga flux impinging onto the surface of the SiO_2 mask, and therefore, the number of these Ga adatoms is insufficient to get incorporated into the nanoholes. On the other hand, lowering the V/III BEP ratio from 15 to 10 (Figure 4.6(e)) with a growth rate of ~120 nm/h resulted in 83 % filling of nanoholes. When there is not enough As, Ga adatoms have less chance to incorporate with As inside the holes. As a consequence, the crystal quality of *n*-GaAs nanostubs was much worse than those grown with higher V/III ratio. Therefore, Ga BEP and V/III ratio were chosen to be $1x10^{-7}$ Torr and 15, respectively at the substrate temperature of 590 ℃ for the SAE of *n*-GaAs nanostubs. Feasibility of the optimized growth conditions was verified through repeatable growth experiments over time.

Having made some initial optimization of the growth parameters, the growth deposition time was varied in order to investigate the initial nucleation stages of the *n*-GaAs nanostubs to aggressively scale the height of these nanostubs. In this set of experiments, the growth conditions were as follows: substrate temperature=590 ℃, V/III=15, GaAs growth rate=120 nm/hr. After 10 minutes of deposition time, *n*-GaAs island nucleation starting from the edges of the patterned nanoholes via the Volmer-Weber (VW) growth mode (Figure 4.6(g)) was observed. As growth proceeded, these GaAs islands increased in size both vertically and laterally by their coalescence. After 20 minutes of growth, they formed uniform single-crystalline *n*-GaAs nanostubs with clear top and sidewall facets (Figure 4.6(h)). These facets demonstrate the efficacy of SAE where additional sidewalls help minimize the surface energy by strain relaxation in the GaAs nanostubs. These facets were formed during the early stage of the growth shown in Figure 4.6, which make

the subsequent nanostub growth nearly strain-free. Further increase in the deposition time resulted in full filling of the nanoholes with complete selectivity as shown in Figure 4.6(f). Moreover, the morphology and coverage of the *n*-GaAs nanostubs was independent of nanohole diameter and hole-to-hole distance over the ranges in this study (50−200 nm and 100−1000 nm, respectively). Smooth morphology with a precise control of the nanostub height of 30nm was obtained via migration-enhanced approach shown in Figure 4.7.

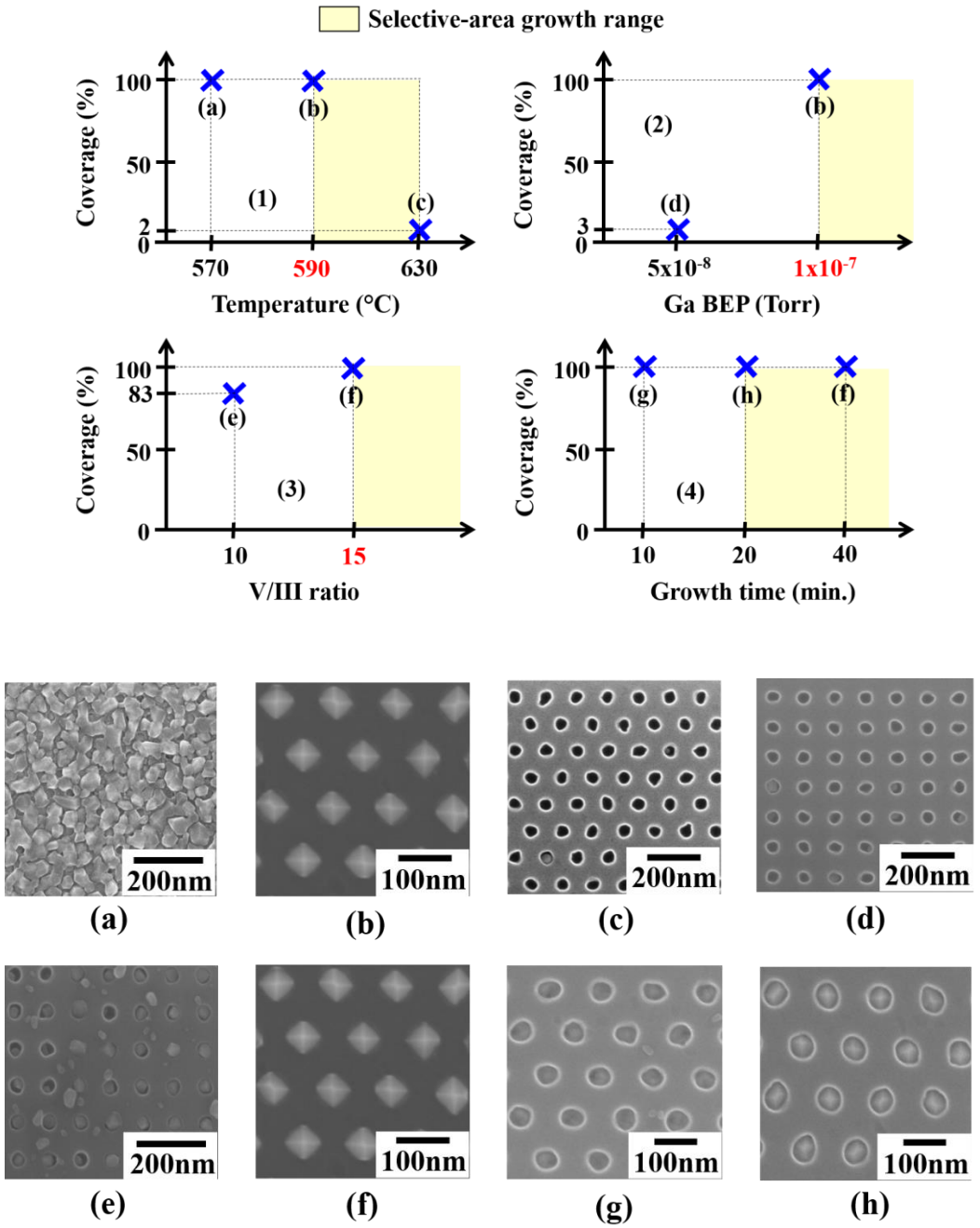


Fig. 4.6 MBE growth optimization windows with its parameters for *n*-GaAs buffer on Si(001) substrates (top) and their plan-view SEM images (bottom); (1) growth temperature; (2) Ga beam-equivalent pressure (BEP) (i.e. Ga BEP of $5x10^{-8}$ and $1x10^{-7}$ Torr are equivalent to GaAs growth rate of 70 and 120 nm/hr, respectively.); (3) V/III BEP ratio; (4) growth time

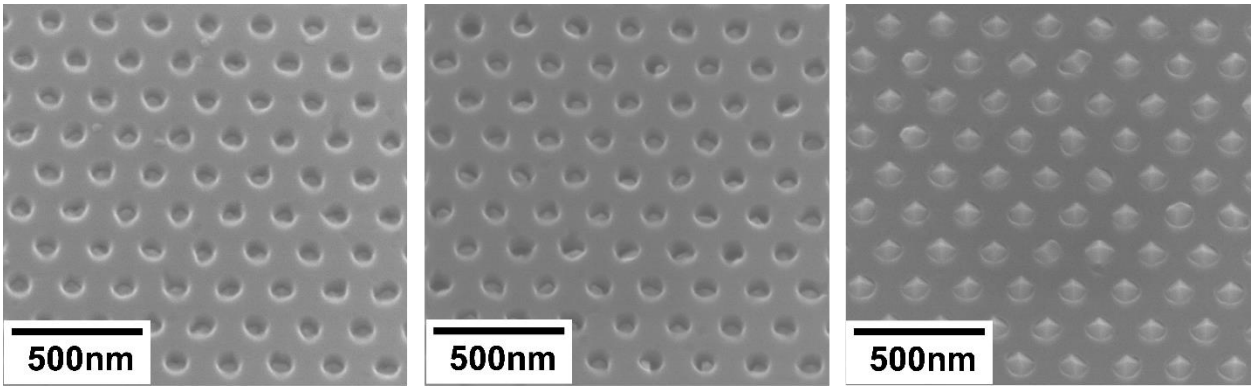


Fig. 4.7 Tilted-view SEM images of *n*-GaAs nanostub arrays of 50 nm in diameter and a hole-to-hole distance of 100 nm, with growth time of (a) 10 min, (b) 20 min, (c) 40 min (T_{SUB}=590–620 °C)

The black dashed box in Figure 4.8 summarizes the optimized MBE growth window found for the SAE of *n*-GaAs nanostubs. Red and blue dots outside this box indicate conditions that resulted in a lack of selectivity due to incomplete filling of nanoholes and polycrystal formation, respectively. Based on the optimized window, fine-tuning of the substrate temperature within the range 590 ℃ and 630 ℃ at a fixed growth rate of 120 nm/hr was performed. To compensate for the higher desorption rate of arsenic at higher temperature, V/III ratio was increased from 15 to 50. TEM samples were extracted to contain a single row of nanostubs with a zone axis of [110]. Uniform *n*-GaAs nanostubs, with clear top/side facets and stacking faults (SFs) at the base, were grown across the whole array of nanoholes at 590 ℃ (Figure 4.8(a)). *n*-GaAs nanostubs grown at T_{SUB}=605−620 ℃ were identical to those grown at 590 ℃ (Figure 4.8(b) and 4.8(c)), confirming that increased V/III ratio maintains GaAs stoichiometry and crystal quality.

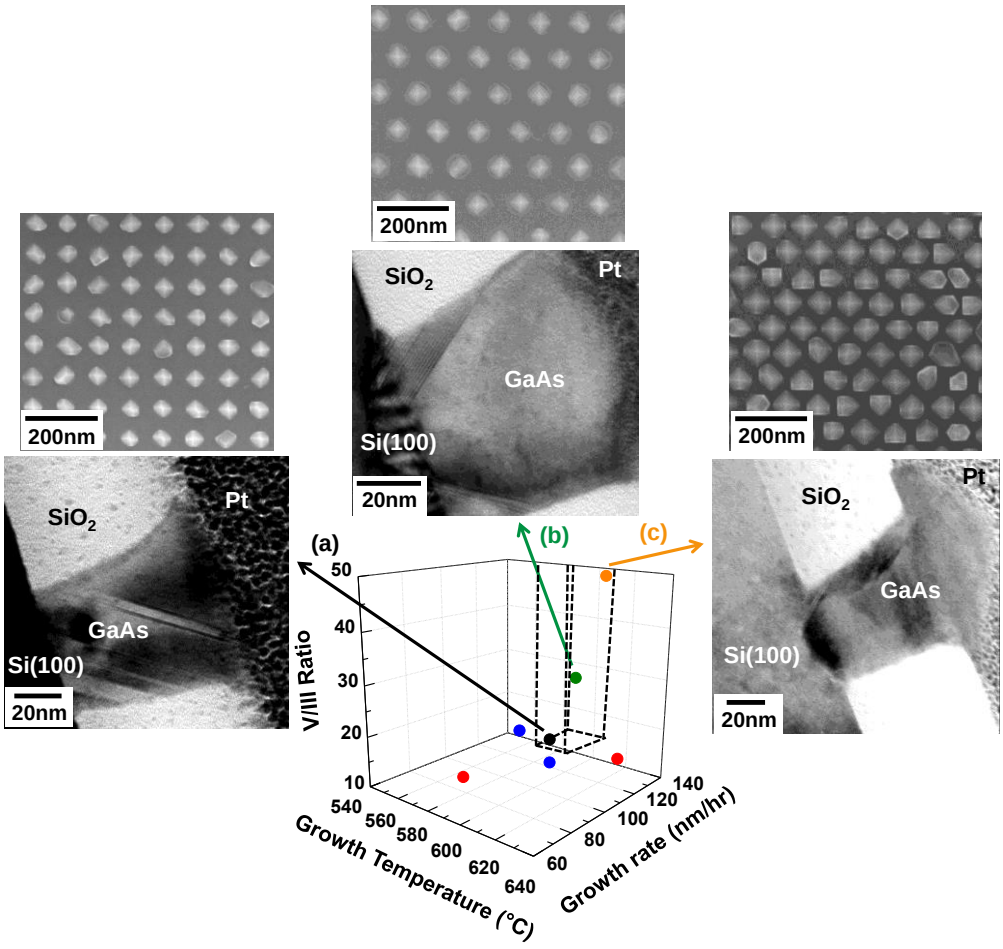


Fig. 4.8 3D optimization window for GaAs/Si nanostub SAG: (a) T_{SUB}=590 ℃/V/III=20 (b) T_{SUB}=605 ℃/V/III=30 and (c) T_{SUB}=620 ℃/V/III=50 (hole diameter: 50 nm, hole-to-hole distance: 100 nm). FESEM (upper) and bright-field XTEM (lower) images are shown for each sample [81]

4.5.2 Selective-Area *n*-GaN Growth

Prior to *n*-GaN SAE, MBE growth of a planar *n*-GaN film with 10 nm-thick *n*-GaAs buffer layer on a 3-inch bulk Si(001) substrate was attempted to verify the feasibility of utilizing a thin *n*-GaAs buffer to obtain zinc-blende GaN on Si. The grown 100 nm-thick *n*-GaN film resulted in

a mixture of wurtzite and zinc-blende phases and its RMS roughness was 8.72 nm shown in Figure 4.9. The result of initial planar *n*-GaN MBE growth demonstrated 85 % zinc-blende *n*-GaN by X-ray diffraction (XRD) ω-2θ scan in Figure 4.10. Since the inter-planar spacing of h-GaN(0002) is 2.593Å, the Bragg's angle (θ) is calculated to be 17.3 º. The XRD ω-2θ scan was performed separately on GaAs/Si(001) sample to confirm the absence of GaAs(002) peak (i.e. θ = 16.2 º) very close to the h-GaN(0002) peak position. Similar to *n*-GaAs buffer MBE growth, *n*-GaN SAE optimization window had been extensively investigated based on four critical MBE parameters: substrate temperature (T_{SUB}), N flux, N plasma power and growth rate. Direct *n*-GaN MBE growth on Si(001) substrates at T_{SUB}=795 ℃ and V/III ratio=5/N plasma=400 W with a low temperature *n*-GaN buffer layer is illustrated in Figure 4.11. The *n*-GaN growth rate in this case has a large variation from 30 nm/hr to 200 nm/hr. Moreover, irregular diameter and height of *n*-GaN pillars were observed as well as droplets formed on the SiO_2-mask. In addition, the SiO_2-patterned holes are incompletely filled, and these nanopillars are grown towards different directions ranging from 0 º to ~30 º with respect to the Si(001) surface normal. Very low yield has been achieved by direct *n*-GaN MBE-based SAE.

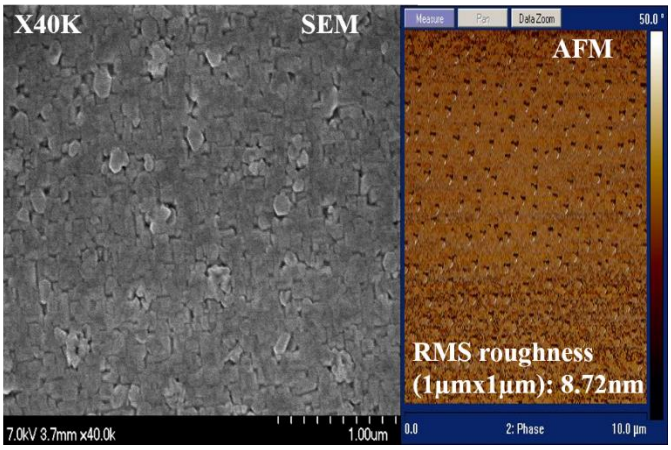


Fig. 4.9 Plan-view SEM (left) and AFM (right) images of a planar *n*-GaN film with 10 nm-thick *n*-GaAs buffer layer on a 3-inch bulk Si(001) substrate (AFM scan area:1 μm x 1 μm)

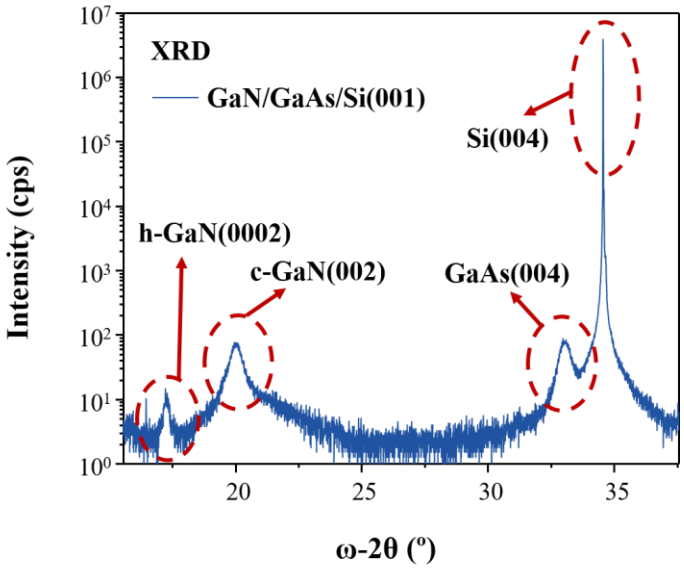


Fig. 4.10 ω-2θ scan of X-ray diffraction on a planar *n*-GaN film with 10 nm-thick *n*-GaAs buffer layer on a 3-inch bulk Si(001) substrate (zinc-blende to wurtzite peak intensity ratio: 6)

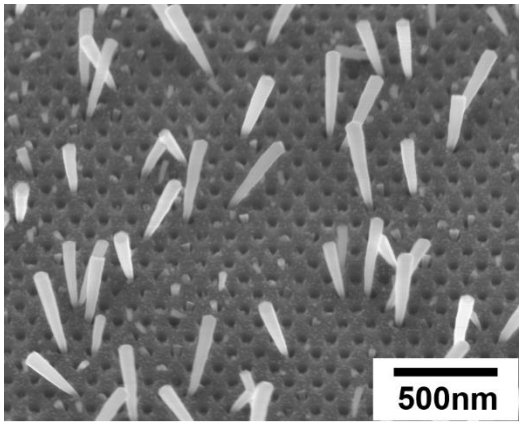


Fig. 4.11 Tilted-view SEM image of direct heavily *n*-doped GaN MBE growth on SiO_2-patterned Si(001) substrates with a low-temperature *n*-GaN buffer layer (hole diameter: 50 nm, hole-to-hole distance: 100 nm)

In order to increase the yield of the direct *n*-GaN growth, As-terminated Si(001) substrates were prepared by soaking the substrates with As_2 for 15 minutes at 300 ℃. *n*-GaN nanostub growth on these substrates at T_{SUB}=795 ℃ and V/III ratio=6/N plasma=400 W with a low temperature *n*-GaN buffer layer resulted in a complete selective-area growth shown in Figure 4.12. However, no coalescence of individual nucleus at the initial nucleation stage was observed, resulting in inhibition of further growth. Further increase in growth yield was obtained by exposing the Si(001) substrate to Ga and As flow prior to the *n*-GaN growth given in Figure 4.13. The growth conditions were T_{SUB}=780 ℃ and V/III ratio=3/N plasma=400 W with a low temperature *n*-GaN buffer layer. This surface treatment resulted in *n*-GaN nanopillars of 400−500 nm in height grown towards <111>-direction with parasitic growth on top of SiO_2 mask. *n*-GaN growth after proper optimization of its growth parameters (i.e. T_{SUB}=795 ℃ and V/III ratio=6/N plasma=400 W) is shown in Figure 4.14. Complete selectivity was achieved with an increase in the substrate temperature by 15 ℃ with higher yield compared to that of the previous methods such as direct

growth and As_2 pre-treatment. However, as the SiO_2-patterned hole size increases, multiple nanopillars are grown from a single hole without their coalescence (Figure 4.15), and thus, it is difficult to control the diameter of *n*-GaN nanopillars using this approach. With regard to the yield, *n*-GaN nanostubs grown on Si(001) with Ga pre-seed growth [87]-[89] at low temperature had the most promising results given in Figure 4.16. The same *n*-GaN growth conditions (i.e. T_{SUB}=795 °C and V/III ratio=6/N plasma=400 W) were applied here as well. However, increasing the growth time did not proceed to further increase in the thickness of these nanostubs, although small nucleation sites tended to agglomerate into a single site. Based on these set of MBE growth experiments, necessity of a thin *n*-GaAs buffer in obtaining complete selective-area growth of single-crystalline zinc-blende *n*-GaN on Si(001) substrates with uniform size is apparent.

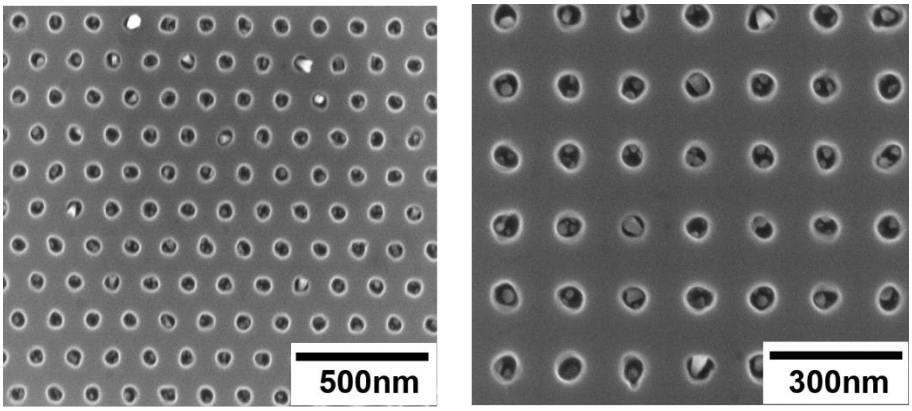


Fig. 4.12 Plan-view SEM images of heavily *n*-doped GaN MBE growth on As-terminated SiO_2-patterned Si(001) substrates with low temperature GaN buffer layer for growth time of 1 hour (left) and 2 hours (right) (hole diameter: 50 nm and hole-to-hole distance: 100 nm)

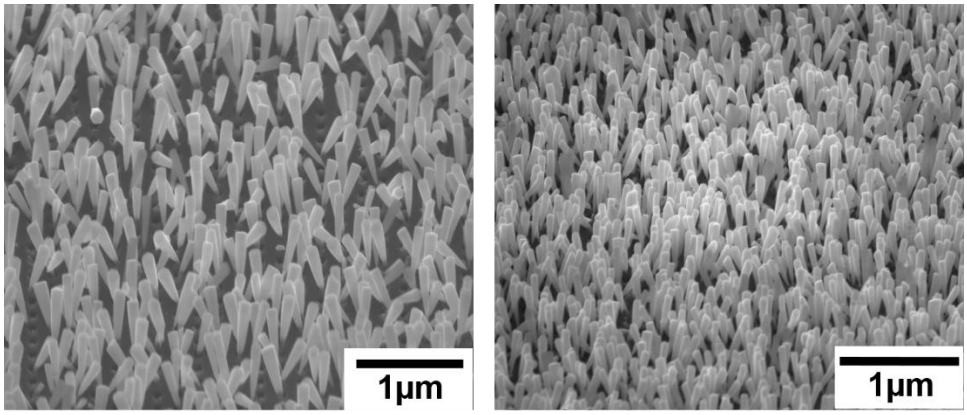


Fig. 4.13 Tilted-view SEM images of heavily *n*-doped GaN MBE growth on Ga/As-pre-treated SiO_2-circle (left)/square (right)-patterned Si(001) substrates with a low-temperature *n*-GaN buffer layer (hole diameter: 50 nm and hole-to-hole distance: 100 nm)

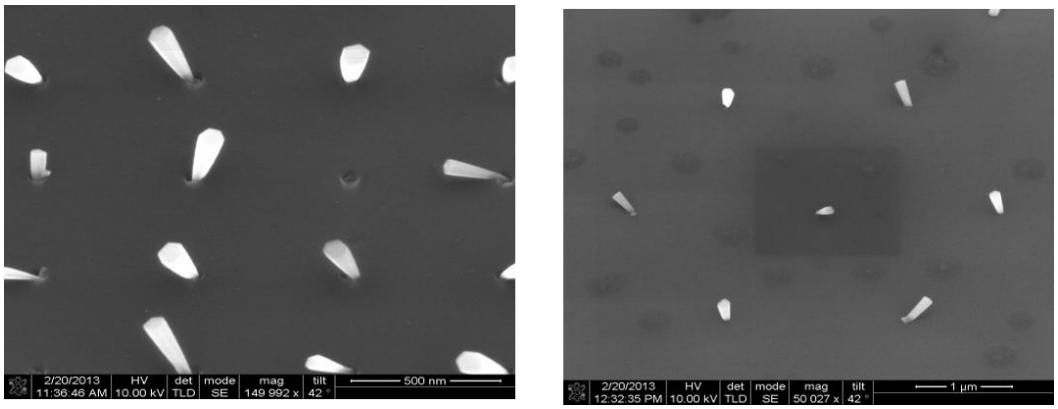


Fig. 4.14 Tilted-view SEM images of heavily *n*-doped GaN MBE growth on Ga/As-pre-treated SiO_2-patterned Si(001) substrates with a low-temperature *n*-GaN buffer layer after proper optimization (hole diameter: 50 nm and hole-to-hole distance: 0.5 μm (left), 2 μm (right))

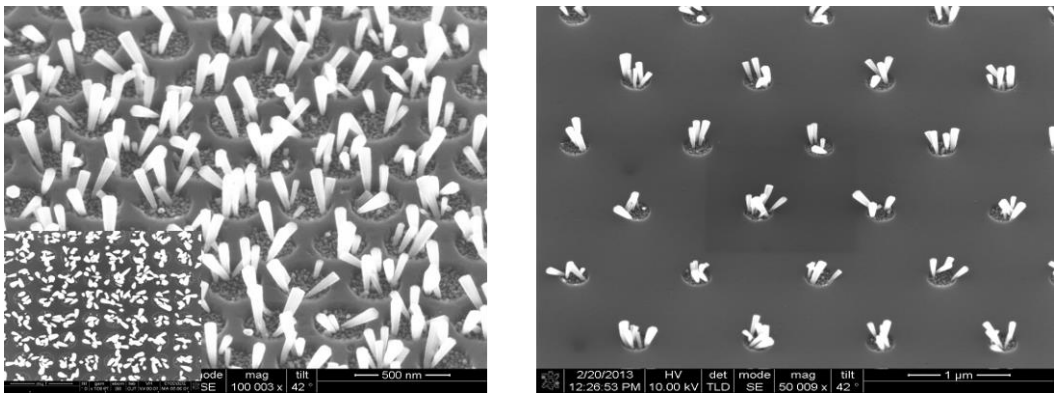


Fig. 4.15 Tilted-view SEM images of heavily *n*-doped GaN MBE growth on Ga/As-pre-treated SiO_2-patterned Si(001) substrates with a low-temperature *n*-GaN buffer layer after proper optimization (hole diameter: 260 nm and hole-to-hole distance: 0.1 μm (left, inset: plan-view), 1 μm (right))

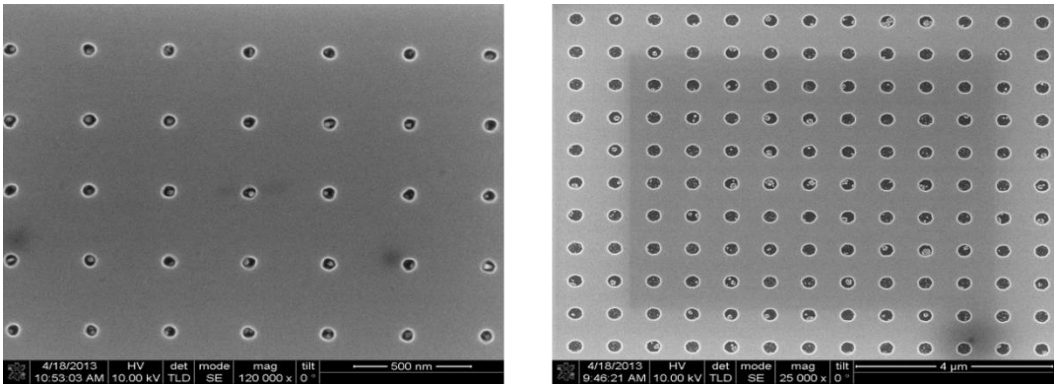


Fig. 4.16 Plan-view SEM images of heavily *n*-doped GaN MBE growth on Ga pre-seed-grown SiO_2-patterned Si(001) substrates with a low-temperature *n*-GaN buffer layer (hole diameter: 50 nm (left)/300 nm (right) and hole-to-hole distance: 300 nm (left)/500 nm (right))

n-GaN MBE-based SAE was performed inserting the *n*-GaAs buffer layer with optimized growth parameters (i.e. T_{SUB}=590 ℃, Ga BEP=1x10^{-7} Torr, and V/III ratio=15) that resulted in a complete selective-area growth. The final results are illustrated in Figure 4.17. This set of

experiment showed the best results compared to all other previous ones. This once again confirmed the need of an *n*-GaAs buffer layer for the complete MBE-based SAE of *n*-GaN on Si(001). However, due to multiple *n*-GaAs facets on top, multiple *n*-GaN pillars in different directions had grown from a single hole. These facets acted as nucleation sites for the subsequent *n*-GaN growth, and thus, it is difficult to grow uniform size *n*-GaN nanostubs. Furthermore, partial evaporation of *n*-GaAs buffer at high growth temperature of *n*-GaN led to a rough surface of *n*-GaAs buffer layer, which also caused multiple *n*-GaN pillars to grow from a single hole without their coalescence. This issue is aggravated for larger SiO_2-patterned hole dimensions illustrated in Figure 4.18. In an attempt to prevent *n*-GaAs buffer evaporation, two-step growth approach was chosen. Low-temperature *n*-GaN was grown at T_{SUB}=520 ℃, followed by high-temperature *n*-GaN growth at T_{SUB}=795 ℃ with Ga BEP=1x10^{-7} Torr and V/III ratio=1, on *n*-GaAs/Si(001). The resulted *n*-GaN pillars show larger diameters compared to those obtained from previously mentioned methods, but growth selectivity was lost due to its low-temperature growth as shown in Figure 4.19.

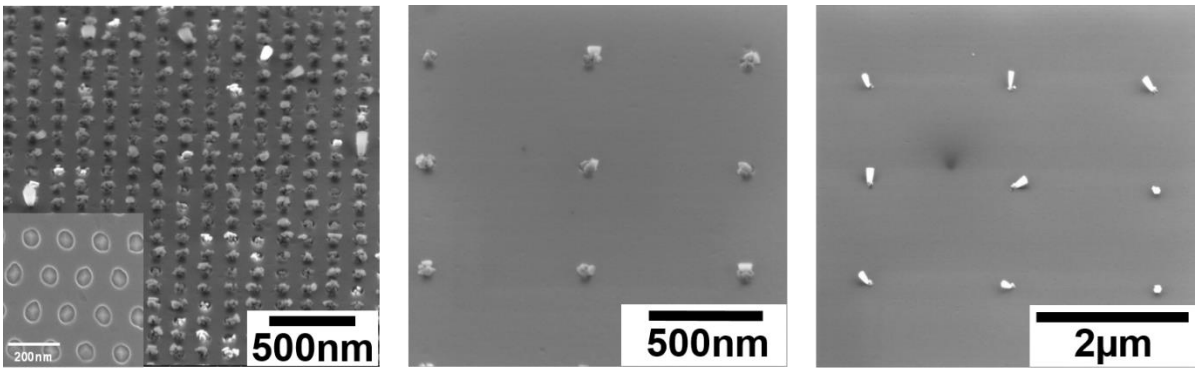


Fig. 4.17 Tilted-view SEM images of heavily *n*-doped GaN MBE growth on SiO_2-patterned thin *n*-GaAs buffer/Si(001) substrates with a low-temperature *n*-GaN buffer layer (hole diameter: 50 nm and hole-to-hole distance: 0.1 μm (left, inset: 40 nm-thick *n*-GaAs buffer layer)/0.7 μm (center)/2 μm (right))

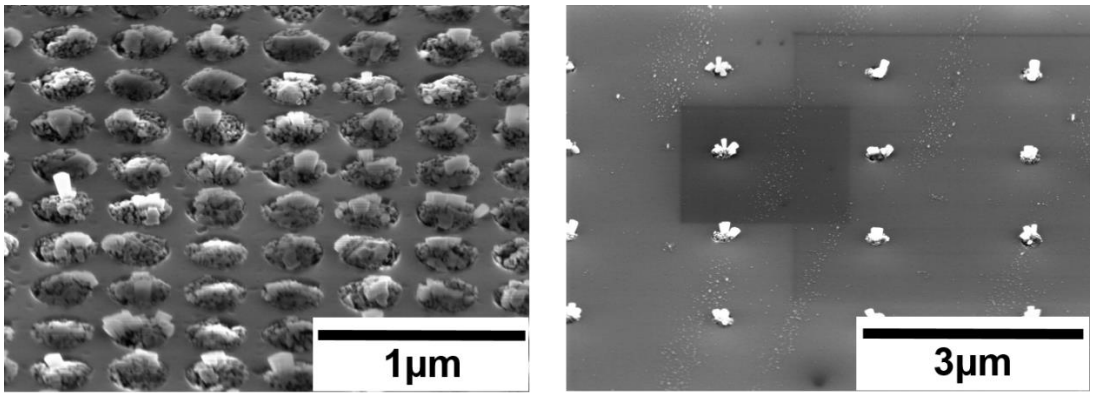


Fig. 4.18 Tilted-view SEM images of heavily *n*-doped GaN MBE growth on SiO_2-patterned thin *n*-GaAs buffer/Si(001) substrates with a low-temperature *n*-GaN buffer layer (hole diameter: 260 nm and hole-to-hole distance: 0.1 μm (left)/2 μm (right))

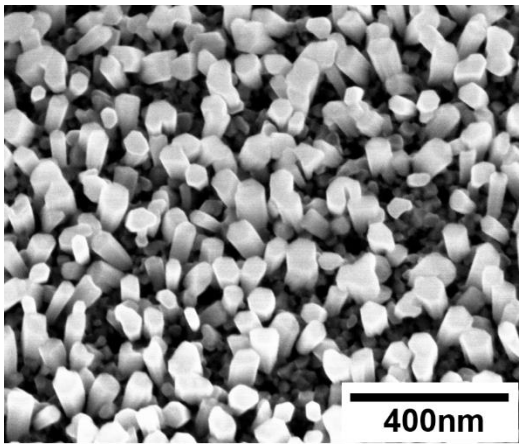


Fig. 4.19 Tilted-view SEM images of heavily *n*-doped GaN MBE growth on SiO_2-patterned thin *n*-GaAs buffer/Si(001) substrates by two-step growth approach (hole diameter: 50 nm and hole-to-hole distance: 100 nm)

Selective-area Ga droplet deposition with subsequent nitridation approach [88], [90] has been investigated as a viable solution to avoid the *n*-GaAs buffer loss during a high-temperature (> 800 ℃) *n*-GaN SAE by capping the whole *n*-GaAs buffer underneath, and to grow uniform size *n*-GaN nanostubs on top of faceted *n*-GaAs buffer layer. It has been understood that higher Ga droplet deposition temperature is required for larger droplet size. Hence, optimization study of the Ga droplet deposition temperature as well as its deposition time was performed. Subsequent nitridation conditions were also optimized in order to minimize the reduction in the droplet size due to the nitridation.

After *n*-GaAs buffer SAE on SiO_2-patterned Si(001) substrate in III-As/Sb chamber, the substrate was directly transferred into III-N chamber under vacuum for Ga droplet deposition. Its temperature was first varied to determine the selective-area deposition window with the time fixed to 5 minutes. The temperature range was kept below 600 ℃ to minimize *n*-GaAs buffer

evaporation underneath. The results imply that the temperature at which Ga droplets are deposited cannot drop below 540 °C for a complete selective-area *n*-GaN growth, as can be seen in Figure 4.20. Selective-area Ga droplet deposition without *n*-GaAs buffer loss was obtained by increasing the T_{SUB} to 570 ℃ shown in Figure 4.21. Interestingly, the deposition preferentially occurred on one of the four facets on top of *n*-GaAs buffer layer, resulting in incomplete coverage of *n*-GaAs layer underneath. Further optimization on the SAE of Ga droplets on *n*-GaAs buffer was performed to effectively prevent the buffer layer loss during the subsequent high-temperature *n*-GaN SAE. As a result of optimizing both the Ga droplet deposition temperature and time, the SAE of Ga droplets with either 90 % coverage of the *n*-GaAs buffer with complete selectivity or a full coverage of the buffer layer with no selectivity was achieved, demonstrated in Figure 4.22. Precise control of complete selective-area Ga droplet deposition fully capping the *n*-GaAs buffer underneath was still difficult. In the earlier approach, the substrate after *n*-GaAs buffer SAE in III-As/Sb chamber was first cooled down to < 300 ℃ in order to get transferred into III-N chamber. It was then heated up to the desired Ga droplet deposition temperature to obtain growth selectivity. Therefore, to eliminate the effect of temperature variation on the Ga droplet coverage of *n*-GaAs buffer underneath, a better approach is to perform *n*-GaAs buffer SAE followed by Ga droplet deposition in III-As/Sb chamber. The results given in Figure 4.23 clearly demonstrate the effectiveness of the proposed method to minimize *n*-GaAs buffer loss during high-temperature *n*-GaN SAE. These Ga droplets were deposited at T_{SUB}=550 ℃ and Ga BEP=$1x10^{-7}$ Torr with 30 minutes of deposition. As shutter was closed several minutes before the start of Ga droplet deposition for removal of background residual As.

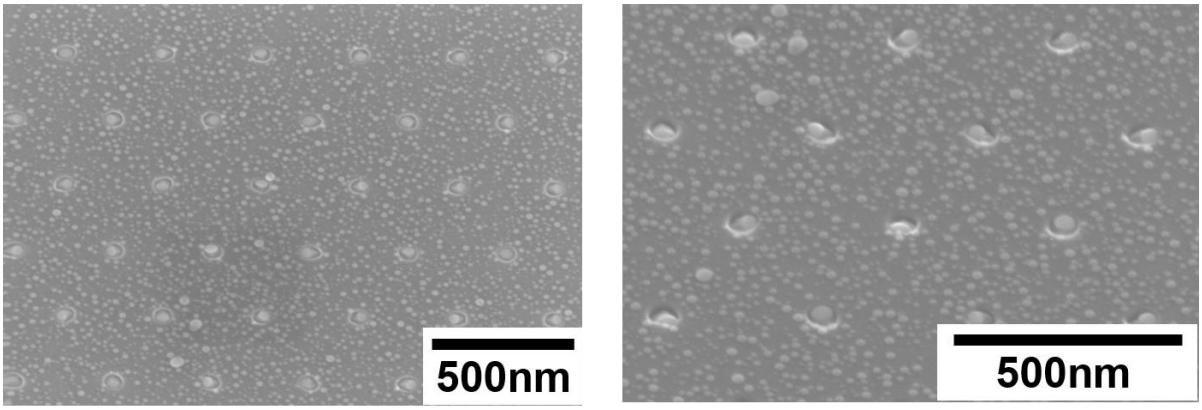


Fig. 4.20 Tilted-view SEM images showing realization of Ga droplet SAE at T_{SUB}=540 °C utilizing 40 nm-thick *n*-GaAs buffer on Si(001) substrates (hole diameter: 50 nm)

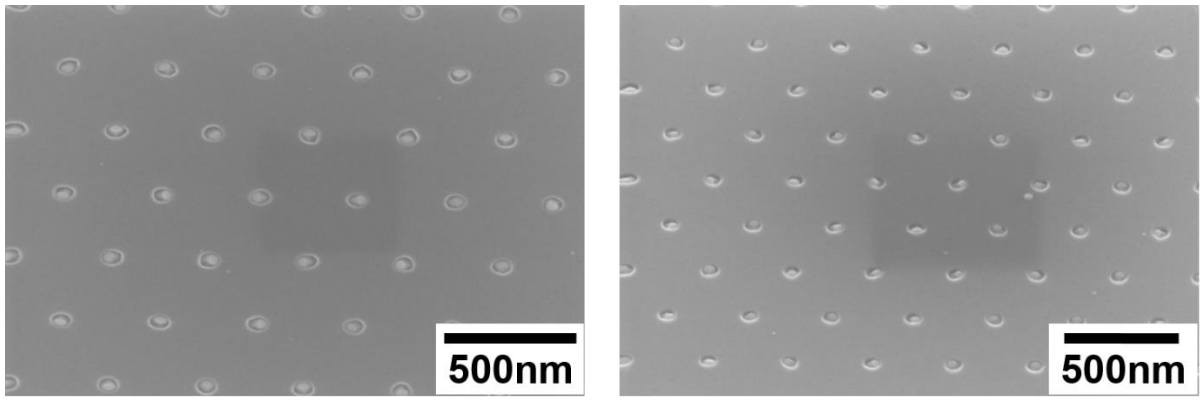


Fig. 4.21 Tilted-view SEM images showing realization of Ga droplet SAE at T_{SUB}=570 °C utilizing 40 nm-thick *n*-GaAs buffer on Si(001) substrates (hole diameter: 50 nm)

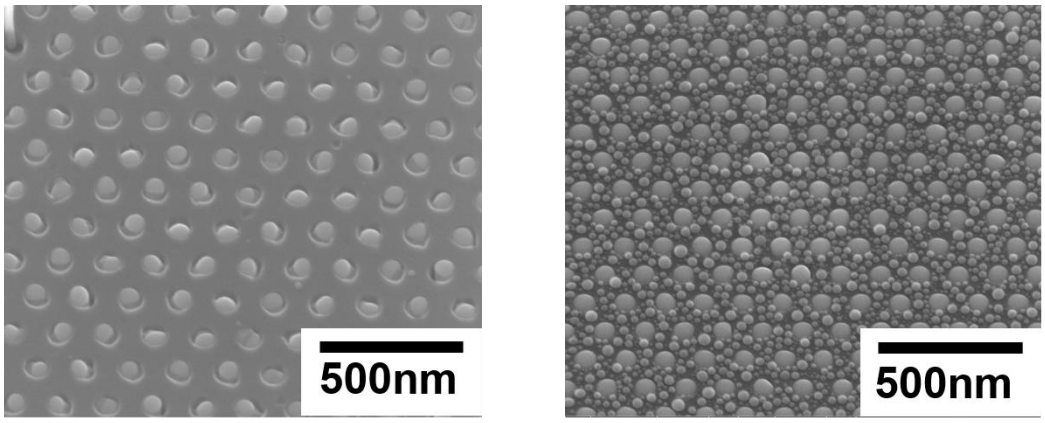


Fig 4.22 Tilted-view SEM images showing realization of Ga droplet SAE at T_{SUB}=550 °C utilizing 40 nm-thick *n*-GaAs buffer on Si(001) substrates (hole diameter: 50 nm, deposition time: 10 min (left)/20 min (right))

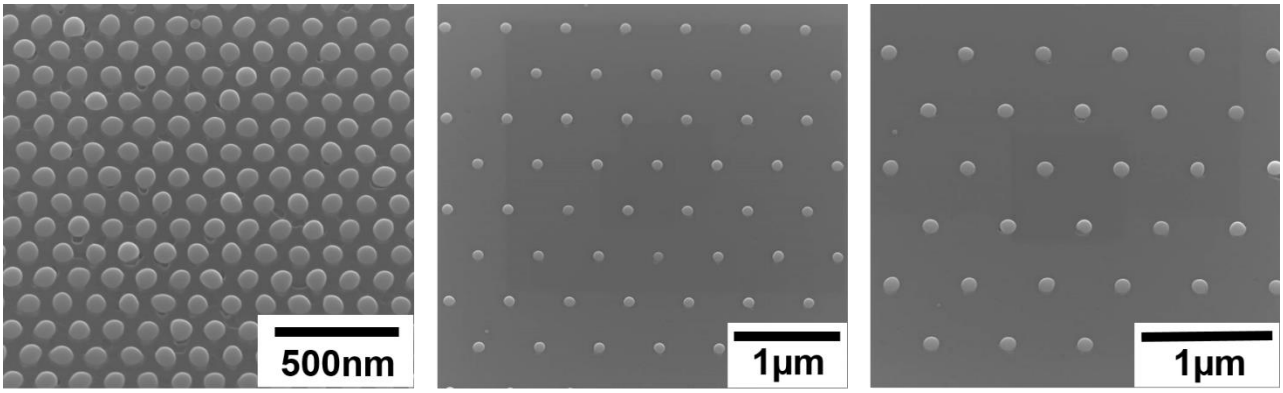


Fig 4.23 Tilted-view SEM images showing realization of Ga droplet SAE at T_{SUB}=550 °C utilizing 40 nm-thick *n*-GaAs buffer on Si(001) substrates in III-As/Sb chamber (hole diameter: 50 nm (left)/75 nm (center)/100 nm (right), deposition time: 30 min)

Subsequent nitridation of selectively deposited Ga droplets on *n*-GaAs/Si(001) substrates was performed at T_{SUB}=300 ℃ with V/III BEP ratio=7/N plasma=350 W. The nitridation time was varied from 5 minutes to 20 minutes, and the results are illustrated in Figure 4.24. The Ga droplets

had been deposited in III-As/Sb chamber for 30 minutes. Selective nitridation only on the four facets of *n*-GaAs buffer underneath was observed at T_{SUB}=300 °C. Moreover, there was no difference in *n*-GaN morphology after 5 minutes of nitridation, and thus, 5-minute was sufficient to nitridize the Ga droplets on *n*-GaAs/Si(001). On the other hand, nitridation at a higher temperature of T_{SUB}=500 °C led to a more uniform coverage of *n*-GaAs buffer shown in Figure 4.25.

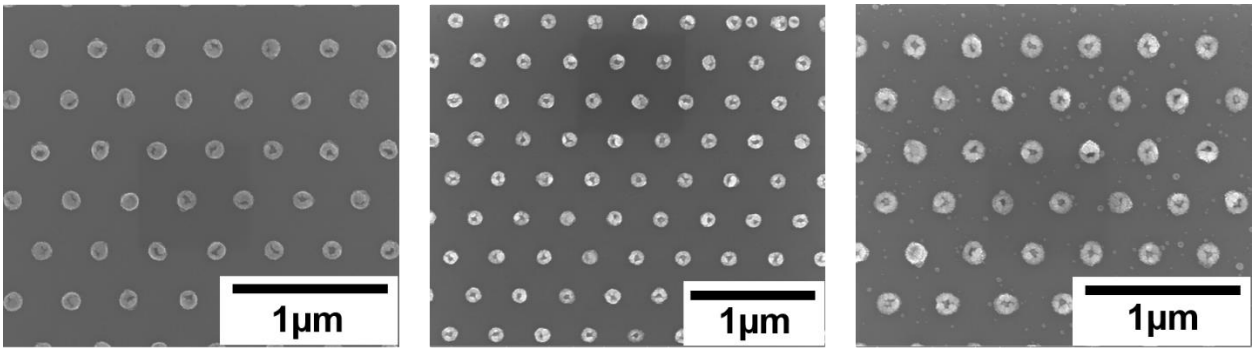


Fig 4.24 Plan-view SEM images of nitridation of selectively-deposited Ga droplets on *n*-GaAs/Si(001) substrates at T_{SUB}=300 °C (hole diameter: 75 nm, nitridation time: 5 min (left)/10 min (center)/20 min (right))

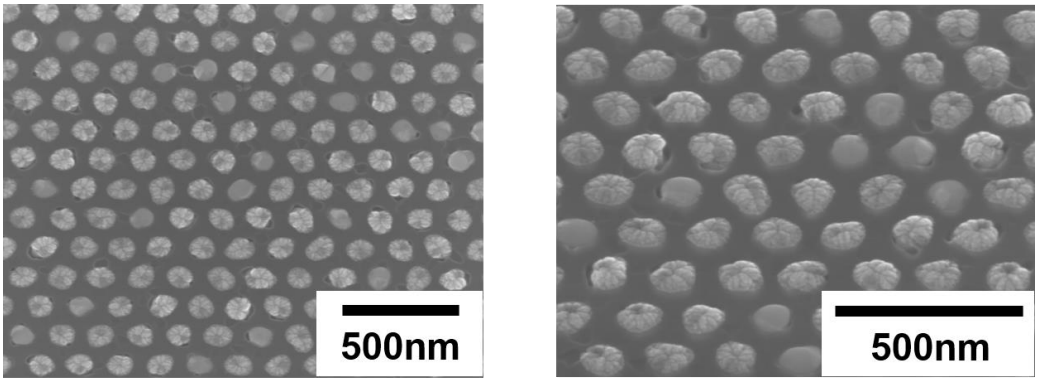


Fig 4.25 Plan-view (left) and tilted view (right) of Ga droplet nitridation at T_{SUB}=500 ℃ (hole diameter: 75 nm, nitridation time: 5 min)

4.6 MBE Film Characterization

High quality single-crystalline *n*-GaAs buffer is a prerequisite for obtaining the subsequent defect-free zinc-blende *n*-GaN films. It is, therefore, important to characterize *n*-GaAs buffer layer, especially in the early growth stage of its nucleation. Study on the morphologies of the *n*-GaAs nanostubs on SiO_2-patterned Si(001) substrates was done using a FEI Nova 600 dual-beam field-emission scanning electron microscopy (FESEM). Furthermore, cross-sectional transmission electron microscopy (XTEM) images were taken with a FEI Titan microscope operated at 300 kV to assess the structural properties and crystalline quality.

Figure 4.26(a), (b), and (c) show the structure of the Si/GaAs/SiO_2 heterointerface at the base of the ART-grown *n*-GaAs nanostubs. These nanostubs were grown up to 140 nm in height at 620 °C with V/III ratio of 50 and a growth rate of 120 nm/hr. Nanostubs grown at 590 °C and 605 °C are not shown here but their structural properties are very similar to those shown in Figure 4.26. The TEM images were obtained along the [110] zone axis. Fast Fourier transform (FFT) analysis of the area marked (d) in Figure 4.26(c) reveals the single-crystalline nature of the Si(001)

substrate (Figure 4(d)). FFT analysis of the interface area (e) in Figure 4.26(c) reveals streaking along the (-111) plane. These streaks in the FFT are consistent with the low density stacking faults along the preferred {111} plane [45], [91] we can see in this region in Figure 4.26(c). In contrast, the FFT in Figure 4.26(f) (from area (f) in Figure 4(c)) shows that away from the interface the ART-grown *n*-GaAs nanostubs are zinc-blende in structure and dislocation-free. No threading dislocations were observed in the nanostub, in agreement with other ART-grown nanostructures in the literature [57], [92], [93]. Although the complete elimination of defects was not achieved, Figure 4.26(c) shows that the penetration of these stacking faults to the upper regions of the GaAs nanostubs was effectively suppressed.

There is an additional benefit that arises from this procedure. During the patterning of the nanoholes in the SiO_2 mask, the RIE process creates slight, concave-shaped pits in the Si surface. It transpires that by forming additional atomic steps, this pit helps eliminate the anti-phase domain boundaries prevalent in the heteroepitaxial growth of planar GaAs films on Si substrates [94]. The out-of-plane and in-plane lattice parameters of *n*-GaAs nanostubs grown between 590 °C and 620 °C were measured from high-resolution FFTs. Looking both at the Si substrate (Figure 4.26(d)) and the GaAs above the stacking fault region (Figure 4.26(f)), strain relaxation in the *n*-GaAs nanostubs is ≥99 % in the in-plane direction (Figure 4.27). Furthermore, two methods for statistical defect quantification were performed on XTEM images from samples with growth conditions as follows: (a) T_{SUB}=590 °C/V/III=16 (b) T_{SUB}=605 °C/V/III=30 and (c) T_{sub}=620 °C/V/III=50 (growth rate=120 nm/hr for each). The first method seeks to quantify defects in the nanostubs in terms of area. In Figure 4.28(a), the red dotted line marks the total area of a single nanostub, while the region containing stacking faults is bounded by a yellow dotted line. On average, stacking faults occupy less than 40 % of the total area of the nanostub with a standard deviation of 17.5 %

across the substrate temperature range 590 °C-620 °C. The second method aims to quantify the number of defects that propagate to the top facets. Total facet perimeter is defined as the sum of top two facet perimeters, shown Figure 4.28(b) with red dotted lines. Regions in Figure 4.28(b) where stacking faults intersect these facets are highlighted with yellow dotted lines. Stacking faults make up on average, less than 10 % of the total perimeter of the top facets with a standard deviation of 8.6 % across the substrate temperature range 590 °C-620 °C (Figure 4.28(a) and (b)). We attribute the fact that the defect densities are very low in the *n*-GaAs nanostubs to the necking effect of the nanopatterned substrate, which means that stacking faults often annihilate at the GaAs/SiO_2 sidewall interfaces.

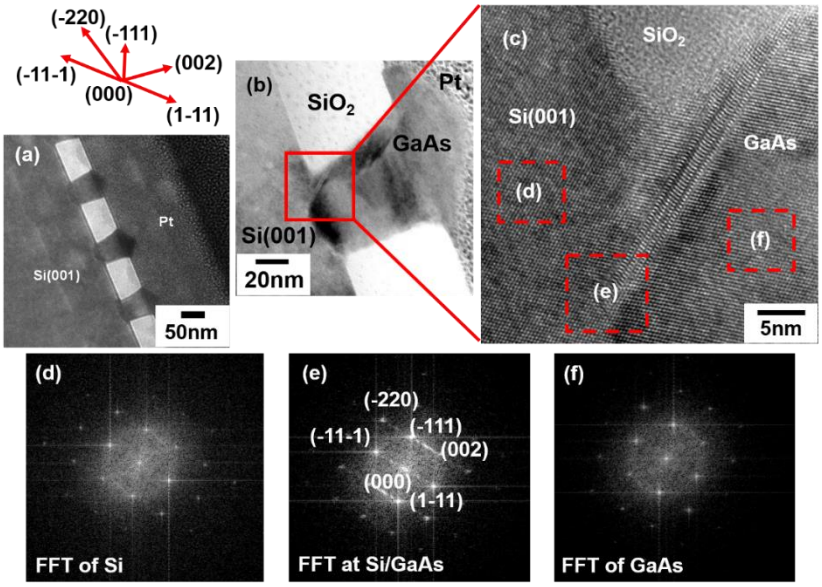


Fig 4.26 MBE-based SAE of *n*-GaAs nanostub on SiO_2-nanopatterned Si(001) substrate (T_{SUB}=620 °C/V/III=50/growth rate=120 nm/hr): Bright-field XTEM images of (a) an array of *n*-GaAs nanostubs (b) enlarged *n*-GaAs nanostub (c) HRTEM image near the Si/GaAs interface (d) FFT of Si (e) FFT at Si/GaAs interface (f) FFT of GaAs (hole diameter: 50 nm, hole-to-hole distance: 100 nm)

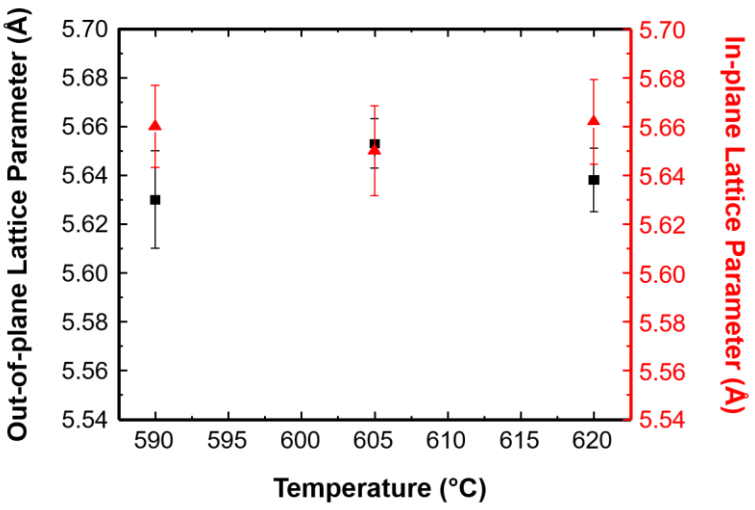


Fig 4.27 Lattice parameter calculations in various 50 nm-diameter *n*-GaAs nanostubs using fast Fourier transform (FFT) images generated from TEM measurements (Both out-of-plane and in-plane lattice constants confirm the nearly strain-free (≥99 %) *n*-GaAs nanostubs using SAE (Strain-free GaAs lattice parameter: 5.65325 Å))

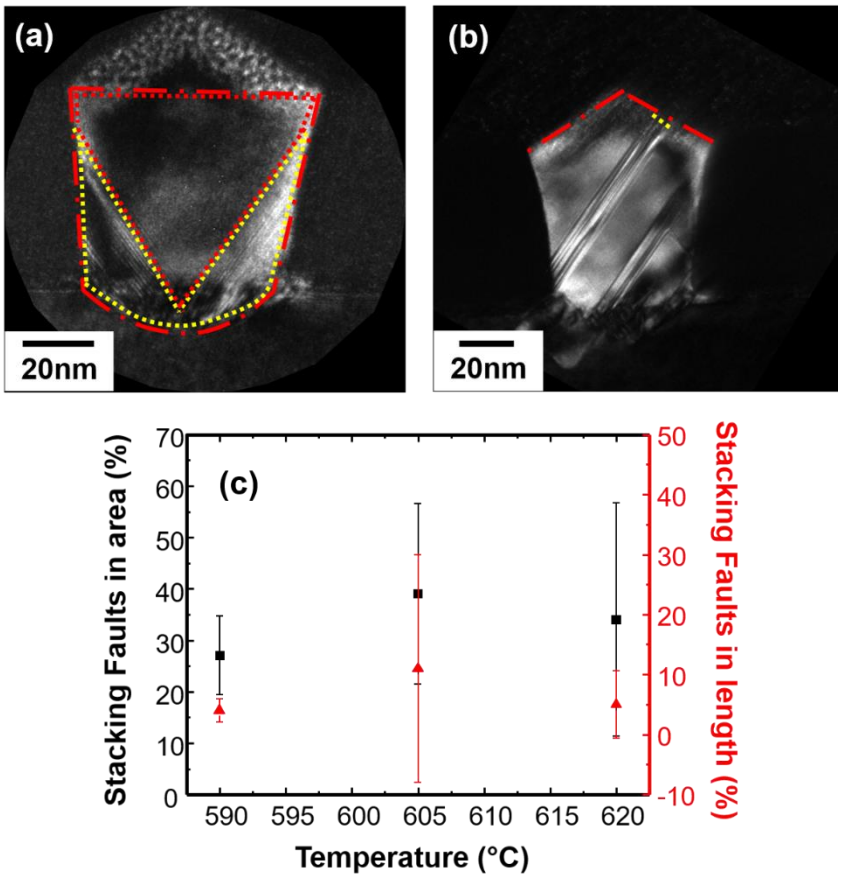


Fig 4.28 (a) Defect quantification method 1 (yellow square dotted region: stacking faults region, red square dotted region: defect-free n+GaAs region, red dash dotted region: total area of the nanostub) and (b) defect quantification method 2 (yellow square dotted line: stacking faults region, red dash dotted line: total facet perimeter) via dark-field XTEM images of single *n*-GaAs nanostub with diameter of 50 nm and hole-to-hole distance of 100 nm; (c) defect quantification results using method (a) and (b) at various growth temperatures (left axis: the percentage of stacking faults contained in total nanostub area; right axis: the percentage of stacking faults propagated onto top two facets)

4.7 Summary

Complete selective-area MBE-based *n*-GaAs buffer growth on SiO_2-nanopatterned Si(001) substrates utilizing ART technique successfully resulted in nearly strain-free *n*-GaAs nanostubs without the presence of threading dislocations prevalent in planar GaAs film growth. Further reduction in stacking faults can be obtained through proper surface treatments to remove etch damages. On top of this high quality *n*-GaAs buffer on Si(001), MBE-based ART of uniform *n*-GaN nanostubs with complete selectivity was achieved by selective-area Ga droplet deposition with its subsequent nitridation approach. Extensive studies and precise control of initial nucleation stage of *n*-GaN/*n*-GaAs/Si(001) demonstrate its feasibility of successful heterogeneous integration of III-V materials with Si CMOS for various device/system applications.

4.8 Bibliography

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CHAPTER 5

Fabrication of GaAs/Si Heterogeneous PN Diodes

5.1 Introduction

In realizing the proposed device structure, wide bandgap drain heterogeneous multiple-gate field-effect transistor, understanding the effect of defects in GaAs/GaN and/or at the heterointerface between Si and GaAs/GaN on device performances is of great importance. This can be done by electrical measurements utilizing a simple PN diode, in order to investigate the quality of the heterointerface as well as crystallinity of the MBE-grown films. Moreover, experimental study on the effect of nanostub size on the defect density utilizing the aspect-ratio trapping (ART) technique is necessary in order to realize a successful 'junction-level' heterogeneous integration of III-V materials with Si CMOS.

5.2 Process Flow

Proposed process flow and its details are given in Figure 5.1 and Table 5-1.

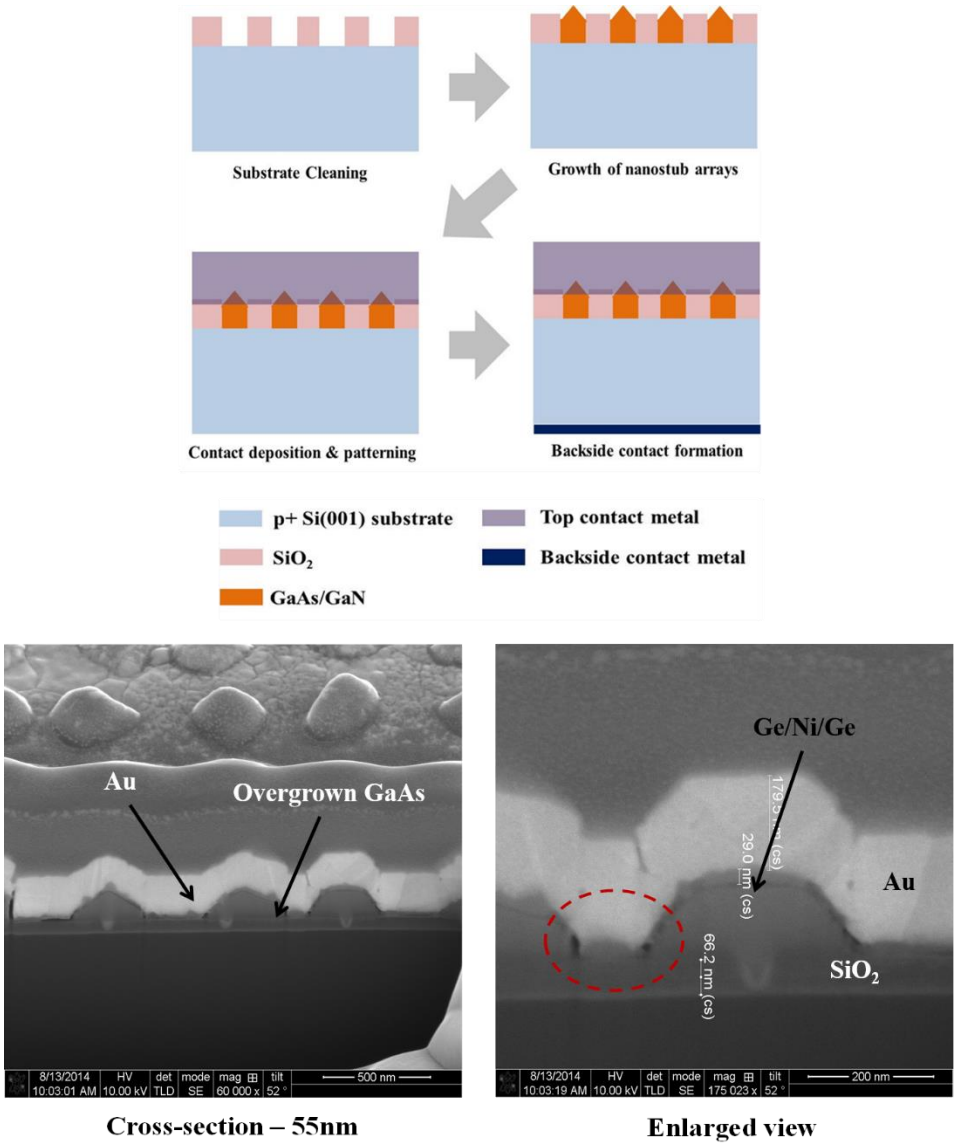

Fig 5.1 Schematic diagram of brief heterogeneous vertical GaAs/Si diode process flow (top) & cross-sectional SEM (XSEM) images of the fabricated diode structure (bottom)

Table 5-1 Details of Heterogeneous GaAs/Si Diode Process Flow

Step	Process	Conditions/Comments
1	Substrate preparation	AMI rinse + Piranha clean + HF dip
2	Growth of vertical GaAs/GaN nanostub arrays	p+Si/n-GaAs & p+Si/n+GaAs
3	Removal of native oxide on top of GaAs/GaN	BOE dip
4	Top contact definition/patterning with different contact sizes	Pd/Ge/Au, Ge/Ni/Ge/Au
5	Backside contact formation	Ti/Al
6	Rapid thermal annealing (RTA)	< 450℃

5.3 Experimental Setup

In order to realize the proposed structure including a small-area (<0.1 μm^2) GaN drain, substrate nano-patterning technique on a bulk Si(001) substrate using e-beam lithography and reactive ion etching (RIE) has been developed, in agreement with aspect-ratio trapping (ART) discussed in the previous section. This technique prevents random positioning and size variation of GaAs/GaN nanostubs, and thus allows good controllability and reproducibility for the subsequent selective-area MBE growth. Heterogeneous n+GaAs/p+Si PN diodes with variations in n+GaAs nanostub height were fabricated with Pd/Ge/Au and Al metal contacts to n+GaAs nanostubs and p+Si substrate, respectively. An array of n+GaAs nanostubs with 55nm in diameter selectively grown on SiO_2-patterned Si(001) substrates was covered with blanket Pd/Ge/Au films. These metal films were then patterned using lift-off to form metal contacts to n+GaAs nanostubs.

5.4 Device Performance

As can be seen from the I-V curves in Figure 5.2, a vertical PN diode with taller n+GaAs nanostubs (i.e. 100 minutes of growth) resulted in less leakage currents than that of shorter ones (i.e. 45 minutes of growth). However, the measured current density even without contact annealing is unacceptably high for these diode currents, verifying the penetration of metal contact (Au) into the n+GaAs nanostubs, further reducing their effective height. In order to choose appropriate contact materials to n+GaAs nanostubs, various contacts were investigated. Along with Pd/Ge/Au films, Ge/Ni/Ge/Au films were deposited as contact materials for n+GaAs nanostubs in the heterogeneous vertical PN diodes. I-V measurements of these diodes with and without contact annealing were performed and shown in Figure 5.3. Vertical PN diodes with Ge/Ni/Ge/Au contact behave as a rectifier before annealing. However, their reverse bias leakage currents increased to the similar level of their forward bias currents after the heat treatment for ohmic contact formation. From these results, it can be concluded that Pd/Ge/Au contact is not suitable for sub-100 nm n+GaAs nanostubs with 120 nm in height, although it is extensively utilized as an ohmic contact to planar n+GaAs films. Therefore, two other diode structures were fabricated in order to minimize the interaction between contact metal and GaAs underneath. First, Ti was used as a diffusion barrier material to prevent the metal/GaAs interaction [1], [2]. Vertical PN diodes of the same dimension n+GaAs nanostubs as in Figure 5.3 with Ti/Pt/Au contact were measured before and after contact annealing. Due to a high Schottky barrier (0.26 eV) formed between metal and GaAs, the measured currents were still in the noise level after the contact annealing at less than 600 °C. Contact annealing at above 600 °C leads to ohmic behavior for the Ti/Pt/Au contact to n+GaAs layer. However, due to a possible As out-diffusion above 400 °C, annealing temperature above

600 °C is unacceptable for small-dimension n+GaAs nanostubs. Another method used to eliminate the interaction of metal and GaAs is to grow planar 2D GaAs films on top of the nanostubs. However, due to coalescence of neighboring n+GaAs nanostubs as well as growth on the SiO_2 mask layer, crystal quality of grown n+GaAs layer is expected to be much worse than that of GaAs nanostubs without coalescence. This conjecture was verified through I-V measurements of these PN diodes shown in Figure 5.4. Effect of heat treatment on the measured diode currents especially in the reverse bias region was still observed in the PN diodes with thicker n+GaAs layer. Moreover, due to a rough GaAs surface, contact metal adhesion to the GaAs surface is weak and can be easily peeled off during lift-off. Furthermore, very long growth of GaAs film is necessary in order to smooth out the rough surface with much smaller hole-to-hole distance for eliminating the growth from the SiO_2 mask layer. This method is obviously very time-consuming as well as costly.

Based on the electrical measurement results utilizing different contact metals and n+GaAs nanostub height, there is likely an enhancement in the contact metal diffusion into the n+GaAs nanostubs in the presence of high density of stacking faults penetrating towards the n+GaAs nanostub top facets. From previous TEM results, most of the stacking faults are generated from the GaAs/Si heterointerface. Therefore, methods to obtain the smooth interface such as KOH dip for etch damage removal and combination of dry/wet oxide etch can lower the reverse bias leakage current. To conclude, I-V characteristics of various sizes of n+GaAs nanostubs were studied, and reduction in nanostub diameter from 100 nm to 55 nm resulted in an improvement in the diode performance by reducing the distance that dislocations have to glide before termination on a sidewall, shown in Figure 5.5. However, despite GaAs/Si(001) nanostubs are threading dislocation-free, reverse leakage current is higher than was reported for a selectively grown GaAs/Si(111) *p-i-n* solar cell [3]. This is believed to be the result of lower surface/interface

energies of Si(111), providing superior film quality and heterointerfaces compared to the growth on Si(001). Since few studies measured the GaAs/Si(001) electrical properties and none have looked specifically at the electrical behavior of its heterointerface [4], [5], this work provides valuable information and the promise of this approach for future nanoscale heterostructure devices integrated with Si CMOS.

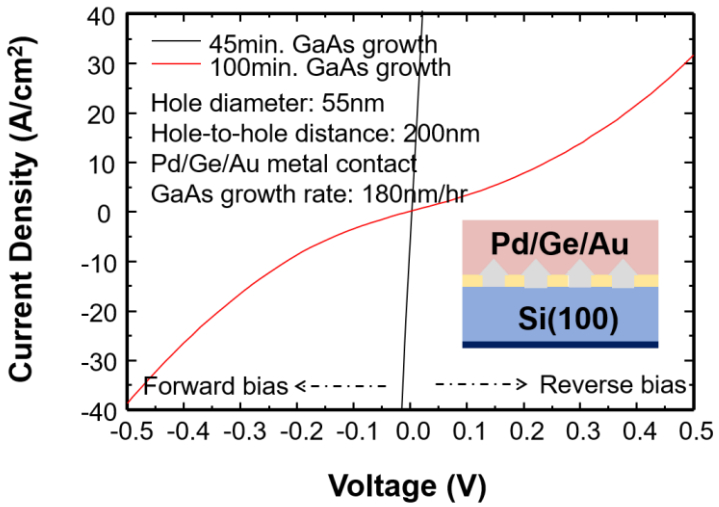

Fig 5.2 Electrical characteristics (I-V curves) of heterogeneous n+GaAs/p+Si vertical PN diodes with different n+GaAs nanostub height with Pd/Ge/Au and Al metal contacts to n+GaAs and p+Si, respectively (PN junction occurs at GaAs/Si heterointerface in the vertical direction)

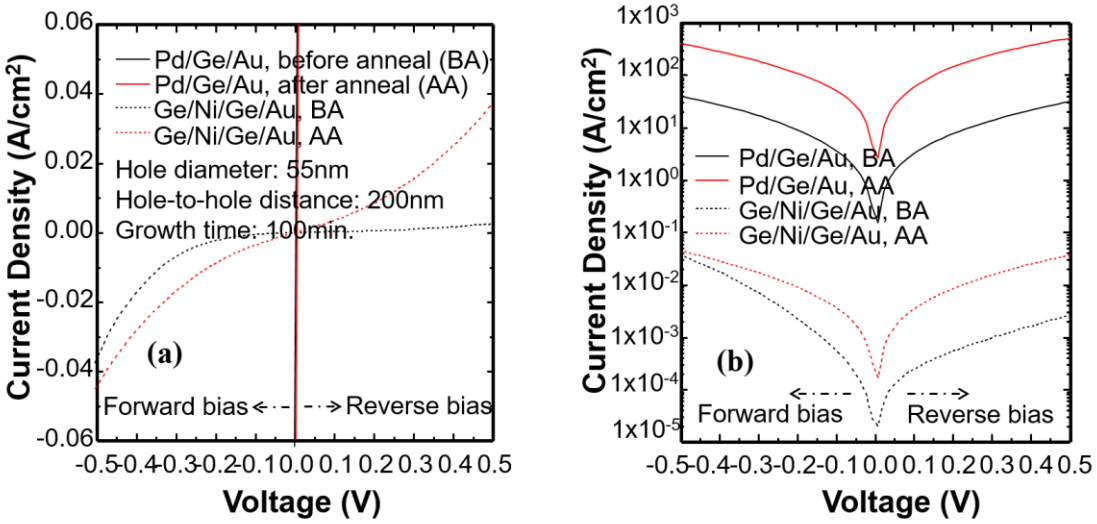

Fig 5.3 Electrical characteristics (I-V curves) of heterogeneous n+GaAs/p+Si vertical PN diodes with different metal contacts to n+GaAs nanostubs before and after contact annealing: (a) linear I-V curves and (b) logarithmic I-V curves

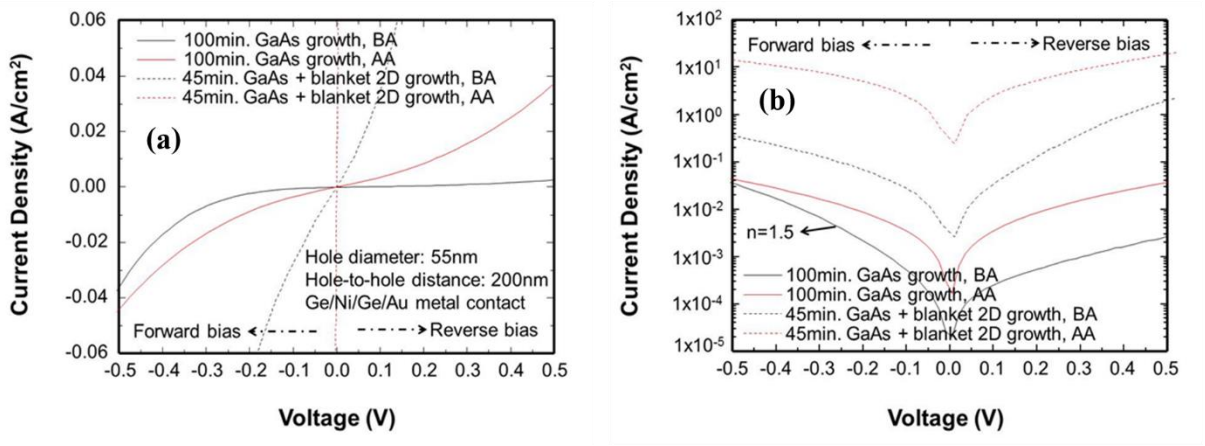

Fig 5.4 Electrical characteristics (I-V curves) of heterogeneous n+GaAs/p+Si vertical PN diodes with different n+GaAs nanostub heights before and after contact annealing using Ge/Ni/Ge/Au metal contact: (a) linear I-V curves and (b) logarithmic I-V curves

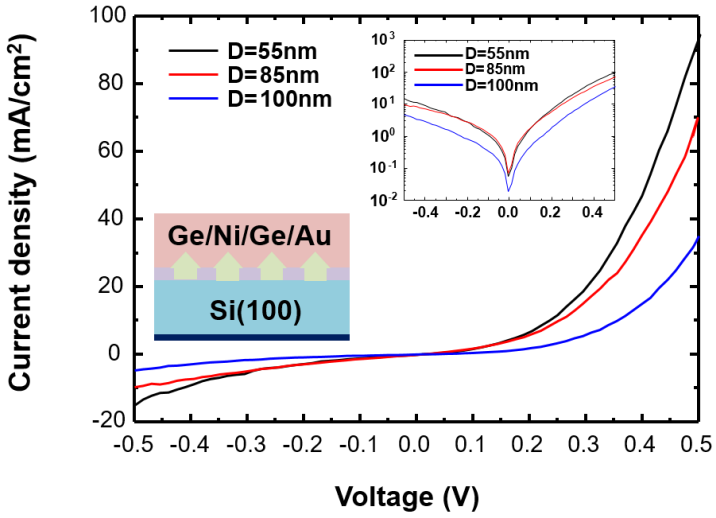

Fig 5.5 Current-voltage (I-V) electrical measurement plot of heterogeneous n+GaAs/p+Si vertical PN diode (T_{SUB}=605 °C/V/III=30/growth rate=120 nm/hr)

Table 5-2 Process Flow of Widegap Drain Heterogeneous SOI Multiple-Gate MOSFET

Step	Process flow	Description
(1)	Pre-alignment (PM) marker definition	(a) DUV lithography, ASML stepper (b) HBr/Cl_2-based Si dry etch, 30 sec
(2)	Multi-layer deposition	(a) Pad oxidation @900 °C, 1 hr (b) Si_3N_4 deposition @800 °C, 1 hr 30 min (c) LTO deposition @450 °C, 20 min (d) Si_3N_4 deposition @800 °C, 5 min (e) Poly-SiGe deposition @450 °C, 3 hrs
(3)	Sidewall image transfer (SIT)	(a) DUV lithography, ASML stepper (b) HBr/Cl_2-based SiGe dry etch, 1 min (c) LTO spacer deposition, 20 min (d) CF_4/CHF_3-based LTO spacer dry etch, 50 sec (e) HBr/O_2-based SiGe removal dry etch, 2 min (f) CF_4/CHF_3-based LTO dry etch, 30 sec (g) CF_4/CHF_3-based Si_3N_4 dry etch, 1 min (h) HBr/Cl_2-based Si fin dry etch, H_{fin}=50/100 nm
(4)	Hard mask removal	(a) LTO removal by dilute HF (b) Si_3N_4 removal by hot phosphoric acid

(5)	Gate stack formation	(a) H_2 annealing @900 °C (b) Sacrificial oxidation @780 °C (c) Sacrificial oxide removal by dilute HF (d) Gate oxidation @780 °C (e) n+poly-Si deposition @615 °C (f) LTO deposition @450 °C
(6)	Gate patterning	(a) DUV lithography, ASML stepper (b) Resist trim (c) CF_4/CHF_3-based LTO dry etch (d) HBr/Cl_2-based n+poly-Si gate patterning (e) n+poly-Si reoxidation @900 °C
(7)	S/D ion implantation	(a) Screen oxide deposition @450 °C (b) Source implantation, outsourcing
(8)	Drain growth mask formation	(a) LTO spacer deposition @450 °C (b) CF_4/CHF_3-based LTO spacer dry etch (c) LTO deposition @450 °C (d) LTO anneal @800 °C (e) LTO wet etch by dilute HF (f) Si dry/wet etch
(9)	Drain selective-area growth	(a) Si drain selective-area epitaxy by RPCVD (b) GaAs/GaN and/or AlN/GaN selective-area epitaxy by MBE (c) Screen oxide deposition @450 °C (d) Si drain extension implantation, outsourcing (e) LTO deposition @450 °C (f) CF_4/CHF_3-based LTO dry etch (g) Screen oxide deposition @450 °C (h) Deep Si drain implantation, outsourcing
(10)	S/D activation	(a) Passivation oxide deposition (b) Anneal/activation @900 °C
(11)	Backend process	(a) CF_4/CHF_3-based contact hole dry etch (b) Contact metal (Ti) sputtering (c) Contact pad (Al(98 %)/Si(2 %)) deposition (d) Cl_2/BCl_3-based contact pad (Al(98 %)/Si(2 %)) dry etch (e) Body contact (Al(98 %)/Si(2 %)) deposition (f) Forming gas anneal @400 °C

5.5 Summary

Detailed electrical analysis on the performance of heterogeneous n+GaAs/p+Si vertical PN diodes with various contact metals as well as its *n*-GaAs nanostub height was performed. Careful choice of metal contact is crucial in 55 nm-diameter GaAs nanostubs with its height of 120 nm. In addition, possibility of metal diffusion into n+GaAs nanostubs with the help of stacking faults as well as their presence in the grown nanostubs and at GaAs/Si heterointerface resulted in a higher reverse leakage current than that of selectively grown GaAs/Si(111) *p*-*i*-*n* solar cell due to superior Si(111) film quality coming from its lower surface/interface energies compared to that of Si(001). However, the initial electrical characteristics study on MBE-based selective-area GaAs/Si(001) growth gives physical insights into the feasibility of 'junction-level' heterogeneous integration of III-V materials with Si CMOS for realizing transistors in analog/RF/mixed signal and high voltage/power SoC applications.

5.6 Bibliography

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CHAPTER 6

Conclusions and Future Work

6.1 Conclusions

In this dissertation, extensive theoretical analysis/simulations of the proposed device concept/architecture were performed utilizing numerical simulation tools. Device performance assessment utilizing a 3D multiple-gate structure for low-power analog/RF/mixed-signal SoC applications was completed, followed by analyses on the impact of channel engineering on analog/RF/mixed-signal metrics. Moreover, wide bandgap drain heterogeneous 3D multiple-gate field-effect transistor was thoroughly studied utilizing numerical simulation tools for high-power RF SoC applications. Complete selective-area growth of single-crystalline *n*-GaAs buffer layer using MBE system has been achieved with a complete fill of nanoholes across the whole array. Furthermore, initial stages of *n*-GaN nanostubs grown on GaAs/Si(001), adopting Ga droplet

epitaxy and its subsequent nitridation method has shown the possibility in obtaining a single GaN nanostub in a hole with reasonable growth rate. Detailed electrical analysis on the performance of heterogeneous n+GaAs/p+Si vertical PN diodes with various contact metals as well as its GaAs nanostub height was performed and is given in the experimental section. Careful choice of metal contact is crucial in 55 nm-diameter GaAs nanostubs with its height of 120 nm. Furthermore, process flow of wide bandgap drain heterogeneous planar multiple-gate MOSFETs is well designed, highlighting the sidewall image transfer technique for narrow-fin formation.

6.2 Future Work

The study demonstrated the possibility of 'junction-level' integration of III-V materials such as GaAs and/or GaN with Si CMOS to implement in the state-of-the-art transistor architectures for low/high power analog/RF/mixed-signal SoC applications. Both detailed simulation and growth experimental studies have been performed and optimized to show the promise of future nanoscale transistors with III-V channel integrated into a single Si chip. However, there is still room for improvements in various aspects to realize an ultra-scaled 'junction-level' heterogeneous integration onto Si CMOS platform. Regarding theoretical/simulation analysis, MBE-based selective-area III-V growth on Si(001), and wide bandgap drain multiple-gate device fabrication, several suggestions which would be helpful in future research are listed as the following:

- **Comprehensive study of high voltage/power analog/RF/mixed-signal performances of the wide bandgap GaN drain heterogeneous III-V high mobility channel multiple-gate MOSFET**: Based on the previous simulation studies on III-V channel MOSFET and wide bandgap drain MOSFET in this

dissertation, a more thorough and complete set of metrics such as output power, power-added efficiency, insertion loss, isolation, linearity, etc. with the help of circuit-level and system-level simulations including the back-end-of-line (BEOL) would provide a more accurate picture of demonstration of merits of 'junction-level' heterogeneous integration of III-V materials with Si CMOS. Moreover, various applications such as high-frequency power amplifier (PA) and RF switches that are built utilizing the proposed transistor structure would aid further performance assessment.

- **Study of various growth parameters on zinc-blende GaN growth on Si(001) substrates:** Complete selective-area growth of initial stages of GaN nanostubs on Si(001) has been successfully demonstrated by utilizing a thin GaAs buffer layer underneath in this dissertation. However, there is still room for improvement in its film quality as well as defect density in the film. Since selective-area nanostub growth is very sensitive to its growth conditions, N plasma, V/III BEP ratio, growth rate as well as substrate temperature can further be systematically varied to study the effect of these parameters on the nanostub quality and defect formation mechanisms. Moreover, higher aspect-ratio SiO_2-mask patterns greater than 1.5 can be designed by a variety of lithography techniques to effectively suppress the propagation of planar defects towards the top surface. In addition, a detailed film characterization by transmission electron microscope (TEM), x-ray diffraction (XRD), and photoluminescence (PL) would be necessary in controlling a single-phase (i.e. zinc-blende) GaN grown on Si(001) substrates. Si surface treatment is also very important to achieve high quality GaN on Si with a complete selectivity,

and therefore, its further investigation would help improve its interface quality. Final current-voltage electrical characterization of GaN/Si(001) vertical PN diodes would be needed as well.

- **Fabrication of wide bandgap GaN drain heterogeneous multiple-gate MOSFET:** Process flow of the proposed device structure has been designed and given in this dissertation based on a detailed simulation study and successful demonstration of complete selective-area growth of dislocation-free single-crystalline GaAs/GaN nanostubs on Si(001). Schematics of this device process flow is illustrated in Figure 6.1. Several critical process steps need to be thoroughly investigated to realize the concept of 'junction-level' heterogeneous integration of GaN materials with Si. Owing to dislocation-free single-crystalline GaAs/GaN nanostubs on Si(001) implementing as drain, the proposed device would provide improvements in breakdown characteristics.

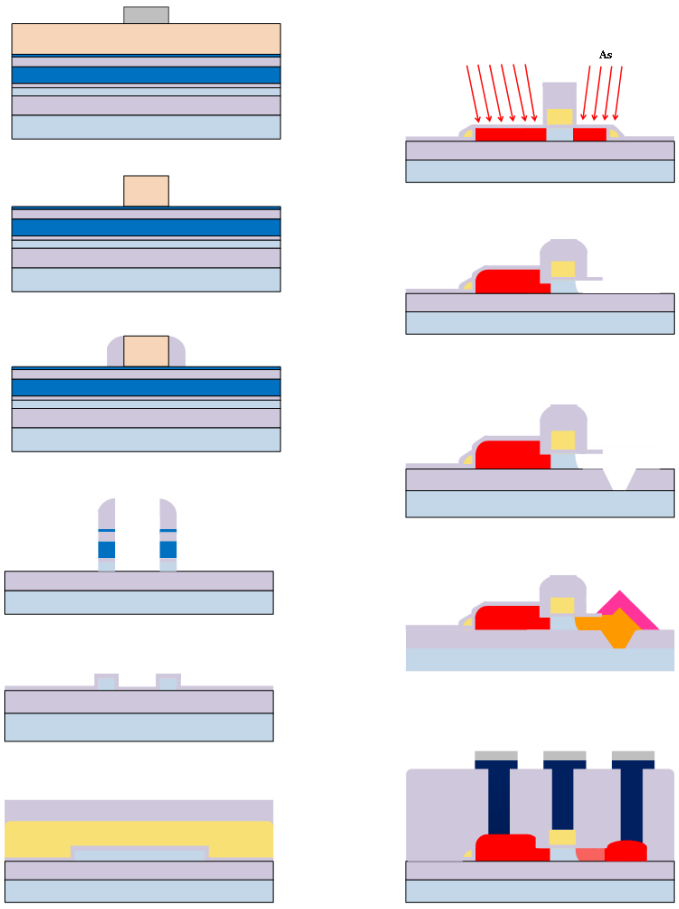

Fig 6.1 Schematic diagrams of a process flow of wide bandgap GaN drain heterogeneous multiple-gate MOSFET