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Material Science and Device Physics of Semiconductors on Arbitrary Substrates

By

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Committee in charge:

Professor Ali Javey, Chair
Professor Sayeef Salahuddin
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Material Science and Device Physics of Semiconductors on Arbitrary Substrates

Abstract
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Since the beginnings of the semiconductor revolution, device engineering and material development have been deeply interconnected. Innovations in one invariably spurred development in the other. One of the most important current challenges are developing techniques which enable deposition of materials on arbitrary substrates and the design constraints of devices fabricated via these techniques. This thesis focuses on furthering the materials development-device design cycle for three techniques: (i) epitaxial lift-off, (ii) nanowire growth via the vapor-liquid-solid growth mode, and (iii) the thin-film vapor-liquid-solid growth technique. The physics of devices made via (i) and (ii) are discussed in chapters two and three, the material science of (iii) is discussed in chapter four, and a method to engineer the physical and electronic properties of individual nanowires made via (ii) is discussed in chapter

Chapter two deals with the device physics and performance of ultra-thin compound semiconductor on insulator field effect transistors. Due to its excellent electron transport properties, InAs is used as the material of choice for the transistors, termed XOI FETs. These devices are fabricated utilizing an epitaxial layer transfer technique, enabling highly lattice mismatched single-crystalline layers of InAs to be deposited on Si wafers. Allowing devices which combine the excellent transport properties of compound-semiconductors and the established processing infrastructure for silicon. Chapter three discusses the design constraints and guidelines for nanopillar photovoltaics, specifically those fabricated utilizing the CdS/CdTe material system. Critically, the materials parameters that are favorable to non-planar cells are discussed, and the performance expectations for CdS/CdTe nanopillar photovoltaics are discussed.

Chapter four focuses on a growth technique developed to enable growth of ultra-large grain III-V semiconductors on non-epitaxial substrates, termed thin-film vapor-liquid-solid growth. This growth technique takes advantage of the vapor liquid solid growth mode to enable films with thickness down to 500 nm and grain sizes greater than 50 μm. This represents a significant advance over all conventional growth techniques, which produce films with grain sizes 10-100x smaller. Furthermore, the optoelectronic quality of these materials is within a few percent of single crystal, as determined by quantitative luminescence efficiency measurements. Finally, Chapter five discusses the use of nanowires as physical templates, allowing engineering of Van der Waals forces to fabricate self-selective electrical connectors. By utilizing nanowire forests as starting templates, successive layers of material are deposited, each playing a specific role in the final structure, enabling composite material properties otherwise not possible.

To

my family

my friends

my mentors

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Acknowledgements

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I would also like to thank all the excellent post-doctoral scholars with whom I've had the opportunity to work, a majority of who are now professors. I have to especially thank Professor Zhiyong Fan, Professor Hyunhyub Ko, Professor Yu-Lun Chueh, Professor Johnny Ho, Professor Morten Madsen, Professor Junghyo Nah, Professor Paul Leu, and Prof. Min Hyung Lee. I learned a great deal while working of each of these excellent researchers. Additionally, I would like to thank Dr. Zhibin Yu, Dr. Corsin Battaglia, Dr. Daisuke Kiriya, Dr. Yuping Zheng, and Dr. Yongjing Lin, especially Dr. Yu whom I worked very closely with for my last year. Moreover, I'm lucky to have been surrounded by an excellent group of graduate researchers, all of whom made graduate school a more enjoyable experience. I would especially like to thank Maxwell Zheng, Daniel Ruebusch, Toshitake Takahashi, Hui Fang, and Steven Chuang. I've also had the opportunity to work with and mentor many excellent undergraduates over the past years, particularly: Rebecca Lee, Johnathan Lin Ern Sheong, Alex Fung, and Rebeca Park.

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1

Introduction

1.1 Device Scaling and Materials Development

From the humble beginnings of the Au/Ge schottky barrier FET, the revolution in information technology has built upon a foundation of materials driven device innovation. In this paradigm, milestones in material development enable previously unrealizable device structures, and device innovation imposes greater demands on materials development. This symbiotic relationship between materials development and device innovation has seen the individual transistor shrink from macro-scale down to the 22 nm gate length state-of-the-art transistors available today. Furthermore, this march towards progressively smaller devices has driven advancements in nearly every aspect of semiconductor materials growth and device fabrication, including (i) homo- and hetero-epitaxy, (ii) single-crystal wafer growth, (iii) semiconductor doping technologies, (iv) lithography, (v) etching, and (vi) thin-film deposition. However, despite the tremendous advances over a wide range of areas, the growth of high-quality semiconductors on non-lattice matched substrates is still a key challenge, severely limiting the material systems and geometries available to device designers.

In this thesis, multiple methods which overcome this limitation are explored. First, the use of epitaxial lift off is explored for the fabrication of high performance III-V FETs on Si; next, the materials constraints and device design of II-VI nanopillar solar cells are studied; and finally, a method for growing high-quality compound semiconductor layers on non-epitaxial substrates is presented.

1.2 Epitaxial Lift-off as a route towards III-V field effect transistors on Si

The key driver for MOSFET scaling is the improved performance of heavily scaled logic gates. Device scaling, in general, enables higher device densities, increased clock frequency, and reduced per device switching energy, enabling the exponential increase in performance that is often termed Moore's Law. One of the most important consequences of device scaling is that the supply voltage of a logic gate may be reduced. Recently, however, the supply voltage has effectively bottomed out for Si, as further voltage scaling would cause a tradeoff between untenable off-state leakage or a reduction in processor speed, both undesirable. Consequently, further increases in transistor density would cause unreasonable increases in power density, rendering us unable to effectively keep the processor operating temperatures within tolerance.

Due to their excellent electron and hole transport properties, compound semiconductors, specifically III-V's, have garnered significant interest as a Si replacement. Using channel materials with improved mobility and saturation velocity would likely enable further supply voltage scaling by removing the leakage-speed tradeoff currently faced by Si logic gates. Thus, III-V MOSFETs and high electron mobility transistors (HEMT) have been extensively explored. However, while the excellent materials properties make III-V's an ideal candidate for a Si replacement, the methods for direct growth of III-V layers and the following transistor processing would require special equipment, thus preventing the exploitation of the extensive Si processing infrastructure. Thus, it is highly desirable to have III-V's layers directly on a Si substrate, combining the benefits of III-V FETs with the ease of Si processing.

It is well known that the higher the quality of thin film desired, the more complex the growth process required to grow it. The highest quality III-V's are achieved via epitaxial growth of these layer via metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) on lattice matched substrates, a process termed homo-epitaxy. Due to the large lattice constant mismatch between Si and III-V's, any attempts to directly grow these materials on Si would result in defective, low-quality layers, and, consequently, low-performance devices. Thus to enable high-quality single crystalline layers on Si, the layers must first be grown on a lattice-matched substrate and then transferred to Si substrate utilizing a process known as epitaxial lift-off.

Since its introduction, epitaxial lift-off has played a key role in the fabrication of high quality III-V devices on arbitrary substrates. Specifically, this technique consists of (i) the growth of a high-quality single crystal layer on a lattice-matched substrate, followed by (ii) an undercut etch to release the layer, and finally (iii) the transfer of this layer to the substrate of choice. The high-quality crystalline layer on the arbitrary substrate can then be processed in whatever fashion is desired, enabling various solid-state devices such as: photovoltaic devices, light emitting diodes, and transistors.

The key requirements for successful use of this procedure are: a lattice matched growth substrate and/or a sacrificial layer on which to grow the desired crystalline layer, a high etch

selectivity between the desired layer and sacrificial layer or substrate, and a stable medium to allow transfer of the released layer. This method was first reported by Konagi et al, and popularized by Yablonovitch et. al. utilizing the GaAs/AlGaAs material system, selected due to the extremely high etch selectivity of HF between the GaAs and AlGaAs. In these systems, the layers of interest were on the order of microns in thickness and were continuous films.

In this thesis, the material of choice is InAs, not GaAs, with thicknesses between 5 nm and 50 nm, and instead of utilizing film geometries, nanoribbon (300 nm width x 10-100 μm length) are used. This material geometry provides multiple advantages: first, the use of ultra-thin ribbons enables control over the bandgap via quantum confinement as well as superior gate-control due to the thin body; and second, the use of ribbons mitigates any issues with distance dependent undercut etch rates, facilitating transfer from the growth substrate to the Si handle wafer. Further details of the process are given in chapter two.

1.3 Vapor-Liquid-Solid Nanowire growth as a route towards three-dimensional photovoltaics on metal foils

While epitaxial lift-off is an excellent method for fabrication of high-performance III-V transistors on Si, the process is limited to semiconductors with lattice matched substrates, appropriate sacrificial layers and planar geometries. If high-quality single crystalline materials in non-planar geometries on non-epitaxial substrates are desired, vapor-liquid-solid (VLS) growth of nanowires (NW) provides an excellent route towards fabrication.

Specifically, VLS NW growth involves preferential precipitation from a liquid catalyst drop over the vapor phase environment. Thus this process requires a catalyst, such as Au, Ni, Fe, etc and a precursor gas, e.g. Si, Ge, etc. The catalyst is exposed to a precursor gas at high temperatures, causing absorption of the gas into the precursor until saturation occurs. Once the catalyst is saturated, precipitation of a crystalline solid occurs, enabling growth of NWs. Since the crystalline material precipitates solely from the liquid droplet, the cross-sectional shape of the NW often takes that of the liquid. The reason for the wire geometry is simply due to the liquid remaining attached to the end of the precipitating solid and continuously absorbing the gaseous precursor atoms and precipitating the crystalline solid.

Since the liquid defines the location of the solid, templating the liquid enables complete control over the location of the crystalline solid. We have shown that not only can templated NW growth enable control over the shape of the nanowire, but can also be utilized to grow single crystalline wires which have multiple diameters. Thus this is a promising method to fabricate non-planar photovoltaics.

A distinct advantage of non-planar PV, particularly those fabricated from NWs, over traditional planar PV is the orthogonalization of light absorption and minority carrier collection directions. By decoupling the absorption and collection, it is possible to design a cell with thickness large enough to absorb all of the incident light and then separately tune the inter-NW spacing to optimize the carrier collection even with materials which have poor minority carrier lifetimes.

In chapter 3, design constraints of this growth method as applied to nanopillar (NPL) photovoltaics are explored. In particular, the materials properties that make the NPL geometry beneficial over the planar geometry are discussed. Then the CdTe/CdS material system is explored in detail, discussing how the cells may be engineered for optimal properties given certain materials properties. Finally, the expected performance limits for NPL cells are given, based on published materials properties.

1.4 Thin-film vapor-liquid-solid growth as a route towards high-performance, scalable III-V photovoltaics

Epitaxial lift-off and VLS growth are both key technologies that enable us to work around the growth complexity-material quality trade-off, without directly addressing this challenge. The thin-film vapor-liquid-solid (TF-VLS) growth method overcomes this trade-off. Before delving into the details of the method, a brief description of why the trade-off exists will be given.

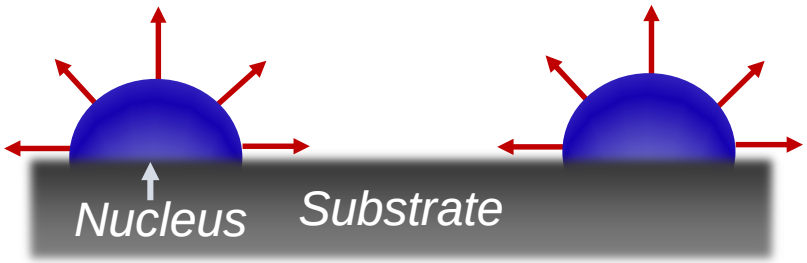

Figure 1: Nucleation and growth in the vapor-solid growth mode. The arrows represent growth velocities in the various directions, illustrating isotropic growth. This sets the

It should be noted that almost all conventional thin film growth techniques (e.g. MOCVD, MBE, & CVD) used for semiconductors utilize the vapor solid growth mode. Specifically, the desired material is heterogeneously precipitated onto the desired substrate from a supersaturated vapor. The gas phase growth precursors vary from atoms of the desired semiconductor, to molecules (e.g. SiH_4 or GeH_4), or metalorganic precursors. If non-epitaxial substrates are used for growth, then the growth will proceed as illustrated in Figure 1, with each nuclei, represented by the blue hemispheres, having disparate crystal orientations. Since the lateral grain size is generally set by the nucleation density, if larger grain size films are desired, then the nucleation densities must be reduced. However, for the majority of material systems, the growth is near isotropic. Thus, if the nuclei spacing is t, the film thickness will need to be at a minimum, t/2 to ensure a continuous film. This sets the rule of thumb for polycrystalline growth today: for a continuous film, the lateral grain size will be roughly the same as the film thickness, if not smaller.

In order to work around this limitation, the thin-film vapor-liquid-solid growth technique has been developed. This method enables growth of thin films on non-epitaxial substrates without the limitation of vapor-solid growth techniques. In chapter 4, thin films with thicknesses between 500 nm – 3 μm are grown. These films have grain sizes of >50 microns, excellent mobilities of up to 500 cm^2/V-s and excellent optical properties, near that of single crystalline InP with similar doping concentrations.

1.5 Nanowire Connectors

Conventional self-selective connectors generally use lock-and-key mechanisms that are provide physical binding forces, specificity to a specific connector, and durability. For nearly all macro-scale applications, these lock-and-key mechanisms, such as Velcro or electrical plug/sockets, are highly effective. However, when scaling these connectors below the millimeter regime, nearly all connector technologies lose effectiveness, as the physical binding mechanisms, such as those for Velcro or electrical plugs, are not practically implementable. Thus, utilization of chemical binding forces such as Van der Waals represents an opportunity to create connectors that may be scaled to the mm regime or below. However, in order to utilize this binding mechanism and generate sufficient adhesion force, there must be an amplification of contact area. This can be easily done by engineering a composite nanowire. Here, this is done by first growing inorganic Ge nanowires, and then depositing conformal coatings of parylene and Ag to fabricate self-selective electrical connectors which may be scaled down below the mm regime.

2

Novel Channel Materials for Next Generation Transistors

2.1 Introduction

Steady scaling of transistors, from 1970 till today, has been a key driver for technological development in the area of computation and telecommunications. These efforts have seen an increase in number of transistors on one die from ~10^3 to ~10^9 over a 40 year time period. However, this massive increase in transistor count, and corresponding computing power, has come at the price of a steep increase in the power per CPU, from just over 1 W to over 100 W. Thus, there have been significant efforts to find materials and structures that would enable continued scaling with lower power consumption. Structurally, the efforts have focused on the FINFET and Ultra-thin body FETs, as these structures show the least short channel effects as the transistors are scaled. Material-wise, the III-V semiconductor family has been of primary interests for replacing silicon specifically due to their high electron and hole mobilities.

2.2 Ultrathin compound semiconductor on insulator layers for high performance nanoscale transistors

Over the past several years, the inherent scaling limitations of electron devices have fueled the exploration of high carrier mobility semiconductors as a Si replacement to further enhance the device performance[1,2,3,4,5,6,7,8]. In particular, compound semiconductors heterogeneously integrated on Si substrates have been actively studied[7,9,10], combining the high mobility of III-V semiconductors and the well-established, low cost processing of Si technology. This integration, however, presents significant challenges. Conventionally, heteroepitaxial growth of complex multilayers on Si has been explored[9,11,12,13]. Besides complexity, high defect densities and junction leakage currents present limitations in the approach. Due to the high leakage current, a quantum well architecture is the presently the dominant approach for fabrication of FETs utilizing III-V channel materials. Here, we present a novel route towards the fabrication of III-V channel FETs utilizing an epitaxial transfer method for the integration of ultrathin layers of single-crystalline InAs on Si/SiO_2 substrates. As a parallel to silicon-on-insulator (SOI)

technology[14], we use the abbreviation "XOI" to represent our compound semiconductor-on-insulator platform. Through experiments and simulation, the electrical properties of InAs XOI transistors are explored, elucidating the critical role of quantum confinement in the transport properties of ultrathin XOI layers. Importantly, a high quality InAs/dielectric interface is obtained by the use of a novel thermally grown interfacial $InAsO_x$ layer (~1 nm thick). The fabricated FETs exhibit an impressive peak transconductance of ~1.6 mS/μm at V_{DS}=0.5V with ON/OFF current ratio of greater than 10,000 and a subthreshold swing of 107-150 mV/decade for a channel length of ~0.5 μm.

Epitaxial lift-off and transfer of crystalline microstructures to various support substrates has been shown to be a versatile technique for applications ranging from optoelectronics to large-area electronics[15,16,17,18]. Specifically, high performance, mechanically flexible macro-electronics and photovoltaics have been demonstrated on plastics, rubbers, and glass substrates by this method[19,20,21]. Here, we use a modified epitaxial transfer scheme for integrating *ultrathin* InAs layers with *nanometer-scale* thicknesses on Si/SiO_2 substrates for use as high performance nanoscale transistors. The nanoscale thick InAs layers are fully depleted which is an important criteria for achieving high performance FETs with respectable OFF currents based on small band gap semiconductors. The transfer is achieved without the use of adhesive layers, thereby allowing for purely inorganic interfaces with low interface trap densities and high stability. The process schematic for the fabrication of InAs XOI substrates is shown in Figure 1a (see Methods for the details).

Atomic force microscopy (AFM) was utilized to characterize the surface morphology and uniformity of the fabricated XOI substrates. Figures 1b-c show representative AFM images of an array of InAs NRs (~18 nm thick) on a Si/SiO_2 substrate, clearly depicting the smooth surfaces (< 1 nm surface roughness) and high uniformity of the enabled structures over large areas. Uniquely, the process readily enables the heterogeneous integration of different III-V materials and structures on a single substrate through a multi-step epitaxial transfer process. To demonstrate this capability, a two-step transfer process was utilized to form ordered arrays of 18 and 48 nm thick InAs NRs that are perpendicularly oriented on the surface of a Si/SiO_2 substrate (Figs. 1d-e). This result demonstrates the potential ability of the proposed XOI technology for generic heterogeneous and/or hierarchical assembly of crystalline semiconducting materials. In the future, a similar scheme may be utilized to enable the fabrication of both *p*- and *n*- type transistors on the same chip for complementary electronics based on the optimal III-V semiconductors.

To shed light on the atomic structure of the interfaces, cross-sectional transmission electron microscopy (TEM) images of an InAs XOI device were taken and are shown in Figure 2. The high-resolution TEM (HRTEM) image (Fig. 2c) illustrates the single-crystalline structure of InAs NRs (~13 nm thick) with atomically abrupt interfaces with the SiO_2 and ZrO_2 layers. The TEM image of the $InAs/SiO_2$ interface does not exhibit visible voids (Fig. 2c), although only a small fraction of the interface is examined by TEM. As described in more depth later in this paper, InAs NRs were thermally oxidized prior to the top-gate stack deposition to drastically lower the interfacial trap densities. The thermally grown $InAsO_x$ layer is clearly evident in the HRTEM image (Fig. 2c) with a thickness of ~1 nm.

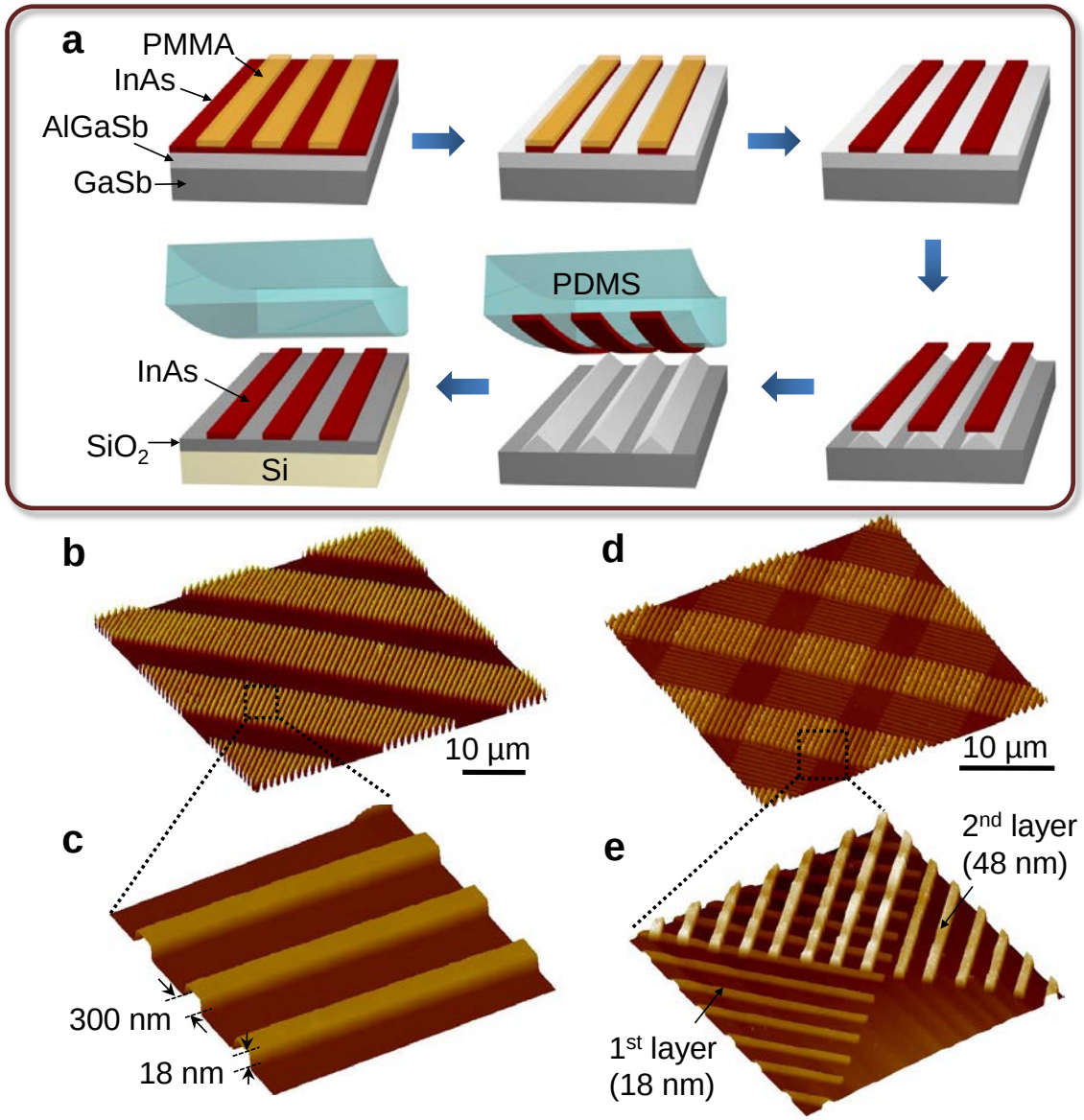

Figure 1: Ultrathin InAs XOI fabrication scheme and AFM images. a, Schematic procedure for the assembly of InAs XOI substrates by an epitaxial transfer process. The epitaxially grown, single-crystalline InAs films are patterned with PMMA and wet etched into NR arrays. A subsequent selective wet etch of the underlying AlGaSb layer and the transfer of NRs by using an elastomeric PDMS slab result in the formation of InAs NR arrays on Si/SiO_2 substrates. **b-c,** AFM images of InAs NR arrays on a Si/SiO_2 substrate. The NRs have a length of ~10 µm, height of 20 nm and width of ~300 nm. **d-e**, AFM images of InAs NR superstructures on a Si/SiO_2 substrate, consisting of two layers of perpendicularly oriented NR arrays with 18 and 48 nm thicknesses as assembled by a two-step epitaxial transfer process.

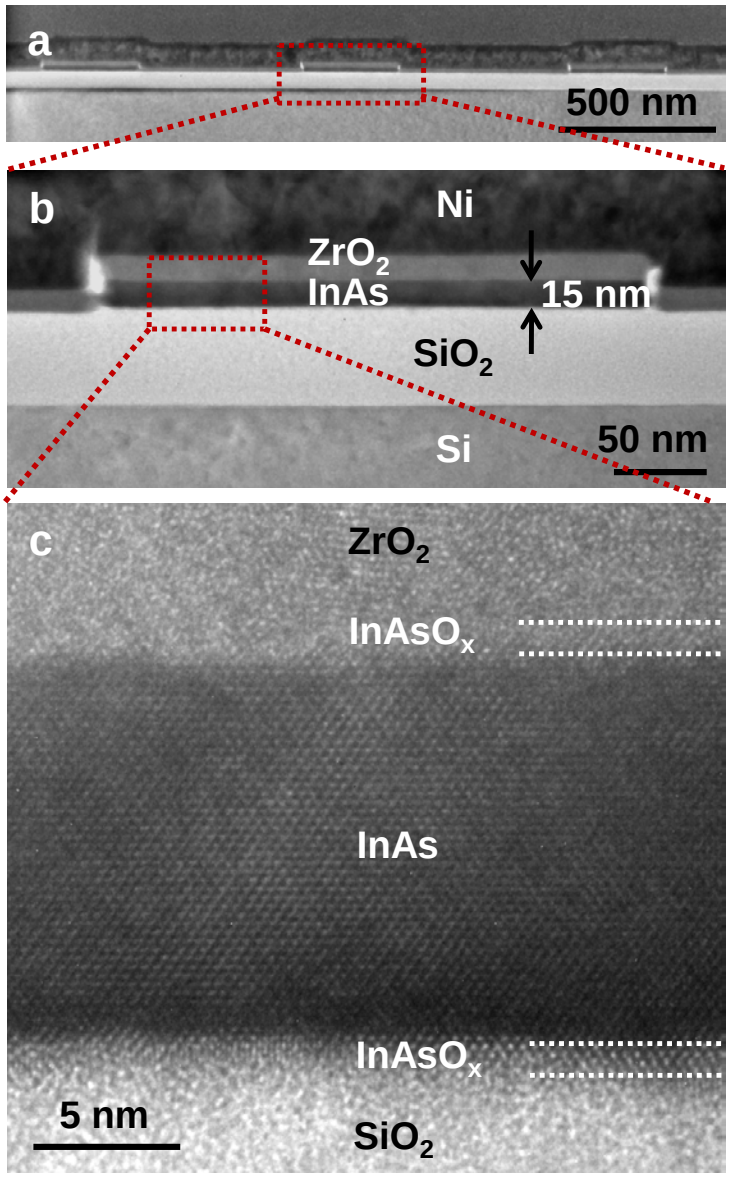

Figure 2: Cross-sectional TEM analysis of InAs XOI substrates. a, A TEM image of an array of three InAs NRs on a Si/SiO_2 substrate. **b**, A magnified TEM image of an individual ~13 nm thick InAs NR on a Si/SiO_2 (~50 nm thick) substrate. The NR is coated with a ZrO_2 /Ni bilayer (~15 and ~50 nm, respectively) which acts as a top-gate stack for the subsequently fabricated FETs. **c**, A HRTEM image showing the single-crystalline structure of an InAs NR with abrupt atomic interfaces with ZrO_2 and SiO_2 layers on the top and bottom surfaces, respectively. A ~1 nm thick $InAsO_x$ interfacial layer formed by thermal oxidation and used for surface passivation is clearly evident.

Long-channel, back-gated field-effect transistors (FETs) based on individual NRs were fabricated in order to elucidate the intrinsic electron transport properties of InAs NRs as a function of thickness. The process scheme involved the fabrication of XOI substrates with the desired InAs thickness followed by the formation of source/drain (S/D) metal contacts by lithography and lift-off (~50 nm thick Ni). The p^+ Si support substrate was used as the global back-gate with a 50 nm thermal SiO_2 as the gate dielectric. Ni contacts were annealed at 225ºC for 5 min in a N_2 ambient to enable the formation of low resistance contacts to the conduction band of InAs (Fig. S6) [22]. The transfer characteristics at V_{DS}=0.1V of the back-gated XOI FETs with a channel length, L~5 μm and InAs thicknesses of 8-48 nm are shown in Figure 3a. Two trends are clearly evident from the measurements. First, the OFF current monotonically increases with increasing thickness due to the reduced electrostatic gate coupling of the back-gate. Second, the ON current increases with InAs thickness due to the thickness dependency of electron mobility, μ_n. Since L~ 5μm, the devices are effectively operating in the diffusive regime, thereby, enabling the direct extraction of the field-effect mobility by using the relation $\mu_{n,FE} = (g_m)(L^2/C_{ox}V_{DS})$, where $g_m = dI_{DS}/dV_{GS}\big|_{V_{DS}}$ is the transconductance and C_{ox} is the gate oxide capacitance (Fig. S5). For this analysis, parasitic resistances were ignored since Ni forms near ohmic metal contacts[22]. The gate oxide capacitance was estimated from the parallel plate capacitor model $C_{ox} = (\varepsilon A)/d$, where ε=3.9 and d=50 nm are the dielectric constant and thickness of SiO_2, respectively. The effect of quantum capacitance, C_Q was neglected due to the relatively thick gate dielectrics used in this study (*i.e.*, C_{ox}<<C_Q). Figure 3b shows the peak $\mu_{n,FE}$ as a function of InAs thickness, T_{InAs}. The mobility at first linearly increases with thickness for T_{InAs} < ~18 nm with a slope of ~221 (cm^2/Vs)/nm, beyond which it nearly saturates at $\mu_{n,FE}$ ~5,500 cm^2/Vs. The measured XOI field-effect mobility is close to the reported Hall mobilities for InGaAs (~10,000 cm^2/Vs)[10] and InAs (13,200 cm^2/Vs)[23] quantum well (QW) structures. It should be noted that the Hall mobility is typically higher than the field-effect mobility for any given material as a number of device and surface state contributions to carrier transport are not accounted in the Hall effect measurements.

To shed light on the observed mobility trend, the low-field phonon mobility, $\mu_{n,phonon}$ was calculated as $\mu_{n,phonon} = e/(m^*\langle 1/\tau \rangle)$, where e is the electronic charge and m^* is the effective mass (see Supp. Info.). Average scattering rate $\langle 1/\tau \rangle$ is calculated from

$$\left\langle \frac{1}{\tau} \right\rangle = \frac{\int \frac{1}{\tau(E)} \frac{\partial f_0}{\partial E} dE}{\int \frac{\partial f_0}{\partial E} dE}$$

where f_0 is the equilibrium Fermi-Dirac distribution function. $\tau(E)$ was calculated using Fermi's golden rule, with the matrix elements of the scattering potentials evaluated in the basis of the NR eigenfunctions. Both acoustic and optical (including polar) phonon scattering events were considered[24]. The calculated $\mu_{n,phonon}$ vs. T_{InAs} is shown in Fig. 3b. For small thicknesses, the mobility linearly increases with the thickness. This behavior is attributed to the gradual transition of the channel from a 2D to 3D system as the NR thickness is increased, with more transport modes (i.e., sub-bands) contributing to the current flow. As the thickness surpasses the Bohr radius of bulk InAs (~34 nm), the electronic structure of NRs approaches the 3D regime, resulting in a mobility saturation for T_{InAs}>~35 nm to the well-known bulk value of InAs (~40,000 cm^2/Vs)[25]. While the onset thickness of saturation closely matches the experiments, there is 5-10× discrepancy in the actual mobility values. This is expected since the extracted data represents the

field-effect mobility, consisting of phonon scattering along with other device contributions, including interface trap states, surface roughness scattering, and vertical-field-induced mobility degradation. Both surface roughness and vertical-field (i.e., gate field) induce additional carrier scattering events at the surface/interface, while the primary effect of interface trap states is to deteriorate the modulating the channel conductance (i.e., charge density) by the gate-field. These effects degrade the extracted g_m and thereby $\mu_{n,FE}$. To simulate $\mu_{n,FE}$, a full device simulation was performed (see Supp. Info.). An interface trap density, $D_{it}= 6\times10^{12}$ states $cm^{-2}eV^{-1}$ was used as the fitting parameter. The simulated I-V characteristics of XOI back-gated FETs are shown in Figure 3a. Clearly, the simulated I-V curves match the experimental data closely for all InAs thicknesses, especially in the ON-state. Next, peak $\mu_{n,FE}$ was extracted from simulation and plotted as a function of T_{InAs} (Fig. 3b), once again closely matching the experimental $\mu_{n,FE}$. The close matching of the experimental and simulated results demonstrate the effectiveness of the XOI platform as a clean and predictable material system for exploring high performance devices while highlighting the critical role of quantum confinement and surface contributions on the transport properties of InAs, even at relatively large thicknesses. It should be noted that since the ribbon width used in this work is 10~30 times larger than the thickness, there is minimal dependence of the device performance on the NR width (Fig. S13), thereby, the structures can be effectively treated as thin films.

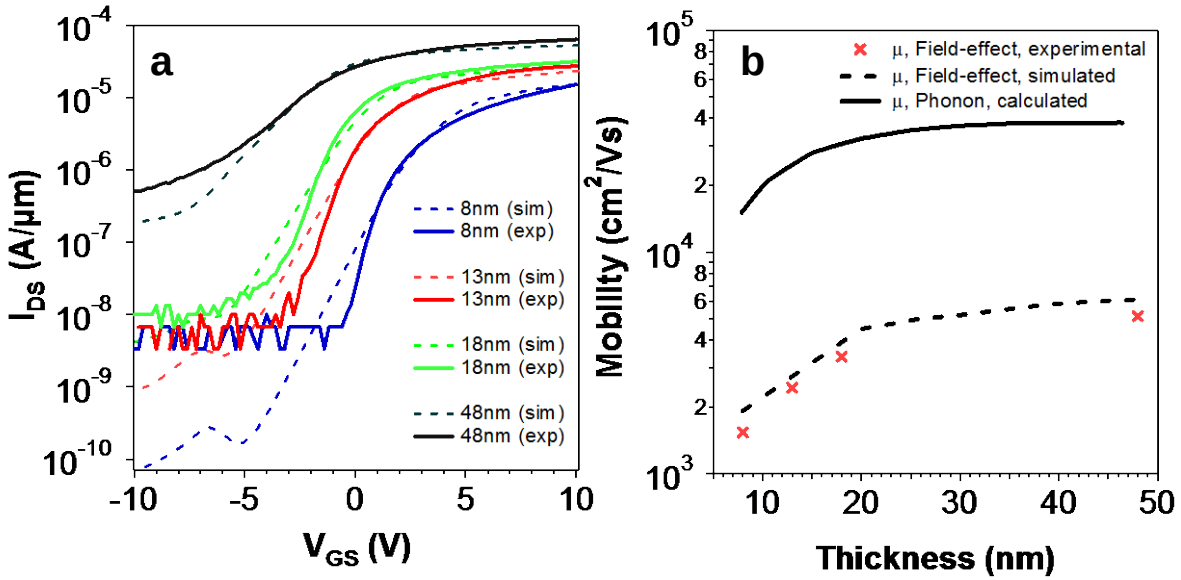

Figure 3: Back-gated, long-channel InAs XOI FETs. a, The experimental (solid lines) and simulated (dashed lines) I_{DS}-V_{GS} characteristics of back-gated (50 nm SiO_2 gate dielectric) XOI FETs at V_{DS}=0.1V with L~5 μm for different InAs NR thicknesses (8, 13, 18, 48 nm). Each FET consists of a single NR. **b**, The experimental and simulated peak field-effect electron mobilities of InAs NRs as a function of NR thickness. The calculated phonon mobility is also shown.

In order to explore the performance limits of InAs XOI devices, top-gated FETs with high-κ gate dielectrics and L~0.5 µm were fabricated. Briefly, Ni S/D contacts were lithographically patterned on InAs NRs followed by the atomic layer deposition of ~8 nm thick ZrO_2 (ε ~ 20) as the gate dielectric. A local top-gate (Ni, 50 nm thick), underlapping the S/D electrodes by ~100 nm was then lithographically patterned. Importantly, thermal oxidation of InAs was found to significantly improve the interfacial properties and FET characteristics (Fig. S8). In this regard, prior to the S/D contact formation, the XOI substrates were first treated with 3% NH_4OH to remove the native oxide followed by the thermal oxidation at 350ºC for 1 min to form ~1 nm thick $InAsO_x$ layer as observed from TEM analysis (Fig. 2c). Figure 4a shows a typical I_{DS}-V_{GS} characteristic of a top-gated FET, consisting of an individual ~18 nm thick InAs NR with a width of ~320 nm. The XOI FET exhibits a respectable I_{ON}/I_{OFF}~10^4, a subthreshold swing of SS=dV_{GS}/d(logI_{DS}) ~ 150 mV/decade (Fig. 4b), and a peak g_m ~ 1.6 mS/µm at V_{DS}=0.5V (Fig. S9). The lowest measured SS for our XOI FETs is ~107 mV/decade (Fig. S10) as compared to InAs and InGaAs QW-FETs in literature which have exhibited SS ~ 70 and 75 mV/dec, respectively [10,23]. The devices reported here use a relatively thick gate dielectric which can be scaled down in the future to further improve the gate electrostatic control and the SS characteristics. The single NR transistor output characteristic is shown in Fig. 4b, delivering an impressive I_{ON}~1.4 mA/µm at an operating voltage, V_{DD}=V_{DS}=V_{GS}=1V. To further analyze the performance, a full device simulation was performed. A close match of the experimental data is obtained with D_{it}=10^{11} states $cm^{-2}eV^{-1}$ used as the fitting parameter (see Supp. Info., Fig. S7), which is a ~60× improvement over devices without any surface treatment (i.e., with a native oxide layer). The fitted D_{it} values represent only estimation. Note that while C-V measurement is conventionally utilized for D_{it} extraction in Si devices, doing so is rather challenging and prone to a large uncertainty for narrow bandgap semiconductors, such as InAs[26]. In the future, the development of more accurate techniques for D_{it} measurement in InAs XOI devices is needed. The explored thermal oxidation process for surface passivation is counter-intuitive as the previous works have focused on the removal of surface oxides[7]. We speculate that unlike the native oxide layer, thermal oxidation results in the formation of a dense oxide with minimal dangling bonds. Similar to the thermally grown SiO_2, the thermal oxide of InAs provides an ideal and simple surface passivation layer, addressing one of the important challenges in InAs devices.

In conclusion, a new technology platform and device concept for the integration of ultrathin layers of III-V semiconductors directly on Si substrates is demonstrated, enabling excellent electronic device performances. While in this work we focus on InAs as the active channel material, in the future, other compound semiconductors could be explored using a similar scheme. In the future, research on the scalability of the process for 8" and 12" wafer processing is needed. We envision that wafer bonding of Si/SiO_2 and III-V wafers followed by the etch release of the sacrificial layer may be utilized to enable a manufacturable process scheme for ultrathin XOI devices.

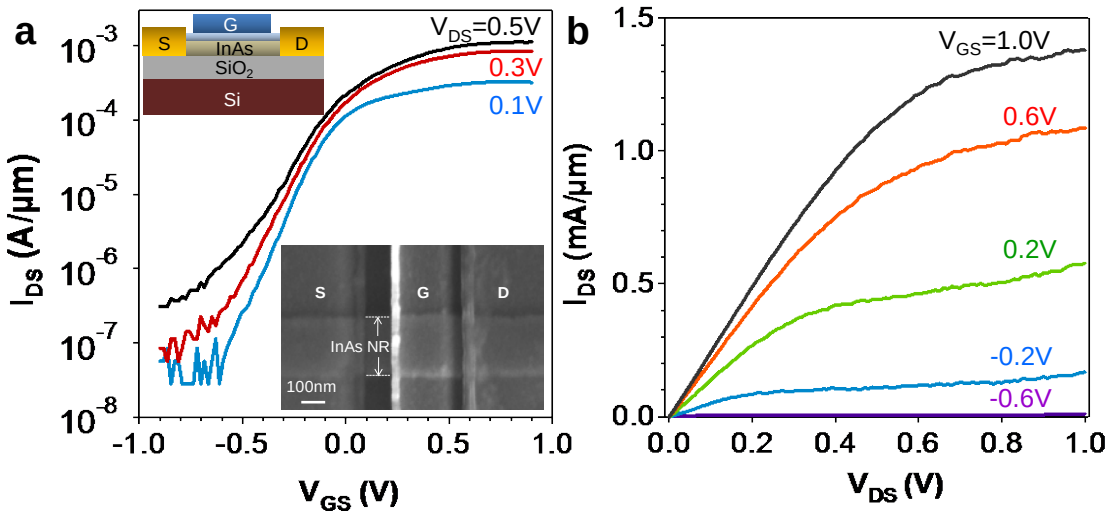

Figure 4: Top-gated InAs XOI FETs. a, Transfer characteristics of a top-gated InAs XOI FET, consisting of an individual NR (~18 nm thick) with *L*~0.5 μm and 8 nm thick ZrO_2 gate dielectric. A device schematic (top) and a representative SEM image (bottom) of a top-gated FET are shown in the inset. **b**, Output characteristics of the same device shown in (**a**). NRs were thermally oxidized at 350ºC for 1 min to form ~1 nm thick interfacial InAsOx layer for surface passivation of InAs.

2.3 Experimental and Theoretical Details

2.3.1 Methods summary

Single-crystalline InAs thin films (10-100 nm thick) were grown epitaxially on a 60 nm thick $Al_{0.2}Ga_{0.8}Sb$ layer on bulk GaSb substrates (see Supp. Info., Fig. S1). Polymethylmethacrylate (PMMA) patterns with a pitch and line-width of ~840 nm and ~350 nm, respectively, were lithographically patterned on the surface of the source substrate. The InAs layer was then pattern etched into nanoribbons (NRs) by using a mixture of citric acid (1 g/ml of water) and hydrogen peroxide (30%) at 1:20 volume ratio, which was chosen for its high selectivity and low resulting InAs edge roughness[27]. To release the InAs NRs from the source substrate, the AlGaSb layer was selectively etched by ammonium hydroxide (3%, in water) solution for 110 min[28]. Note that the selective etching of the AlGaSb layer was high enough not to affect the nanoscale structure of the InAs NRs (see Supp. Info., Fig. S2). Next, an elastomeric polydimethylsiloxane (PDMS) substrate (~2 mm thick) was used to detach the partially released InAs NRs from the GaSb donor substrates and transfer them onto Si/SiO_2 (50 nm, thermally grown) receiver substrates by a stamping process (Fig. S3-S4) [29]. Notably, in this process scheme, the initial epitaxial growth process is used to control the thickness of the transferred InAs NRs, while the lithographically defined PMMA etch mask is used to tune the length and width.

2.3.2 Preparation of the $GaSb/Al_{0.2}Ga_{0.8}Sb/InAs$ source wafers used for the epitaxial transfer process

The source layers were grown in a solid source VG-80 molecular beam epitaxy (MBE) reactor on n-type (Te-doped, 5×10^{17} cm^{-3}) epi-ready GaSb (001) double-side polished substrates using As_2 and Sb_2 valved cracker sources. Indium and gallium growth rates were determined by monitoring the intensity oscillations in the reflected high-energy electron diffraction (RHEED) patterns and set to 0.35 ML/s for Ga, 0.30 ML/s for In and 0.43 ML/s for AlGaSb. Group-V fluxes were adjusted using a conventional ion gauge to satisfy a group V/III beam equivalent pressure (BEP) flux ratio equal to 3.6 for GaSb and 9 for InAs. Initially, the substrate was outgassed under a vacuum, and then the surface oxide was removed at high temperature (535 ºC) under an Sb flux. The GaSb and $Al_{0.2}Ga_{0.8}Sb$ layers of the structure were grown at 490 ºC whereas the InAs layer was grown at 410 ºC. Cross-sectional TEM images of an as-grown source sample is shown Figure S1.

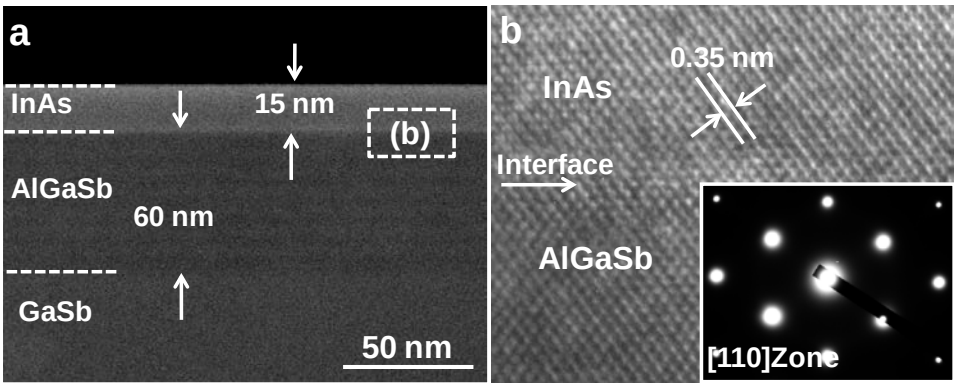

Figure S1. TEM analysis of the source substrate. a, The cross-sectional TEM image of a GaSb/AlGaSb/InAs source substrate, showing the InAs thin film (15 nm thick) grown epitaxially on a ~60 nm thick $Al_{0.2}Ga_{0.8}Sb$ layer on a bulk GaSb wafer. **b,** High-resolution TEM showing the single-crystalline structure of the InAs thin film on AlGaSb. The corresponding diffraction pattern is shown in the inset, indicating the [110] zone.

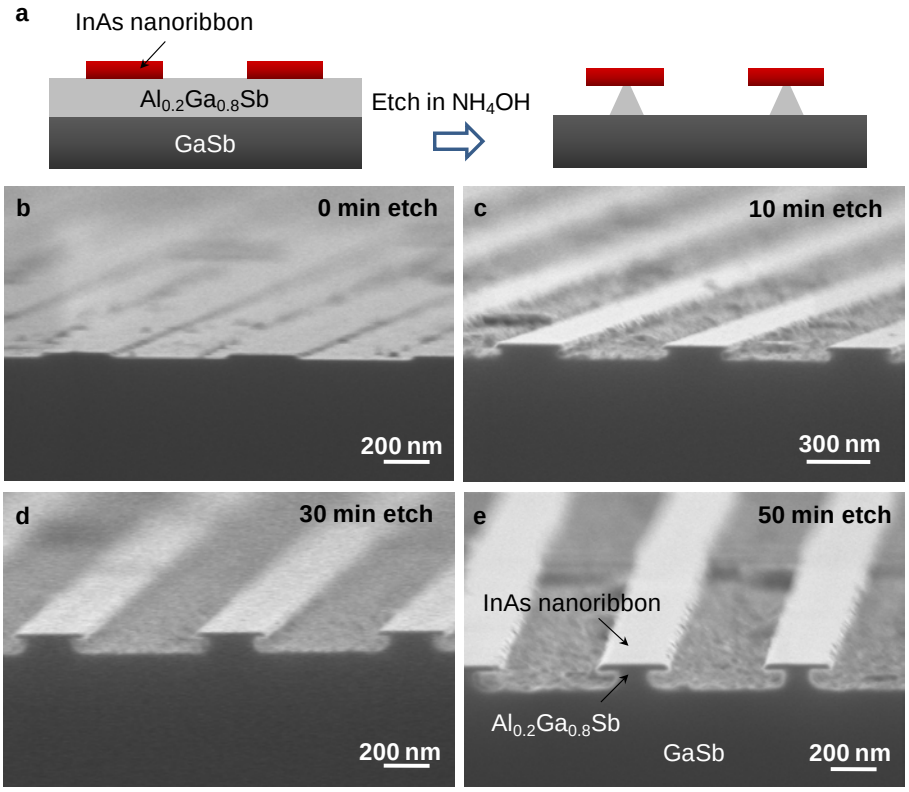

Figure S2. Selective wet etching of the AlGaSb sacrificial layer. a, Schematic illustration of the selective etching of AlGaSb. **b-f**, Scanning electron microscopy (SEM) images of InAs NRs on the source substrate after the wet etching of the AlGaSb layer for 0, 10, 30, 50 mins, respectively.

2.3.3 Selective wet etching of the AlGaSb sacrificial layer during the epitaxial transfer process

To release the InAs NRs from the source substrate after the etching of InAs film into NRs, the underlying $Al_{0.2}Ga_{0.8}Sb$ layer was selectively etched. Here, we used ammonium hydroxide (3%, in water) solution for the selective wet etching of the $Al_{0.2}Ga_{0.8}Sb$ layer. Figure S2 shows the SEM images of InAs NRs on the source substrate after different NH_4OH etching times (0, 10, 30, 50 mins), clearly demonstrating the highly selective etching of the AlGaSb sacrificial layer.

Following the partial etch of the AlGaSb layer in ammonium hydroxide (3%, in water) solution for 110 min (for 350 nm wide NRs), an elastomeric polydimethylsiloxane (PDMS) substrate (~2 mm thick) was brought in contact with the source wafer. The PDMS stamp was used to detach the partially released InAs NRs from the source substrate followed by their transfer onto Si/SiO_2 (50 nm, thermally grown) receiver substrates. The step by step transfer process is as followed.

1. 10:1 ratio mixture of PDMS prepolymer and curing agent (Sylgard 184, Dow Corning Co., USA) was cured at 80 °C for 4-5 hrs.
2. The cured PDMS slab was cleaned by dipping into toluene for ~30 min and dried completely on top of a hot plate for ~2-3 hrs.
3. The cleaned PDMS slab (~2 mm thick) was pressed (10–200 N/cm^2, ~10 sec) on top of the partially released InAs NRs on the source substrate.
4. The PDMS slab was gently detached from the source substrate, resulting in the transfer of InAs NRs from the source wafer to the PDMS slab.
5. The PDMS slab with InAs NRs was dipped in 50:1 HF for 1 min to remove any residues of the sacrificial layer on the surface of InAs NRs.
6. InAs NRs were transferred by pressing (10–200 N/cm^2, ~10 sec) the PDMS slab on a Si/SiO_2 receiver substrate in ambient laboratory condition (*e.g.* room temperature and air environment). Before the transfer of InAs NRs, the receiver substrate was cleaned by acetone, IPA, and DI water.
7. The PDMS slab was gently removed from the Si/SiO_2 substrate, leaving behind the InAs NRs.

Figure S3 shows the SEM images of the source substrate before and after the transfer by a PDMS stamp. The results show that InAs NRs are cleanly cleaved from the source wafer.

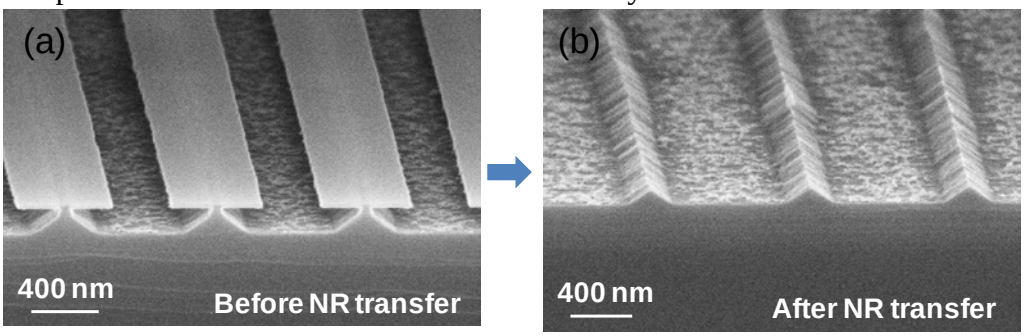

Figure S3. a, SEM image of the source substrate after the partial release of InAs NRs (110 min, 3% NH_4OH etch) and before the transfer step. **b,** SEM image of the source substrate after the transfer process, showing pyramidal AlGaSb posts.

During the transfer process, residues from the AlGaSb sacrificial layer may remain on the back surface of InAs NRs. To remove any potential residues on the backside, the PDMS slab with InAs NRs was dipped in 50:1 HF for 1 min. From the AFM analysis (Fig. S4), InAs NRs exhibit clean surfaces after the HF treatment, which is critical for making a conformal contact during the subsequent transfer to the Si/SiO_2 substrate. To perform AFM analysis of the back side of InAs NRs, a two-step PDMS transfer process was used in which InAs NRs on a PDMS slab were first transferred to a second PDMS slab before getting transferred to a Si/SiO_2 substrate. This results in InAs XOI substrates with the original back surface (*i.e.*, on the source wafer) now being on the top. The effect of HF cleaning is clearly depicted in Fig. S4b.

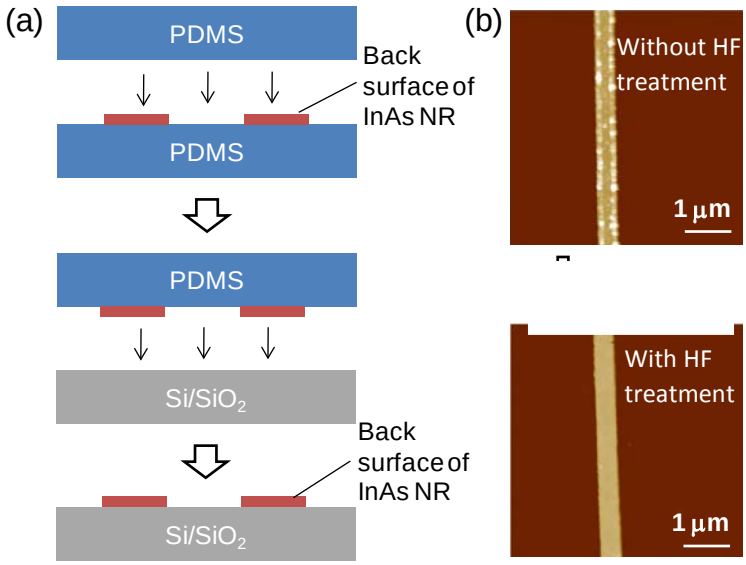

Figure S4. Effect of HF treatment on the back-surface residues of InAs NRs. a, Double transfer procedure for the AFM analysis of the back surface of InAs NRs. **b,** AFM images of InAs NRs on a Si/SiO_2 substrate without (top) and with (bottom) the use of 50:1 HF treatment for 1 min. The HF treatment was performed while the NRs were on the PDMS slab (*i.e.*, the back surface was exposed), prior to their transfer to the Si/SiO_2 substrate.

2.3.4 Field-effect mobility of long-channel, back-gated XOI FETs based on individual InAs NRs

The transconductance ($g_m = dI_{DS}/dV_{GS}|_{V_{DS}}$) as a function of V_{GS} for back-gated InAs XOI FETs, consisting of individual NRs, was first obtained from the measured transfer characteristics at V_{DS}=0.1V. The field-effect electron mobility was then estimated from the relation $\mu_{n,FE} = (g_m)(L^2/C_{ox}V_{DS})$, where L is the channel length and C_{ox} is the gate oxide capacitance. Fig. S5 shows the extracted field-effect electron mobility as a function of V_{GS} for representative XOI FETs with InAs NR thickness of 8, 13, and 48 nm. The peak field-effect mobility increases with the thickness of InAs as depicted in Figure 3b of the main text. It is also evident from the $\mu_{n,FE}$ - V_{GS} plots that the field-effect mobility increases with the gate voltage at first and then decreases at high gate voltages due to the enhanced surface scattering of electrons at high electric fields, similar to the conventional MOSFETs.

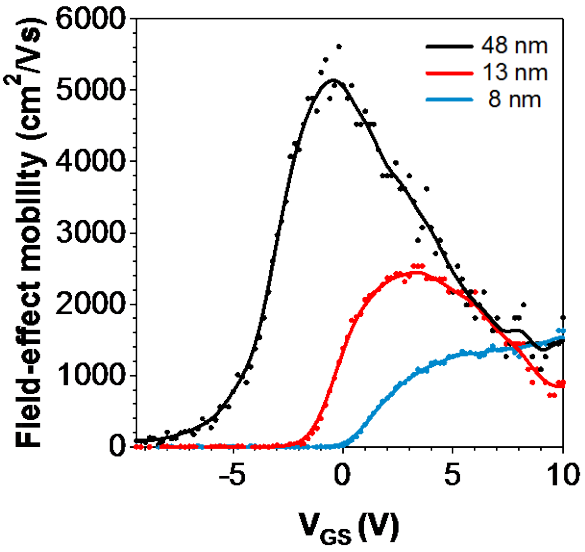

Figure S5. Low-field, field-effect mobility of back-gated InAs XOI FETs as a function of V_{GS} for different InAs NR thickness (8, 13, 48 nm) at V_{DS}=0.1 V. The field-effect mobility is extracted from the measured I_{DS}-V_{GS} curves at V_{DS}=0.1 V (Fig. 3a).

2.3.5 Calculation of phonon mobility of InAs NRs

This section outlines the calculation of low-field mobility of InAs NRs by considering various phonon scattering mechanisms. As the NRs are not intentionally doped, we assume an electron concentration n~ 10^{15} cm^{-3} arising due to unintentional doping. The density of states of NRs can be approximated by $m^*/\pi\hbar^2 T_{InAs}$, where T_{InAs} is the NR thickness. Since this density of states is much larger than n, it is reasonable to assume that the equilibrium Fermi energy E_F lies within the bandgap for all values of T_{InAs}. Hence, the peak mobility measured in experiments corresponds to the maximum transconductance g_m, which occurs when E_F coincides with the first conduction sub-band in the channel. We consider the contribution of acoustic and optical phonons along with polar optical phonons - the dominant source of scattering in polar semiconductors like InAs. The

scattering rate due to acoustic and optical phonons is summed over longitudinal and transverse modes. The energy dependent scattering rate is averaged over the range of a few k_BT around E_F.

$$\left\langle \frac{1}{\tau} \right\rangle = \frac{\int \frac{1}{\tau(E)} \frac{\partial f_0}{\partial E} dE}{\int \frac{\partial f_0}{\partial E} dE}$$

Here $\left\langle 1/\tau \right\rangle$ is the average scattering rate, $1/\tau(E)$ the total scattering rate of an electron with an energy E due to all scattering mechanisms and f_0 the equilibrium Fermi-Dirac distribution function. The low-field NR phonon mobility $\mu_{\text{n,phonon}}$ is then calculated as $\mu_{\text{n,phonon}} = e/m^* \left\langle 1/\tau \right\rangle$, where e is the electronic charge *and* m^* *is the effective mass*. An 8×8 Kane's second order *k.p* Hamiltonian is used to model the quantum confinement effects like the change in the bandgap, effective mass etc. in the dispersion relation of InAs NRs[30,31]. Three approximations are used for the calculations. i) The parabolic band approximation was used for the estimation of the conduction band density of states. This is justified due to the fact that we are interested in the peak mobility that arises at the onset of threshold where the Fermi level is near the bottom edge of the conduction band. For both bulk and thin InAs NRs, the bottom of the conduction band along the direction of transport (100) is largely parabolic. ii) 3D (*i.e.,* bulk) phonon modes were used for all thicknesses[32]. iii) Finally, interband scattering was ignored for simplicity.

The rate for each of the scattering mechanisms is calculated using the Fermi's golden rule wherein the matrix elements of each of the scattering potentials are evaluated in the basis of eigenfunctions of the NR[4].

The scattering rate due to acoustic phonons in a NR of width T_{InAs} is given by32:

$$\frac{1}{\tau_{ac}(E)} = \sum_{p=LA,TA1,TA2} \frac{3\pi D_A^2 k_B T}{2hC_p T_{\text{InAs}}} g_{2D}(E)$$

where

$$g_{2D}(E) = \frac{m^*}{\pi\hbar^2} \sum_n \Theta(E - E_n)$$

$$E_n = \frac{\mathrm{h}^2}{2m^*_{conf}} \left(\frac{n\pi}{T_{\text{InAs}}} \right)^2,\ n = 1,2,3 \ldots n_{\max}$$

Here, $1/\tau_{ac}(E)$ is the acoustic phonon scattering rate, D_A is the electron intravalley acoustic deformation potential, C_p is the elastic constant corresponding to mode p, related to velocity of sound in that mode $v_{s,p}$ by $v_{s,p} = \sqrt{\frac{C_p}{\rho}}$, ρ being the density of InAs, $g_{2D}(E)$ the 2D density of states in the NR, $\Theta(.)$is the unit step function, m^* is the effective mass in the direction of confinement and $n_{\max} = \frac{T_{\text{InAs}}}{a_0}$, a_0 being the lattice constant of InAs. We used the reported values of D_A and $v_{s,p}$ from Ref. [33] and Ref. [34], respectively.

Similarly, the scattering rate due to optical phonons is given by[32]

$$\frac{1}{\tau_{op}(E)} = \sum_{p=LO,TO} \frac{3\pi D_0^2}{4\rho\omega_p W_{rib}} g_{2D}(E \pm \hbar\omega_p)(N_0 + \tfrac{1}{2} \mp \tfrac{1}{2})$$

where

$$N_0 = \frac{1}{\exp(\frac{\hbar\omega_p}{k_B T}) - 1}$$

Here, $1/\tau_{op}(E)$ is the scattering rate due to optical phonons, D_0 the electron optical deformation potential, ω_p the optical phonon frequency of mode p. The top sign corresponds to phonon absorption and bottom one to phonon emission. The values for ω_p and d_0 ($=D_0\, a_0$) are obtained from Ref. [35] and Ref. [36], respectively.

The scattering rate due to polar optical phonons is given by[32]:

$$\frac{1}{\tau_{pop}(E)} = \frac{e^2\omega_{LO}\left(\frac{\kappa_0}{\kappa_\infty} - 1\right)}{2\pi\kappa_0\varepsilon_0\hbar\sqrt{2E/m^*}} \left[N_0 \sinh^{-1}\left(\frac{E}{\hbar\omega_{LO}}\right)^{1/2} + (N_0 + 1)\sinh^{-1}\left(\frac{E}{\hbar\omega_{LO}} - 1\right)^{1/2} \right]$$

where $1/\tau_{pop}(E)$ is the polar optical phonon scattering rate, ω_{LO} is the longitudinal optical phonon frequency, κ_0 and κ_∞ are the static and high frequency permitivities respectively. It must be noted that the polar optical phonon scattering rate, owing to the nature of the scattering potential, does not depend explicitly on T_{InAs} unlike the other two scattering mechanisms and the dependence comes through m^*.

The calculated mobility vs. thickness is shown in Fig. 3(b) by the solid black curve. For small thicknesses the mobility increases almost linearly with thickness. This is due to the fact that with increasing thickness more modes start to creep into the energy window that contributes to the current flow. As the thickness increases, the additional increase in the number of modes starts to saturate and beyond a threshold point, the mobility saturates to the well known bulk value of InAs[37].

From the measured field-effect and calculated phonon mobilities as a function of T_{InAs} (Fig. 3b), the following observations can be made. First, the calculated value of $\mu_{\mathrm{n,phonon}}$ for large values of T_{InAs} (i.e., ~50 nm) is close to the bulk Hall mobility of InAs reported in the literature[37] thus ascertaining that all the dominant scattering mechanisms are considered. Second, the drop in the measured value of field-effect mobility with thickness miniaturization, which signals the onset of confinement effects, occurs for T_{InAs}=30-40 nm. This critical thickness which is consistent with the experimental result is close to the Bohr radius of bulk InAs (~34 nm). Notably, the thickness where the system transitions from 3D to 2D depends strongly on m^*. A quantitative agreement with experiments in this regard further validates the m^* values calculated from InAs NR dispersion relations. It should be noted that in all the calculations, NRs are effectively treated as thin films, since the widths are large enough (>~300 nm) not to cause confinement effects along the width of the NRs. Only the thickness affects the electronic properties.

2.3.6 Device simulation of InAs XOI FETs

The two dimensional simulations were carried out by self consistently solving Poisson's Equation, the electron and hole drift diffusion equations using TCAD Sentaurus 2009. Both top-gated and back-gated device structures were simulated. The back-gated FET consisted of a p-Si substrate with $N_A=10^{21}$ cm^{-3} used as the global gate with 50 nm of SiO_2 (ε=3.9) gate dielectric. A 2 nm thick indium oxide layer (ε=3.4) was assumed on the top and bottom surfaces. The channel length was assumed 5 µm, and the InAs thickness was varied from 5-50 nm. The InAs NR was assumed n-type with $N_D=4\times10^{16}$ cm^{-3}. This value was chosen to best match the experimental ON current for the devices. In addition, thin regions of heavily doped InAs were inserted between the contacts and the channel to minimize contact effects on the simulated data. Interface traps were placed at the InAs/Indium Oxide interfaces on both the top and bottom surfaces of NRs. The interface trap density was used as a fitting parameter with D_{it} = 6×10^{12} states eV^{-1}-cm^{-2} was found to fit the experimental results the best for all NR thicknesses. The major contribution of D_{it} is reducing the efficiency of the gate-field in modulating the channel charge density. In addition, field-dependent mobility and velocity saturation models were both considered. The interface scattering was treated by using the vertical-field mobility degradation model of Sentaurus. This models the mobility degradation at the interface as a function of the vertical-field using calibrated parameters for conventional MOSFETs. A one-band effective-mass model was used which ignores the effect of quantum confinement on the density of states. In the future, a more accurate device simulation that incorporates the density of states as a function of quantization and InAs thickness is needed. For each NR thickness, the calculated phonon mobility, confined bandgap, and confined effective mass were used as input parameters. Due to the weak gate coupling to the channel (arising from the back-gate geometry) and the high D_{it}, the current in the V_{GS} = -0.5V to 0.5V region is not properly handled by Sentaurus. In order to provide for a smooth transition between the subthreshold and accumulation regimes, the simulated I_{DS}-V_{GS} curves were fit to an error function, with the points mentioned above removed. This allowed for a more accurate fitting for the region between the subthreshold and ON-state regimes. The threshold voltage of each simulated curve was shifted to match that of the corresponding experimental device. After fitting, the field-effect mobility was deduced as a function of the gate voltage from the simulated *I-V* characteristics by using the analytical expression described previously. The peak mobility was then extracted for each InAs thickness and plotted in Figure 3b. Note that the 5-10x reduction of the field-effect mobility as compared to the calculated phonon mobility is expected due to the various device contributions, including vertical-field induced carrier scattering and D_{it}. As a parallel, for lightly doped Si, the measured mobility for an effective field of 1MV/cm is ~250 cm^2/V-s, while, for the same doping, the sheet mobility is ~1100 cm^2/V-s [38,39]. This behavior is similar to that observed in our InAs XOI FETs.

Similarly, the top-gated XOI FETs were simulated with 2 nm of indium oxide assumed on the two surfaces of InAs with a body doping concentration of $N_D=4\times10^{16}$ cm^{-3}. The top gate stack was composed of 7 nm of ZrO_2 (ε=20) and a metal gate electrode with a workfunction of 5eV. The source and drain contacts were assumed ohmic. To fit the subthreshold swing of the experimental devices, the trap density at the $InAs/InAsO_x$ interfaces was chosen to be $D_{it}=10^{11}$ states eV^{-1}-cm^{-2}. Notably, this extracted D_{it} is ~60× lower than that of the back-gated FETs as the former consists of thermally grown $InAsO_x$ passivation layer while the latter consists of a native oxide layer. To fit the linear region, the series resistance at the source and drain (R_s, R_d) were chosen to be 100 Ω.μm (unit width normalized) as obtained from the length dependent transport studies (Fig. S6). The threshold voltage was shifted to match that of the corresponding experimental device. The simulation results are show in Figure S7, clearly depicting the close match between the experiment and simulation, further demonstrating the near ideal material and device system presented in this work with deterministic electrical properties. Note that this simulation is valid only for low to moderate gate overdrives where the Fermi level is near the conduction band edge. Within this regime, the parabolic band approximation used in this work is valid. In the future, a more accurate simulation of the XOI FETs with the proper band structure treatment and quantum confinement effects is needed.

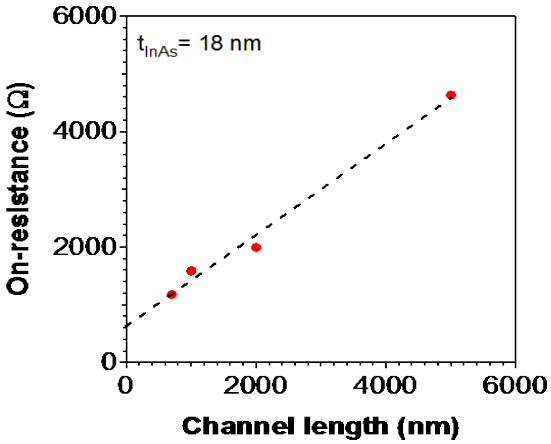

Figure S6. Extraction of the parasitic contact resistance. ON-state resistance vs. channel length, L for single NR FETs (back-gated) with T_{InAs}~18 nm and width ~350 nm. On-resistances are extracted from back-gated I_{DS}-V_{GS} curves at V_{GS}=10V and V_{DS}=0.3V. The experimental data are shown as red dots and the dashed line is the best fit line. The extrapolated resistance at L=0 nm corresponds to the parasitic contact resistance. From the data, a parasitic resistance of ~600 Ω is obtained, corresponding to ~300 Ω for the S/D electrodes individually. The unit width normalized parasitic resistance for each contact electrode is ~100 Ω.μm.

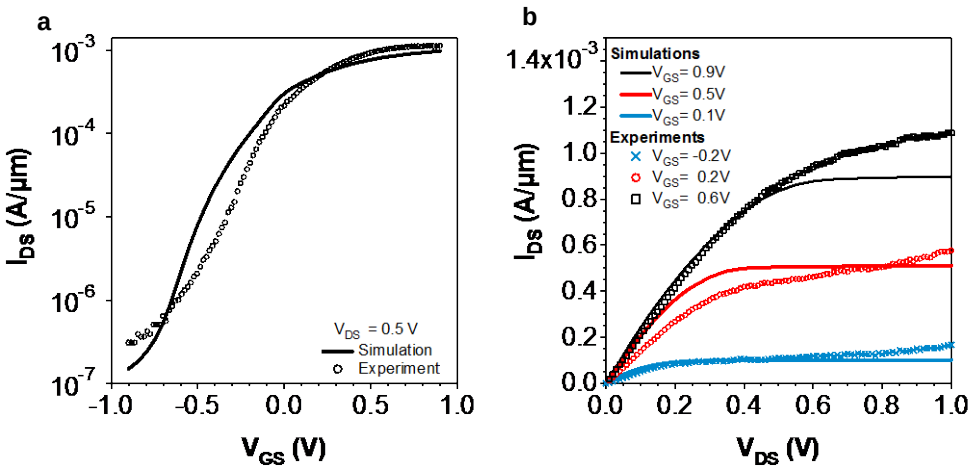

Figure S7. Electrical characterization of top-gated InAs XOI FETs. **a**, Transfer and **b**, output characteristics of an InAs XOI FET (~18 nm thick) with *L*~0.5 μm, showing a close fit between the experiment and simulation. Note that the device is the same as the one shown in Figure 4b-c of the main text.

2.3.7 Electrical properties of InAs XOI top-gated FETs as a function of surface/interface treatment

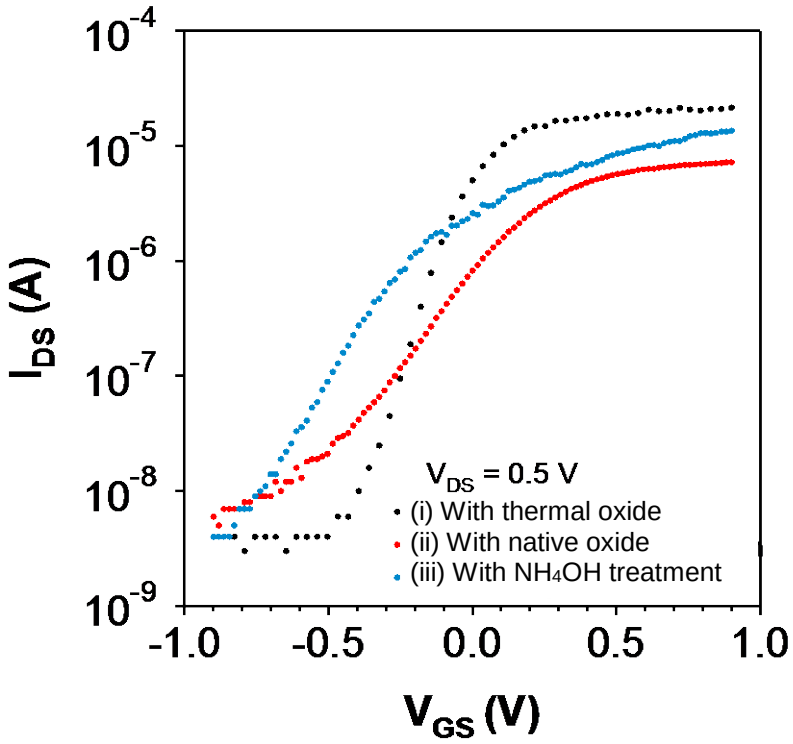

Figure S8. **Transfer characteristics of three InAs XOI top-gated FETs with different surface treatment prior to the ALD of the ZrO_2 gate dielectric.** (i) With a thermal oxidation of InAs at 350ºC for 1 min (resulting in ~1 nm thermal $InAsO_x$) prior to the ALD (black marks), (ii) without any surface treatment (*i.e.*, consisting of ~ 1 nm native surface oxide layer) before ALD (red marks), and (iii) with NH_4OH immediately prior to the ALD to remove the surface oxide layer (blue marks). For the thermally oxidized sample, the native oxide was first removed by a treatment with 3% NH_4OH. The results clearly depict the drastic enhancement of the subthreshold characteristics due to the effective surface passivation role of the thermally grown $InAsO_x$ layer, resulting in enhanced electrostatic coupling of the gate electrode. The SS is 107, 290, and 230 mV/decade for devices (i)-(iii), respectively. The channel lengths are 2 µm, 5 µm, and 5 µm for devices (i)-(iii), respectively.

2.3.8 Experimental transconductance as a function of gate bias for a top-gated XOI FET

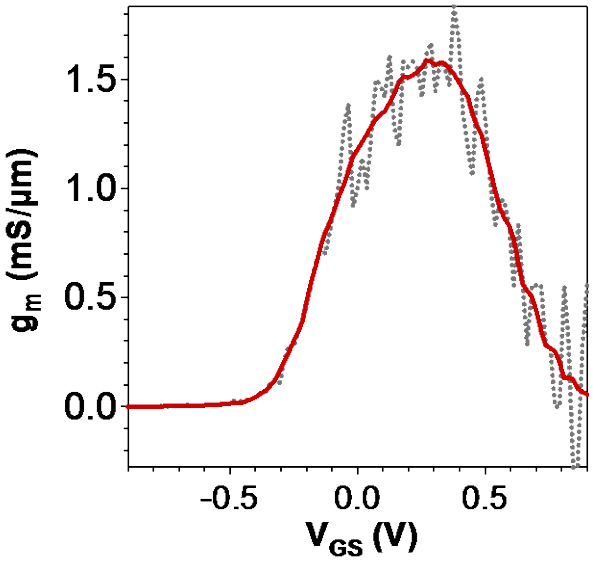

Figure S9. Transconductance, $g_m = dI_{DS}/dV_{GS}\big|_{V_{DS}}$ at V_{DS}=0.5 as a function of V_{GS} obtained from the I_{DS}-V_{GS} data shown in Figure 4c. The dashed gray line represents the obtained transconductance after current differentiation while the red line is after 2nd order Savitsky-Golay smoothing.

The transconductance (Fig. S9) extracted from the measurement includes the effect of series resistance. The intrinsic transconductance can be extracted from the measured by $g_{mi} = g_m/(1-g_mR_S-g_dR_{SD})$[40], where R_S is the source series resistance and R_{SD} is the source and drain series resistance and g_d is the drain conductance ($=dI_{DS}/dV_{DS}$). Using this analysis, the g_{mi} of the device presented here is ~2 mS/μm.

To analyze the transconductance, it is beneficial to look at the basic equation for current in a MOSFET, $I_{DS} = v_{drift}*n*q$, where v_{drift} is the electron drift velocity, n is the carrier density, and q is the charge of an electron. This leads to a $g_{mi}=v_{drift}(C_{ox}/L)$ in the high field regime. Since C_{ox} is the total capacitance, it is a linear function of L, making g_{mi} independent of L at high fields. From the v_{drift} vs. electric field curve[41] for bulk InAs, at a field of 10 kV/cm, the drift velocity is ~1.5 x 10^7 cm/s. For the presented device, this leads to a calculated g_{mi} ~2 mS/μm, which is close to the extracted value. This is a rough estimate, since the bulk field vs. velocity relation was used as the same for confined InAs is not readily available.

When compared to InAs HEMTs in literature, the transconductance of our FETs is comparable. The values of intrinsic transconductance for InAs FETs with 10 nm InAs thickness is reported to be ~3mS/ μm for L from 40 nm – 100 nm[42].

References

1. Lundstrom, M. Moore's law forever? *Science* **299**, 210–211 (2003).
2. Heyns, M., Tsai, W. Ultimate scaling of CMOS logic devices with Ge and III-V materials. *MRS Bull.* **34**, 485-488 (2009).
3. Theis, T. N., Solomon, P. M. It's time to reinvent the transistor! *Science* **327**, 1600-1601 (2010).
4. Chau, R., Doyle, B., Datta, S., Kavalieros, J., Zhang, K. Integrated nanoelectronics for the future. *Nature Mater*. **6**, 810-812 (2007).
5. Javey, A., Guo, J., Wang, W., Lundstrom, M., Dai, H. Ballistic carbon nanotube transistors. *Nature* **424**, 654-657 (2003).
6. Wong, P. H.-S. Beyond the conventional transistor. *Solid-State Electron.* **49**, 755–762 (2005).
7. Wu, Y. Q., Xu, M., Wang, R. S., Koybasi, O., Ye, P. Y. High performance deep-submicron inversion-mode InGaAs MOSFETs with maximum Gm exceeding 1.1 mS/um: new HBr pretreatment and channel Engineering. *IEEE IEDM Tech. Digest **2009***, 323-326 (2009).
8. Bryllert, T., Wernersson, L. E., Froberg, L. E., Samuelson, L. Vertical high-mobility wrap-gated InAs nanowire transistor. *IEEE Electron Device Lett.* **27**, 323-325 (2006).
9. Liu, Y. *et al*. Device physics and performance potential of III-V field-effect transistors. *Fundamental of III-V Semiconductor MOSFETs* (Springer, New York, 2010).
10. Radosavljevic, M. *et al.* Advanced high-k gate dielectric for high-performance short-channel In0.7Ga0.3As quantum well field effect transistors on silicon substrate for low power logic applications. *IEEE IEDM Tech. Digest **2009***, 319-322 (2009).
11. Javorka, P. *et al.* AlGaN/GaN HEMTs on (111) silicon substrates. *IEEE Electron Device Lett*. **23**, 4-6 (2002).
12. Balakrishnan, G. *et al*. Room-temperature optically-pumped GaSb quantum well based VCSEL monolithically grown on Si (100) substrate, *Electron. Lett.* **42**, 350-351 (2006).
13. Yonezu, H. Control of structural defects in group III-V-N alloys grown on Si. *Semicond. Sci. Technol*. **17**, 762-768 (2002).
14. Celler, G.K., Cristoloveanu, S. Frontiers of silicon-on-insulator. *J. Appl. Phys.* **93**, 4955-4978 (2003).
15. Yablonovitch, E., Hwang, D. M., Gmitter, T. J., Florez, L. T. & Harbison, J. P. Van der Waals bonding of GaAs epitaxial liftoff films onto arbitrary substrates. *Appl. Phys. Lett.* **56**, 2419–2421 (1990).
16. Kim, D.-H. *et al*. Ultrathin silicon circuits with strain-isolation layers and mesh layouts for high-performance electronics on fabric, vinyl, leather, and paper. *Adv. Mater*. **21**, 3703–3707 (2009).
17. Melosh, N. *et al*. Ultrahigh density nanowire lattices and circuits. *Science* **300**, 112-115 (2003).
18. Yokoyama, M. *et al*. III-V-semiconductor-on-insulator n-channel metal-insulator-semiconductor field-effect transistors with buried Al2O3 layers and sulfur passivation: Reduction in carrier scattering at the bottom interface. *Appl. Phys. Lett*. **96**, 142106 (2010).
19. Yuan, H.-C., Ma, Z. Microwave thin-film transistors using Si nanomembranes on flexible polymer substrate. *Appl. Phys. Lett.* **89**, 212105 (2006).
20. Kim, D.-H. *et al*. Stretchable and foldable silicon integrated circuits. *Science* **320**, 507-511 (2008).

21. Yoon, J. *et al*. GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature* **465**, 329-333 (2010).
22. Chueh, Y.-L. *et al*. Formation and characterization of NixInAs/InAs nanowire heterostructures by solid source reaction. *Nano Lett*. **8**, 4528–4533 (2008).
23. Kim, D.-H. *et al.* Scalability of Sub-100 nm InAs HEMTs on InP Substrate for Future Logic Applications. *IEEE Trans. Elec. Dev*. **57**, 1504 (2010).
24. Lundstrom, M. Carrier scattering. *Fundamentals of Carrier Transport* (Cambridge University Press, Cambridge, 2000).
25. Mikhailova, M. P. Indium Arsenide. *Handbook Series of Semiconductor Parameters, vol 1: Elementary Semiconductors and A3B5 Compounds Si, Ge C, GaAs, GaP, GaSb InAs, InP, InSb* (World Scientific, 1996).
26. Martens, K. *et al*. On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates. *IEEE Trans. Electron Devices* **55**, 547-556 (2008).
27. DeSalvo, G. C., Kaspi, R., Bozada, C. A. Citric acid etching of GaAs1-xSbx, Al0.5Ga0.5Sb, and InAs for heterostructure device fabrication, *J. Electrochem. Soc*. **141**, 3526-3531 (1994).
28. Yoh, K., Kiyomi, K., Nishida, A., Inoue, M. Indium arsenide quantum wires fabricated by electron beam lithography and wet-chemical etching. *Jpn. J. Appl. Phys*. **31**, 4515-4519 (1992).
29. Meitl, M. A. *et al*. Transfer printing by kinetic control of adhesion to an elastomeric stamp. *Nature Mater*. **5**, 33-38 (2006).
30. Gershoni, D., Henry, C. H., Baraff, G. A. Calculating the optical properties of multidimensional heterostructures: application to modeling of quaternary quantum well lasers. *J. Quantum Electron*. **29**, 2433–2450 (1993).
31. Foreman, B. A. Elimination of spurious solutions from eight-band k. p theory. *Phys. Rev. B* **56**, R12748 (1997).
32. Mark Lundstrom. Carrier scattering. In *Fundamentals of Carrier Transport* (Cambridge, 2000).
33. Van de Walle, C. G. Band lineups and deformation potentials in the model-solid theory. *Phys. Rev. B* **39,** 1871-1883 (1989).
34. Adachi, S. Indium arsenide (InAs). *Handbook on Physical Properties of Semiconductors* (Kluwer Academic Publishers, 2004).
35. Groenen, J., Priester, C., Carles, R. Strain distribution and optical phonons in InP/InAs self-assembled quantum dots. *Phys. Rev. B* **60,** 16013-16017 (1999).
36. Pötz, W., Vogl, P. Theory of optical-phonon deformation potentials in tetrahedral semiconductors. *Phys. Rev. B* **24**, 2025 – 2037 (1981).
37. Mikhailova, M. P. Indium arsenide. *Handbook Series of Semiconductor Parameters, vol 1: Elementary Semiconductors and A3B5 Compounds Si, Ge C, GaAs, GaP, GaSb InAs, InP, InSb* (World Scientific, 1996).
38. Chau, R. et al., Advanced CMOS Transistors in the Nanotechnology Era for High-Performance, Low-Power Logic Applications, *ICSICT Tech. Dig.* 26-30 (2004).
39. Sze, S. M., Irvin, J. C. Resistivity, Mobility and Impurity Levels in GaAs, Ge, and Si at 300K. *Solid-State Electronics* **11**, 599-602 (1968).
40. Chou, S. Y., Antoniadis, D.A., Relationship Between Measured and Intrinsic Transconductances of FET's, *IEEE Elec. Dev. Lett*, 448 – 450 (1987).
41. Brennan, K., Hess, K., High Field Transport in GaAs, InP and InAs, *Solid-State Electronics*, **27**, 347-357, (1984)

42. Kim, T.-W., Kim, D.-H., del Alamo, J. A., Logic characteristics of 40 nm thin-channel InAs HEMTs, *Indium Phosphide and Related Materials (IPRM)*, 2010

3

Nanopillar Photovoltaics

3.1 Introduction

The main requirement for any competitive photovoltaic (PV) technology is the cost per watt installed. To achieve this goal, a PV technology must not only have a low unit area cost, but also high efficiency. Nanopillar (NPL) and nanowire (NW) PV[1,2,3] address these requirements in three ways: i) direct growth of crystalline materials on low-cost substrates without the use of complex epitaxial processes, ii) maximization of carrier collection efficiency by decoupling the light absorption and carrier collection directions, and iii) minimization of optical losses by reduced reflection and enhanced absorption. Significant work has been carried out in recent years on all aspects of NPL/NW photovoltaics including synthesis[4,5,6,7], optical properties [8,9,10,11,12,13,14,15,16,17], and device physics[18,19,20,21,22]. Additionally, both single NW devices[23,24,25,26] and arrays[13,27,28] have been studied in detail. Here, we review the recent work in our group and others on developing viable fabrication processes for NPL/NW PVs as well as the optical and electronic properties of the resulting structures.

Of the possible architectures for NPL PVs, the two that enable enhanced carrier collection are NPLs embedded in a film[28] (Fig 1a), and core-shell NPLs[29,30,31] (Fig 1b). Considering these architectures, the optical and electronic design constraints on NPL PV are considerably relaxed compared to their planar counterparts. To prevent efficiency degradation through optical losses, the thickness of the cell must be greater than the absorption length of the material (Fig 1c). Due to the excellent anti-reflective and light trapping properties of wire arrays[15,17], a significantly lower volume of active material, as compared to planar cells, can be used to absorb the majority of the incident solar photons. Similarly, by carefully tuning the geometry of the NPL cell, it is possible to maximize minority carrier collection for a given material quality[18]. This design parameter is not available to planar cells since the carrier collection and light absorption directions are parallel. This design parameter enables NPL PV from even moderate quality materials to display excellent carrier collection efficiencies. However, the surface and interface area in NPL PV is significantly enhanced over planar cells. Thus it is critical to choose material systems with low interfacial and surface recombination rates to minimize carrier loss at interfaces. For instance, InP[32], CdS[33] and CdTe[34] exhibit low surface recombination velocities in the range of $10^2 – 10^4$ cm/s. For Si, the recombination velocities of untreated surfaces are

reported to be in the range of 10^{4}-10^{7} cm/s, but can be reduced to ~10^{2} cm/s by appropriate surface passivation[35].

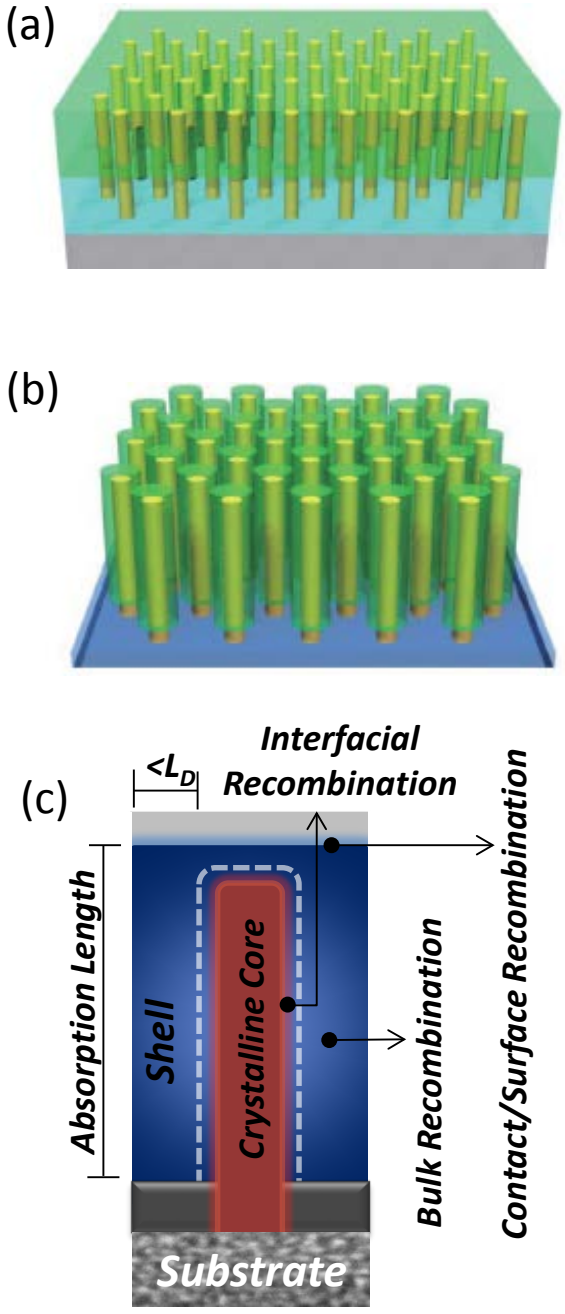

Figure 1. Nanopillar architectures. (a) Array of NPLs embedded in a thin film; (b) NPL radial junctions (c) Schematic of a NPL PV cell with important lengths and recombination processes identified. Reprinted with permission from Ref. [1] (Copyright 2009, Tsinghua University Press)

Each architecture has its advantages and drawbacks with respect to the control over optical properties and electronic properties as well as ease of fabrication. Embedded NPLs enable maximization of carrier collection by adjusting the NPL pitch, allowing moderate efficiencies to be achieved even if the absorber material has a low bulk minority carrier lifetime. However, due to the planar top surface, the optical properties are similar to planar cells when the thin film is the absorber material. On the other hand, free-standing core-shell NPLs, enable optical engineering of the structure by controlling the size and pitch of the NPLs, as well as the possibility to tune the carrier collection by varying the core-shell radii. This method is more challenging to fabricate, as a conformal coating is needed to form a p-n junction.

While many promising material systems have been explored for thin film solar cells, CdS/CdTe is one of the most prevalent. The advantages of the CdS/CdTe system include the near-ideal bandgap of the CdTe absorber layer, good defect tolerance of poly-CdTe, good quality of the CdS/CdTe hetero-interface, and ease of deposition of this material system. The main limitations are the toxicity of Cd, scarcity of Te, and the lower efficiencies when compared to single-crystalline PV from materials such as Si and GaAs. Regardless, the high quality of the CdS/CdTe interface makes this material system ideal for studying the properties of NPL PV.

Various fabrication approaches have been explored. In one example, to fabricate embedded CdS/CdTe NPL PV cells, a porous anodic aluminum oxide (AAO) was used as a template for nanomaterial growth[28]. In this architecture, the CdTe is the absorber layer, and the CdS NPLs acts as current collectors. Figure 2 shows a schematic of a CdS/CdTe NPL cell fabrication process. In short, a porous AAO template is fabricated with electroplated Au catalyst seeds for subsequent NPL growth at the bottom of each pore. The CdS pillars are grown via a vapor-liquid-solid (VLS) growth process. The AAO template is etched back, exposing the pillars, and the CdTe absorber layer is then deposited. A semitransparent top contact of copper/gold was then deposited. This process enables the fabrication of an NPL cell on a low-cost metal foil entirely through processes that are compatible with a roll-to-roll fabrication scheme.

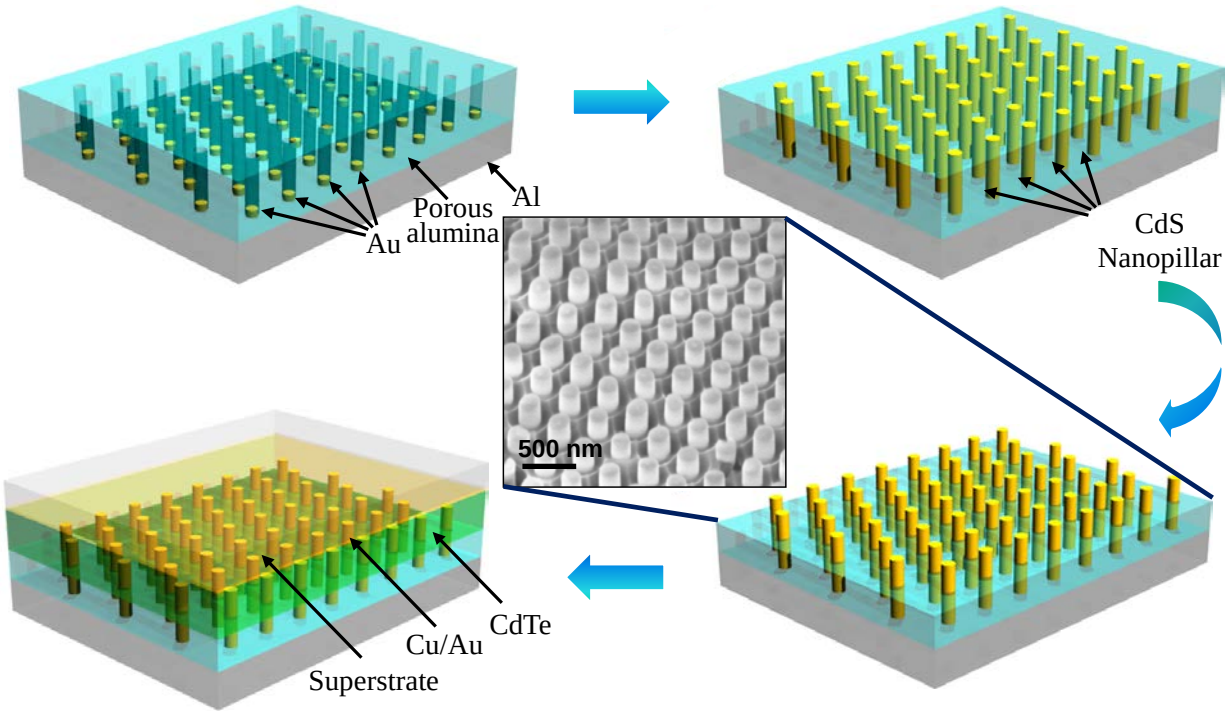

Figure 2. 3D solar nanopillar (SNOP) cell fabrication process flow. Reprinted with permission from Ref. [28] (Copyright 2009, Nature Publishing Group)

3.2 Design constraints and guidelines for CdS/CdTe nanopillar based photovoltaics

The performance dependence of a CdS/CdTe nanopillar solar cell on various device and materials parameters is explored while examining its performance limits through detailed device modeling. The optimized cell enables efficiencies >~20% with minimal short circuit current dependence on bulk minority carrier diffusion length, demonstrating the efficiency in collecting photogenerated carriers, therefore, lowering the materials quality and purity constraints. Given the large p-n junction interface area, the interface recombination velocity is shown to have detrimental effect on the device performance of nanopillar solar cells. In that regard, the CdS/CdTe material system is optimal due to its low interface recombination velocity.

Over the past several years, nanostructured materials have been extensively explored for photovoltaic (PV) devices. Specifically, nanowire (NW) and nanopillar (NPL) devices have been studied experimentally and computationally[1-3]. Recently, we reported a CdS/CdTe solar nanopillar (SNOP) cell with ~6% conversion efficiency, despite non-optimal contacts,[3] a ~5x improvement over previously reported NW/NPL array solar cells[4,5]. This performance advance is attributed to the proper use of device architecture and material system. Here, we explore the effects of materials quality and interface properties on the performance of CdS/CdTe SNOP cells through detailed device simulation while examining their performance limits. This work presents an important guideline for future fabrication of high performance NPL cells, shedding light on their materials/device constraints.

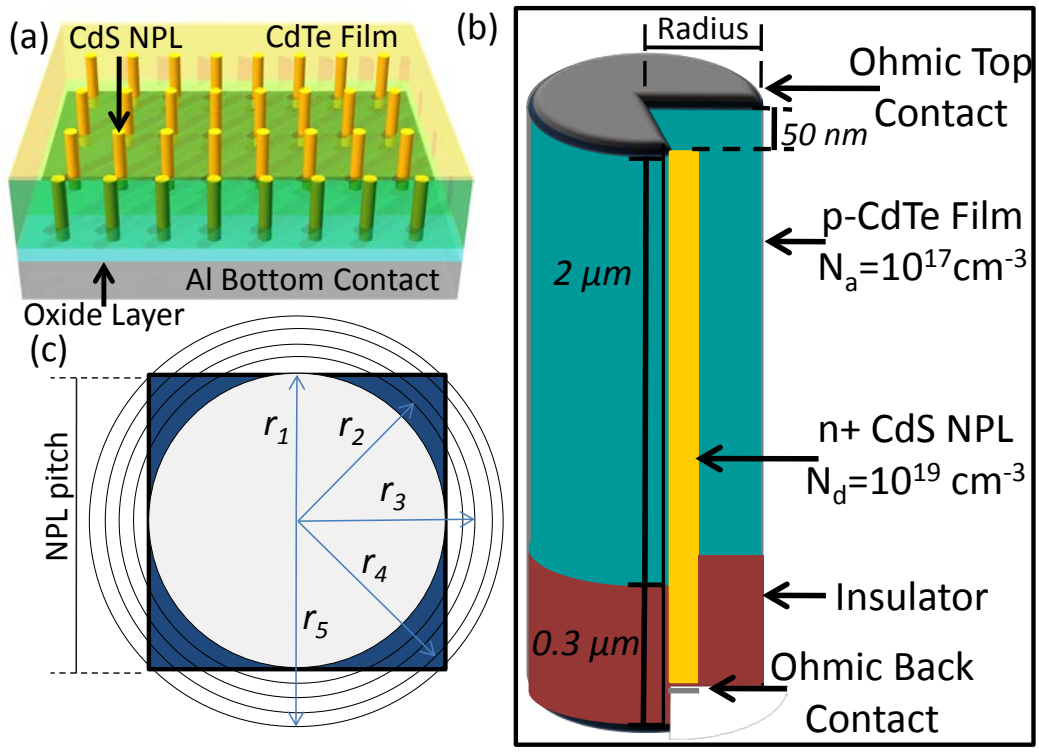

Figure 3: (a) Schematic of a SNOP-cell. (b) The structure used for device modeling after assuming cylindrical symmetry. (c) An overhead view of the unit cell.

The SNOP cell (Fig. 3a) consists of an array of CdS NPLs partially embedded in a CdTe thin film. The n-CdS NPLs serve as electron collectors, while the CdTe thin film serves as the absorber layer. Sentaurus Device 2009 was used to simulate the performance of these cells by solving Poisson's equation, the electron continuity, and the hole continuity equation self-consistently. Auger and Shockley-Read-Hall (SRH) recombination process were considered. The SRH recombination was assumed to be due to a single midgap trap level. Since Auger recombination in the CdTe film was orders of magnitude lower than SRH, the carrier lifetimes were set by controlling the SRH lifetime. To represent the effect of CdS/CdTe interface quality, interfacial SRH recombination through a midgap trap state was set by defining an interfacial recombination velocity (S_i) at the CdS/CdTe interface. In practice, there is generally a Schottky barrier at the contacts. The effect of this barrier is often modeled as a diode opposing the p-n junction of the device. For larger barriers (>0.3 eV), the fill factor is degraded and the V_{oc} is decreased. For smaller barriers, both FF and Voc are affected only slightly. The enhanced recombination at the contact can be mitigated by a minority carrier reflector, minimizing the effect of the barrier on J_{sc}. Thus, through optimization, the effect of the barriers can be minimized. Therefore, here we assume both the top and bottom contacts to be ohmic. The AM1.5g spectrum was simulated by binning the energy within the 0.831 μm to 0.32 μm range into 25 discrete wavelengths. The absorption for each wavelength was then calculated using a Beer's law model with the appropriate absorption coefficients.

The SNOP cell is simulated by defining half of a 2-d cross section of the (Fig. 3b) and then assuming cylindrical symmetry in the device equations, using a scheme previously used for Si core/shell NW cells[2]. However, the simulated SNOP cell consisted of a square lattice of NPLs embedded in a CdTe film. This gives rise to a square 'unit cell' as shown in Fig. 3c, which is not accurately represented by the cylindrical structure in Fig. 3b. Thus, to simulate the results for a SNOP-cell with a given pitch, multiple simulations with fixed NPL radius and increasing outer radius were simulated as show in Fig. 1c. The parameters of the SNOP cell were then calculated using the formula: $p = p(r_1) - \sum A(r_i, r_{i+1})[(p(r_i) - p(r_{i+1})]/[\pi {r_{i+1}}^2 - \pi {r_i}^2]$; where p represents the parameter of interest (i.e., conversion efficiency, η, open circuit voltage, V_{oc}, or photocurrent, J_{sc}), $p(r_1)$ is the parameter evaluated at radius r_1, $A(r_i,r_{i-1})$ is the area bounded by circles of radius r_i, r_{i+1}, and the square. This approximation corrects for the missing area through the 1st order Taylor expansion terms from each of the larger diameter simulations. Therefore, it requires that the parameter, p, is close to linear with circular area of the simulation for the radii of interest. It should be noted that this result is only valid when the junctions are sufficiently far apart such that their depletion regions do not interact.

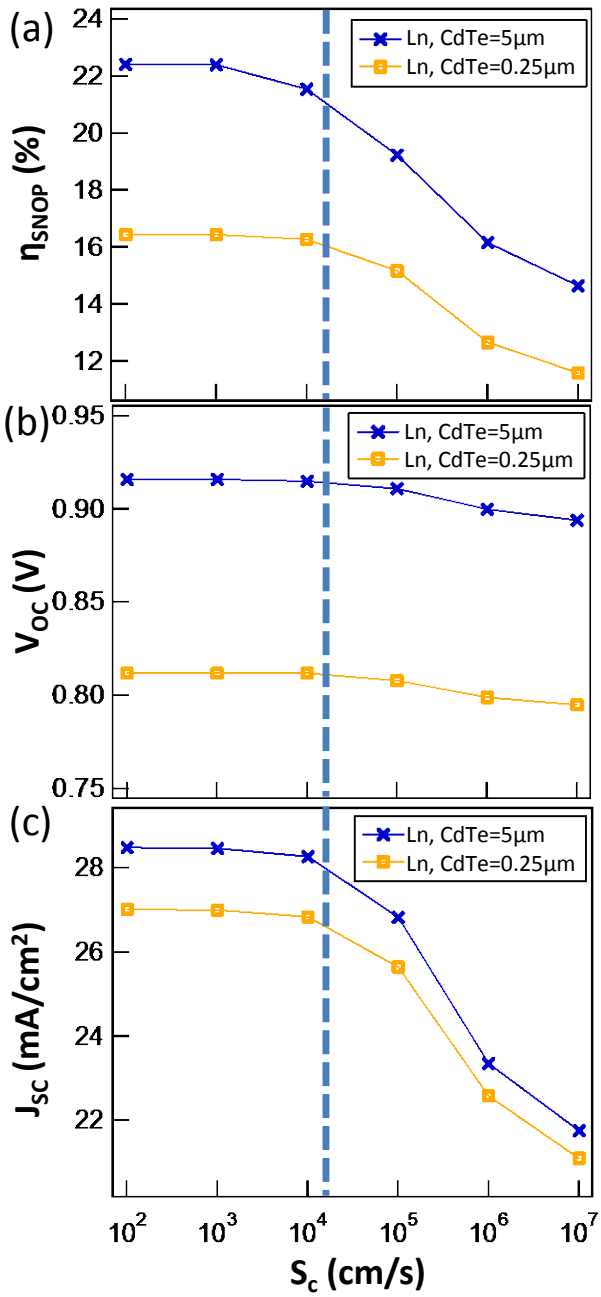

Figure 4: S_c dependency of (a) η, (b) V_{oc}, and (c) J_{sc} are shown for $S_i = 10^3$ cm/s and $L_{n,CdTe}$=0.25 and 5 µm. The dashed lines represent the "effective" S_c when a 5 nm p+ electron reflector is added under the top contact with $S_c = 10^7$ cm/s.

The CdS NPL and CdTe thin film doping concentrations were set to $N_d=10^{19}$ cm^{-3} and $N_a=10^{17}$ cm^{-3}, respectively. The CdS is highly doped to minimize parasitic resistance since it simply serves as an electron collector with minimal carrier generation. The CdTe doping concentration was chosen in order to maintain a moderate depletion region width of ~60nm and still allow for accurate simulation of the device. The electron and hole mobilities used for CdS were μ_n =100 cm^2/V-s and μ_p=25 cm^2/V-s, respectively.[6] For CdTe, μ_n =100 cm^2/V-s and μ_p=40 cm^2/V-s were chosen as a

median from the spread of values reported in literature[7,8]. The minority carrier diffusion lengths were set by varying the SRH lifetime. In CdS, the hole diffusion length was fixed at $L_{p,CdS}$=0.4 μm.[9] Since the CdS contribution to the photocurrent is negligible, $L_{p,CdS}$ is not a critical parameter. For CdTe, a range of electron diffusion lengths, $L_{n,CdTe}$ =0.25-5 μm was chosen, as these represent the lower and upper bounds for CdTe thin films[10]. The thickness of the CdTe layer was set to 2 μm, corresponding to absorption of ~85% for an AM1.5 spectrum[11]. A 0.3 um thick insulator separates the bottom contact from the CdTe layer (Fig. 3b), and the NPL radius and pitch was chosen to be 0.1 and 0.5 μm, respectively.

Although there is significant emphasis on the effects of top surface and metal contact recombination processes on planar cells[12], these effects have been poorly studied for the nanostructured cells. In the CdS/CdTe SNOP cell, only the top contact (i.e., CdTe/contact interface) contributes to the minority carrier loss since minimal light absorption takes place in the CdS NPLs. To determine the effect of contact recombination velocity (S_c) on SNOP cell performance, the structure in Fig. 1 was simulated with S_i=10^3 cm/s, a typical experimentally measured value.[13] S_c was then varied to represent a range of shielding qualities, from heavily shielded (10^2 cm/s) to unshielded (10^7 cm/s). The η shows a strong dependence on S_c (Fig. 4a), dropping ~1.5x and ~1.3x for $L_{n,CdTe}$=0.25 and 5 μm, respectively, as the S_c is increased from 10^2 to 10^7 cm/s. This efficiency drop is predominantly due to the degradation of J_{sc} (Fig. 4b-c), which is an indicator of the aggregate minority carrier collection efficiency. Interestingly, J_{sc} shows minimal dependence on $L_{n,CdTe}$ for the SNOP-cells, in distinct contrast to the planar cells. This trend is expected since for the SNOP-cell geometry explored here, all excess minority carriers are generated <$L_{n,CdTe}$ from the CdS/CdTe interface, resulting in their efficient collection. This presents an important advantage of the SNOP-cell configuration. For all further simulations, a 5 nm thick region of N_a=10^{19} cm^{-3}, which is an upper experimental limit for CdTe doping[14], directly under the top contact is used as a reflector.

The reflector reduces the effect of contact recombination by shielding the minority carriers from the contacts through a potential barrier. In the previously reported experimental SNOP-cells, a heavily p-doped layer was formed underneath the top contact through Cl and Cu treatment of the CdTe surface[3] to effectively lower the S_c. When S_c =10^7 cm/s is enforced at the top contact, the reflector increases the performance of the cell to that of one with a S_c~10^4 cm/s, as confirmed by simulation, which effectively removes the impact of contact recombination on the cell performance (Fig. 2a). It should be noted that in terms of contact recombination, SNOP-cell geometry presents an important advantage over coaxial NW cells since the planar contact of the SNOP-cells has significantly lower surface area (equivalent to that of the planar cells). Due to the enhanced CdS/CdTe interfacial area of the SNOP-cell, the interface recombination processes can significantly alter the device performance. The effect of interface quality on the device performance is modeled for S_i =1 - 10^6 cm/s. Within this range, the interface recombination is found to affect the efficiency only when the bulk recombination rates are relatively low (Fig. 5a). Specifically, we observed η ~15% with minimal S_i dependency for $L_{n,CdTe}$=0.25 μm. On the other hand, when $L_{n,CdTe}$=5 μm, the efficiency is reduced from ~20% to ~16% as the S_i is increased from 1-10^6 cm/s (Fig. 3a). The primary effect of enhanced S_i is a reduction in V_{oc} (Fig. 5b) with the J_{sc} being nearly constant (Fig 5c). For thin film CdS/CdTe, S_i=10-10^3 cm/s has been previously measured and reported in the literature.[13] As a result, the CdS/CdTe material system is optimal for the SNOP-cell due to its low interface recombination velocity.

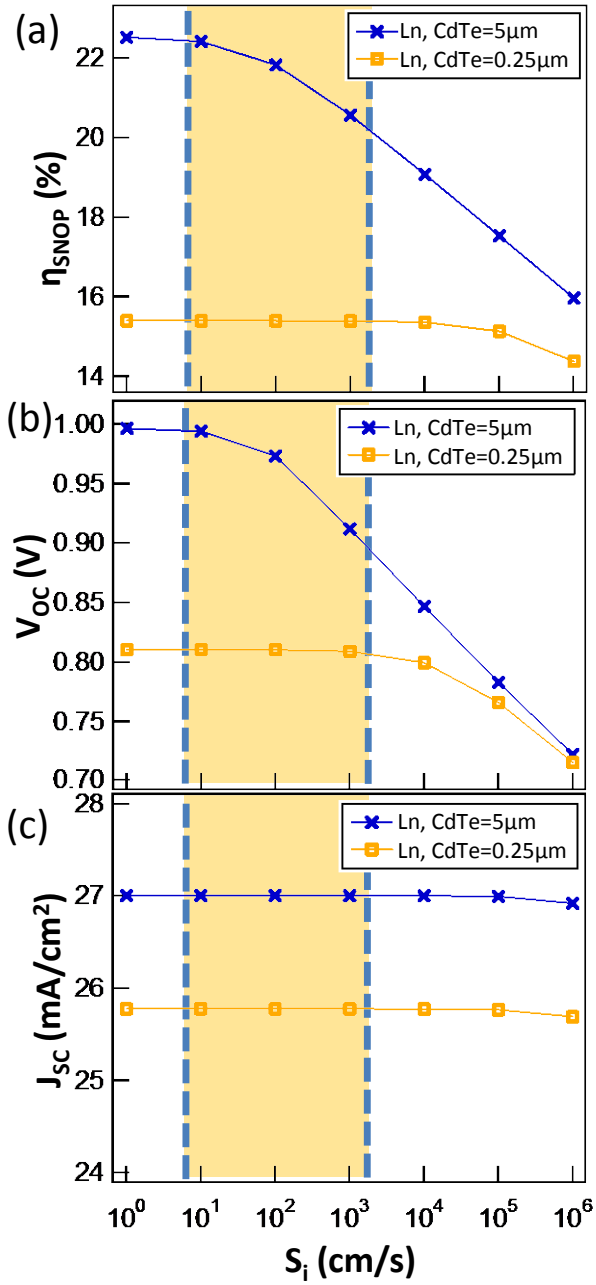

Figure 5: S_i dependency of (a) η, (b) V_{oc}, and (c) J_{sc} are shown for S_c =10^7 cm/s with a 5 nm p+ electron reflector under the top contact, and $L_{n,CdTe}$=0.25 and 5 µm. The experimentally reported range for S_i is highlighted for each graph.

A simple analysis of the results can be carried out by defining an effective carrier lifetime, $1/\tau_{eff} = 1/\tau_0 + 1/\tau_c + 1/\tau_i$, where τ_0 is the bulk lifetime, τ_c is the lifetime due to recombination at the top contact, and τ_i is the lifetime due to interfacial recombination. To calculate τ_c and τ_i, S_c and S_i are first changed to equivalent surface trap densities, $N_{s,c}$ and $N_{s,i}$, respectively. This is achieved by using the relations $S_c = N_{s,c} \times \sigma \times v_{th}, S_i = N_{s,i} \times \sigma \times v_{th}$, and $\tau = 1/(N_t \times \sigma \times v_{th})$, where σ is the capture cross section, v_{th} is the thermal velocity, and N_t is the trap density for a given volume. For the purposes of calculation, we assume the cross sections are the same for all cases. By assuming the surface traps are spread uniformly over a volume, τ_c and τ_i can be approximated from the recombination velocities. For interface recombination, the appropriate volume would be the depletion region. On the other hand, the contact recombination affects minority carriers within $L_{n,CdTe}$ of the surface, unless the CdTe thickness is $<L_{n,CdTe}$, in which case it affects carriers through the entire film. This leads to the relation: $1/\tau_{eff} = 1/\tau_0 + S_c/L_{n,CdTe} + S_i/W_d$. For the case of $L_{n,CdTe}$= 5 μm, $\tau_0 = 9.6*10^{-8}$ s, and for $L_n = 0.25$ μm, $\tau_0=2.4*10^{-10}$ s. This indicates that, for L_n= 5 μm and with a p+ reflector, the performance is limited by the interface recombination when $S_i > \sim 10^2$ cm/s. For $L_n = 0.25$ μm, the interface recombination is dominant when $S_i > \sim 2x10^4$ cm/s. This is clearly visible from Figure 5, and indicates that this simple analysis is valid for estimating the dominant recombination processes in a SNOP cell, given the known material properties.

The effect of pitch on the performance of the SNOP cells was simulated by holding fixed the NPL radius while varying the pitch from 350 nm to 1 μm. The simulation structure was the same as that show in Fig. 3, using $S_i=10^3$ cm/s, $S_c=10^7$ cm/s and a 5 nm thick minority carrier reflector (i.e., effective $S_c \sim 10^4$ cm/s). The data shows two key trends: (i) as the diffusion length increases, the optimal pitch increases, and (ii) even for a system with a moderate diffusion length of 0.25 μm, proper NPL pitch can enable respectable efficiencies of 16% (Fig. 6). These results can be explained as a competition between the CdTe filling factor (i.e., the amount of the absorber layer), and the reduction in carrier collection efficiency with increased pitch. For lower quality materials, η is highly sensitive to NPL spacing and must be considered carefully for cell optimization. Higher quality materials are not as strongly affected by pitch since the drop in carrier collection efficiency occurs over a longer length scale. The median reported experimental value of minority carrier lifetimes[15] in polycrystalline CdTe films correspond to diffusion lengths of ~0.5 μm, further indicating the importance of the SNOP geometry with optimized NPL pitch for the CdS/CdTe material system.

In conclusion, the projected performance limits of CdS/CdTe SNOP-cells are explored by examining the effects of various materials and device parameters on the conversion efficiency, showing that η>~20% should be attainable through materials and device optimization. This work presents an important guideline for future experimental work, and highlights the importance of direct measurement of various recombination rates of nanopillar structures to further advance the efficiency of the cells; an area that has been poorly explored to date.

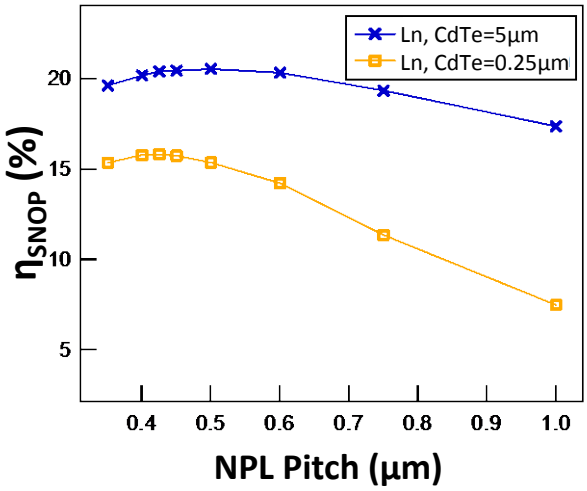

Figure 6: A plot of efficiency vs. NPL pitch for $L_{n,CdTe}$=0.25 and 5 µm. S_i= 10^3 cm/s, S_c =10^7 cm/s with a 5 nm p+ top contact electron reflector.

References

1. Z. Fan, D.J. Ruebusch, A. A. Rathore, R. Kapadia, O. Ergen, P. W. Leu, A. Javey, Nano. Res. (2009) 829.
2. E. C. Garnett, M. L. Brongersma, Y. Cui, M. D. McGehee Annu. Rev. Mater. Res. (2011) 269.
3. B. Tian, T. J. Kempa, C. M. Lieber, Chem. Soc. Rev. 38 (2009) 16.
4. A. I. Hochbaum, P. Yang, Chem. Rev. 110 (2010) 527.
5. M. Law, J. Goldberger, P. Yang, Annu. Rev. Mater. Res. 34 (2004) 83.
6. V. Schmidt, J. V. Wittemann, U. Gosele, Chem. Rev. 110 (2010) 361.
7. H.J. Fan, P. Werner, M. Zacharias, Small 2 (2006) 700.
8. T. Stelzner, M. Pietsch, G. Andra, F. Falk, E. Ose, S. Christiansen, Nanotechnology 19 (2008) 295203.
9. K. Q. Peng, Y. Xu, Y. Wu, Y. J. Yan, S. T. Lee, J. Zhu, Small 1 (2005) 1062.
10. O. L. Muskens, J. G. Rivas, R. E. Algra, E. P. A. M. Bakkers, A. Lagendijk, Nano Lett. 8 (2008) 2638.
11. J. Zhu, Z. F. Yu, G. F. Burkhard, C. M. Hsu, S.T. Connor, Y. Q. Xu, Q. Wang, M. McGehee, S. H. Fan, Y. Cui, Nano Lett. 9 (2009) 279.
12. H. Stiebig, N. Senoussaoui, C. Zahren, C. Haase, J. Muller, Prog. Photovoltaics 14 (2006) 13.
13. L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, J. Rand, Appl. Phys. Lett. 91 (2007) 233117.
14. Y. B. Tang, Z. H. Chen, H. S. Song, C. S. Lee, H. T. Cong, Nano Lett. 8 (2008) 4191.
15. Z. Fan, R. Kapadia, P. W. Leu, X. Zhang, Y.-L. Chueh, Nano Lett. 10 (2010) 3823.
16. E. D. Kosten, E. L. Warren, H. A. Atwater, Opt. Expr. 19 (2011) 3316.
17. M. D. Kelzenberg, S. W. Boettcher, J. A. Petykiewicz, D. B. Turner-Evans, M. C. Putnam, E. L. Warren, J. M. Spurgeon, R. M. Briggs, N. S. Lewis, H. A. Atwater, Nat. Mater. 9 (2010) 239.
18. R. Kapadia, Z. Fan, A. Javey, Appl. Phys. Lett. 96, (2010), 103116.
19. B. M. Kayes, H. A. Atwater, N. S. Lewis, J. Appl. Phys. 97 (2005) 1901835.
20. K. R. Catchpole, S. Mokkapati, F. J. Beck, J Appl. Phys. (2011) 084519.
21. A. Wangperawong, S. F. Bent, Appl. Phys. Lett. 98 (2011) 233106.
22. M. D. Kelzenberg, M. C. Putnam, D. B. Turner-Evans, H.A. Atwater, Predicted Efficiency of Si Wire Array Solar Cells Proceedings of the 34th IEEE PVSC (2009)
23. M. D. Kelzenberg, D. B. Turner-Evans, B. M. Kayes, M. A. Filler, M. C. Putnam, N. S. Lewis, H. A. Atwater, Nano Lett. 8 (2008) 710.
24. M. C. Putnam, D. B. Turner-Evans, M. D. Kelzenberg, S. W. Boettcher, N. S. Lewis, H. A. Atwater, Appl. Phys. Lett. 95 (2009) 163116.

25. B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, C. M. Lieber, Nature 449 (2007) 885.
26. T. J. Kempa, B. Z. Tian, D. R. Kim, J. S. Hu, X. L. Zheng, C. M. Lieber, Nano Lett. 8 (2008) 3456.
27. M. C. Putnam, S. W. Boettcher, M. D. Kelzenberg, D. B. Turner-Evans, J. M. Spurgeon, E. L. Warren, R. M. Briggs, N. S. Lewis, H. A. Atwater, Energy & Environmental Science 3 (2010) 1037.
28. Z. Fan, H. Razavi, J. W. Do, A. Moriwaki, O. Ergen, Y.-L. Chueh, P. W. Leu, J. C. Ho, T. Takahashi, L. A. Reichertz, S. Neale, K. Yu, M. Wu, J. W. Ager, A. Javey, Nature Mater. 8 (2009) 648.
29. J. A. Czaban, D. A. Thompson, R. R. LaPierre, Nano. Lett. 9 (2009) 148.
30. E. C. Garnett, P. D. Yang, J. Am. Chem. Soc. 130 (2008) 9224.
31. E. C. Garnett, P. Yang, Nano Lett. 10 (2010) 1082.
32. C. A. Hoffman, K. Jarasuinas, H. J. Gerritsen, and A. V. Nurmikko, Appl. Phys. Lett. 33 (1978) 536.
33. Y. Rosenwaks, L. Burstein, Y. Shapira, and D. Huppert, Appl. Phys. Lett. 57 (1990) 458.
34. R. Cohen, V. Lyahovitskaya, E. Poles, A. Liu, and Y. Rosenwaks, Appl. Phys. Lett. 73 (1998) 1400.
35. C. Leguijt, P. Lolgen, J. A. Eikelboom, P. H. Amesz, R. A. Steeman, W. C. Sinke, P. M. Sarro, L. A. Verhoef, P. –P. Michiels, Z. H. Chen, A. Rohatgi, Solar Energy Materials and Solar Cells 34 (1994) 177.

4

Thin-Film Vapor-Liquid-Solid Growth

4.1 Introduction

III-V photovoltaics (PVs) have demonstrated the highest power conversion efficiencies for both single- and multi-junction cells[1,2,3]. However, expensive epitaxial growth substrates, low precursor utilization rates, long growth times, and large equipment investments restrict applications to concentrated and space photovoltaics (PVs)[4]. Here, we demonstrate the first vapor-liquid-solid (VLS) growth of high-quality III-V thin-films on metal foils as a promising platform for large-area terrestrial PVs overcoming the above obstacles. We demonstrate 1-3 μm thick InP thin-films on Mo foils with ultra-large grain size up to 100 μm, which is ~100 times larger than those obtained by conventional growth processes. The films exhibit electron mobilities as high as 500 cm^2/V-s and minority carrier lifetimes as long as 2.5 ns. Furthermore, under 1-sun equivalent illumination, photoluminescence efficiency measurements[5] indicate that an open circuit voltage of up to 930 mV can be achieved with our films, only 40 mV lower than what we measure on a single crystal reference wafer.

4.2 A Direct Thin-Film Path Towards Low-Cost Large-Area III-V Photovoltaics

The growth of semiconductor nanowires (NWs)[6,7,8,9,10] via the VLS growth mode and the epitaxial layer transfer[11,12] of semiconductors has proven to be very versatile, yielding a wide variety of materials on a multitude of substrates with excellent optoelectronic properties[9,10,13]. VLS-grown NWs exhibit circular or faceted cross-sections[14], depending on the surface energy constraints of the nucleation seed on the substrate. Shape- and geometry-controlled[15] nanowire growth using tubular templates has also been reported. Here, by utilizing a planar reaction template that (i) prevents dewetting of the growth seed from the substrate, and (ii) is permeable to the vapor phase, the VLS growth technique is extended to *thin film* geometries for the first time. InP is chosen as a prototypical model system to demonstrate the TF-VLS growth process as it not only has a near-optimal band gap for a single junction PV device[16], but is reported to have a low unpassivated surface recombination velocity[13,17,18,19], making it a promising material system for polycrystalline films-based optoelectronics. We show that large grain (up to 100 μm), continuous, polycrystalline

InP thin films are readily grown on Mo foils within a large growth parameter window, with optical and electronic properties approaching those of similarly-doped, single-crystalline InP.

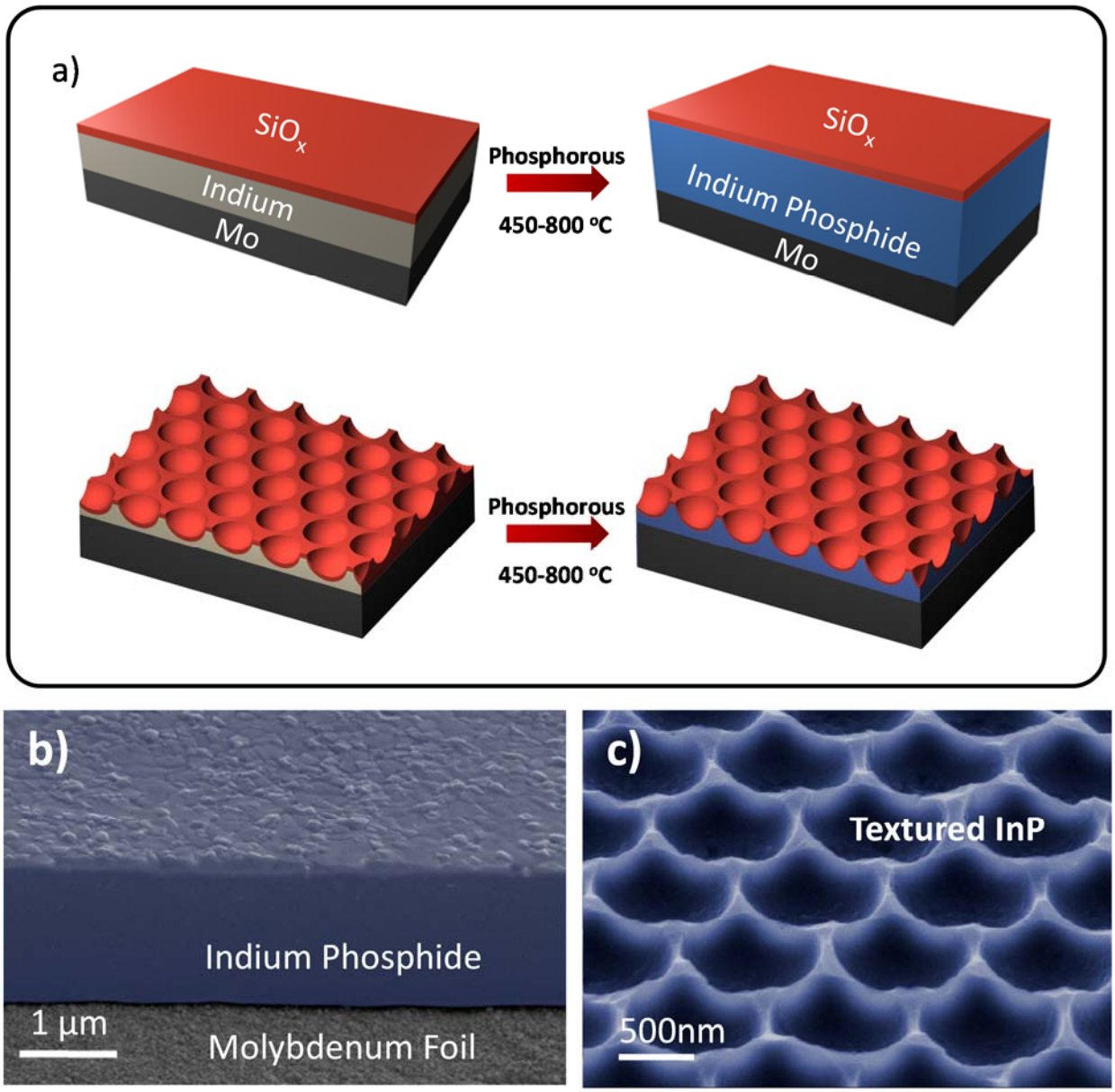

Figure 1: Growth technique and resulting InP films. a, Schematic view of the thin-film VLS growth technique for planar and textured InP films. **b**, 30° tilt view SEM of planar InP film on Mo foil, showing the InP surface, cross-section, and the Mo foil surface. **c**, Tilt view SEM image of contoured InP grown via pre-texturing the Indium film.

The TF-VLS process is schematically illustrated in Fig. 1a. Indium films (tunable thickness of 0.2-2 μm) are deposited on electropolished molybdenum foils (thickness of ~25 μm) by either electron-beam (e-beam) evaporation or electroplating, followed by e-beam evaporation of a 50 nm silicon oxide (SiO_x) cap. The Mo/In/SiO_x stack is then heated in hydrogen to a growth temperature of 450- 800 ºC, which is above the melting point of indium (~157 ºC). The thin SiO_x capping layer enables the liquid indium to maintain a planar geometry by preventing it from dewetting. After temperature stabilization, phosphorous vapor is introduced into the chamber, either by PH_3 gas or a heated red phosphorous solid source. The diffusion of phosphorous vapor through the capping layer and dissolution in the liquid indium results in the precipitation of solid InP crystals as predicted by the indium-phosphorus phase diagram. This process closely resembles the self-catalyzed VLS growth of nanowires[7], but instead produces continuous polycrystalline thin films. Figure 1b shows a tilt-view cross-sectional scanning electron microscope (SEM) image of a TF-VLS InP film on Mo foil. This image is representative of the film across the growth substrate. The as-grown InP film thickness is roughly double the original indium thickness (Fig. S1), matching the expected volume expansion from In to InP and implying near unit utilization of the indium film.

Interestingly, the morphology of the grown InP films can be tuned by the morphology of the starting In film and its corresponding template. As an example, an evaporated indium thin film was coated with closely packed silica beads (~1μm in diameter) through a Langmuir-Blodgett (LB) process (see Methods) followed by a mechanical press to embed the beads into the indium film. After subsequent capping by SiO_x and phosphorization, a nanotextured InP thin film with a hermispherical morphology was obtained (Fig. 1c). The ability to readily control the shape and morphology of the semiconductor film presents a unique feature of the TF-VLS process with important implications for light management[20,21] and carrier collection[22] in future devices.

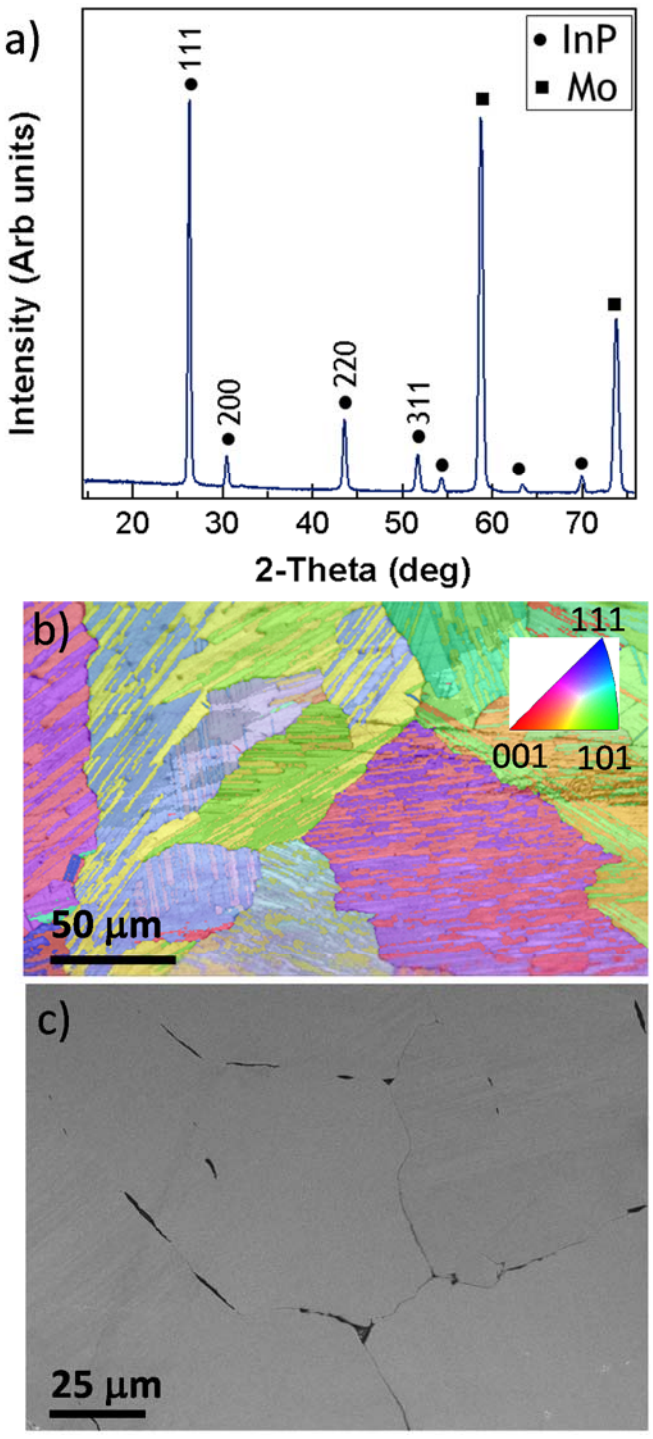

Figure 2: Structural characterization. a, XRD spectrum of an InP film grown at 750 ^{o}C. **b**, EBSD image of the backside of a peeled off TF-VLS InP film, indicating large grain sizes of ~10-100 µm. **c**, Top-view SEM image of InP peeled off from Mo foil, partially etched in 1% HCl to highlight grain boundaries.

The structural characteristics of the TF-VLS InP were probed by x-ray diffraction (XRD), electron backscatter diffraction (EBSD) and SEM. Both as-grown InP films on Mo and free standing InP films, which were obtained by peeling off the InP layer from the substrate, were examined. XRD analysis (Fig 2a) establishes three points. First, the films are zinc blende InP. Second, the lack of indium peaks indicates that, to the detection limit of the XRD, the film has turned entirely into InP. Third, the films are polycrystalline and slightly textured as evident by the larger 111 peak intensity as compared to that of 200. EBSD mapping of the InP films was used to determine the grain size. The maps (Fig. 2b) show that the grain sizes vary between 10 μm to greater than 100 μm, despite a film thickness of ~3 μm. These grains are 10-100 times larger than those previously reported for vapor phase growth of InP thin films on metal foils using metal organic chemical vapor deposition (MOCVD)[17] and close spaced sublimation[18]. The large crystal grain size obtained with TF-VLS leads to excellent optoelectronic properties as discussed in detail below. A plan view SEM image is shown in Fig. 2c; faceted edges of the grains are visible, providing further evidence of the large grain size.

Important features of the TF-VLS growth process are highlighted through a qualitative model (Fig. 3a). The process involves P diffusion through the SiO_x cap into the liquid indium film, increasing the P concentration, [P], until the concentration slightly exceeds saturation, $[P]_{Sat}$, enabling nucleation of the solid InP phase on the Mo substrate. It should be noted that InP does not nucleate on the SiO_x surface (Fig. S3) because of the high surface energy[23]. Once InP nuclei are formed, they grow via diffusion of nearby P to the In/InP interface, and subsequent incorporation into the solid phase. This diffusion/incorporation process creates a depletion zone near each nucleus, limiting subsequent nucleation events allowing large grain sizes. Growth continues until the entire In film becomes InP (Fig. 3b).

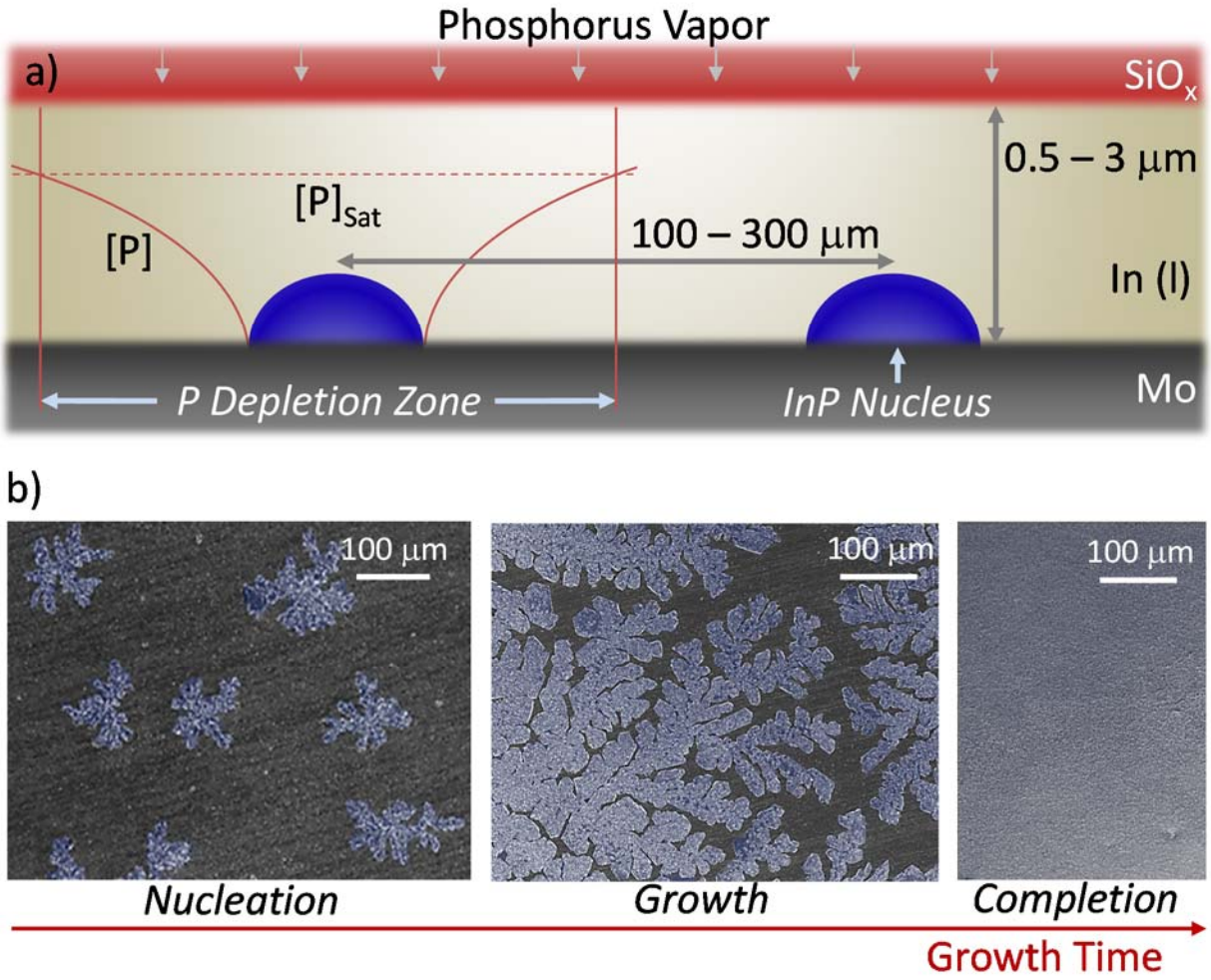

Figure 3: Growth schematic. a, Qualitative diagram of the TF-VLS growth process, showing the phosphorous vapor diffusing through the cap layer, initial InP nucleus, and phosphorus concentration [P] as a function of distance from the nucleus. The depletion zone is defined as the area where $[P]<[P]_{Sat}$. **b,** SEM images of the growth of the InP films. Initially, separate InP nuclei/islands form, followed by growth outwards in a dendritic fashion. Finally, separate InP islands converge together and growth completes as all In turns into InP.

A simple model helps to identify the factors that determine the density of nuclei (see Supplementary Information for details). The model suggests that the number density of nuclei scales as $(Fh^4/D)^{\alpha}$, where F is the flux of P into the liquid indium, D is the diffusivity of P within the liquid phase, h is the initial thickness of the indium film, and α is a positive constant less than one related to the critical nucleus size. Based on this simple scaling law, the key to producing a small number of nuclei and thus large grains is to insure that the flux of the incoming P is slow in comparison to the rate at which P diffuses within the liquid phase. Experimentally, the capping layer limits the flux of incoming P as the solid phase diffusivity through the SiO_x cap (estimated to be ~10^{-12} cm^2/s at 750 ^oC) is orders of magnitude lower than that in liquid indium (D~$1.2x10^{-4}$ cm^2/s).[24] When phosphorization of indium without the SiO_x cap is performed, grain size is drastically reduced to ~1 μm (Fig. S3) - an observation that supports the model and highlights the importance of the cap. Figure 3b shows SEM images at various stages of the film growth (*i.e.* different growth times). Starting with separate InP nuclei formation, spaced ~100-300 μm apart, the separate islands begin to converge, followed by the completion of film growth. The dendritic morphology[25] is indicative of the rapid diffusion of phosphorous towards the nuclei relative to the rate at which the solid phase relaxes towards its equilibrium shape[25]. These data further support the proposed growth mechanism and model.

Next, we focus on the detailed electrical and optical characterization of InP thin films (~3 μm in thickness) as a function of growth temperature (T_{Growth} =450-800 ^oC). After growth, the SiO_x cap was etched away in HF. Surface cleaning and passivation was then carried out by consecutive 30 second treatments of 1% HCl and 1% HNO_3. The HCl treatment removes the native oxide, while the HNO_3 treatment results in a dense surface oxide layer which is previously shown to improve the surface carrier properties[26]. The resulting films were characterized via Hall measurements, steady state photoluminescence (SSPL), time resolved PL (TRPL), and external luminescence efficiency measurements (η_{ext}).

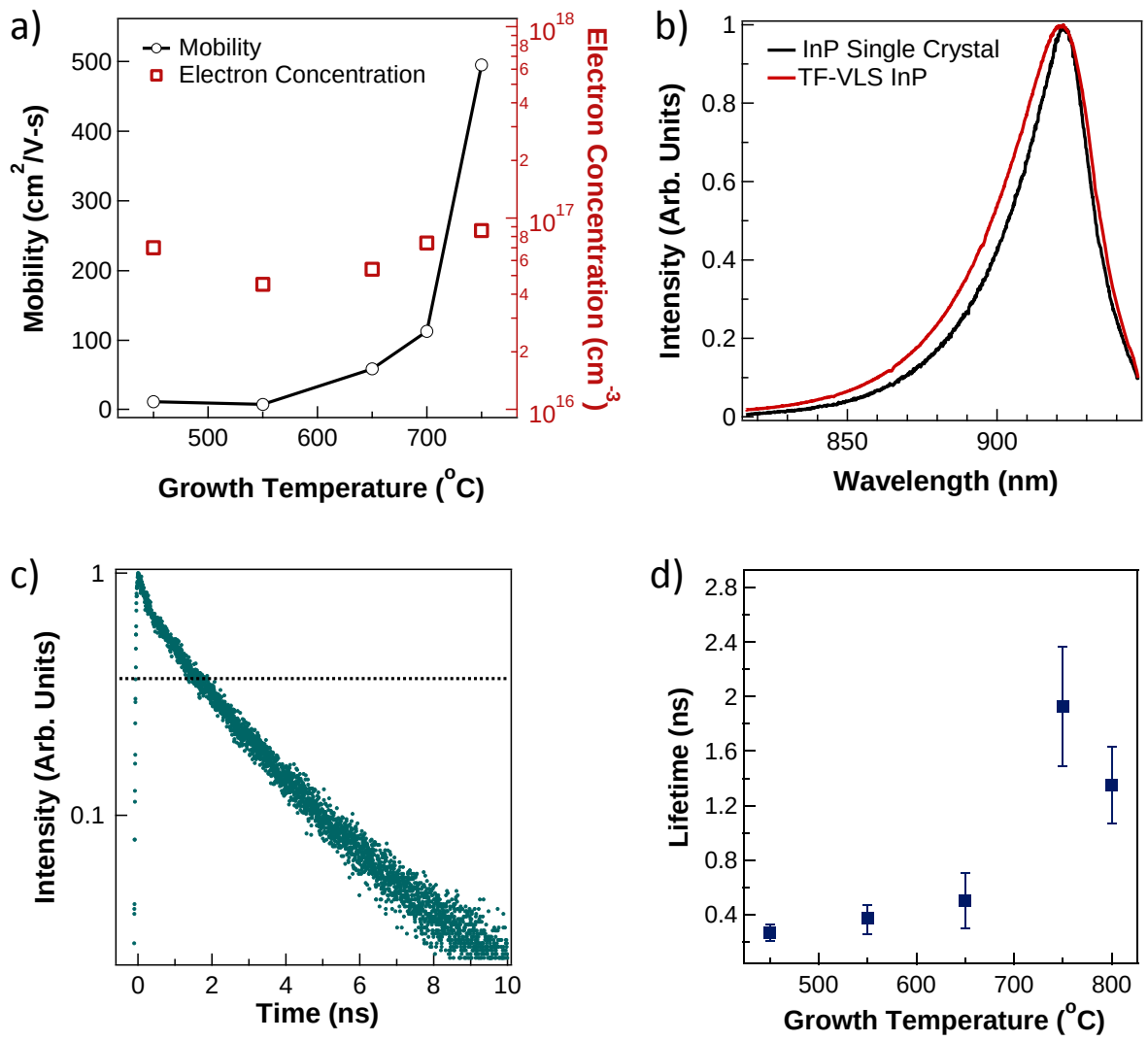

Figure 4: Optoelectronic characterization. a, Mobility and carrier concentrations as a function of growth temperature obtained from Hall measurements carried out on peeled off InP films. **b,** Steady state photoluminescence characterization of a TF-VLS InP film grown at 750°C (red line) and a similarly doped single-crystal wafer as a reference (black line). **c**, Representative TRPL curve for a TF-VLS InP sample grown at 750 °C. The dashed line represents 1/e of the initial peak intensity. **d**, Average time-resolved photoluminescence lifetimes as a function of InP growth temperature. All measurements were performed at room temperature.

Hall measurements (Fig. 4a) were carried out on InP films peeled off from the Mo substrate to extract carrier concentration and mobility. InP films were found to be *n*-type with an unintentional doping concentrations between 4 to 8×10^{16} cm^{-3}, regardless of growth temperature. Notably, this relatively low carrier concentration is obtained without the use of ultrahigh purity Mo foil and indium source. Electron mobility across multiple-grains (over an area of ~1 cm^2), however, exhibits a strong dependence on the growth temperature, increasing from ~12 cm^2/V-s for T_{Growth} = 450 ^oC, to ~500 cm^2/V-s for T_{Growth} = 750 ^oC. The electron mobility values for the optimal growth temperature approach those of single crystal InP, which range from ~1500-4000 cm^2/V-s depending on doping and compensation ratio[27].

Micro-SSPL was used to determine (i) the wavelength of the peak photoluminescence intensity, and (ii) the quantum yield of the emission, used to measure the external luminescence efficiency (η_{ext}) and calculate the quasi Fermi level splitting (ΔE_F). A representative polycrystalline InP (T_{growth}=750 ^oC) SSPL curve is shown in Fig 4b. As a reference, a single crystal *n*-type InP wafer with a comparable doping concentration (~3 x 10^{16} cm^{-3}) is also plotted. A HeNe laser at λ=632.8 nm was used as the excitation source and measurements were performed at ambient temperature. The polycrystalline InP exhibits a SSPL peak position of ~921.7 nm (1.345 eV) and full width half maximum (FWHM) of ~37 nm. These measured values are similar to the single crystal reference, which exhibits a peak position of 922.2 nm and a FWHM of 29 nm. TRPL measurements were carried out at room temperature on the polycrystalline InP films to determine the effective minority carrier lifetimes (Fig. 4c). The samples were illuminated with a 800 nm pulsed laser, and the time dependent photoluminescence intensity was recorded at the peak wavelength, as measured by SSPL. Figure 4d shows the 1/e lifetime as a function of InP growth temperature. The measured effective lifetimes show a clear dependence on the growth temperature, with the InP grown at 450 ^oC exhibiting the lowest average effective lifetime of ~0.25 ns, while the films grown at 750 ^oC exhibit the highest average effective lifetime of ~2 ns. We hypothesize that at higher temperatures, the InP is more thoroughly annealed during growth, reducing the excess number of point defects and thereby improving the electronic and optoelectronic properties.

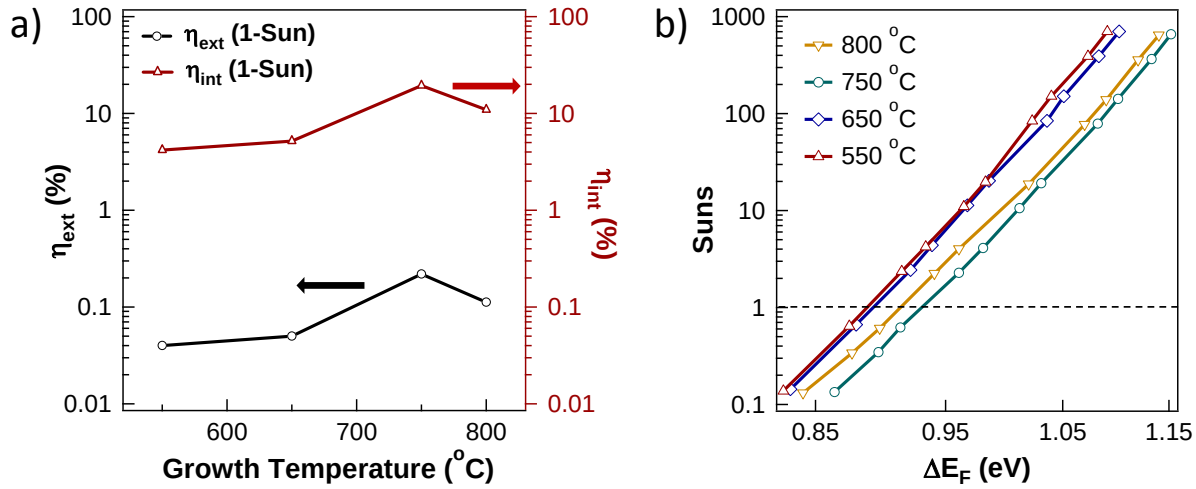

Figure 5: Luminescence yield. a, Measured external luminescence efficiency and extracted internal luminescence efficiency as a function of growth temperature. **b**, Optically measured "I-V" curves obtained from external luminescence efficiency measurements. Here, Suns represents the intensity of the absorbed laser light (1-sun = 100 mW/cm^2), and corresponds to the photogenerated current level. The quasi-Fermi level splitting (ΔE_F) represents the resulting V_{OC} that would occur to balance the photogenerated current.

While minority carrier lifetimes offer some insight into the material quality, the key metric for solar cell performance is the open-circuit voltage, V_{OC}[1,2]. In a semiconductor under illumination, the upper limit for V_{OC} is the difference in the chemical potential between the electron and hole population, defined as the quasi-Fermi level splitting, ΔE_F. Thus, extraction of ΔE_F allows for a quantitative prediction of the photovoltaic performance limits of a material. ΔE_F may be extracted[1] by direct measurement of the external luminescence efficiency, η_{ext} = (number of photons emitted)/(number of photons absorbed), as described in the methods section. The dependence can be qualitatively understood by considering that for a solar cell to reach the Shockley-Quessier (SQ) limit, the only loss mechanism should be radiative recombination[16]. Thus, at the SQ limit under open circuit conditions, one photon must be emitted for each photon absorbed (η_{ext}=100%)[1,2]. The η_{ext} is determined by two factors, the internal luminescence efficiency, η_{int} = (radiative recombination rate)/(total recombination rate), and the parasitic optical absorption. From the data obtained by varying incident laser intensity and monitoring the output photoluminescence intensity, we extract the external luminescence efficiency, internal luminescence efficiency, and quasi-Fermi level splitting (Fig. 5 and Fig. S4). Details of the measurement and analyses are provided in the methods section.

Figure 5a shows η_{ext} and η_{int} at 1-sun equivalent power as a function of InP growth temperature. As expected, the trend follows that of the measured minority carrier lifetimes in Fig. 4d, with the luminescence efficiency increasing as the growth temperature up to 750 °C. Importantly, the peak η_{ext} is ~0.2% and η_{int} is ~20%. These values compare favorably to other polycrystalline materials used in the state-of-the-art thin film cells, including copper indium gallium selenide (CIGS) and CdTe which exhibit η_{ext} between 0.0001 - 0.19%[2]. It should be possible to further increase the luminesce yields for TF-VLS InP by replacing the Mo foil with a more reflective back contact, while exploring various surface and grain boundary passivation techniques. Nevertheless, the obtained values confirm that TF-VLS growth results in optoelectronic quality InP; quite remarkable considering that the material was grown non-epitaxially on a metal substrate without the use of ultra-high purity materials.

Figure 5b shows the optically measured "I-V" curves for TF-VLS InP films. Specifically, the incident excitation intensity is plotted versus the extracted quasi-Fermi level splitting (ΔE_F) for various growth temperatures (see methods for analyses details). Here, the incident light intensity correlates to the photogenerated current level while $\Delta E_F/q$ represents the corresponding V_{OC} that would occur to balance the photogenerated current. This technique presents a simple approach for projecting the device performance limit of a given material. The data illustrates that InP samples grown at 750 ^oC exhibit a high ΔE_F of ~0.93 eV under 1-sun illumination. This extracted ΔE_F value is only ~40 meV lower than that of a single-crystalline InP wafer with a similar unintentional doping concentration ($N_d = 10^{16}$ cm^{-3}) measured using the same experimental set-up. Additionally, ΔE_F for the TF-VLS InP is higher than those previously reported for CIGS thin films (ΔE_F = 0.75–0.87 eV)[28]. This is an important observation given that the highest efficiency polycrystalline PVs reported to date have been based on CIGS; suggesting favorable performance projection for the TF-VLS InP. Additionally, the inverse slope of the incident light intensity versus ΔE_F curves is given as $\eta \ln(10) kT$, where η is the ideality factor (analogous to that of a diode), k is the Boltzmann's constant and T is the temperature. From the inverse slopes, we obtain η ~1.2 which is close to the ideal limit (where η=1), further suggesting the high optical quality of our material.

In conclusion, the ability to grow InP thin films on metal foils with ultra-large crystallites and material properties approaching those of single crystals presents a route towards low-cost, large-area III-V photovoltaics. Specifically, it should be noted that the TF-VLS process has important advantages in terms of processing costs, especially given the high material utilization yield for indium (which can be electrodeposited) as compared to conventional epitaxial growth processes, such as MOCVD/MOVPE. While in this work, we focused on the use of non-epitaxial metal foil substrates, the TF-VLS process also enables single crystalline film growth with epitaxial substrates. As a proof of concept, TF-VLS of homoepitaxial single-crystalline thin films of InP is demonstrated in the Supplementary Information (Fig. S5). These results demonstrate the versatility of this process for growth on both epitaxial and non-epitaxial substrates. Finally, although InP was utilized as a model system here, this growth technique should be general within the constraints presented here, and may be extended to a variety of other material systems in the future.

4.3 Experimental and Theoretical Details

4.3.1 Methods Summary

InP Growth: InP was grown from starting Mo/In/SiO_x stacks utilizing a 1-zone furnace with a phosphorus source of 10% PH_3 (99.9995%) in H_2 (99.9999%), or utilizing a 2-zone furnace with a red phosphorus (99.999%) source and H_2 carrier gas. Samples were first heated in a hydrogen environment, followed by exposure to the phosphorus source once the furnace stabilized at the growth temperature. Samples were held at the growth temperature and exposed to the phosphorous source for 20 minutes, followed by cooling (~20 seconds) to room temperature.

InP Transfer: For certain characterization work, including Hall measurements, InP was peeled from the Mo foil substrate. First, polyimide (PI) was spin coated onto the InP films, followed by thermal curing at 200 ^oC for 6 hours. Once the PI film was cured, the InP was removed from the Mo foil by mechanical peeling.

Indium Texturing via Langmuir-Blodgett: In order to grow patterned InP, a planar Mo/In stack was uniformly coated with a monolayer of 1 μm silica beads via a Langmuir-Blodgett process. First, the silica beads were dispersed in DI water; next, the Mo/In substrate was dipped into suspension and slowly removed. These beads were then mechanically pressed into the underlying indium.

Luminescence Yield: To simulate the response of these materials under varying solar illumination, samples were excited with a HeNe laser (λ=632.8nm) of varying intensity from ~15 mW/cm^2 (.15 suns) to ~7x10^4 mW/cm^2 (700 suns). This intensity represents the absorbed photon flux, calculated by multiplying the incident photon flux by the normal transmission coefficient, separately measured at the laser wavelength. The resulting external luminescence efficiency was calculated by: $\eta_{ext} = (\phi_{InP}/\ \eta_{sys})/\ (\phi_{inc} \times T)$ where ϕ_{inc} and ϕ_{InP} are the incident HeNe photon flux and the measured InP photon flux, respectively, T is the transmission coefficient at the air/InP boundary as measured via absorption measurements, and η_{sys} is the collection efficiency of the system for a Lambertian reference. Here, the Lambertian reference used was a thick (>3mm) Spectralon® layer was used as the Lambertian reference.

The internal luminescence efficiency, η_{int} is extracted via[29]:

$$(1) \quad \eta_{int} = \frac{\eta_{ext}(1 + 4Ln^2\alpha)}{1 + 4Ln^2\alpha\eta_{ext}}$$

where L is the InP thickness, n is the band-edge refractive index, and α is the band-edge absorption coefficient. It should be noted that Eqn. 1 assumes an ideal back surface mirror. In the experimental work, the back surface (*i.e.,* Mo substrate) is a non-ideal mirror which provides a loss mechanism for the emitted photons. Thereby, the extracted η_{int} values reported here are lower bounds.

The quasi-Fermi level splitting (ΔE_F) is calculated by[1]:

$$(2) \quad \Delta E_F = kT \ln\left(\frac{R_{abs}}{\int_0^{2\pi}\int_0^{\frac{\pi}{2}}\int_{-\infty}^{\infty} a(E,\theta)b(E)\cos(\theta)\, dE d\theta d\emptyset}\right) + kT \ln(\eta_{ext})$$

where R_{abs} is the absorbed photon flux per unit area in the InP, $a(E,\theta)$ is the absorbance of the semiconductor, and $b(E)$ is the blackbody spectrum at temperature T. The absorbance of the InP was taken to be: $a(E,\theta)= a(E)\times T(\theta)$, where $a(E)=1$ for $E>1.344$ eV, and $a(E)=0$ for $E<1.344$ eV. This simplifying assumption was made due to the relatively long optical path of the InP films here (3 μm). The angular dependence $T(\theta)$ is the transmission coefficient as determined by the Fresnel equations. The black body spectrum was given by: $b(E) = \frac{2n^2}{h^3c^2}E^2(\frac{1}{exp(\frac{E}{kT})-1})$. Here, n is the refractive index of air, h is Planck's constant, c is the speed of light, k is the Boltzmann constant, and $T=300$ K is temperature. It should be noted that since the surface is not truly random, nor flat, the assumption of Fresnel transmission at the top surface adds a small error of ~5 meV, which is a relative error of ~0.5%.

4.3.2 Thickness Control of TF-VLS InP

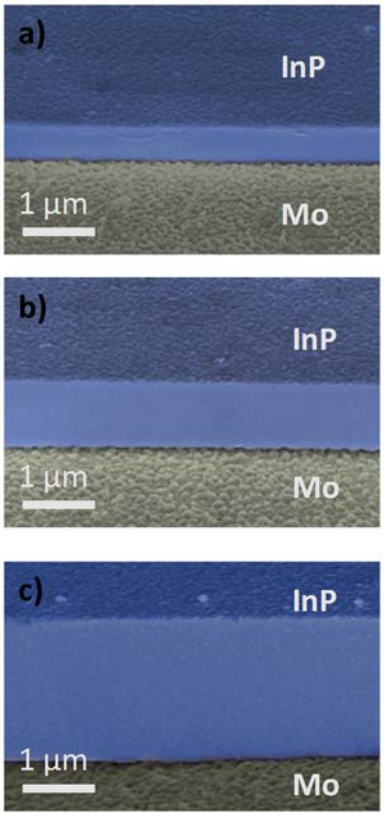

Figure S1. Thickness Control. 30º tilt view SEM images (false color) of TF-VLS grown InP of varying thickness, **a**, ~500 nm, **b**, 1 μm, **c**, 2 μm, obtained by varying the thickness of the initial indium layer (250 nm, 500 nm and 1 μm, respectively).

4.3.3 Control Experiment: Attempted phosphorization of indium on a *SiO_2 substrate*

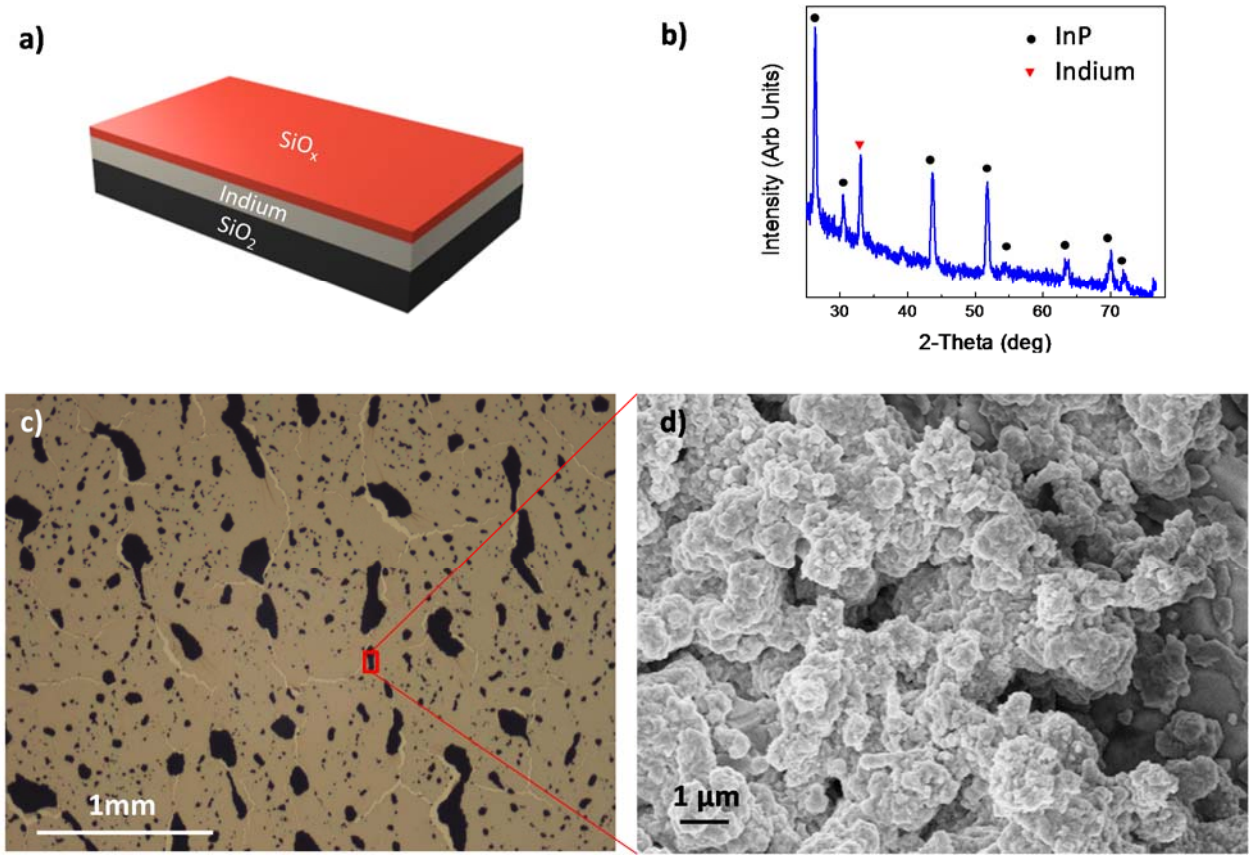

Figure S2. Attempted phosphorization of indium on a SiO_2 substrate (instead of Mo). a, Schematic of the starting SiO_2/In/SiO_2 substrate. **b**, XRD of the substrate after attempted phosphorization at 750 °C. In contrast to samples on a Mo substrate, the large indium peak indicates that a significant portion of the indium film has not turned into InP. **c**, Optical microscope image of the substrate after exposure to phosphorous. The indium clearly dewets from the SiO_2 surface, indicating that the surface energies of both sides of the template are high. **d**, SEM image of the resulting film showing morphology of the In/InP clumps. These results show that InP does not nucleate effectively on SiO_2.

4.3.4 Control Experiment: Phosphorization of indium *without* a SiO_x cap layer

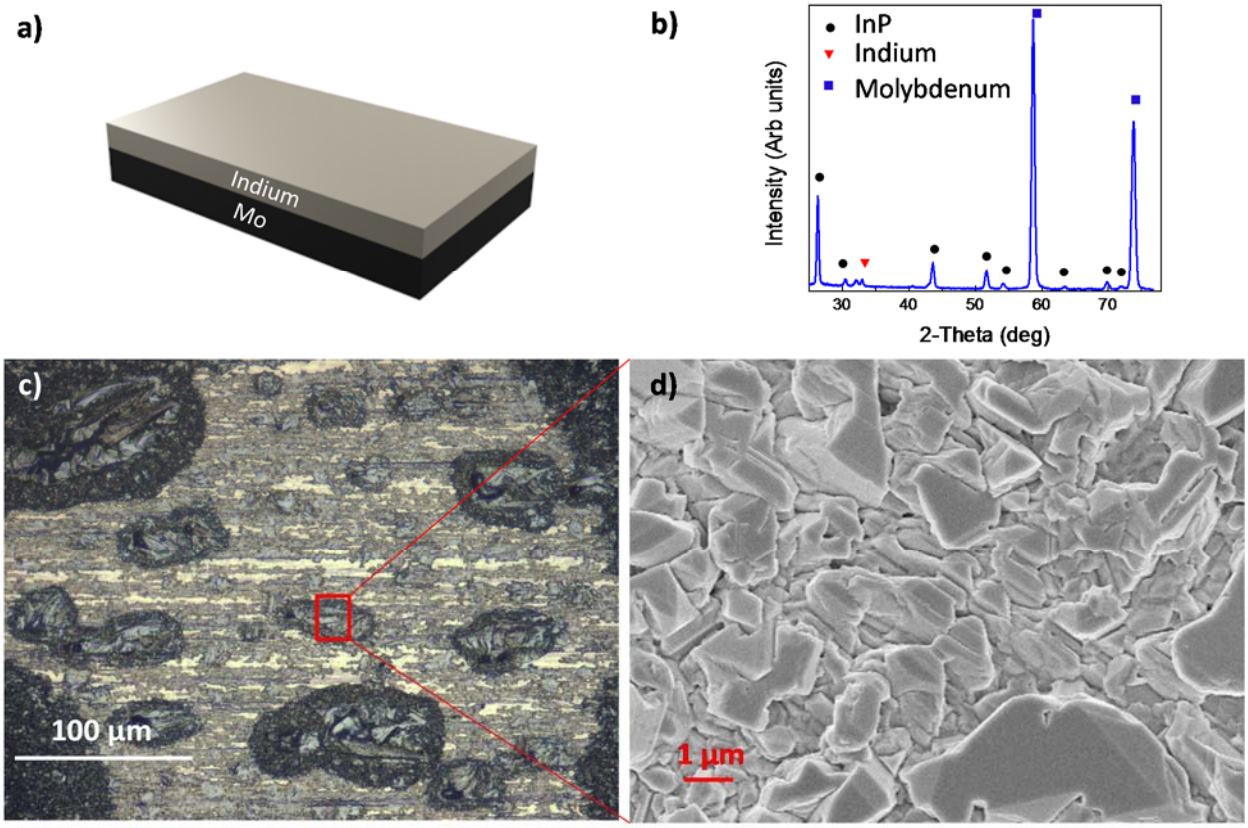

Figure S3. Phosphorization of indium without a cap. a, Schematic of a starting In/Mo substrate. **b**, XRD of In phosphorized *without* a SiO_x cap, depicting that majority of the indium has turned into InP. Trace amount of indium was left due to indium dewetting to form large aggregates which became difficult to fully phosphorize under the explored growth conditions. **c**, Optical microscope image of indium phosphorized without a cap. In contrast to TF-VLS growth *with* a SiO_x cap, indium clearly dewets from the Mo surface. **d**, SEM image of InP showing significantly smaller grain sizes compared to the TF-VLS grown InP *with* a cap. This is attributed to the much larger flux of P into the liquid indium during phosphorization *without* a cap.

4.3.5 Luminescence Yield

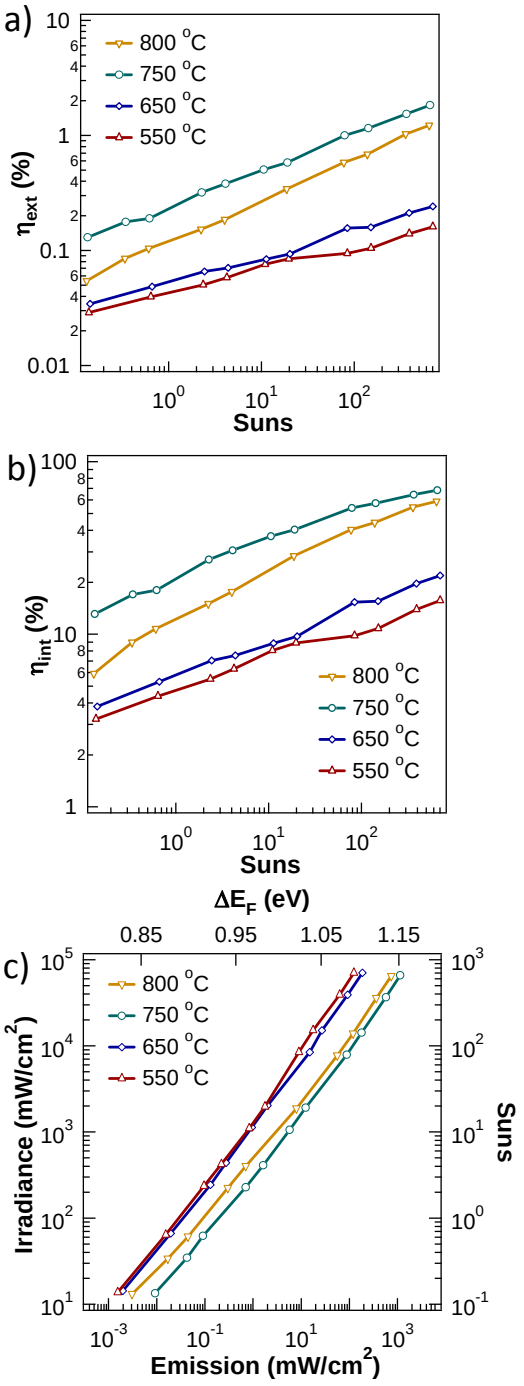

Figure S4: Luminescence Yield. a, The measured external luminescence efficiency as a function of incident photon intensity for multiple growth temperatures. **b**, The extracted internal luminescence efficiency as a function of incident photon intensity for different growth temperatures. **c,** Photons-in vs. photons-out curves for each growth temperature. The emission intensity is correlated to the quasi Fermi level splitting as discussed in the Methods section.

4.3.6 Single-Crystal InP TF-VLS Growth

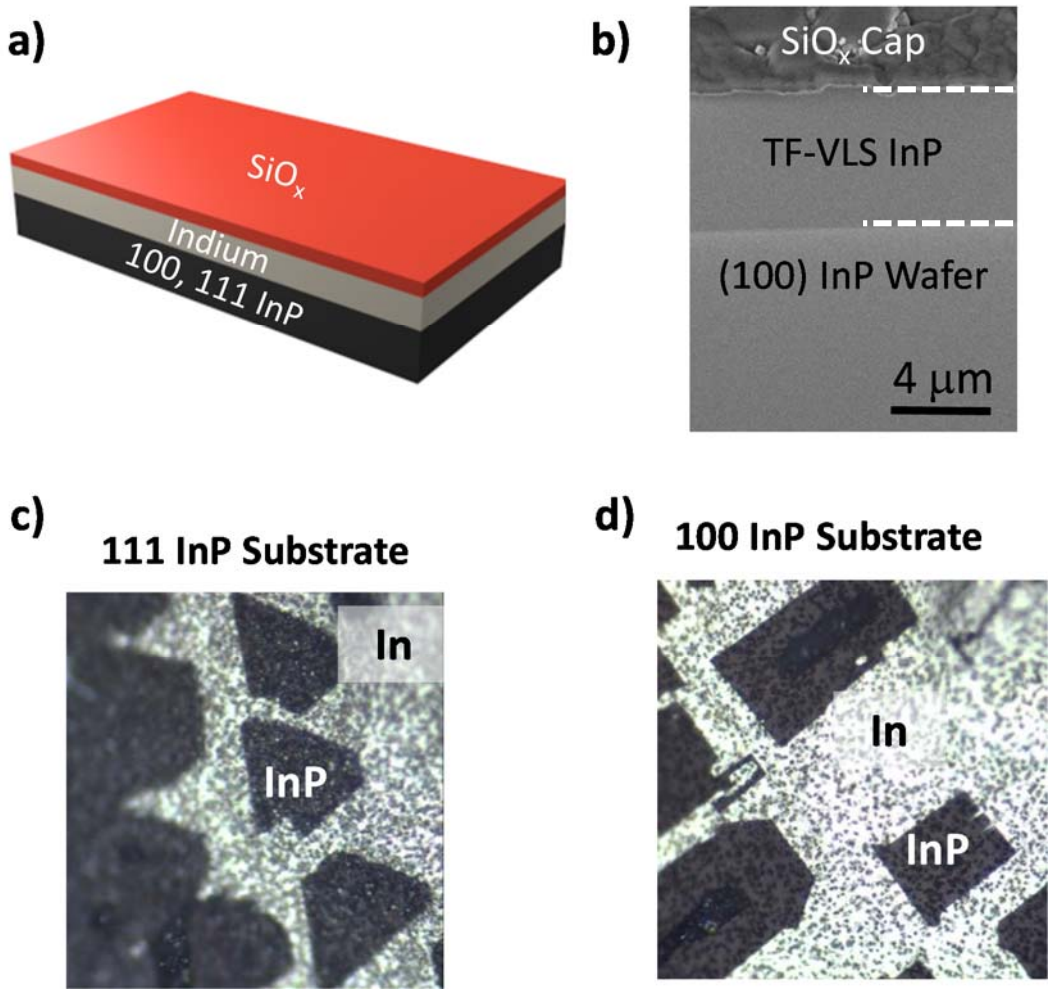

Figure S5: InP Epilayer Growth by VLS. a, Schematic of the initial growth stack. **b**, Cross-sectional SEM image of a fully grown (i.e., continuous) InP thin film grown on a (100) InP wafer using the TF-VLS process. **c, d,** Optical microscope images of *partially* grown InP on (111) and (100) InP substrates, respectively. The optical images depict the epitaxial relationship of the InP islands with the underlying substrate. Here the growth is stopped short on purpose to clearly depict the nucleation islands for each crystal orientation substrate.

4.3.7 Growth Scaling Law

The modeling of nucleation and growth poses a substantial theoretical challenge. However, certain scaling laws can be derived through simple arguments. In the present case, we wish to understand how experimentally controllable parameters might influence the density of nuclei we form during TF-VLS growth. We can construct and analyze simple coupled differential equations that govern the process, and use their solutions to guide our growth conditions.

We begin by assuming that phosphorous enters the liquid indium film at a steady state flux of F atoms/(cm^2-sec). We assume that the initial film thickness is *h* (in cm). One can define a characteristic time τ by the product $\tau = \left(F h^2\right)^{-1}$. Scaling all lengths in the problem by *h*, and scaling all times in the problem by τ, one can develop a dimensionless theory for the number of nuclei per unit volume. Let the dimensionless number density of nuclei in the film be N, and the dimensionless number density of excess P atoms (i.e. the number density P of atoms beyond the solubility limit) still within the liquid be n. Further, suppose that the critical nucleus contains η atoms and consequently, the nucleation rate depends on the excess concentration of P atoms raised to the power $\eta \geq 2$. The dimensionless equations governing growth can be written as:

$$\begin{aligned} \frac{dN}{d\theta} &= \tilde{D}\sigma_1 n^{\eta} \\ \frac{dn}{d\theta} &= 1 - \tilde{D}\bar{\sigma} n N - \eta \tilde{D}\sigma_1 n^{\eta} \end{aligned} \quad , \tag{S1}$$

where $\tilde{D}$ is the dimensionless diffusivity of P in the liquid In, σ_1 is a dimensionless parameter describing the capture cross section of the excess P atoms in the liquid by other P atoms in the liquid to form a new nucleus, $\bar{\sigma}$ is a dimensionless capture length characterizing the capture of the excess P atoms by the existing nuclei, and θ is the dimensionless time.

In the limit that nucleation has saturated one can assume a nearly steady state condition in which $\frac{dn}{d\theta} \approx 0$, and $\tilde{D}\bar{\sigma} n N << \eta \tilde{D}\sigma_1 n^{\eta}$. Under these conditions, Eqs. (S1) can be integrated to yield:

$$N = \left[(1+\eta)\tilde{D}^{1-\eta} \frac{\sigma_1}{\bar{\sigma}^{\eta}} \theta + C \right]^{\frac{1}{1+\eta}} , \tag{S2}$$

with C as the constant of integration. Assuming that the first term dominates the expression (certainly true in the case $\eta = 2$), the number of nuclei scales with $\tilde{D}^{\frac{1-\eta}{1+\eta}}$. Expressing the dimensionless diffusivity in terms of dimensioned quantities, one finds $\tilde{D} = \frac{D}{Fh^4}$ with *D* being the dimensioned diffusivity of P in the indium liquid. Rearranging, one concludes that the number density of nuclei scales according to $N \sim \left(\frac{Fh^4}{D} \right)^{\alpha}$, with $\alpha = \frac{\eta - 1}{\eta + 1}$.

References

1. Miller, O.D., Yablonovitch, E. & Kurtz, S.R., Strong Internal and External Luminescence as Solar Cells Approach the Shockley-Queisser Limit. *IEEE J. Phot.* **2**, 303-311 (2012).
2. Green, M.A. Radiative efficiency of state-of-the-art photovoltaic cells. *Prog. Photovolt: Res. Appl.* **20**, 472-476 (2012).
3. Green, M.A., Emery, K., Hishikawa, Y., Warta, W., & Dunlop, E.D. Solar cell efficiency tables (version 41). *Prog. Photovolt: Res. Appl.* **21**, 1 (2013).
4. Bosi, M. & Pelosi, C. The Potential of III-V Semiconductors as Terrestrial Photovoltaic Devices. *Prog. Photovolt: Res. Appl.* **15**, 1 (2007).
5. Yablonovitch E., & Miller, O.D. The Opto-Electronics of Solar Cells. *IEEE Phot. Soc. News* **27**, 4 (2013).
6. Morales, A.M. & Lieber, C.M. A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires. *Science* **279**, 208-211 (1998).
7. Wang, Z.L. & Song, J. Piezoelectric Nanogenerators Based on Zinc Oxide Nanowire Arrays. *Science* **312**, 242-246 (2006).
8. Mandl, B., Stangl, J., Hilner, E., Zakharov, A.A., Hillerich, K., Dey, A.W, Samuelson, L., Bauer, G., Deppert, K. & Mikkelsen, A. Growth Mechanism of Self-Catalyzed Group III-V Nanowires. *Nano Lett.* **10**, 4443-4449 (2010).
9. Gudiksen, M.S., Lauhon, L.J., Wang, J., Smith, D.C. & Lieber, C.M. Growth of nanowire superlattice structures for nanoscale photonics and electronics. *Nature* **415**, 617-620 (2002).
10. Fan, Z., Razavi, H., Do, J.-W., Moriwaki, A., Ergen, O., Chueh, Y.-L., Leu, P.W., Ho, J.C., Takahashi, T., Reichertz, L. A., Neale, S., Yu, K., Wu, M., Ager, J.W. & Ali Javey Three-dimensional nanopillar –array photovoltaics on low-cost and flexible substrates. *Nature Mater.* **8**, 648-653 (2009).
11. Tanabe, K., Fontcuberta i Morral, A., Aiken, D.J., Wanlass, M.W. & Atwater H.A. Direct-bonded GaAs/InGaAs tandem solar cell. *Appl. Phys. Lett.* **89**, 102106 (2006).
12. Zhai, Y., Mathew, L., Rao, R., Xu, D. & Banerjee, S.K. High-Performance Flexible Thin-Film Transistors Exfoliated from Bulk Wafer. *Nano Lett.* **12**, 5609 (2012).
13. Wallentin, J., Anttu, N., Asoli, D., Huffman, M., Aberg, I., Magnusson, M. H., Siefer, G., Fuss-Kailuweit, P., Dimroth,F., Witzigmann, B., Xu, H.Q., Samuelson, L., Knut, D., Borgstrom, M.T. InP Nanowire Array Solar Cells Achieving 13.8% Efficiency by Exceeding the Ray Optics Limit. *Science* **339**, 1057-1060 (2013).
14. Kuykendall, T., Pauzauskie, P., Lee, S., Zhang, Y., Goldberger, J. & Yang, P. Metalorganic Chemical Vapor Deposition Route to GaN Nanowires with Triangular Cross Sections. *Nano Lett.* **3**, 1063-1066 (2003).
15. Ergen, O., Ruebusch, D.J., Fang, H., Rathore, A.A., Kapadia, R., Fan, Z., Takei, K., Jamshidi, A., Wu, M. & Javey, A. Shape-Controlled Synthesis of Single-Crystalline Nanopillar Arrays by Template-Assisted Vapor-Liquid-Solid Process. *J. Am. Chem. Soc.* **132**, 13972-13974 (2010).
16. Shockley, W. & Queisser, H.J., Detailed balance limit of efficiency of p-n junction solar cells. *J. Appl. Phys.* **32**, 510-519 (1961).
17. Zheng, M., Yu, Z., Seok, T.J., Chen, T.-Z., Kapadia, R., Takei, K., Aloni, S., Ager, J.W., Wu, M., Chueh, Y.-L., Javey, A. High optical quality polycrystalline indium phosphide

grown on metal substrates by metalorganic chemical vapor deposition. *J. Appl. Phys.* **111**, 123112 (2012).
18. Kiriya, D., Zheng, M., Kapadia, R., Zhang, J., Hettick, M., Yu, Z., Takei, K., Wang, H.-H. H., Lobaccaro, P., & Javey, A. Morphological and spatial control of InP growth using closed-space sublimation. *J. Appl. Phys.* **112**, 123102 (2012).
19. Rosenwaks, Y., Shapira, Y. & Huppert, D. Evidence for low intrinsic surface-recombination velocity on p-type InP. *Phys. Rev. B* **44**, 13097-13100 (1991).
20. Liang, D., Huo, Y., Kang, Y., Wang, K. X., Gu, A., Tan, M., Yu, Z., Li, S., Jia, J., Bao, X., Wang, S., Yao, Y., Wong, H. –S. P., Fan, S., Cui, Y., & Harris, J. S. Optical absorption enhancement in freestanding GaAs thin film nanopyramid arrays. *Advanced Energy Materials* **2**, 1254-1260 (2012).
21. Zhu, J., Hsu, C. –M., Yu, Z., Fan, S., & Cui, Y. Nanodome solar cells with efficient light management and self-cleaning. *Nano Lett.* **10**, 1979-1984 (2010).
22. Kayes, B.M., Atwater, H.A. & Lewis, N.S. Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells. *J. Appl. Phys.* **97**, 114302 (2005).
23. Naritsuka, S. & Nishinaga, T. Epitaxial lateral overgrowth of InP by liquid phase epitaxy. *J. Cryst. Growth* **149** 314-318 (1995).
24. Srnanek, R., Habovcik, P., A method for diffusion coefficient determination of phosphorus in liquid indium. *J. Cryst. Growth* **46**, 55-58 (1979).
25. Bales, G.S., & Chrzan, D.C. Dynamics of irreversible island growth during submonolayer epitaxy. *Phys. Rev. B* **50**, 6057-6062 (1994).
26. Bertrand, P.A. XPS study of chemically etched GaAs and InP. *J. Vac. Sci. Technol.* **18**, 28-33 (1981).
27. Anderson, D.A., Apsley, N., Davies, P., & Giles, P.L. Compensation in heavily doped n-type InP and GaAs. *J. Appl. Phys.* **58**, 3059-3067 (1985).
28. Bauer, G.H., Bruggemann, R., Tardon, S., Vignoli, S. & Kniese, R. Quasi-Fermi level splitting and identification of recombination losses from room temperature luminescence in Cu(In1-xGax)Se2 thin films versus optical band gap. *Thin Solid Films* **480**, 410-414 (2005).
29. Schnitzer, I., Caneau C., Gmitter, T.J., Scherer, A. & Yablonovitch, E. 30% external quantum efficiency from surface textured, thin-film light-emitting diodes. *Appl. Phys. Lett.* **63**, 2174-2176 (1993).

5

Nanowire Connectors

5.1 Introduction

Electrical connectors based on hybrid core-multi-shell nanowire forests that require low engagement forces are demonstrated. The physical binding and electrical connectivity of the nanowire electrical connectors arise from the van der Waals interactions between the conductive metallic shells of the engaged nanowire forests. Specifically, the nanofibrillar structure of the connectors causes an amplification of the contact area between the interpenetrating nanowire arrays, resulting in strong adhesion with relatively low interfacial resistance. The nanowire electrical connectors may enable the exploration of a wide range of applications involving reversible assembly of micro- and macro-scale components with built-in electrical interfacing

5.2 Hybrid core-multi-shell nanowire forests for electrical connector applications

As the active areas of systems scale down, physical and electrical connectors based on conventional paradigms fail to provide the necessary performance due to issues of scalability.[1,2] Conventional reusable electrical connectors lack scalability due to separate mechanisms for electrical contact and physical engagement[3], or connector geometries that present significant challenges when scaling to sub mm regimes.[4,5] Synthetic gecko adhesives and other technologies that rely on chemical interactions can maintain adhesive performance down to the micro- to nano-scale[6-12], but lack the selectivity necessary for electrical connectors, which require contact between specific components in a system. Recently, hybrid core-shell nanowire (NW) forests were used to fabricate self-selective connectors that required low engagement/disengagement forces.[13] Here, we demonstrate *electrical* connectors based on hybrid core-multi-shell NW forests that use the same active area for electrical contact and physical adhesion, and require low engagement forces. The multishell structure allows control of both the shear adhesion and the

electrical properties. The strong shear adhesion of the connectors is due to the large contact area caused by interpenetration of the engaged NW forests, while the electrical connectivity is due to physical contact of the conductive outer shells. Thus, low engagement force electrical connectors with controllable adhesive and electrical properties are demonstrated.

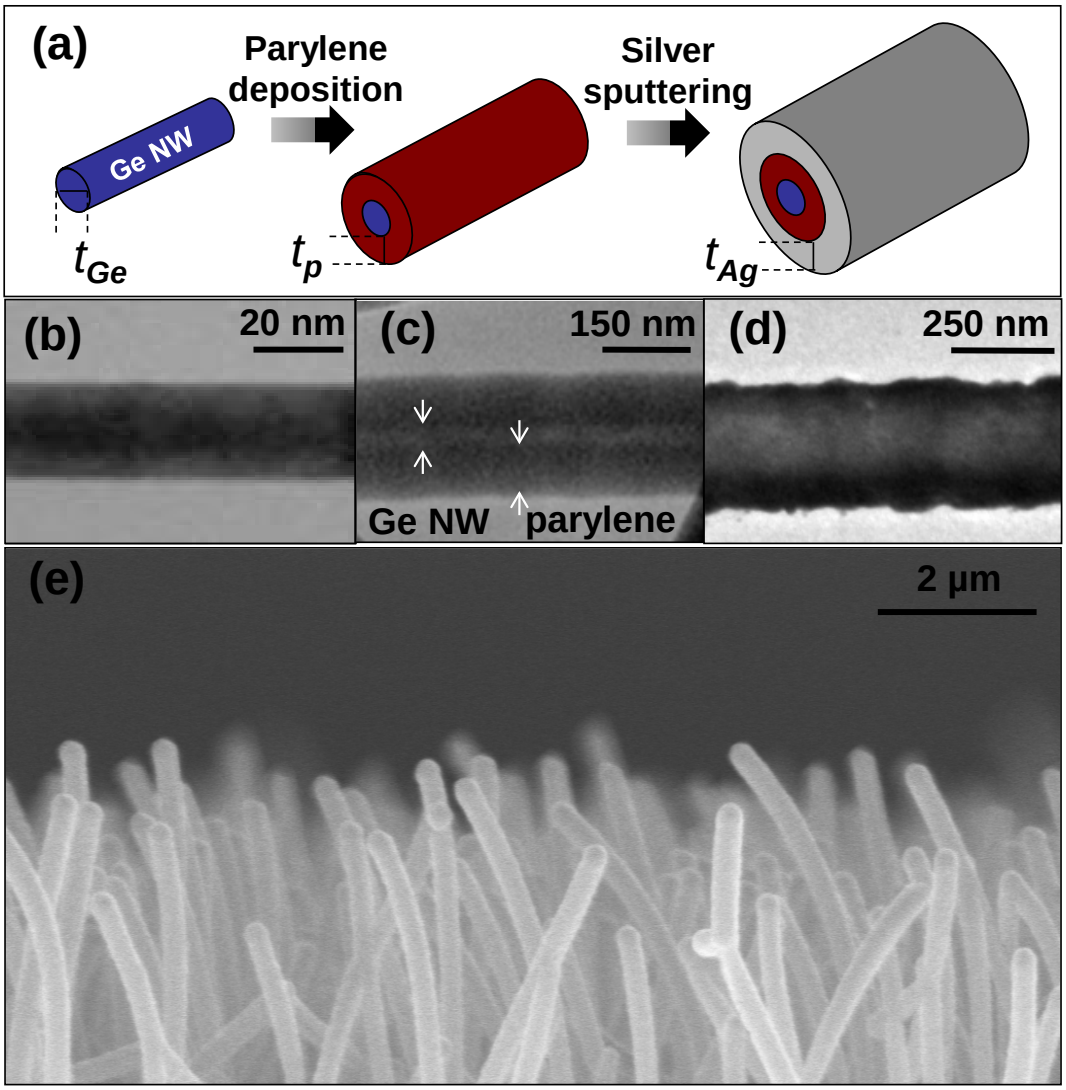

Figure 1. Ge/parylene/Ag core-multi-shell hybrid NW forests. (a) Illustration of the process flow used to fabricate the core-multi-shell NW forests. TEM images of (b) Ge NW, (c) Ge/parylene core/shell NW, and (d) Ge/parylene/Ag core-multi-shell NW. (e) SEM image of a representative core-multi-shell NW forest.

The NW electrical connectors are composed of hybrid core-multi-shell NW forests on silicon substrates, as illustrated in Fig. 1a. Ge NW forests were first grown by vapor-liquid-solid (VLS) method to make high-aspect-ratio nanofibrillar structures.[13,14] The density of the NW forests was 10-20 NWs/μm^2 at the base, and 1-2 NWs/μm^2 at the canopy. Next, parylene shells with varying thickness, t_p = 50-300 nm, were deposited on the Ge NW forests through gas phase deposition. Finally, a conformal silver shell with thickness, t_{Ag}=45 nm, was deposited via sputtering. The conformal coating of parylene and silver layers is confirmed by transmission electron microscopy (TEM) analyses of individual NWs (Fig. 1b-d). A scanning electron microscopy (SEM) image of a typical NW forest is shown in Figure 1c, clearly indicating the mainly vertical orientation and the uniform thickness of the NWs. Each of the components plays an essential role in achieving the desired functionality of NW electrical connectors. The Ge core (modulus ~100-150GPa)[15] provides: (i) a template upon which the shells can be deposited and (ii) prevents aggregation and/or collapse of the resulting structures. The parylene inner-shell enhances the surface compliance of the NW forests, therefore, increasing the total contact area and enhancing the adhesion. The Ag shell is required to enable electrical interfacing between the engaged NW forests.

The macro-scale shear adhesion of the NW electrical connectors was tested by first applying a normal preload force, F_N, to engage the connectors followed by the application of a shear force, F_S (Fig. 2a). This procedure was repeated with increasing F_S until the connectors separated. The shear adhesion strength corresponds to the maximum F_S held without failure. To demonstrate the importance of the parylene shell, we systematically studied shear adhesion as a function of t_p at a constant t_{Ag}=45 nm (Fig. 2b). The shear adhesion of NW connectors without parylene coating is <0.8 N/cm^2, while a parylene coating of t_p=50 nm increases the shear strength to ~30 N/cm^2 for a preload force of ~6.5 N/cm^2. This drastic enhancement of the shear adhesion strength with t_p is explained by an increase in the contact area between the engaged NW forests, resulting in increased van der Waals (vdW) interactions. The contact area between two parallel core-multi-shell NWs as a function of t_p can be calculated by using Johnson-Kendall-Roberts mechanics.[16] In detail, $P=\pi w^2 E_{NW}/(16R_{NW}(1-\nu^2)) - (\pi w W E_{NW}/2(1-\nu^2))^{0.5}$ was used to find the contact width w as a function of t_p, where P is the applied normal force per unit length, W is the work of adhesion, E_{NW} is the effective Young's modulus of the NWs, and R_{NW} is the radius of the NWs. The radius, R_{NW}, is the sum of the thicknesses of the three materials, $R_{NW} = t_{Ge}/2 + t_p + t_{Ag}$. The effective Young's modulus of the NWs were calculated by using $1/E_{NW} = (t_{Ge}/(2E_{Ge}) + t_p/E_p + t_{Ag}/E_{Ag})\times(1/R_{NW})$ with E_{Ge} = 103 GPa, E_p = 2.8 GPa, E_{Ag} = 78 GPa. The Poisson's Ratio, ν, was taken to be 0.35. The increase in contact area with t_p is clearly illustrated in Figure 3 for two parallel NWs with t_{Ge}=30 nm and t_{Ag}=45 nm, overlapping by 5 μm under a 200 nN normal force. The results demonstrate the importance of parylene inner-shell in achieving enhanced contact area[13] despite the fact that the polymeric shell is covered with an outer silver layer.

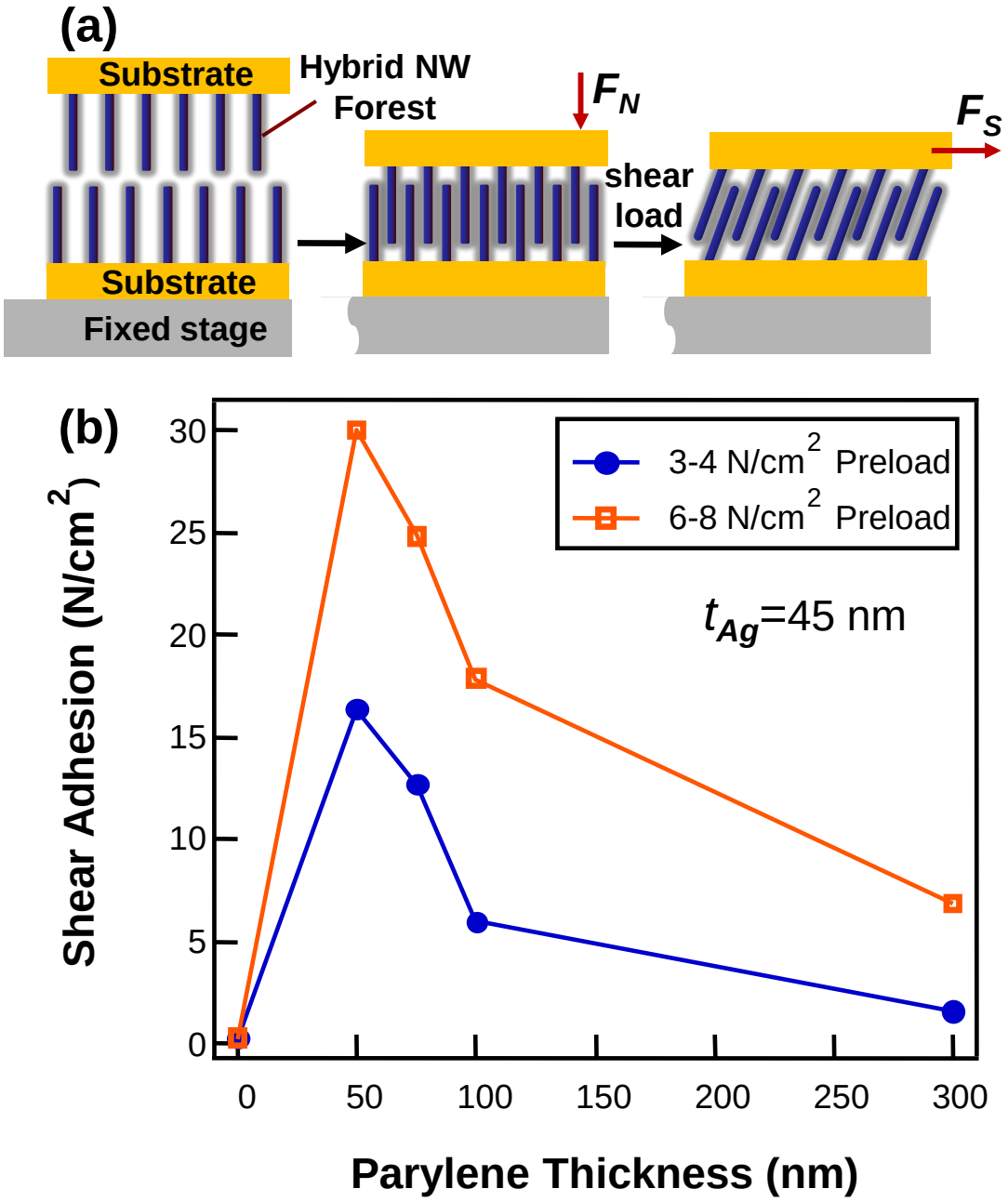

Figure 2. Macroscopic shear adhesion tests of NW electrical connectors. (a) Illustration of the method used to measure the shear adhesion strength. (b) Shear adhesion strength as a function of parylene shell thickness, t_p. Here, the silver shell thickness is maintained constant at t_{Ag}~45 nm.

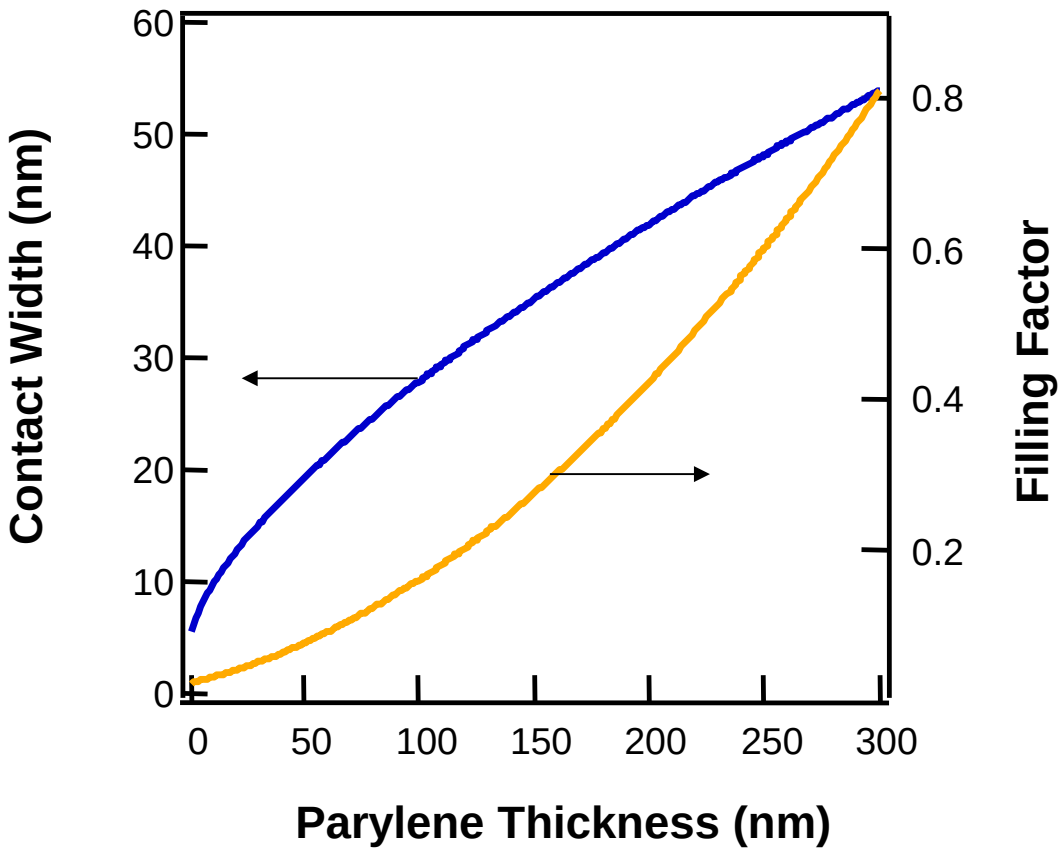

Figure 3. The calculated contact width between two parallel NWs with 5 μm overlap under a normal force of 200 nN (blue curve). The calculated filling factor (orange curve) as a function of t_p is also shown. Vertical NW density of 2 NW/μm^2 is assumed.

A decrease in the shear adhesion is observed for t_p>50 nm (Fig. 2b). This trend is attributed to a decrease in interpenetration depth (i.e., total contact area) for a given F_N due to an increase in the filling factor (*FF*) of the NW forests. The *FF* is estimated by using $FF = (\pi R^2 \times$ total # of NWs)/(total area), assuming perfectly vertical NWs (Fig. 3). Therefore, increasing t_p results in two competing effects – an increase in the surface compliance and an increase in the *FF*, resulting in the observed shear adhesion trend with a peak at t_p~50 nm. Our previous work on NW connectors also shows a similar trend.[13]

To further depict the importance of the parylene inner shell for obtaining high adhesion strength, control tests were carried out with t_p=0 nm while systematically increasing t_{Ag} from 45 nm to ~300 nm. In all cases, the adhesion was <2 N/cm^2 at a preload of ~4 N/cm^2. This low shear adhesion for NW connectors without a parylene coating clearly demonstrates the necessity of the parylene inner shell for achieving high shear adhesion.

The normal preload force (F_N) applied also affects the shear adhesion. As can be seen in Fig. 2b, an increase in the shear adhesion is observed with increasing F_N. This trend is attributed to the greater interpenetration depth of the NW forests with larger preload, resulting in higher effective contact area. Finally, the NW connectors provide highly specific binding with low adhesion to non self-similar surfaces (e.g., glass, planar parylene coated surfaces, and cloth) as previously demonstrated.[13] This is due to the relatively high stiffness of the NW connectors as compared to those used in synthetic gecko[12] adhesives. As a result, small contact area and low adhesion is observed when engaged with non self-similar surfaces. This selective adhesion is an important and highly desired characteristic of a connector technology.

In addition to the strong adhesion capabilities, the connectors are also electrically active due to the silver outer-shell. The performance of NW electrical connectors was investigated by measuring the electrical resistance in the engaged mode (Fig. 4a). The nominal contact area between the engaged connectors was ~25 mm^2. By applying voltages from 0 V to 0.5 V, *I-V* curves were generated and the resistance was directly extracted. A representative *I-V* characteristic for t_p=100 nm and t_{Ag}=45 nm NW connector is shown in the inset of Figure 4a, exhibiting ohmic behavior over the entire range of measurement. The resistance of the engaged connectors as a function of t_p (Fig. 4a) clearly indicates that the resistance of the connectors is not limited by the contact area between NW forests. Instead, the overall resistance is dominated by the parasitic resistances across the individual NW forests. To characterize the parasitic resistance, resistance across a single NW forest was measured as a function of length. For a connector of width ~ 5 mm, t_p=100 nm, and t_{Ag}=45 nm, the resistance per mm length scale was ~3 Ω/mm. This is attributed to the relatively thin Ag films used in this work. In particular, the Ag coating at the base of the NW forests is expected to decrease in thickness when thicker parylene films are used, which is consistent with the observed resistance versus t_p trend (Fig. 4a). In the future, further materials optimization is necessary to reduce the parasitic resistance across the NW forests.

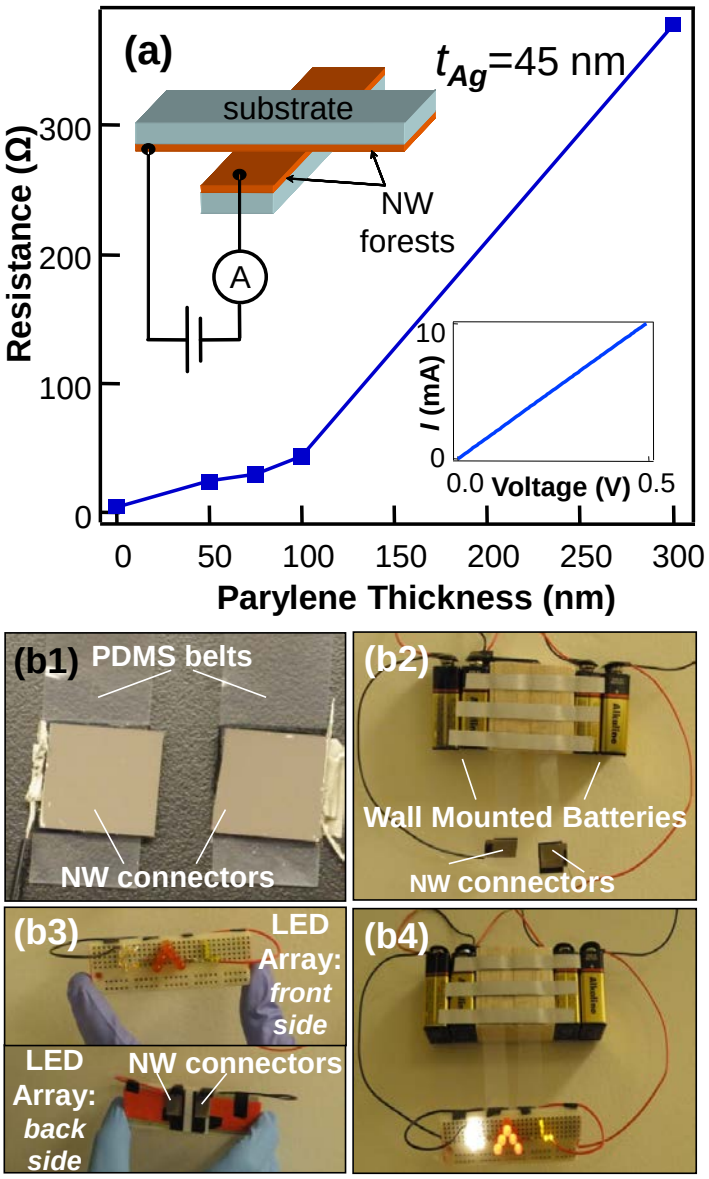

Figure 4. Electrical properties of the NW connectors. (a) Measured resistance as a function of t_p for connectors with ~25 mm^2 overlap. The inset shows the setup used to measure the resistance. A representative *I-V* curve for engaged connectors with t_p=100 nm and t_{Ag}=45 is also shown. (b1) NW electrical connectors are attached to two PDMS belts and (b2) electrically connected to a wall mounted battery array. (b3) Two complementary connectors are also attached to the back of an LED array. (b4) Once the connectors are engaged, the LED array is physically and electrically connected to the battery array, demonstrating the macroscale operation of the NW electrical connectors (enhanced online).

As a demonstration of a potential application of NW connectors, an LED array was connected to a wall-mounted battery array both physically and electrically by using NW electrical connectors (Fig. 4b). Two connectors were attached to the ends of two PDMS belts (Fig. 4b1), each of which was then connected to the negative and positive ends of a battery array (Fig. 4b2). Two additional connectors were attached to the back of an LED array and were electrically connected to the positive and negative ends (Fig. 4b3). By engaging the NW electrical connectors, the LED array was physically and electrically connected to the battery array (Fig. 4b4). The engaging and disengaging was repeated multiple times (Fig. 4b).

In conclusion, physical adhesion with built-in electrical interfacing is demonstrated by using hybrid core-multi-shell NW connectors. NW connectors allow for highly specific binding with low engagement forces arising from their nanofibrillar structure. The multi-shell configuration is required to simultaneously provide both the necessary surface compliance and electrical conductivity. Uniquely, the use of multi-component NWs allows for the precise control and engineering of the connector properties, a feature that is attractive for making connectors optimally suited for a wide range of technological applications.

References:

1. M. Yim, Y. Zhang, K. Roufas, D. Duff, C. Eldershaw, IEEE/ASME Trans. Mechatron. **7**, 442 (2002).
2. M. B. Cohn, K. F. Böhringer, J. M. Novorolski, A. Singh, C. G. Keller, K. Y. Goldberg, R. T. Howe, Proc. SPIE **3511**, 2 (1998).
3. B. Chan, P. Singh, Proc. 46th IEEE Elec. Comp. Tech. Conf. 460 (1996).
4. Electrical Contacts: Principles and Applications; P. G. Slade/Editor; Marcel Dekker; New York, NY 1999.
5. M. Braunovic, V. Konchits, N. Myshkin, Electrical Contacts: Fundamentals, Applications and Technology; CRC Press; Boca Raton, FL 2007.
6. E. Arzt, S. Gorb, R. Spolenak, Proc. Natl Acad. Sci. USA **100**, 10603 (2003).
7. M. Murphy, B. Aksak, M. Sitti, J. Adhesion Sci. Technol. **21**, 1281 (2007).
8. Y. Zhao, T. Tong, L. Delzeit, A. Kashani, M. Meyyappan, A. Majumdar, J. Vac. Sci. Technol. B **24**, 331 (2006**)**.
9. L. Qu, L. Dai, Adv. Mater. **19**, 3844 (2007).
10. L. Ge, S. Sethi, L. Ci, P. M. Ajayan, A. Dhinojwala, Proc. Natl Acad. Sci. USA **104**, 10792 (2007).
11. J. Lee, R. S. Fearing, K. Komvopolous, Appl. Phys. Lett. **93**, 191910 (2008).
12. K. Autumn, Y. A. Liang, S. T. Hsieh, W. Zesch, W-P. Chan, W. T. Kenny, R. Fearing, R. J. Full, Nature **405**, 681 (2000).
13. H. Ko, J. Lee, B. E. Schubert, Y. Chueh, P. Leu, R. S. Fearing, A. Javey, Nano Lett. ASAP DOI: 10.1021/nl900343b (2009).
14. A. Javey, ACS Nano, **2**, 1329, (2008).
15. L. T. Ngo, D. Almécija, J. E. Sader, B. Daly, N. Petkov, J. D. Holmes, D. Erts, J. J. Boland, Nano. Lett. **6**, 2964 (2006).
16. K. L. Johnson, K. Kendall, A. D. Roberts, Proc. R. Soc. London. A. **324**, 301 (1971).

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