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Design and Analysis of Digitally Modulated Transmitters for Efficiency Enhancement

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Design and Analysis of Digitally Modulated Transmitters for Efficiency Enhancement

by

Lu Ye

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University of California, Berkeley

Committee in charge:

Professor Ali M. Niknejad, Chair
Professor Elad Alon
Professor Paul Wright

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Abstract

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The last decade has witnessed a tremendous growth in wireless communications. Consumer demands for battery-operated mobile devices with versatile, high data-rate communication capabilities that are of low cost, small form-factor and long operating cycle have motivated the research on fully-integrated, back-off-efficient and coexistence-friendly wireless transceivers in CMOS VLSI technology. However, the full integration of an efficient CMOS power amplifier (PA) into such a transceiver is still among the most difficult challenges towards a true System-On-Chip (SOC) solution. This thesis investigates the PA efficiency enhancement techniques for a complete power transmitter system that is fully-integrated and coexistable. Direct digitally modulated transmitter architecture has been identified as one of the most promising solutions to the above challenges. Within such a transmitter, the PA efficiency is able to back off from a high peak efficiency at least with class-B characteristic; meanwhile, the transmit linearity can be more easily improved by digital predistortion due to the direct digital modulation scheme. To validate such a promising architecture, we have built a fully-integrated CMOS digital power transmitter for the IEEE 802.11g 54Mbps application. System-level considerations and design choices are presented with an aim for low out-of-band noise and good transmit linearity. As the core of the transmitter, the RF switching PA is designed for high efficiency with minimum number of on-chip passives that only exercise an accurate control over fundamental and second-harmonic terminations. The class-B efficiency back-off characteristic is further improved by a dynamic impedance modulator which boosts the PA drain impedance at a low instantaneous envelope level. Open-loop phase interpolator based topology is used for the polar phase modulator, which achieves wideband phase modulation with competitive power consumption. Digital baseband filtering is fully optimized at both the algorithm and the hardware level, which offers larger than 60dB attenuation on the close-in spectral images with reduced filter complexity. The prototype has been implemented in a 65nm bulk CMOS technology and has demonstrated a combination of good output power, overall efficiency and spectral purity with a very high level of system integration.

To the loving memory of my maternal grandfather (2000), grandmother (2013), and my mother-in-law (2008).
To the memory of the good, old days.

Contents

List of Figures

List of Tables

Acknowledgments

Although it took me six years to get help and support from various sources to complete my PhD, it only takes me more than one page to acknowledge those who have made this happen. Therefore this acknowledgment is never going to be complete; nor is it enough to fully express my gratitude.

First of all, my faculty advisor, Prof. Ali M. Niknejad. He is knowledgeable and has a logical and rigorous way of technical thinking. I appreciate the opportunity of being part of his research group and working with him on interesting topics. A true gentleman, Ali is always calm, patient and considerate. In fact, he has almost all the characteristics I would picture out of a "good person" in a well-cultivated society. I am as impressed by his nice personality as by his academic vision. Being treated nicely, I have gradually learned to "be nicer" to others.

I want to thank Prof. Elad Alon, who has also taken the time and the pains to improve my work which was sometimes not solid, my oral presentation which was always awkward, and my paper draft which was often poorly organized. Advising on the digital transmitter project, Elad has made millions of challenges to my technical statements, which urged me to re-examine my understandings and make my work more compelling. For some of my drafts for paper submissions, Elad almost edited every single sentence (if he was not completely rephrasing it); the fact that he (as well as Ali) is not giving up the effort of helping me out is one of the reasons I myself did not give up during difficult times.

Prof. Paul Wright has kindly agreed to serve on my dissertation committee and I really appreciate his valuable time and feedback. Upon his first read, he shared with me some harsh criticisms, which, in addition to making me feel really bad, helped to improve the readability and organization of this dissertation.

I have been very fortunate to work with a group of brilliant and fun students at Berkeley Wireless Research Center (BWRC). We have gone through tough tapeouts together and also enjoyed lots of fun all through. Especially I want to thank Debo Chowdhury for setting an excellent example in research and technical communication which I can only approach over my entire career. A complete enumeration would not be practical here; but once again I want to thank the BWRC folks and wish you all the best. I truly hope our paths will cross sometime in the future.

Many thanks to my friends from Peking University as well my "Cedar 2008" housemates. I cherish the enjoyable times with you.

This dissertation has been completed in a rush within two weeks (dear committee members, please do not disapprove it simply because this short length of time!). Also on my plate is another hard cutoff at the company, perhaps even harder than 60dB per decade. My supervisor, Julian Tham, has generously allowed me to interleave work with dissertation writing. Without Julian's support, I can easily screw up either one. I also want to acknowledge the supervision from Ali Afsahi in the same company; working with him during my internship has exposed me to the various real-world transmitter issues that are sometimes not easily encountered in academia.

I dedicate this dissertation to the whole of my family, without whose unconditional love and enduring support this work would have never been possible. My passed maternal grandfather (2000), my grandmother (2013) and my mother-in-law (2008), I miss you from the bottom of my heart and I am sure you will be proud of my achievement. Last, but never the least, my wife; please continue to "be my co-driver", whenever and wherever.

Part I

Introduction and Background Studies

Chapter 1

Introduction

The last decade has seen a spectacular surge in the wireless industry, and wireless connectivity has now become an indispensable ingredient of everyday life. The trend has been partially fueled by the recent explosive growth in the popularity of mobile devices featuring personal computing as well as versatile, high data rate communication capabilities such as Long Term Evolution (LTE) and Wireless Local Area Network (WLAN). As seen in Fig. 1.1, the mobile data traffic is forecast to expand by 35x from 2009 to 2014. Meanwhile, a vast plethora of other applications such as gaming, multimedia streaming and home networking have also motivated the development of low-cost and high data-rate radios.

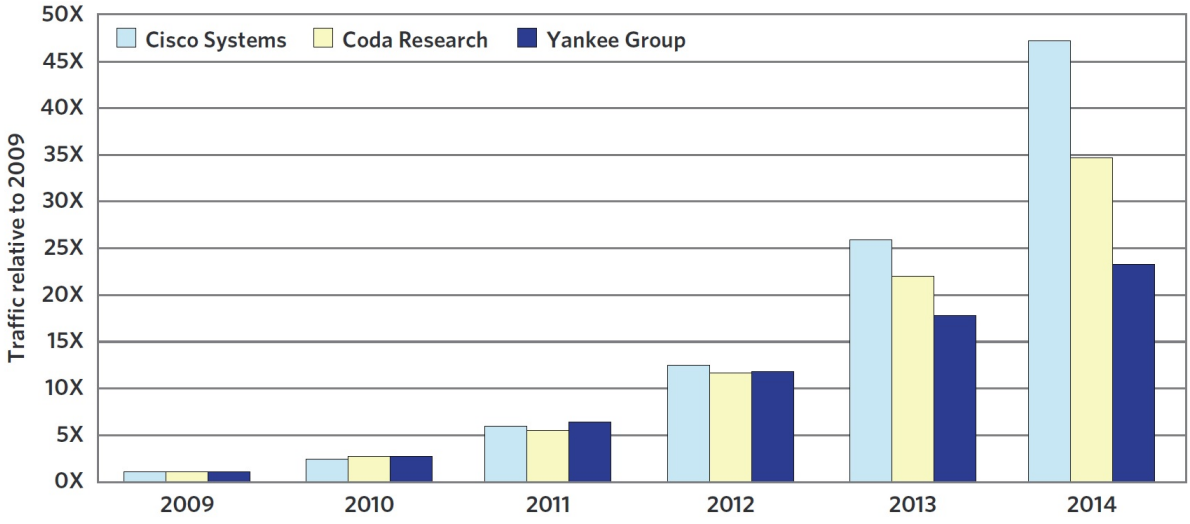


Figure 1.1: Industry forecast of mobile data traffic from 2009 to 2014 ([1]).

Driven by the need for high data-rates in spite of a highly crowded spectrum (Fig. 1.2), the modulation schemes for various wireless standards have evolved towards spectrally-efficient (e.g. Orthogonal Frequency Division Multiplexing (OFDM)) and higher-order (e.g. 256-

QAM as opposed to BPSK) ones. For example, IEEE 802.11ac, an amendment to the 802.11-2007 standard (including 802.11a/b/g/n), offers a peak throughput of 200Mbps within 40MHz channel bandwidth; if BPSK modulation is used on the per-sub-carrier basis as opposed to 256-QAM, it can only support 15Mbps over the same bandwidth (Fig. 1.3). The improved spectral efficiency in the frequency domain comes at the expense of an increased Peak-to-Average-Power-Ratio (PAPR) in the time domain. For 802.11ac OFDM signals of 40MHz bandwidth, for example, the theoretical PAPR (as calculated by Eq.(1.1), where $N_{sub,tr}$ is the number of carriers transmitting data) is 20.6dB.

$$\text{PAPR} = 10 \times \log_{10}(N_{sub,tr}) \qquad \text{[dB]} \tag{1.1}$$

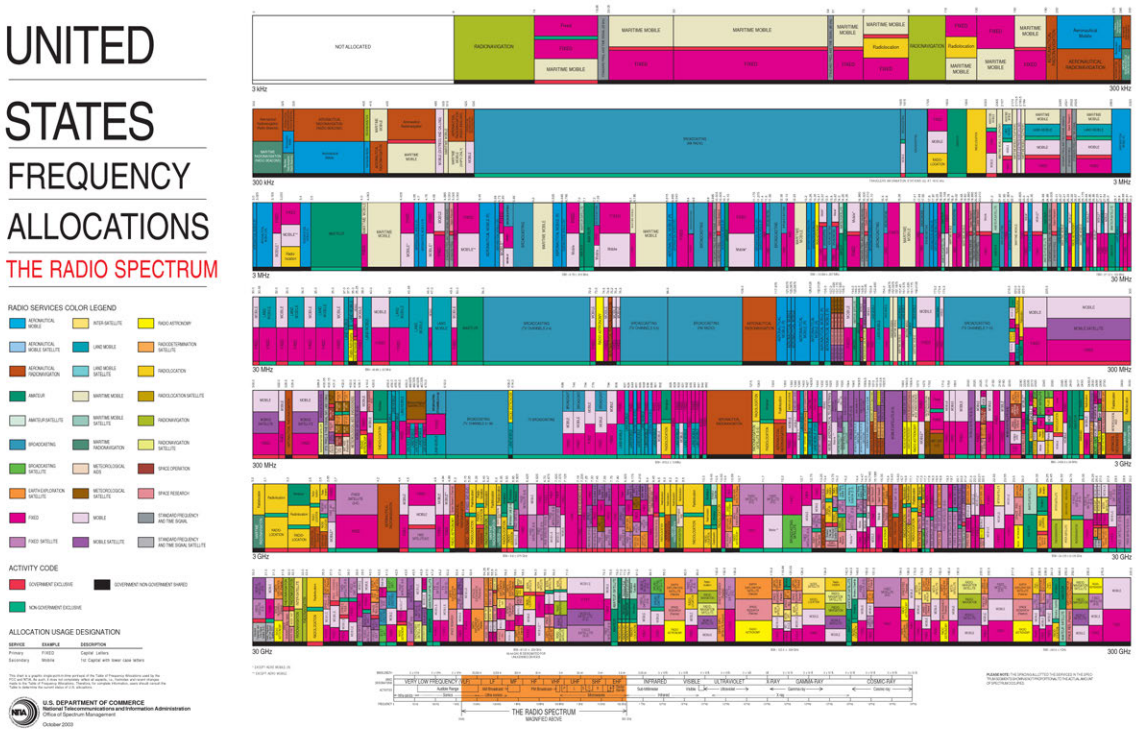


Figure 1.2: United States frequency allocations.

In contrast to constant envelope modulation, such as Quadrature Phase Shift Keying (QPSK), high-PAPR modulations typically require a highly linear power amplifier (PA) (Fig. 1.4). This is typically achieved by employing a class-A PA with a large back-off from its saturated output power (P_{sat}). Due to the efficiency loss associated with the large back-off, the average power efficiency is severely compromised. With the fast-growing data rates, this issue has become increasingly problematic for battery-operated mobile devices, because the PA is often times the most power hungry within a wireless transmitter (TX). To extend

Theoretical throughput for single Spatial Stream (in Mb/s)										
MCS index	Modulation type	Coding rate	20 MHz channels		40 MHz channels		80 MHz channels		160 MHz channels	
			800 ns GI	400 ns GI	800 ns GI	400 ns GI	800 ns GI	400 ns GI	800 ns GI	400 ns GI
0	BPSK	1/2	6.5	7.2	13.5	15	29.3	32.5	58.5	65
1	QPSK	1/2	13	14.4	27	30	58.5	65	117	130
2	QPSK	3/4	19.5	21.7	40.5	45	87.8	97.5	175.5	195
3	16-QAM	1/2	26	28.9	54	60	117	130	234	260
4	16-QAM	3/4	39	43.3	81	90	175.5	195	351	390
5	64-QAM	2/3	52	57.8	108	120	234	260	468	520
6	64-QAM	3/4	58.5	65	121.5	135	263.3	292.5	526.5	585
7	64-QAM	5/6	65	72.2	135	150	292.5	325	585	650
8	256-QAM	3/4	78	86.7	162	180	351	390	702	780
9	256-QAM	5/6	N/A	N/A	180	200	390	433.3	780	866.7

Figure 1.3: Theoretical throughputs of a single spatial stream for IEEE 802.11ac.

battery life, the TX must be efficient not only at peak power but also at backoff. TX efficiency enhancement at back-off powers has therefore become one of the key research focuses in recent years.

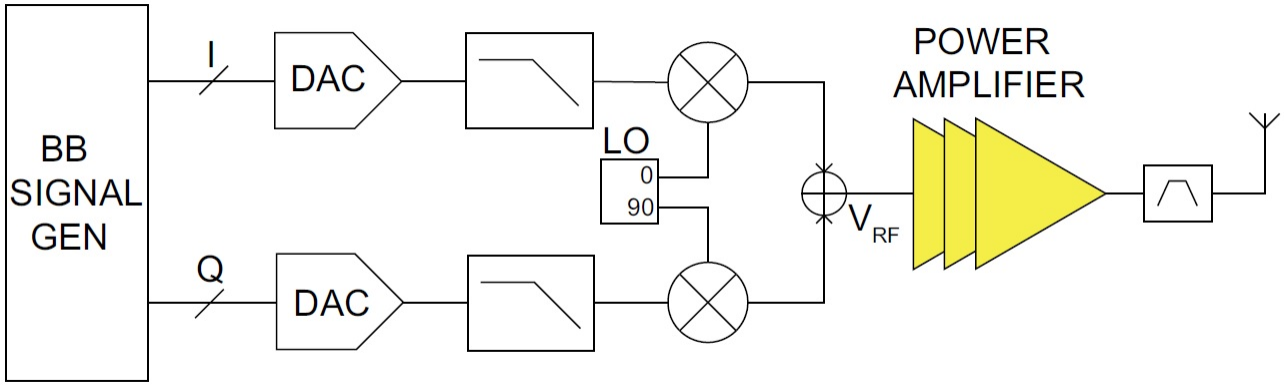


Figure 1.4: A generic Cartesian transmitter [2].

On the other hand, portable devices generally require small form-factor radios to reduce the overall size and packaging costs for high volume productions. Therefore, a high level of integration of merging as many components into a single die in an inexpensive technology is one of the long term visions for wireless transceivers. Over the last decade, most of the transceiver building blocks have been successfully integrated into CMOS technology as possible and co-exist with Digital Signal Processing (DSP) modules on the same die. Although several advances have been made recently, the full integration of CMOS PAs is

still among the most difficult challenges towards achieving a true System-On-Chip (SOC) solution. This is further exacerbated by supply voltage reduction due to device geometry and gate dielectric scaling, which poses significant challenges in terms of power handling capabilities to integrated CMOS PAs. Meanwhile, increased losses of on-chip passives due to the semi-conducting silicon substrate as well as the closer proximity of the metal stack to such a lossy substrate also tends to degrade the overall efficiency of a fully integrated CMOS PA [18].

The primary goal of this dissertation is hence to investigate fully-integrated, power-efficient RF transmitter designs with a special emphasis on the direct digitally modulated TX architecture. The key design trade-off is the TX linearity and efficiency for high output power levels. Although the full TX power consumption is dominated by the PA output stage, we still provide a complete treatment at the system level to investigate various efficiency enhancement techniques. That is because the baseband (BB) stage (comprising of DSP modules, Digital-to-Analog Converter (DAC) and filters) and the up-conversion and driver stages all contribute a significant portion to the total power consumption of a TX, especially at back-off power levels where the PA power consumption is usually scaled down accordingly while the overhead from the BB and the up-conversion stages are usually fixed (Table 1.1). Linear and efficient preceding stages are therefore equally important as the PA output stage.

Table 1.1: Power breakdown of an 802.11n TX at P_{out}=-8.3dBm [17].

TX block	**Power dissipation [mW]**	**Percentage [%]**
LO Dividers+Buffer	124	33
Up-conversion	39.3	10
RF filter	40.7	11
VGA	110	29
Output driver	61.4	16

Furthermore, we will also investigate the out-of-band (OOB) spectral purity and its trade-off with various efficiency enhancement techniques. Contemporary mobile solutions are most likely to integrate multiple radios together to offer a complete and versatile user experience. It is not uncommon today to have the simultaneous availability of cellular, WLAN, Bluetooth, GPS and FM functionality all from a single mobile terminal. Co-existence among multiple radios is therefore an important consideration. The key requirement for the TX in this regard would be the OOB transmit noise be low enough not to de-sensitize the receiver (RX) of another radio in that band. Ideally, the far-out noise should be below the thermal noise floor defined by Eq.(1.2)

$$P_n = 10 \times \log_{10}(k_B T) \qquad \text{[dBm/Hz]} \tag{1.2}$$

where k_B is the Boltzmann constant and T is temperature. At room temperature ($T = 300K$), the thermal noise floor is about -174dBm/Hz. With a modest isolation of 40dB from antenna-to-antenna and/or diplexers, the OOB transmit noise floor should be below -134dBm/Hz. Compared with state-of-the-art analog Cartesian WLAN TXs, this specification is still challenging to achieve across a wide bandwidth at >15dBm OFDM power levels. On the other hand, the direct digitally modulated TX inherently has spectral images at offsets equal to multiples of the BB sample rate due to its zero-order-hold operation at the digital/RF-DAC interface. Furthermore, the OOB noise floor is also contributed by digital quantization, besides the Adjacent Channel Power Regrowth (ACPR) due to TX non-linearities purely in the analog domain. Due to these two additional noise contributing factors that are absent in an analog Cartesian TX, the spectral purity of a digitally modulated TX tends to be worse at similar output power levels, jeopardizing its co-existence with other radios. It is for this reason that the OOB spectrum is also an important consideration in our research on digitally-modulated TXs.

1.1 Thesis Organization

To rephrase, this thesis is focused on the design and analysis of a fully-integrated, power-efficient and co-existable digitally-modulated CMOS power transmitter system. Part I of this thesis serves as the background studies for our research work: we review the various techniques to enhance PA efficiencies at back-off power levels in Chapter 2; digitally modulated TX architecture is introduced with its advantages as well as fundamental limitations. We then proceed with the design and analysis of fully-integrated digitally modulated polar TX system for efficiency enhancement in Part II. We first outline TX system-level considerations in Chapter 3, cover the design of the core switching PA in Chapter 4, and then the transformer-based impedance modulator in Chapter 5. The design considerations of the power-efficient, open-loop phase modulator are explained in Chapter 6, while Chapter 7 is dedicated to the design and synthesis of baseband digital filters to knock down the close-in spectral images. Measurement results are presented in Chapter 8, and concluding remarks in Chapter 9.

Chapter 2

Overview of Efficiency Enhancement Techniques at Back-off Output Powers

2.1 Efficiency Back-off of Class-A, Class-B and Class-AB PAs

The PA drain efficiency is defined as the output power delivered the load normalized by the total power drawn from the supply

$$\eta_{de} = \frac{P_{out}}{P_{supply}} = \frac{I_{out} \times V_{out}}{I_{vdd} \times V_{dd}} = \frac{I_{out}}{I_{vdd}} \times \frac{V_{out}}{V_{dd}} \tag{2.1}$$

where P_{out} is the output power delivered to the load, P_{supply} is the total power drawn from the supply, I_{out} is the room-mean-square (RMS) output current, V_{out} is the RMS output voltage, V_{dd} is the supply voltage, and I_{vdd} is the supply current. As shown above, the drain efficiency can be calculated as the normalized output current, $\frac{I_{out}}{I_{vdd}}$, times the normalized output voltage, $\frac{V_{out}}{V_{dd}}$. Drain efficiencies of an ideal class-A, class-B and switching PA are analyzed below at both peak and back-off power levels.

In an ideal class-A PA (Fig. 2.1) where the drain voltage is allowed to swing up to $2 \times V_{dd}$, the RMS output voltage at peak power is

$$V_{out} = \frac{V_{dd}}{\sqrt{2}} \tag{2.2}$$

because the amplitude of V_{out} is V_{dd}. In a proper design, the drain current has an amplitude equal to its quiescent level such that the drain current transiently reaches zero at peak power. In other words,

$$I_{out} = \frac{I_{vdd}}{\sqrt{2}} \tag{2.3}$$

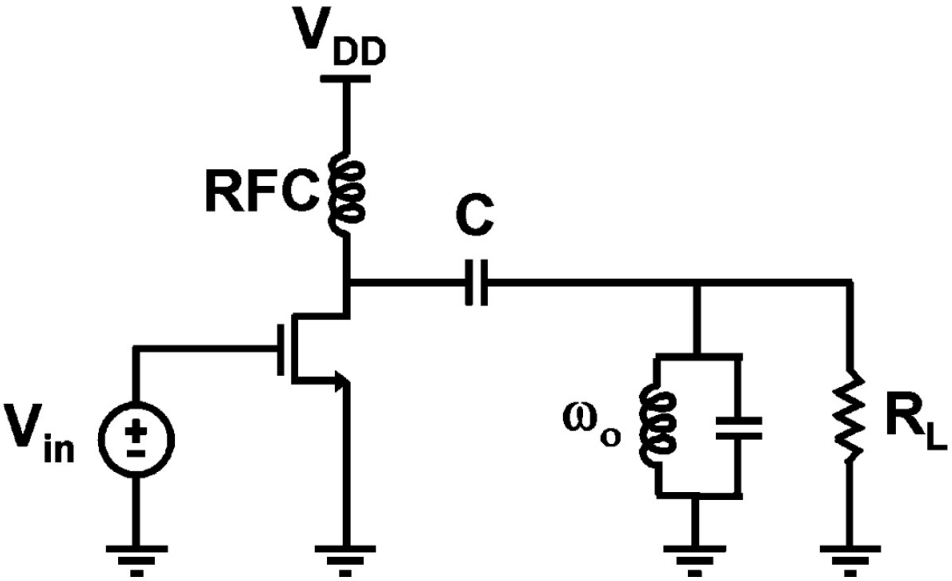


Figure 2.1: A generic class-A power amplifier with RF-choke (RFC) [3].

Substituting Eq.(2.2) and Eq.(2.3) into Eq.(2.1), the peak drain efficiency of a class-A PA, which occurs at peak power, is

$$\eta_{class-A,pk} = \frac{I_{out} \times V_{out}}{I_{vdd} \times V_{dd}} = 50\% \tag{2.4}$$

To derive the efficiency back-off characteristics for a class-A PA, assume the load for power delivery is a real impedance, Z_L

$$Z_L = \frac{V_{out}}{I_{out}} \tag{2.5}$$

The drain efficiency for a class-A PA is therefore

$$\eta_{class-A} = \frac{I_{out} \times V_{out}}{I_{vdd} \times V_{dd}} = \frac{I_{out}^2 \times Z_L}{P_{const}} = \frac{V_{out}^2}{Z_L \times P_{const}} \tag{2.6}$$

where P_{const} is the constant power drawn by the class-A PA from the supply

$$P_{const} = V_{dd} \times I_{vdd} \tag{2.7}$$

The drain efficiency of a class-A PA therefore reduces quadratically with output amplitude. At 6-dB power backoff, the drain efficiency is only 25% of its peak value.

In class-B operation, the transistor drain current is a half-wave rectified sine-wave, whose time-average is the current drawn from the supply

$$I_{vdd} = \frac{\sqrt{2} \times I_{out}}{\pi} \times 2 \tag{2.8}$$

where the factor of 2 accounts for the dual power transistors in a push-pull fashion. The class-B operation inherently scales its quiescent current in proportion to signal amplitude, which is much more efficient than class-A where the quiescent current is a constant regardless of signal level. The drain efficiency of a class-B PA is therefore

$$\eta_{class-B} = \frac{I_{out} \times V_{out}}{I_{vdd} \times V_{dd}} = \frac{V_{out} \times I_{out}}{V_{dd} \times \frac{2\sqrt{2}}{\pi} I_{out}} = \frac{\pi}{2\sqrt{2}} \frac{V_{out}}{V_{dd}} \tag{2.9}$$

Therefore, the class-B efficiency backs-off linearly with output amplitude, due to the linear scaling of quiescent current with signal amplitude. Similar to a class-A PA, the drain voltage can swing up to $2 \times V_{dd}$ for a class-B PA at peak power, yielding

$$V_{out} = \frac{V_{dd}}{\sqrt{2}} \tag{2.10}$$

and giving a peak efficiency of

$$\eta_{class-B,pk} = \frac{I_{out} \times V_{out}}{I_{vdd} \times V_{dd}} = \frac{\pi}{4} = 78.5\% \tag{2.11}$$

The class-B PA can achieve better efficiency at peak power (78.5% vs. 50%) and back-off power levels (linear vs. quadratic), as shown in Fig. 2.2. Despite of the efficiency advantage, a class-B PA suffers from degraded linearity as opposed to class-A, because the transistor is only conducting for half the RF period. To get a descent efficiency back-off characteristic without much linearity hit, a transconductance-based PA is usually biased in the hybrid of class-A and class-B mode (hence the name class-AB). The efficiency and linearity of a class-AB PA are between those of an ideal class-A and class-B.

In this chapter, various techniques to improve the PA efficiency at back-off power levels are briefly reviewed [19]. Note that some of these techniques only achieve the class-B back-off characteristic. However, those are still significant improvements over a conventional class-B/class-AB PA if they have linearity as good as class-A. In other words, the goal of the various techniques is to improve the trade-off between efficiency and linearity inherent in the class-A/B/AB PA; this can be accomplished by either achieving an ideal class-B back-off with better linearity, or achieving a better-than-class-B back-off with similar linearity.

2.2 Dynamic Current Biasing

For a transconductance(g_m)-based PA, a significant portion of non-linearity comes from the current domain, where the gate/base voltage non-linearly trans-conducts the drain current. To reduce this g_m non-linearity, the RF current swing normalized by quiescent current should be low enough. Partially due to a constant quiescent current regardless of signal

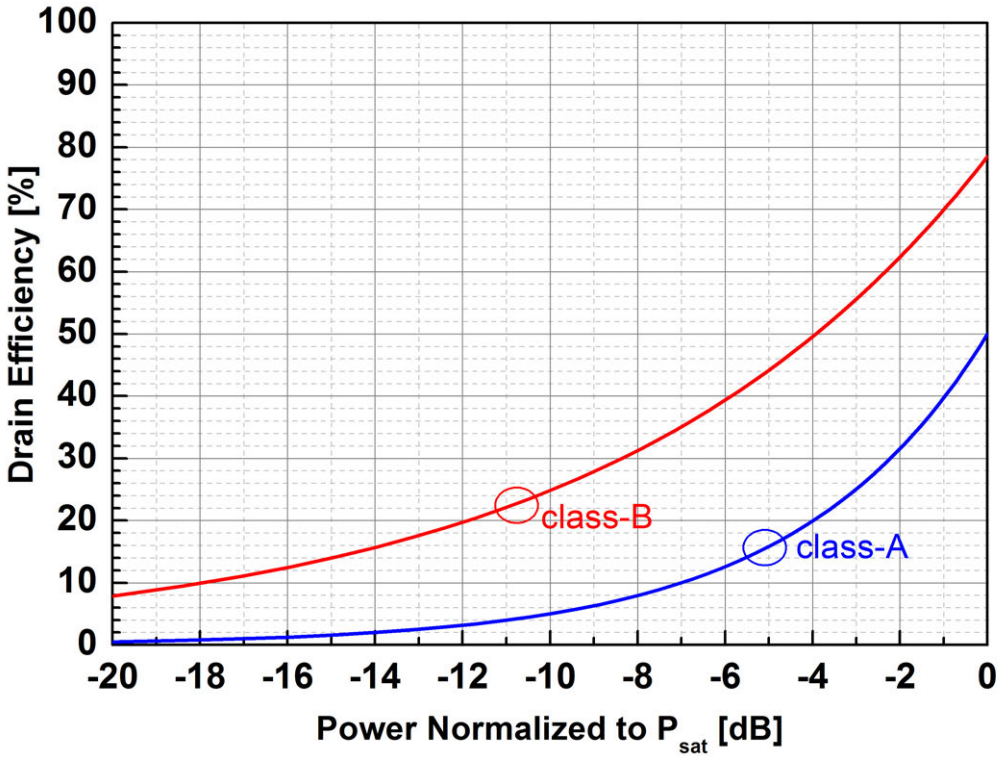


Figure 2.2: The drain efficiency of an ideal class-A and class-B power amplifier.

level and the resultant low normalized signal current, a g_m-based PA that is biased deep into class-A region exhibits superior current linearity. At very low signal levels, however, the normalized current swing is unnecessarily low, wasting power and degrading efficiency. The dynamic current biasing technique (Fig. 2.3) therefore attempts to scale the bias current according to the average transmit power across a short period of time (on the order of several RF cycles and above) and hence maintain a roughly constant normalized current swing. Much the same way as class-B (Eq.(2.8)), the quiescent current as regulated by this technique is able to linearly track signal amplitude and therefore achieve class-B back-off in the best case. At the same time, the normalized current swing is still maintained at a low enough level that linearity is not significantly degraded with respect to class-A.

The potential linearity improvement from this technique can be derived in the following way. Since the g_m-based PA provides higher small-signal gain with higher bias current, this technique essentially increases the small-signal gain with increased signal level. This just compensates the compressive AM-AM characteristic where the apparent gain (i.e. the large-signal gain) is reduced with increased input power. Essentially a "pre-distortion" technique, it therefore helps to maintain a constant large signal gain across a wider range of input power levels. It should be noted that although this technique compensates the compressive AM-AM non-linearity of the PA and hence improves the linearity, it does not improve the

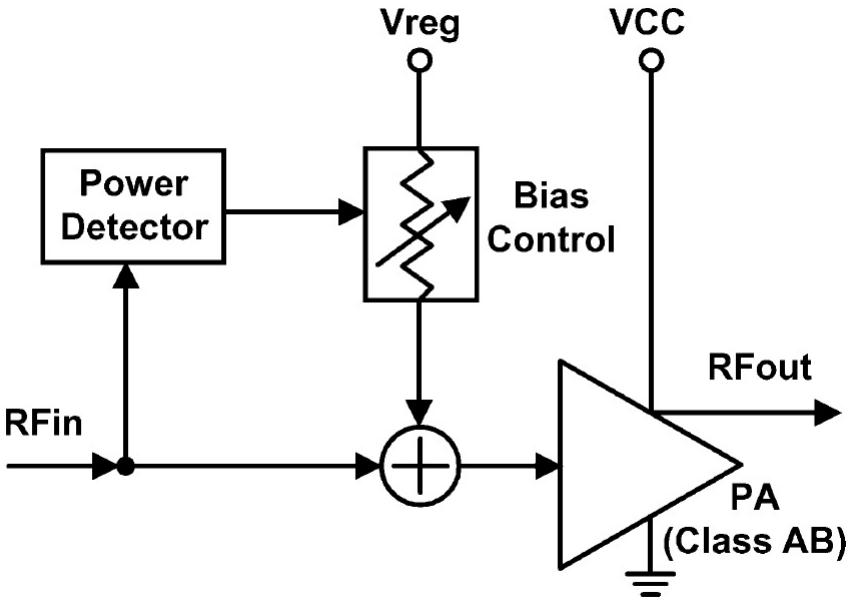


Figure 2.3: An adaptive current biasing scheme for the class-AB PA [4].

AM-PM distortion which is another important non-linearity source.

The implementation of this technique requires input power (envelope) sensing, filtering (to determine the time-average of a varying envelope) as well as a bias control to convey the detected average envelope to the biasing voltage. It can be implemented in a closed-loop fashion ([4]) as shown in Fig. 2.4. In the circuits, C_{bypass} is used as the envelope filter. By adjusting the base resistor R_b and the emitter area of HBT2, the slope of the biasing current with respect to input signal level can be adjusted and high efficiency at low output powers and high linearity at high output powers can be achieved simultaneously. With Wideband Code-Division Multiple Access (WCDMA) modulated signal and for a fixed -33dBc of Adjacent Channel Leakage Ratio (ACLR) target, this technique increases the PA output power from 27.5dBm to 28.3dBm, although with a Power Added Efficiency (PAE) degradation from 54% to 52.4% ([4]). With the PA Probability Distribution Function (PDF) based on an IS-95 CDMA urban environment, the dynamic current biasing technique achieves an average power efficiency of 11.8% at 5dB output power.

Dynamic current bias control can also be implemented with a separate feedforward path ([5]), as shown in Fig. 2.5. Fig. 2.6 shows the measured gain flatness improvement with this technique, where the gain is intentionally lowered at low power levels to extend the output 1-dB compression point (P_{1dB}) by 1.6dB. The linearity improvement is also readily verified by the measured EVM (Fig. 2.7), which is improved from -25.3dB to -28.5dB at 17dBm WLAN OFDM (64-QAM, 54Mbps) power; the low quiescent current in low power regions also improves the PAE in the same condition from 3.3% to 8.9%.

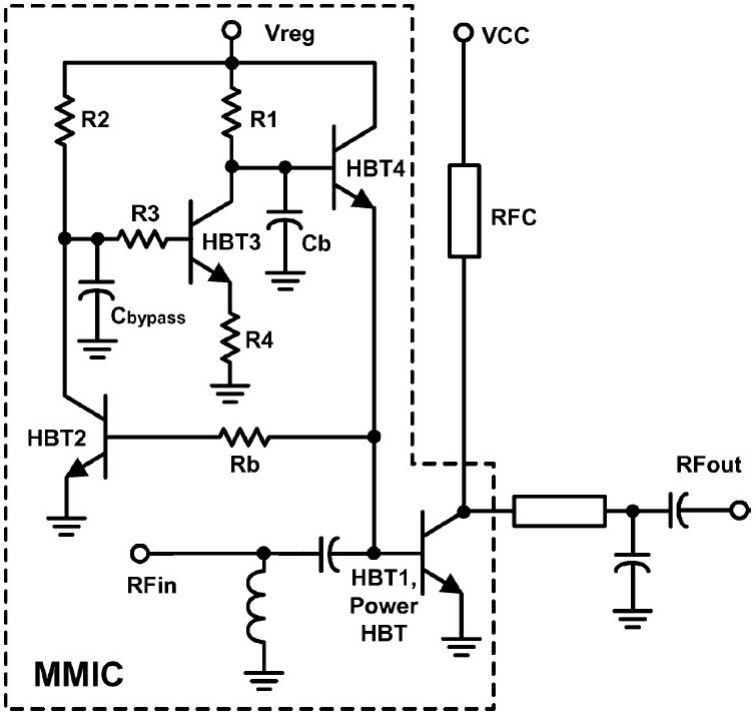


Figure 2.4: Adaptive current bias control implemented with a feedback loop [4].

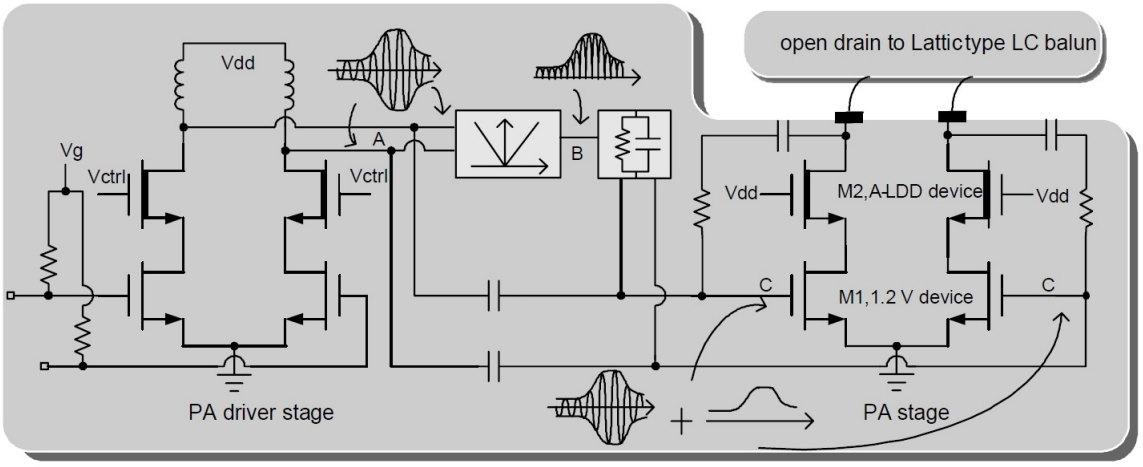


Figure 2.5: Dynamic current bias control implemented with a feedforward path [5].

Dynamic current biasing can also be implemented by current-combining various PA branches that are biased differently ([6]), as illustrated in Fig. 2.8. The auxiliary PA (aux-PA) is biased deep into class-B and it only conducts enough quiescent current to deliver signal power when the input power is higher than some threshold. The idea can be further

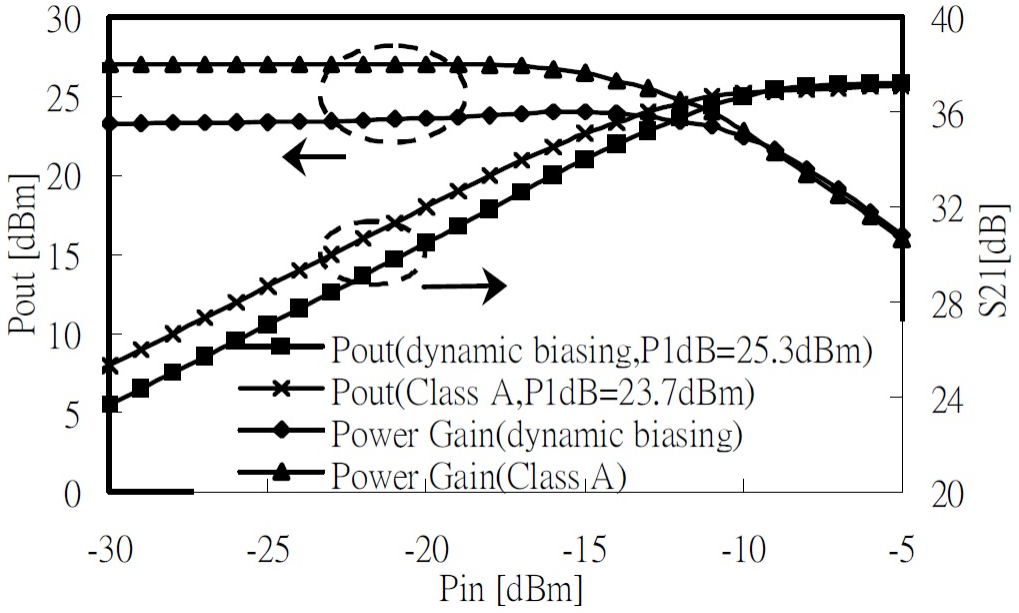


Figure 2.6: The measured large-signal gain flatness is improved by dynamic current biasing [5].

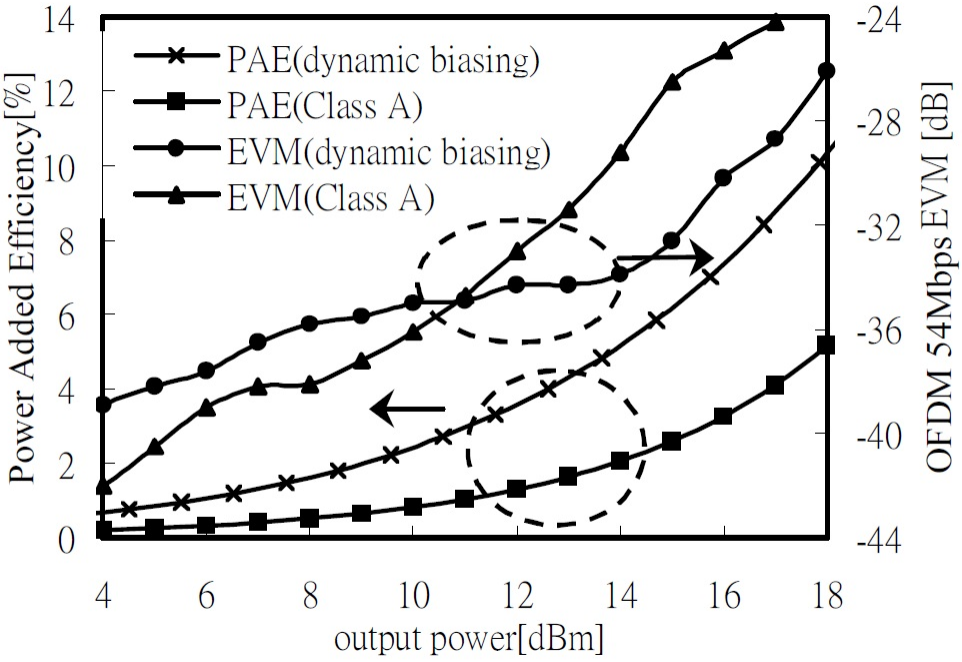


Figure 2.7: The measured EVM and PAE are improved by dynamic current biasing [5].

extended to the case where multiple aux-PAs are current-combined and therefore multiple levels of biasing currents would respond to multiple input power levels. In [6], the biasing for the main- and aux-PA can be designed differently, allowing one more degree of design freedom for the tradeoff between linearity and efficiency. The linearized PA delivers a P_{sat} of 28.3dBm with 35.3% drain efficiency; the WLAN OFDM power at -28dB EVM is 21.2dBm with 19% drain efficiency. This implementation is inherently more amenable to static predistortion, because it gets rid of an explicit envelope filter for time-averaging, which would otherwise be realized with memory elements (i.e. capacitors) ([4][5]). The employment of the envelope filter makes the present biasing also strongly dependent on previous history of input power levels, posing challenges to static predistortion.

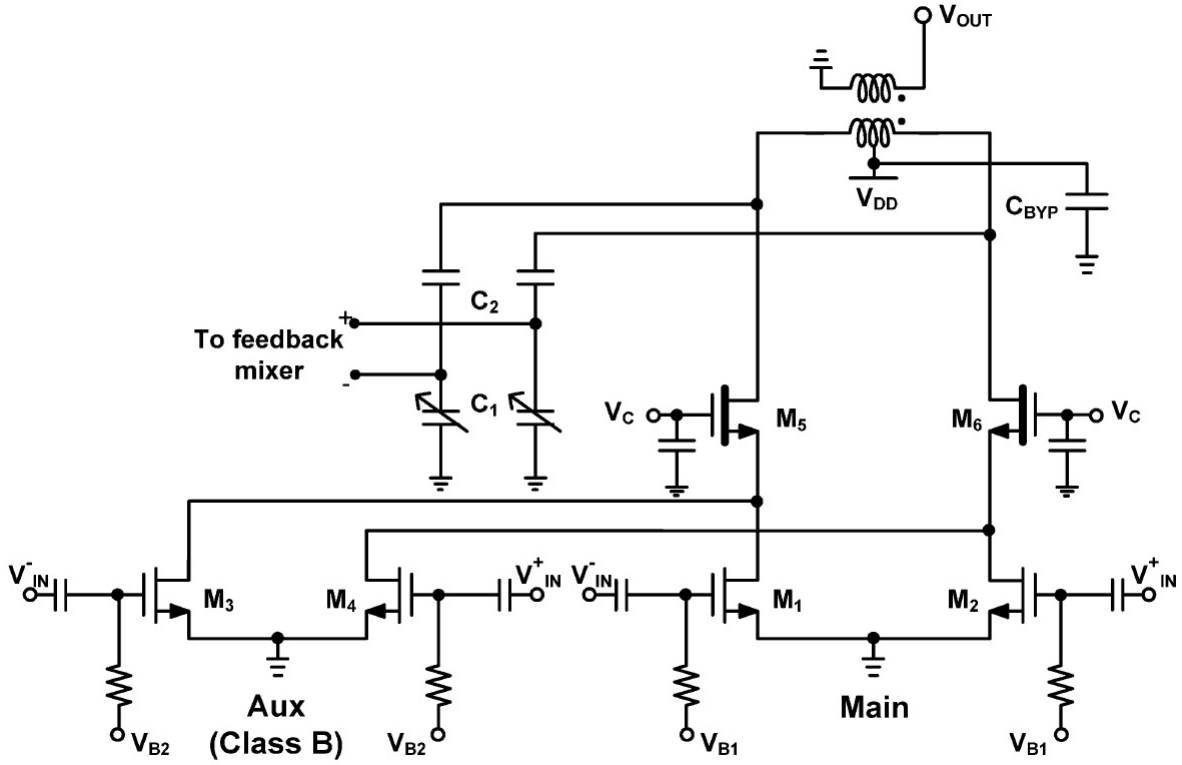


Figure 2.8: Dynamic current biasing implemented by an aux-PA biased differently [6].

The dynamic current biasing technique, which attempts to have the biasing level track the signal amplitude, can only achieve class-B efficiency back-off characteristic at best (Table 2.1). As summarized in Table 2.1, efficiencies at the same P_{out} with class-B backoff characteristic are calculated by Eq.(2.12) and shown in the third column.

$$\eta_{class-B,P_{out}} = \eta_{P_{sat}} \times 10^{-\frac{P_{backoff}}{20}} \tag{2.12}$$

where $P_{backoff}$ is the power backoff from P_{sat} in dB. With two exceptions ([6] and [20]), the class-B extrapolated efficiencies are all better than the measured results. For [6], it has been confirmed that the measured efficiency at P_{sat} is degraded by the elevated temperature due to the increased heat dissipation under this high power condition; as the P_{out} backs off by more than 7dB from P_{sat}, the temperature goes down and the efficiency increases. Therefore the exact $\eta_{P_{sat}}$ for [6] in Eq.(2.12) is higher than the measured value that is actually used in the equation. In [20], the measured PAE remains roughly the same over a P_{out} range from 25.0 to 27.5dBm, indicating some other mechanisms that are also affecting the PAE.

Table 2.1: Efficiency back-off characteristics with dynamic current biasing.

Ref	**P_{sat}/η [dBm/%]**	**Linear P_{out}/η [dBm/%]**	**η with class-B backoff [%]**
[4]	28.3 / 52.4	17.3 [1]/ 11.8	14.8
[5]	25.3 / N.A.	17.0 / 8.9	N.A.
[6]	28.3 / 35.3	21.2 / 19.0	15.6
[20]	27.5 / 15.0	20.0 / 7.2	6.3
[21]	26.0 / 27.0	15.0 [1]/ 5.0	7.6

[1] PAPR of 11dB is assumed for WCDMA downlink carrier.

As shown in Eq.(2.1), the drain efficiency is the normalized output current times the normalized output voltage. Dynamic current biasing tries to make the supply current track the signal amplitude to improve the efficiency of transconductance-based PAs. The efficiency can also be enhanced by making the supply voltage to track signal levels. This can be achieved by either the supply modulation with fixed drain impedances seen by the PA or by the drain impedance modulation with a fixed supply voltage. If the modulation scheme can convey a non-linear envelope without relying on the transistor g_m, a switching-mode PA can be used and a constant peak efficiency can be theoretically achieved regardless of output power levels, as discussed below.

2.3 Envelope Elimination and Restoration (Polar Modulation)

In an Envelope Elimination and Restoration system ([22]), a phase modulated signal with constant envelope is amplified by an efficient, non-linear switching PA while the amplitude information is restored through the PA supply modulation (Fig. 2.9). Because the non-linear envelope is conveyed by supply modulation, a non-linear switching PA (class-D, class-E, class-F and etc) can be employed to amplify the constant-envelope and phase-modulated signal at its input, offering higher efficiency compared to its linear counterpart (e.g., class-A and class-AB PA). With an ideal supply modulator, this architecture can achieve 100% theoretical

efficiency regardless of power levels. In fact, an EER system is a polar transmitter where the modulated signal is decomposed into a phase-modulated RF component and a baseband envelope component.

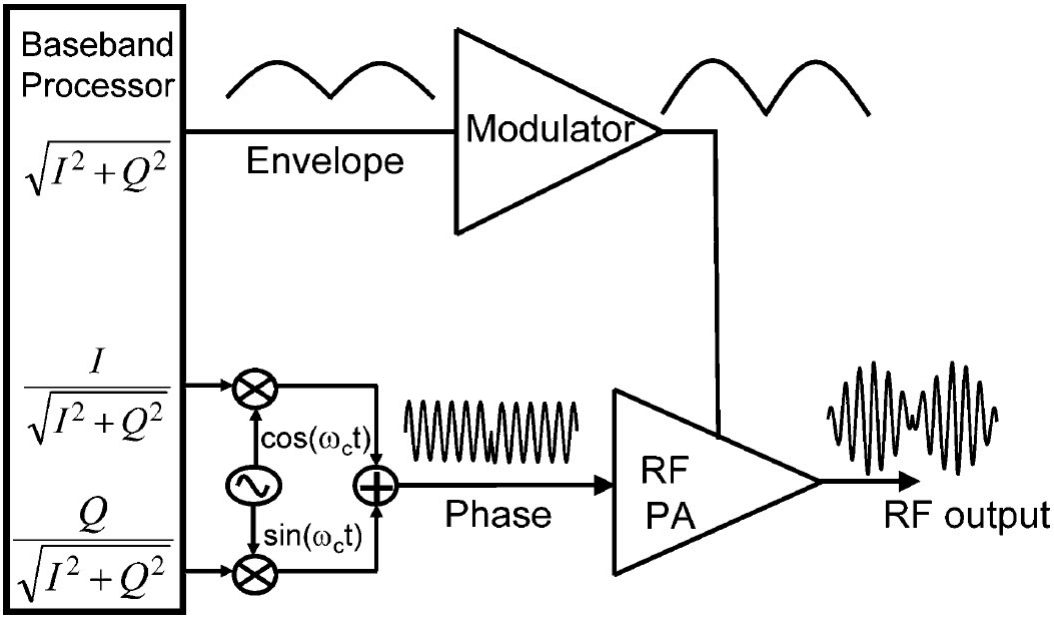


Figure 2.9: An Envelope Elimination and Restoration (EER) TX [7].

The implementation of the supply modulator for an EER system, however, typically suffers from a serious trade-off among efficiency, bandwidth and linearity. It has to support a supply current to the order of several hundred milli-amperes (mAs) and above, with a high Peak-to-Average-Ratio (PAR) and a large bandwidth. The bandwidth requirement for the supply modulator may be much more (3–10x) than the corresponding BB signal bandwidth due to bandwidth expansion from Cartesian to polar conversion ([23]). In this section, our review will focus on the design of the supply modulator, which is usually the efficiency bottleneck in an EER system.

The supply modulator is traditionally implemented as a linear regulator (Fig. 2.10(a)), for its wide bandwidth, reduced output ripple, and therefore excellent out-of-band spectral purity ([9]). However, the power efficiency of the linear regulator itself backs off as class-B at best. To see this point, note that the PA in Fig. 2.10(a) draws the same current from its regulated supply as the linear regulator does from the actual supply (V_{DD}). Therefore, this EER system with linear regulator essentially makes the supply current to track the signal amplitude while the actual supply is still fixed regardless of power levels, yielding class-B type efficiency back-off (similar to Eq.(2.9)). Another way to look at this is that the voltage drop across the linear regulator increases at lower signal powers (and hence lower PA supply), introducing a larger degradation on top of the PA efficiency. As seen from Fig. 2.11,

efficiency degradation from the linear regulator in an EER system is significant especially at low power levels. It is for this reason that a linear regulator is not suitable for EER systems with modulated signals of a high PAPR.

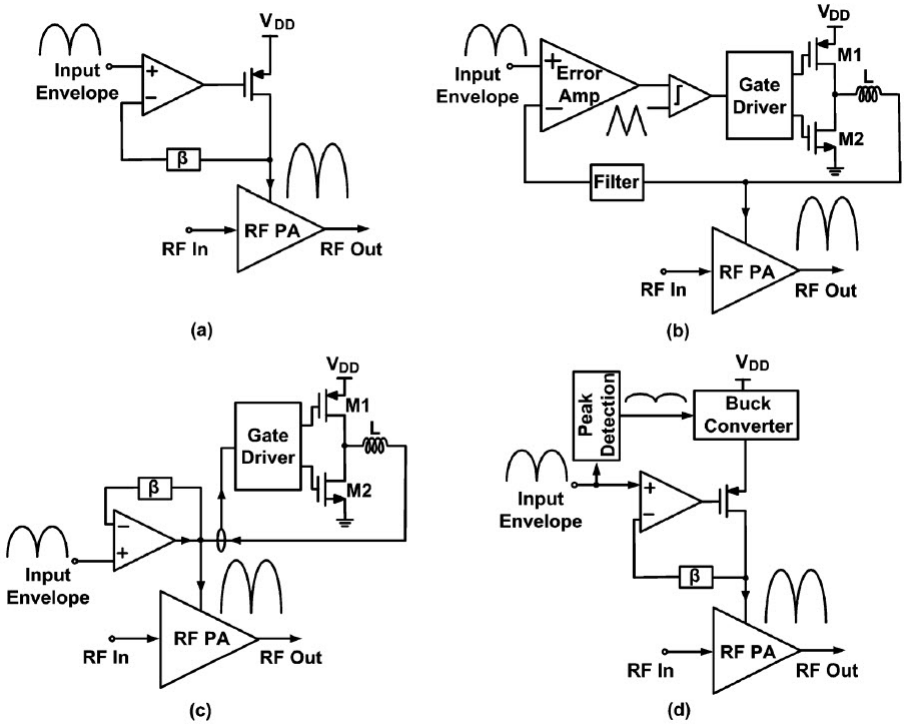


Figure 2.10: Supply regulators constructed from linear and switching amplifiers [8].

A switching regulator (Fig. 2.10(b)), on the other hand, offers high efficiency across a much broader range of regulated output voltages ([24]). However, it can only support a signal bandwidth that is a small fraction of the switching frequency, otherwise the output ripples will become excessive, degrading transmit linearity. Meanwhile, output ripples and the intense switching actions inherent within a switching regulator tend to produce noise humps (Fig. 2.12) and spurs (Fig. 2.13) in the out-of-band, which are highly undesirable for co-existence. To support a high bandwidth while meeting the stringent spectral performances required by modern communication systems, a sufficiently high switching frequency has to be used (to both minimize the ripples and push the spurs far away from in-band), introducing higher switching (CV^2f) losses and hence larger efficiency degradation.

To overcome the poor efficiency of the linear regulator at back-off power levels and the spectral spurs from the switching regulator, researchers have proposed a variety of hybrid architectures. A hybrid consisting of linear and switching regulators connected in parallel (Fig. 2.10(c)) is one of the most popular architectures ([7]). The switching regulator provides the power for the low-frequency component of the envelope while the residual power, which is mainly concentrated around high modulation frequencies, is supplied by the linear regulator.

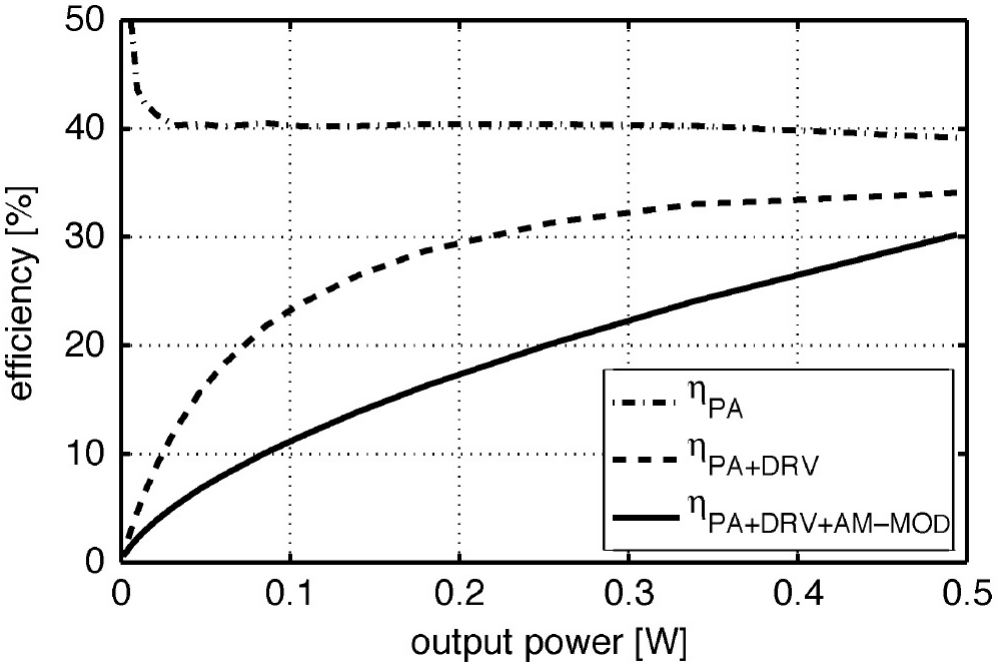


Figure 2.11: The efficiency of PA-only and PA with linear regulator in an EER system [9].

The linear regulator also provides a low output impedance in shunt with the loading from the PA, and hence sinks most of the ripple current if the former is much lower than the latter. Therefore, the ripple within the regulated voltage is reduced, offering better out-of-band noise performance. This architecture is well suited for modulation schemes where the envelope has significant low frequency components (e.g. WLAN OFDM). The overall back-off efficiency of the parallel hybrid, however, is limited by the linear regulator, which has to present low enough output impedance up to the switching frequency of the switching regulator. Since the switching frequency is usually chosen high enough to reduce output ripple and push the ripple frequency components far away from inband, the power penalty from the wideband low impedance requirement for the linear regulator is sometimes significant. In [7], the parallel hybrid regulator delivers a 22.7dBm of peak output (DC) power to a 5.3Ω load with 87.5% peak efficiency under a 1.2V supply; the efficiency is 40% at 10dB backoff. Measured with a 5Ω load, it has a -3dB small-signal bandwidth of 285MHz and power bandwidth of 45MHz. The switching ripple is 4.3mV_{rms} at a switching frequency of 118MHz. Powered by the regulator, a class-E PA delivers a P_{out} of 11.7dBm with -26.1dB EVM for WLAN 802.11g 54Mb/s data.

Alternatively, the low back-off efficiency of a linear regulator can be overcome by inserting a switching regulator in series ([25]), as shown in Fig. 2.10(d). While the switching regulator lowers the input voltage for the Low-Dropout (LDO) regulator at back-off and therefore reduces the voltage drop across the LDO and the associated efficiency loss, the LDO atten-

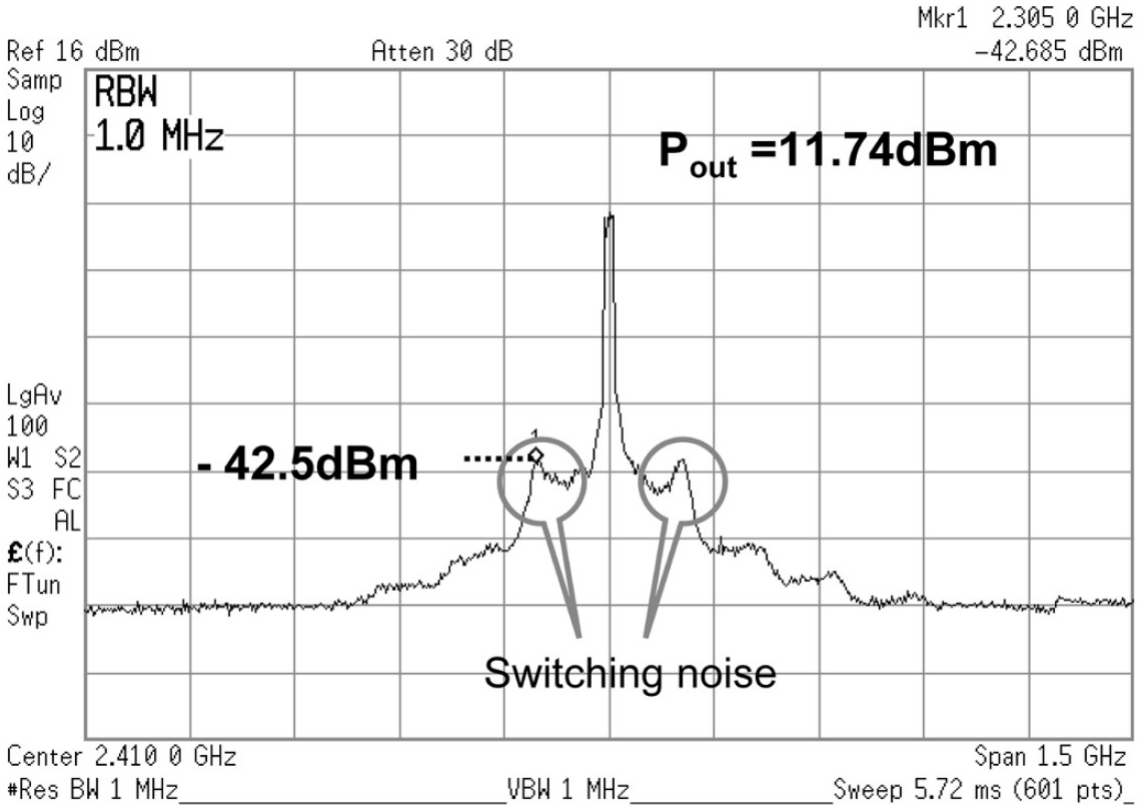


Figure 2.12: Noise humps in the transmit spectrum due to switching regulator [7].

uates the ripples from the switching regulator by its Power Supply Rejection Ratio (PSRR). However, since the switching regulator is connected in series with the LDO, its switching frequency still has to be high for wideband applications in order to accommodate the full supply power to the PA; in those cases, the out-of-band spectral purity of the series hybrid might be degraded due to a similar degradation of the LDO's PSRR at higher frequencies. In [25], the series hybrid delivers 30.8dBm of maximum output power with 75.5% efficiency under 3.6V supply; at 10dB backoff, the efficiency is 36%. The LDO PSRR is 33dB up to 700kHz and degrades to 11dB at 2MHz. With digital pre-emphasis, the series hybrid can support up to 4MHz input bandwidth. Powered by the series hybrid, a commercial PA delivers 25.5dBm of P_{out} with 8% EVM for 1625kbps 8-PSK modulation with 1.8dB PAPR.

A series-parallel hybrid regulator (Fig. 2.14) is proposed in [8] to reduce the efficiency loss of the linear regulator in a parallel hybrid. A separate switching regulator is inserted between the linear regulator and the supply and generates a varying supply for the linear regulator with bandwidth much lower than the envelope. Since the linear stage only provides 20-30% of the overall output power, the additional switching regulator can be small and therefore efficient even for wideband applications. It delivers an average power of 29.7dBm with 82% efficiency under a 4.5V supply, for a 10MHz LTE signal with 6dB PAPR, although the

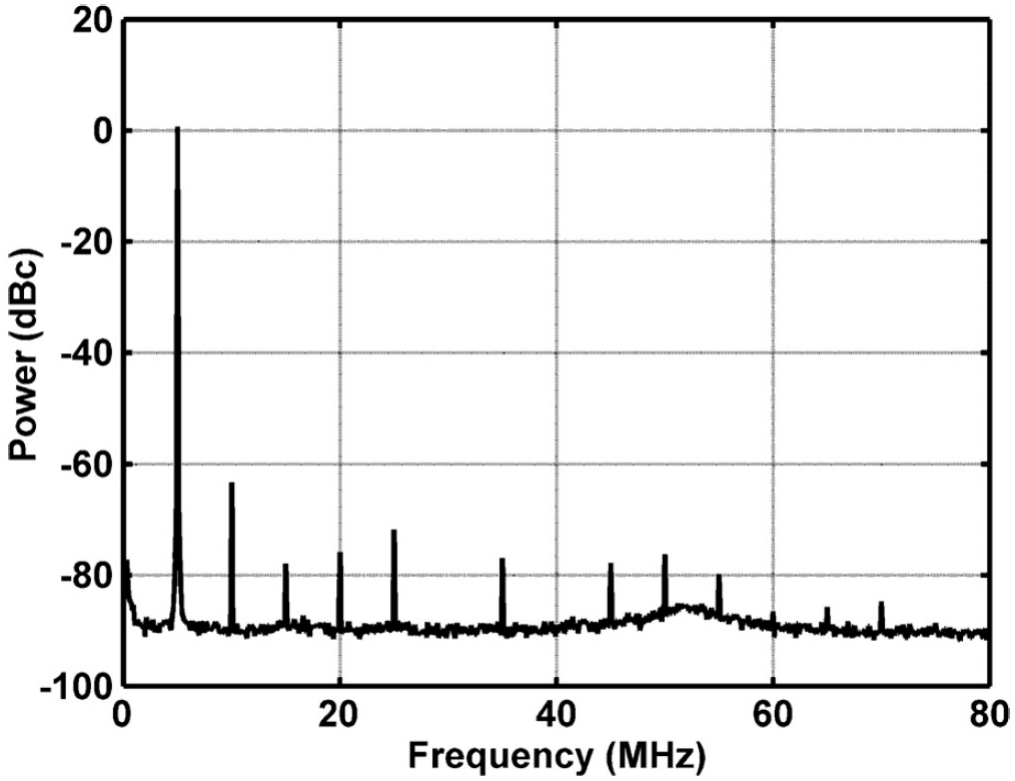


Figure 2.13: Noise spurs in the transmit spectrum due to switching regulator [8].

LTE EVM/ACPR measurements are missing. One major challenge with this architecture is that, it requires the generation of a reduced bandwidth envelope as the input to the series switching regulator; the reduced-bandwidth envelope can be generated by digital filtering from the original EER envelope and needs to be time aligned with the original one for proper operation. The required timing adjustment has to accommodate Process Voltage and Temperature (PVT) variations, which introduces overhead at the system level.

The performance of state-of-the-art supply modulators are summarized in Table. 2.2. As seen from the table, relatively few works have supported wideband high-PAPR modulations, which are typically employed by modern high data-rate RF communication systems for spectral efficiency. Furthermore, EVM measurements for the complete EER/polar system consisting of both the PA and the supply modulator are sometimes missing. For the two works ([26] and [7]) supporting the 20MHz bandwidth of WLAN 802.11g signals, the efficiencies of the supply modulators themselves are still not high enough to demonstrate significant enhancement available from the EER scheme. In a class-B backoff, the efficiency degrades to 50% of its peak at 6dB backoff, which is comparable to the power overhead from a supply modulator with 50-60% efficiency at 6-7dB backoff, especially taking into account the overhead from the phase path of the EER system as well as the timing alignment be-

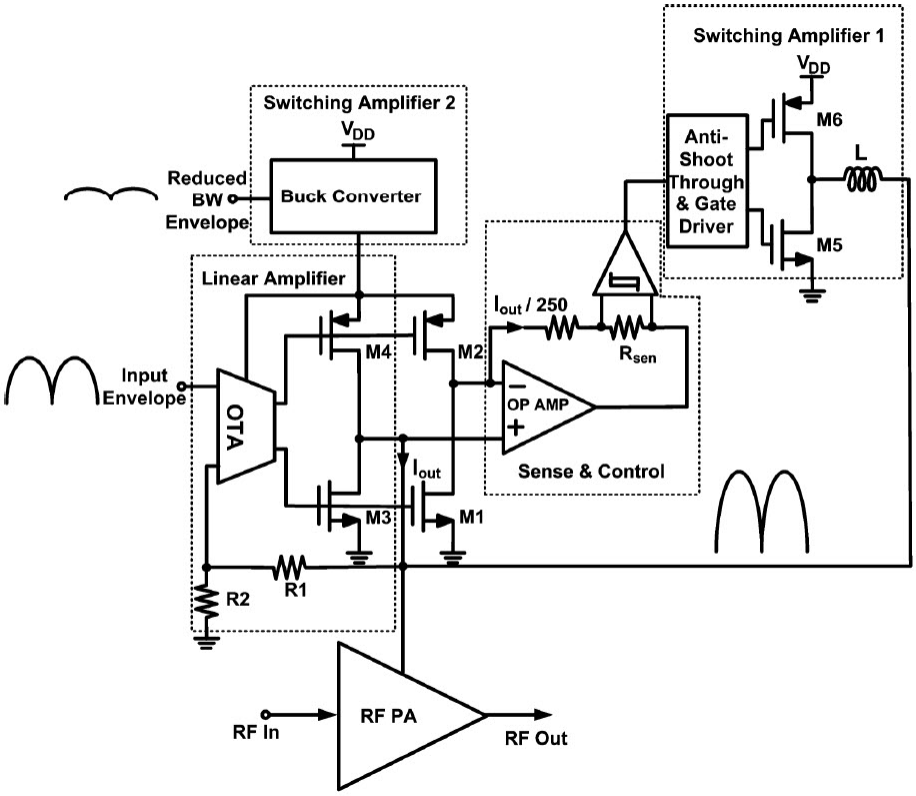


Figure 2.14: A combined series-parallel hybrid supply regulator [8].

tween the phase and the supply modulation path. Since the design of supply modulators for high-power, high-bandwidth and high-PAPR applications is unfortunately challenging, the envelope tracking architecture has been proposed to ease the design of supply modulator, as discussed below.

Table 2.2: Performance comparison for state-of-the-art supply modulators.

Ref	**Appl.**	**BW [MHz]**	**PAPR [dB]**	**Supply [V]**	P_{out} **[dBm]**	η **[%]**	**EVM [dB]**
[25]	8-PSK	1	1.8	3.6	29.0	72	-21.9
[8]	LTE	10	6.0	4.5	29.7	82	N.A.
[27]	WCDMA	4	3.5	N.A.	29.5	74	N.A.
[26]	WLAN	20	6.6	3.3	23.2	65	-30.4
[7]	WLAN	20	9.0	1.2	14.7	52	-26.1

2.4 Envelope Tracking

In an Envelope Tracking (ET) system (Fig. 2.15), a supply modulator is also used to have the PA supply voltage closely track the output envelope. Unlike an EER system, a linear class-AB PA (if not slightly compressed) is used and the gate/base modulation (through the g_m of the power transistors) is also part of the envelope modulation scheme. Therefore, the supply modulator in an ET system only handles the lower frequency components within the envelope while the higher frequency components of the envelope is conveyed through the gate/base input. By comparing the target envelope and the reduced bandwidth supply (at the supply modulator output) in Fig. 2.16, we can clearly see that the PA supply in the ET system does not track the sharp "dips" in the target envelope that are rich in high-frequency components. Through the introduction of g_m-based gate/base modulation, the ET scheme offers one more degree of freedom to trade the supply bandwidth (and hence the drain efficiency of the PA) for the power efficiency of the supply modulator.

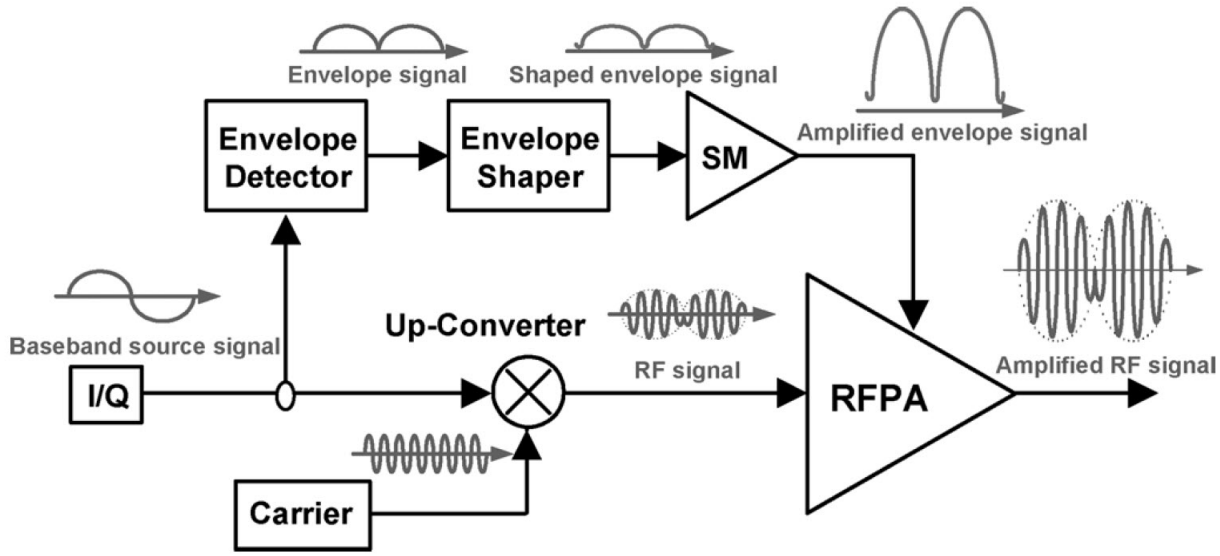


Figure 2.15: An Envelope Tracking (ET) TX [10].

Theoretically, the EER scheme is more efficient than ET since the PA in an EER system always operate in the switching mode, providing higher efficiency compared to a linear PA in an ET system. The ET scheme, however, allows the use of a supply modulator whose bandwidth can be lower than the bandwidth of the envelope, and hence can be more efficient if the high bandwidth supply modulator is the efficiency bottleneck in the overall system. Meanwhile, the ET system requires less precise timing alignment between the envelope and the gate/base RF modulation path than that between the envelope and phase paths in an EER system ([28]); it has been found in [28] that the EVM degradations are similar for 1x timing mismatch in an EER system and for 2x in an ET system.

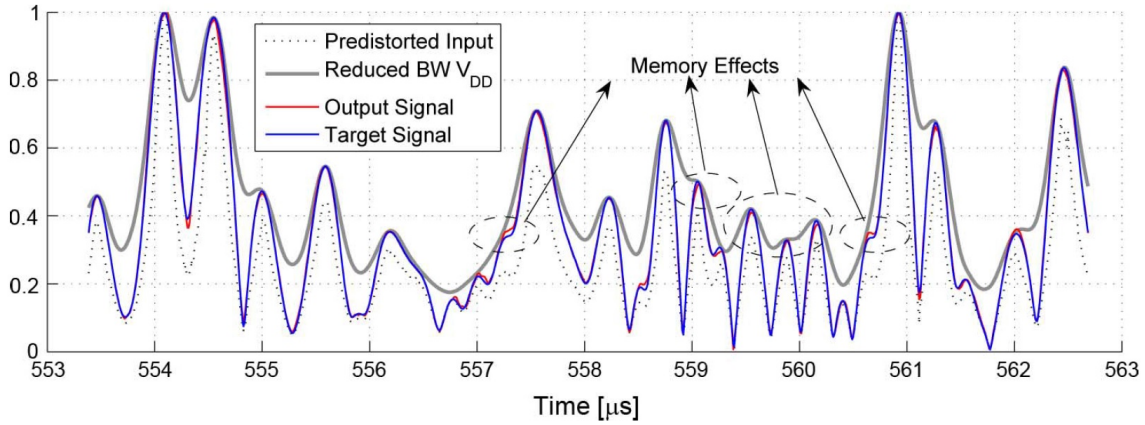


Figure 2.16: Time domain waveforms of the target, output, reduced bandwidth supply, and predistorted RF input envelope in an ET system [11].

Efficiency enhancements at back-off power levels for various ET PAs are benchmarked against class-B characteristic (Table. 2.3). The PAE of the core class-AB PA without the Envelope Modulator (EM, i.e. the supply modulator in the context of the ET system) at P_{sat} is first calculated according to the PAE reported for the PA with EM and the efficiency for stand-alone EM; next, the efficiency at the reported linear output power is calculated assuming class-B backoff from the same P_{sat} according to Eq. (2.12). Therefore, the values tabulated in the column of "Class-B no-EM η" represents the efficiency estimate for the case where the same class-AB PA for the ET system is used to deliver the same power levels with only the g_m-based envelope modulation. While an absolute performance benchmark may not be an exact apples-to-apples comparison due to the differences in the process, technology, supply voltage and etc, this "relative" benchmark between the ET-PA and the same linear-PA reveals more insight into the efficiency enhancement from the ET architecture.

As shown in Table. 2.3 and from our literature studies, some works do not clearly specify the peak power and efficiency numbers of the ET-PA system, which makes a fair comparison difficult. Overall, the ET architecture can potentially achieve better efficiencies as compared to a similar class-AB PA without EM; the improvements, however, are much more obvious at large backoff (PAPR>7∼8dB), due to the relatively flat efficiencies (to the order of 50-70%) of the envelope modulator at those back-off levels; recall that a class-B backoff has a 50% degradation in the drain efficiency compared to the peak at 6dB PAPR. Note that the comparison does not include the out-of-band spectral performance; also, the complexity of pre-distortion (and hence the potential linearity degradation of an ET system compared to a linear class-AB PA) is not considered, which is discussed below.

The complexity of predistortion in an ET system fundamentally arises from the fact that both the modulated supply and the modulated gate/base have an effect on the RF output. Consider only AM-AM predistortion. For a standalone class-AB PA, AM-AM predistortion

Table 2.3: Efficiency backoff characteristic with envelope tracking TXs.

Ref	**Mod./BW [MHz]**	P_{sat}/η **[dBm/%]**	P_{out}/η **[dBm/%]**	**Class-B no-EM** η **[%]**
[29]	LTE 16QAM / 10	N.A.	24.0 / 41	N.A.
[30]	LTE 16QAM / 10	32.0 / 44.1	25.8 / 31.6	28.7
[10]	LTE 16QAM / 10	32.2 / 55	27 / 39.8	39.8
[31]	WLAN 64QAM / 20	29.3 / 69	19.6 / 22.6	22.6
[26]	WLAN 64QAM / 20	29.0 / 40	20.0 / 28	22

is conceptually implemented by searching an AM-AM characteristic for an input power level that gives the desired output power. For the linear PA in an ET system, however, the AM-AM characteristic for the "look-up" also depends on the instantaneous supply (Fig. 2.17). In other words, the Look-Up-Table (LUT) for AM-AM predistortion in an ET system takes two entries, the supply voltage and the desired output level, both on an instantaneous basis (Fig. 2.18).

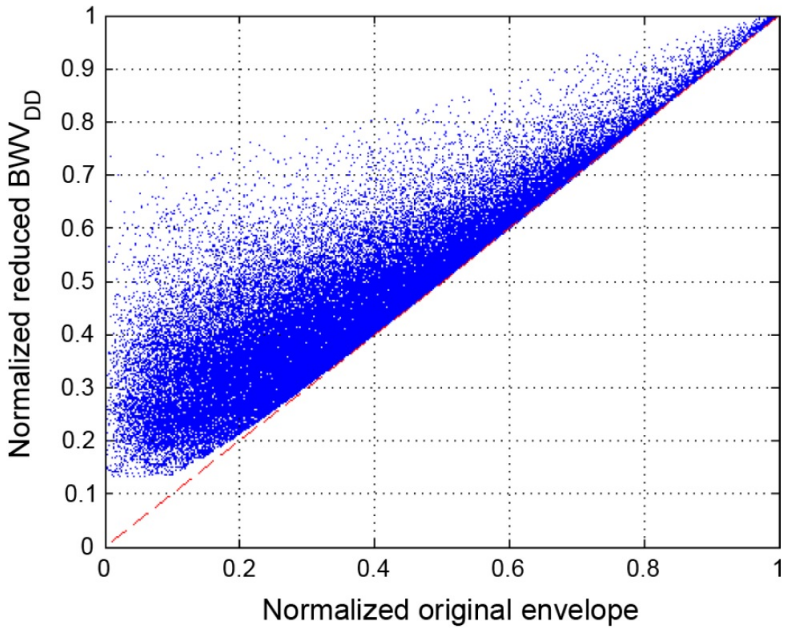


Figure 2.17: The supply voltage corresponding to a particular envelope level has a wide spread in an ET system [11].

The above observations have several implications. First, for accurate predistortion, the AM-AM and AM-PM of the linear PA in an ET system have to be characterized under a sufficient number of supply voltages over the entire output range of the envelope modulator;

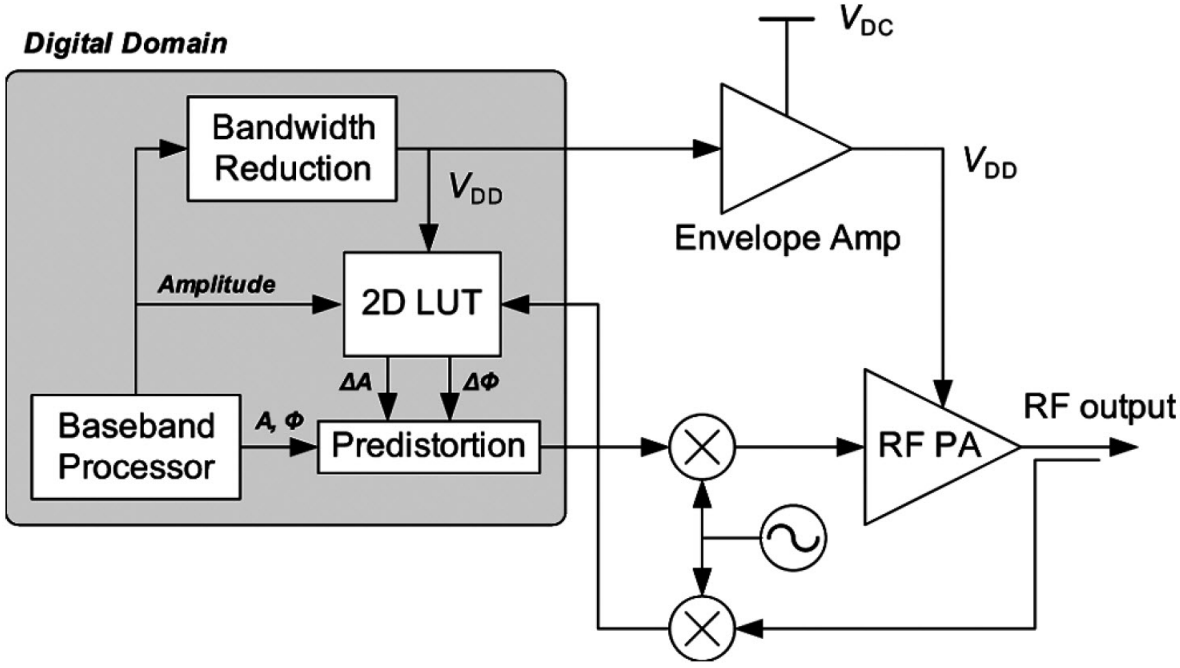


Figure 2.18: Digital predistortion for an envelope tracking PA [11].

therefore the LUTs for digital predistortion in an ET system are of much larger size compared to a standalone linear PA; therefore, predistortion for an ET PA is usually much more power hungry. Second, the time-domain output waveform of the supply modulator has to be predicted accurately for an effective feedforward digital predistortion (Fig. 2.18). To satisfy that requirement, the bandwidth of the supply modulator has to be high enough compared to its regulated output. Meanwhile, if the supply modulator employs a hybrid architecture to optimize for power efficiency, bandwidth and spectral purity, the transient handoff between the linear and the switching regulator has to be modeled accurately, especially during large and sharp supply transitions. The requirement for an accurate, power-efficient and self-calibrated digital predistortion scheme has posed serious challenges to the design of an ET TX. The ET transmit spectrum often times have humps in the out-of-band (e.g. at 100–300MHz offset) as a signature of inadequate predistortion ([32][11]).

2.5 Impedance Modulation

When PA power is low, the impedance seen at the drain can be increased to boost voltage swing and efficiency. To understand this, consider an idealized design where the powers from two identical PAs (PA1 and PA2) are transformer (XFMR) power-combined and delivered to the load, R_L (Fig. 2.19). The two sections of the XFMR are connected in series at their secondaries for power combining. In the following analysis, the $\sqrt{2}$ factor correlating

root-mean-square with peak value for a sine-wave is skipped for simplicity.

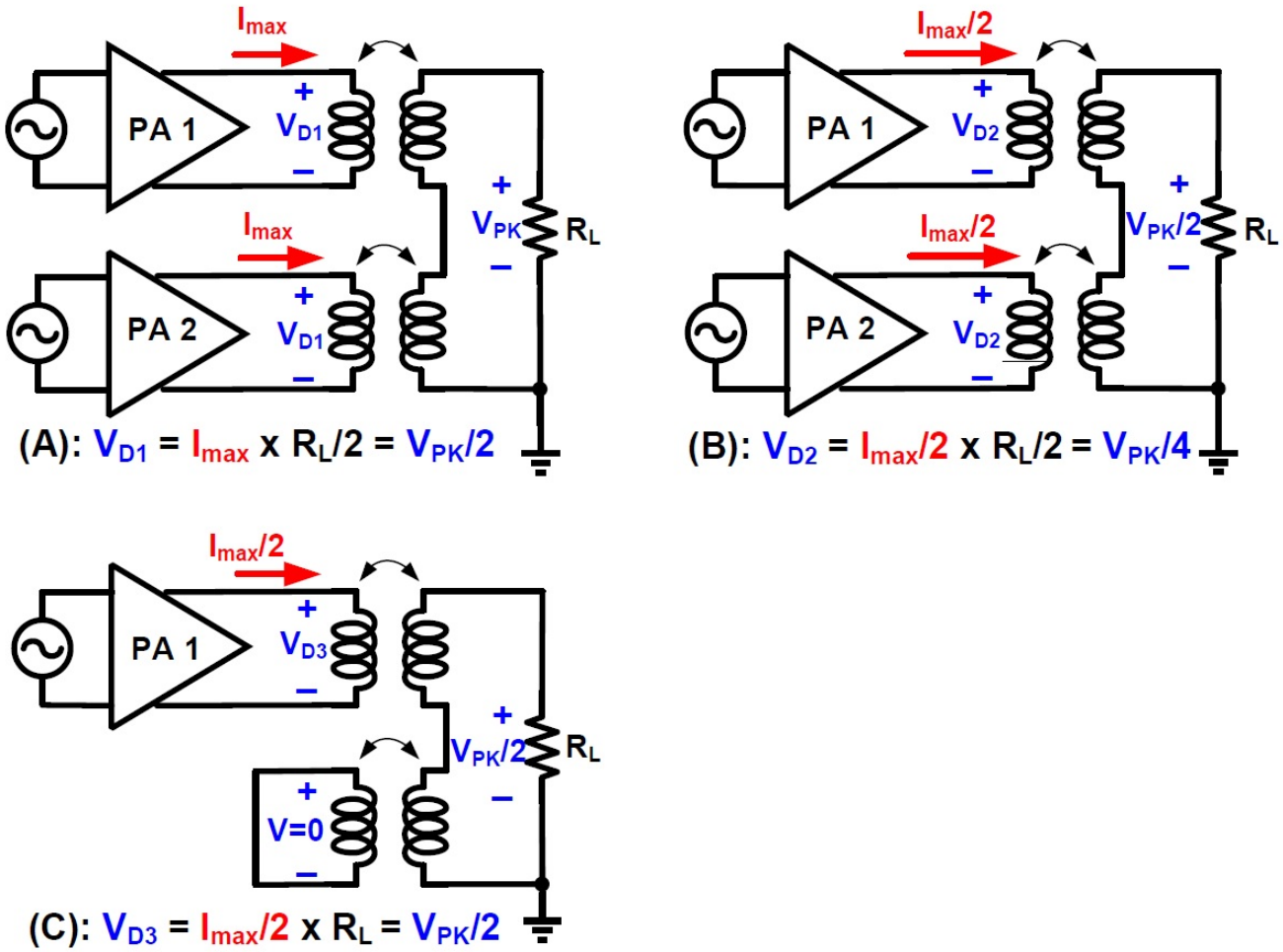


Figure 2.19: Efficiency enhancement through boosted drain impedance.

In the case where the peak power is required (Fig. 2.19(A)), each PA is delivering the maximum signal current, I_{max}, and sees equal load impedance, Z_{D1}, at its drain due to the transformer action.

$$Z_{D1} = \frac{1}{2} \times R_L \tag{2.13}$$

The drain voltage swing is therefore

$$V_{D1} = \frac{1}{2} \times I_{max} \times R_L \tag{2.14}$$

In a proper design, the drain voltage swing is the maximum allowed by reliability. Due to the transformer operation, the signal voltage across the load is

$$V_{R_L1} = 2 \times V_{D1} = I_{max} \times R_L \tag{2.15}$$

and the signal current flowing into the load is

$$I_{R_L1} = I_{max} \tag{2.16}$$

In this case, each PA is delivering a power of

$$P_{PA1} = V_{D1} \times I_{max} = \frac{1}{2} \times I_{max}^2 \times R_L \tag{2.17}$$

And the total power delivered to the load is

$$P_{R_L1} = V_{R_L1} \times I_{R_L1} = I_{max}^2 \times R_L \tag{2.18}$$

Consider a second case (Fig. 2.19(B)) where the output power delivered to the load is backing off by 6dB through halving the drain current of each PA (gate/base modulation through the g_m of the power transistors). Since each PA is still operating concurrently and identically, it still sees half the load impedance

$$Z_{D2} = \frac{1}{2} \times R_L = Z_{D1} \tag{2.19}$$

Since the drain current is reduced to half the peak value to achieve the power backoff, the drain voltage swing is also half the peak value

$$V_{D2} = \frac{1}{2} I_{max} \times \frac{1}{2} R_L = \frac{1}{4} I_{max} \times R_L = \frac{1}{2} \times V_{D1} \tag{2.20}$$

And the swing across the load is halved accordingly

$$V_{R_L2} = 2 \times V_{D2} = \frac{1}{2} \times I_{max} \times R_L = \frac{1}{2} \times V_{R_L1} \tag{2.21}$$

Also, the signal current flowing into the load is

$$I_{R_L2} = \frac{1}{2} \times I_{max} = \frac{1}{2} \times I_{R_L1} \tag{2.22}$$

In this case, each PA still delivers the same output power to the load

$$P_{PA2} = V_{D2} \times \frac{1}{2} I_{max} = \frac{1}{8} \times I_{max}^2 \times R_L = \frac{1}{4} \times P_{PA1} \tag{2.23}$$

And the total power delivered to the load is a quarter of the peak power (i.e. 6-dB backoff from P_{sat})

$$P_{R_L2} = V_{R_L2} \times I_{R_L2} = \frac{1}{4} \times I_{max}^2 \times R_L = \frac{1}{4} \times P_{R_L1} \tag{2.24}$$

Consider a third case (Fig. 2.19(C)) where the output power is still at 6-dB backoff but the drain impedance presented to PA1 is boosted. This is achieved by simultaneously turning on PA1, disabling PA2 and shorting the PA2 XFMR primary such that PA1 sees the full of the load impedance, R_L, at its drain

$$Z_{D3,PA1} = R_L = 2 \times Z_{D2} \tag{2.25}$$

Note the drain current of PA1 is the same as in the second case (Fig. 2.19(B)). Therefore, the drain voltage swing of PA1 is increased by two times

$$V_{D3,PA1} = \frac{1}{2} \times I_{max} \times R_L = 2 \times V_{D2} \tag{2.26}$$

And the swing across the load is the same as the second case

$$V_{R_L3} = 1 \times V_{D3,PA1} = \frac{1}{2} \times I_{max} \times R_L = V_{R_L2} \tag{2.27}$$

Also, the signal current flowing into the load remains unchanged

$$I_{R_L3} = \frac{1}{2} \times I_{max} = I_{R_L2} \tag{2.28}$$

In this case, only PA1 is delivering power to the load

$$P_{PA3} = V_{D3,PA1} \times \frac{1}{2} I_{max} = \frac{1}{4} \times I_{max}^2 \times R_L = 2 \times P_{PA1} \tag{2.29}$$

And the total power delivered to the load is identical to the second case

$$P_{R_L3} = V_{R_L3} \times I_{R_L3} = \frac{1}{4} \times I_{max}^2 \times R_L = P_{R_L2} \tag{2.30}$$

According to Eq.(2.1), since the PA1 drain current is the same but the drain voltage swing is doubled with respect to the second case, the drain efficiency is also doubled

$$\eta_3 = 2 \times \eta_2 \tag{2.31}$$

To see this, note Eq.(2.1) can be re-written in terms of drain voltage and current due to the transformer action

$$\eta_{de} = \frac{P_{out}}{P_{supply}} = \frac{I_{out}}{I_{vdd}} \times \frac{V_{out}}{V_{dd}} \propto \frac{I_{drain}}{I_{vdd}} \times \frac{V_{drain}}{V_{dd}} \tag{2.32}$$

In other words, the total current drawn from the PA supply is reduced to half in the third case as opposed to the second case since PA2 is disabled and PA1 delivers the same level of drain current; therefore the third case has twice the efficiency of the second case. If the normalized drain current is held constant regardless of power levels as in the case of a class-B PA or a PA with direct digital amplitude modulation as discussed in Section. 2.6, the drain

efficiency in the third case is actually the same as the first (i.e. at peak power) because the normalized drain current is the same in between. Therefore, we have

$$\eta_1 = \eta_3 = 2 \times \eta_2 \tag{2.33}$$

The above equations for the three different cases are summarized in Table. 2.4. At a single low power level (6-dB backoff), the drain impedance can be boosted to increase voltage swing with the same drain current, and restore efficiency to its peak value. As powers reduce from 6-dB backoff, the efficiency again decreases from the peak as in class-B. The scheme does not help with efficiency for powers higher than 6-dB backoff, where lower impedance is required. Efficiencies for an ideal class-A PA, class-B PA and a class-B PA with the above impedance modulation are plotted in Fig. 2.20, where peak efficiencies are assumed to be the same.

Table 2.4: Summary of efficiency enhancement through boosted impedance.

Scenario	Fig. 2.19(A)	Fig. 2.19(B)	Fig. 2.19(C)
P_{out}	0 dB	-6 dB	-6 dB
Drain Z	1x	1x	2x
Drain I_{swing}	1x	0.5x	0.5x
Drain V_{swing}	1x	0.5x	1x
Drain η	1x	0.5x	1x

The idea can be extended to more than two sections of XFMRs/sub-PAs with finer impedance control and potentially larger efficiency improvement ([12][33]), as shown in Fig. 2.21. However, that is often accompanied by an undesirably large layout area due to increased number of XFMR sections, unless more XFMR sections are in any case required to extract very high power levels (e.g. 1-Watt) out of CMOS PAs ([33]). At the same time, while [12], [34] and [35] adjusted impedance statically for power control, recent works ([33][36]) also demonstrate that the impedance can be modulated dynamically according to the instantaneous envelope levels to enhance average efficiency for a fixed transmit power.

Efficiency enhancement through impedance modulation is compared against class-B back-off characteristic for various works (Table. 2.5). A 15–30% of improvement has been achieved by impedance modulation. Increased XFMR loss when the multi-sections are driven differently adversely affects the efficiency at back-off mode. Furthermore, the employment of dynamic impedance modulation to track the dynamics of the envelope requires the XFMR and the associated impedances be switched fast enough and in timing synchronization with the rest of the modulation scheme. These two topics are discussed in more detail in the following chapters.

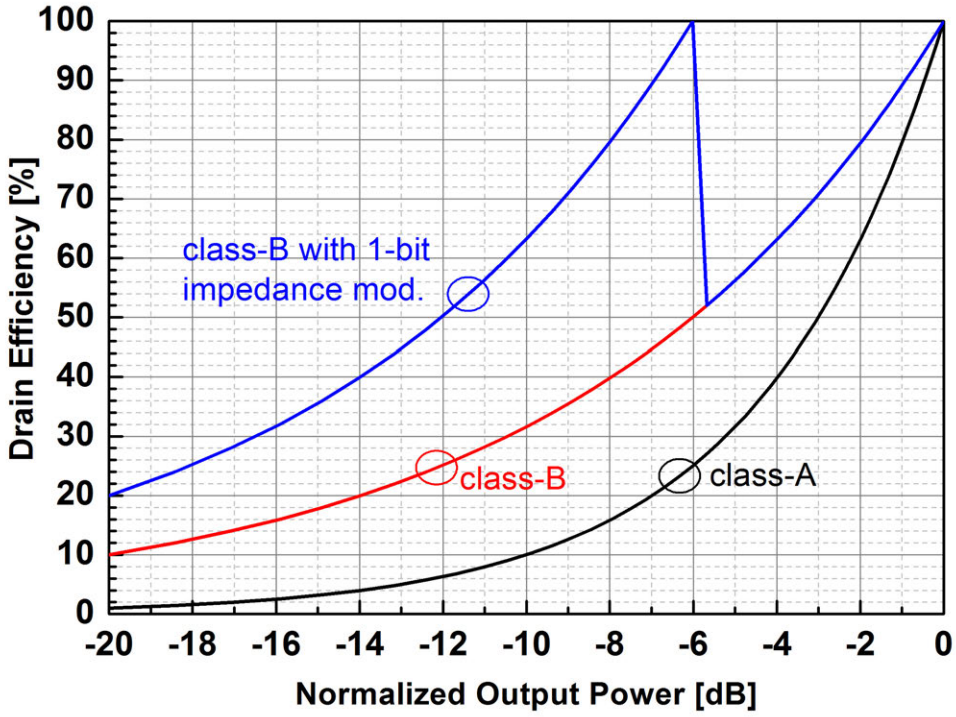


Figure 2.20: Efficiency back-off characteristics for an ideal class-A, class-B and class-B PA with 1-bit drain impedance modulation

Table 2.5: Efficiency backoff characteristic with impedance modulation.

Ref	Appl.	P_{sat}/η **[dBm/%]**	P_{out}/η **[dBm/%]**	**Class-B η/enhance [%/1x]**
[12]	WLAN OFDM	27.0 / 32	14.5 / 9	7.6 / 1.18
[34]	WiMAX OFDM	30.1 / 33	18.0 / 10.4	8.2 / 1.27
[35]	WLAN OFDM	31.0 / 34.8	22.3 / 15	12.8 / 1.17
[33]	WLAN OFDM	31.5 / 27	24.8 / 16	12.5 / 1.28 [1]
[36]	WLAN OFDM	23.3 / 43	16.8 / 24.5	20.3 / 1.21

[1] The efficiency enhancement is also partially from an outphasing PA architecture.

2.6 Direct Digital Amplitude Modulation

As discussed in Section. 2.3, in a polar TX, the modulated signal is decomposed into the amplitude and the phase path. While the amplitude path conveys a non-linear envelope at

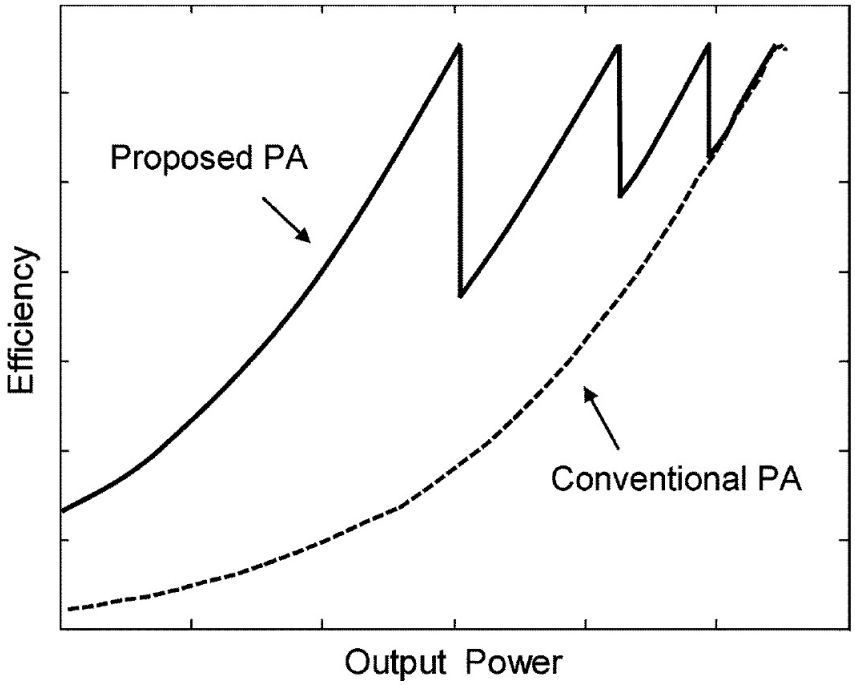


Figure 2.21: Efficiency enhancement through multi-level drain impedance modulation [12].

baseband, the phase path carries constant-envelope and phase-modulated RF signal to the gate/base input of the PA. Mathematically, the RF signal transmitted by a Cartesian TX can be written as a function of its quadrature components as

$$s(t) = I_{BB}(t)\cos(\omega_c t) - Q_{BB}(t)\sin(\omega_c t) \tag{2.34}$$

where ω_c is the carrier frequency and $I_{BB}(t)$ and $Q_{BB}(t)$ are the time-domain baseband signals. The polar equivalent of the transmitted signal is

$$s(t) = A(t)\cos(\omega_c t + \phi(t)) \tag{2.35}$$

where the amplitude component is

$$A(t) = \sqrt{I_{BB}(t)^2 + Q_{BB}(t)^2} \tag{2.36}$$

and the phase component is

$$\phi(t) = \arctan(\frac{Q_{BB}(t)}{I_{BB}(t)}) \tag{2.37}$$

A Polar TX with direct digital amplitude modulation has been proposed as another way to optimize for efficiency and linearity ([3][37][38][39][40][41][13][42]). Instead of relying on a high-bandwidth supply modulator to convey the nonlinear envelope as in an analog

polar scheme, a direct digitally modulated polar TX achieves the amplitude modulation by turning on a discrete number of unit PA elements (Fig. 2.22). In other words, the amplitude modulation is realized by the RF Digital-to-Analog Conversion (RF-DAC). The nomenclature of "direct digital amplitude modulation" emphasizes the fact that the digital modulation is applied directly on the PA (i.e. the "RF-DAC"), which is different from a conventional TX where the digital modulation first acts on the baseband DAC and is then fed to the PA through several intermediate stages.

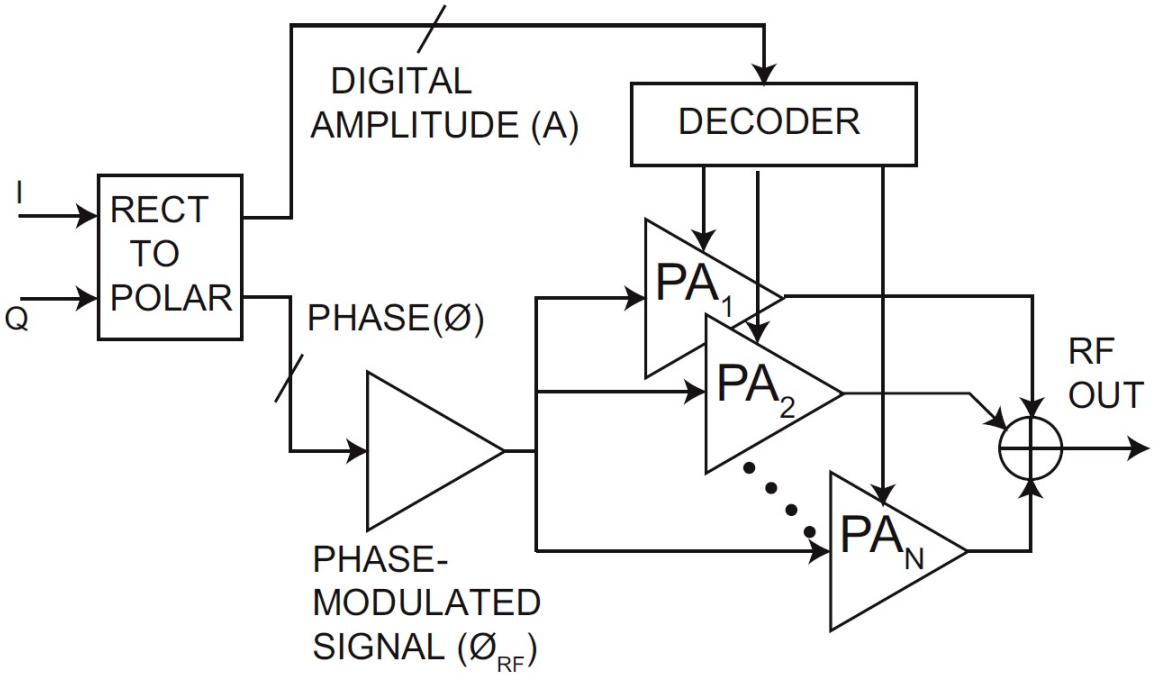


Figure 2.22: A polar TX with direct digital amplitude modulation [3].

Since the core PA in a direct digitally modulated polar TX is only driven by a constant-envelope RF signal and does not have to convey the nonlinear envelope from its gate/base modulation, the PA is typically implemented as a more efficient switching class (e.g. class-D/E/F). As a result, the peak efficiency of the core PA can be higher compared to the TX where a linear class-AB PA is employed. Meanwhile, because the unit PAs, when turned on, are always driven by rail-to-rail signals, the total drain current of the core PA as normalized by supply current, is a constant regardless of power levels. Therefore, the digital amplitude modulation scheme inherently offers a class-B efficiency backoff characteristic, as shown in Fig. 2.23. Although the back-off characteristics are only as good as an ideal class-B PA, the peak drain efficiency from which the back-off starts is higher in the digitally modulated polar TX due to the use of a switching-mode PA. That is illustrated in Fig. 2.24, where drain efficiencies of an ideal class-A, class-B and digitally-modulated PA with class-B backoff are plotted.

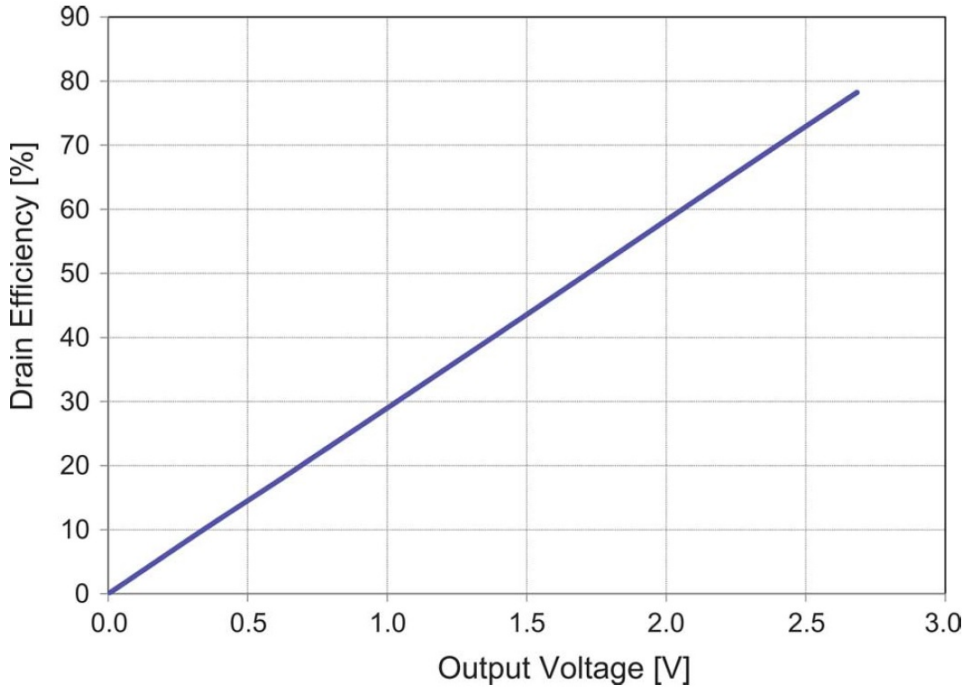


Figure 2.23: Linear back-off of drain efficiency with output amplitude in a polar TX with direct digital amplitude modulation [13].

Since amplitude modulation is realized by the RF-DAC operation, the baseband DAC and the up-conversion mixer in a conventional Cartesian TX are no longer required on the amplitude path of the digital polar TX system (Fig. 2.25). That helps to save overall TX power consumption. Although the polar phase path would still require the DAC and the mixer, they can be implemented in an efficient way not to introduce excessive power overhead ([36]).

The direct amplitude modulation scheme also potentially offers better linearity after predistortion. That is because the amplitude modulation and predistortion, without going through the DAC, the filter, the up-conversion mixer, and the PA driver as in a conventional TX chain, are directly applied to the final PA stage. Therefore the time-domain amplitude response of the PA can be predicted more accurately and also can be better correlated with the static (continuous-wave) AM-AM and AM-PM measurements in a self-calibrated predistortion scheme. As a result, the predistortion can be applied more efficiently and accurately due to less involvement of non-linearities of other baseband and RF stages.

State-of-the-art digitally-modulated PAs are benchmarked against the class-B backoff characteristic in Table. 2.6. In [39] and [40], the average efficiencies at OFDM output power levels are much better than class-B. However, the continuous-wave (CW) measurements reported in those works show a lower efficiency at similar power levels. [39] also confirms the linear back-off of drain efficiency with output amplitude in the CW measurements. In [42], a

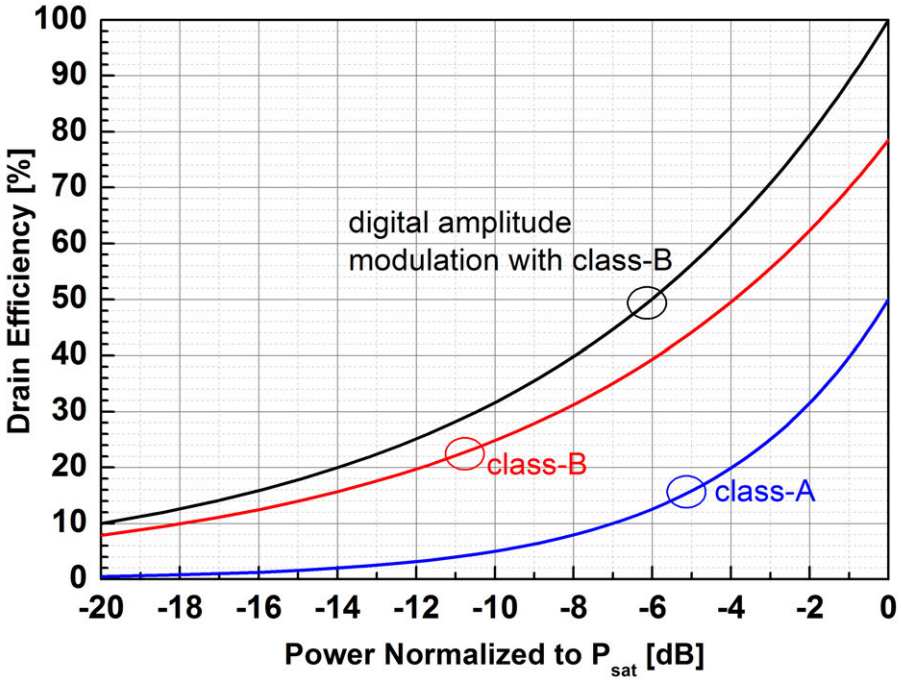


Figure 2.24: Drain efficiency of an ideal class-A, class-B and digitally-modulated PA with class-B backoff.

switched-capacitor based architecture is used to achieve much better back-off characteristic than class-B; however, the FCC spectral mask for WLAN 802.11g is violated by 3–5dB at 30MHz offset and above.

Table 2.6: Efficiency backoff characteristic with digital amplitude modulation.

Ref	**Appl.**	P_{sat}/η **[dBm/%]**	P_{out}/η **[dBm/%]**	**Class-B** η **[%]**
[3]	WLAN OFDM	N.A.	13.6 / 6.7	N.A.
[39]	WiMAX OFDM	24.0 / 47.6	15.3 / 22	17.5
[40]	WLAN OFDM	24.8 / 51	16.7 / 24	20.1
[41]	WLAN OFDM	N.A.	17.0 / 14	N.A.
[13]	WLAN OFDM	21.8 / 44	14.0 / 18	17.9
[42]	WLAN OFDM	25.2 / 45	17.7 / 27	19.0

In terms of spectral purity for co-existence, however, digitally-modulated PAs are often times inferior to their linear counterparts (e.g. class-A, class-B and class-AB analog PA) for two reasons. First, the sample-and-hold operation inherent within an RF-DAC creates images at multiples of the baseband sample rate; those spurs are usually at least 10–20dB

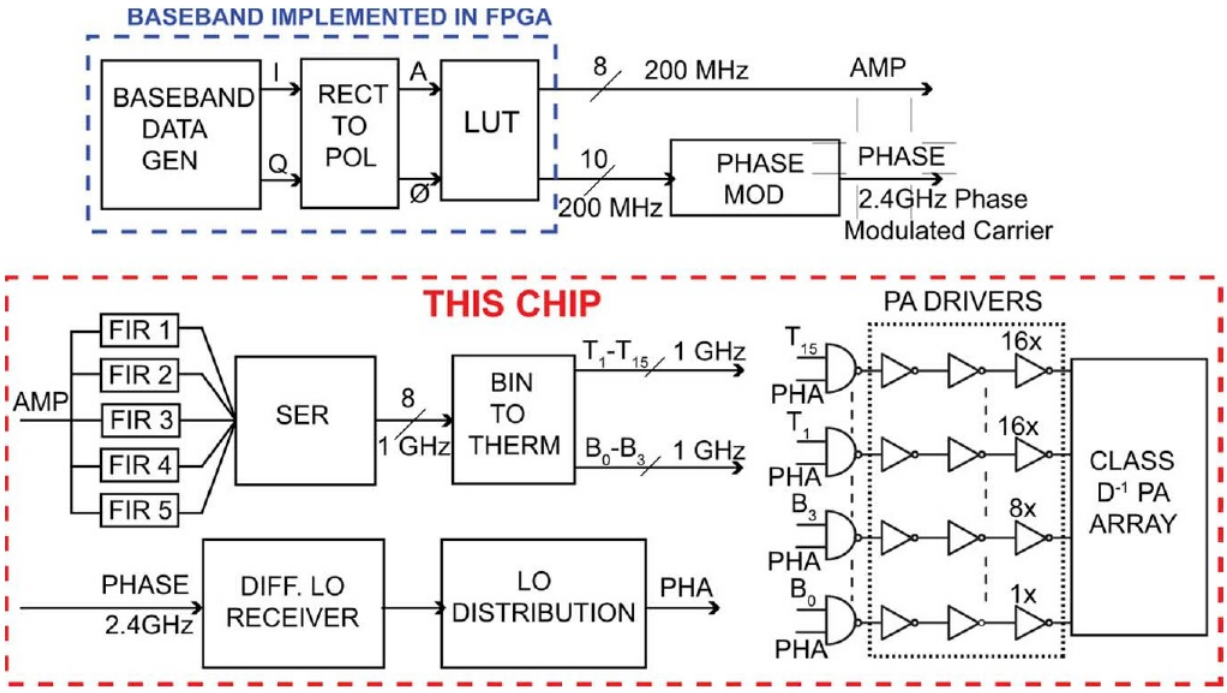


Figure 2.25: A direct digitally modulated polar TX system [13].

higher than the noise floor and require explicit RF filtering. Second, the out-of-band (OOB) noise floor is also limited by digital quantization, in addition to the Adjacent Channel Power Regrowth (ACPR) due to the TX non-linearities. Any additional RF filtering at the TX output to improve the spectral purity might significantly degrade the overall efficiency (by at least 1–2dB). That seriously limits the application of efficient, digitally-modulated PAs for high-power wireless communications where stringent spectral performances is required.

2.7 Conclusion

Various block-level efficiency enhancement techniques are briefly introduced and benchmarked against the class-B backoff characteristic. Dynamic current biasing achieves at best a class-B backoff, but typically requires a memory element for envelope averaging, posing challenges to static predistortion. Analog polar modulation, or Envelope Elimination and Restoration (EER) shifts the problem of the design of a linear and back-off efficient power amplifier at RF to that of a high-bandwidth, low-spur and back-off efficient supply modulator at baseband. Envelope Tracking (ET) attempts to relieve the design requirements on the supply modulator by further splitting the amplitude path into supply modulation as well as gate/base modulation paths. Also, the delay matching requirement between the supply modulation path and the rest of the modulation schemes is more relieved in an ET system

as compared to in an EER system. However, the predistortion in an ET system involves the interactions between the supply and the gate/base modulation path, which typically requires a multi-dimensional look-up-table as well as accurate predictions of the time-domain behavior of the supply modulator. The impedance modulation provides another way of making the transistor RF voltage swing track the supply voltage at back-off power levels, and offers a relative improvement of 10–30% in the average efficiency. The direct digital amplitude modulation scheme in a "polar" TX realizes the non-linear envelope by turning on a dynamically varying number of unit elements (the "RF-DAC" operation). The efficiency in such a digital amplitude modulation scheme is therefore able to back-off from a higher peak efficiency with class-B characteristic. The digital amplitude modulation scheme is also more amenable to digital predistortion, because of the direct application of the modulation on the core RF-DAC.

Some of the techniques discussed above are able to offer a relative efficiency improvement of 10–40% with respect to a class-B reference backing off from the same peak efficiency. Those promising results can potentially extend the continuous standby cycle of a battery operated mobile terminal by more than 20%. However, relatively few works have integrated these techniques into a complete TX and examined the linearity-efficiency trade-off at a system level and/or in the context of radio co-existence. For example, most designs employing digital polar or outphasing architecture often realized phase modulation off-chip. Similarly, while good close-in spectral performance has been demonstrated, far-out spectral images remain problematic for TXs where the Digital-to-Analog Conversion is incorporated into the PA itself. At the same time, out-of-band noise humps and spurs often times show up in an EER/ET system where a switching regulator is employed to accomplish efficient supply modulation and/or the pre-distortion is not complete and accurate enough to take into account the interactions between the supply modulation and the RF signal path. Moreover, previous works often do not include overhead from components such as extra DC-DC converters for multiple PA supplies or did not implement on-chip matching networks (MNs) and/or baluns, all of which directly affect the overall efficiency of integrated CMOS TXs.

With a high level of system integration, our work attempts to re-investigate the various design trade-offs herein while providing some concrete numbers in terms of efficiency, linearity and spectral purity that have been achieved by our silicon prototype ([36]) in a practical way. Part II describes the design and analysis of a digitally-modulated polar transmitter with dynamic impedance modulation for IEEE 802.11g application, as well as the measurement results for the silicon prototype, which forms the core of our research work.

Part II

Design of Digitally Modulated TX for Efficiency Enhancement

Chapter 3

TX System Level Considerations

3.1 Target Application: IEEE 802.11g

The target application for this prototype is the IEEE 802.11g (WLAN) standard employing the OFDM modulation scheme. It should be noted that most of the system-level considerations presented in this chapter are also applicable to other wireless communication applications, especially those that also employ OFDM, such as WiMAX and 4G-LTE standards.

OFDM modulation helps the WLAN standard to achieve good spectral efficiency and cope with severe channel conditions (e.g. Inter-Symbol Interference (ISI) and frequency-selective fading due to multi-path) without complicated equalization filters. Each OFDM symbol consists of 52 sub-carriers, out of which 4 are pilot tones and the remaining 48 carry the data. On a per-sub-carrier basis, the modulation dependent parameters are shown in Table. 3.1.

In Table. 3.1, the data bits per symbol, N_{DBPS}, can also be easily calculated as

$$N_{DBPS} = N_{BPSC} \times N_{SD} \times R_C \tag{3.1}$$

where N_{BPSC}, N_{SD} and R_C are the coded bits per sub-carrier, the number of data sub-carriers, and the coding rate, respectively. The data rate is therefore

$$R_D = \frac{N_{DBPS}}{T_{\text{SYM}}} \tag{3.2}$$

where T_{SYM}, the symbol interval, is

$$T_{\text{SYM}} = T_{FFT} + T_{GI} \tag{3.3}$$

and T_{FFT}, the Inverse Fast Fourier Transform (IFFT) / Fast Fourier Transform (FFT) period, is

$$T_{FFT} = \frac{1}{\Delta_F} \tag{3.4}$$

Table 3.1: 802.11g Modulation-dependent parameters

Subcarrier Modulation	**Coding Rate**	**Coded Bits per Subcarrier**	**Coded Bits per OFDM Symbol**	**Data Bits per OFDM Symbol**	**Data Rate [Mbps]**	**Max EVM [dB]**
BPSK	1/2	1	48	24	6	-5
BPSK	3/4	1	48	36	9	-8
QPSK	1/2	2	96	48	12	-10
QPSK	3/4	2	96	72	18	-13
16-QAM	1/2	4	192	96	24	-16
16-QAM	3/4	4	192	144	36	-19
64-QAM	2/3	6	288	192	48	-22
64-QAM	3/4	6	288	216	54	-25

in which the sub-carrier frequency spacing, Δ_F, is

$$\Delta_F = \frac{20\text{MHz}}{64} \tag{3.5}$$

and the duration of the guard interval (for ISI prevention), T_{GI}, is

$$T_{GI} = 0.8\ [\mu s] \tag{3.6}$$

The various frequency- and timing-related parameters are summarized in Table. 3.2. As shown in Table. 3.1 and Table. 3.2, with an occupied bandwidth of 16.6MHz and a channel bandwidth of 20MHz, 802.11g supports a data rate up to 54Mbps. The carrier frequency is from 2412MHz to 2484MHz, spanning a frequency range from 2401 to 2495MHz.

The digitally-modulated TX therefore has to meet the EVM requirement of -25dB to support the highest rate. In practice, 2–3dB of EVM margin is budgeted for the degradations from the antenna impedance mismatch and extreme Process Voltage and Temperature (PVT) corners. Those considerations lead to a measured EVM of -28dB at 54Mbps for the typical case. In addition, the transmit spectrum has to satisfy the mask (Fig. 3.1) as regulated by the Federal Communication Commission (FCC) within the US.

3.2 Spectral Purity for Coexistence

As discussed in Chap. 1, coexistence among multiple radios is an important concerns for contemporary consumer products. Due to the high occupancy around the 2.4GHz Industrial, Scientific and Medical (ISM) band, coexistence considerations pose serious challenges even to

Table 3.2: 802.11g Frequency and timing related parameters

Parameter	**Symbol**	**Value**
Number of total sub-carriers	N_{ST}	52
Number of data sub-carriers	N_{SD}	48
Number of pilot sub-carriers	N_{SP}	4
Sub-carrier frequency spacing	Δ_F	312.5kHz
Occupied bandwidth	BW_O	16.6MHz
Occupied bandwidth	BW_{CH}	20.0MHz
Fourier period	T_{FFT}	$3.2\mu s$
Duration of guard interval	T_{GI}	$0.8\mu s$
Symbol interval	T_{SYM}	$4.0\mu s$

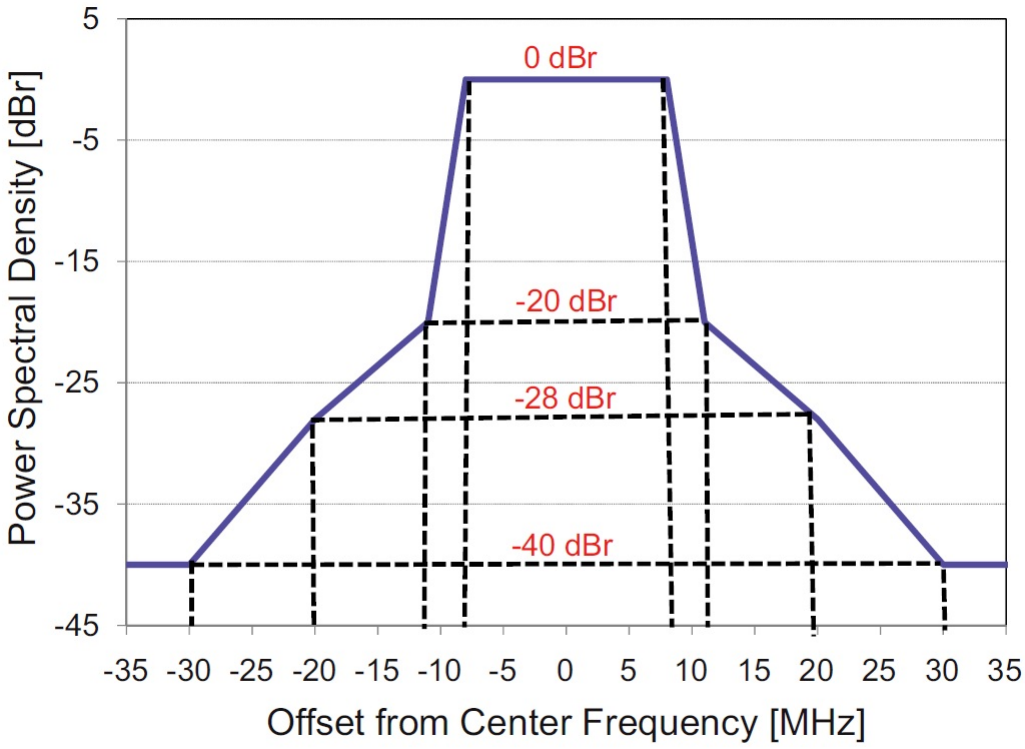


Figure 3.1: The transmit spectral mask of 802.11g [2].

a conventional analog PA. As shown in Fig. 3.2, the worst-case offset between the 2412MHz carrier of 802.11g and the LTE band edge is only 30–40MHz. In this case, the WLAN transmit spectrum should be ideally down to the thermal noise floor at 40–50MHz offset ([43]), which is typically achieved by cascading a bandpass Film Bulk Acoustic Resonator (FBAR) filter with very sharp roll-off characteristic (Fig. 3.3) at the TX output. The filter inband loss (1–2dB), however, degrades the overall efficiency of the TX by 20–40%. Note that the filter attenuation performance degrades by 10–20dB at the far-out (Fig. 3.4), making a wideband filtering even more difficult.

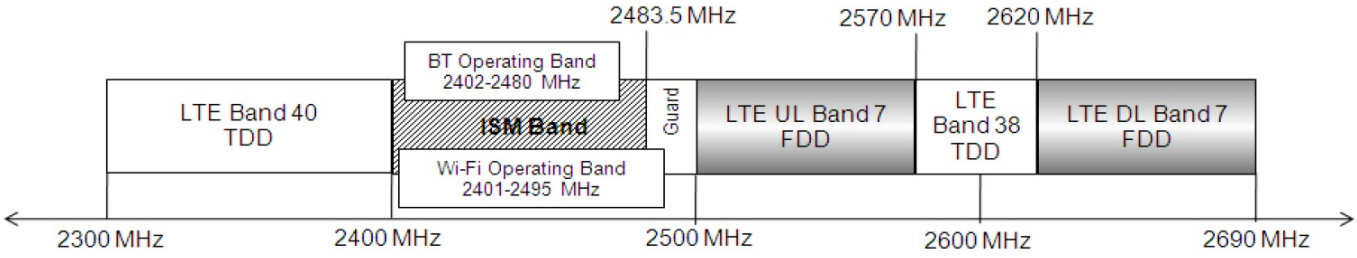


Figure 3.2: Coexistence of LTE with 2.4GHz WLAN and Bluetooth [14].

In a coexistence scenario, assuming the G-band WLAN and the LTE frontend are sharing the same antenna due to the frequency proximity, as well as a "close-in" attenuation of 40dB from the FBAR filter, the noise density immediately at the TX output should be below -130dBm/Hz at 50MHz offset in order to avoid significant desensitization to the LTE receiver (with -110dBm/MHz sensitivity). With a modest receiver sensitivity of -100dBm/MHz, the transmit spectrum should still be below -120dBm/Hz at 50MHz offset. This specification is still much more stringent than the FCC spectral mask and is challenging especially for the digitally-modulated TX where the out-of-band spectrum is also limited by digital quantization and image spurs (although the images are located only at some discrete frequencies).

As a result, in our design investigations on the digitally-modulated TX, we would like to compare the transmit spectrum not only with the mask from standard regulations, but also with co-existence requirements so as to achieve a truly efficient solution.

3.3 TX System Overview

To investigate efficiency enhancement techniques within a complete TX system, we have designed and fabricated a prototype for WLAN 802.11g in a 65nm digital bulk CMOS technology. The TX is implemented as a polar architecture, with digital amplitude modulation directly applied to the core RF-DAC (PA). The TX also includes a 1-bit dynamic impedance modulation technique to improve the PA efficiency at dynamic back-off power levels. The amplitude and phase paths are fully integrated along with baseband digital filters to suppress

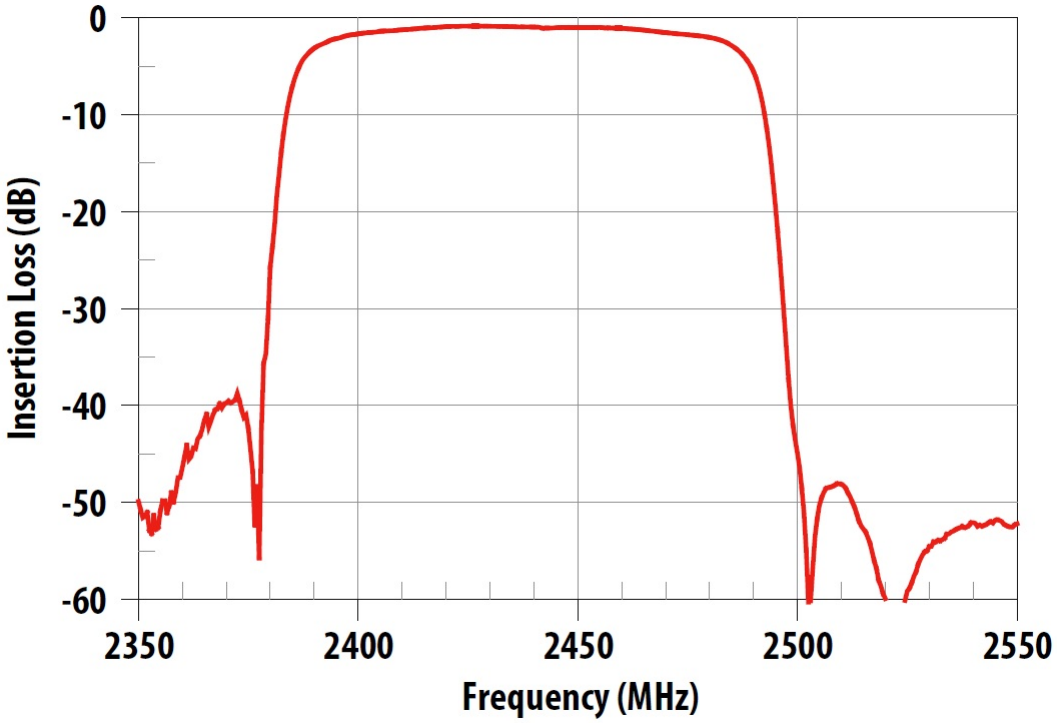


Figure 3.3: The close-in magnitude response of a typical ISM bandpass filter for LTE coexistence [15].

spectral images. A 9-bit open-loop phase path employs a phase interpolator architecture to achieve power-efficient wideband phase modulation. The core RF-DAC is a current-mode class-D differential cascode PA sliced into 8-bits with integrated matching network and output balun. The chip directly interfaces with the 50Ω environment without any explicit off-chip passive component. The PA runs off a separate 1.2V supply while the rest of the circuitry operate on 1V domains that are ultimately connected on-board.

In the following sections, we present our design investigations at a system level, and attempt to correlate circuit-level specifications (the PAPR, the amplitude and phase path resolution, the baseband sample rate and etc) with system-level performance (EVM, ACPR, the out-of-band noise floor and etc). System simulations at the transistor-level are time consuming and also include various artifacts that further complicate the overall picture. To get a clear idea of how a single circuit specification affects the system-level performances, we only performed system simulations (with Agilent ADS Ptolemy simulation) at a behavior level of an otherwise ideal TX except for the circuit specification that is currently under investigation. Due to the assumption of an almost ideal TX, we will allow margin for circuit-level non-idealities that are not captured in simulations in our system budget. After that, a more detailed behavior model including the various circuit non-idealities was simulated to verify the adequacy of the system performances.

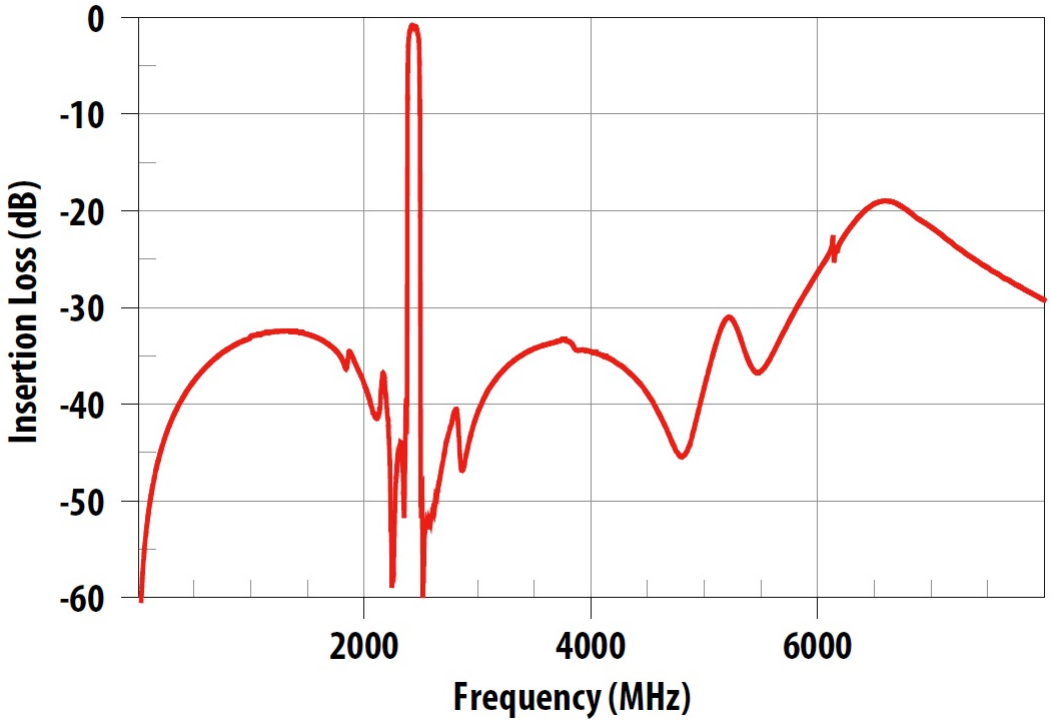


Figure 3.4: Wideband magnitude response of the same ISM bandpass filter for LTE coexistence [15].

3.4 Crest Factor Reduction

The Crest Factor, or Peak-to-Average-Ratio (PAR), is defined as the ratio between the peak magnitude and the root-mean-square (RMS) value of a waveform

$$C = \frac{|y|_{peak}}{y_{rms}} \tag{3.7}$$

The Peak-to-Average Power Ratio (PAPR), is related to the Crest Factor in the following way

$$\text{PAPR} = \frac{|y|^2_{peak}}{y^2_{rms}} = C^2 \tag{3.8}$$

According to Eq. (1.1), an 802.11g OFDM signal consisting of 52 sub-carriers has a theoretical PAPR of 17dB. However, the transient peak in the envelope which only occurs when all the sub-carriers attain to its maximum amplitude simultaneously is both rare and brief. As a result, it is possible to reduce the PAPR for the transmitted signal, as opposed to the original one, and therefore improve the transmit power and efficiency.

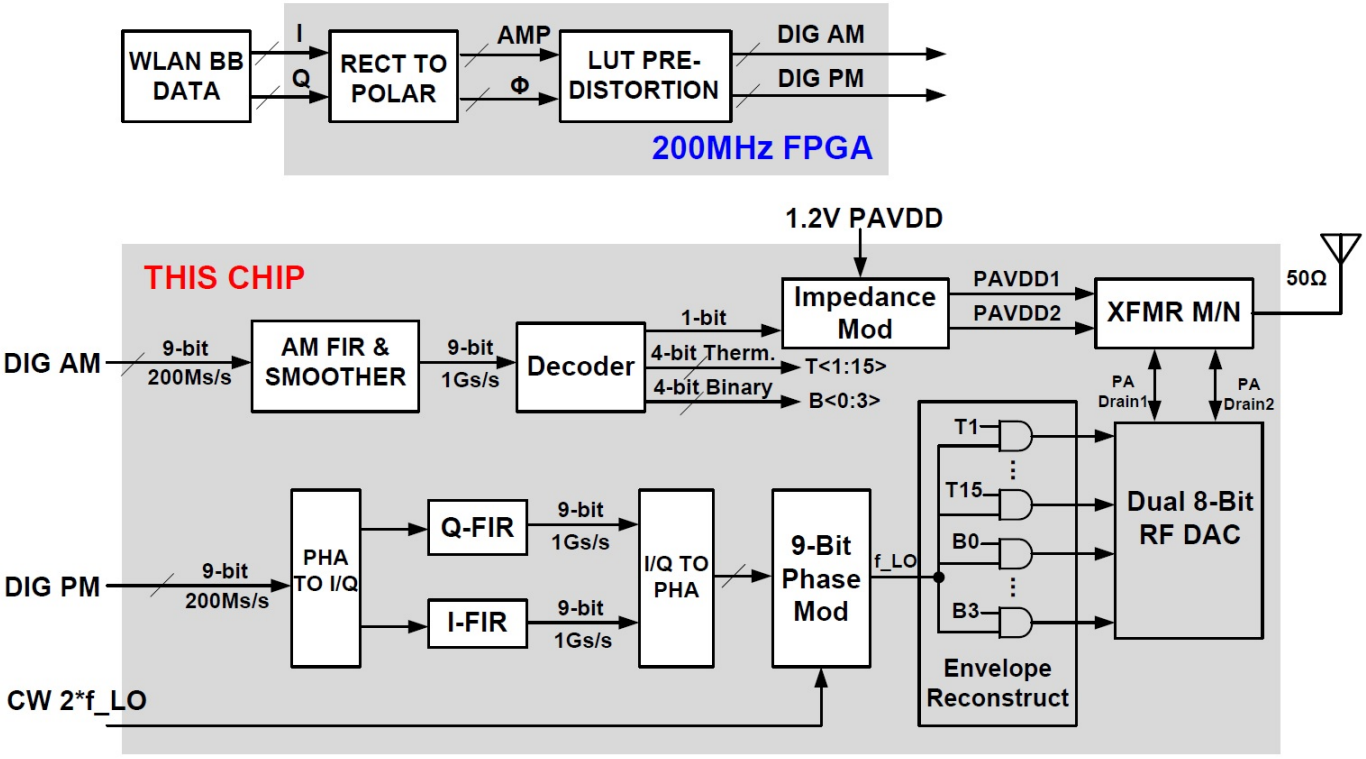


Figure 3.5: Block diagram of a digitally-modulated WLAN polar TX.

In the communications and signal processing community, Crest Factor reduction of OFDM signals is historically implemented by two groups of algorithms ([44][45]). The first group applies signal processing techniques at both the transmitter and the receiver side ([46][47]) to reduce PAPR without much degradation in Signal-to-Noise Ratio (SNR). However, these algorithms introduce a considerable overhead to the communicated signal and therefore tend to reduce the actual data rate, which is undesirable for high data-rate and spectrally efficient communications. Also, the requirement for additional processing functions at the receiver side makes the compatibility more challenging among products employing different algorithms. The second group of Crest Factor reduction algorithms essentially apply signal clipping only at the transmitter side ([48][49][50][51][52]). However, hard-clipping of the signal inevitably introduces in-band distortions and also increases out-of-band spectrum regrowth (which is in agreement with the famous saying that "the spectral efficiency in the frequency domain comes at the expense of an increased PAPR in the time domain"). To mitigate these issues, [49], [50], [51] and [52] have proposed an additional filtering on the clipped signals to reduce the ACPR degradation at 10–30MHz offsets. However, filtering tends to increase the PAPR of the clipped signal without much improvements in EVM; in [44], it was found that the hard-clipping only algorithm offers the lowest PAPR for a fixed EVM

target, as compared to a clipping+filtering algorithm. In this work, a simple hard-clipping is performed by the FPGA to reduce the PAPR of the transmitted signal.

To investigate the effect of Crest Factor reduction, system simulations are performed on an ideal polar TX with 9-bit amplitude and phase resolution and a baseband sample rate of 1Gs/s. For the in-band performances, EVM and ACPR (measured as a margin with respect to the FCC transmit mask at 30MHz offset) are compared (Fig. 3.6). It is seen from the figure that EVM is relatively sensitive to the Crest Factor, which improves by about 6dB for every dB increase of PAPR over a PAPR range of 5–8dB. To achieve an EVM of -28dB, the required PAPR for an ideal TX is roughly 5.5dB, which is much lower than the theoretical worst-case value of 17dB. The close-in ACPR is relatively insensitive to the Crest Factor reduction over an EVM range of -45—25dB. In measurements, the PAPR is chosen as the minimum value for the TX to satisfy a particular EVM target (e.g. -28dB) while the "cost" in terms of close-in ACPR degradations are assumed to be negligible.

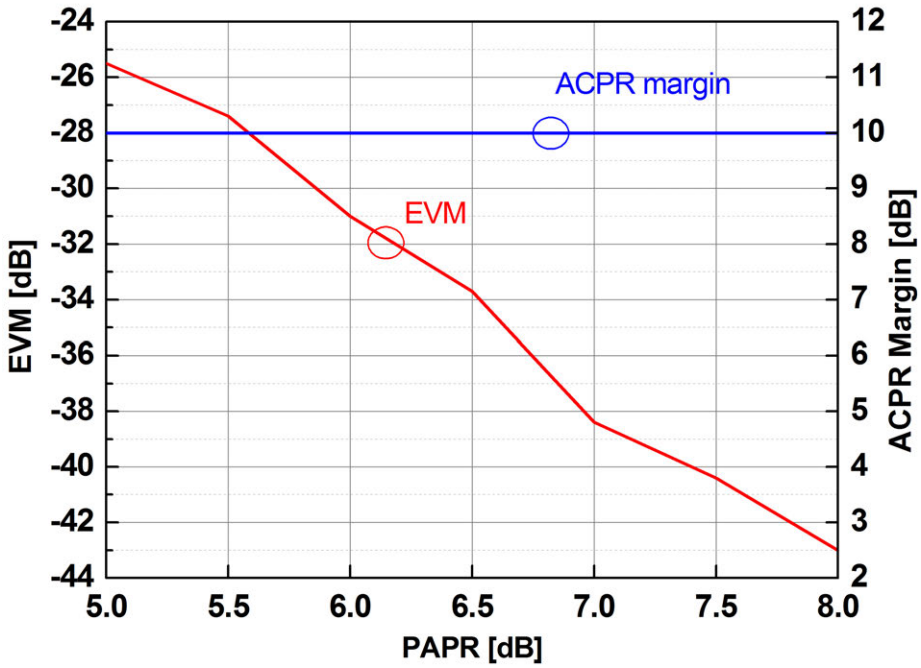


Figure 3.6: EVM and ACPR versus PAPR of an ideal WLAN TX.

Out-of-band spectral purity is also compared for different Crest Factor values (Fig. 3.7), measured as the ratio (dBr) between the signal power density, and the average noise power density between 250 and 350MHz offset. The higher the measured SNR, the better the out-of-band spectral purity. As can be seen from the figure, the far-out noise density is relatively insensitive to the Crest Factor over a PAPR range of 5–8dB.

In the following simulations, a PAPR of 6dB is used to introduce a reasonable amount of clipping while not limiting the performance. With 9-bit amplitude and phase resolution, the EVM is roughly -31dB with noise floor about 64dB down compared to the inband signal.

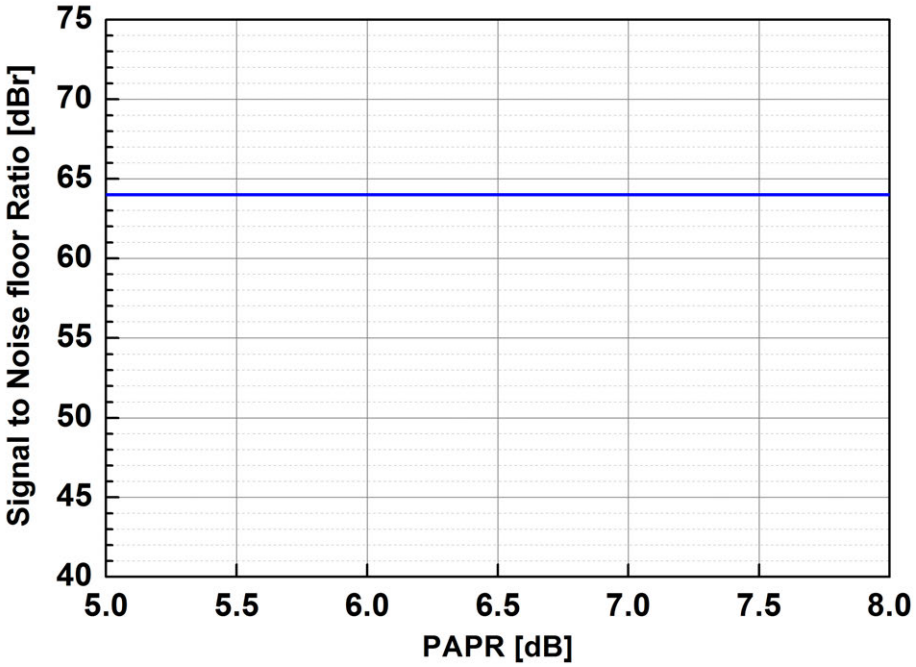


Figure 3.7: Out-of-band noise versus PAPR of an ideal WLAN TX.

3.5 Amplitude Resolution

The choice of amplitude and phase resolution is based upon two major considerations– signal integrity (as measured by EVM and close-in ACPR), and out-of-band noise floor. System simulations with 6dB of PAPR, 9-bit of phase resolution and 1Gs/s of baseband sample rate are performed the determine the effect of amplitude resolution on the in-band performances (Fig. 3.8). While 4-bit of amplitude resolution is still good enough to achieve a -30dB EVM, at least 5-bit of amplitude resolution is required to comfortably satisfy the close-in FCC spectral mask. With 4-bit amplitude resolution, the transmit spectrum barely meets the mask at 30MHz offset (Fig. 3.9).

Next, the effect of amplitude resolution on far-out noise floor is studied (Fig. 3.10). At low amplitude resolution regime, the noise floor is lowered by approximately 5dB for every 1-bit increase in the amplitude resolution, which is in good agreement with the classical relationship between the SNR and the number of bits

$$\text{SNR} = 6.02 \times N_{bits} + 1.76 \text{ [dB]} \tag{3.9}$$

where a full-scale sinusoidal signal is assumed. When the amplitude resolution is close to the 9-bit phase resolution, however, the slope of noise floor improvement becomes much more smooth with increasing the amplitude bits. When the amplitude resolution increases from 8-bit to 9-bit, the SNR barely changes. That means with an amplitude resolution of 8-bit, the noise floor is almost dominated by the 9-bit phase resolution. The different number of

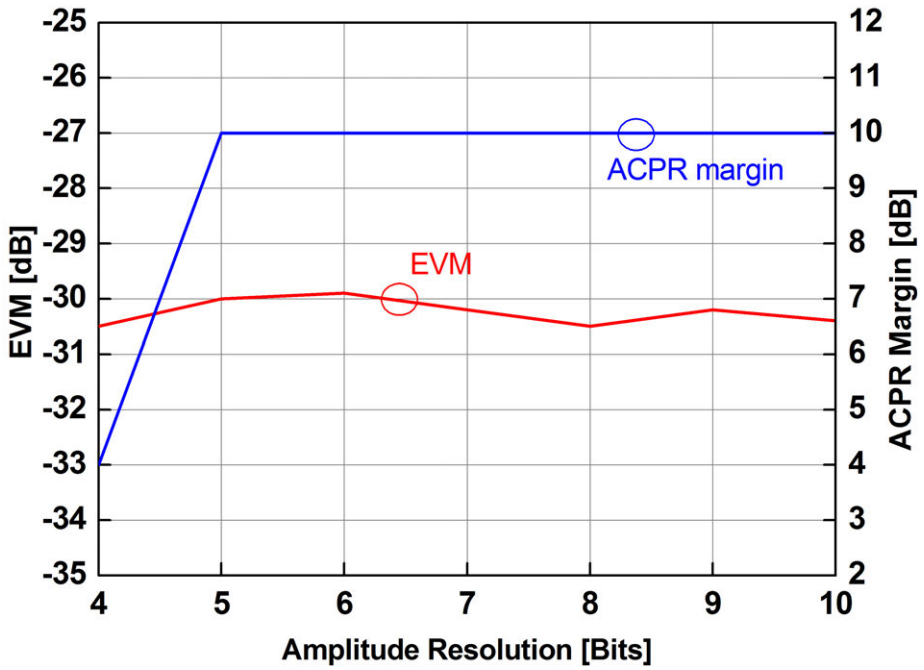


Figure 3.8: EVM and ACPR versus amplitude resolution of an ideal WLAN TX.

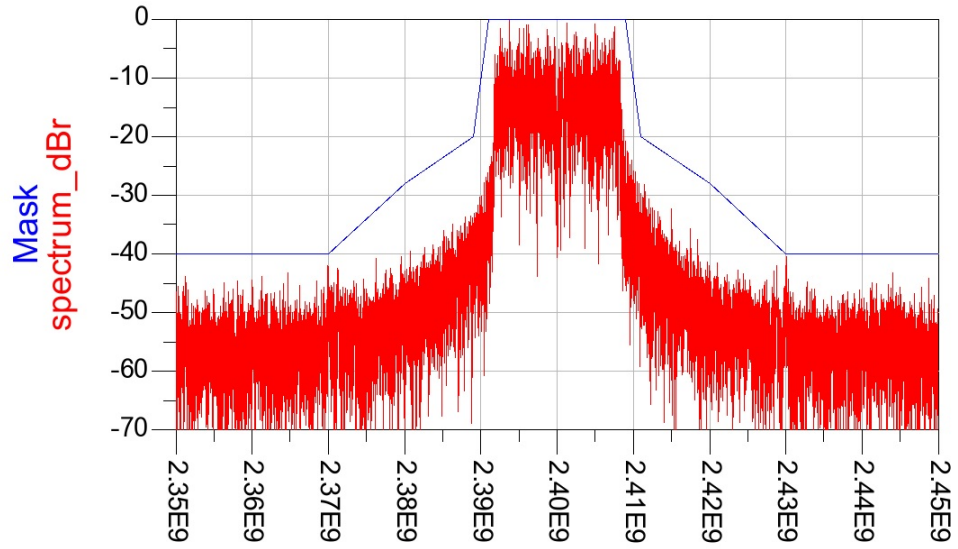


Figure 3.9: The transmit spectrum of an ideal polar TX with 4-bit amplitude resolution.

bits between the amplitude and phase path in this noise-limiting characteristic stems from the non-linear Cartesian-to-Polar conversion as specified by Eq. (2.36) and Eq. (2.37).

In this work, dual RF-DAC with 8-bit amplitude resolution each is used. Due to the highly compressive AM-AM characteristic of each single RF-DAC, the amplitude resolution

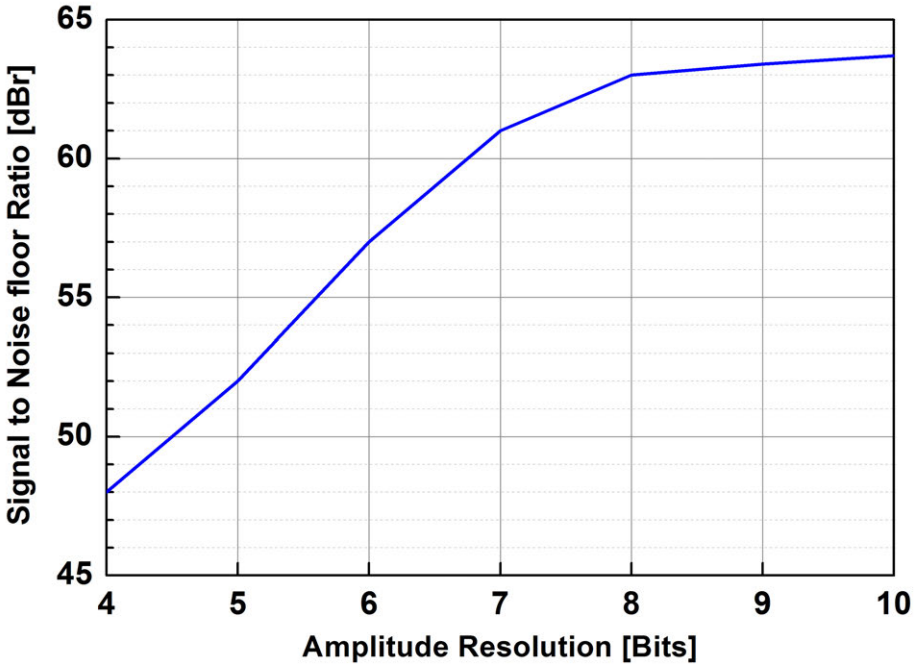


Figure 3.10: The out-of-band noise versus amplitude resolution of an ideal WLAN TX.

is lower than 8-bit, especially at low output power regions the resolution is much degraded due to an "excessive" signal gain. Benefiting from the impedance modulation scheme, which offers more output levels at low power regime, the dual RF-DAC, in combination with the impedance modulator, roughly provides 8-bit effective amplitude resolution. Therefore, the amplitude resolution is not the major limiting factor for the out-of-band noise floor.

3.6 Phase Resolution

Similar experiments are performed with varying the phase resolution for a fixed amplitude resolution of 9-bit. It is seen from Fig. 3.11 that a phase resolution of at least 7-bit is good enough not to considerably degrade EVM or close-in ACPR. Compared to the minimum requirement of 5-bit on the amplitude path, the in-band performances are more more sensitive to the phase resolution.

Similar conclusions can be drawn for the out-of-band noise performance (Fig. 3.12). For a fixed amplitude resolution of 9-bit, increasing the phase resolution from 5 to 11-bit consistently improve the noise floor with an approximately 5dB/bit slope. Therefore, both the in-band signal integrity and out-of-band quantization noise floor are more sensitive to the phase resolution as opposed to the amplitude resolution, for a similar number of bits. Also, the phase resolution would have to be higher than the amplitude resolution by 2–3bit to contribute equally to the overall system performance. These observations are important

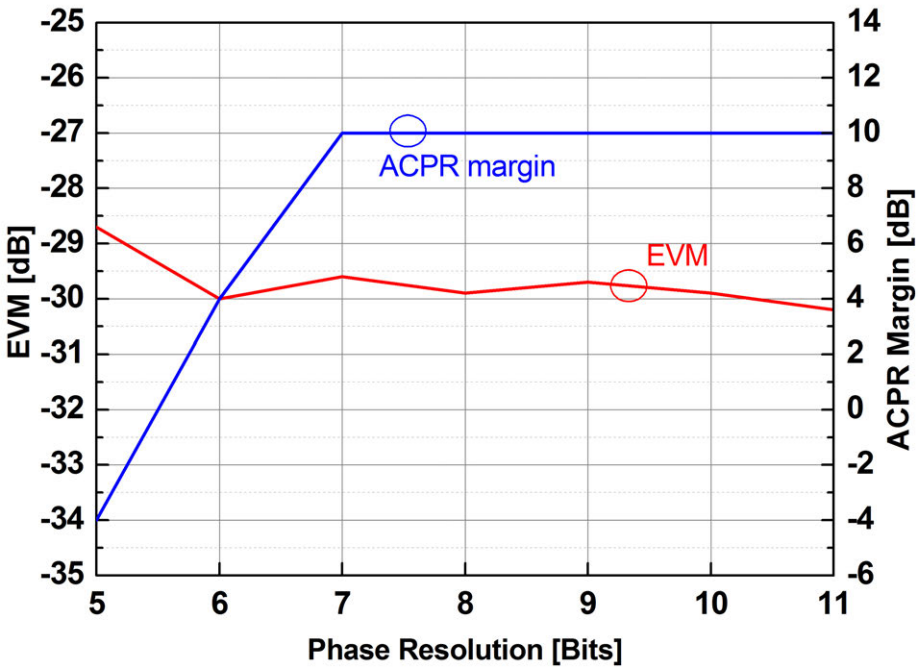


Figure 3.11: EVM and ACPR versus phase resolution of an ideal WLAN TX.

in the system-level budget for the phase path. At the same time, they tend to imply that the phase path design in a polar TX is challenging.

In this work, 9-bit phase resolution is chosen. Ideally, it provides an RMS phase error of approximately 0.2° (corresponding to about 0.25ps at 2.4GHz), according to the following equation for the quantization noise of a random signal with flat statistical distribution over the entire full-scale range.

$$\sigma_{qn,rms}^2 = \frac{\Delta^2}{12} \tag{3.10}$$

where Δ is the quantization step and $\sigma_{qn,rms}$ is the RMS quantization noise. The actual distribution of the phase signal for 802.11g may not be purely random so the equation just provides a ball-park estimate. The power penalty of increasing the phase resolution is discussed later in the dissertation.

3.7 Bandwidth Expansion due to Cartesian-to-Polar Conversion

As seen in Eq.(2.36) and Eq.(2.37), the conversion from the Cartesian to the polar baseband signals is a non-linear function. Therefore, the bandwidths of the polar signals are increased with respect to the original Cartesian signals (Fig. 3.13 and Fig. 3.14). Note that

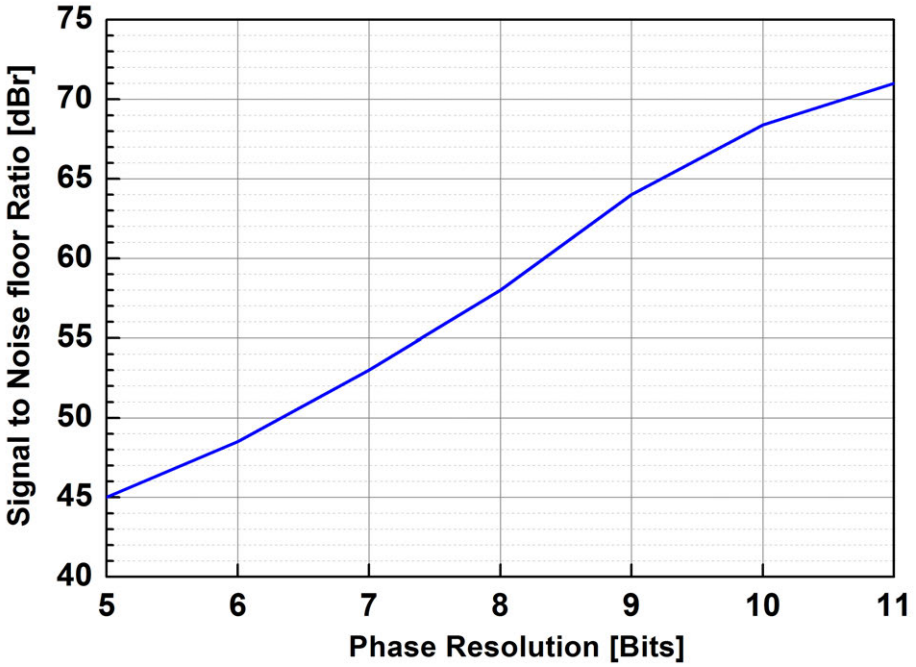


Figure 3.12: The out-of-band noise versus phase resolution of an ideal WLAN TX.

the Cartesian in-phase component is the $I_{BB}(t)$ in Eq.(2.36) and Eq.(2.37). As shown in Fig. 3.13, the amplitude component of the polar TX has a strong DC component, because its time-average is not zero. The spectrum comparison in Fig. 3.13 is carried out in such a way that the DC component of the polar amplitude signal has been removed and the in-band spectrum have a peak power of 0dBr, same as the Cartesian in-phase component. Unlike the Cartesian in-phase component which has a sharp roll-off beyond the occupied baseband bandwidth of 8.3MHz, the roll-off of the polar amplitude component is much smoother versus frequency, which is a clear indication of bandwidth expansion.

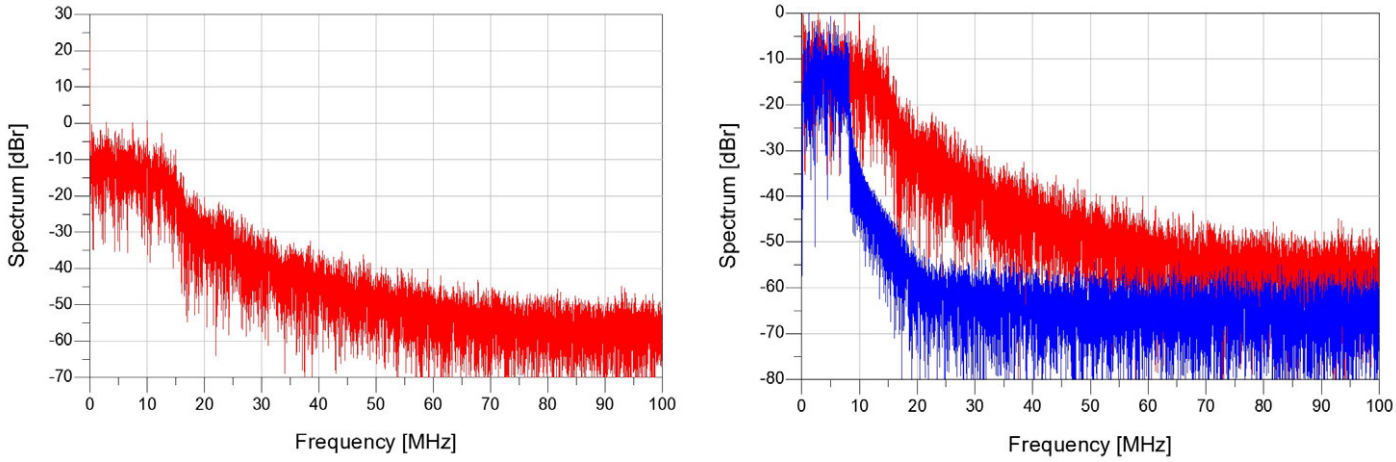
In Fig. 3.14, a similar comparison between the polar phase component and the Cartesian in-phase component is carried out. Note that a comparison on the polar phase value ($\phi(t)$ in Eq.(2.37)) is meaningless. The polar phase component are thus expressed as a combination of the in-phase component of

$$I_{\phi}(t) = \cos(\phi(t)) = \frac{I_{BB}(t)}{\sqrt{I_{BB}(t)^2 + Q_{BB}(t)^2}} \tag{3.11}$$

and the quadrature-phase component of

$$Q_{\phi}(t) = \sin(\phi(t)) = \frac{Q_{BB}(t)}{\sqrt{I_{BB}(t)^2 + Q_{BB}(t)^2}} \tag{3.12}$$

Note that in Fig. 3.14 the comparison is between the in-phase component ($I_{\phi}(t)$ in Eq. (3.11)) of the polar phase signal and the in-phase component of the Cartesian signal

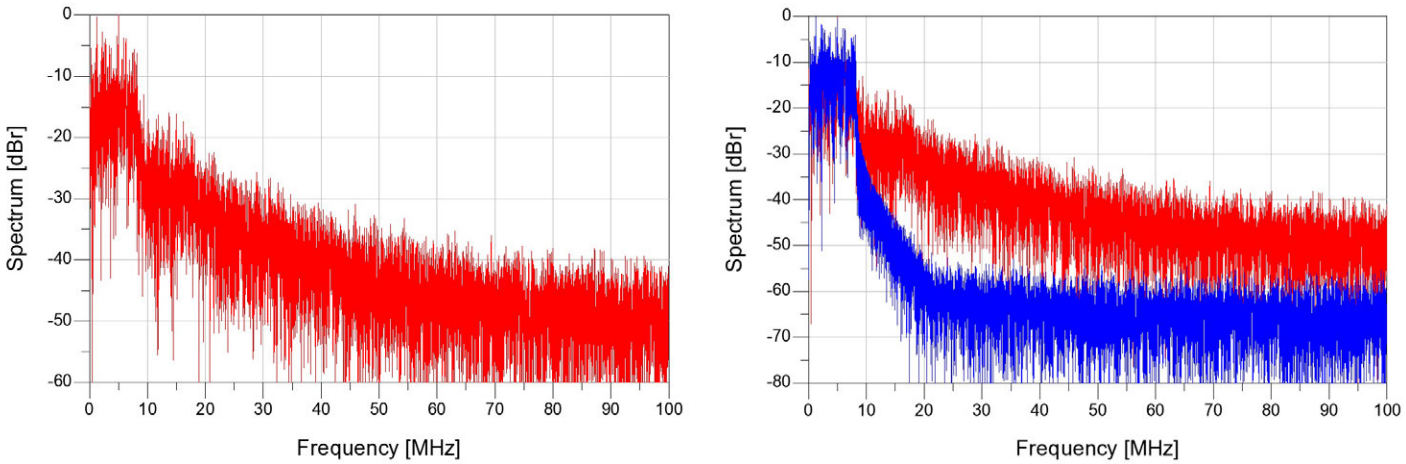


(a) The spectrum of polar amplitude component.

(b) The spectrum of polar amplitude and Cartesian in-phase component.

Figure 3.13: Bandwidth extension of the amplitude signal due to Cartesian-to-polar conversion.

($I_{BB}(t)$ in Eq. (3.11)). Similar to the amplitude signal, the phase signal has also experienced significant bandwidth expansion after the Cartesian-to-polar conversion.



(a) The spectrum of polar phase component.

(b) The spectrum of polar phase and Cartesian in-phase component.

Figure 3.14: Bandwidth extension of the phase signal due to Cartesian-to-polar conversion.

It is instructive to compare the bandwidth of polar amplitude and phase signal. As shown in Fig. 3.15, the amplitude signal expands much more significantly than the phase component

around the close-in spectrum. At the far-out spectrum, though, the phase component is slightly higher.

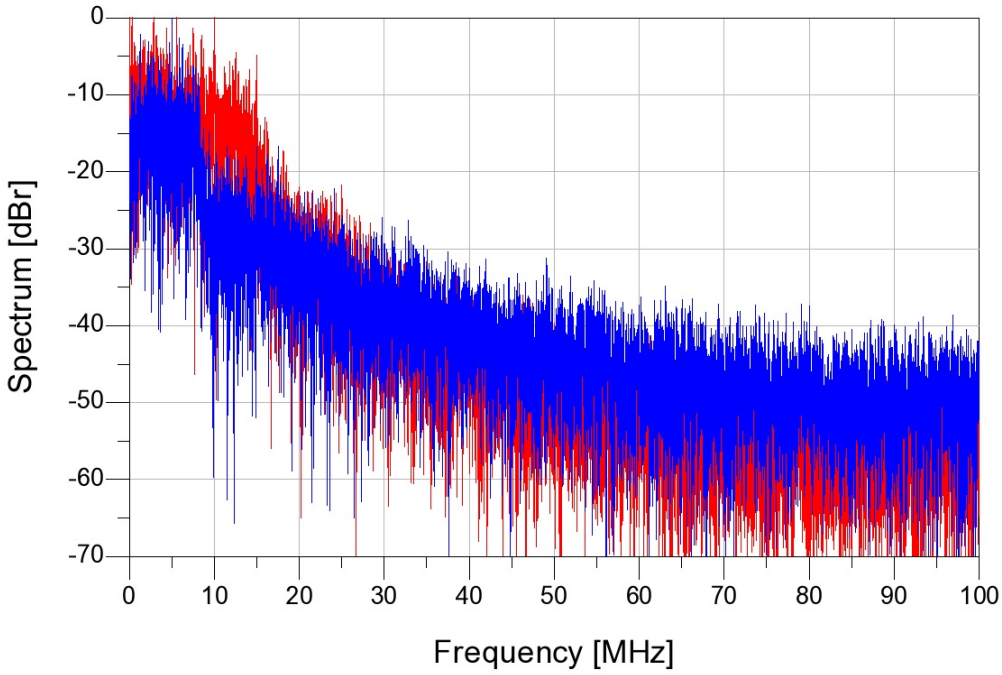


Figure 3.15: The spectrum of the amplitude (red) and phase (blue) component of an ideal polar WLAN TX.

3.8 Bandwidth Expansion due to Transmit Predistortion

Predistortion techniques are usually employed in a TX to improve linearity at power levels close to P_{sat}. It allows the satisfaction of a particular EVM target with a smaller back-off from P_{sat} for a WLAN TX, thereby improving efficiency and output power. The predistortion process essentially applies an inverse of the TX non-linearity to the signals to compensate the distortions in the following stages. Due to the inherent non-linearity associated with this process, the predistortion also tends to expand the actual bandwidth on the modulated signals. Note that this bandwidth expansion mechanism occurs in both a Cartesian and a polar TX; also, it is more pronounced with worse TX non-linearities because the predistortion, which is essentially creating the inverse of the non-linearities, will tend to be more non-linear in that case.

In Fig. 3.16 and Fig. 3.17, pre-distortions are applied to a polar modulated signals according to the AM-AM and AM-PM characteristics of a single RF-DAC in [36], and the

spectrum of the baseband signals before and after pre-distortion are compared by overlaying them on top of each other. Comparing these results with Fig. 3.13 and Fig. 3.14, we find that the bandwidth expansion due to transmit predistortion in this case is less pronounced than due to the Cartesian-to-polar conversion.

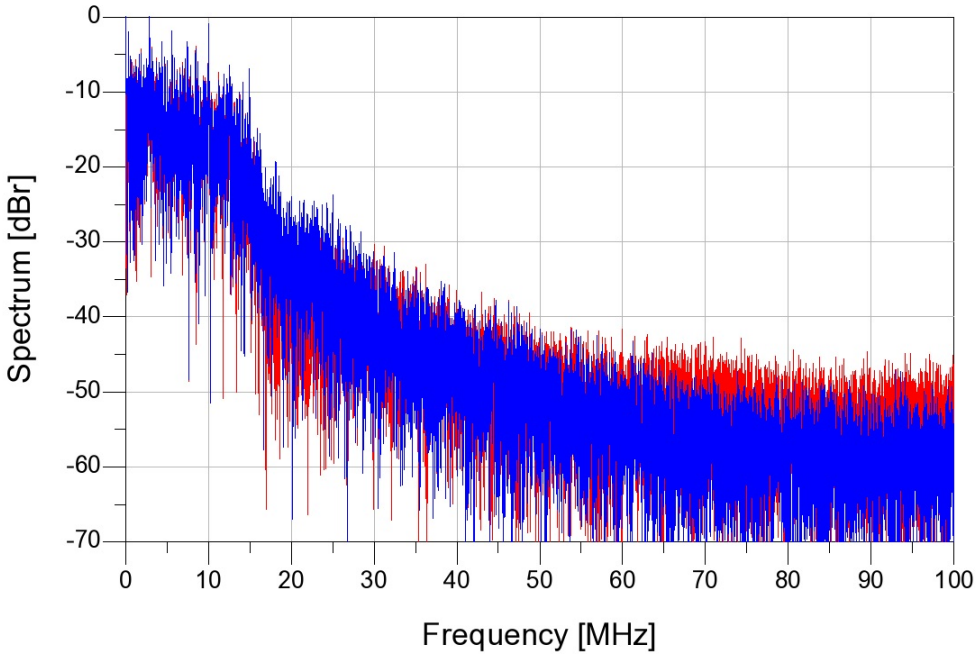


Figure 3.16: The spectrum of the amplitude component before (blue) and after (red) predistortion in a WLAN TX.

3.9 Baseband Output Sample Rate

As shown in Fig. 3.5, the digital baseband for the transmitter (including both the external FPGA and the on-chip circuitry) is clocked at different rates. The FPGA is running at 200MHz; in other words, the baseband input sample rate (as relative to the chip) is 200MHz. In contrast, the on-chip digital circuitry is clocked at 1GHz (i.e. the baseband output sample rate). The reason for such a multi-rate digital baseband is explained in this and the following sections.

Due to its sample-and-hold operation, the direct digital modulation creates spectral images at offsets equal to multiples of the baseband sample rate. As shown in Fig. 3.18 which was obtained from a system-level simulation of a digitally-modulated WLAN TX (without including any analog/RF filtering), the spectral images are usually 20–30dB higher than the noise floor and become increasingly problematic for coexistence considerations. To push the images far away from the desired signal and ease the subsequent RF filtering (as avail-

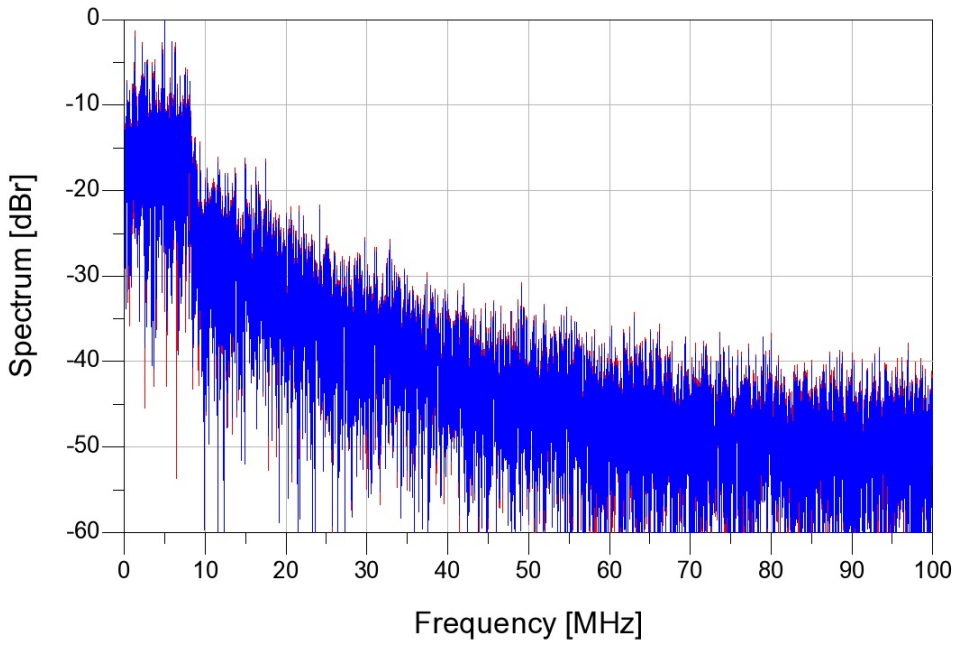


Figure 3.17: The spectrum of the phase component before (blue) and after (red) predistortion in a WLAN TX.

able from the antenna, the diplexer, or an explicit bandpass filter), the sample rate at the digital/RF-DAC interface should be relatively high.

The spectral image as a result of the sample-and-hold (zero-order hold, or, ZOH) operation is attenuated by a sinc characteristic with respect to the in-band ([53]) as defined below

$$|H(f_n)| = \frac{\sin(\pi f_n)}{\pi f_n} \tag{3.13}$$

where the normalized frequency, f_n, is defined as

$$f_n = \frac{f_{\text{offset}}}{f_s} \tag{3.14}$$

where f_{offset} and f_s are the offset frequency of interest and the sampling frequency, respectively. According the above equations, the ZOH characteristic places nulls right at offsets equal to an integer multiple of the sampling frequency. As the frequency deviates from the nulling frequencies, the attenuation reduces and the spectral images result. A higher f_s therefore reduces the offset between the nulling frequency and the frequency of interest on a relative basis as defined by Eq. (3.14) and hence the height of the spectral image. As shown in Fig. 3.19, the sinc shaping provides an attenuation of 43dB on the closest spectral image

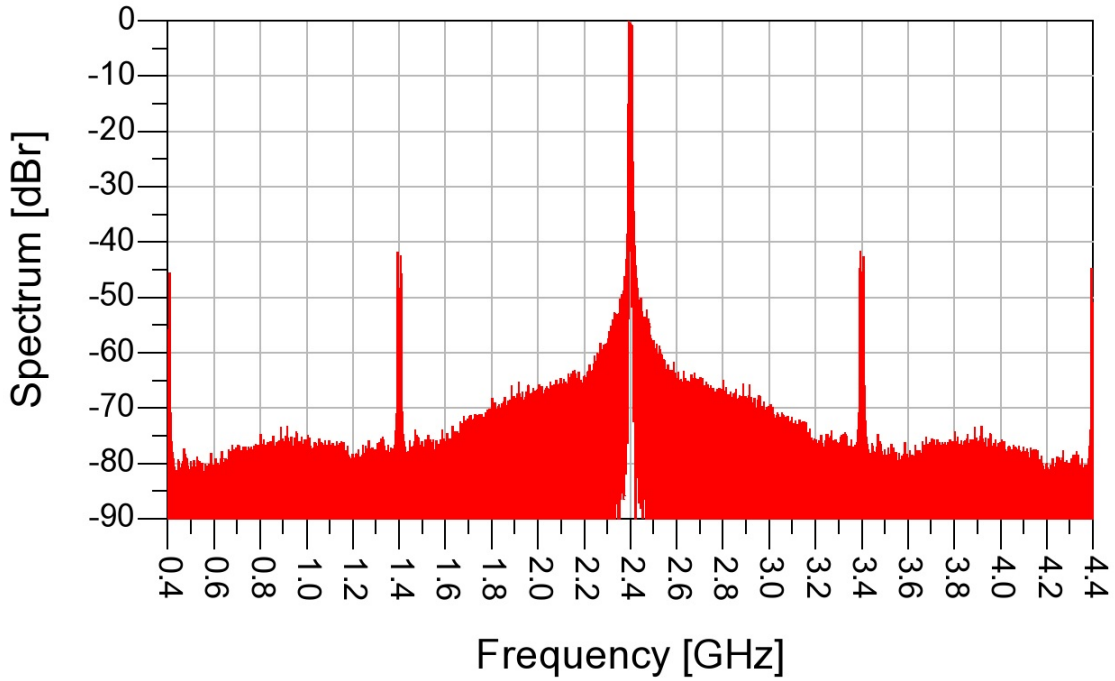


Figure 3.18: The sample-and-hold (S/H) spectral images of an ideal polar TX with a baseband output sample rate of 1GS/s.

for an ideal WLAN polar TX with a final baseband sample rate of 1GS/s, in good agreement with results directly calculated from Eq. (3.13).

Higher sampling rate also helps to increase oversample ratio and lower the quantization noise density, although it has an negligible effect on EVM (Fig. 3.20). Note that in Fig. 3.20, the close-in noise floor (at a fixed offset from 80 to 100MHz) quickly saturates without significant improvement as the BB output sample rate increases beyond 600MHz, while the far-out noise floor (as measured at a fixed proportional offset, i.e. larger offset with higher sample rate) is considerably lowered by increasing the sample rate; in this experiment, the far-out proportional offset is from 0.25 to 0.35 (as normalized to the baseband sample rate), and the baseband input sample rate is fixed at 200MS/s.

In this design, a 1GS/s sample rate was chosen at the digital/RF-DAC interface. According to the simulations of an ideal polar TX, the far-out noise floor is roughly 63dB down with 8-bit amplitude and 9-bit phase resolution, while the the closest spectral image is 20dB higher than the noise floor.

3.10 Filter-First and Filter-Last Architecture

Although the digital/RF-DAC interface should be clocked at a relatively high rate as explained in Section 3.9, most of the digital BB modules for a typical WLAN TX run

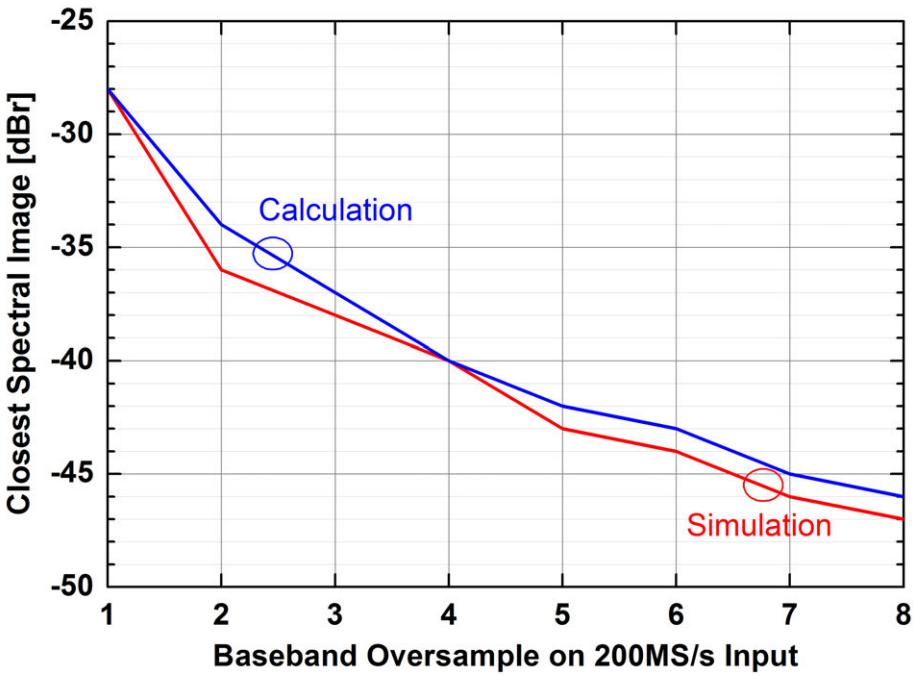


Figure 3.19: The level of the closest spectral image versus baseband output sample rate of an ideal polar TX.

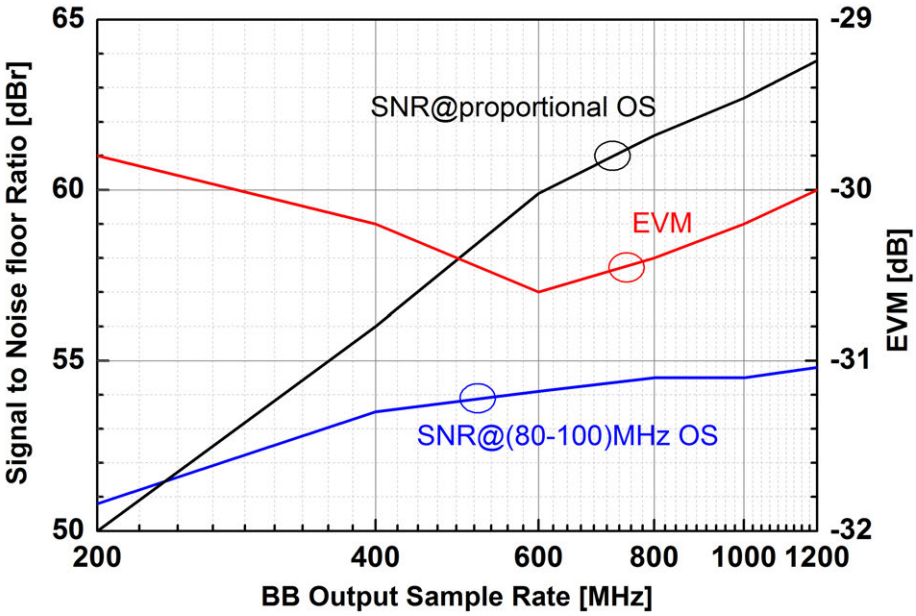


Figure 3.20: The out-of-band noise and EVM versus baseband output sample rate of an ideal WLAN TX.

much slower to save power. Digital Finite-Impulse-Response (FIR) interpolation filters were therefore employed in this work to attenuate the images present in the low-rate input data when they are up-sampled to 1GS/s.

Since Look-Up-Table (LUT) based digital predistortion is required to correct for the PAs non-linearities, the interaction between predistortion and filtering must be taken into account. On one hand, if predistortion is performed before filtering, the LUT can run at a much lower speed (Fig 3.21(a)). On the other hand, placing the LUT after the filter produces more accurate data since the filter first performs linear operations on a linear version of the signal to be filtered (Fig 3.21(b)). In this design, the LUT-first approach was chosen for power efficiency; however, several techniques were employed to make sure its output closely resemble that of the filter-first approach. These techniques include the choice of a high enough input sample rate (as explained in the next section), the choice of a Nyquist filter type (as explained in Section 7.1), and adding a waveform smoother to the amplitude filter (as explained in Section 7.8).

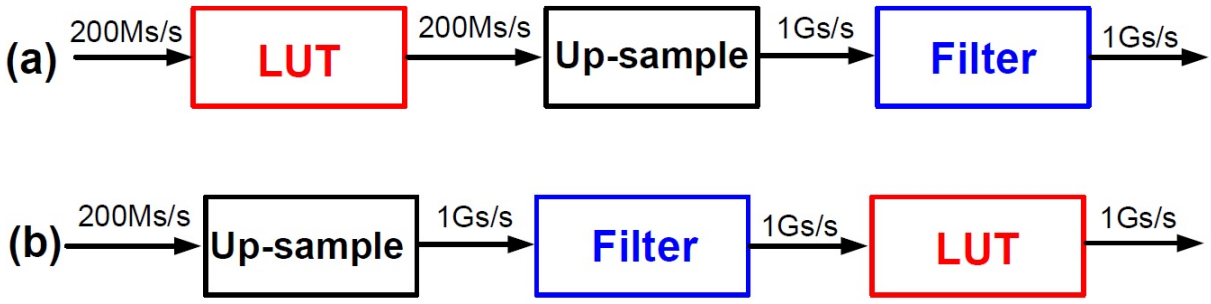


Figure 3.21: The filter-last (a) and filter-first (b) baseband architecture.

3.11 Baseband Input Sample Rate

Despite of an interpolation filter, the baseband input sample rate, however, cannot be arbitrarily low so as just to satisfy the Nyquist-Shannon sampling theorem (e.g. 20MS/s for a 10MHz baseband for 802.11g). Shown in Fig 3.22, the baseband input sample rate has to be higher than at least 160MS/s in order not to considerably affect close-in ACPR, even for an ideal WLAN polar TX. Compared to the Cartesian counterpart where the baseband is well contained within 10MHz bandwidth and therefore requires only a sample rate of 20MS/s, we find that the baseband signal in the polar TX, with its expanded bandwidth, requires at least an 8-times higher sample rate to capture the wideband energy.

Therefore the expanded BB bandwidth (due to the Cartesian-to-polar conversion and the non-linear LUT operation) has to stay well within the filter input sample rate, in order

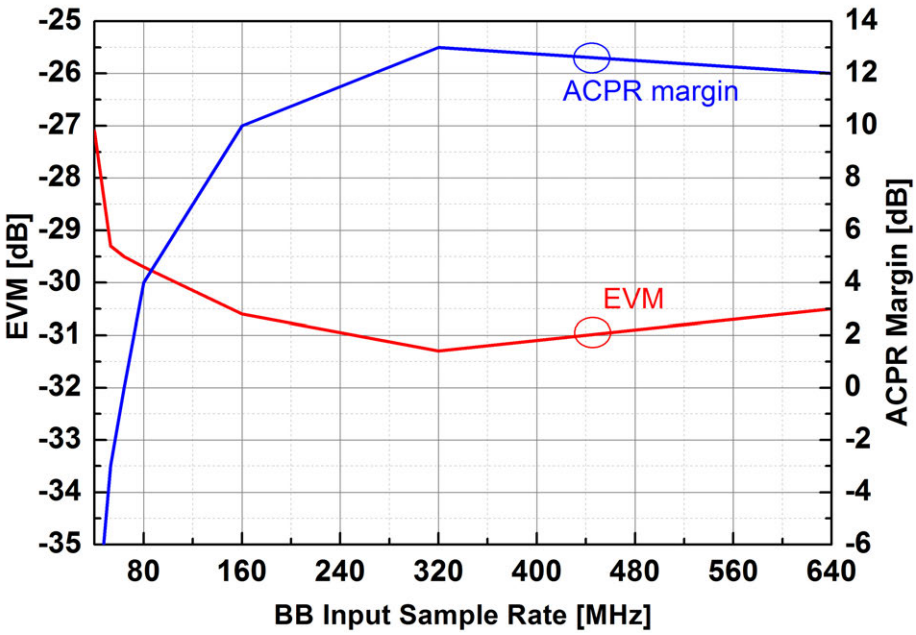


Figure 3.22: EVM and ACPR versus baseband input sample rate of an ideal WLAN polar TX.

for the the filter output to remain reasonably accurate. In other words, the LUT-first architecture ((Fig 3.21(a))) can closely approximate the filter-first approach ((Fig 3.21(b))) if the filter input has been sufficiently oversampled to smooth out any sharp transitions. This is satisfied by choosing the filter input rate of 200MHz, which is much higher than the LUT output bandwidth (at most 30 40MHz). There is however one exception to this that is described in Section 7.8.

3.12 AM/PM Delay Alignment

The AM/PM path in a polar system always suffer from a finite delay mismatch because each consists of heterogeneous circuitry before being combined ([54]). This issue is discussed in more detail as follows.

It was shown in [55] and [22] that the intermodulation distortion product (IMD) due to AM/PM delay mismatch in a polar system with two equal input tones can be approximated by

$$\text{IM3D} \simeq 2\pi \times (B_{RF} \times \Delta\tau)^2 \tag{3.15}$$

where B_{RF} is the 2-tone frequency spacing, $\Delta\tau$ is the delay mismatch, and IM3D is the magnitude of the third-order intermodulation product normalized by the main tone. The accuracy of the approximation was verified in [22] against a behavior simulation for an IM3D

range of -60 to -20dBc. The intermodulation distortion calculated according to Eq.(3.15) is ploted in Fig. 3.23, assuming a tone spacing of 16.6MHz, which is the occupied bandwidth of the 802.11g modulated signal. The distortion is of course lower than the case where the polar system is amplifying a wideband signal with 16.6MHz bandwidth. It however gives insight into the sensitivity of the polar system to the AM/PM delay mismatch. As seen from the figure, the distortion is better than -50dBc for a delay mismatch of 1.5ns. Also, for every 1ns degradation in the timing alignment, the distortion is worse by 4–7dB.

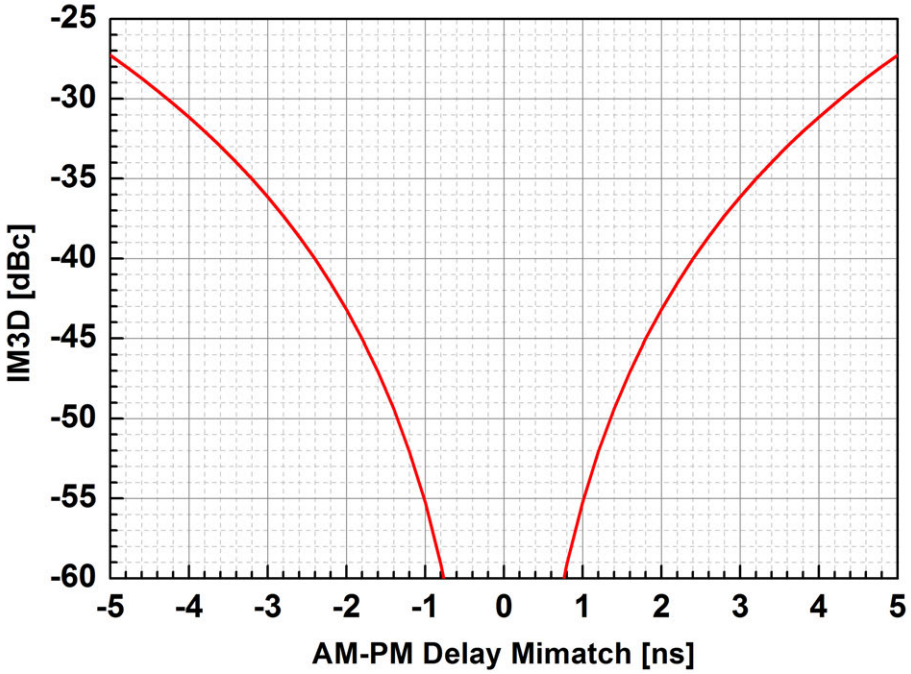


Figure 3.23: The calculated third-order intermodulation distortion due to AM/PM delay mismatch.

The impacts of AM/PM delay mismatch are also simulated for an otherwise ideal polar TX, with the 802.11g modulated signal. In the simulation, a resolution of 8 and 9 bit is used for the amplitude and the phase path, respectively; the PAPR is set to be 7.5dB, with a baseband sample rate of 1Gs/s. As shown in Fig. 3.24, the EVM degradation increases by approximately 5dB for every 1ns of delay mismatch increase, which matches reasonably well with the slope identified for IM3D calculation; the EVM remains below -35dB for a 1ns mismatch. The close-in ACPR is not significantly affected either so long as the delay mismatch stays within 1ns.

Compared to the in-band performances, the out-of-band noise performance is relatively insensitive to the delay mismatch (Fig. 3.25). Over a delay mismatch range of $\pm$ 4ns, the SNR changes by less than 2dB. Therefore, the impacts of AM/PM delay mismatch primarily manifest themselves in performances related to the signal integrity.

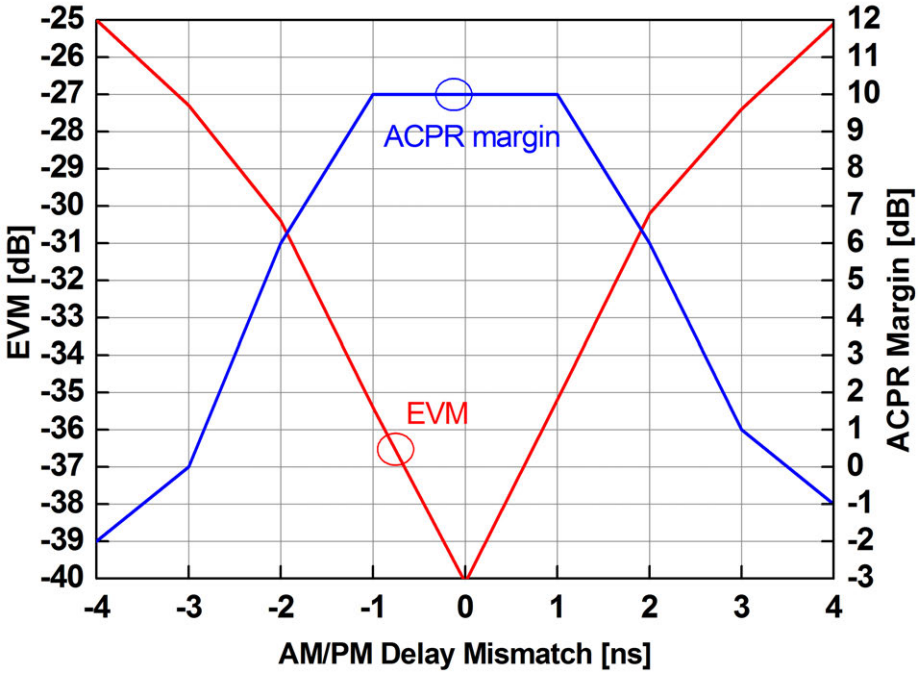


Figure 3.24: EVM and ACPR versus AM/PM delay mismatch of an ideal WLAN TX.

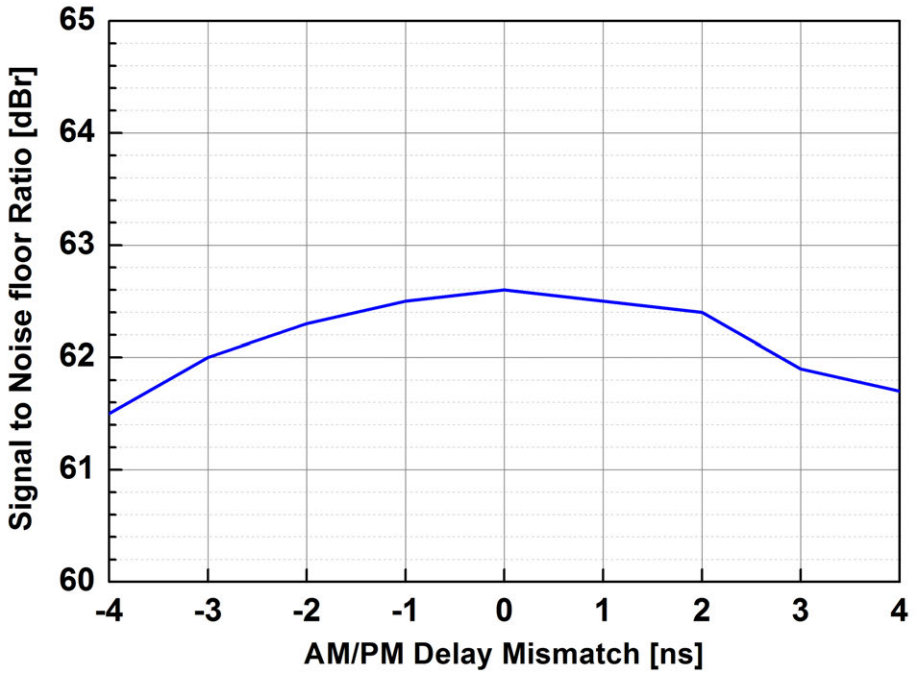


Figure 3.25: The out-of-band noise versus AM/PM delay mismatch of an ideal WLAN TX.

Overall the AM/PM delay mismatch has a significant impact on the in-band performances. However, Fig. 3.24 suggests that so long as the delay mismatch stays within 1ns, the EVM and ACPR are not considerably degraded. In fact, this result was previously verified in a digitally-modulated polar TX where the phase path was realized off-chip and its delay could be more easily adjusted ([13]). As shown in Fig. 3.26, the EVM stays within 1dB of its best value when the phase path delay is varied by more than 1ns with a fixed amplitude path delay.

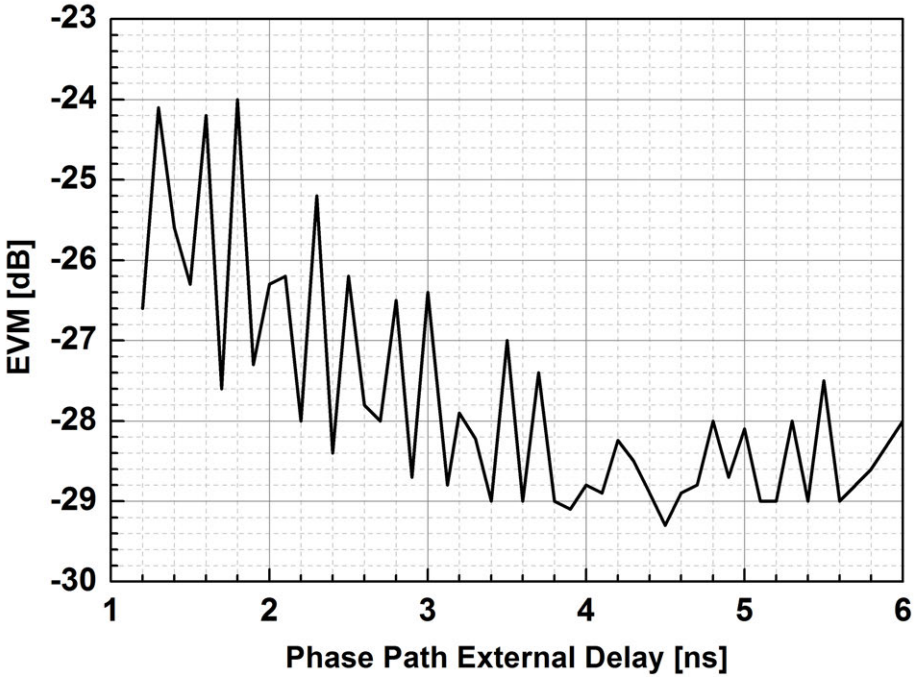


Figure 3.26: The measured EVM versus AM/PM delay mismatch for a WLAN polar TX [13].

In this work, coarse delay matching in excess of 1ns was accomplished by adjusting the number of clock cycle latencies inside the 1GHz baseband, while finer delay matching is achieved through proper design of the BB driver chains. Although the actual delay does deviate from its nominal value due to systematic Process, Voltage and Temperature (PVT) drift as well as random variations, the resultant delay variation is usually only a fraction (10–30%) of the total path delay [3]. Benefiting from a fine-line CMOS process, the nominal propagation delay through our AM/PM path (not accounting for the several of BB clock cycles) is small compared to the delay matching requirement ($1ns$), since the circuitry all consists of high-speed digital gates and open-loop high-bandwidth analog/RF stages. The AM/PM alignment can therefore easily be achieved even in the presence of PVT and random variations.

From the above perspective, the technology scaling, which often has an adverse effect on

high-power RF PA design, tends to benefit the digital polar TX. It should be pointed out that for other communication standards featuring higher bandwidths and data rates (e.g. 802.11ac), the alignment requirements of the AM/PM path would require re-examination.

3.13 Conclusion

Extensive system-level simulations have been carried out to investigate the various design trade-offs for the targeted 802.11g 54Mbps application. It has been established that even the close-in (10–20MHz offset) spectrum noise floor should be ideally low enough to allow the WLAN transmitter to coexist with cellular transceivers especially for LTE Band-40 which is only several MHz away from the edge of the lowest 2.4GHz WLAN channel. Crest factor (PAPR) reduction through hard-clipping the envelope signals is an effective way to improve the transmit power and average efficiency, although at a slight expense of the close-in spectrum skirt. The amplitude and phase resolution has been chosen to 8- and 9-bit respectively, primarily for low out-of-band noise density. The choice of baseband input sample frequency should factor in the power-efficient filter-last baseband architecture as well as the bandwidth expansion due to Cartesian-to-polar conversion and transmit predistortion. It is found in simulations that the bandwidth of the polar-modulated signal is 4–5 times expanded as compared to the original, unpredistorted Cartesian signals, and the expansion is more from the Cartesian-to-polar conversion as opposed to the predistortion. As a result of the bandwidth expansion, the baseband input signal should get enough oversampling, resulting in a choice of 200MS/s as the input sample rate. Meanwhile, a high output sample rate of 1GS/s has been chosen to lower the out-of-band noise floor as well as to provide enough sinc-shaping attenuation on the spectral images due to the sample-and-hold operation at the digital/RF-DAC interface. The impact of AM/PM delay mis-alignment on the 20MHz bandwidth of the modulated signals is also studied, both from the system-level simulations and from measurement results on a digitally-modulated polar TX. It has been found that the AM/PM delay misalignment has to be within 1ns in order not to significantly affect EVM and ACPR. With these system-level considerations in mind, we will proceed to circuit-level implementations of the WLAN TX in the following chapters.

Chapter 4

RF Switching PA Tuned to Limited Harmonics

The core RF-DAC employs a differential cascode switching PA topology loaded by a transformer matching network (Fig. 4.1). The cascoded design improves the power handling capability (i.e. the maximum tolerable drain voltage swing) under the fixed supply voltage, although at the expense of increased switch on-resistance due to the additional cascode device. This chapter will focus on a practical "low-frequency" (sub-10GHz as opposed to post-60GHz, e.g.) PA design methodology that attempts to address the design problem with very limited freedom on the passive network and also with as light math as possible.

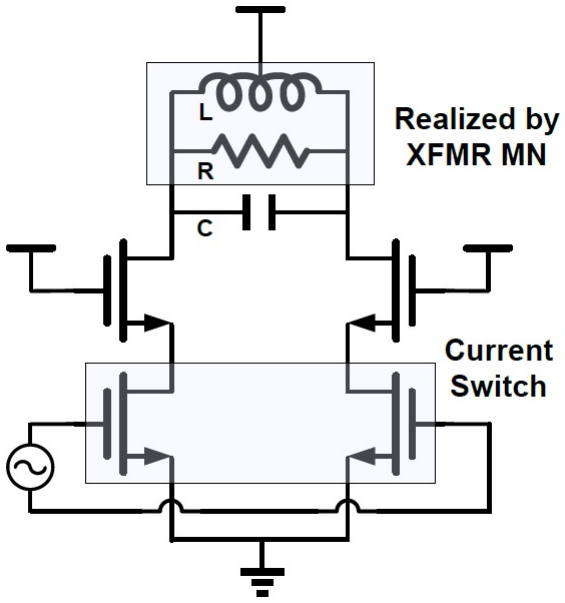


Figure 4.1: The differential cascode switching PA with XFMR matching network as the core RF-DAC.

4.1 Ideal Switching PA Operation

The transition frequency (f_T) of the core oxide transistor in a typical nanoscale CMOS technology tends to exceed 100GHz with a reasonable bias current density. As a result, it is not too difficult to drive the gate input of the g_m transistors in (Fig. 4.1) to a square-wave with finite rise/fall time (10–80ps) for sub-10GHz RF operation. For this reason, the cascode branch as a whole (at least for the transconductance portion excluding the finite shunt parasitics) conceptually acts like a switch, which toggles between the "ON" and "OFF" state fast enough. When the switch is turned "OFF", the transconductance portion has zero current flowing through it while it presents a small resistance when it is turned "ON".

4.1.1 Transistor as Voltage Switch or Current Switch?

It is claimed in [56] that the transistors act as current switches in the topology of (Fig. 4.1). It contradicts with the fact that when the transistor is turned "ON" it is driving the drain voltage to "zero" (or any well-defined level in other cases); the transistor alone does not have control over the current flowing through it. When the transistor is turned "OFF", however, it does fix the current flowing through the transconductance portion to zero while the passive network drives the drain voltage away from its initial conditions. From this standpoint, it is more accurate to state that the transistor acts as a voltage switch when it is on and as a current switch when it is off.

In reality, however, neither the voltage or the current waveform is a square-wave; instead, they are both distorted by the finite number of harmonics tuned by the passive network. Therefore, the distinction above is less important. It is often times when a pre-defined switching PA class is assigned to the topology that the statements on the transistor functionality are being made. For example, for a switching PA that ideally operates in class-D^{-1}, the transistors "naturally" act as a current switch, which is the dual of the voltage-switching transistors in a class-D PA.

4.1.2 Zero Voltage Switching

Despite of the confusing statements on the ideal functionality of the transistor, it is clear that the ideal waveforms of a switching PA should at least satisfy the Zero Voltage Switching (ZVS) condition ([57]). ZVS requires the drain voltage be driven to zero right before the switch is turned on. In this way, the drain parasitics does not contribute the CV^2f charge/discharge loss, improving the overall efficiency ([58]). With the assumption of ZVS, the transistor size can be increased freely to reduce switch on-resistance for higher efficiency; otherwise the design tradeoffs should involve balancing the loss between those from R_{ON} and from CV^2f, which is less straightforward to optimize and also typically yields a lower optimum efficiency as compared to the ZVS case. Since the capacitive charging/discharging loss increases in proportion to the operating frequency, satisfying ZVS is even more important for high-frequencies switching PA designs.

It is important to note that the ZVS condition is a time-domain requirement that is not simply equivalent to specifying termination impedances for a finite number of harmonics on the frequency-domain. Therefore, the simulation of a ZVS-PA should always include a broadband characteristic of the passive network (e.g., an ideal capacitor or inductor). In Fig. 4.1, the impedance of the transformer at the frequency range over which it is not large enough as compared to the shunt capacitor is also important to accurately simulate the time-domain waveforms of the PA.

Also, even though the the drain parasitics in Fig. 4.1 can be conveniently absorbed into the matching network at least for frequency tuning at the fundamental, they may still have dynamic power loss associated with them; in other words, "absorbing the drain capacitance into the matching network" does not automatically satisfy ZVS and hence does not necessarily eliminate the CV^2f loss.

4.1.3 Zero Voltage Slope Switching?

In [57], it was also suggested that the waveforms satisfy the zero voltage slope switching (dZVS) requirement. The voltage has to not only attain to zero but also with zero slope before the switch turn-on instant. That allows a time interval during which the switch turn-on can occur without severe loss of efficiency, which permits slight mistuning of the amplifier. Also, the dZVS, together with ZVS, guarantees the switch current at the start of the "ON" state would be zero, thereby providing a larger tolerance for the finite device turn-on time due to the finite transit speed of the channel/base charge.

However, the dZVS requirement reduces another degree of freedom in the design of the passive network. In the case of a fully integrated CMOS PA, the passive matching network is partially realized by the on-chip transformer structure, which presents minimum loss only within a finite range of inductance values for a fixed secondary termination ([18]). Since the sensitivity of the overall efficiency to the transformer loss is not obviously lower than to the dZVS performance, higher priority is usually given to the satisfaction of ZVS while dZVS is to be satisfied only when the transformer loss itself is not sacrificed.

4.1.4 Half-Wave Rectified Sinusoidal Drain Voltage

In Fig. 4.1, the differential drain voltage is converted to single-ended and applied across the actual 50Ω load with a transformer, which is inherently broadband. To reduce the harmonic radiation, the harmonic components within the differential drain voltage should be low enough. With a parallel RLC network at the drain, it is natural to assume the differential voltage there is ideally sinusoidal. This assumption, in combination with the differential symmetry, as well as the fact that the single-ended drain voltage is driven to zero by an ideal switch when it is turned on, leads to the fact that the desired single-ended drain voltage is a half-wave rectified sine.

A current-mode class-D (class-D^{-1}) switching PA, or equivalently, a class-F^{-1} PA, ideally puts out a half-wave rectified sinusoidal voltage across its switch. For this reason, we argue

that the "best" fit for our PA topology as depicted in Fig. 4.1 is a class-D^{-1} or a class-F^{-1} operation. The single-ended drain voltage normalized to the DC supply voltage, and the switch current (excluding the drain parasitics) normalized to the DC supply current, are shown in Fig. 4.2. Note that peak voltage is π times the supply while the peak switch current (measured single-endedly) is equal to the average supply current due to the balanced (differential) operation. Also note that in these two switching classes, ZVS is satisfied but dZVS is violated; actually the voltage slope prior to switch turn-on attains to its peak value over the entire RF period.

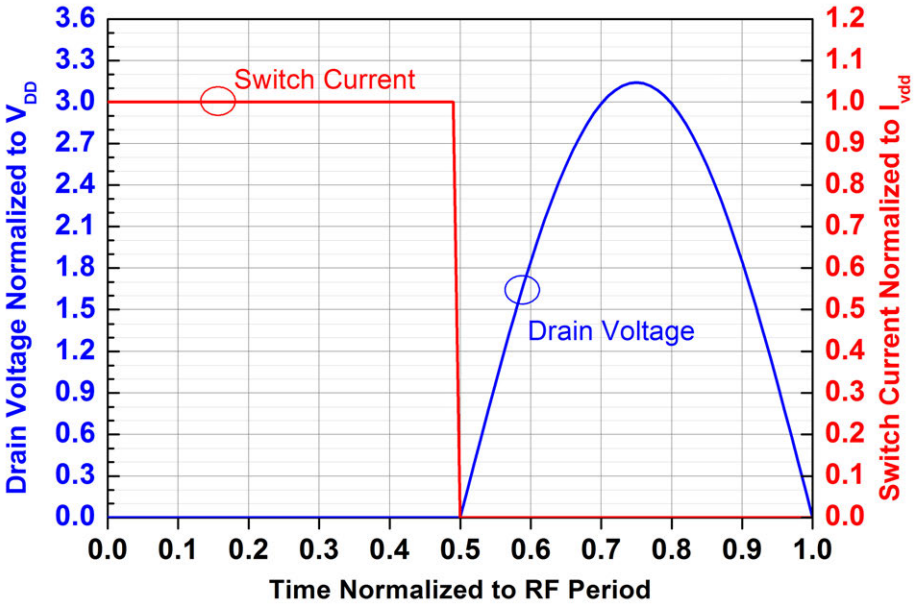


Figure 4.2: The ideal waveforms of the drain voltage and the switch current in a class-D^{-1} and class-F^{-1} PA.

In class-D^{-1} or class-F^{-1} operation, the equivalent single-ended termination should be short for odd harmonics and open for even harmonics, because the single-ended voltage (the half-wave rectified sine) does not contain odd harmonics while the switch current (the square wave) does not contain even harmonics. The fundamental termination consists only of a resistive part. Impedance termination requirements for a ideal class-D^{-1} and class-F^{-1} are summarized in Table. 4.1.

4.1.5 Ideal Inverse-Class-D/F with Finite Switch On-Resistance

With a real transistor as the switch, it presents a finite on-resistance when acting as the voltage switch (i.e. the V_{ds} is low enough)

$$R_{ON} = \frac{1}{\mu C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}})} \tag{4.1}$$

Table 4.1: Impedance termination requirements for a class-D^{-1} and class-F^{-1} PA.

Termination Impedance	**Frequency Component**
R_{diff}	Fundamental
Open	Even harmonics
Short	Odd harmonics

In this case, the closed switch can only drive the drain voltage to a finite knee voltage, V_k, as follows

$$V_k = I_{pk} R_{ON} \tag{4.2}$$

We will derive analytic expressions for the waveforms under this condition and express the drain efficiency as a function of switch on-resistance. Firstly, according to the Fourier series of an ideal square-wave with zero rise/fall time and 50% duty-cycle, the single-ended drain current is

$$i_D(t) = \frac{I_{pk}}{2} \times (1 + \frac{4}{\pi} \sum_{n=odd} \frac{\sin n\omega t}{n}) \tag{4.3}$$

where I_{pk} is the peak of the square-wave current and is equal to the average supply current. By a similar Fourier expansion, the single-ended drain voltage is

$$v_D(t) = V_k + (V_{pk} - V_k)(\frac{1}{\pi} - \frac{1}{2}\sin \omega t + \frac{2}{\pi} \sum_{n=even} \frac{\cos n\omega t}{n^2 - 1}) \tag{4.4}$$

whose DC component is equal to the supply voltage, V_{dd}, as below

$$V_{dd} = V_k + \frac{1}{\pi}(V_{pk} - V_k) \tag{4.5}$$

In the above, V_{pk} is the peak single-ended drain voltage. It is readily verified that the load impedance presented to the switch is a resistor at the fundamental frequency without any reactive component, as there is no phase shift between the fundamental component of $-i_D(t)$ and $v_D(t)$.
The fundamental component of the differential voltage across the load is

$$V_{L,\text{fund}} = V_{pk} - V_k \tag{4.6}$$

The fundamental component of the current flowing through the load is

$$I_{L,\text{fund}} = \frac{2}{\pi} I_{pk} \tag{4.7}$$

The load impedance, R_L, is

$$R_L = \frac{\pi}{2}\frac{V_{pk} - V_k}{I_{pk}} \tag{4.8}$$

The DC power drawn from the supply is

$$P_{dc} = I_{pk}V_{dd} = P_{L,\text{fund}} + P_{R_{ON}} \tag{4.9}$$

The fundamental power delivered to the load is

$$P_{L,\text{fund}} = \frac{1}{2}V_{L,\text{fund}}I_{L,\text{fund}} = I_{pk}(V_{dd} - R_{ON}I_{pk}) = \frac{2}{\pi^2}I_{pk}^2R_L \tag{4.10}$$

which attains to P_{dc} for a R_{ON} of zero.
The power dissipated across the R_{ON} of the transistor is

$$P_{R_{ON}} = I_{pk}^2R_{ON} \tag{4.11}$$

The efficiency only considering the finite R_{ON} of the transistor is

$$\eta = \frac{P_{L,\text{fund}}}{P_{dc}} = \frac{1}{1 + \frac{\pi^2 R_{ON}}{2R_L}} \approx \frac{1}{1 + 4.93\frac{R_{ON}}{R_L}} \tag{4.12}$$

Efficiency degradation due to the finite switch on-resistance is plotted in Fig. 4.3. The single-ended switch on-resistance should be smaller than 2% and 5% of the differential load resistance in order for the efficiency degradation to be within 10% and 20%, respectively.

4.2 Practical Considerations

A differential cascode PA with separate differential and common-mode tuning network is shown in Fig. 4.4. By the magnetic mutual coupling factor of -1, the effective differential inductance is equal to L_{diff} while the effective common-mode inductance is equal to L_{CM}; therefore, the tuning inductance can be independently changed for the differential or common-mode signal path without affecting one another. In the figure, the common-mode shunt capacitor, C_{CM}, represents the capacitance due to the metal routings in the layout; the total effective common-mode shunt capacitance is defined as $C_{CM,tot}$ which is the sum of C_{CM} and device parasitics. Several practical considerations will be outlined before we discuss the optimization methodology.

4.2.1 Number of Harmonics To Be Controlled

According to the frequency domain analysis, as the number of harmonic terminations under control increases, the waveforms of a switching PA more closely approach the idealized one, and hence efficiency tends to improve. In reality, however, the controlled harmonic termination is provided by the on-chip passives, which suffer from a finite loss especially in

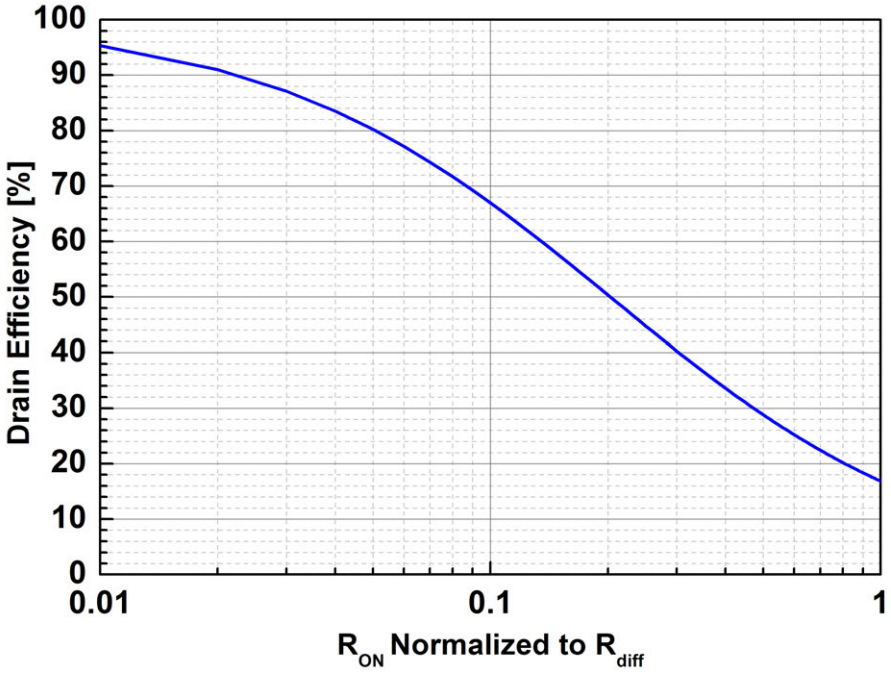


Figure 4.3: Efficiency degradation due to the switch finite on-resistance for a class-D^{-1} and class-F^{-1} PA.

the case of inductors and transformers ([18]). Practically speaking, the passive topology in Fig. 4.4 can only freely control the termination impedances for the fundamental and one of the even-order harmonics, through the differential and common-mode tuning, respectively. It is difficult to synthesize an on-chip transformer which simultaneously satisfies impedance requirements at multiple frequencies. Recent work in [16] has demonstrated that by exploiting mutual magnetic coupling, the impedances of the transformer at the fundamental and second-order harmonic can be adjusted relatively independent of each other while achieving low loss at the same time. Controlling harmonic terminations beyond the second-order would generally require more inductive elements, which might actually degrade the overall efficiency due to their high losses themselves.

On the other hand, [59] mathematically proves that with a half-wave rectified sinusoidal voltage, the best achievable efficiency from controlling the first $(2m-1)$ harmonics (including the fundamental) is

$$\eta = \frac{\pi}{2(m+1)} \cot[\frac{\pi}{2(m+1)}] \tag{4.13}$$

which is also tabulated in Table. 4.2. Since the efficiency improvement from controlling one more harmonic beyond the third-order is much less than 10% while adding one more on-chip inductive passive usually introduces loss in excess of 0.5dB, harmonic tuning up to the third-order is often times good enough to achieve the best efficiency number.

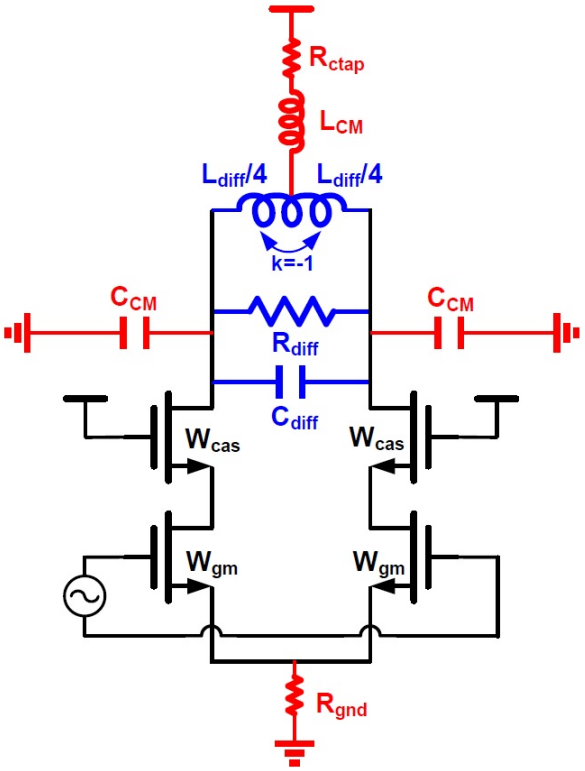


Figure 4.4: A differential cascode PA with separate differential (blue) and common-mode (red) tuning network.

Table 4.2: Maximum achievable efficiency with half-wave rectified sinusoidal voltage.

Number of Harmonics Tuned	**Maximum Achievable Efficiency** [%]
1	78.5
3	90.7
5	94.8
7	96.7
9	97.7
11	98.3

In Fig. 4.4, though, harmonic terminations can only be well controlled up to the second order, while higher-order harmonics (within the drain voltage) tend to be shorted by the differential and common-mode capacitances.

4.2.2 Choice of Device Width for Efficiency

It is shown in Section 4.1.5 that the switch on-resistance has to be low enough to introduce minimal degradation in efficiency. It naturally follows from that result that the device size has to be as large as possible, at least at RF frequencies where the capacitance tolerance is not exhausted. In reality, however, the following considerations prevent excessive increase of the device size.

First, as shown in Fig. 4.3, the device size has to increase to approximately twice to improve the drain efficiency from 80% to 90%. The resultant driver power requirement, however, also increases to twice. Therefore, the device sizing should at the same time take into account the effect of driver power on Power Added Efficiency (PAE).

Second, as shown in Fig. 4.4, the parasitic routing resistances in series with the drain, the ground (R_{gnd} in Fig. 4.1) and the balun center tap (R_{ctap} in Fig. 4.1) also introduce considerable efficiency loss. In this work, the metal routings, without Ultra Thick Metal (UTM), are estimated to degrade the efficiency by about 13%. Therefore, any attempt to enlarge the switch device to bring the efficiency up to 90% or more only yields very diminishing returns due to the limitation from metal routing resistance.

Third, as shown in Table 4.2, harmonic tuning up to the third-order only provides a maximum efficiency of 91% for a half-wave rectified sinusoidal drain voltage. Again, the device enlarging should also take into account the limitation from the finite harmonic controllability on the impedance termination.

Last, but not the least, a larger switch device gives a more compressive AM-AM characteristic in that the gain at the low output power region is excessive. As a result, the required amplitude codeword to deliver a mid-range power level (e.g. 6-dB backoff) may be small, leading to a very coarse amplitude quantization at lower power regions for the RF-DAC which is uniformly sliced. That will degrade the transmit linearity and out-of-band noise floor and should be avoided even with slight efficiency degradation.

In this work, the device size is chosen such that the switch on-resistance is about 4% of the differential load impedance, giving a relatively 17% hit on the efficiency due to the switch R_{ON}.

4.2.3 Choice of Another Switching PA Class

Since the controllable harmonics are only the fundamental and the second-order, the actual voltage and current waveforms will significantly deviate from the ones of class-D^{-1} or class-F^{-1}. In this case, it is not clear whether a tuning methodology exactly the same as in Table.4.1 (i.e. the differential path is tuned to fundamental while the common-mode path is tuned to the second-order harmonic) results the best efficiency performance. It is therefore worthwhile to briefly survey the literature for optimal designs with a finite number of harmonics possibly from another switching PA class.

Historically, class-E power amplifier was proposed to satisfy both the time-domain ZVS and the dZVS requirements with two passive components ([57]). Several variants of class-E

topologies exist, such as one that employs an ideal RF choke ([60]), or that consists of finite L and C component ([61][62][63]), or that both employs an RF choke and second-harmonic tuning ([64]). However, most class-E designs employ an "ideal" bandpass filter and possibly an inductor in series with the load which is difficult to be adapted to the topology of Fig. 4.1. A recent work in [65] uses a single pair of LC resonant network to achieve ZVS and dZVS waveforms with over 95% efficiency; the only difference between the class-E topology in [65] and that of Fig. 4.1 is the absence of an explicit differential tuning capacitor (C_{diff} in Fig. 4.1) in the former.

A hybrid topology between class-E and class-F^{-1} has also been proposed ([58]) to achieve ZVS and possibly dZVS with larger switch capacitance tolerance than the pure class-E operation. The only applicable hybrid for Fig. 4.1) is class E/F_2, where the second harmonic is open-circuited while the fundamental is tuned according to the ZVS and dZVS requirement. A different suggestion, however, arises from [56] that instead of tuned exactly to the second harmonic, the common-mode path should be tuned to 2.3 times the fundamental frequency for optimum efficiency.

In summary, a variety of harmonic tuning strategies as well as time-domain analytical techniques exist in literature for a switching PA with limited controllability on harmonic terminations. However, no single technique guarantees to offer the optimum efficiency; an iterative procedure of trial-and-error is required in simulations.

4.3 A Simplified Design Methodology for An RF Switching PA with Limited Controllability Over Harmonic Terminations

To simplify the design of the PA as shown in Fig. 4.4, we propose the following procedure. The end result is to provide some guidelines with design freedom on L_{CM} and L_{diff} which can be exploited later in the design of transformer matching network.

4.3.1 Impedance level and Device Size

First, the peak voltage (after the various parasitic series resistances) allowable across the drain-gate of the cascode transistor is determined to be 1.8V, 1.5 times the supply voltage. The choice is mainly limited by reliability concerns. However, the peak voltage only occurs transiently at the peak power, while the WLAN OFDM power is generally lower than 6dB backoff. Also, the TX duty-cycling ($\ll 50\%$) as a result of the Time Division Duplexing scheme of the WLAN standard helps to mitigate the excessive voltage stress. Furthermore, the high voltage stress only occurs when the transistor is off in a reasonably good ZVS design, thereby posing less reliability concerns in terms Hot Carrier Injection (HCI) effect due to the absence of device conduction current ([66][67]). Since the cascode gate is biased at 1.2V, the peak voltage of the half-sine (V_{pk} in Section 4.1.5) is assumed to be 3.0V. According

to Eq (4.10), a power target of 23.0dBm (twice of which is transformer-combined to a final P_{out} of 24.0dBm with 1.5dB of transformer loss and 0.5dB of other losses), and a zero knee voltage, the differential load resistance, R_{diff}, is calculated to be 22Ω.

Next, with the considerations outlined in Section 4.2.2, the device size is chosen such that the switch on-resistance is about 4% of R_{diff}, giving a 17% efficiency degradation due to switch R_{ON}. Accordingly, the device parasitics can be back-annotated to Fig. 4.4 as part of the $C_{CM,tot}$.

4.3.2 Insensitivity of Efficiency and Output Power with Fixed Harmonic Tuning Frequencies

Then, it is summarized that in our case where only the fundamental and second harmonic termination can be well controlled, the efficiency and output power are relatively sensitive to the following two parameters, A_1, and A_2, as defined by

$$A_1 \equiv L_{\text{diff}}(C_{\text{diff}} + \frac{1}{2}C_{CM,tot}) \tag{4.14}$$

$$A_2 \equiv L_{CM}(2C_{CM,tot}) \tag{4.15}$$

In other words, so long as the differential path and the common-mode path are tuned to fixed frequencies (which are not necessarily the fundamental and second harmonic), the baseline performances can be guaranteed regardless of changes in the various component values.

Simulations including post-layout parasitics (but excluding the R_{gnd} and R_{ctap} for the global metal routings) are performed to verify the above assumptions. First, the differential inductance, L_{diff}, is swept with a fixed A_1 by adjusting the differential capacitance, C_{diff} (Fig. 4.5). In this experiment, the second-harmonic tuning as realized by the common-mode path is unaffected. It is seen from Fig. 4.5 that the efficiency stays within 3% while the output power varies by less than 0.2dB over the entire inductance range.

Next, the common-mode inductance, L_{CM}, is swept with a fixed A_2 by adjusting the common-mode capacitance, $C_{CM,tot}$ (Fig. 4.6). In this experiment, the fundamental tuning as realized by the differential path is also altered since C_{diff} has to change in response to a changing $C_{CM,tot}$ to keep a fixed A_1. It is seen from Fig. 4.6 that the efficiency stays within 3% while the output power varies by less than 0.1dB over the entire inductance range.

Last, the common-mode capacitance, $C_{CM,tot}$, is swept with a fixed A_2 by adjusting the common-mode inductance, L_{CM} (Fig. 4.7). In this experiment, the fundamental tuning as realized by the differential path is also altered since C_{diff} has to change in response to a changing $C_{CM,tot}$ to keep a fixed A_1. It is seen from Fig. 4.7 that the efficiency stays within 1% while the output power varies by less than 0.1dB over the entire capacitance range.

In sum, with fixed harmonic tuning frequencies for the differential and the common-mode paths, changing the various component values in Fig. 4.4 only introduces minimal changes on the efficiency and output power. Therefore, with a fixed A_1 and A_2 defined by Eq (4.14)

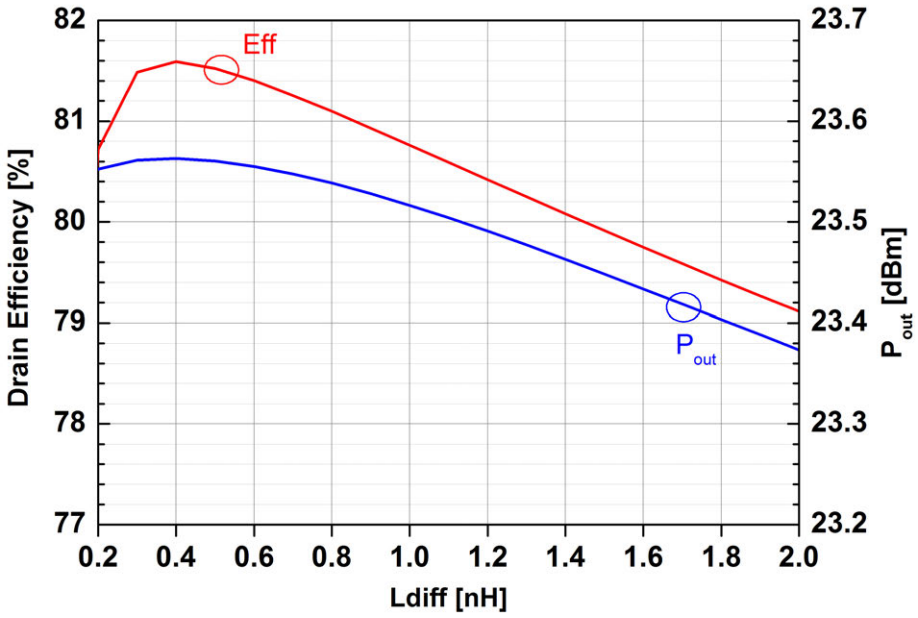


Figure 4.5: Drain efficiency and output power versus L_{diff} with a fixed A_1 and A_2 defined by Eq (4.14) and Eq (4.15).

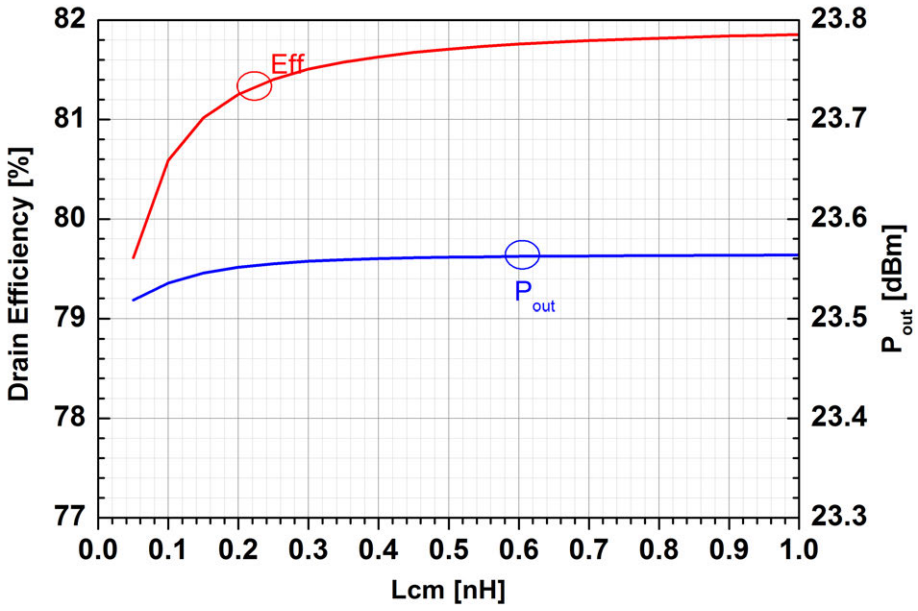


Figure 4.6: Drain efficiency and output power versus L_{CM} with a fixed A_1 and A_2 defined by Eq (4.14) and Eq (4.15).

and Eq (4.15), we can choose the component values of L_{diff}, L_{CM}, C_{diff} and $C_{CM,tot}$ with

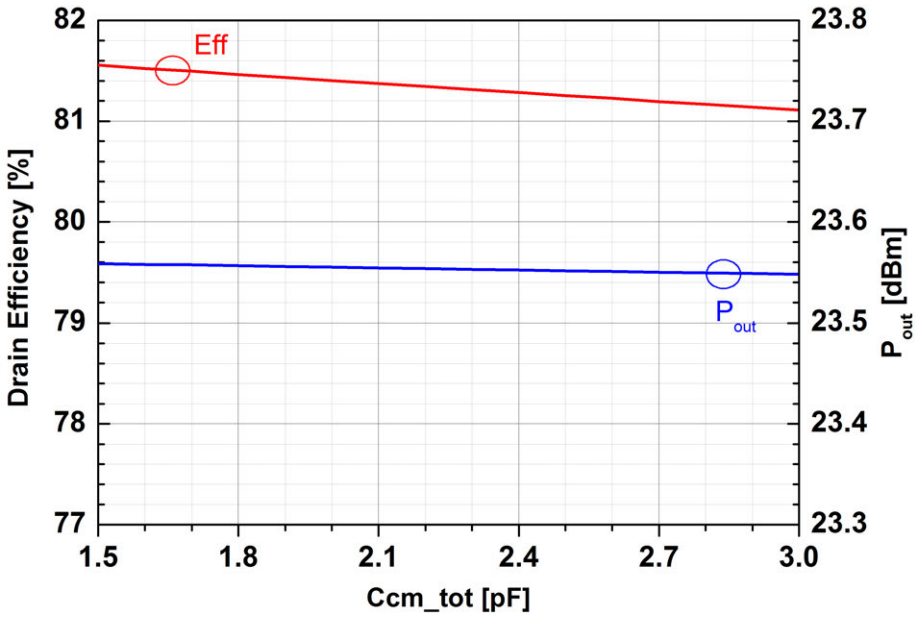


Figure 4.7: Drain efficiency and output power versus $C_{CM,tot}$ with a fixed A_1 and A_2 defined by Eq (4.14) and Eq (4.15).

relative design freedom for other considerations.

4.3.3 Sensitivity of Efficiency and Output Power to Harmonic Tuning Frequencies

In terms of optimum A_1 and A_2 (i.e. the frequencies to which the differential (purely resistive) and the common-mode (open) paths are tuned), we turn to SPICE simulations for the guidance. Compared to lengthy mathematical derivations, these parametrized sweeps are fast and convenient with today's CAD tools; they also provide useful design insights as discussed below.

First, the parameter A_1 is swept by changing only the differential capacitance, C_{diff} (Fig. 4.8). Optimum efficiency is obtained with a C_{diff} of 5.7pF, with a total differential tuning capacitance (including a $C_{CM,tot}$ of 2pF) of 6.7pF in this case. With an L_{diff} of 600pH, the differential path is tuned to 2.51GHz, which is 2.5% higher than the operating frequency of 2.45GHz. It is also seen from Fig. 4.8 that the efficiency is relatively more sensitive to the tuning than the output power is.

Next, the parameter A_2 is swept by changing only the common-mode inductance, L_{CM} (Fig. 4.9). Optimum efficiency is obtained with an L_{CM} of 250pH. With a $C_{CM,tot}$ of 2pF, the common-mode path is tuned to 5.03GHz, which is 2.7% higher than the second harmonic frequency of 4.9GHz. It is also seen from Fig. 4.9 that the efficiency does not change much once the common-mode inductance is increased beyond some low threshold.

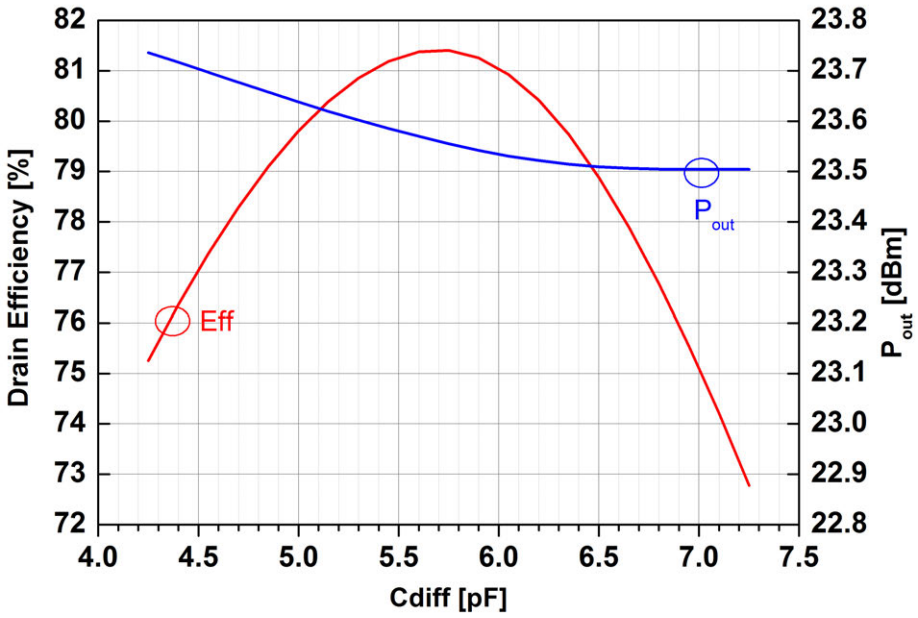


Figure 4.8: Drain efficiency and output power versus C_{diff} with a fixed A_2 defined by Eq (4.15).

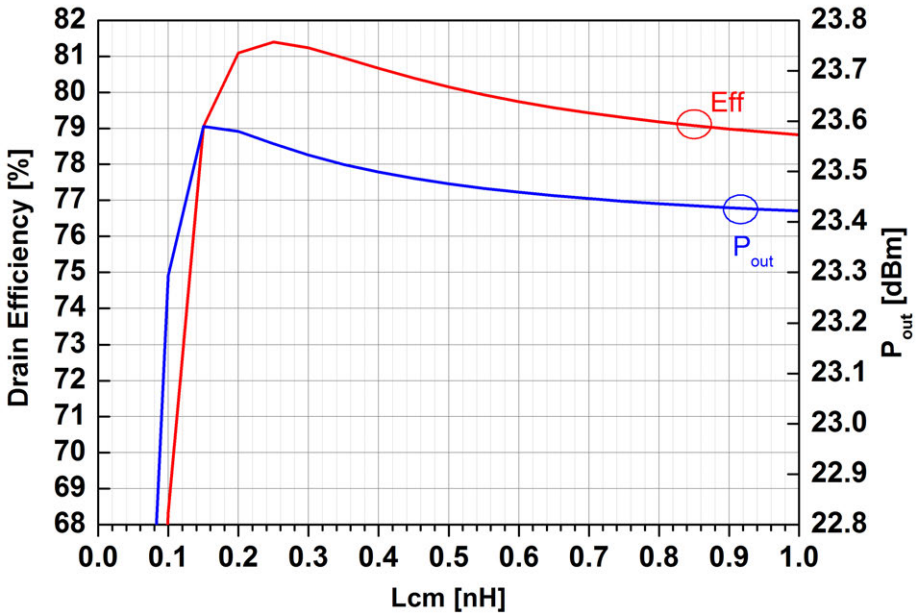


Figure 4.9: Drain efficiency and output power versus L_{CM} with a fixed A_1 defined by Eq (4.14).

It can also be seen from the above results that the harmonic tuning optimum for efficiency

is to present an open at roughly the second harmonic, and a purely resistive termination at approximately the fundamental, which is very similar to the harmonic tuning requirements of class-D^{-1} and class-F^{-1}.

Last, after correlating the simulation conditions for Fig. 4.8 and Fig. 4.9, we confirmed that A_1 is tuned to its optimum for efficiency with A_2 fixed at its optimum for efficiency and vice versa. Therefore, by fixing both A_1 and A_2, the component values of L_{diff}, L_{CM}, C_{diff} and $C_{CM,tot}$ can be changed with relative design freedom without considerably affecting the efficiency and output power.

In reality, L_{diff} and L_{CM} are chosen to maximize the transformer power efficiency when it is terminated by a pre-defined antenna impedance. The design procedures are outlined in Chapter 5. To avoid excessively small L_{CM}, the $C_{CM,tot}$ is usually realized by the parasitics of the device and the metal routings themselves which should be modeled accurately to yield the desired tuning performance; therefore $C_{CM,tot}$ is also relatively fixed by the device size and the layout. In contrast, C_{diff} can be varied easily without factoring in too many other design trade-offs.

4.4 Effect of PA Input Drive Characteristics

As discussed previously, at RF frequencies below 10GHz, it is not power intensive to drive the PA gate input to a square-wave even with simple digital inverters. In this condition, the PA devices act closely like a switch that toggles between "ON" and "OFF" state fast enough, facilitating efficient switching PA operations. Since the input drive directly affects how fast the transistor switches toggle, its effects on the switching PA performances are studied in this section.

In this experiment, the PA output stage is driven by an ideal voltage source with an edge type of half-sine. The half-sine edge type captures the fact that the transition between "HIGH" and "LOW" voltage levels of an inverter output is not linear versus time; instead, the voltage slope gets progressively less steep as it moves away from the trip point; in fact, a model incorporating linearized transistor I-V characteristic suggests the time-domain voltage is moving along an exponential trajectory when a CMOS inverter drives a linear capacitor ([68]). Nevertheless, the square-wave with half-sine edge serves as a good approximation to the actual driving signal to the PA.

First, the effect of the transition time on the drain efficiency and output power is shown in Fig. 4.10. It is seen from Fig. 4.10 that neither the efficiency nor the output power is very sensitive to the rise/fall time once the PA has been designed properly as shown in the previous section. In reality, however, we still want to maintain a sharp enough edge to reduce the conversion from the supply noise of the CMOS inverter buffer to the phase noise of the input drive during the signal transition. In this design, the fan-out of each stage of CMOS inverter buffers (including post-layout parasitic) is chosen to be roughly 3, which gives a 10% to 90% transition time of about 30ps (7.4% of the RF period) under typical conditions.

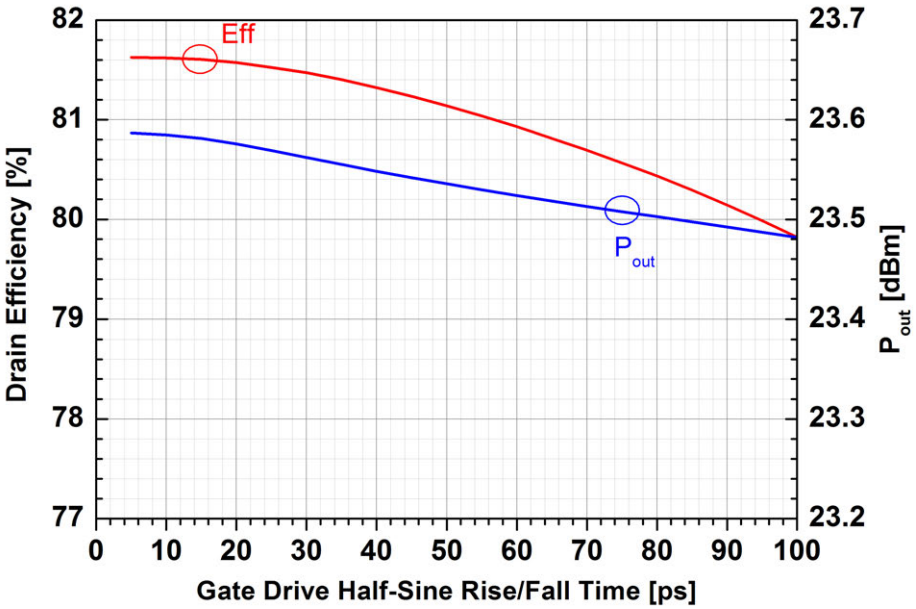


Figure 4.10: Drain efficiency and output power versus the rise/fall time of the PA input drive with a half-sine edge.

Since the PA employs a differential topology, the effect of the overlapping characteristic between the differential square-wave drives is also studied (Fig. 4.11). Note that in Fig. 4.11, a crossover at 0V means the differential square-waves are just non-overlapping while a crossover equal to the supply voltage (1V) indicates that the gate of at least one-side of the PA transistors is driven to the supply at any instant of time. It is seen from the figure that a crossover of 600mV (which is above the midway between the supply rails) gives the best efficiency; once the crossover is lower than about 300mV which is the threshold voltage of the transistors, the efficiency and output power degrades dramatically. The message is therefore to properly size the CMOS inverter drivers such that the PMOS which is responsible for the pull-up action is strong enough relative to the NMOS across Process Voltage and Temperature (PVT) corners. In this design, the PMOS in the CMOS inverter is sized slightly larger than twice the size of NMOS.

4.5 Capacitive Feedforward for Cascode Parasitics

Due to finite cascode on-resistance, the parasitics associated with cascode node (C_{cas}) cannot be completely absorbed into the tank (Fig 4.12) even only at the fundamental, degrading efficiency. To alleviate this, the source and drain fingers of the cascode are locally viaed and connected to as many metal layers as possible in the layout. This increases the coupling capacitance between the cascode drain and source (C_{ds}), providing a high-frequency feed-forward path to charge and discharge C_{cas}.

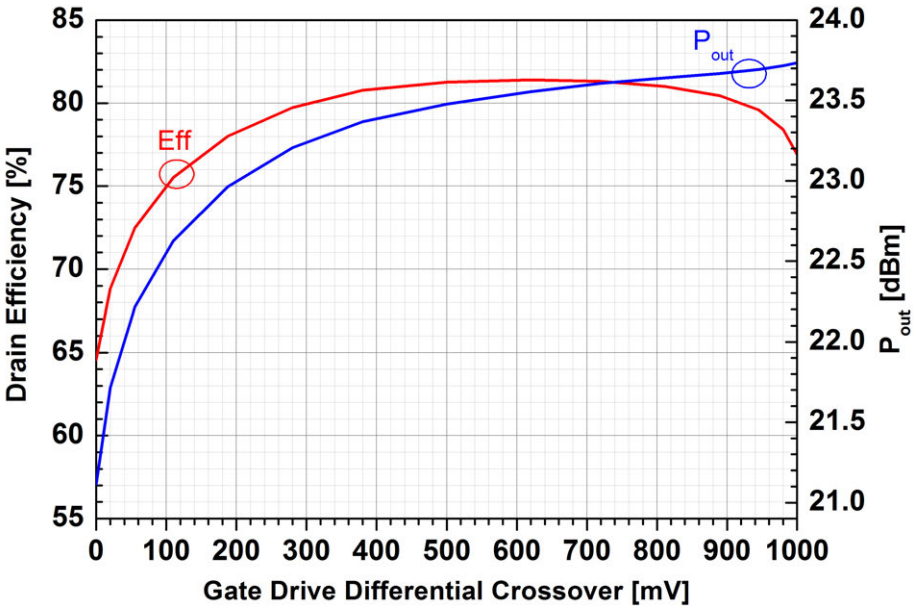


Figure 4.11: Drain efficiency and output power versus the differential crossover of the PA input drive.

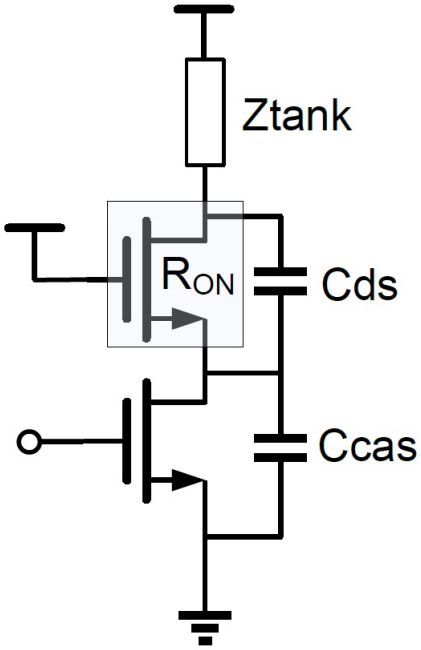


Figure 4.12: Capacitive feedforward through C_{ds} of the cascode device.

Often referred to as negative capacitance, this technique de-sensitizes the effect of excessive C_{cas} on efficiency ([69]). Dense connected metals on top of the power transistors also act as a heat sink. No explicit metal capacitance was added in this design to ensure robust stability.

4.6 Performance Summary of the Harmonic Tuned Switching PA

Simulated performances of the PA, excluding the transformer RF loss, are summarized in Table 4.3, for two cases with and without the global metal routings and DC resistances of the transformer. In the simulation, it was found the DC voltage drop across the transformer (R_{ctap}), the drain metal connections, and the ground metal connections are 50mV, 41mV and 20mV, respectively. The single-ended drain voltage and the current flowing into the device (including both the switch portion and the drain parasitics) are shown in Fig. 4.13.

Table 4.3: Simulated performances of the harmonic-tuned switching PA.

Scenario	**W/o global routing**	**W/t global routing**
Operating Frequency [GHz]	2.45	2.45
Differential Tuning [GHz]	2.51	2.51
Common-mode Tuning [GHz]	5.03	5.03
Pout [dBm]	23.6	22.4
Drain Efficiency [%]	81.4	70.4
Supply Current [mA]	232	205

4.7 Conclusion

A simplified design methodology has been proposed for a differential RF switching PA loaded by an on-chip transformer matching network. Due the relatively lossy on-chip inductors and transformers, we have chosen to exercise an accurate control only on the fundamental impedance (as realized by the differential signal path) and the second-harmonic impedance (as realized by the common-mode path). Instead of deriving lengthy mathematical expressions with a few simplifying assumptions which are sometimes not realistic, we directly turn to simulations for the best achievable efficiency and power. It has been found that with a highly limited controllability on the harmonic terminations, the strategy optimized for efficiency would be to provide a purely resistive termination at roughly the fundamental

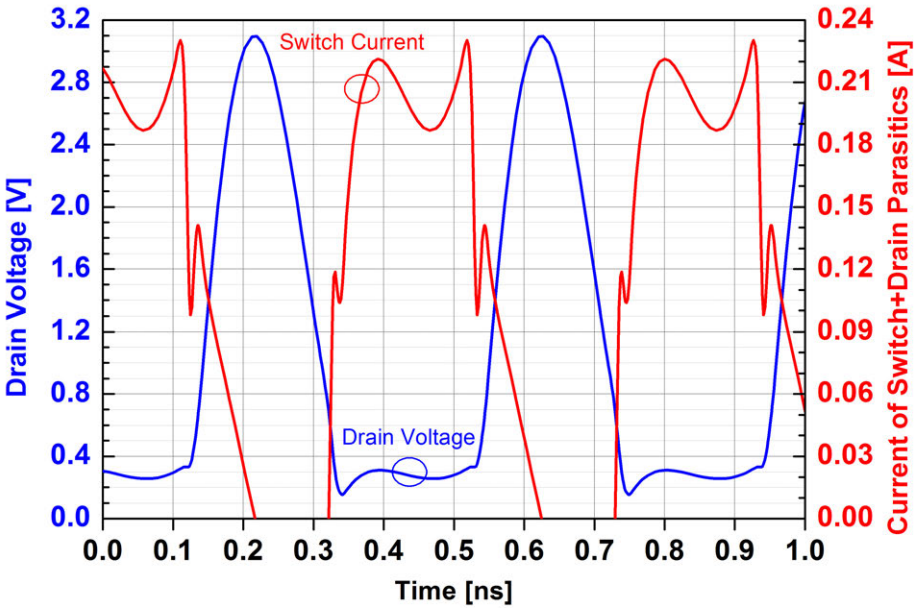


Figure 4.13: Simulated drain voltage and current with global metal routing resistances and the transformer DC IR drop taken into account.

frequency and an ideally open at roughly the second harmonic frequency. Once these requirements are met, fine tuning of the various passive component values only introduces small changes on the power and efficiency. The relative insensitivity of the performances to the changing component values with fixed harmonic tuning frequencies opens the door to the possibility of independent optimizations of inductors/transformers for minimum RF loss for a fixed antenna impedance. For our switching PA, the device should not be over-sized since the efficiencies are also affected by other mechanisms different from switch on-resistance; an excessive device size only yields diminishing returns while leading to a lower resolution for a uniformly-sized RF-DAC. The RF input waveforms to the switching PA have to be engineered to ensure a certain amount of overlapping and a sharp enough transition edge. Finally, the efficiency loss due to charging and discharging the parasitics associated with the internal cascode can be minimized by capacitive feedforward which naturally exists in the power device layout.

Chapter 5

Transformer-Based Impedance Modulator

5.1 Dual-Section Transformer Power Combiner

A dual-section power combiner is used as part of the impedance modulation scheme. Each of the two sections is a 1:1 XFMR with their secondaries connected in series for power combining (Fig 5.1). Secondary openings are placed at the upper half of each XFMR to minimize the vertical length of the connections to the external load and the associated loss.

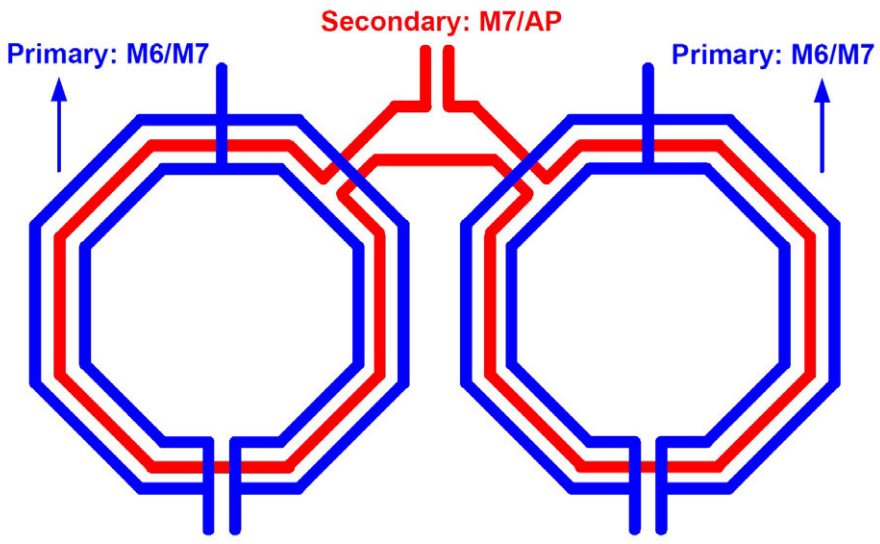


Figure 5.1: Dual-section transformer power combiner with parallel primary windings.

To satisfy DC electro-migration requirements, we split the one primary winding of each XFMR into two parallel ones, and hence avoid design-rule incompliant excessive ($> 20\mu m$) metal width. The secondary is then wound in between the two parallel primary turns; this

interleaved configuration helps to create a more uniform AC current distribution across the secondary trace width, reducing series RF losses ([70]).

To best exploit our specific process, the top two thicker (thickness$< 1\mu m$) copper layers (M6/M7) are strapped together to route the primary, while the secondary is routed in M7 and the Aluminum-capping layer. This vertical misalignment between the primary and secondary metal layers reduces the side-wall capacitance and electrical coupling, thus promoting magnetic coupling. When properly terminated, the XFMR presents 1.5dB loss at 2.4GHz, and has a DC IR drop of 40mV (out of a 1.2V PA supply) under peak power.

5.1.1 Performance Optimization

A large body of literature (e.g. [71][72][18]) has investigated the design on inductive passives in an IC process. Those works have revealed useful insights into the different loss mechanisms (i.e. substrate loss due to capacitive shunting and metal series loss due to skin effect and proximity effect) of the on-chip passives. In reality, however, parametrized simulations are often employed to fine-tune the layout geometries to squeeze out the last percent of power efficiency, as shown below.

First, the XFMR dimension is mainly fixed by the inductance requirement, for a fixed number of turns (1 in this case). As shown in Fig 5.2, the inductance increases roughly in proportion to the diameter of the winding (instead of the area), which makes sense for this single-winding design. Also, there is an optimum inductance value for minimized loss for a fixed secondary termination (50Ω in this case), which is also in good agreement with [18].

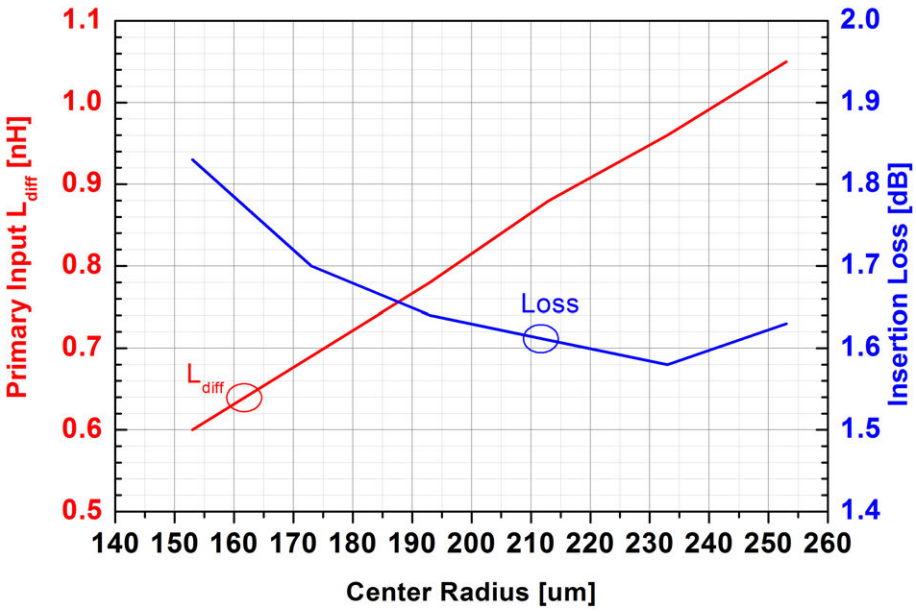


Figure 5.2: Differential input inductance and loss versus XFMR radius.

Next, the effect of the turn spacing is studied (Fig. 5.3). As shown in the figure, the loss slowly increases over a 5x increase (from 2um to 10um) in the turn spacing, due to reduced magnetic coupling between the primary and secondary windings. In this design, a turn spacing of $4\mu m$ is chosen to reduce the capacitive coupling between the primary and the secondary; this would help to reduce the odd harmonics in the supply/ground path due to the capacitive coupling between the balanced primary to the un-balanced (single-ended) secondary, and hence reduce the supply/ground bounce with a finite series inductance ([13]).

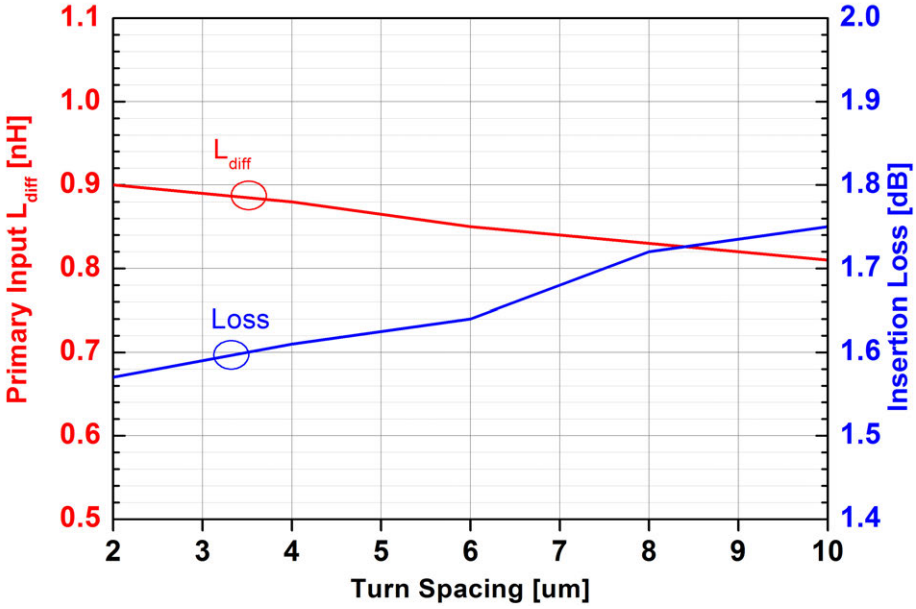


Figure 5.3: Differential input inductance and loss versus turn spacing.

Then, the width of secondary metal trace is swept (Fig. 5.4) to verify that it is not the limiting factor on the XFMR power efficiency. In this design, a secondary width of $12\mu m$ is chosen, as well as a primary width of $12\mu m$, both of which are the maximum allowable in the DRC rules. It should be noted that metal slotting can be used to have an effective total width exceeding the DRC limit; however, the slotting tends to introduce less improvement for AC-resistance as compared to DC-resistance since the RF current ideally would like to see a continuous and solid conducting path. Constrained by DC electromigration requirements, the primary width cannot be reduced anyways; therefore a sweep of primary metal width is not performed.

Since the XFMR power combiner used in this design has two sections, the spacing between each section of the XFMRs might play a role in the loss. As shown in Fig 5.5, the effect of mutual magnetic coupling between the adjacent XFMRs is not limiting the loss so long as the two sections are separated by a reasonable distance. For this reason, a "figure-8" structure as proposed in [73] is not used here to specifically optimize for the reduced mutual coupling between the adjacent XFMR sections. Simulations showed that the "figure-8" structure is

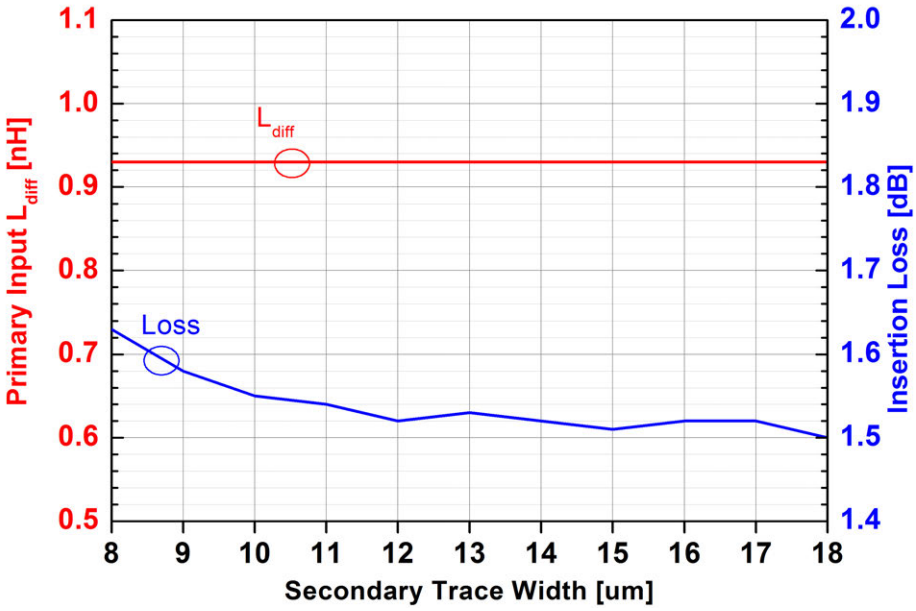


Figure 5.4: Differential input inductance and loss versus secondary trace width.

able to improve the loss by at most 0.1dB (which is the difference between the existing dual-section XFMR without "figure-8" structure and a completely isolated single-section XFMR of the same geometry); meanwhile, the cross connections at the intersection between the two XFMRs in a "figure-8" structure is challenging without the simultaneous availability of two highly-conducting metal layers.

Note that in each of the above parametrized sweeps, the secondary shunt capacitance has to be adjusted accordingly to give the optimum loss, as shown in Fig 5.6. In this experiment of optimizing secondary tuning capacitance, Cadence schematic simulations are performed where the XFMR is driven differentially from the primary, and is terminated single-endedly at the secondary by a fixed 50Ω load in parallel with a variable capacitance; the secondary tuning cap is optimized for the lowest insertion loss. In this design, 0.8pF shunt capacitance realized as Metal-Oxide-Metal (MOM) capacitor is placed at the secondary.

Finally, the input shunt inductance (measured in the differential mode) and the loss are swept versus frequency under the typical- and max-resistance corners (Fig 5.7). It is shown that a 22% increase in the metal resistivity (as in max-resistance corner) results in about 0.2dB loss increase but introduces much less significant change to the inductance value.

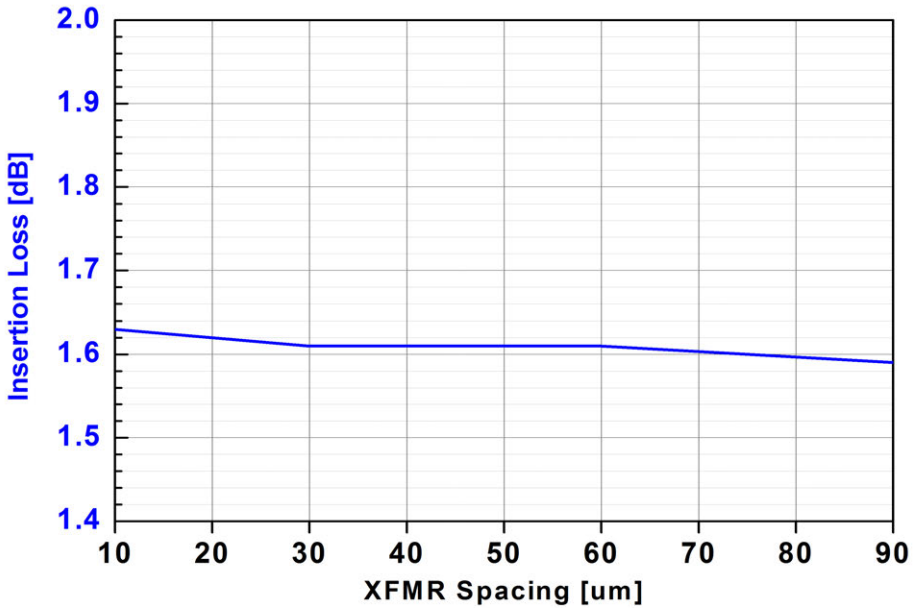


Figure 5.5: Loss versus XFMR spacing.

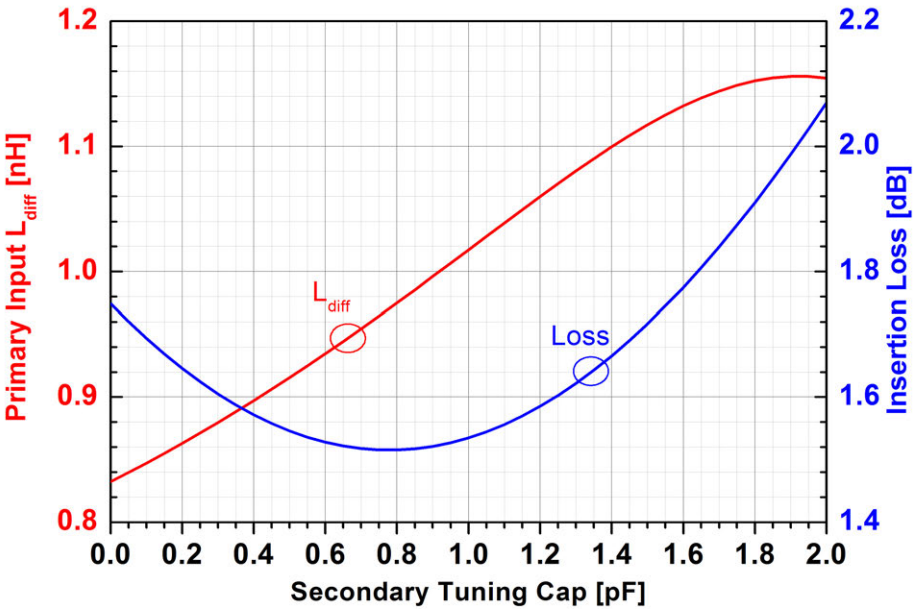


Figure 5.6: Differential input inductance and loss versus XFMR secondary tuning capacitance.

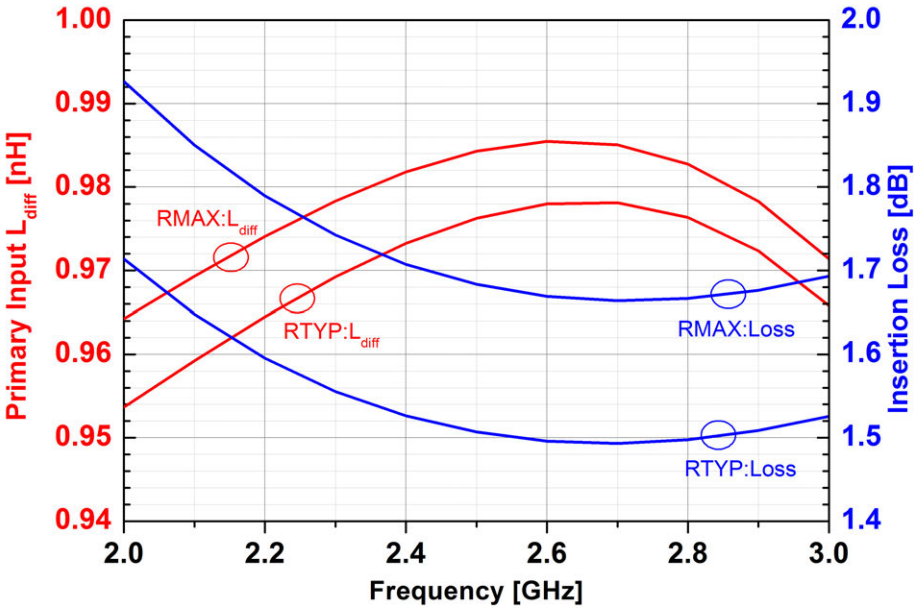


Figure 5.7: Differential input inductance and loss versus frequency under typical and max resistance corners.

5.2 Impedance Boosting

5.2.1 Shorting the Primary

The primary connected to the off-PA is shorted in high impedance mode to ensure it does not add excessive loss. This is often done by an additional shunt switch (Fig 5.8(a)) that is implemented by a thick-oxide (e.g. 2.5/3.3V) device to reliably withstand the high voltage swings present when this PA is operating [12]. However, dynamic impedance modulation requires that the shunt switch be time-synchronized with the rest of the modulation (amplitude and phase). This is difficult to achieve because the desired synchronization is between different supply domains (2.5/3.3V versus 1.0V core digital). Meanwhile, the large parasitics associated with the switch tend to introduce additional loss and degrade the overall efficiency.

To resolve the above issues, we re-use the PA itself as the shorting switch (Fig 5.8(b)) ([74]). To prevent short-circuit current directly from the supply to ground when the PA devices are used in this manner, a PMOS series switch that is turned off in this condition is inserted between the XFMR center tap and the supply. Although the width of this PMOS is even larger than the additional shunt device would have been, it is separated from the RF signal path and is switched on/off slower than the BB modulation rate. Therefore, the parasitics of this switch as well as the power consumed by driving it are manageable. Simulations show that even with the tuned (albeit wideband) XFMR, the PA output settles sufficiently quickly after impedance switching events. The PA can therefore be dynamically

configured between the two impedance modes summarized in Table 5.1, with the detailed circuitry illustrated in Fig 5.9. In simulations, the supply switch introduces a DC IR drop of 50mV (in slow corner and at elevated temperature) at peak power.

Table 5.1: Dynamic impedance configurations.

	Low Drain Impedance	**High Drain Impedance**
P_{out} **Range**	(P_{sat}-6.5dB) $\leqslant P_{out} \leqq P_{sat}$	$P_{out} \leqslant$ (P_{sat}-6.5dB)
Supply Switch	ON	OFF
PA1	Transmitting	Transmitting
PA2	Transmitting	g_m-gate pulled high (Fig 5.8(b))

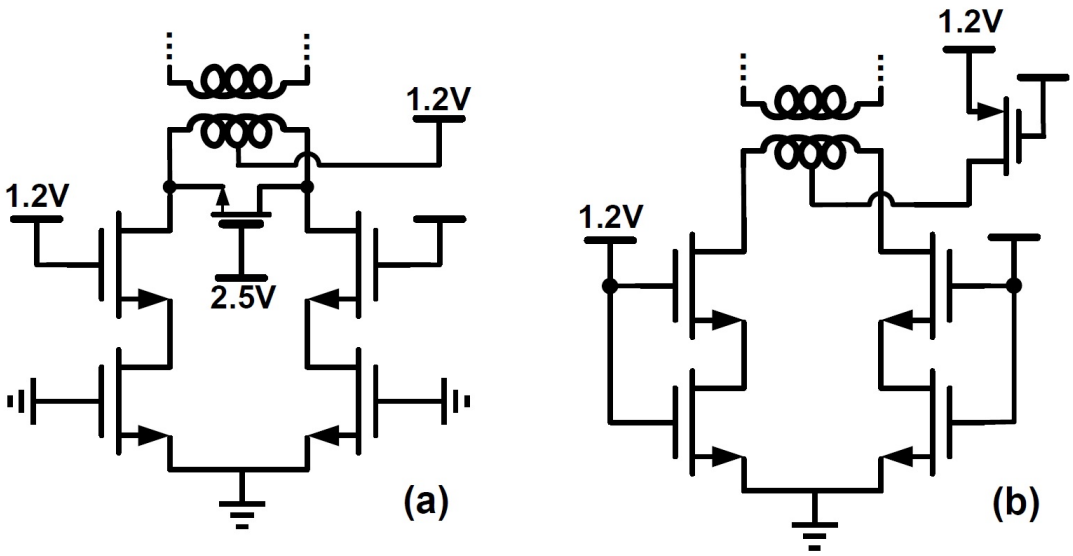


Figure 5.8: Shorting the XFMR primary with a) additional thick-oxide device and b) PA-device itself.

5.2.2 Efficiency Loss in Backoff Mode

In the high impedance configuration, the primary connected to the on-PA presents a similar inductive susceptance and roughly half the conductance, compared to the case where both XFMR sections are driven identically (Table 5.2). Tuning out the inductive susceptance with shunt capacitance ensures that the impedance is indeed doubled without frequency re-tuning at the primary.

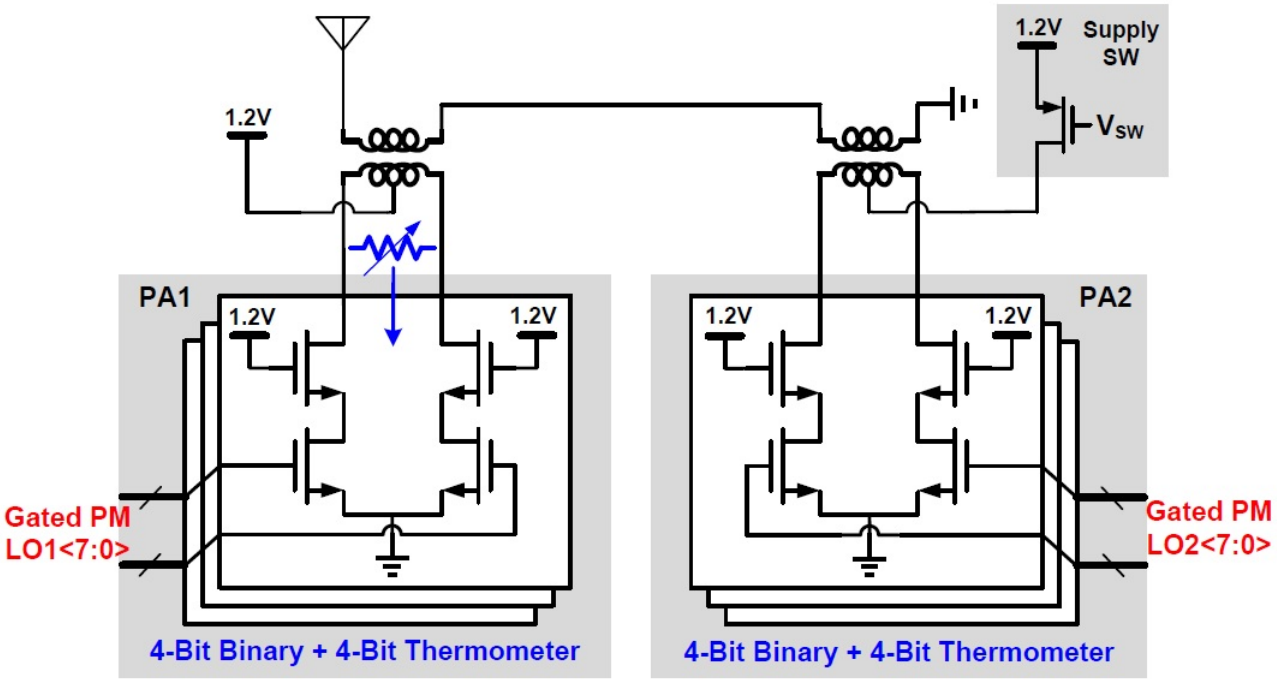


Figure 5.9: Two 8-bit RF-DACs with XFMR-based impedance modulator.

Table 5.2: Simulated XFMR performance.

	Both primaries driven identically	**One primary driven while the other shorted**
Insertion Loss [dB]	1.5	2.3
Power Efficiency [%]	71	59
Primary Input Impedance	22Ω || 0.93nH	40Ω || 0.89nH
Secondary Termination	50Ω || 0.8pF	

The insertion loss of the active XFMR, however, increases by 0.8dB (Table 5.2) due to an increase in the secondary termination (50ohm as opposed to 25ohm) ([18]). As a result, the efficiency of the PA with XFMR at 6-dB backoff in the high impedance configuration degrades from the peak efficiency. Nonetheless, impedance boosting still offers a significant efficiency improvement; at the same 6-dB backoff in simulations, the boosted impedance reduces PA power consumption by 112mW i.e., by 41% (Table 5.3).

Table 5.3: Simulated performance of PA with XFMR.

Power Level	**Power [dBm]**	**Drain Efficiency [%]**	**Supply Current [mA]**
P_{sat}	23.9	49	417
6dB backoff, w/o impedance boost	17.8	23	218
6dB backoff, w/t impedance boost	17.7	39	125
PA supply	1.2V		
PA g_m width	2mm		
PA cascode width	3mm		

5.3 Timing Synchronization

If the PA2 shorts the XFMR primary to ground while the supply switch is simultaneously on, excessive short-circuit current will flow, destroying metal traces and devices. Furthermore, such a large current spike could significantly degrade the efficiency. Non-overlapping control waveforms for the supply switch and PA2 are thus enforced by digital logic to eliminate the potential glitch and ensure reliable operation (Fig 5.10).

In fact, to minimize glitches and avoid degradation in EVM and ACPR, delay matching should be ensured not only among BB AM/PM/impedance-modulation paths, but also between the two RF-DACs (when they are both transmitting), as well as among the unit elements inside the RF-DAC (Fig 3.5). Dummy stages are added after the final re-timing flip-flops (Fig 5.10) to improve the delay matching. In addition, the low-skew BB clock and differential PM-LO distribution networks are shielded and laid out in a manner that maintains low timing mismatch.

5.4 Conclusion

A dual-section transformer power combiner is implemented with low loss in a process without Ultra Thick Metals. Parallel primary windings help the transformer to meet the DC-electromigration requirements with relatively narrow metal traces; they also help to reduce the series AC loss by counter-acting the proximity effect. For the transformer-based impedance modulator, we re-use the PA device itself to short the primary of the transformer in the boosted-impedance mode. Doing so improves the timing synchronization between the impedance modulation and the rest of the modulation schemes; also, it eliminates an additional large device on the RF signal path and the associated loss. To avoid short-circuit

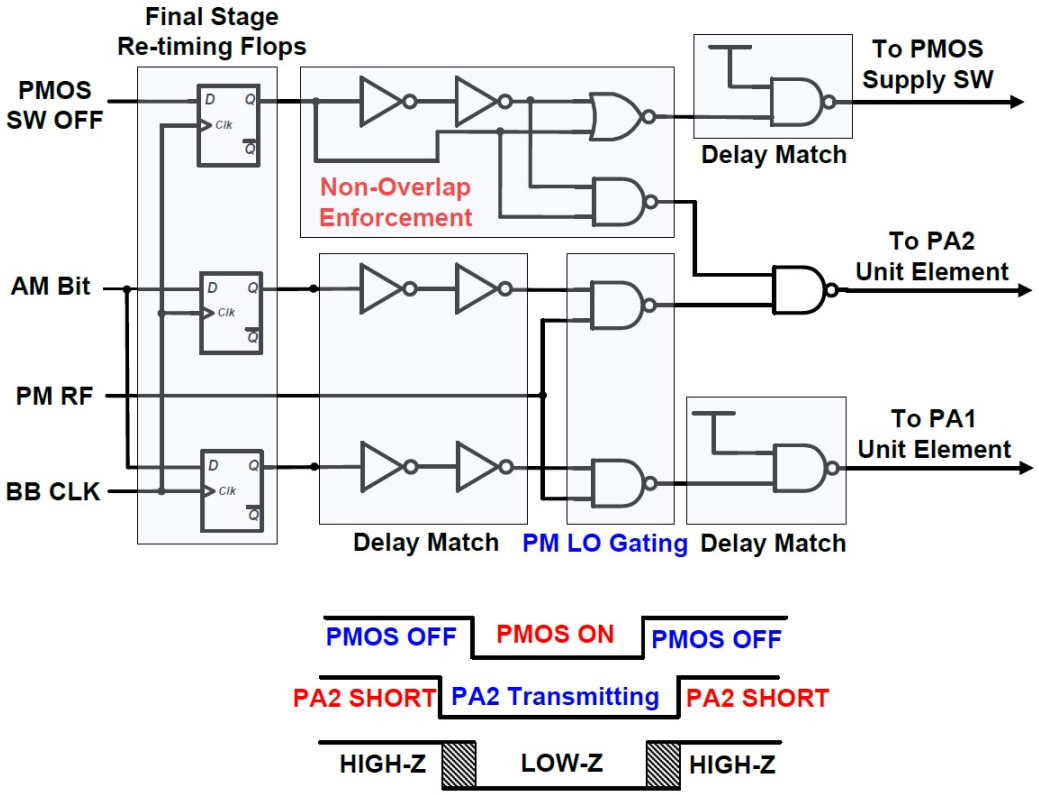


Figure 5.10: Digital logic to combine AM bits and PMOS supply switch control with PM-LO.

current between the supply and the ground when the PA device is used in such a manner, we add a PMOS supply switch in series which is turned off in the same condition. Although our scheme ensures the primary can be shorted by low-enough resistance, the insertion loss of the active transformer still increases considerably due to a significant increase in the effective secondary termination. This mechanism plays a major role in the efficiency degradation at 6dB backoff power with boosted impedance as compared to at peak power with lower impedance.

Chapter 6

Open-Loop Phase Modulator

6.1 Open-Loop Phase Interpolator Architecture

Due to the higher bandwidth on the phase path, an open-loop architecture (Fig 6.1) is chosen for the phase modulator ([75]). The core component is a high-resolution I/Q phase interpolator (PI), as shown in Fig 6.2. The quadrature LO inputs to the PI are generated from a differential sine-wave at twice the carrier frequency through a divider implemented in Current-Mode Logic (CML). Inside the PI, phase modulation is achieved by weighted summation of the I/Q-LO signals, much like a quadrature mixer in an analog transmitter. Differential current-DACs are used to implement the I/Q weighting with constant output common-mode level. The digital I/Q weights are derived from 9-bit PM signal in such a way that the sum of the weightings ($|I| + |Q|$) is kept constant for all phase codes; this minimizes output amplitude variation without increasing logic complexity.

6.2 Phase Resolution and Current-DAC Mismatch

The 9-bit PI comprises of two 8-bit DACs, each providing 7-bit magnitude resolution as well as 1-bit sign control. Segmented into 4bit binary- and 3bit thermometer-weighted structure, the DAC device sizes are mainly fixed by matching requirements. In order to elucidate these size requirements, we will next describe the effect of the DAC unit-element mismatch on the phase resolution of the PI. As shown in Fig 6.3, given that phase is related to "length" in a polar coordinate system by

$$\theta = \frac{L_{arc}}{R} \tag{6.1}$$

where L_{arc} is the length of the arc and R is the radius of the circle. The Differential Non-Linearity (DNL) of the equivalent phase-DAC is related to the DNL of the current DAC by

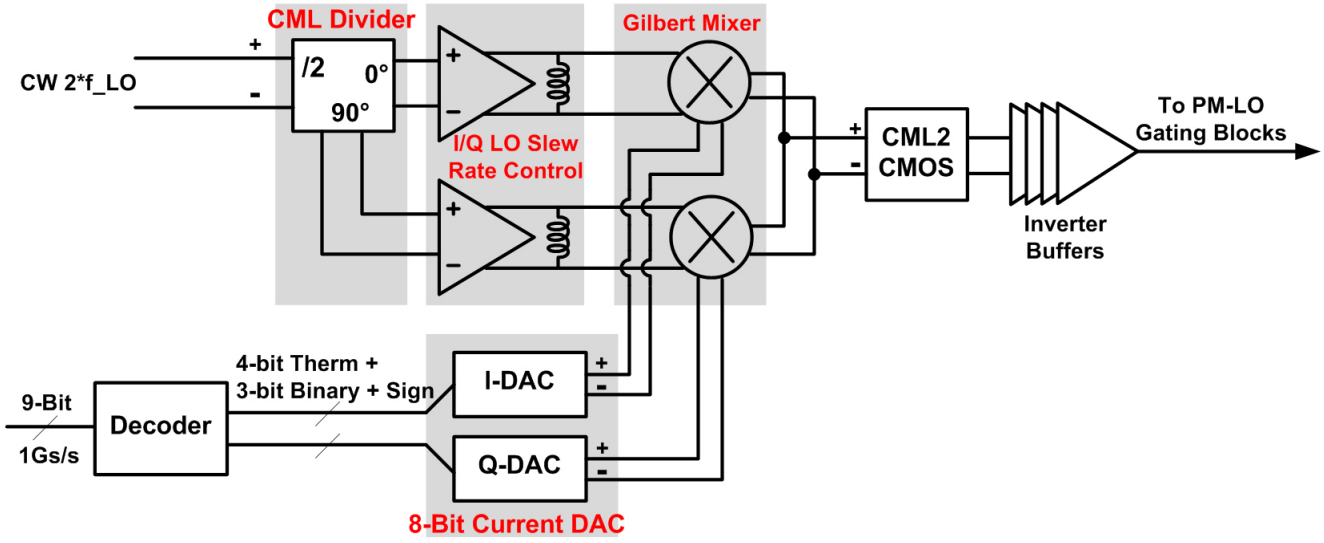


Figure 6.1: The open-loop phase modulator architecture.

$$\sigma_{\mathrm{DNL,phase}} \approx \frac{\sigma_{\mathrm{DNL,IQ}}}{\sqrt{I^2+Q^2}} \tag{6.2}$$

With fixed mismatch (usually by fixing unit device size and the number of binary-weighted devices), the phase resolution can be improved by 1-bit by doubling the number of DAC unit elements and therefore doubling the denominator in Eq (6.2). This is in contrast to the case where a voltage DAC has a fixed full-scale range and therefore increasing the resolution by 1-bit incurs reducing the mismatch between unit elements to $\frac{1}{2}$, which leads to a quadrupled device size as well as power consumption. In this work, the DAC is sized so that the 3σ phase DNL due to mismatch is half the phase Least Significant Bit (LSB).

6.3 Code-to-Phase Linearity

In this work, several steps were taken to ensure sufficient the codeword-to-phase linearity. First, interpolating between two pure square-waves that are time-shifted by $\frac{1}{4}$-cycle between each other would result in large phase discontinuity, especially around 45-degrees. That is because the two square waves contain significant harmonics that are not quadrature-related in the same way as at fundamental ([76]). An LC resonant network is therefore used to suppress harmonics at the PI quadrature-LO inputs. With a two-layer differential structure, the inductor used within this network has an equivalent shunt inductance of 8.1nH with a Q-factor of 3.6 at 2.4GHz (Fig 6.4) within a small area of $60\mu m \times 60\mu m$.

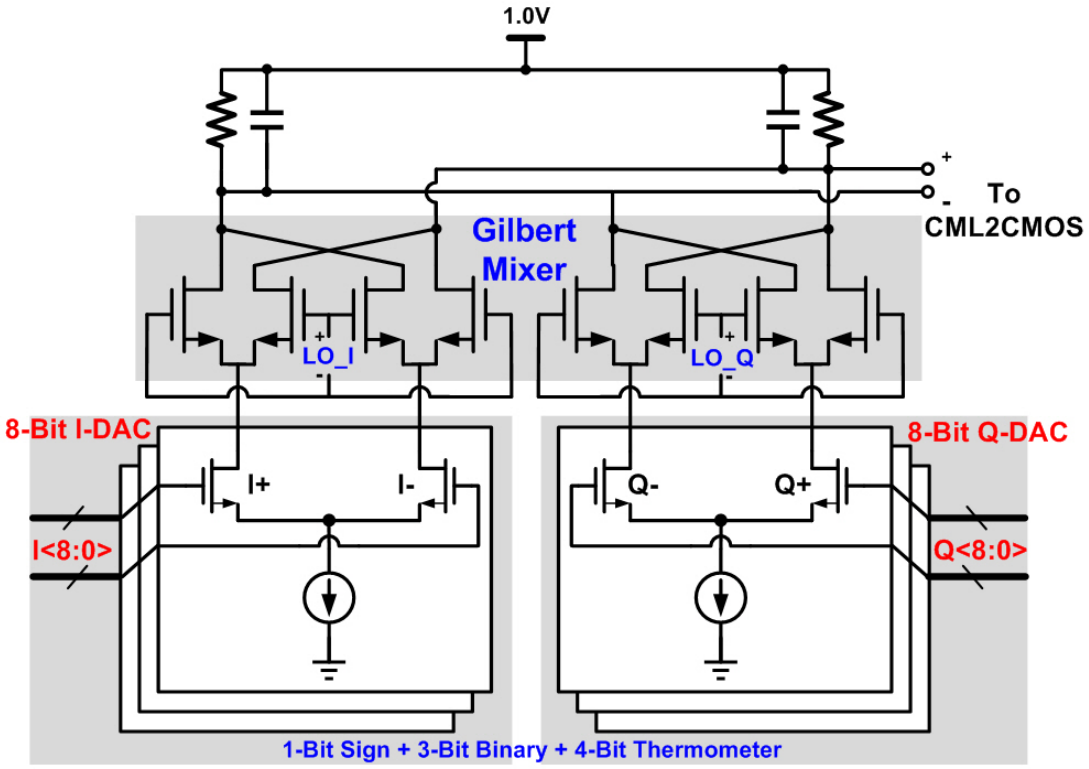


Figure 6.2: The phase interpolator circuitry.

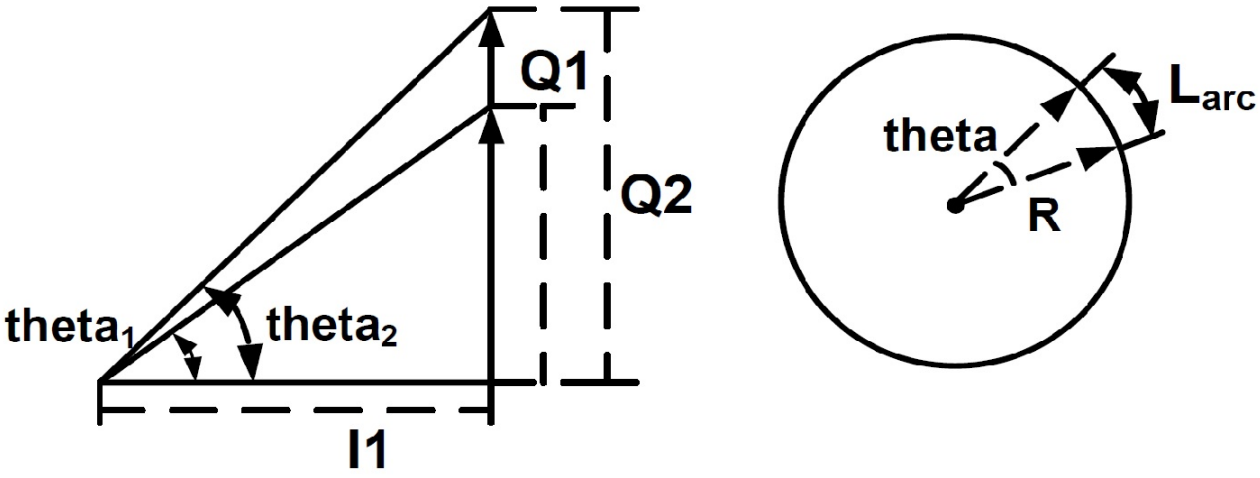


Figure 6.3: Phase approximation and phase representation in a polar coordinate.

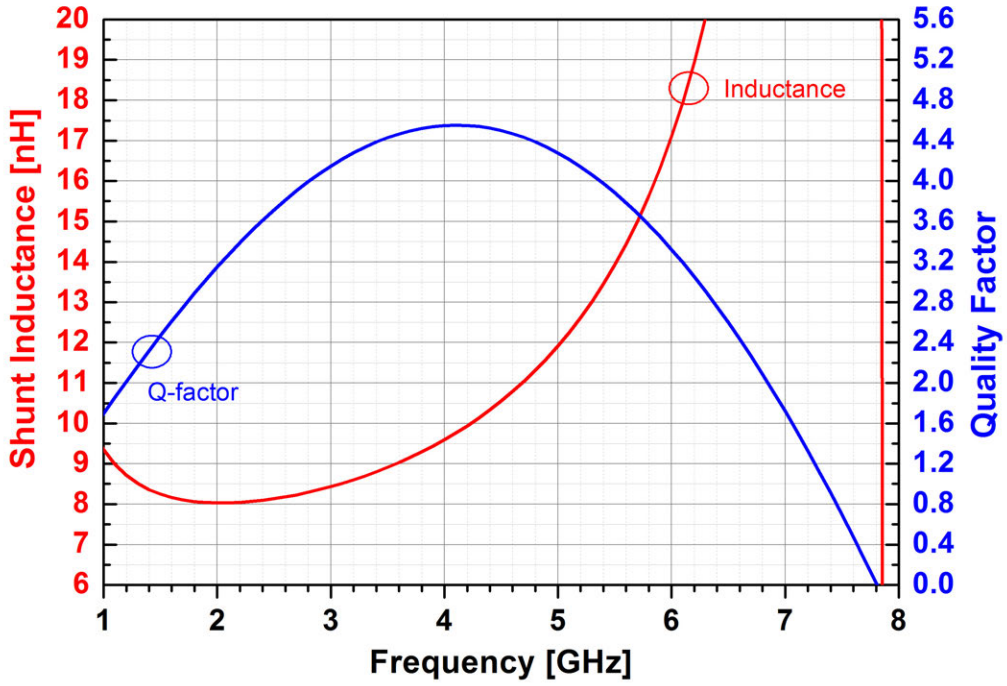


Figure 6.4: The simulated shunt inductance and qualify factor of the multi-layer differential inductor.

Second, harmonics arising from the nonlinear switching actions inside the Gilbert core also degrade phase linearity. Rather than using a band-pass network which would have larger in-band group delay variation than a low-pass at a similar cut-off frequency (such group delay variation would lead to distortion of the wideband PM signal), an RC low-pass network with corner frequency slightly higher than the carrier is used at the PI output. Meanwhile, the amplitude (200mV differential) of the I/Q-LO is carefully engineered to be able to fully steer the currents within the Gilbert core while minimizing hard-switching induced harmonics.

6.4 CML-to-CMOS PM-LO Receiver

A CML-to-CMOS converter is used at the PI output to regenerate rail-to-rail swing for the succeeding inverter buffers. Since the PI output has a code dependent output swing level (varying between 150mV and 200mV, due to non-constant $\sqrt{I^2+Q^2}$ despite a constant $|I|+|Q|$), the converter needs to have minimum AM-PM distortion. A wide-band two-stage Operational Trans-conductance Amplifier (OTA) biased deep into class-A region (Fig 6.5) was therefore used. The entire phase modulator achieves a worst-case simulated phase step

of 1.2-degrees at 2.4GHz.

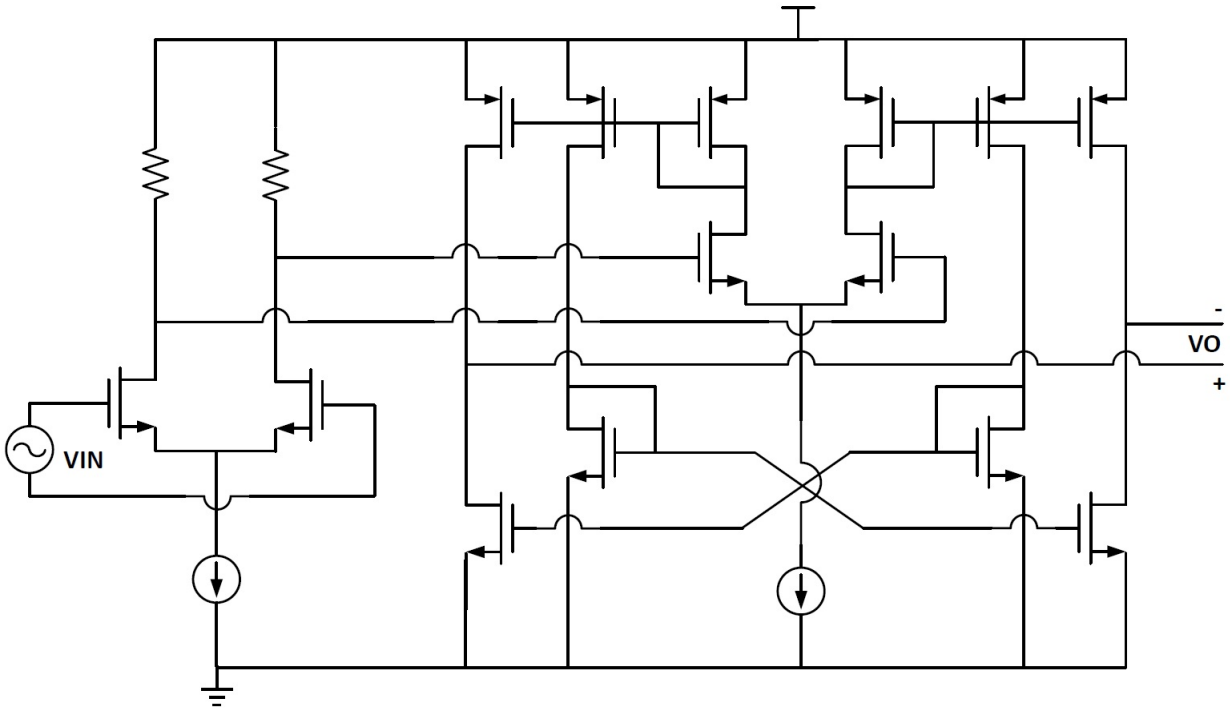


Figure 6.5: The two-stage OTA as CML-to-CMOS PM-LO receiver.

6.5 Polar Phase Path Power Overhead

Running from a 1V supply, the entire phase modulator consumes 9mW of total power (Table 6.1). This power would also have to be spent (or perhaps even more due to the additional need for amplitude linearity) in a Cartesian TX, where a quadrature mixer is required to up-convert the I/Q baseband to drive the analog PA. Therefore, our open-loop implementation does not necessarily introduce power overhead to the polar architecture as compared to a Cartesian approach. The phase path does have to handle a higher bandwidth, but the resultant 9mW of power consumption (note that the only extra power due to the high bandwidth requirement is mostly from the digital gates that drive the high-speed current-DACs, which are a small fraction of the total) compares favorably (though not in a precise manner since the functionality is quite different) with up-conversion mixers in Cartesian WLAN TXs ([6][77][78]).

Table 6.1: Phase modulator power breakdown

Phase Modulator Block	**Power Consumption [mW]**
I/Q Divider	1.5
I/Q Buffer	1.5
Gilbert Mixer + DAC	4
CML2CMOS Buffer	1
1-GHz Clocking + Logic	1
Total	9

6.6 Conclusion

To achieve wideband phase modulation with good power efficiency, we employ an open-loop phase interpolator architecture on the polar phase path. The phase interpolator is essentially an I/Q up-conversion mixer to produce a weighted summation between the quadrature LO inputs according to the baseband current DACs. The LO port to the phase interpolator is tuned by an area-efficient LC network to suppress harmonic contents within the otherwise square-wave shaped LO signals. The phase interpolator output is further filtered by an RC low-pass network with low in-band group delay variation to reduce the harmonic contents due to the nonlinear Gilbert switching actions. The LO slew-rate control and RC-filtering improve the codeword-to-phase linearity for the phase interpolator. At the phase interpolator output, the low swing signal is regenerated to full-rail by an two-stage OTA-based CML2CMOS receiver with good phase linearity and low AM-PM distortions. The entire phase path achieves 8.7-bit static phase resolution in measurements with 2.2-GHz carrier, while consuming only 9mW total power under 1V supply. We have therefore demonstrated the power overhead from the polar phase path is not necessarily prohibitive as compared to a Cartesian transmitter where an I/Q up-conversion mixer is also needed, and possibly with even better amplitude linearity.

Chapter 7

Baseband Digital Filtering

Baseband digital filtering is fully integrated on the amplitude and the phase path to knock down the spectral images associated with the baseband input sample rate. The filter takes the input samples at 200MS/s, does the interpolation and outputs data at 1GS/s. The output data at the digital/RF-DAC interface, however, would still have spectral images at multiples of 1GHz away from the carrier in the RF output spectrum.

7.1 Choice of Nyquist Filter Type

In the filter-last baseband architecture as shown in Fig. 3.21, we have to make sure the final output closely resembles that in the filter-first architecture (also shown in Fig. 3.21). Based upon this consideration, a Nyquist filter type is chosen as opposed to an equi-ripple one. At a slight expense of stopband attenuation for a fixed filter order, the Nyquist filter exactly preserves the input samples within the down-sampled output data ([79][80]). In this way, the output data at 1GS/s, when down-sampled to 200MS/s at the correct phase, are made to be exactly the same as the input samples before interpolation. The predistortion results are therefore faithfully relayed to the filter output, which ensures the down-sampled version of the final output samples are exactly the same as those in the filter-first architecture.

7.2 Nyquist Filter Specification

In this design, a generic Nyquist filter is synthesized in Matlab for coefficient quantization (to be explained later). The filter synthesis takes the performance specifications as its input, including the interpolation ratio, the transition bandwidth and the stopband attenuation. In this design, the interpolation ratio (which is 5) is fixed by the baseband input sample rate of 200MS/s and the output rate of 1GS/s. The transition bandwidth is the frequency spacing between the pass-band and the stopband, as normalized to the sampling frequency. Since the Nyquist filter faithfully relays the input samples to the down-sampled output, the physical meaning of a pass-band in such a context is somewhat vague; independent of the “pass-band

ripple" or "pass-band bandwidth", one of the down-sampled output data is guaranteed to be equal to the input. As a result, the only remaining specification for the Nyquist filter is the stopband attenuation.

It has been estimated in system-level simulations that the quantization noise floor is about -60dBr (as normalized to the in-band signal) at 200MHz offset. For coexistence considerations, the spectral images would ideally be attenuated down below the noise floor, rather than just below the FCC spectral mask (which is -40dBr as shown in Fig 3.1). Therefore, the specification of stopband attenuation is chosen to be 60dB in this design. The magnitude response of the interpolation filter after coefficient quantization is shown in Fig 7.1.

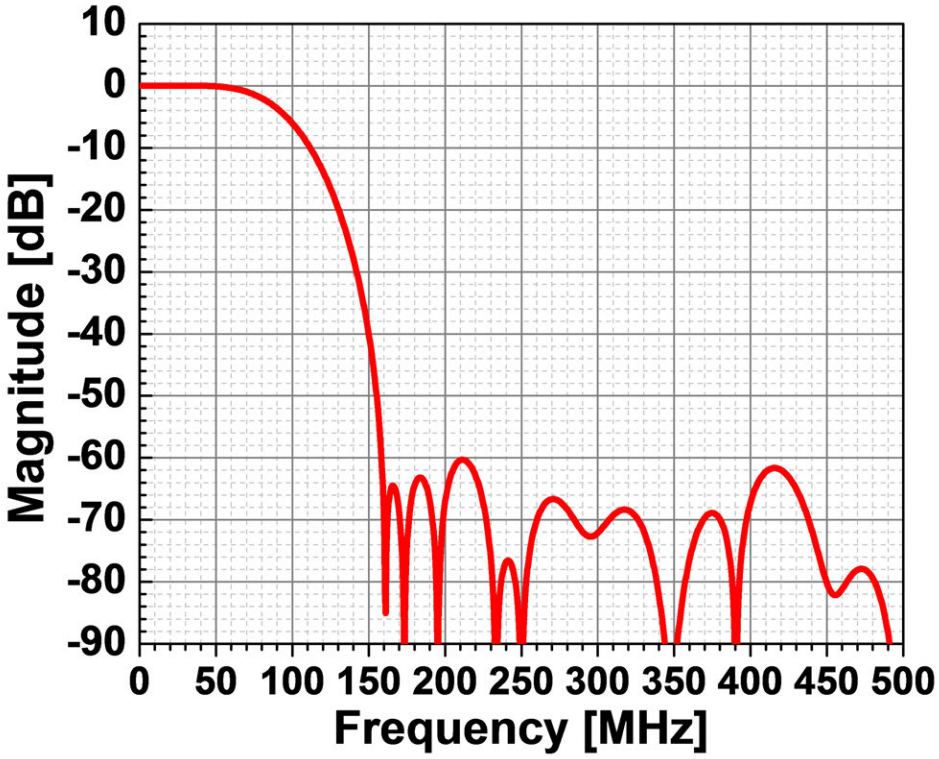


Figure 7.1: The magnitude response of the interpolation filter after coefficient quantization.

7.3 Poly-Phase Decomposition

For an interpolation filter, the input samples are conceptually first up-sampled by sample-and-hold (zero-order hold) or zero insertion. Depending on the exact up-sampling method, different poly-phase decomposition techniques are used to parallelize the generic 1G/s filter into five 200MS/s sub-ones. The outputs of the five sub-filters can then be combined into a single stream of 1GS/s. Parallelism allows each sub-filter to run at a much lower speed,

opening up the feasibility for digital synthesis of the sub-filters directly from standard cells. An automatic synthesis procedure is desirable because it streamlines the design procedures and greatly reduces the design effort. The 5-to-1 serializer as well as the divide-by-5 circuitry, however, would still have to be custom designed. Furthermore, the parallelism technique might help to simplify the actual design and therefore save the power consumption in some cases, as explained later in this chapter.

7.3.1 Poly-Phase Decomposition for Up-Sampling by Zero Insertion

The input-output characteristic of a generic Finite Impulse Response (FIR) filter can be expressed as

$$y = \sum_{i=1}^{i=n+1} a_i x_i \tag{7.1}$$

where x_i is the up-sampled input data, a_i is the filter coefficient, and n is the filter order, i.e. a filter with $(n+1)$ taps is said to be of order n.

For a Nyquist filter, the input is up-sampled by zero insertion. Therefore, for an input sequence of v_i, and an up-sampling ratio of 5, the filter output at any instant of time can be expressed as one the following expressions

$$\begin{cases} y(1) = \sum_{i=1}^{i=n+1} a_i x_i = a_1 v_1 + a_6 v_6 + a_{11} v_{11} + ... \\ y(2) = \sum_{i=1}^{i=n+1} a_i x_i = a_2 v_1 + a_7 v_6 + a_{12} v_{11} + ... \\ y(3) = \sum_{i=1}^{i=n+1} a_i x_i = a_3 v_1 + a_8 v_6 + a_{13} v_{11} + ... \\ y(4) = \sum_{i=1}^{i=n+1} a_i x_i = a_4 v_1 + a_9 v_6 + a_{14} v_{11} + ... \\ y(5) = \sum_{i=1}^{i=n+1} a_i x_i = a_5 v_1 + a_{10} v_6 + a_{15} v_{11} + ... \end{cases} \tag{7.2}$$

Thus, we see from the above equations that after up-sampling by zero insertion, the input data before up-sampling (v_i) can only be associated with the filter coefficients, a_i, in the five different ways. If we designate a different phase to each of $y(1)$, $y(2)$, $y(3)$, $y(4)$, $y(5)$, we can use a different sub-filter to implement each difference equation, with the coefficients of each sub-filter being

$$\begin{cases} b(1)_1 = a_1 \\ b(1)_2 = a_6 \\ b(1)_3 = a_{11} \\ \quad\quad ... \end{cases} \tag{7.3}$$

$$\begin{cases} b(2)_1 = a_2 \\ b(2)_2 = a_7 \\ b(2)_3 = a_{12} \\ \quad\quad ... \end{cases} \tag{7.4}$$

$$\begin{cases} b(3)_1 = a_3 \\ b(3)_2 = a_8 \\ b(3)_3 = a_{13} \\ \quad\quad ... \end{cases} \tag{7.5}$$

$$\begin{cases} b(4)_1 = a_4 \\ b(4)_2 = a_9 \\ b(4)_3 = a_{14} \\ \quad\quad ... \end{cases} \tag{7.6}$$

$$\begin{cases} b(5)_1 = a_5 \\ b(5)_2 = a_{10} \\ b(5)_3 = a_{15} \\ \quad\quad ... \end{cases} \tag{7.7}$$

where $b(i)_j$ is the j-th coefficient for the i-th sub-filter. Since the input data, v_i, is entering each sub-filter at 200MS/s, the sub-filter output only has to update its value every $5ns$. In other words, each sub-filter is clocked at 200MHz. Therefore, poly-phase decomposition of a Nyquist filter indeed parallelizes the original fast filter into a number of slower sub-ones.

The filter architecture in this design is shown in Fig 7.2, where the five sub-filters are synthesized as a whole from digital standard cells while the clock divider as well as the serializer are custom designed.

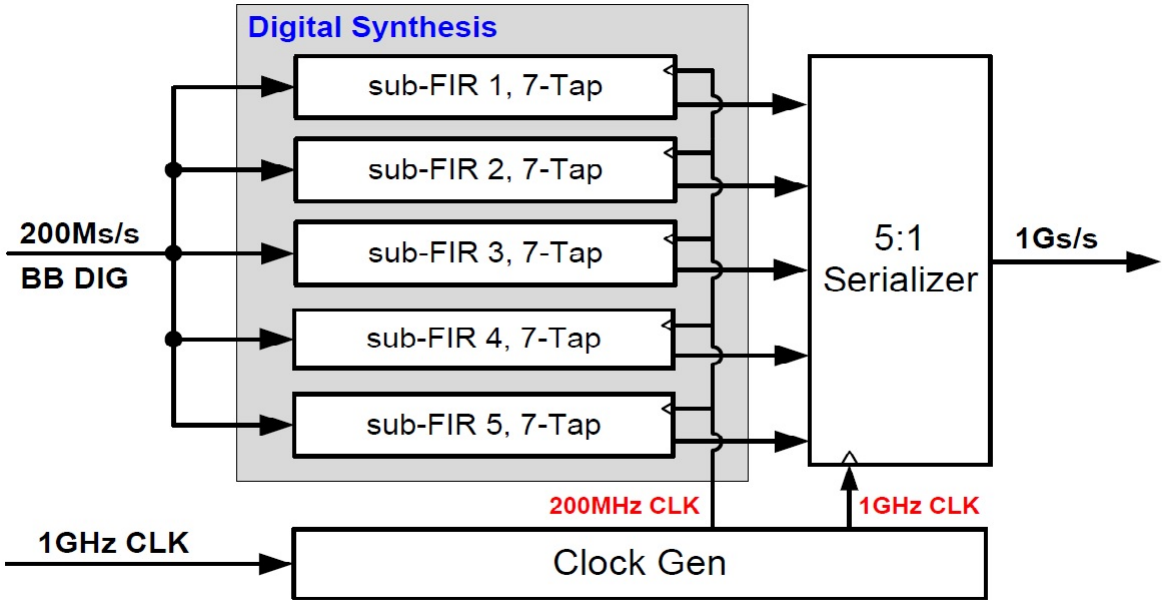


Figure 7.2: The poly-phase FIR architecture.

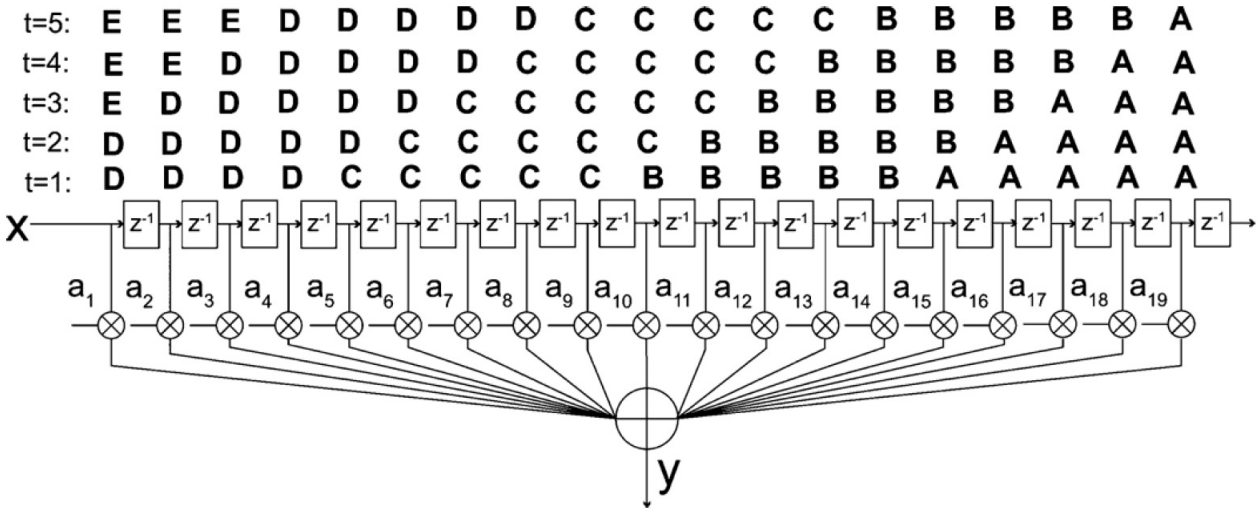


Figure 7.3: The concept of coefficient grouping in a parallelized FIR filter with zero-order-hold up-sampling.

7.3.2 Poly-Phase Decomposition for Up-Sampling by Zero-Order-Hold

In [13], we have proposed another poly-phase decomposition technique for up-sampling by zero-order-hold. It allows us to parallelize the design into 5 sub-ones without incurring 5x increase in the hardware cost, as explained below.

Assume the filter input signal is obtained from 5x up-sampling by sample-and-hold of the 200-MS/s consecutive time-domain data samples, A, B, C, D, and E, where A arrives first. Then, every five consecutive data at the filter input are identical. After 5x up-sampling, the five consecutive samples are identical at the filter input, as shown in Fig 7.3. Therefore, for each of the individual sub-FIR filters in the interleaved implementation, all coefficients with the same input data can be lumped together into a single term. For example, assume the first sub-filter corresponds to time instant $t = 1$ in Fig 7.3. The difference equation representing that sub-filter at that time instant would be

$$y = \sum_{k=1}^{4}(a_k \cdot D) + \sum_{k=5}^{9}(a_k \cdot C) + \sum_{k=10}^{14}(a_k \cdot B) + \sum_{k=15}^{19}(a_k \cdot A) \tag{7.8}$$

However, the above equation can also be written as

$$y = 0 \cdot E + (\sum_{k=1}^{4} a_k) \cdot D + (\sum_{k=5}^{9} a_k) \cdot C + (\sum_{k=10}^{14} a_k) \cdot B + (\sum_{k=15}^{19} a_k) \cdot A \tag{7.9}$$

Thus, we see that because of repeating samples, it is possible to group five consecutive coefficients. The above difference equation can be readily implemented by a fourth-order FIR filter

$$y = \sum_{k=1}^{5} b_k \cdot x_k \tag{7.10}$$

where the coefficients are given by

$$\begin{cases} b_1 = 0 \\ b_2 = a_1 + a_2 + a_3 + a_4 \\ b_3 = a_5 + a_6 + a_7 + a_8 + a_9 \\ b_4 = a_{10} + a_{11} + a_{12} + a_{13} + a_{14} \\ b_5 = a_{15} + a_{16} + a_{17} + a_{18} + a_{19} \end{cases} \tag{7.11}$$

Similarly, the filter outputs at time instants $t = 2, 3, 4$ and 5, can be expressed as the sum of each 200-Ms/s data sample (A, B, C, D, and E) multiplied with a different set of coefficients, with these coefficients repeating every 5 up-sampled cycles. This observation allows us to implement the generic interpolating 1-GS/s FIR filter as five parallel 200-MS/s

sub-FIR filters followed by a 5:1 serializer. Unlike conventional parallelism, our architecture dose not require a 5x increase in hardware cost since the total number of Signed Power-of-Two (SPT, to be explained later) terms representing the sub-filter coefficients are now greatly reduced by the coefficient grouping. As a result, the adder count and power can be greatly reduced by this poly-phase decomposition technique with coefficient grouping and pre-computation.

7.4 Measure of Filter Complexity

According to Eq (7.1), a generic FIR filter can be implemented as a number of adders and flip-flops. Also shown in Fig 7.3, each output sample is calculated as the sum of delayed versions of the input samples multiplied by different coefficients. In the digital signal processing community, it is well known that if each filter coefficient is a sum of signed power-of-two (SPT) terms, the filter can be implemented without using multipliers. However, in a typical DSP IC with two's complement as its number representation system, a filter coefficient is always represented as a sum of SPT terms and the multiplication operation is always accomplished by shift-and-add operations; there is no such "multiplier" as is implemented without adders. Despite the confusing statements, it is clear that the primary operations inside a filter include delay and addition.

As a result, the power consumption of an IC filter usually consists of those from the memory elements (e.g. flip-flops) that are responsible for the delay operations and those from the adders. It is then postulated that the complexity of a filter can be measured by the number of adders. This is not so mathematically rigorous since it does not count the complexity of the memory elements and the associated clock distribution network. Nonetheless, a larger number of adders tend to imply a larger number of filter taps, and hence more storage and clocking elements. In fact, the total number of SPT terms to represent all the filter coefficients is historically used within the DSP community as a gauge of filter complexity and the associated hardware cost. Suppose a filter requires x of SPT terms for coefficient representation, it would require $(x-1)$ two-way adders to compute each output sample at any instant of time.

Therefore, the total number of SPT terms required to represent its coefficients is also used here as a measure of filter complexity. For example, an FIR filter with two taps being $\frac{3}{8}$ and $\frac{5}{8}$ would require a total of 4 SPT terms for coefficient representation. It should be noted that a coefficient can be represented by the same number of SPT terms in different ways, as shown below

$$\begin{cases} \frac{3}{8} = \frac{1}{8} + \frac{1}{4} = \frac{1}{2} - \frac{1}{8} \\ \frac{5}{8} = \frac{1}{8} + \frac{1}{2} \end{cases} \tag{7.12}$$

7.5 Filter Synthesis with A Minimum Number of SPT Terms

The Matlab filter synthesis only provides a filter with coefficients ("taps") in floating-point precision. To facilitate power-efficient IC implementation, the filter coefficients have to be truncated to finite precision to save area and power. This process is called "coefficient quantization". After coefficient quantization, however, the filter performance tends to degrade: the stopband attenuation might get reduced while the pass-band ripple increases. Therefore, an IC-implementable filter synthesis problem, at the behavior level, can be formulated as the one to find the minimum total number of SPT terms such that a filter, with its coefficients quantized to this total number of SPT terms, is able to meet the performance specification.

The above synthesis problem can be solved in the following steps:

Step 1: The total number of SPT terms is fixed to 1.
Step 2: A brand new filter whose performance exceeds the specifications is synthesized from Matlab with floating-point precision.
Step 3: The filter coefficients are quantized by a total number of SPT terms as defined in Step 1.
Step 4: The filter performance after coefficient quantization is benchmarked against specifications. If the performance fails to meet the spec, go to Step 5; otherwise go to Step 6.
Step 5: If a "sufficient" number of filters have been tried, restart and go back to Step 1 and increase the total number of SPT terms by 1; otherwise restart and go back to Step 2.
Step 6: A minimum number of SPT terms to meet the filter specifications has been found.

In the above process, a brand new filter can be obtained by perturbing the performance input (stopband attenuation, transition bandwidth and etc) to the Matlab synthesis protocol. Although it does not guarantee a global optimum, the above process does provide a filter which meets the expectations with low enough complexity. Throughout the process, Step 3 is the most important: it has to allocate a fixed total number of SPT terms to the filter coefficients in such a way that the resultant performance degradation is minimized. This by itself is challenging, as discussed in the following section.

7.6 Allocation of Signed Power-of-Two Terms For Filter Coefficient Quantization

In literature, quite a number of methods have been proposed to optimize the frequency response of a digital filter subject to discrete constraints imposed on its coefficient values. For example, the algorithm proposed in [81], [82] and [83] employs mixed-integer linear programming, and [84] proposes the weighted least-squares method, while [85], [86] and

[87] apply local search techniques. These methods, however, focus on the case where each filter coefficient is quantized to have the same number of SPT terms. In contrast, [88] has demonstrated the significant advantage of an allocation scheme where different coefficients are allowed to be presented by different numbers of SPT terms.

In this design, an SPT allocation scheme similar to [89] is used. It allows different coefficients to be quantized to different precisions. However, it does not guarantee the optimum assignment of SPT terms. The SPT-term assignment procedure is simply as follows.

Step 1: Let R be the total number of SPT terms to be allocated. Let a_i be the filter coefficients. Let $c(i)$ be the residual error for coefficient a_i after the quantization. Initialize $c(i) = |a_i|$ for all coefficients.
Step 2: Let $c(j)$ be the largest residual error among all coefficients.
Step 3: Allocate one more SPT term to coefficient a_j. Let the SPT term be S.
Step 4: Update $c(j) \Leftarrow c(j) - S$, $R \Leftarrow R - 1$.
Step 5: If $R = 0$, stop; otherwise, go back to Step 2 and repeat.

The only difference from the algorithm proposed in [89] is that, the "cost function", $c(i)$, is simply defined as the magnitude of the coefficient after quantization, while in [89], it is initialized as $0.36 \log_2(|a_i|)$ and has an update of $c(j) \Leftarrow c(j) - 1$ after one SPT term allocation. In simulation, it is found that the approach in [89] does not guarantee the assignment of SPT term to the coefficient with the largest magnitude, a rule which is more intuitively satisfying to us. For this reason, we have modified the initialization and update for $c(i)$.

In this design, to achieve 60dB stopband attenuation out of the 5x interpolation filter, the optimized generic filter has an order of 34, and 78 SPT terms for coefficient quantization.

7.7 Pipelining for Synthesis Timing Closure

To simplify the design effort and reduce design cycle, all the sub-filters as a whole are first synthesized by Synopsys Design Compiler (DC) from 65nm standard cell libraries, and then placed-and-routed in Synopsys IC Compiler (ICC). An automated synthesis script has been hand-crafted from scratch to make the full use of the various advanced features that have not been introduced into DC and ICC until very recently. The synthesis flow is even able to achieve the timing closure on a 1.8GHz filter design ([16]) under the worst PVT corner of slow, $0.9V_{dd}$ and $125°C$.

For the ultra high-speed design, a sufficient number of pipeline stages should be added into the synthesis flow to trade latency for speed. Also, the synthesis feature of register re-timing is exploited to allow the synthesis tool to freely move the flip-flops within a cloud of combinational logic to balance the delay among all pipeline stages, thereby achieving the best timing and power results. As shown in Fig 7.4, as the number of pipeline stages

increases to a certain number (8 in this case), the timing closure (indicated by a zero Worst-Negative-Slack) is achieved for the first time and with minimum power consumption. As we continue to increase the pipeline stages, the power consumption slightly increases due to a similar increased power from the sequential logic.

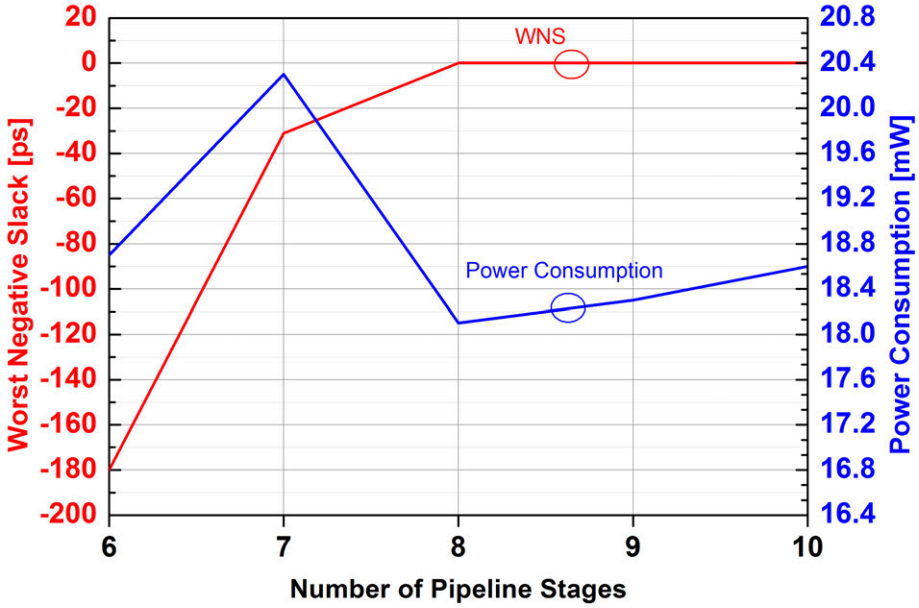


Figure 7.4: Worst-Negative-Slack and power consumption of a 1.8GHz filter ([16]) in a Design Compiler synthesis.

7.8 Amplitude Filter with Waveform Smoother

With impedance modulation, the amplitude codewords corresponding to 6.5-dB back-off differ greatly with different impedances (Fig. 8.4). When the desired RF amplitude varies smoothly across 6.5-dB backoff and triggers impedance switching, the amplitude filter will see a sharp transition between two consecutive codewords, due to a similar abrupt AM-AM step (Fig. 7.5). Although the down-sampled filter output is still accurate by virtue of utilizing a Nyquist type filter, inaccurate interpolated (filtered) values will result in between. To mitigate this, pre- and post-smoothers are embedded within the AM filter (Fig. 7.6) to maintain correctly interpolated AM codewords during impedance transitions. The pre-smoother scales the filter input so that the AM codewords being filtered effectively correspond to a unified and smooth AM-AM curve regardless of impedance modulation (Fig. 7.5); the post-smoother then re-maps the raw filter output based on the impedance setting. In our design, the scaling factor (A in Fig. 7.6) is chosen to be 2 and is conveniently implemented as a binary shift operation.

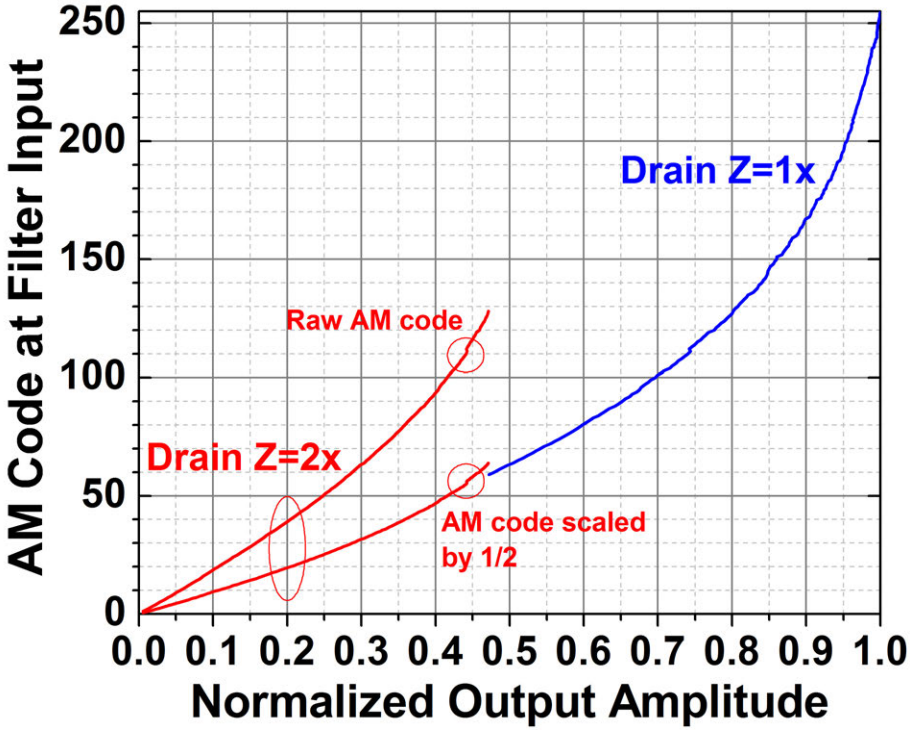


Figure 7.5: The amplitude discontinuity with and without pre-scaling.

7.9 Filtering on the Phase Path

On the phase path, the filter input transition is smooth enough even during impedance switching and no additional smoother is required. Digital filtering on the phase path is different from the amplitude path also in that the filtering cannot directly operate on the raw phase values since the filter cannot wrap/unwrap phase over the $0/2\pi$ boundary. The phase input is thus first mapped to Cartesian format, and these phase-I/Q signals are then filtered separately before being combined to feed the phase modulator (Fig 3.5).

7.10 Conclusion

Baseband digital filtering is fully integrated on both the amplitude and the phase path to knock down the spectral images due to the finite baseband input sample rate. Nyquist filter type is chosen to accurately relay the digital predistortion results to the down-sampled filter output, which helps to maintain signal integrity in the filter-last architecture. On the amplitude path, waveform pre- and post-smoother are embedded within the filter to improve the accuracy of the interpolated (filtered) output samples especially around impedance transitions. On the phase path, filtering is done by first splitting the phase signal into phase-I/Q and then having each separately going through a digital filter, and finally combining the

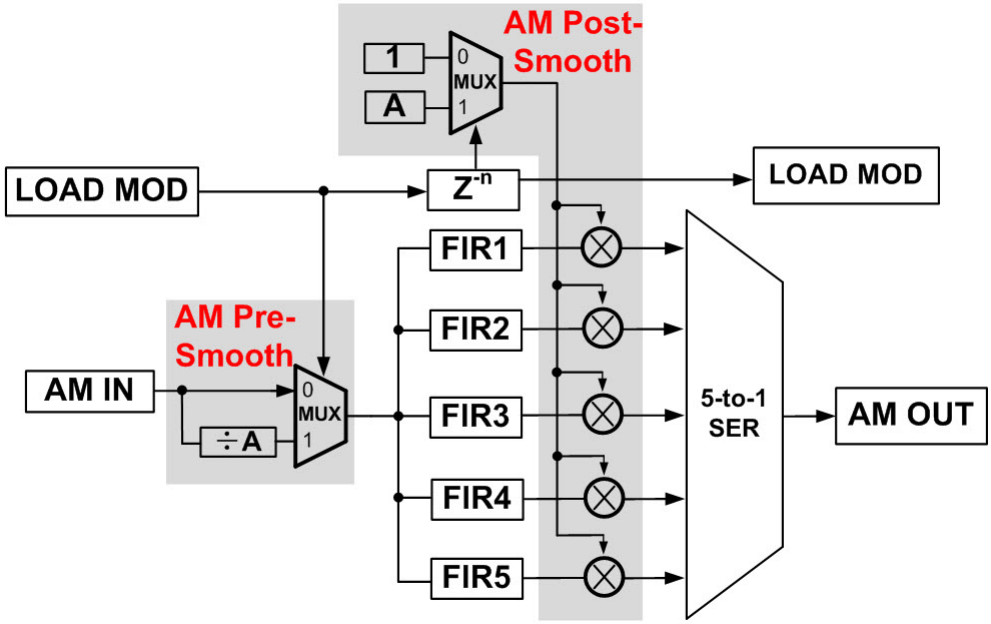


Figure 7.6: The amplitude filter with waveform smoother.

two into a single phase signal to feed to the phase modulator. This solves the problem that a linear digital filter cannot correctly wrap and un-wrap the phase values across the $0/2\pi$ boundary, although at the expense of increased power consumption for phase filtering due to the requirement of one more filter as compared to the amplitude path. Poly-phase decomposition technique can be used to have several sub-filters run in parallel at a much lower speed, thereby opening up the possibility for digital synthesis. The total number of Signed Power-of-Two (SPT) terms has been identified as a measure of filter complexity. The algorithm to find a filter with minimum number of SPT terms that meets the performance specifications has been discussed. Specifically, an SPT term assignment scheme is presented which gives intuitively satisfying results.

Chapter 8

Measurement Results

The design was fabricated in a 65nm digital bulk CMOS process without ultra-thick metal. The die measures 2.5mm × 2.5mm, and chip area is mainly limited by the 18-bit differential pads for the digital baseband (Fig. 8.1). The chip is wire-bonded to an FR-4 PCB and interfaces with the single-ended 50-ohm load without external balun or matching network. The PA runs off a separate 1.2V supply while the rest of the circuitry operates on 1V domains that are ultimately connected on-board.

8.1 Measurement Setup

In measurements (Fig. 8.2), a -10dBm low phase-noise sine-wave at twice the carrier frequency is generated externally, converted to differential through an on-board balun, and then fed onto the chip. The chip also takes a 1-GHz clock from a pulse generator, as well as 200MS/s baseband data from the FPGA. The RF output is directly routed to the spectrum analyzer for measurements. The spectrum analyzer, the sine-wave generator, the pulse generator, and the FPGA are frequency-locked to a common 10MHz reference. The RF cable loss has been calibrated out.

8.2 Continuous-Wave Test

First, the peak output power is swept with frequency (Fig. 8.3). The PA delivers a maximum P_{sat} of 23.3dBm with 43% drain efficiency and 38% PAE at 2.2GHz. Note that the results are achieved in a digital CMOS process without ultra-thick metal and under a 1.2V PA supply. The frequency low-tuning (as compared to the targeted 2.45GHz) is possibly due to the additional bond-wire inductance which was not fully accounted for at design time. All of the following measurements are performed at a 2.2GHz carrier. No frequency re-tuning is performed off-chip to adjust the center frequency.

Next, the AM-AM and AM-PM curves of the TX were measured by sweeping the amplitude codewords (Fig. 8.4). To deliver similar output power, the high-impedance case requires

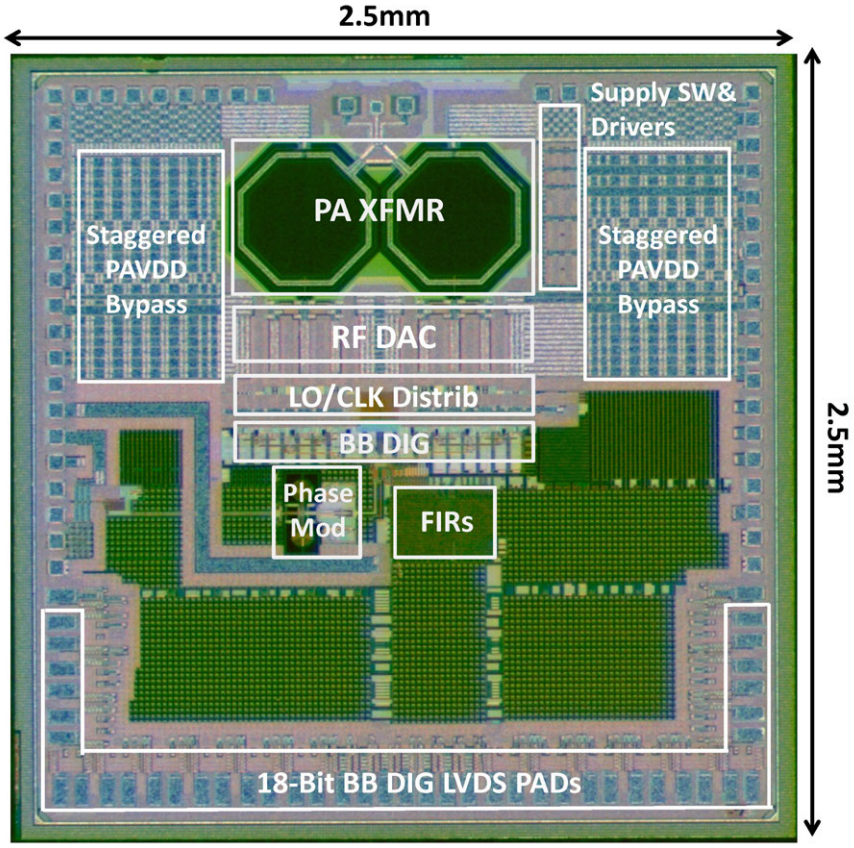


Figure 8.1: Die photograph of the prototype WLAN polar TX in 65nm CMOS.

codewords that are approximately twice as large as the low-impedance case, validating the pre-scaling factor for AM filter smoother. The peak AM-PM distortions are around 18° for both impedances.

Ideally, the drain voltage swings are similar between Psat with low impedance and 6-dB back-off with 2x impedance. For 2x impedance, the average output power level was therefore constrained within 6.5-dB back-off in modulated tests to keep the swing within reliability limit; the 0.5dB margin is to account for additional loss and/or higher than 2x impedance from the XFMR that may not be accurately modeled in simulations. As seen from Fig. 8.5, the boosted impedance offers a 40–60% relative improvement in efficiency.

Finally, the output phase was swept while holding the amplitude codewords constant (Fig. 8.6). The phase was measured by a sampling oscilloscope in terms of the relative delay in zero-crossing between the PA output and a stable continuous-wave reference. The phase modulator achieves 8.7-bit static phase resolution and consumes 9mW of power (Table. 6.1), which to our knowledge is the lowest reported power consumption for an integrated WLAN polar phase modulator. Although the codeword to phase linearity is generally good, we still

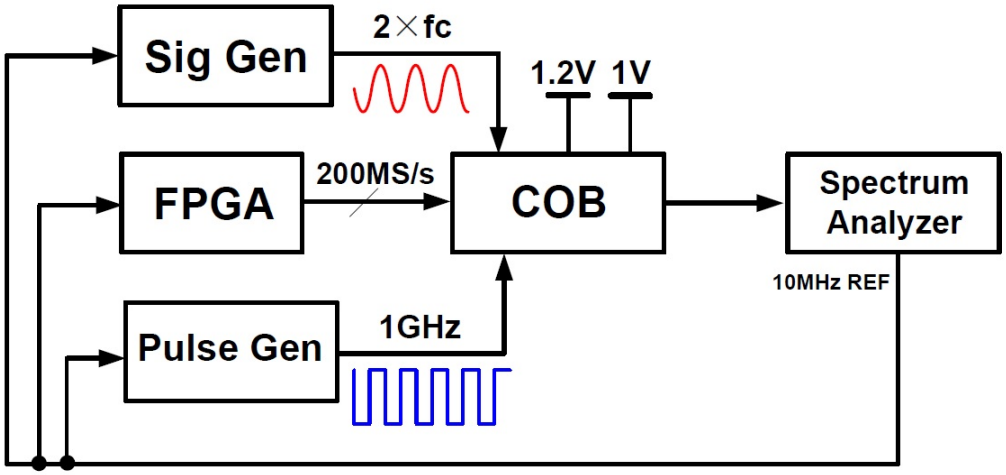


Figure 8.2: Measurement setup.

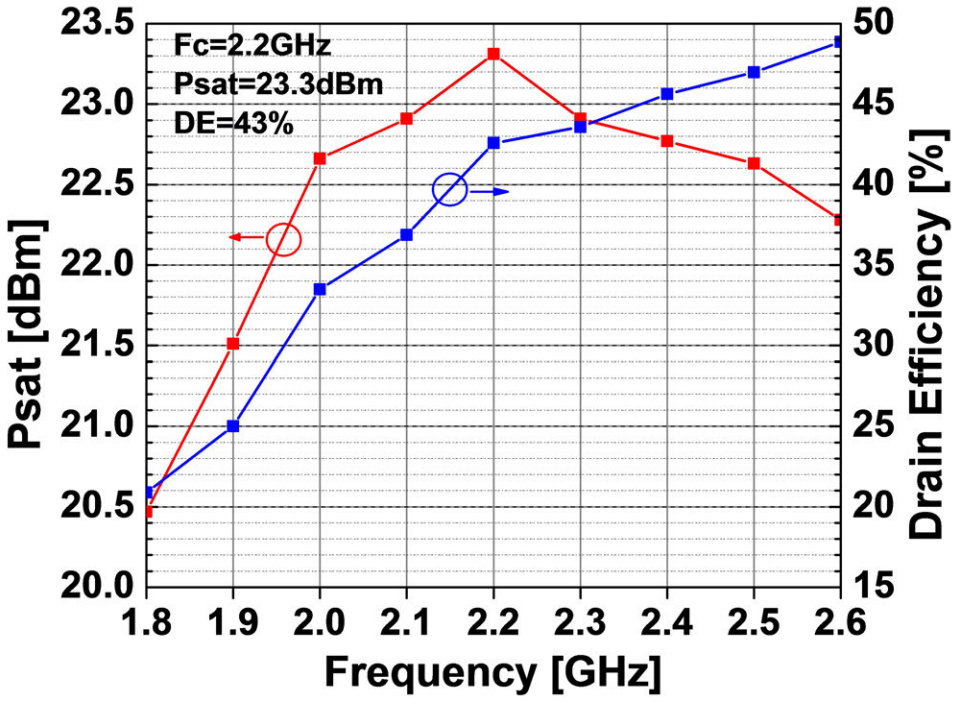


Figure 8.3: Measured P_{sat} and drain efficiency versus frequency.

implement the PM-PM pre-distortion in modulated tests to ensure that it does not limit performance. Measurements also showed negligible PM-AM distortions, enabling independent AM-AM, AM-PM and PM-PM pre-distortion.

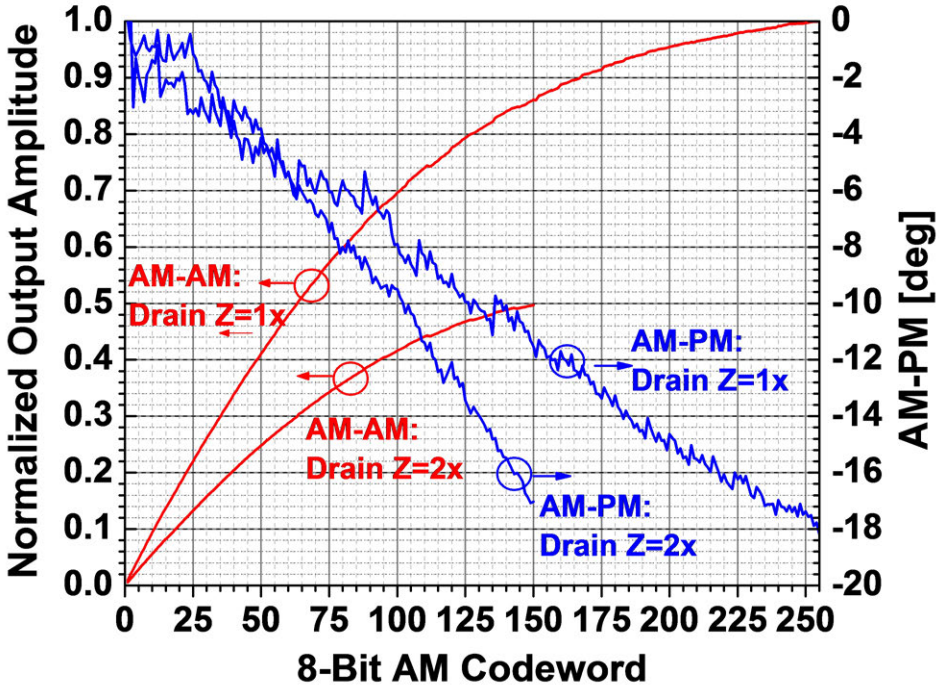


Figure 8.4: Measured AM-AM and AM-PM.

8.3 Modulated Signal Test

With independent LUTs for static AM-AM, AM-PM, and PM-PM predistortion, we tested the TX with a 802.11g 54-Mbps 64-QAM signal. No timing alignment between the amplitude and phase path was applied externally.

The close-in spectrum meets the mask with large margin (Fig. 8.7). Further out (Fig. 8.8), the -60dBr spurs at 200MHz offset are likely caused by ground coupling between the digital BB and RF; these can be reduced by decoupling the on-chip digital and RF grounds. There are hardly any other spurs above the noise floor within 1-GHz offset, proving the effectiveness of filtering. The noise floor is -125dBm/Hz at 200MHz offset, and is primarily limited by amplitude/phase quantization. Note that this spectrum was obtained without any explicit off-chip filtering.

Ideally, the out-of-band noise floor (at about 100MHz offset and above) injected into a nearby RX within another band has to be below thermal noise floor (-175dBm/Hz at 300K as calculated by Eq.(1.2)) to avoid any de-sensitization and hence allow multiple radios to co-exist (Section 3.2). With a modest isolation of 40dB from antenna-to-antenna and/or diplexers, the noise floor of -125dBm/Hz is still short by about 10dB. This issue can be mitigated by improving both the amplitude and phase resolution, where the large unit PA can be further reduced in size ([90]), and the DAC on the phase path can have more bits. In addition, the sample rate can be increased even further to lower noise spectral density;

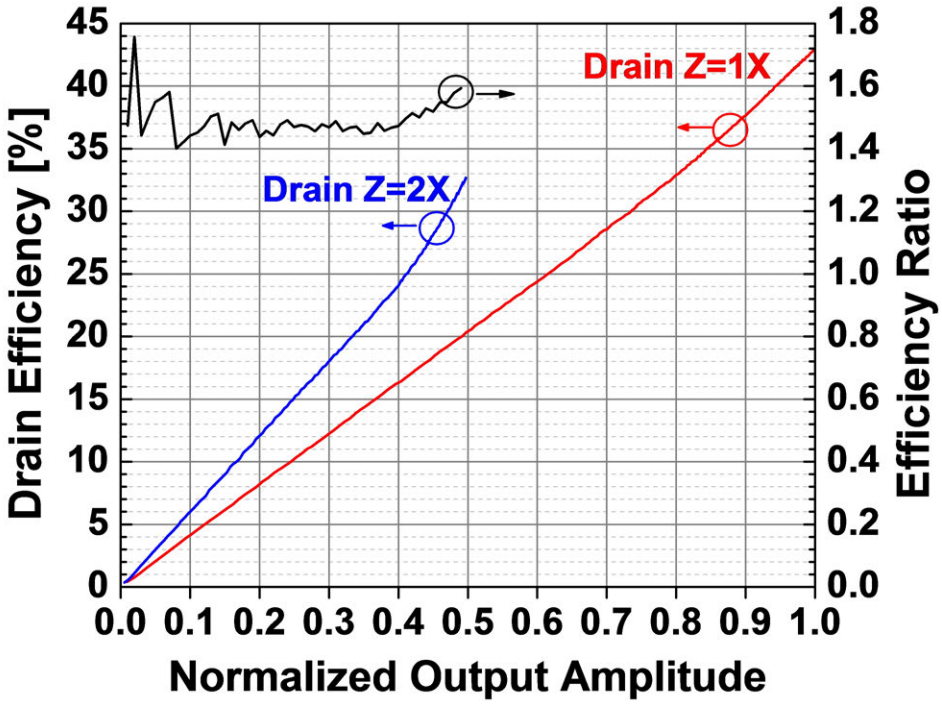


Figure 8.5: Measured efficient improvements with drain impedance modulation.

further technology scaling is likely to make this solution increasingly attractive in terms of power consumption.

At 1-GHz offset, -65dBr of images are measured, while in simulations they are around -55dBr. One possible reason for the discrepancy is the filtering from finite settling speed of phase path and PA-supply that is not fully captured by simulations; bond-wire and board parasitics might also contribute some additional filtering.

At -28dB EVM, the TX delivers 16.8dBm power with 24.5% drain efficiency, 21.8% PAE, and 19.3% system efficiency (Fig. 8.9). The entire TX consumes 247mW (Table 8.1) under the same condition.

8.4 Comparison with State-of-Art

Table 8.2 compares our prototype with the state-of-the-art. While an exact comparison is difficult due to the many variations in the level of integration, PA supply voltage, metal thicknesses, process and etc., we have attempted to normalize the results by including the following factors for designs that are not fully integrated: 1dB loss for external balun/matching network, and 85% efficiency for DC-DC converter (for two or more PA supplies). We believe these values to be fair estimates for on-chip CMOS realizations. With the highest level of integration, this prototype demonstrates a combination of good power, spectral purity, and

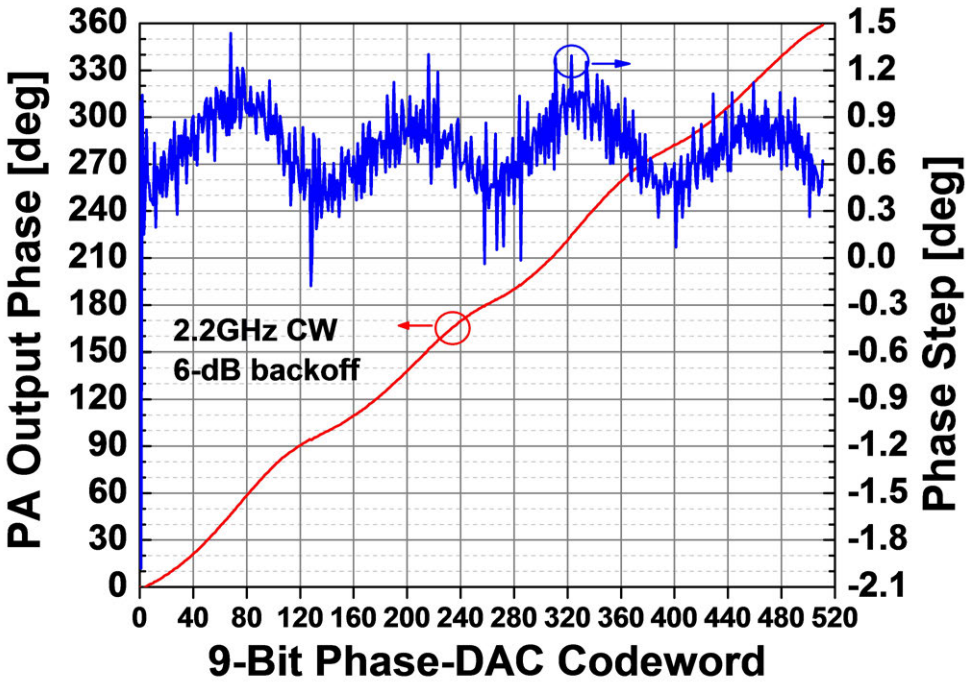


Figure 8.6: Measured phase path response (PM-PM).

Table 8.1: TX power breakdown for WLAN 802.11g 54Mbps

TX Block	**Power Consumption [mW]**
PA output stage	195
PM-LO distribution	25
Phase modulator	9
FIR (phase)	8
FIR (amplitude)	3.5
Other digital baseband	6.5
TX total	247
WLAN OFDM P_{out}	16.8dBm
PA drain efficiency	24.5%
PA PAE	21.8%
TX system efficiency	19.3%

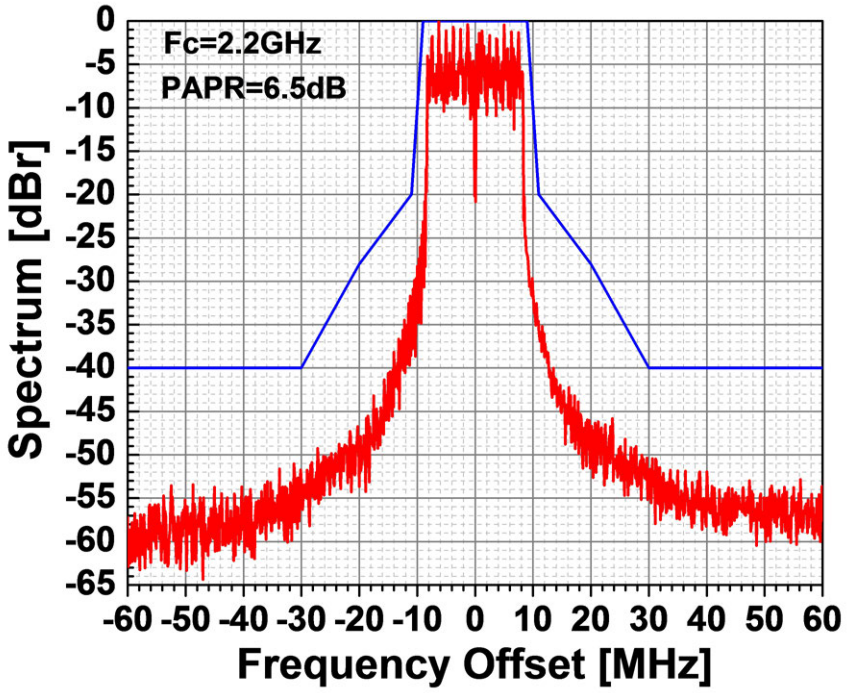


Figure 8.7: WLAN 802.11g 54Mbps: measured close-in spectrum.

overall efficiency under a highly-constrained PA supply.

8.5 Conclusion

We have implemented a prototype of the digitally-modulated polar transmitter for IEEE 802.11g in a 65nm bulk CMOS technology without ultra-thick metal. The transmitter delivers a peak power of 23.3dBm at 2.2GHz with 43% drain efficiency and 38% PAE, all from 1.2V power supply. The efficiency enhancement from the boosted drain impedance is 40–60% relatively, at power levels lower than 6.5dB backoff. Static digital predistortion helps the TX to achieve -28dB EVM at 16.8dBm OFDM power, with 24.5% drain efficiency, 21.8% PAE, and 19.3% system efficiency for the 802.11g 54Mbps application. The transmit noise floor is -125dBm/Hz at 200MHz offset. The entire TX consumes 247mW under the same condition. Comparing with state-of-the-art, our prototype has demonstrated a combination of good transmit power, spectral purity, and system efficiency with the highest level of integration. At the same time, we have identified the out-of-band emissions as one of the bottlenecks for the actual commercialization of this transmitter architecture.

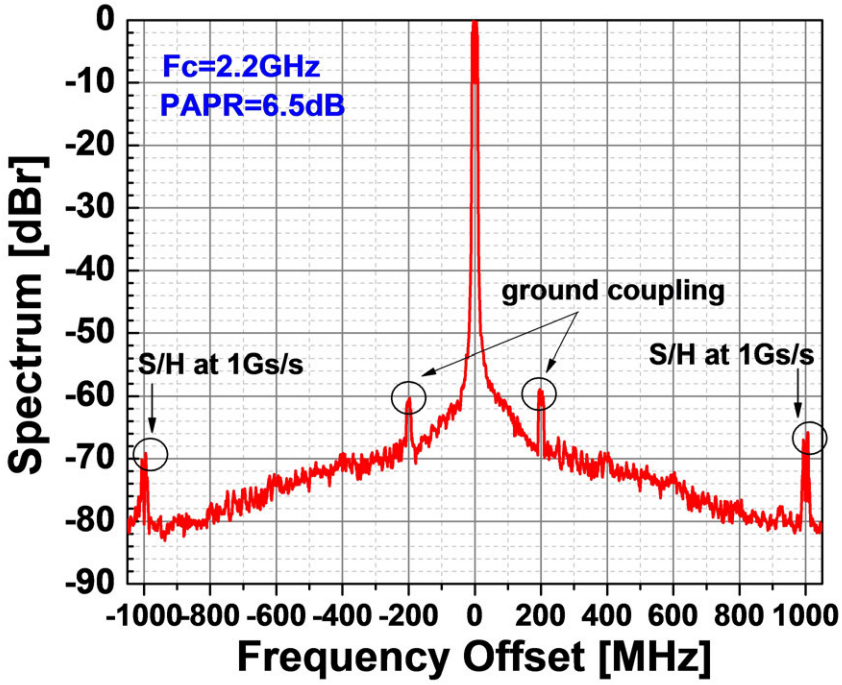


Figure 8.8: WLAN 802.11g 54Mbps: measured far-out spectrum.

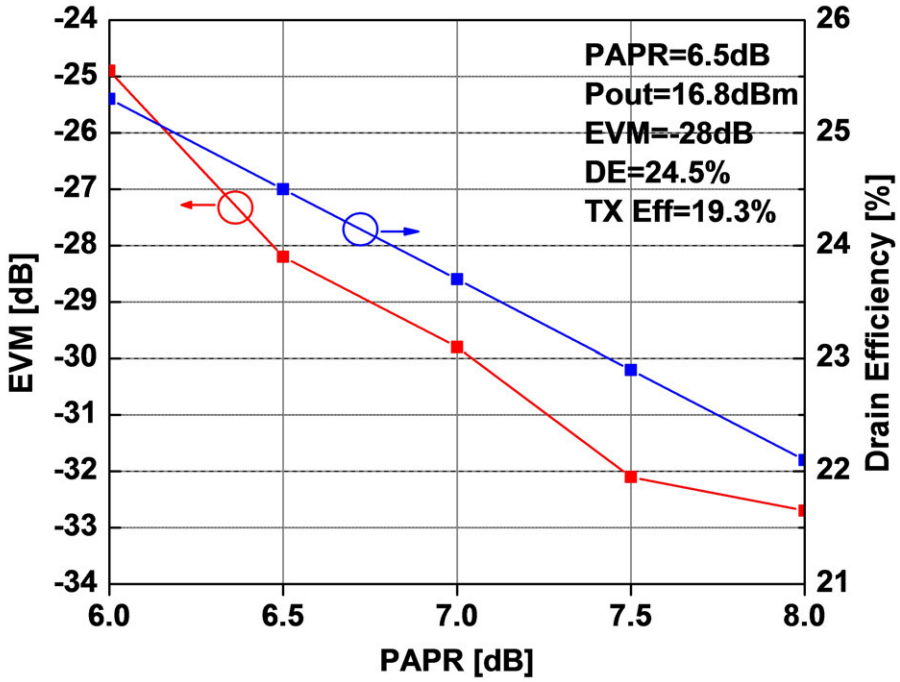


Figure 8.9: WLAN 802.11g 54Mbps: measured EVM and efficiency versus PAPR.

Table 8.2: Comparison with state-of-the-art

Reference	**[42]**	**[91]**	**[92]**	**[93]**	**This Work**
Architecture	Switched-Capacitor Digital PA	Outphasing Digital TX	Uneven Doherty Analog PA	Asymmetric Multilevel Outphasing PA	**Digital Polar TX**
Ultra-Thick Metal	Yes	Yes	No	Yes	**No**
PA Supply [V]	3.0/1.5	2.05	2.0	0.85/1.35/ 1.8/2.5	**1.2**
WLAN EVM [dB]	-32	-25	-25	-31.4	**-28**
WLAN Pout [dBm]	17.7	20.0	20.2	20.2	**16.8**
PA PAE [%]	27	22	24.7	27.6	**21.8**
WLAN Pout [1] [dBm]	16.7	19.0	20.2	18.5	**16.8**
PA PAE [1][%]	21.4	17.5	24.7	18.7	21.8
Noise floor @200MHz OS [dBm/Hz]	-103	-110	N.A.	-102	-125
On-chip TX chain	N.A.	Phase modulator	N.A.	N.A.	**Phase modulator, BB filters**
TX chain power [2][mW]	N.A.	82	N.A.	N.A.	26

[1] Includes 1dB loss for external balun / matching network, and 85% efficiency for DC-DC converters for multiple PA supplies.

[2] Exclude PA and its driver stages.

Chapter 9

Conclusion

9.1 Thesis Summary

The explosive growth in the wireless communication market for the last decade has led to the consumer demands for low-cost, small-form-factor and power-efficient mobile devices featuring versatile communication capabilities. A high-level integration of the wireless RF front-ends into the cost-efficient CMOS VLSI technology is therefore one of the long-term visions for the mobile industry. On the other hand, high data-rate and spectrally efficient modulation schemes have continued to evolve as a result of a relentless demand for higher throughputs despite of an increasingly crowded spectrum. Fully-integrated and back-off-efficient CMOS transmitters are therefore a key requirement for the battery-operated mobile terminals. Furthermore, the ubiquitous availability of cellular, WLAN, Bluetooth, GPS, FM and etc from a single mobile product has put stringent coexistence requirements on each individual radio. Trading out-of-band spectral purity for good in-band performances is no longer acceptable in a co-existence scenario.

This thesis therefore investigates the design and analysis of a fully-integrated, back-off-efficient and co-existence-friendly CMOS power transmitter system, with a special emphasis on the digitally-modulated polar architecture which the author thinks is among the promising solutions to the above key challenges facing the wireless industry.

A brief survey of the PA efficiency enhancement techniques has identified a dynamically-varying impedance technique in the context of the direct digital modulation scheme as one effective measure of improving efficiency. To build a complete TX system to wrap these two techniques, extensive behavior-level simulations involving an ideal digital transmitter are first carried out, to help understand the interactions between the various blocks in such a complex system; we have also relied on the system-level simulations as a vehicle to budget such performance specifications as resolution, sample rate and peak-to-average-power-ratio. At the core of the transmitter, an RF switching PA is designed for high efficiency with a simplified harmonic tuning methodology. With the design of a low-loss transformer power combiner, the PA devices can be properly configured as part of the impedance modulation

scheme. Since the phase path is historically power hungry for a polar transmitter, we have made an effort to achieve wideband phase modulation with good power efficiency by employing an open-loop phase interpolator architecture. The open-loop, high-bandwidth analog/RF topology on the phase path also helps to reduce the total path delay, and hence relax the delay matching concerns between the amplitude and phase path under process, temperature and voltage variations. For baseband digital filters that knock down the close-in spectral images, the interactions between the nonlinear predistortion and the linear filtering have to be taken into account to preserve signal integrity.

Measurement results on a 65nm-CMOS prototype showed that it has achieved a combination of decent output power, good efficiency and reasonable spectral purity. However, the out-of-band spectrum is still not clean enough for radio co-existence, which suggests some future directions for the follow-up work, which are discussed below.

9.2 Future Directions

Although our mixed-signal power transmitter has demonstrated good performances, the out-of-band transmit spectrum is still not "clean" enough in a radio coexistence scenario. Specifically, the noise floor as limited by the digital quantization is not low enough. To make it worse, there are spurs higher than the noise floor by 20–30dB as a result of the sample-and-hold operation at the digital/RF-DAC interface. An investigation on the wideband spur canceling techniques, as well as the trade-offs between a low quantization noise floor versus baseband/RF power penalty, would be a natural extension of this work. A power-efficient baseband architecture that is able to dynamically relocate the spurs to some other frequency bands where the co-existence requirements can be somewhat relaxed is an interesting research problem; in this case, a dynamically varying frequency plan, according to the instantaneous user scenario, would be required. That generally requires a wideband and fast-switchable LO generation scheme.

Moreover, it would be worthwhile to explore the possibility of a wideband RF-FPGA architecture based upon the core RF-DAC in this work. In such an RF-FPGA, a versatile DSP module can process the digital baseband signals according to the requirements of different communication standards, while efficient power amplification is realized by the RF-DAC. In this way, a single transmitter core is able to support multiple communication standards, thereby achieving a truly software defined radio.

Also, the digital predistortion is performed manually in this work by first characterizing the AM-AM, AM-PM and PM-PM characteristics of the TX in the CW mode, and then building and applying the look-up-tables through the external FPGA. It would be ideal to be able to couple the transmitted signal back to the receiver on the same chip and accomplish the predistortion in a self-calibrated fashion. Unlike a manual implementation, the self-calibrated digital predistortion can occur much more frequently to track any dynamics of the antenna impedance changes, the die temperature drift, and the supply voltage drop due to battery aging. By this means, the predistortion would be able to correct for the

dynamically changing (although still much slower than the modulation rate) characteristics of the TX, and therefore potentially achieve better linearity which may have an impact on the actual throughput available from the mobile devices.

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