Title
AC vs. DC Boost Converters: A Detailed Conduction Loss Comparison

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AC vs. DC Boost Converters: A Detailed Conduction Loss Comparison

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Motivation

Background

- DC power distribution has the potential for efficiency savings, improved power quality, ease of islanding, reduced costs, and combined data/power
- US Department of Energy focuses on quantifiable efficiency comparison
- Numerous studies compare efficiency of AC and DC buildings
- Most loss occurs at the load input converters

Gaps in Prior Research

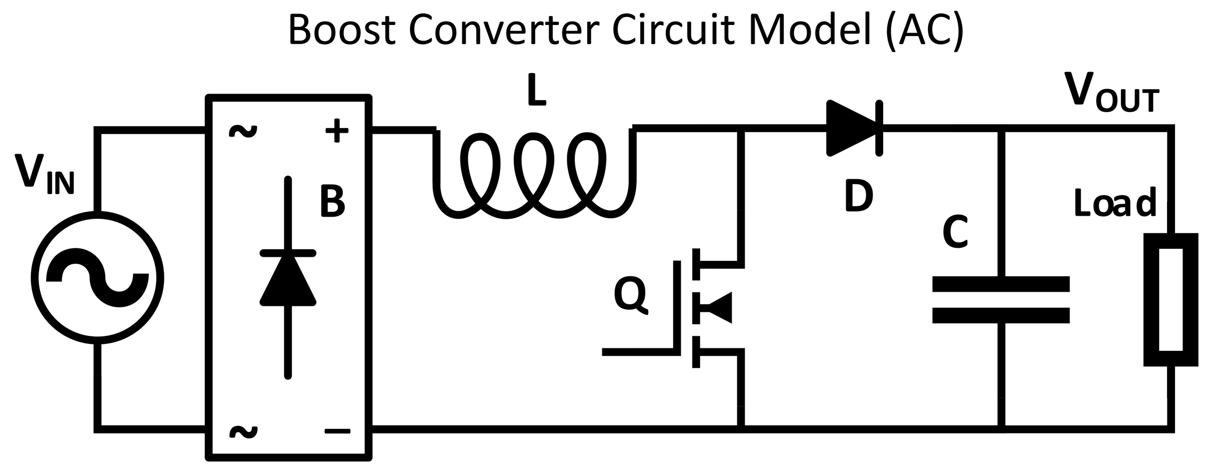
- In all prior research, converter efficiency is based on product data. It is hard to compare AC and DC converters using product data because:
  - Requires a lot of data, which is often unavailable
  - Products only use standard inputs such as 120 V AC or 48 V DC. High-voltage converters are often more efficient regardless of AC or DC
  - Different products use different components with different parasitics

Project Goal

- Develop a detailed loss model of a boost converter
- Compare AC/DC PFC boost and DC/DC boost converter with the same voltage and same components

Deriving the Conduction Loss Model

Boost Converter Circuit Model (AC)



How to find converter loss?

- Determine steady state currents in each component
- For resistive loss elements:

$$P_{Loss,R} = R_R * I_{rms}^2$$

- For diode loss elements:

$$P_{Loss,D} = V_D * I_{ave} + R_D * I_{rms}^2$$

- R_R , R_D , and V_D from component datasheet

Resistive loss element currents

- Inductor (L): $I_{L,rms}$
- Switch (Q): $I_{Q,rms}$
- Capacitor (C): $I_{C,rms}$

Diode loss element currents

- Bridge Diode (B): $I_{B,rms}, I_{B,avg}$
- Boost Diode (D): $I_{D,rms}, I_{D,avg}$

Model assumptions

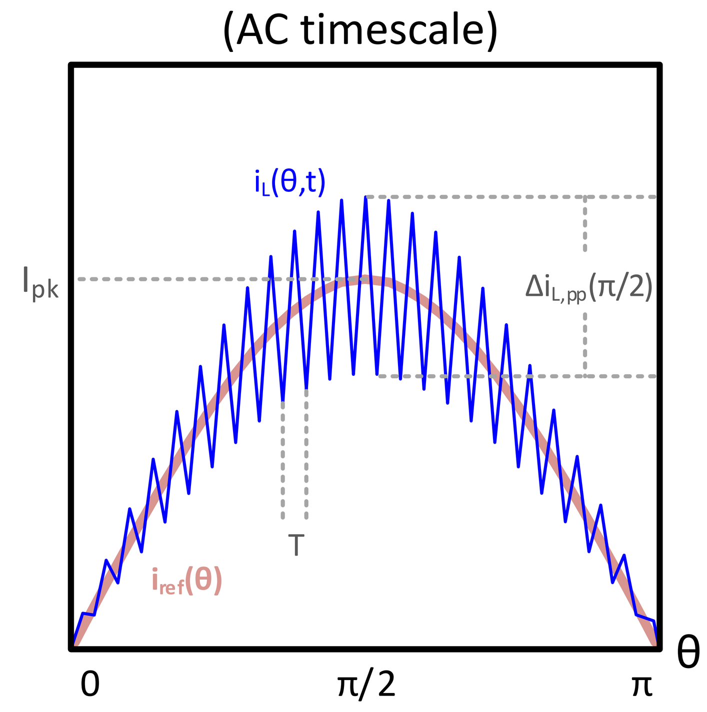
- Continuous conduction mode
- Unity power factor
- No output voltage ripple
- 100% efficiency for determining currents
- No switching and gate-drive losses... for now

How to find component currents?

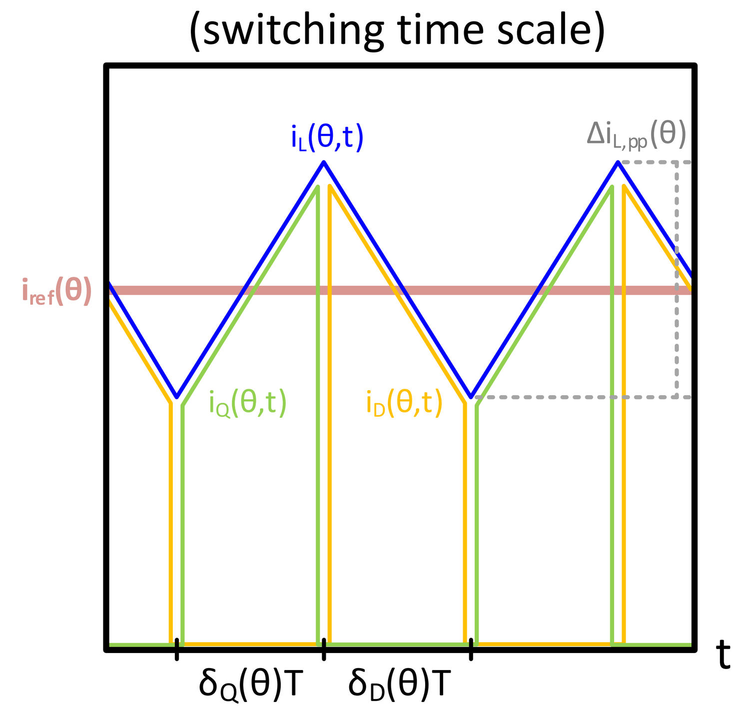
- Take RMS or AVG for two timescales:
  - Switching frequency (i.e. 65 kHz)
  - AC 60 Hz time scale (not necessary for DC-DC boost)
- On the switching timescale, every current can be represented by either:
  - A bilateral triangle (inductor, bridge)
  - An elevated right triangle (switch, boost diode, capacitor)
- Use orthogonality to combine waveforms of different frequency:

$$I_{L,rms} = \sqrt{I_{ref,rms}^2 + \Delta I_{L,rms}^2}$$

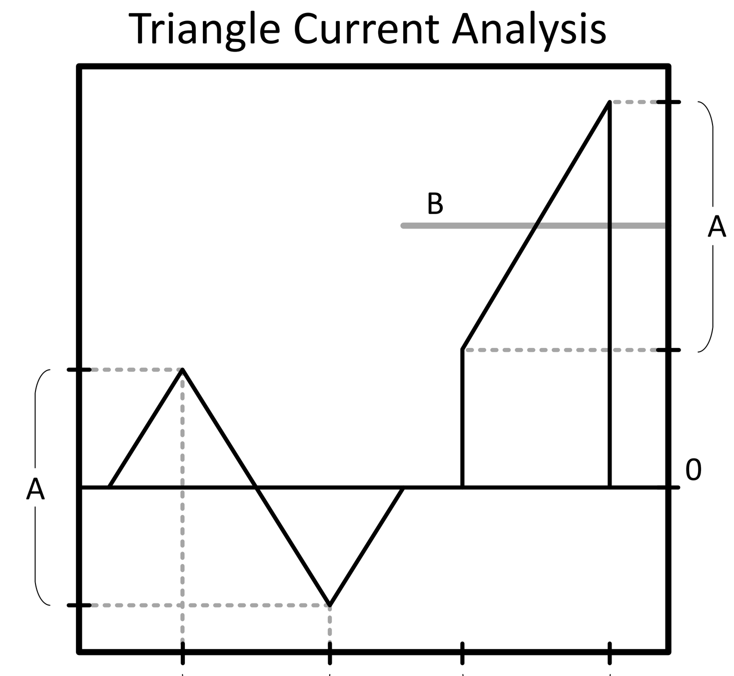
Inductor Current (AC timescale)



Component Currents (switching time scale)



Triangle Current Analysis



Component Currents

Parameter	AC/DC PFC	DC/DC	min($P_{Loss,AC}/P_{Loss,DC}$)
$I_{L,rms}$ $I_{B,rms}$	$\frac{\sqrt{2}P_o}{V_{pk}}$	$\frac{P_o}{V_{pk}}$	2
$I_{B,avg}$	$\frac{4}{\pi}\frac{P_o}{V_{pk}}$	$--$	$--$
$I_{Q,rms}$	$\frac{P_o}{\sqrt{V_o}V_{pk}}\sqrt{2V_o - \frac{16}{3\pi}V_{pk}}$	$\frac{P_o}{\sqrt{V_o}V_{pk}}\sqrt{V_o - V_{pk}}$	2
$I_{D,rms}$	$\frac{4}{\sqrt{3\pi}}\frac{P_o}{\sqrt{V_o V_{pk}}}$	$\frac{P_o}{\sqrt{V_o V_{pk}}}$	$\frac{16}{3\pi} \approx 1.70$
$I_{D,avg}$	$\frac{P_o}{V_o}$	$\frac{P_o}{V_o}$	1
$I_{C,rms}$	$\frac{P_o}{V_o\sqrt{V_{pk}}}\sqrt{\frac{16}{3\pi}V_o - V_{pk}}$	$\frac{P_o}{V_o\sqrt{V_{pk}}}\sqrt{V_o - V_{pk}}$	$\frac{16}{3\pi} \approx 1.70$

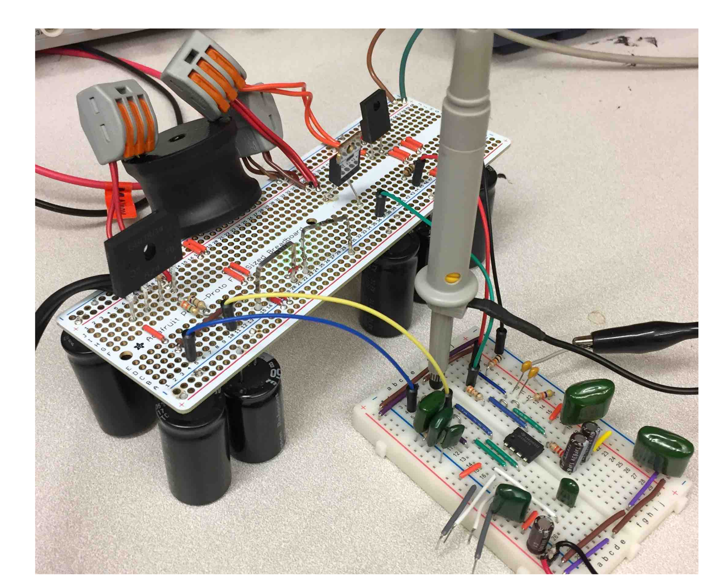
- Component current expressions for simple model (without ripple). Expressions for model with inductor current ripple are in the paper
- Currents are all in terms of output power P_O , output voltage V_O , and peak input voltage V_{pk} (= V_{in} for DC/DC)
- min($P_{Loss,AC}/P_{Loss,DC}$) is the theoretical smallest possible ratio of component loss between the AC/DC boost and DC/DC boost

Simulation, Experiment, and Results

Validation of AC/DC PFC Boost
P_O = 250 W, V_O = 350 V, V_{pk} = 170 V

Parameter	Model (simple)	Model (ripple)	Simulation	Experiment
$I_{L,rms}$ $I_{B,rms}$	2.153	2.161	2.162	2.356
$I_{B,avg}$	1.938	1.938	1.938	2.105
$I_{Q,rms}$	1.655	1.662	1.662	1.723
$I_{D,rms}$	1.376	1.381	1.382	1.323
$I_{D,avg}$	0.733	0.733	0.733	0.781
$I_{C,rms}$	1.165	1.171	1.171	$--$

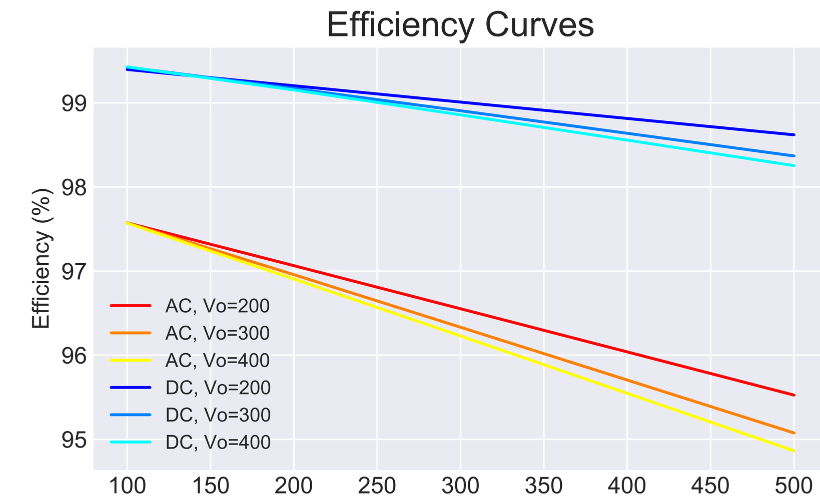
Experimental Validation Setup



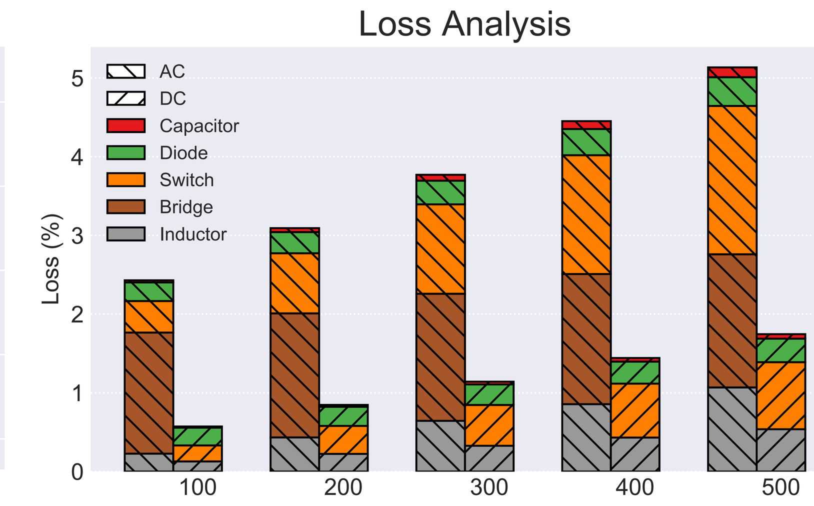
- Model is validated through PSIM simulation and experiment
- Experiment has parasitic wire runs that cause oscillations and increase input current; this will be improved in future work

- Parametric model runs with V_O = 200-400 V and P_O = 100-500 W
- In this range, AC/DC boost has 2.9 to 4.2 times the loss of DC/DC
- Loss analysis shown for V_{pk} = 170 V and V_O = 400 V

Efficiency Curves



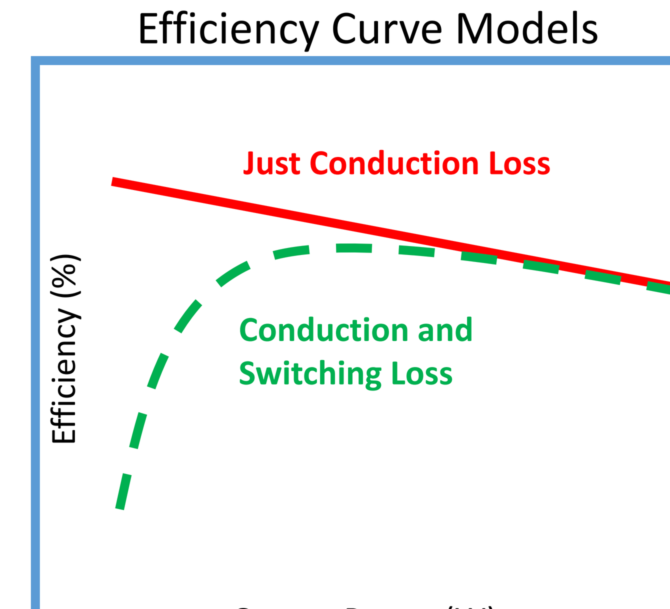
Loss Analysis



Future Work

1. Derive a switching loss model, which will curve at low power
2. Extend the model to an inverter and flyback. These should cover most types of converters in a building
3. Redo boost experiment with a PCB
4. Perform experimental validation for the inverter and flyback

Efficiency Curve Models



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