Title

Effective Schottky barrier lowering of Ni silicide/p-Si(100) using an ytterbium confinement structure for high performance n-type MOSFETs

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Effective Schottky barrier lowering of Ni silicide/p-Si(100) using an ytterbium confinement structure for high performance n-type MOSFETs

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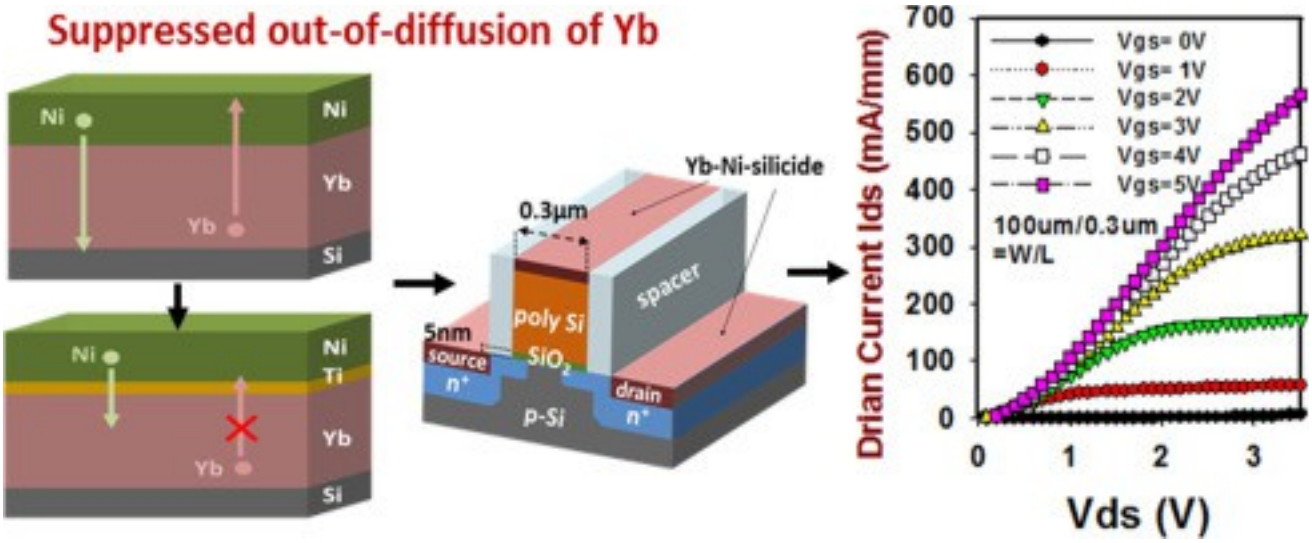
Highlights

- The insertion of Ti layer effectively suppresses Yb out-diffusion and prevents the Yb from oxidation during silicidation.
- Yb atoms are confined by the inserted Ti layer and react with both Ni and Si to form Yb-Ni silicide.
- The confinement leads the SBH of the system to a 0.02 and 0.025 eV lowering at 500 and 600 °C, respectively.
- The RE metal confinement structure provides a CMOS compatible approach for further SBH engineering and technology nodes.

Abstract

A simple but effective rare earth metal (RE) confinement structure is demonstrated to suppress surface accumulation of Yb generally encountered in the RE metal incorporated Ni silicide system. The confinement structure is realized by inserting a Ti diffusion barrier layer between Yb and Ni layers. Yb atoms can be constrained in a specified reaction region during silicidation as evidenced by Auger electron spectroscopy and cross-section transmission electron microscopy analysis. The RE metal confinement structure provides a complementary metal-oxide-semiconductor compatible approach for further Schottky barrierheight engineering and is a promising method for future technology nodes.

Graphical abstract



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Keywords

Schottky barrier
nMOSFET
NiSi
Yb confinement

1. Introduction

Silicides, owing to their low resistivity, good thermal and chemical stability, have been extensively used in the fabrication of conventional planar metal-oxide-semiconductor field effect transistors (MOSFETs), nanometer Fin FETs (FinFETs) or nanowire transistors [1], [2], [3], [4], [5], [6], [7]. Among various silicides, NiSi has a low resistivity of 15 μ Ω cm and less Si consumption during silicide formation [8]. NiSi is promising for ultrashallow junctions required in the present and future technology nodes [9], [10], [11], [12]. One drawback of use NiSi in source/drain (S/D) contacts is the high electron barrier to Si resulting in high contact resistance at NiSi/Si junction. In contrast, most rare earth (RE) metals, such as Yb and Er, can form low work function silicides and reduce the contact resistance [13], [14], [15], [16], [17]. However, RE-based silicides typically have higher resistivity than NiSi which restrains its applications to nano-scale complementary MOS (CMOS) technologies.

In order to circumvent this dilemma of achieving low contact resistance using RE metals while maintaining low resistivity of the bulk silicide, several approaches have been proposed recently [9], [18], [19], [20], [21], [22]. For instance, interfacial segregation of metal at NiSi has achieved the reduction of Schottky barrier height (SBH) by 0.1–0.15 eV with little sacrifice of sheet resistance [23]. Incorporating Yb into NiSi using Yb/Ni metal stack can reduce the silicide work function by about 0.15–0.38 eV [10], [23]. Although RE metals are effective for SBH reduction, it has been revealed that incorporated RE metals are easily piled up at silicide surface with only a small amount remaining at the silicide/Si interface [9], [10], [23]. This phenomenon would severely diminish the efficiency of SBH lowering. Consequently, a method for RE metal confinement in a specified reaction region for silicide formation is a key to further reduce the parasitic resistance and boost device performance.

2. Materials and experimental aspects

To investigate the effectiveness of Yb confinement structure, p-type boron-doped Si (100) substrates with resistivities ranging from 1 to 30 Ω cm were used. There are mainly three metal structures for silicide formation for the present study (Fig. 1): pure Ni (30 nm) on Si [Fig. 1(a)], Yb(30 nm)/Ni(20 nm) on Si (Yb deposited first) [Fig. 1(b)] and Yb(40 nm)/Ti(10 nm)/Ni(20 nm) on Si [Fig. 1(c)]. The metal stacks were deposited by an electron beam evaporation system. Silicidation was carried out by using rapid thermal annealing (RTA) in N_2 ambient. The annealing temperatures are ranging from 400 °C to 850 °C, and the annealing time is from 15 s to 90 s. After silicidation, the unreacted metal was selectively removed by wet etching using H_2SO_4:H_2O_2 solution at 120 °C. The sheet resistance (Rs) of the silicide film was measured by a 4 point probe. For material analysis, atomic depth profile was evaluated by Auger electron spectroscopy (AES); layer structures of the silicide were observed by cross-sectional transmission electron microscopy (TEM); energy dispersive X-ray spectrometer (EDS) was used to determine the atomic compositions of the silicides.

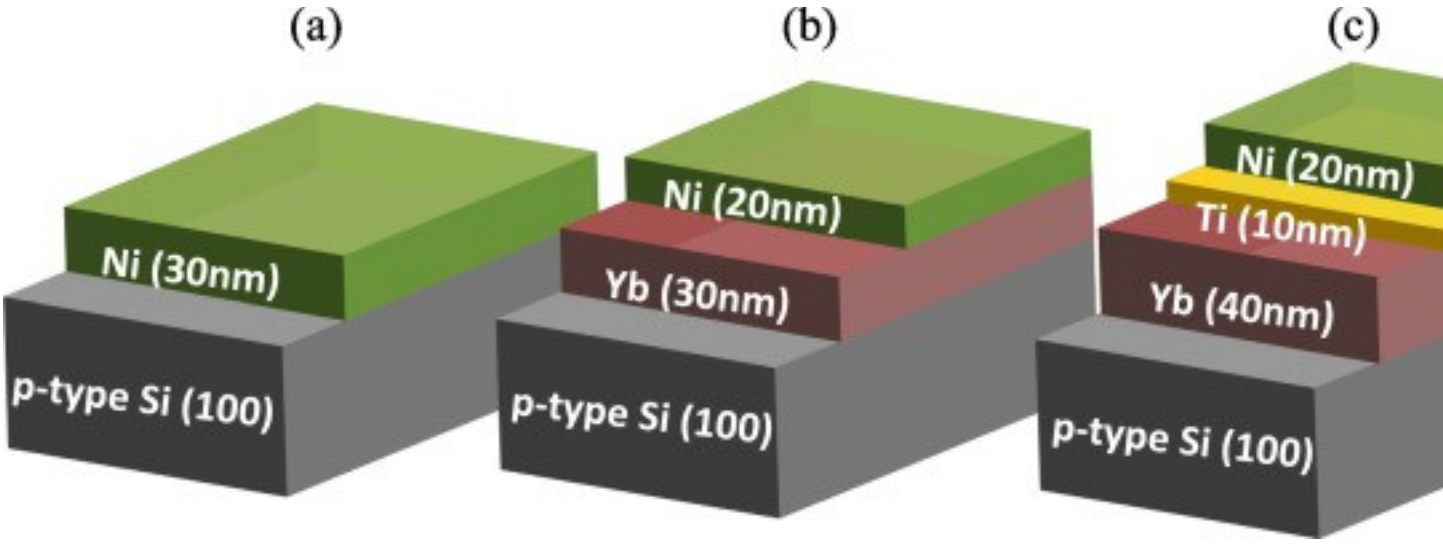

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Fig. 1. Metal structures for silicide formation: (a) pure Ni (30 nm) on Si, (b) Yb (30 nm)/Ni(20 nm) on Si (Yb deposited first), and (c) Yb(40 nm)/Ti(10 nm)/Ni(20 nm) on Si.

As for device applications, Schottky barrier diodes and nMOSFETs were fabricated on the p-type Si substrates. The diodes are circular in shape with diameter of 100 μm. The nMOSFETs has gate length of 0.3 μm. The gate stack comprises of poly-Si/SiO_2 which was grown by low pressure chemical vapor deposition (LPCVD). The gate oxide thickness is 5 nm. The proposed Yb/Ti/Ni structure was deposited sequentially after gate formation. The silicidation was carried out at 500 °C for 15 s to form source/drain contacts of the MOSFETs. HP 4156C semiconductor parameter measurement system was used for electrical characterization to evaluate the performance of the devices.

3. Results and discussion

Fig. 2 shows the AES depth profiles of the structures and the corresponding schematic representations of atomic diffusion. All the samples for AES analysis did not undergo step of removing unreacted metal prior to the probing for better understanding of metal reactions just after thermal annealing. In Fig. 2 (a), without Ti diffusion barrier, surface accumulation of Yb atoms in the Yb/Ni structure after annealing can be observed. Ni atoms diffused through Yb layer and reacted directly with Si beneath to form Ni silicide. This was accompanied with the expulsion of Yb atoms initially below the Ni layer and the formation of Yb depleted region. Rare-earth metal is easily oxidized when exposed

to air. Without Ti diffusion barrier in Ni/Yb stack, Yb atoms tend to be out-diffused into the upper surface which will cause Yb from oxidation during annealing.

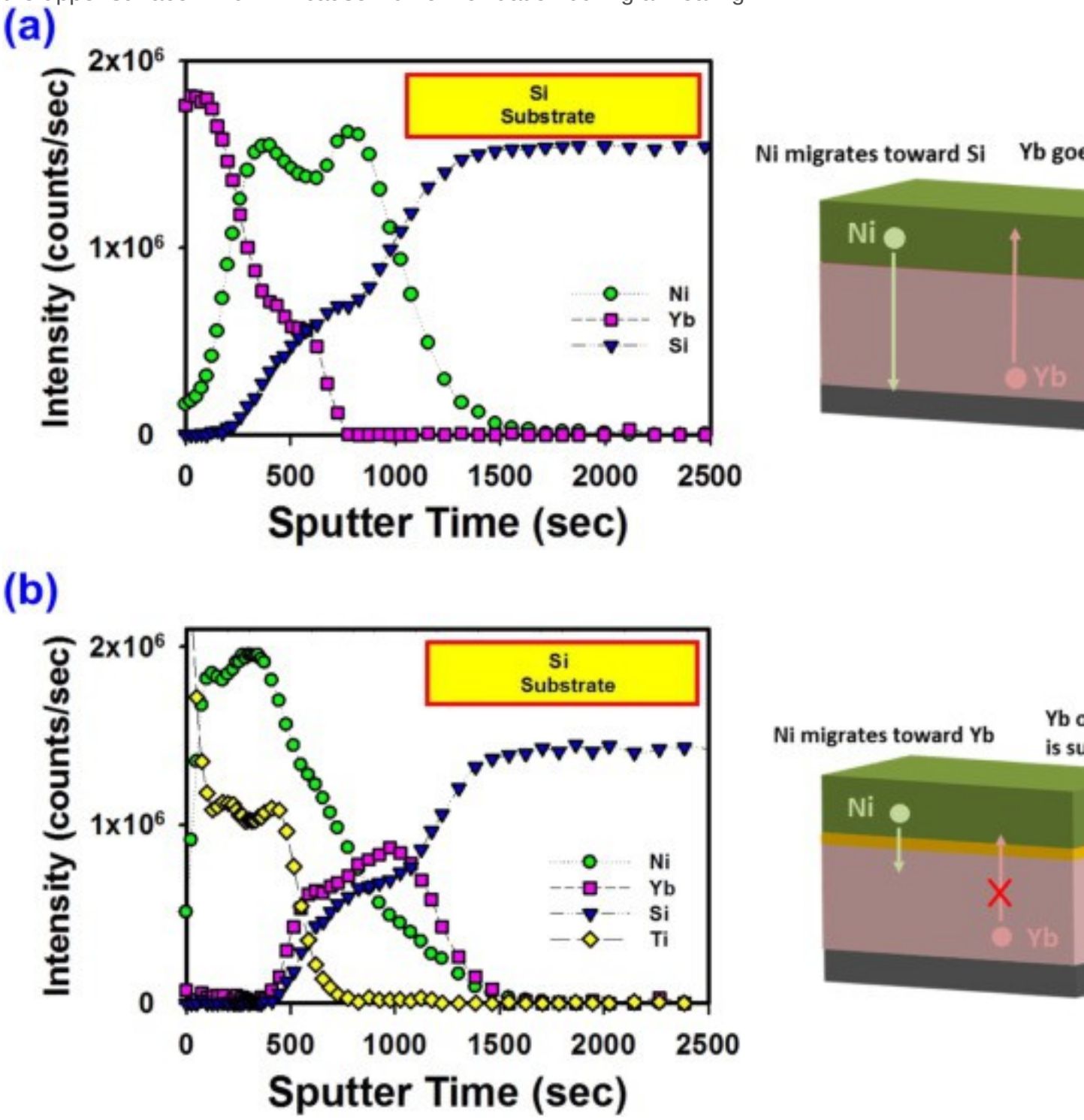

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Fig. 2. Auger electron spectroscopy depth profiles of the (a) Yb/Ni and (b) Yb/Ti/Ni structures after annealing at 400 °C for 15 s. The schematic representations of atomic ec diffusion are shown correspondingly.

Surface accumulation of Yb atoms can be suppressed by the insertion of a Ti diffusion barrier between Yb and Ni layers. In Fig. 2 (b), the supply of Ni was diminished and the Yb out-diffusion was retarded due to the inserted Ti diffusion barrier. Yb atoms were confined and reacted with both Ni and Si to form Yb-Ni silicide. As a result, Ti diffusion barrier is effective to suppress Yb out-diffusion and prevents Yb from surface accumulation. Moreover, the Ti layer also acts as the protecting layer that prevents the Yb from oxidation during annealing.

Fig. 3 is a comparison of sheet resistance (Rs) of the three silicide structures. Pure Ni structure has the lowest Rs in the whole temperature range. In addition, there is an increase of Rs starting around 600 °C which indicates the agglomeration of low resistivity NiSi phase and transformation to high resistivity $NiSi_2$ phase which usually occurs above 750 °C. For Yb/Ti/Ni structure, Yb-Ni silicide was formed and it has higher but near constant value of Rs between 500 °C to 750 °C. Yb/Ni structure, however, follows the same trend of Rs increasing around 600 °C as in the case of pure Ni structure. This is possibly due to the dual silicide structure with Ni-Ti silicide and Yb-Ni silicide formed as the upper and lower layers, respectively. Ni silicide exhibits normal Rs characteristics with annealing temperature and Yb-Ni silicide layer is responsible for a higher overall Rs values.

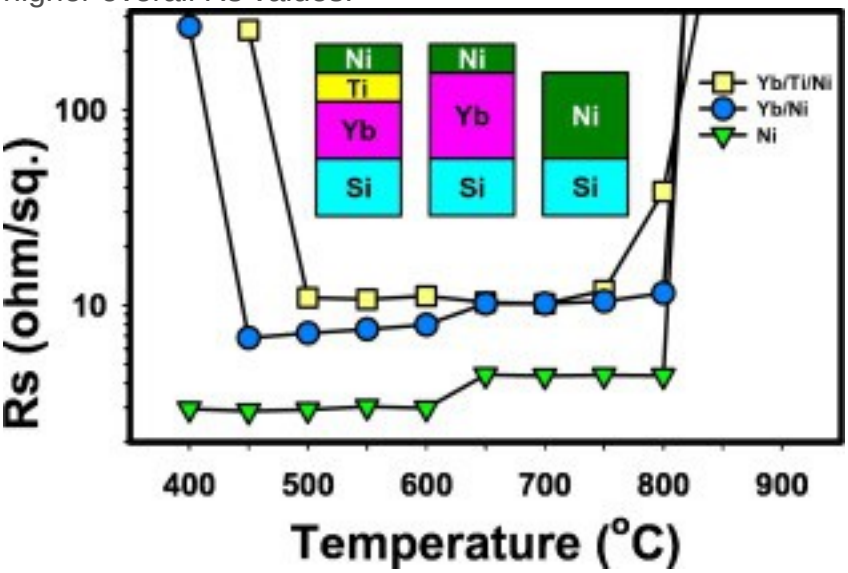

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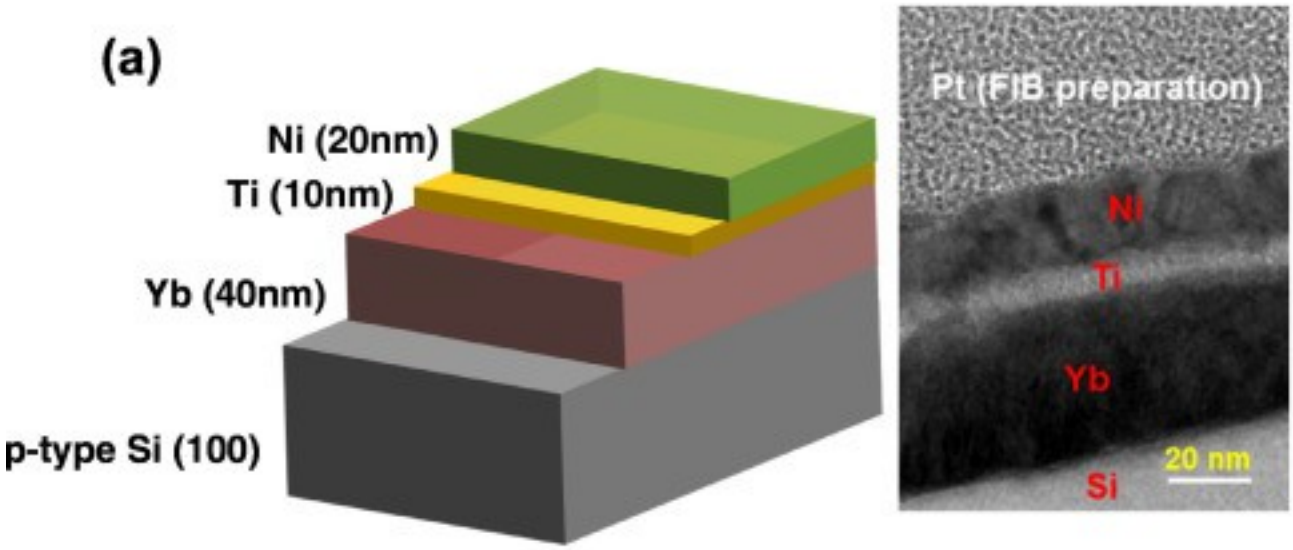
Fig. 3. Sheet resistance of the Ni, Yb/Ni and Yb/Ti/Ni structures after annealing at different temperatures for 15 s.

Fig. 4 are TEM images of the Yb/Ti/Ni structure before [Fig. 4(a)] and after silicidation [Fig. 4(b) and (c)]. In Fig. 4. (b), the upper (light in color) and the lower (dark in color) metal silicides are consisting of Ti-Ni-Si and Yb-Ni-Si intermetallic compounds, respectively. The upper layer was identified to be $Ni_4Ti_4Si_7$ phase and the lower layer was determined to be $YbNiSi_2$ phase from the analysis of atomic resolution images. The lower Yb-Ni silicide has two lamellas, each is polycrystalline with grains extended in direction parallel to Si surface. By EDS analysis, the grains were identified with atomic ratio of 20:32:48 (Yb:Ni:Si) for the upper lamella and 20:26:54 (Yb:Ni:Si) for the lower lamella. The grains in the Yb-Ni silicide layer tend to merge together by increasing the annealing time to 90 s [Fig. 4 (c)]. In this case, the atomic composition of the Yb-Ni silicide keeps near a constant ratio of 20:26:54 (Yb:Ni:Si) along direction perpendicular to the Si surface. Atomic resolution images associated with Fig. 4(b) and (c) indicate that all these phases are of structure based on NiSi. A simple calculation confirms that the atomic fractions of Yb, Ti and Ni are consistent with the deposited Yb(40 nm)/Ti(10 nm)/Ni(20 nm) layers on Si.

Before annealing



After annealing

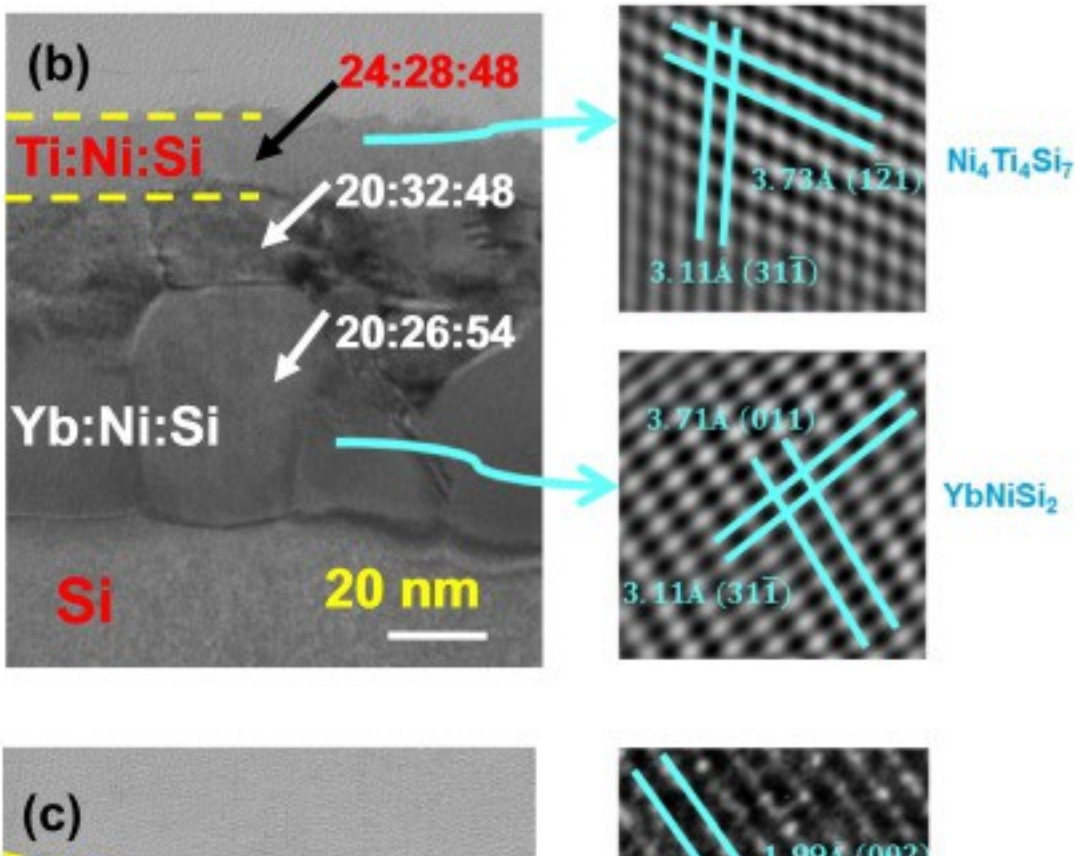


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Fig. 4. TEM images of the Yb/Ti/Ni structures (a) before and (b, c) after annealing at 500 °C for (b) 15 s and (c) 90 s. The schematic illustration of the Yb/Ti/Ni structures before annealing is shown in (a). Atomic ratio determined by EDS analysis are also shown in (b, c).

Fig. 5 (a) is a comparison of I–V characteristics of the p-type diodes. The inset shows the schematic illustrations of the diodes. The reverse current of Yb-Ni-silicide diode is lower than that of Ni-silicide diode. This implies that a higher barrier for hole, or equivalently a lower barrier for electron is formed in the Yb-Ni-silicide diode using Yb/Ti/Ni structure.

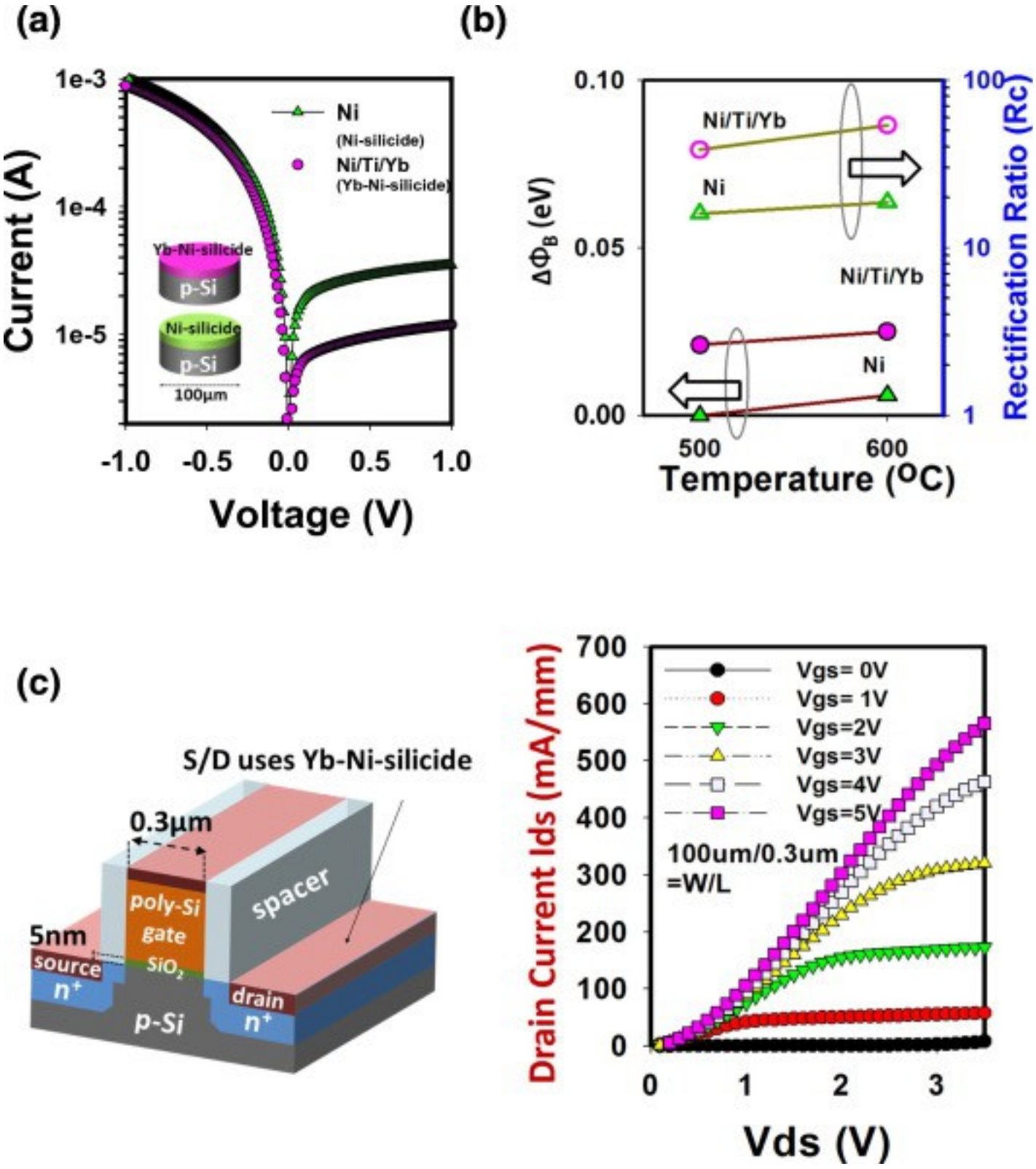

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Fig. 5. (a) Comparison of I–V characteristics of the Schottky diodes using Ni and Yb/Ti/Ni structures. Inset: The schematic illustration of the Schottky diodes. (b) Dependence of ΔΦB and rectification ratio on annealing temperature. (c) I–V characteristics of the fabricated 0.3 μm gate length nMOSFETs using Yb/Ti/Ni structure for S/D contact formation. The schematic representation of the nMOSFETs is also shown. The effective SBHs of the diodes are extracted using the prediction of thermionic emission (TE) theory.

For Schottky diode, the thermionic emission theory predicts that the current–voltage characteristic is given by [24], [25], [26], [27], [28].

(1)I=AA**T2exp−qΦBkTexpqVnkT−1

(2)orI=I0expqVnkT−1forV>3kT

where A is the contact area, Φ_B is the SBH of metal/semiconductor interface, q is the electron charge, k is the Boltzmann constant, I is the measured current of the Schottky diode, T is the absolute temperature, V is the applied voltage n is the ideality factor and I_0 is the saturation current given by:

(3)I0=AA**T2exp−qΦBkT

The ideality factor n is defined as:

(4)n=qkTdVdlnI

The values of saturation current I_0 and ideality factor n are obtained from the linear portion of ln(I) vs V plot at various temperature. The values of zero-bias barrier height at each temperature are determined from saturation current (I_0) using Eq. (3)

Once I_0 is determined, the zero-bias barrier height (Φ_B) is obtained by rewriting Eq. (3) as:

(5)ΦB=kTqlnAA**T2I0

where A^{**} is the effective Richardson constant for p-type silicon, A^{**} = 32 A cm^{-2} K^{-2} and Φ_B is the barrier height at zero bias.

The thermionic emission current density J at a metal/semiconductor interface of a Schottky diode can be expressed as follows:

(6)J=A**T2exp−ΦBkTexpqnkTV−IRS−1

where J is current density, R_S is the series resistance.

SBH of Ni-silicide diode annealed at 500 °C is 0.425 eV and is taken as a reference for the calculation of SBH modulation (ΔΦB) of the Yb-Ni-silicide diode. The calculated ΔΦB at 500 °C (600 °C) is 0.02 eV (0.025 eV) as shown in Fig. 5 (b). The rectification ratios of the diode defined in a previous published work [9] are also present in the same plot.

Since R_C(Contact Resistance) is dependent on contact resistivity ρ_c, sheet resistance of the S/D region R_{SD}, width W_C and length L_C of the contact hole and the transfer length L_T, [29]as given by

(7)RC=ρCRSDWC×tanhLCLT

In the S/D regions of a MOSFET, the contact resistivity ρ_C is given by.

(8)ρC∝e4πεsm*hΦBN

where ε_s, m^*, and N are the permittivity, effective mass, and active dopant concentration of the semiconductor, respectively, h is Planck's constant, Φ_B is the Schottky barrier height (SBH), and ρ_c is an exponential function of Φ_B, and a small reduction of Φ_B can significantly reduce ρ_C and R_C. Φ_B well below 0.5 eV would be needed to realize contact resistivities in the order of 10^{-8} Ω cm^2 needed for MOSFETs in advanced technology nodes.

Therefore, an effective method for reducing R_C is to reduce Φ_B through appropriate selection of metal silicide work function. Rare earth silicides generally have low work function values, and can be used as contact materials for S/D silicide.

In this work, we are tuning Φ_{Bn} through inserted a Ti diffusion barrier layer between Yb and Ni layers. Yb atoms can be constrained in a specified reaction region during silicidation for a work function tuning.

This leads to the formation of metal alloy Ni-Yb silicides. Since the work function of Ni-Yb silicides is lower than NiSi, so getting a smaller Φ_{Bn} than NiSi on n-Si.

The Yb-Ni-silicide diode shows higher rectification ratio and higher SBH for hole which is beneficial for S/D contact formation in nMOSFETs. In order to demonstrate the feasibility of the proposed Yb confinement structure in device applications, 0.3 μm gate length nMOSFETs using Yb/Ti/Ni structure for contact formation were fabricated and characterized. Fig. 5 (c) shows the schematic representation and the drain current-drain voltage curves of the nMOSFET.

The results showed that the Yb confinement structure was successfully developed and integrated into nMOSFET for S/D R_C reduction, leading to enhanced drive current performance that exhibits over 500 μA/μm (drain-to-source = 3 V, Gate = 5 V).

The device has high drive current and shows good electric performance with threshold voltage about − 0.01 V in comparison to other commonly studied silicides such as $NiSi_2$ or $CoSi_2$, for instances [30], [31], since these combinations can lead to low potential barriers at the contact.

For device performance, mobility is an important parameter. The mobility of the device is mainly depending on the semiconductor channel mobility with the influence of the surface roughness of the gate oxide/semiconductor interface under the gate control

region. The introduction of Ni-Yb-silicide in source/drain electrodes is not expected to induce mobility degradation of the device. Furthermore, reduction of the S/D contact resistance does not affect the actual effective mobility for MOSFETs. Instead, it will improve the drive current and effective mobility extraction [32].
In the present study, a RE metal confinement structure, using Yb as an example, is successfully demonstrated for the formation of uniform Yb-Ni silicide for SBH lowering. In this structure, a thin layer of Ti is inserted between Yb and Ni layers. Ti is acting as a diffusion barrier to prevent the out diffusion of Yb and at the same time to control the supply of Ni into the Si substrate during silicide formation. Yb atoms can be confined below the Ti diffusion barrier layer and a composition-uniform Yb-Ni silicide is formed. The Yb confinement structure is also implemented in the source/drain (S/D) contacts of nMOSFETs to verify the usability of this technique. It shall be mentioned that although Ti layer has been widely applied to the various platforms as a diffusion barrier layer, Ti acting as a diffusion barrier for rare-earth based contact metal is investigated for the first time in the present work.

4. Conclusions

In conclusion, a simple but effective RE metal confinement structure for Schottky barrierheight engineering has been extensively explored for the reduction of R_c in advanced MOSFETs. Modulation of Schottky barrier height with an inserted 10 nm Ti barrier layer between Yb and Ni shows effective Schottky barrier reduction for application in a Yb-Ni-silicide diode. We have demonstrated that the Ti diffusion barrier layer can successfully constrain the Yb atoms in a specified reaction region for silicidation in the confinement structure. The Yb confinement structure was also successfully developed and integrated into 0.3 μm gate-length nMOSFET for S/D R_c reduction, leading to enhanced drive current performance that exhibits over 500 μA/μm (drain-to-source = 3 V, Gate = 5 V). The RE metal confinement structure provides a CMOS compatible approach for further SBH engineering and is a promising method for future technology nodes.

Acknowledgments

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