Title

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Authors

Dalakoti, Aditya
Miller, Merritt
Brewer, Forrest

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Pulse Ring Oscillator Tuning via Pulse Dynamics

Aditya Dalakoti
adityadalakoti@ucsb.edu

Merritt Miller
merrittmiller@ucsb.edu

Forrest Brewer
forrest@ucsb.edu

Electrical and Computer Engineering Department, University of California Santa Barbara

***Abstract*— This paper presents a practical method for improving timing uncertainty due to thermal noise in a ring oscillator. The methodology utilizes delay elements with non-linear behavior dependent on *event separation*, the period between successive events. Pulse logic gates are shown to have delay-separation dynamics which can impact the statistics of subsequent events in the oscillators. The slope of the delay-separation is shown to linearly improve the uncertainty in these oscillators. Multiple pulses in a ring is also shown to linearly improve the timing uncertainty.**

I. INTRODUCTION

Distribution of high frequency, low jitter timing over long distances is costly, motivating small localized synchronizing oscillators that maintain some global phase relation. The noise in phase-locked timing oscillators is typically dominated by thermal and other white noise sources. Since phase noise is cumulative [1], and oscillator noise sensitivity is cyclical [2], the total phase noise can be modeled as a random walk where a step is taken in phase space each cycle [3]. Assuming uncorrelated noise, the divergence of the actual phase from the ideal phase is proportional to the square root of time. In this model, the quality of the oscillator is the slope of the phase divergence relative to the square root of time. Methods to modify the random walk to improve this slope include spatially coupled oscillators [4], distributed oscillators [2] and transistor sizing [1]. In all of these techniques, scaling the solution by replication, power, or other means result in improvements proportional to the square root of the scale factor.

Pulse circuits have dynamics where the delay of a gate is a function of the time-separation of pulses allowing the phase and frequency of an oscillator to interact at the gate-level. Non-linear delay-separation dynamics have been observed in asynchronous event-driven logic [5]. This behavior has been exploited in the design of high-performance self-timed pipelines and arbitration circuits [6], [7] and [8].

In this work, delay-separation dynamics is used to improve the statistics of pulse based oscillators. In particular, the slope of the dynamical response and the number of pulses are both shown to *linearly* improve the overall phase uncertainty of the oscillator in contrast to conventional methods aimed at improving high-frequency stability. Basic pulse-gate circuits and the pulse dynamics are explained in section II. Construction and stable operating points of pulse ring oscillators are discussed in section III. Performance improvements analyzed using HSPICE simulations are discussed in section IV.

II. PULSE-GATES AND PULSE DYNAMICS

Pulse gate behavior is easily tuned to create different pulse-to-pulse dynamics, making an effective non-linear delay element. In order to understand gate behavior tuning to achieve different dynamics, gate behavior and meaning of dynamics are explained.

A. Pulse-Gates

The basic topology of a pulse-gate is shown in Figure 1.

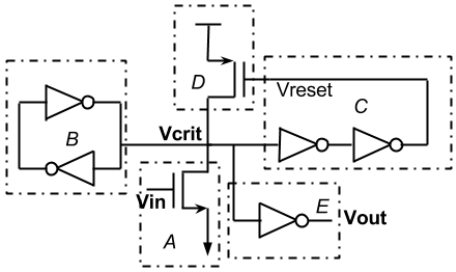


Fig. 1: Pulse-gate Topology:(*A:* Vin : Input Logic Pull-down of Vcrit; *B:* Threshold Control : Controls the threshold for Vcrit; *C:* Reset Loop and Pulse Width : Controls reset behavior; *D:* Pull Up : Pulls up Vcrit on Vreset ; *E:* Vout : Output Buffer)

At steady state, Vin is low and Vcrit is high. A rising edge at Vin pulls down Vcrit. This in turn pulls up Vout and eventually pulls down Vreset, which then pulls up Vcrit. Vcrit then pulls down Vout and pulls up Vreset, making a pulse and reseting the gate. These gates are triggered by, and re-generate brief electrical pulses. They typically have different delays for short triggering intervals than for long intervals. Operated in the transition between short and long intervals, the gate propagation delay is *dependent* on the oscillator frequency. If the dynamics are repulsive, multi-pulse oscillation solutions with uniform timing are possible.

B. Pulse Dynamics with Delay-Separation

Delay-Separation dynamics were observed for asynchronous events interaction in a pipeline [5]. The idea is used in this work to convey the timing information of the current pulse arrival to modify the delay of the subsequent pulse as shown in Figure 2.

For consecutive pulses *A* and *B*, it is often observed that the gate delay of the second pulse D_B is dependent on the relative timing of the first pulse S_A. Effectively, the gate has

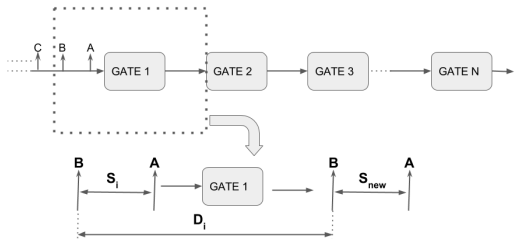


Fig. 2: **Delay** (of a logic gate) for an event is dependent upon the timing **separation** to the immediately previous event.

a relatively long recovery time in which behavior is correct, but the timing of the second pulse is modified. A *delay-separation curve* indicates the propagation delay for a pulse passing through a gate as a function of timing separation from the previous pulse. The simplest curves are *repulsive* shown in 3a or *attractive* shown in 3b. *Repulsion* will result in the separation between pulses to increase in a long chain of gates until the dynamics changes. *Attraction* will cause the pulse separation to decrease. This is the behavior observed for pulses in conventional CMOS logic leading to the pulse-evaporation phenomena.

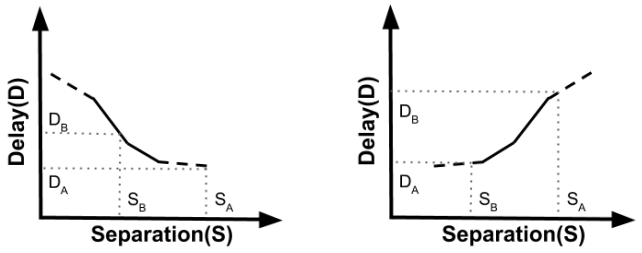


Fig. 3: (a) Repulsion: $D_B > D_A$ Separation between evt A and evt B **increases** after passing the logic circuit. (b) Attraction: $D_A > D_B$ Separation between evt A and evt B **decreases** after passing the logic circuit.

C. Pulse Dynamics in Pulse Buffer

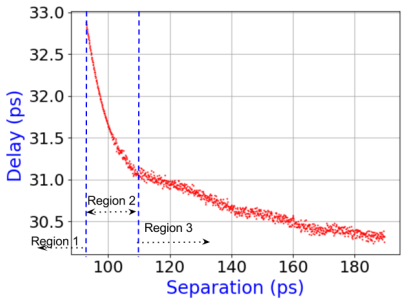


Fig. 4: Delay-vs-Separation Dynamics for Pulse-Gates

For the circuit shown in Figure 1, the delay-vs-separation dynamics observed is shown in Figure 4. This dynamics can be primarily broken into 3 regions of operation.

1) *Region 1* is when Vcrit is still low after the occurence of the first pulse. A subsequent pulse is rejected in this region.
2) *Region 2* is the region of high repulsion slope. It occurs when next rising edge arrives when PMOS has pulled up Vcrit enough that there is a substantial drain-source potential difference across the pull down NMOS. However, there is sufficient voltage swing at Vcrit to cause full swing Vout. On the other hand, both pull-up and pull-down sources are active, delaying the swing of Vcrit. This results in a larger delay as the pulse separation is decreased. This region ends when Vreset goes up.
3) *Region 3* starts after Vreset is pulled up. The lesser delay slope is a function of stored charge in the SRAM hysteresis loop and input transistor network.

In order to model or modify the pulse dynamics, the key behavioral mechanisms need to be understood. These are:

- **Detection**: Detect input pulse rising edge
- **Pulse Generation**: Output a pulse on detection based on current state of the circuit
- **Pulse Width Control**: Maintain output pulse width
- **State Control**: Maintain state to control the next pulse bevavior. It refers to timing control of when pull up and pull down fight at Vcrit in the dynamics plot.

For pulse-gate shown in Figure 1, *Pulse Width Control* and *State Control* are interlinked to each other and hence the freedom to modify the dynamics is limited.

D. Modified Pulse Dynamics

In order to independently adjust the pulse dynamics, pulse-gates were implemented using the updated pulse-gate shown in Figure 5. Separate *Pulse Width Control* and *State Control* allow for independent timing tuning of pulse-width and internal gate reset.

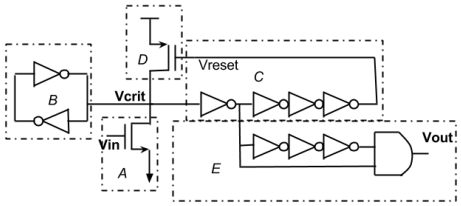


Fig. 5: Pulse-gate with separate *State Control* : **C** path and *Pulse-Width Control* : **E** path

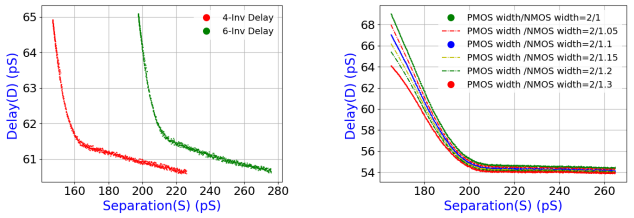
Two functionalities which can be achieved are:

- *Separation axis:* Delay in the reset loop shifts the curve along the separation axis as shown in 6a
- *Delay axis:* PMOS to NMOS ratio at the Vcrit node shifts the curve along the delay axis as shown in fig 6b. It also controls the slope in *Region 2*.

III. Pulse Ring Oscillator

A. Construction

An abstract model for the Pulse Ring Oscillator is shown in Figure 7. M pulses are fired into the ring of N pulse gates,



(a) (b)

Fig. 6: (a) Dynamics along separation axis (b) Dynamics along delay axis and dynamics slope in Region 2

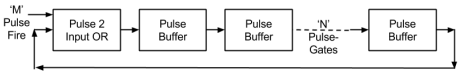
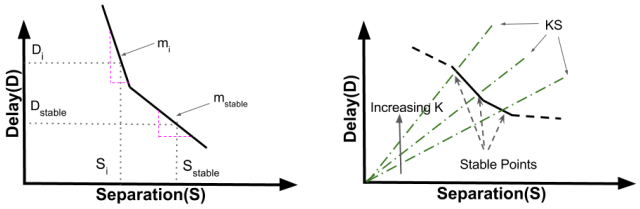


Fig. 7: Abstract Model of Pulse Oscillator with 'M' Pulses and 'N' Stages

each with identical separation curves. The initial separation between the pulses is decided based upon the expected stable operating point of the ring.

B. Stable Point



(a) (b)

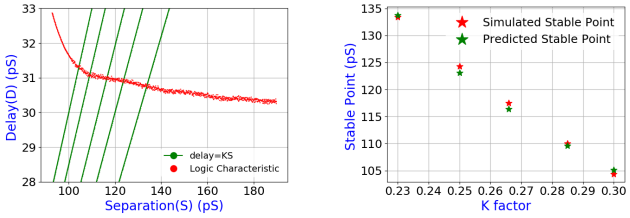
Fig. 8: (a) Slope at different Separation (b) Evaluating the stable point

To estimate the stable point of an oscillator built from a uniform ring of pulse-gates supporting multiple pulses, a constant K is defined as *number of pulses (M)* divided by *number of logic stages (N)*, $K = M/N$.

$$D = KS \tag{1}$$

where D is the gate delay seen by each pulse, S is the separation between pulses(oscillator period). The stable point is the intersection of the delay-vs-separation plot of the logic gates and delay given by Equation 1. For the case of $Repulsion$ dynamics, stable point for different K is approximated as shown in 8b. Repulsion delay-separation results in a stable equilibrium. Any change in separation from the stable point brings the oscillator back to stable point due to the negative slope at this point. Attraction usually results in a non-uniform stream of pulses or pulse loss.

The stable operating point based on intersection of $D = KS$ and delay-separation dynamics of Pulse-Gate is shown in 9a for different values of K. The projected (from intersection as discussed above) and simulated (HSPICE) stable ring periods are shown in 9b.



(a) (b)

Fig. 9: (a) Intersection of $D = KS$ and Delay-Separation (b) Simulated and Predicted Stable points

IV. Performance Improvements

A. Random Walk Slope-vs-Dynamics Slope

Thermal and electrical noise in an oscillator causes both phase and amplitude variations [9]. Ring oscillators, constructed of non-linear amplifiers, suppress amplitude noise. Errors in phase, on the other hand, tend to accumulate. Because the error (in phase) of any given cycle is both independent of previous cycles, and cumulative, the phase offset of a oscillator can be modeled as a random walk.

For a pulse-gate ring, impulse noise changes the separation between pulses. When the separation changes, the gate-delay changes. Effectively, a pulse communicates to the next pulse whether it occurred before or after its nominal time via delay modulation. Similarly, the next pulse communicates its position in turn. A ring of pulse gates will operate at a net slower stable period via the delays induced by repulsion. A disturbance (noise) that changes the timing of a pulse modifies its separation to the next pulse to S_i. The other pulses are witnesses to the modified phase, biased proportionally by the local slope at the interim separation point m_i as shown in Figure 8a. The random walk slope (standard deviation of timing uncertainty-vs-square root of time) was simulated with transient noise Monte Carlo simulations in GFUS8RF. Different repulsion slopes were generated using the modified pulse gates discussed in subsection II-D. Timing uncertainty is shown to improve linearly with magnitude of slope of the dynamics as shown in Figure 10.

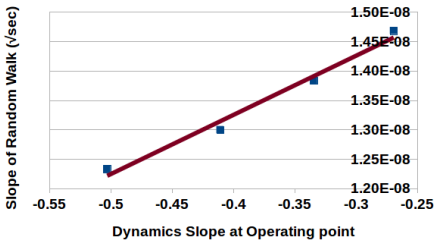


Fig. 10: Timing Uncertainty reduces with increase in magnitude of Dynamics Slope

B. Pulse Interaction

For a conventional ring oscillator or a pulse oscillator with a single pulse, the impulse noise modulation of timing is

approximately identical to the eventual phase shift. However, pulse timing noise is proportionally distributed among all the pulses in a multiple-pulse oscillator. To demonstrate the difference, a comparison between a 1-pulse 4-delay ring and a 2-pulse 8-delay ring (at the same nominal frequency) is made in Figure 11. The response to a voltage impulse (applied to a single delay stage) on a conventional ring oscillator and on a single-pulse ring is shown in 11a and in 11b respectively. The two pulse-ring in 11c shows how the oscillator attempts to reconcile the difference in phase of the perturbed and non-perturbed pulses. The result is lower total phase offset, roughly 2.3ps or less than 50% of the non-interacting perturbation.

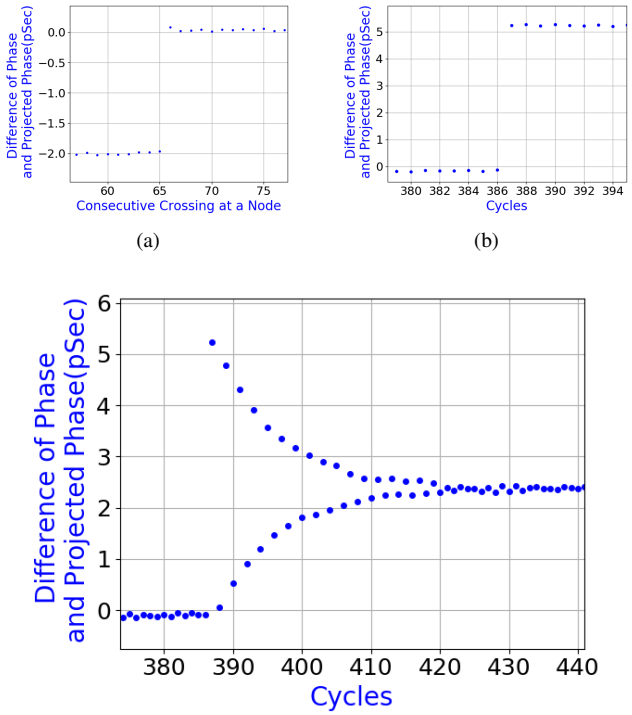


Fig. 11: Phase Change from impulse perturbation for (a) Inverter based ring (b) 1 Pulse Ring (c) 2 Pulse Ring

1) Phase Change vs Impulse: The impulse (injected at gate supply) magnitude to phase change relationship was linear in the oscillators as shown in 12a.

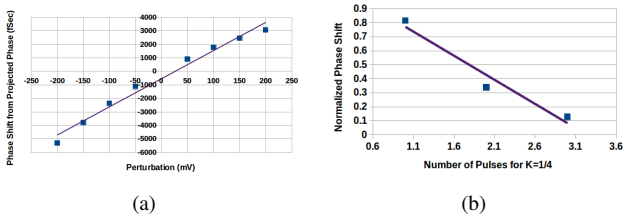


Fig. 12: Impulse phase shift (a) vs. Amplitude (b) vs. number of pulses

The final phase shift from the projected phase (based on mean oscillator period) decreases with number of pulses as shown in 12b.

2) Number of Pulses vs Global Noise: HSPICE Monte Carlo global noise simulations show that the slope of the random walk decreases with increase in number of pulses (scaled to the same operation frequency) as shown in 13a due to division of noise energy in different pulses. This improvement remains *linear* with physical scaling of the oscillators.

3) Comparison to Inverter Ring: The relative slopes for a inverter and pulse oscillator operating at similar frequency and power are shown in 13b. The pulse-gate oscillator has half of the timing uncertainty (the more complex pulse oscillator uses more power in the single pulse case, but its linear noise scaling beats the inverter).

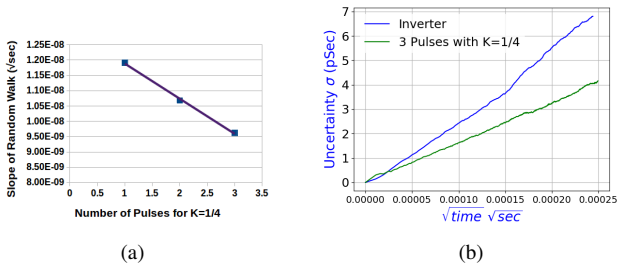


Fig. 13: (a) Random walk slope vs. Number of pulses (b)Random walks of inverter and pulse oscillator with 3 Pulses

V. Conclusion

The non-linear dynamics of pulse-gates offer the potential for linear power scaling of uncorrelated impulse noise in ring oscillators. For multi-pulse oscillator rings, this allows for improvements in high-frequency power/jitter performance over equivalent power/size inverter ring oscillators.

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