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High Speed Integrated Circuits for High Speed Coherent Optical Communications

A Dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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This dissertation is dedicated to my parents

for their love and support.

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But He knows the way that I take; when He has tested me, I will come forth as gold. -Jobs 23:10

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2007	*The Best Research Award* School of Information and Communication Engineering, Sungkyunwan University, Feb. 2007.
2006	*Outstanding Achievement Award, 2nd and 3rd Ranked, Student Design Competition* 2006 IEEE MTT-S Int. Microwave Symp., San Francisco, CA, Jun. 11-16, 2006.

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Abstract

High Speed Integrated Circuits for High Speed Coherent Optical Communications

by

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With the development of (sub) THz transistor technologies, high speed integrated circuits up to sub-THz frequencies are now feasible. These high speed and wide bandwidth ICs can improve the performance of optical components, coherent optical fiber communication, and imaging systems. In current optical systems, electrical ICs are used primarily as driving amplifiers for optical modulators, and in receiver chains including TIAs, AGCs, LPFs, ADCs and DSPs. However, there are numerous potential applications in optics using high speed ICs, and different approaches may be required for more efficient, compact and flexible optical systems.

This dissertation will discuss three different approaches for optical components and communication systems using high speed ICs: a homodyne optical phase locked loop (OPLL), a heterodyne OPLL, and a new WDM receiver architecture.

The homodyne OPLL receiver is designed for short-link optical communication systems using coherent modulation for high spectral efficiency. The phase-locked coherent receiver can recover the transmitted data without requiring complex back-end digital signal processing to recover the phase of the received optical carrier. The main components of the homodyne OPLL are a photonic IC (PIC), an

electrical IC (EIC), and a loop filter. One major challenge in OPLL development is loop bandwidth; this must be of order 1 GHz in order for the loop to adequately track and suppress the phase fluctuations of the locked laser, yet a 1 GHz loop bandwidth demands small (<100 ps) propagation delays if the loop is to be stable. Monolithic integration of the high-speed loop components into one electrical and one photonic IC decreases the total loop delay. We have designed and demonstrated an OPLL with a compact size of $10 \times 10\ mm^2$, stably operating with a loop bandwidth of 1.1 GHz, a loop delay of 120 ps, a pull-in time of 0.55 μs and lock time of <10 ns. The coherent receiver can receive 40 Gb/s BPSK data with a bit error rate (BER) of $< 10^{-7}$, and operates up to 35 Gb/s with BER $< 10^{-12}$.

The thesis also describes heterodyne OPLLs. These can be used to synthesize optical wavelengths of a broad bandwidth (optical wavelength synthesis) with narrow linewidth and with fast frequency switching. There are many applications of such narrow linewidth optical signal sources, including low phase noise mm-wave and THz-signal sources, wavelength-division-multiplexed optical transmitters, and coherent imaging and sensor systems. The heterodyne OPLL also has the same stability issues (loop delay and sensitivity) as the homodyne OPLL. In the EIC, a single sideband mixer operating using digital design principles (DSSBM) enables precisely controlled sweeping of the frequency of the locked laser, with control of the sign of the frequency offset. The loop's phase and frequency difference detector (PFD) uses digital design techniques to make the OPLL loop parameters only weakly sensitive to optical signal levels or optical or electrical component gains. The heterodyne OPLL operates stably with a loop bandwidth of 550 MHz and loop delay of <200 ps. An initial OPLL design exhibited optical frequency

(wavelength) synthesis from -6 GHz to -2 GHz and from 2 GHz to 9 GHz. An improved OPLL reached frequency tuning up to 25 GHz. The homodyne OPLL exhibits -110 dBc/Hz phase noise at 10MHz offset and -80 dBc/Hz at 5 kHz offset.

Finally, the thesis describes a new WDM receiver architecture using broadband electrical ICs. In the proposed WDM receiver, a set of received signals at different optical wavelengths are mixed against a single optical local oscillator. This mixing converts the WDM channels to electrical signals in the receiver photocurrent, with each WDM signal being converted to an RF sub-carrier of different frequency. An electrical IC then separately converts each sub-carrier signal to baseband using single-sideband mixers and quadrature local oscillators. The proposed receiver needs less complex hardware than the arrays of wavelength-sensitive receivers now used for WDM, and can readily adjust to changes in the WDM channel frequencies. The proposed WDM receiver concept was demonstrated through several system experiments. Image rejection of greater than 25 dB, adjacent channel suppression of greater than 20 dB, operation with gridless channels, and six-channel data reception at a total 15 Gb/s (2.5 Gb/s BPSK $\times$ 6-channels) were demonstrated.

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Chapter 1

Introduction

I have worked on the DARPA Photonic Integrations for Coherent Optics (PICO) project during my Ph.D. study for four years (July 2010 - Aug 2014), collaborating with Prof. Larry Coldren's group (Mingzhi Lu, Abi Sivananthan, John Parker and Leif Johannson) and Prof. John Bowers' group (Molly Piels). I have devoted all my efforts to coherent optical systems utilizing our high speed integrated circuit (IC) designs (with Eli Bloch) and system designs and their system experiments (Mingzhi Lu and Molly Piels). The main topics of my research were high-speed ICs, homodyne optical phase locked loop (OPLL), heterodyne OPLL, and new coherent wavelength division multiplexing (WDM) receivers under the direction of Prof. Mark Rodwell. All topics were successfully demonstrated. In my dissertation, I will describe all my work starting from high-speed IC designs to system-level experiments, including their analysis to support our experimental results.

1.1 Background and motivation

Developments in advanced III-V and Silicon transistor technologies [1–5] have made it possible to design high frequency ICs for sub-THz applications [6–17]. High speed ICs using these technologies can improve the performance of optical components, optical fiber communications, and optical sensing systems. There will also be many new applications in optics using high speed ICs, and different approaches may be required for better and more efficient systems.

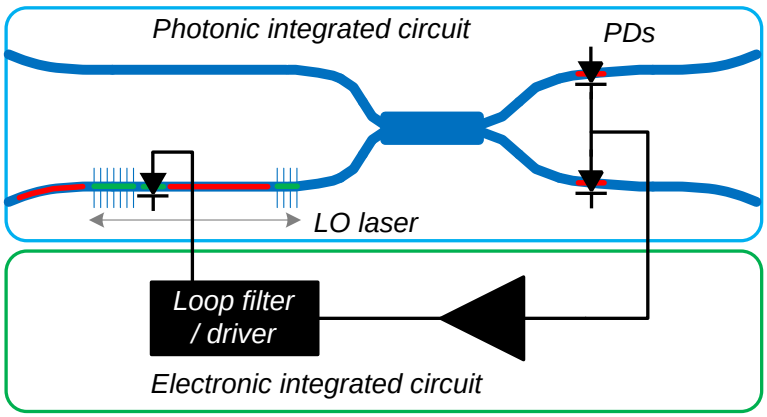
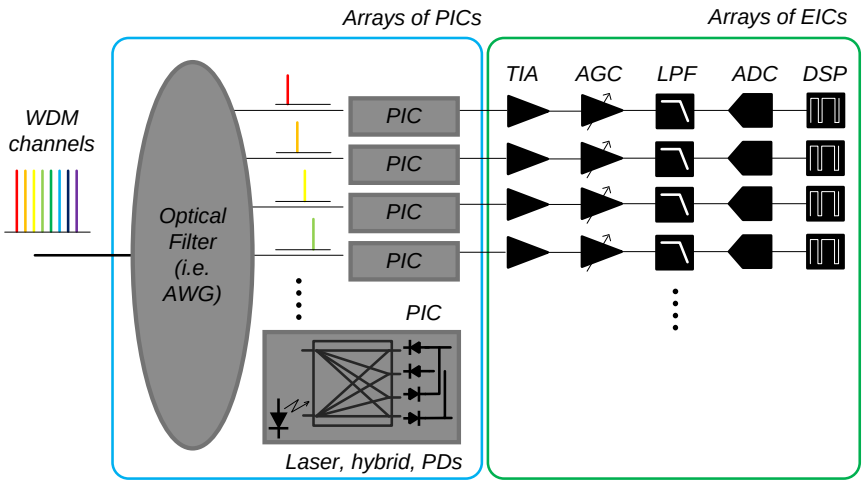


Figure 1.1: Conceptual integrated optical phase locked loop (OPLL) schematic.

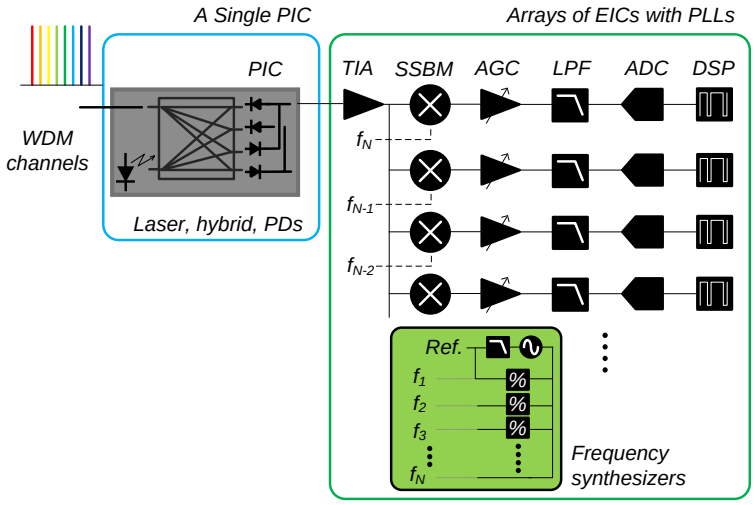
In my dissertation, three main research approaches for coherent optical fiber communication systems using high speed ICs will be discussed: Homodyne OPLL, heterodyne OPLL, and a new WDM receiver architecture.

Optical coherent techniques can improve optical communication and sensor systems, i.e. homodyne detections and wavelength synthesizers. The OPLLs (optical phase synchronous techniques) may have a variety of applications and will be very powerful, similar to their counterpart in the electrical domain [18–24]. However, designs of the OPLLs have been challenging because of feedback loop

delay and laser linewidth. Current OPLLs use 100 ns delay and 10 kHz linewidth lasers which are unsuitable, bulky and expensive [25–28]. The OPLLs must be integrated, have wide loop bandwidth, and have small loop delay, i.e. >1.0 GHz and <0.1 ns, which are known to be challenging [29–41]. In collaboration with Prof. Larry Coldren's group, integrated OPLLs were designed using high speed photonic ICs and electrical ICs as shown in figure 1.1.



(a)



(b)

Figure 1.2: Conceptual WDM receiver schematics for conventional architecture (a) and new proposed WDM receiver architecture (b).

Digital coherent detection (or intradyne detection) techniques are currently very popular in coherent optical fiber communications because of their powerful DSP functions of carrier phase frequency estimation and linear and non-linear compensation [42–47]. A single optical fiber carrying WDM signals can have

capabilities of >100 Gb/s and even toward >1 Tb/s [48–51]. Therefore, many different receiver architectures and strategies have been suggested, i.e. DWDM, super-channels, elastic optics [51–55]. However, conventional WDM receiver architectures still use an optical filter as an optical channel de-multiplexer and arrays of coherent detectors for each channel as shown in figure 1.2 (a). These photonic ICs are still bulky, complicated, and can be better optimized using current high speed electrical ICs [44, 56–58]. Thus, a new coherent WDM receiver architecture using wide bandwidth and precisely designed electrical ICs has been proposed and designed shown in figure 1.2 (b). The previous conventional WDM receivers are expected to improve in terms of complexity, chip size, power consumption, cost, and system robustness.

1.2 Challenges and Previous Work

Historically, a large loop delay and correspondingly narrow bandwidth has been considered an inherent drawback of OPLLs: *The PLL bandwidth was usually limited below 1 MHz because of large loop delay, and it was difficult to maintain system stability when semiconductor lasers had large phase noise and frequency drift. This technical difficulty inherent in OPLL has not been solved perfectly even when we use state-of-the-art distributed-feedback (DFB) semiconductor lasers. - K. Kikuchi* [29]. OPLL designs have been challenging because of feedback loop delay and laser linewidth. Compared to OPLLs using ultra-stable lasers (10 kHz laser linewidth), our integrated SG-DBR lasers are more compact and inexpensive. They have naturally broad linewidth (∼5 MHz linewidth), and drift is several 10's

of MHz [40,59]. Therefore, the integrated lasers in the OPLLs need as wide a loop bandwidth as possible, i.e. >500 MHz loop bandwidth, to stabilize the integrated lasers against wide phase and frequency noise and to track a reference laser. To build the OPLLs with a wide loop bandwidth, a small loop delay τ is necessary. The absolute stability condition for the OPLL designs with significant loop delay has been analyzed [18, 60] as

$$\omega_n \times \tau < 0.736, \tag{1.1}$$

where $\omega_n \times \tau$ is a phase variation. Following equation 1.1, a loop bandwidth $\omega_n =$ 500 MHz must have less than ∼200 ps loop delay. In [61], the minimum total phase error variation (rad^2) and minimum noise penalty are obtained using 2-3 GHz loop bandwidth for our SG-DBR laser including laser linewidth and thermal and shot noise. However, a loop bandwidth of 2-3 GHz is physically difficult to obtain given the loop delays, and therefore, the loop bandwidth should be as wide as permitted by the loop delay. OPLL designs have also been challenging because of laser loop stability. The diode lasers are very sensitive to external variations. For example, temperature variation changes the laser frequency ∼10 GHz/degree, and mechanical vibrations can change optical coupling intensity and vary the phase detector's lock condition which leads to cycle-slip or false lock [30,33,37,38,62,63]. Therefore, we must apply techniques resistant to such external variations to the OPLL designs [37, 38, 64, 65].

Much coherent optical communication research including OPLLs has been performed before the introduction of WDM, Erbium-doped fiber amplifiers (EDFA), and digital coherent detection [28, 66–69]. Recently, OPLL research has been revived. The research focuses on minimizing the loop delay, for instance, through

packaging OPLL with such loop delay of 380 ps [32], by hybrid integration of the PIC and discrete electrical circuits, including amplifiers, XOR gates, and loop filters on a printed circuit board with delay of 1.8 ns [31], OPLL integration on to a small AlN carrier board using FETs for loop filter designs with delay of less than 300 ps [30], and recent flip-chip bonding of PIC and EIC at UCSB. Different approaches of OPLL designs have also been published, using many auxiliary components of the optical VCO with Mach-Zehnder modulator, and even digital sampling using slow ADCs and DSPs [26, 70].

In our OPLL designs [37–41], we have used highly integrated PICs and EICs to minimize the loop delay. In the high speed EIC, we have included complicated functions to stable OPLL operations, i.e. limiting amplifiers, binary phase and frequency detector, digitally operating single sideband mixers and all 50 Ω high-speed interfaces. In addition, we have proposed a dual-path (feed-forward) loop filter to nearly eliminate loop filter delay at high frequencies near loop bandwidth ω_n.

In addition to OPLL designs, we have also focused upon WDM receivers in this dissertation. Coherent WDMs have been widely used in optical fiber communications, because of DSPs' powerful carrier phase and frequency estimations and linear/non-linear distortion and rotation compensations [42–47]. However, current coherent WDM systems (figure 1.2 (a)), which consist of bulk optical filter for de-multiplexing channels and arrays of coherent receivers for data recovery on each channel, can be improved by using our high speed photonic ICs and electrical ICs. The two key challenges are the speed and bandwidth of the electrical ICs and photodiodes in the PIC. The numbers of WDM channels and total bit rates

are limited by their bandwidth, i.e. 25 GHz channel × 8 channels need more than 200 GHz circuit bandwidth. However, technologies of both the ICs have been quickly developed, i.e. EIC's III-V transistors exceed bandwidth 1 THz f_{max} (silicon bandwidth ∼500 GHz) [2, 3] and their circuits can extend bandwidth to >500 GHz (amplifiers) [6–8, 11], 300 GHz (PLLs) [9], 200 GHz (digital logics) [71], and 200-300 GHz transceivers [13–17], and the PIC's UTC photo-detectors (PDs) exceed bandwidth of more than 300 GHz [72]. Advanced circuit technologies also can double the data channel bandwidth using single side frequency band operations (+ and - frequency channels). Hence, we have proposed a new coherent WDM receiver concept of a cascade optical and electrical down-conversion (figure 1.2 (b)). This can improve the current coherent WDM receiver systems in terms of cost, power consumption, complexity, and flexibility [73, 74].

The main key concepts are that a single broadband PIC with one LO laser can handle many WDM channels, i.e. 25 GHz × 8 channels now require 100 GHz bandwidth, and most complicated channel selection work can be done in high speed and precise electrical ICs with electrical frequency synthesizers and single sideband mixers or more advanced circuit technologies of analog FFTs, soft-defined radio (SDR), and cognitive radio (CR) with sampling concepts [75–77]. Moreover, as this concept has recently been spotlighted as super-channel and flexible (or elastic) channel WDM receivers, our proposed WDM receiver concepts can minimize efforts on the ADC and DSPs' circuit speed and bandwidth which directly related to costs and circuit design challenges [51–55].

The similar concepts of broadband coherent receiver systems from 50 MHz to 1 GHz have been very popular in broadcasting DTV tuners [78–80]. The concepts

have been demonstrated and proven in recent wireless communication electrical systems. Many critical design issues of harmonic and image rejections have been figured out by electrical circuit technologies and DSPs. Our proposed WDM receivers from DC to 100 GHz (or even more) will have similar circuit design issues including DSPs as the current WDM receiver systems do, except for electrical circuit bandwidths, chip-to-chip interconnections, and power consumptions.

As initial demonstrations, I have designed various high speed ICs using Teledynes 500 nm InP HBTs. I also have designed high speed ∼100 GHz sub-block ICs such as TIAs, single sideband mixers, Cherry Hooper amplifiers, and poly-phase filters. Also, sub-channel ICs of ±12.5 GHz, ±37.5 GHz, and ±62.5 GHz and full-six channel WDM receiver ICs up to 75 GHz frequency bandwidth have been designed including the sub-blocks. The sub-block ICs and the system ICs have been tested and demonstrated for data recovery experiments to prove our proposed WDM receiver concepts [73, 74, 81, 82].

1.3 Preview of Dissertation

In this dissertation, I have investigated three research topics of homodyne and heterodyne OPLLs and WDM receivers for high-speed coherent optical fiber communications using high speed electrical ICs. In chapter 2, fundamental broadband IC designs and their backgrounds are introduced, and then, our sub-block high speed ICs for the optical systems (OPLLs and WDM receivers) will be shown with their simulation (or measurement) results and chip layouts. In chapter 3, a homodyne OPLL (an optical Costas loop receiver) for a short-link coherent optical

communication is implemented in a compact size of $10\times10\ mm^2$ single board, and the receiver demonstrates 35 Gb/s data recovery with error-free (BER less than 10^{-12}) and 40 Gb/s data recovery with BER less than 10^{-7}. In chapter 4, a heterodyne OPLL as a wavelength synthesizer is implemented, and the synthesizer exhibits sign selectable ±20 GHz frequency offset locking with ultra-low phase noise performance. In chapter 5, a new proposed WDM receiver is proposed and the concept is fully verified from three different experimental demonstrations of image rejection, adjacent channel interference and full six-channel recovery. Six-separate WDM modulated channels with 2.5 Gb/s BPSK (total 15 Gb/s BPSK), 10 GHz spacing are successfully recovered as initial concept demonstrations. In last chapter, I will conclude my Ph.D. works and propose the future research directions. For all results, detail design approaches, experimental methods, experimental results, and their analysis will be following in this dissertation.

Research highlights during my Ph.D are as following.

- *Homodyne OPLL* - collaborating with Mingzhi Lu and Eli Bloch.
  - Highly integrated OPLL within $10\ \times\ 10\ mm^2$.
  - Highly stable OPLL operations: 120 ps loop delay, 1.1 GHz loop bandwidth, ∼550 ps frequency pull-in time, <10 ns lock-time.
  - Up to 40 Gb/s BPSK data reception without DSPs and latency.
- *Heterodyne OPLL* - collaborating with Mingzhi Lu and Eli Bloch.
  - Highly integrated OPLL (the same as the homodyne OPLLs).
  - First single sideband wavelength synthesis up to ±20 GHz.
  - Highly stable OPLL operations: <200 ps loop delay and 550 MHz loop bandwidth.

- Phase noise performance: -110 dBc at 10 MHz offset and -80 dBc/Hz at 5 kHz offset.

- *Single-chip multi-channel WDM receiver* - collaborating with Molly Piels and Eli Bloch

- A new WDM receiver concept using broadband ICs
- Cascade optical and electrical down-conversions.
- First concept demonstrations: image rejection of greater than 25 dB, adjacent channel suppression greater than 20 dB, gridless channel operations, and six-channel recovery.
- A dense WDM channel data recovery of 5 GHz channel spacing with 2.5 Gb/s BPSK for each channel.
- A broadband of 107 GHz trans-impedance amplifiers.

- *Laser linewidth narrowing technique* - collaborating with Abi Sivanathan (not included in this dissertation).

- The first integrated laser stabilization.
- The compact size of less than 10 $\times$ 10 mm^2.
- The 33:1 linewidth narrowing from 19 MHz to 570 kHz.

- *W-band power amplifiers* - collaborating with Saeid Daneshgar (not included in this dissertation).

- The record >30 % PAE W-band (86 GHz) power amplifiers with >200 mW output power.
- The record >24 % PAE W-band (81 GHz) power amplifiers with ∼470 mW output power.
- Novel 2:1 sub-quarter-wavelength baluns for 4:1 output power with <0.6

dB insertion loss.

- Novel 4:1 sub-quarter-wavelength baluns for 16:1 output power with <0.9 dB insertion loss.
- High power density of >1 W/mm^2.
- The highest output power of ∼470 mW (26.7 dBm) at W-band using low DC supply of 2.75 V.

This work was enabled by strong collaboration between the groups of Prof. Larry Coldren (photonic integration), Prof. John Bowers (silicon photonics), and Prof. Mark Rodwell (high speed integrated circuits). Mingzhi Lu, graduate student a student in Prof. Larry Coldren group, developed the high speed coherent photonic ICs including widely tunable laser, 90 degree hybrid and broadband photodiodes (PDs) as key components of the OPLLs. Molly Piels, a graduate student in Prof. John Bowers group, worked with me for the WDM receiver demonstrations using her photonic circuits and BPSK phase estimation Matlab codes. Eli Bloch (a visiting student from Technion University in Israel) and I have worked for Prof. Mark Rodwell and we have designed high speed ICs for the optical systems (most of the ICs worked on the first design cycle). They all will be promising alternative solutions for the coherent optical fiber communications systems in the near future.

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Chapter 2

High Speed ICs and Designs

This chapter is about high speed electrical integrated circuits (ICs) for high speed coherent optical fiber communications systems in the PICO project. I was involved in four main research topics: 1) homodyne optical phase locked loops (OPLLs) for short-link coherent optical communications, 2) heterodyne OPLLs for optical frequency synthesis, 3) integrated sampled grating-distributed Bragg reflector (SG-DBR) laser linewidth narrowing (stabilization) techniques using frequency locked loops, and 4) new single-chip multi-channel WDM receiver IC desisgns and demonstrations. All of the above systems used our high-speed electronic ICs for stable feedback loop operations and wide bandwidth data reception. I designed the ICs with Eli Bloch using Teledyne's 500 nm InP HBT technology, with 300 GHz f_τ and f_{max}. This work led to many conference proceeding and journal publications for separate block ICs and system experiments.

In this chapter, I will introduce several broadband amplifier structures with various characteristics. Then, I will show our electrical circuit designs with anal-

ysis, their schematics, layouts, and simulation or measurement results.

2.1 Transistor Devices and IC Metal Layers

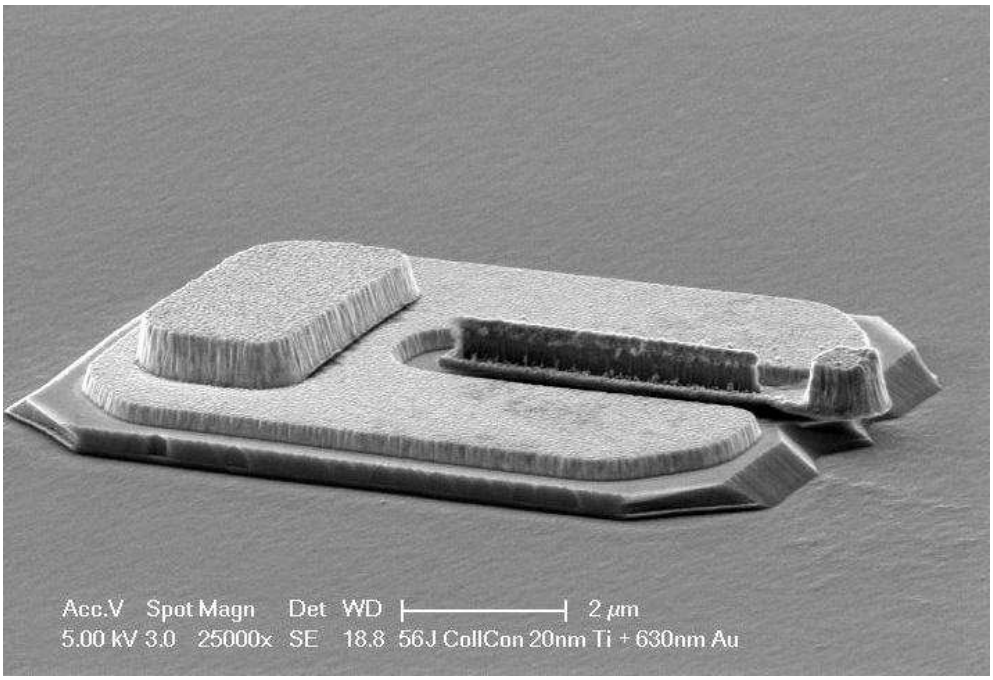


Figure 2.1: An SEM image for a THz HBT device from UCSB's facilities (L_e = 4 μm, W_e = 150 nm, and W_b = 450 nm), image courtesy J. C. Rode.

Transistor technology continues to advance rapidly. For example, THz transistors [1–3] and high-speed, broadband analog/digital circuits with speeds over 100 GHz have been demonstrated recently [4–16]. Therefore, a variety of applications in wireless and optical systems are becoming promising and their paradigms may change in the near future. My research group (Prof. Mark Rodwell's group) has been pursuing 2 THz and 3 THz InP HBTs (figure 2.1) and high-g_m fast logic MOSFET devices together with Teledyne Science (THz program) and with the

SRC program. Commercial silicon-based devices have also been rapidly improving and >500 GHz f_{max} [17] are now accessible for relatively high-speed analog/mixed ICs and complicated digital ICs. For decades my group, Teledyne and others have achieved many high-speed ICs up to 600 GHz using cutting-edge InP HBTs. For examples, 670 GHz amplifiers [4,18], 220 GHz 180 mW power amplifiers [19], DC-300 GHz distributed amplifiers [20], ∼0.5 W 81 GHz power amplifiers and 30% PAE W-band power amplifiers [21–24], 300 GHz PLLs [7, 9], 107 GHz resistive feedback type TIAs [25], 100 GHz Cherry Hooper amplifier [26], 200 GHz static divider [27], 300 GHz dynamic dividers [8], >50 GHz single sideband mixers, and 40 Gb/s sample and hold circuits [28].

I (and Eli Bloch) have also designed many high speed analog-mixed and digital ICs primarily using Teledyne's 500 nm InP HBT process (also 250 nm HBTs and 65 nm CMOS processes) for the optical fiber communication systems in the PICO project, and almost all designs worked after the first run and were used as parts of the optical fiber communication systems (OPLLs and WDM receivers).

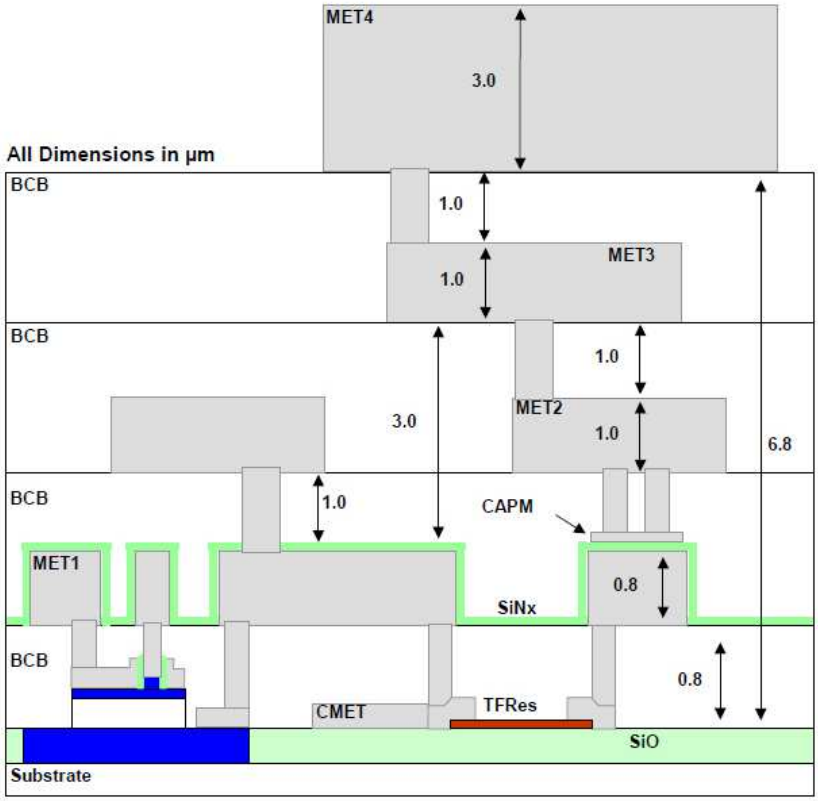
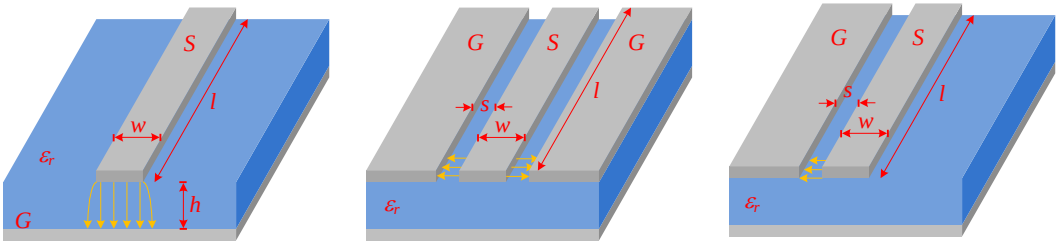


Figure 2.2: Metal layer information provided by TSC's 500 nm InP HBT process. Top metal (MET4) of 3 μm, MET2-MET3 of 1 μm, and bottom metal (MET1) of 0.8 μm thickness and a dielectric BCB ($\epsilon_r = 2.7$) separation of 1 μm between each metal. Metal-insulator-metal (MiM) capacitors have been supported for high dense capacitance. Courtesy of Teledyne Science Company.

Teledyne's 500nm InP HBT process provides four-metal layer stacks for passive elements of capacitors and inductors including various transmission-lines [29, 30]. As shown in figure 2.2, the top metal (MET4) has a thickness of 3 μm, the second and third metals are 1 μm thick, and the bottom (MET1) is 0.8 μm thick. Each metal is separated by benzocyclobutene (BCB) dielectric ($\epsilon_r = 2.7$) material with a thickness of 1 μm and connected by vias. Using the limited four metal layer stacks, 50 Ω transmission lines and 50 Ω resistor terminations have been used for high

speed circuit-to-circuit interconnections, and dielectric separations of more than 3 μm have been used for proper 50 Ω characteristic impedance with relatively wide metal widths for less conductor loss, i.e. MET1 as ground and MET4 as signal line or vice versa. For the complicated mixed IC designs that have many signal and supply lines, MET3 is used as ground and MET1 is used as the high speed signal lines, while MET4 is used for power suppy lines to avoid line crosses. Generally, all interconnections in IC designs have been characterized using ADS electro-magnetic (EM) simulations; the EM simulation setup is explained at the end of this chapter.

2.2 Transmission-lines and Broadband Interconnections



(a) (b) (c)

Figure 2.3: Three different types of transmission lines in IC designs. Microstrip transmission lines (a), co-planar waveguide (CPW) transmission lines (b), and slot-type transmission lines (c).

In high speed IC designs, transmission-lines are generally used in circuit-to-circuit interconnections and matching networks [31–33]. In the limited metal layer stacks, three representative transmission lines are shown in figure 2.3. Figure 2.3

(a) is a micro-strip transmission line which has a top signal-line and a bottom wide ground-plane or vice versa, and this structure is the most popular transmission line because of its well-defined structure, superior high frequency response and easy implementation in ICs. The characteristic impedance of the line is determined by the ratio of width and height. Figure 2.3 (b) is a co-planar waveguide (CPW) transmission line which consists of two ground planes on both sides of a signal line. This line is implemented on the same plane and this characteristic is good for IC design if the IC process only provides a limited number of metal layers. The characteristic impedance is set by the spacing between a signal line and the two ground planes, and the width of the signal line. However, the two ground planes have to be shorted at the edge of the grounds to prevent excitation of parasitic slot modes. Figure 2.3 (c) is a slot-type transmission line which consists of one signal line and one ground plane. The characteristic impedance is determined in the same way as a CPW line, but the insertion loss may be serious if the signal line and ground are thin. At high frequencies, the current crowds at the edges of the signal line and ground.

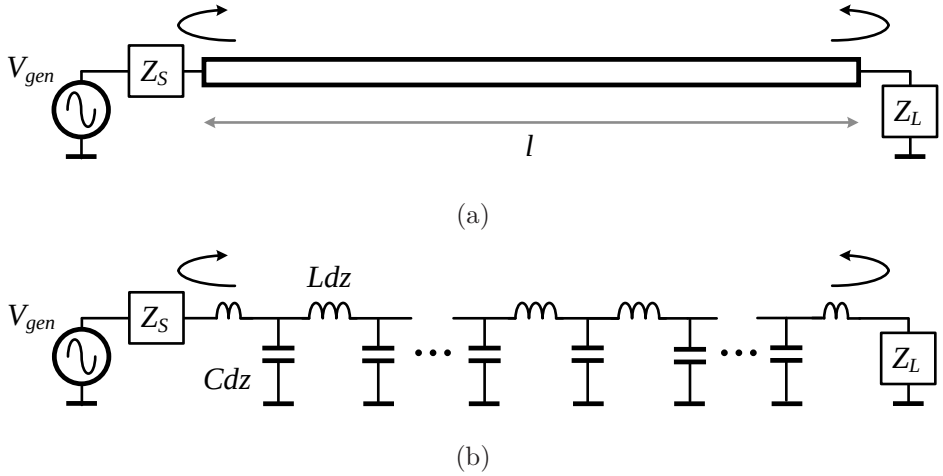


Figure 2.4: Transmission line theory. (a) Transmission line model with source and load impedance, and (b) distributed circuit model using lumped Ldz and Cdz (lossless).

The transmission lines are simply described by the figure 2.4 (a) and are analyzed with periodic distributions of series Ldz and shunt Cdz as shown in figure 2.4 (b). Using nodal analysis, the voltage and current in the transmission lines are extracted as

$$\begin{aligned} dV/dz &= -L(dI/dt) \\ dI/dz &= -C(dV/dt) \end{aligned} \tag{2.1}$$

$$\begin{aligned} V(z,t) &= V^+(t - z/v) + V^-(t + z/v) \\ I(z,t) &= V^+(t - z/v)/Z_0 - V^-(t + z/v)/Z_0 \end{aligned} \tag{2.2}$$

where $Z_0 = \sqrt{L/C}$ and $v = 1/\sqrt{LC} = c/\sqrt{\epsilon_{r,eff}}$. Forward and reverse waves propagate, and reflection and transmission will occur. V^+ and V^- are voltages in forward and reverse waves, respectively, and I^+ and I^- are currents in forward and reverse waves, respectively. Depending on the source and load impedance,

the ratio of the forward and reflective waves is given by the reflection coefficient Γ, defined as:

$$V^- = \Gamma_l V^+$$
$$V^+ = \Gamma_s V^- + T_s V_{gen} \tag{2.3}$$

where $\Gamma_l = (Z_l/Z_0 - 1)/(Z_l/Z_0 + 1)$, $\Gamma_s = (Z_s/Z_0 - 1)/(Z_s/Z_0 + 1)$ and $T_s = Z_0/(Z_s + Z_0)$. For the total line length l_{length}, if the line length is short, the transmission line can be simplified as a lumped component, and the total capacitance C_{length} and inductance L_{length} are

$$C_{length} = \tau/Z_0$$
$$L_{length} = \tau \cdot Z_0 \tag{2.4}$$

where $\tau = l_{length}/v$. The loss term $e^{-\alpha z}$ in the transmission line due to finite metal conductivity ($\sigma_{gold} = 4.10 \times 10^7\ S/m$) is neglected here.

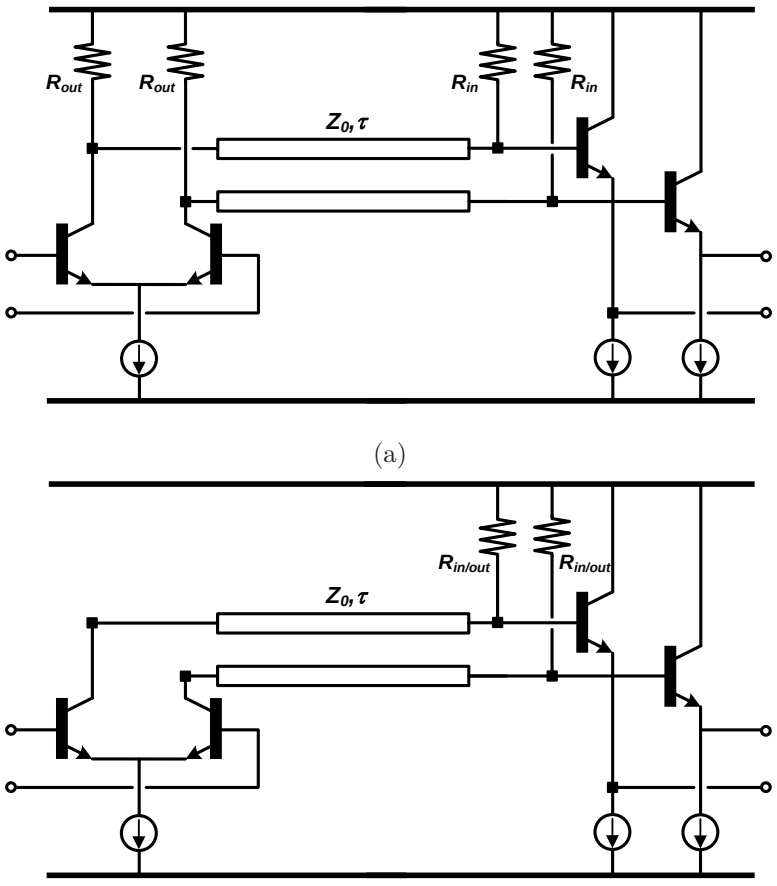


Figure 2.5: Circuit-to-circuit interconnection using transmission lines. (a) Double 50 Ω terminations on the output of the first stage and input of the second stage to minimize reflections and keep high speed interfaces (power consumption is greater than for a single termination), and (b) a single 50 Ω termination on the input of the second stage only. The reflection occurs in the output of the first stage.

In order to minimize reflections and enable high speed interconnections, 50 Ω transmission lines with 50 Ω terminations are used as examples in figure 2.5. Figure 2.5 (a) shows a double terminated circuit-to-circuit interconnection, and 50 Ω resistors are loaded at the outputs of the first stage and used at inputs of the second stage to minimize reflections for both sides. This is good for structures which

have relatively long interconnection lengths, but power consumption is doubled. On the other hand, figure 2.5 (b) is a single-terminated circuit-to-circuit interconnection, and 50 Ω resistors are only used at the inputs of the second stage with transmission lines. This is good for the structure as the interconnection length is relatively short, leading to negligible reflection at the output load. As mentioned above, when the transmission line length is short, the lines are approximated as lumped components C_{length} and inductance L_{length}. This capacitance C_{length} can contribute a switching speed and its power dissipation in logic switches. Therefore, the line length has to be minimized to minimize both reflection and power consumption. A high impedance interface, instead of 50 Ω, may be a good approach in terms of the power consumption (though not for bandwidth).

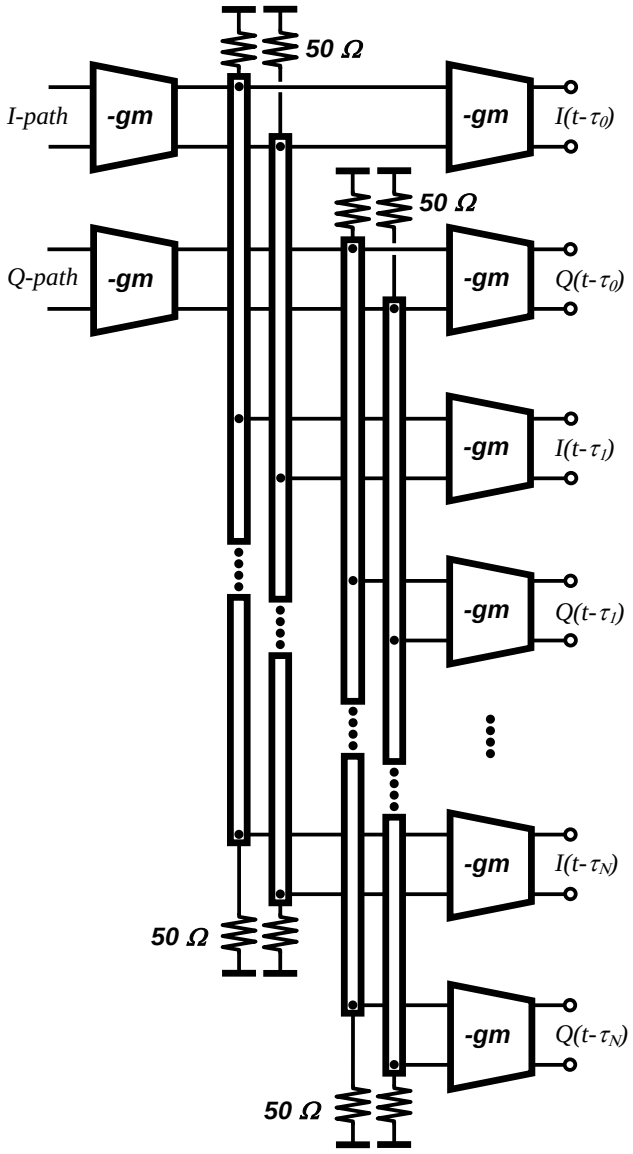


Figure 2.6: Bus-type broadband signal distributions using transmission lines. Two g_m-block outputs are double-terminated at the input of the first g_m-block and the input of the last g_m-block. The voltage signals with different delay are transmitted to each g_m-block.

Using this transmission line and termination concept, broadband input signals can be efficiently distributed to multiple paths as shown in figure 2.6. Figure 2.6

shows bus-type signal distributions with double-terminated structures (figure 2.5), and the periodic g_m-blocks have input delayed voltage signals $V_{OUT}e^{j\omega\tau}$ for each g_m-blocks and equally distributes the voltage and power. If the length of transmission lines are long and signal frequency is high, the conductor losses at longer delay should be considered. This structure has been used in the multi-channel WDM receiver ICs designs.

2.3 High-speed Amplifier ICs

2.3.1 Simple g_m-block Amplifier

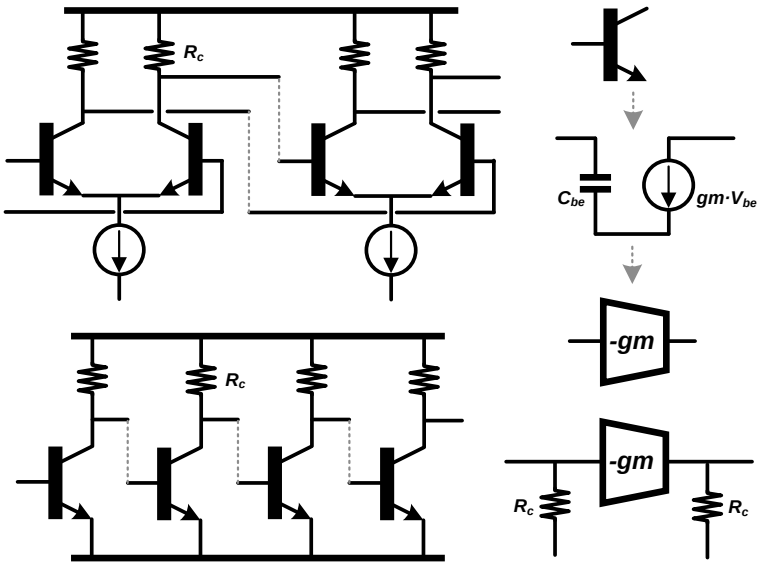


Figure 2.7: g_m-block amplifiers: differential-type on the top and single-ended type on the bottom. In the right section, a bipolar junction transistor (BJT) has been modelled as a simple trans-conductance (g_m), a circuit block as a simple block, which are terminated by shunt resistors at both the input and output.

One of the simplest possible amplifier circuits is a g_m-block resistively loaded amplifier as shown in figure 2.7 and it consists of two differential pairs with load resistors and current sources at the tail. In the following designs, bipolar junction transistors (BJTs) are simply modelled as voltage-controlled current-source, represented as g_m trans-conductance blocks. This amplifier has the voltage gain V_{out}/V_{in} given by

$$V_{out}/V_{in} = -g_m \cdot R_c \tag{2.5}$$

where g_m the trans-conductance of the transistor is

$$g_m = qI_c/(nKT) = I_c/(nV_T) \tag{2.6}$$

where I_c is collector current, V_T is the thermal voltage and n is the ideality factor ($n = 2.2$ in 500 nm InP HBTs at low current density condition of 2.4 mA/μm^2). The gain of the g_m-block amplifier simply increases in proportion to collector current. The bandwidth of the amplifier is

$$f_{3-dB} = 1/(2\pi R_c C_{be}) \tag{2.7}$$

where C_{be} is an input base-emitter capacitance which is derived as

$$C_{be} = g_m/(2\pi f_\tau) \tag{2.8}$$

where f_τ is the unity current gain cutoff frequency of the transistor. Therefore, if the gain increases by the increasing the collector current and the trans-conductance, the bandwidth decreases. In order to have broadband performance, single or double 50 Ω terminations with 50 Ω transmission lines have been used for high speed amplifier circuits. Due to its simple configuration, I have used

the modified g_m-block structure (shown in section 2.3.4 and 2.4.1) for the limiting amplifier chains and buffer amplifiers in ICs for homodyne and heterodyne OPLLs and WDM receiver ICs.

2.3.2 Resistive Feedback Amplifier; In/Output Matching and Bandwidth Enhancement

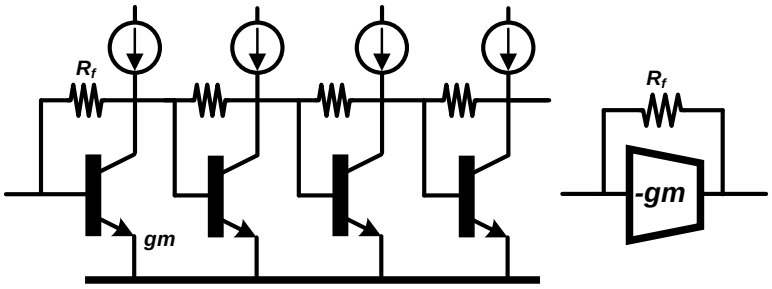


Figure 2.8: Resistive feedback amplifiers for broadband input and output termination condition and higher f_{3-dB} performance.

Resister feedback amplifiers (RFAs) have been also widely used as linear amplifiers with the good characteristics of input and output to 50 Ω matched conditions and higher gain bandwidth product. The circuit schematic of g_m block with feedback resistor R_f is shown in figure 2.8. In resistive feedback amplifiers, the transconductance g_m and feedback resistor R_f are determined by the desired voltage gain A_v and the desired input output impedances $Z_{in} = Z_{out} = 50\ \Omega$. The required g_m of the transistor and the feedback resistor R_f are

$$g_m = (1 - A)/R_{in/out}$$
$$R_f = (1 - A) \cdot R_{in/out}. \tag{2.9}$$

It can also be shown that the resistive feedback amplifier has a bandwidth of

$$f_{3-dB} = 2f_\tau/(1-A). \tag{2.10}$$

Compared with the g_m-block amplifier, the resistive feedback amplifier has nearly doubled the bandwidth. For a given gain, the resistive feedback amplifier requires less g_m and therefore the transistor cell has less C_{be}, which then results in greater bandwidth. Due to this wide gain bandwidth and 50 Ω input and output characteristics, the resistive feedback amplifiers (Darlington-type with feedback R_f) are used as the trans-impedance amplifiers for the front circuits of the WDM receiver ICs and second versions of OPLL ICs. Under linear operating condition, these circuits have 50 Ω input and output impedances.

2.3.3 Cherry-Hooper $g_m - Z_T$ Amplifier; Broadband Limiting Amplifiers

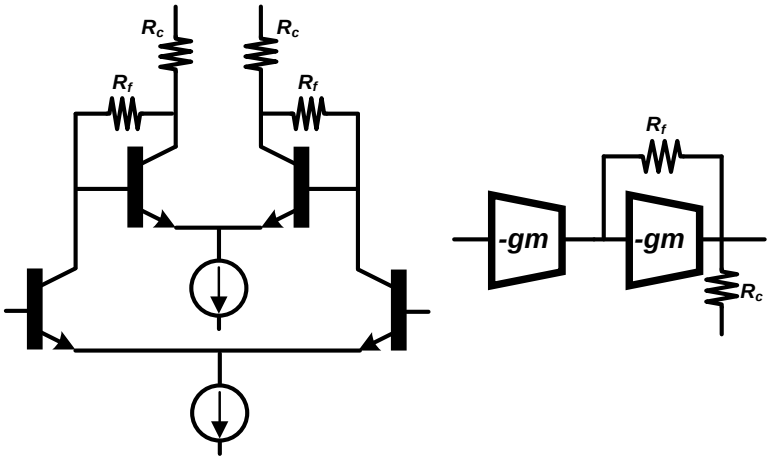


Figure 2.9: Cherry-Hooper amplifiers for broadband limiting amplifications. It consists of a g_m-block at the first stage and a resistive feedback block for the second stage.

Cherry-Hooper amplifiers (CHAs) have been generally used for broadband limiting amplifiers, i.e. optical receivers and high speed digital clock chains. The amplifiers consist of g_m-blocks at the first stage and resistive feedback amplifiers at the second stage as shown in figure 2.9. The input impedance of the second stage is very small as

$$R_{in,2} = (R_c + R_f)/(1 + g_{m2}R_c) \longrightarrow 1/g_{m2} \tag{2.11}$$

where $g_{m2}R_c \gg 1$ and $R_c \gg R_f$. The second stage has a transimpedance gain of

$$Z_{T2} = R_f(g_m - G_f)/(g_m + G_c) \longrightarrow R_f. \tag{2.12}$$

Therefore the Cherry-Hooper amplifier has an overall gain of

$$A_v = g_{m1} \times Z_T. \tag{2.13}$$

If the first stage is resistively terminated and second stage is resistive feedback, under large signal conditions stage 1 will limit before stage 2, ensuring that stage 2 stays in small signal operation, maintaining small input impedance and hence small RC charging times. The dominant time constant $a_1 = (C_{be,2} + C_L)/g_{m2}$, which, if C_L is negligible, is approximately $1/(2\pi f_\tau)$. The first g_m-block works as a limiting amplifier and the second resistive feedback stage works as a broadband linear amplifier.

2.3.4 Darlington-type Amplifiers

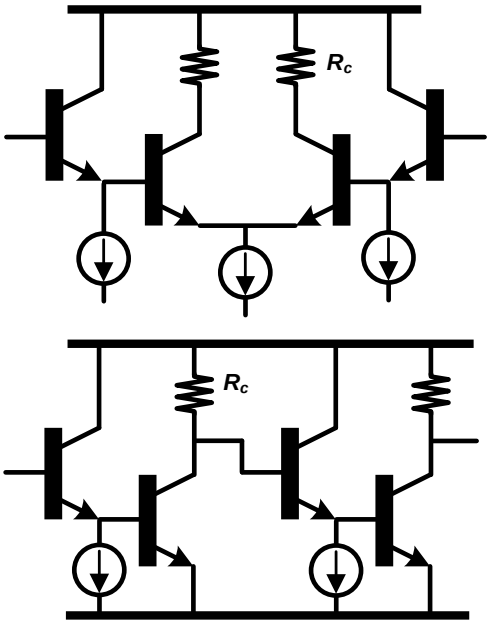


Figure 2.10: Darington Amplifiers for f_τ Doublers or voltage level shifters. It consists of an emitter follower and a g_m-block.

Darlington type transistors have been widely used because of the high current gain of $\sim \beta_1 \cdot \beta_2$ with high frequency bandwidth characteristic of $2f_\tau$ for broadband amplifiers [34]. I have used modified Darlington-types of the emitter follower with shunt resistive load (or current source) and separate collectors as a basic block for most of broadband amplifiers and digital ECL circuits [35, 36].

The modified Dalington-type amplifiers have a gain A_v of

$$A_v \approx g_{m2} \cdot R_c, \tag{2.14}$$

because of the emitter follower connection, where g_{m2} is the second transistor transconductance and R_c is a load resistor. The amplifier bandwidth can be

analyzed by the dominant time constant of

$$a_1 \approx C_{be,2}(R_{bb,2} + r_{e,1}), \tag{2.15}$$

where $C_{be,2}$ is the second stage input capacitor, $R_{bb,2}$ is the second stage parasitic base resistance, and $r_{e,1}$ is the first stage emitter resistance $(1/g_{m1})$. The first order time constant is now very small, and therefore, the charging time for $C_{be,2}$ is greatly reduced using the Darlington connection. On the other hand, the second order time constant is derived as

$$a_2 \approx C_{be,1}C_{be,2}R_{in}r_{e,1}, \tag{2.16}$$

where R_{in} is an input termination resistor. The Darlington structure may have a second-order damping issue, because of the series input capacitance $C_{be,1}$ with a broadband operation. The damping can be reduced using $R_{EE,1}$ shunt resistive load on the emitter follower. I have used the modified Darlington structure for broadband IC designs such as transimpedance amplifiers, g_m-block limiting amplifier chains, analog/digital mixers, and ECL digital logic gates.

2.3.5 High Frequency ECL-type Circuits

The high speed digital logic in this thesis uses emitter-coupled-logic (ECL). The ECL logic generally operates at high current density for high speed. Examples of (N)AND, XOR and static dividers are shown in figures 2.11, 2.12, and 2.13. Analysis of gate delay in ECL logic is similar to bandwidth analysis of the Darlington gain stages discussed earlier [35].

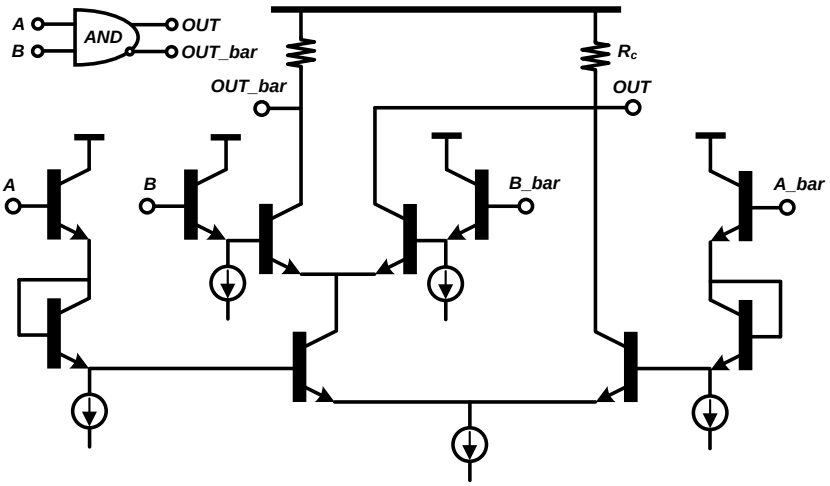


Figure 2.11: ECL-type AND and NAND gate schematic.

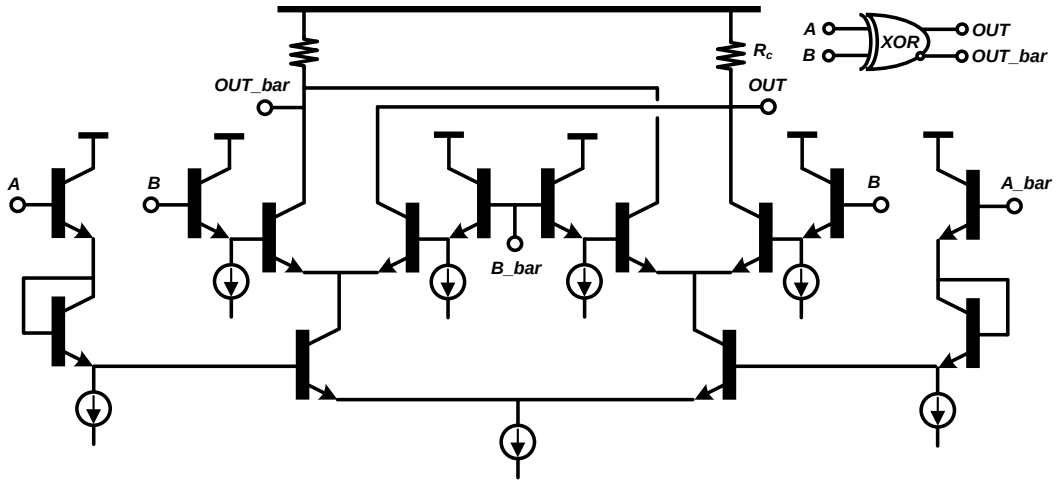


Figure 2.12: ECL-type XOR gate schematic.

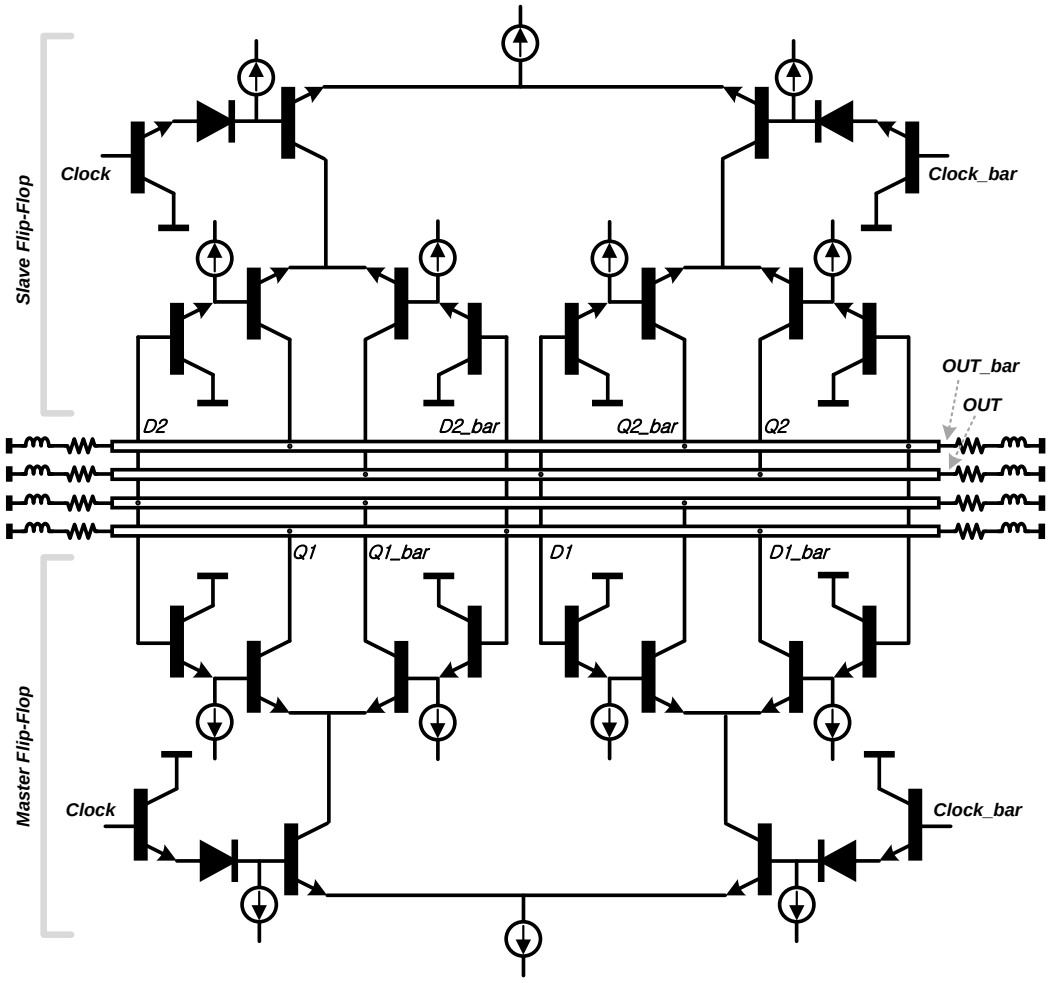


Figure 2.13: ECL-type static frequency divider schematic using two flip-flops of master and slave and distributed microstrip lines. Courtesy of Z. Griffith [27].

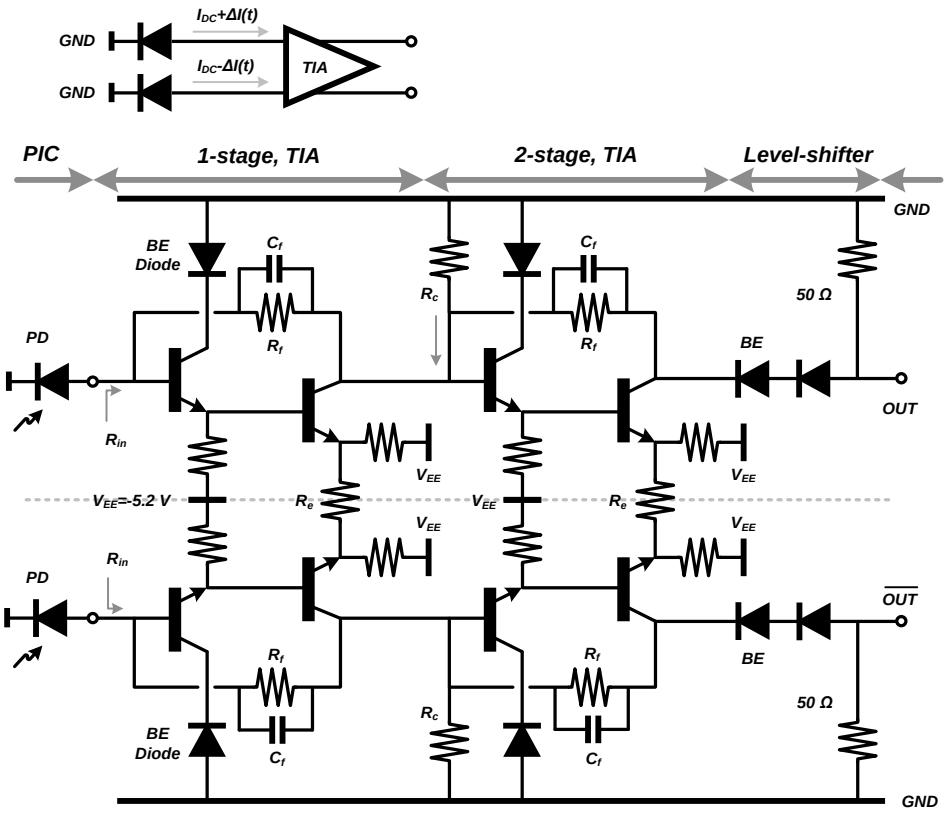
2.4 High-Speed ICs for Coherent Optical Communications

For our optical communication systems in the PICO project, many high speed electrical ICs were designed (with Eli Bloch). Four different systems have been

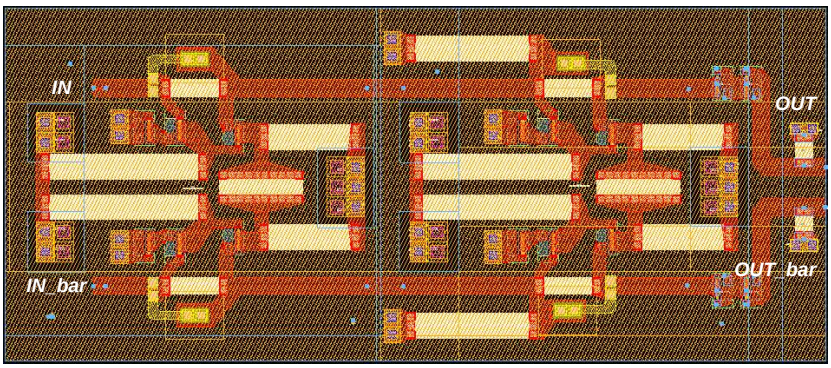
targeted including homodyne OPLL, heterodyne OPLL and single-chip multi-channel WDM receiver ICs. We also designed laser liewidth reduction ICs for A. Sivanathan. These systems all require various high-speed electrical circuits to enhance the optical system performances. In many cases, the electrical ICs were designed to tolerate a wide range of variation in the parameters of the optical components, so as to ease the optical experiments. E. Bloch and I designed various ICs using the Teledyne Science Corporation 500 nm InP HBTs technology mentioned earlier. In this section, several key high speed ICs and their circuit diagrams, layout, simulation and measurement results are described.

2.4.1 Trans-impedance Amplifiers (TIAs)

Extremely wideband transimpedance amplifiers (TIAs) were designed for the single chip WDM receiver ICs of chapter 5. The WDM receiver ICs need differentially operating trans-impedance amplifiers to amplify the outputs of the PIC balanced photodetector outputs. To extend the data bandwidth capacity, greater than 75 GHz TIA bandwidth is desired. Further, the TIA in the EIC should provide -2 V bias to the photodiodes, and the TIA should have 50 Ω input and output impedance to drive transmission lines. The resistive feedback amplifier and Darlington transistor topologies have been adopted because of their wide frequency band characteristics, 50 Ω input and output impedances and desirable voltage level shifting properties.



(a)



(b)

Figure 2.14: Designed two-stage differential trans-impedance amplifiers. (a) Detail TIA schematic, and (b) the layouts as a part of the WDM receiver IC. Courtesy of E. Bloch [25]

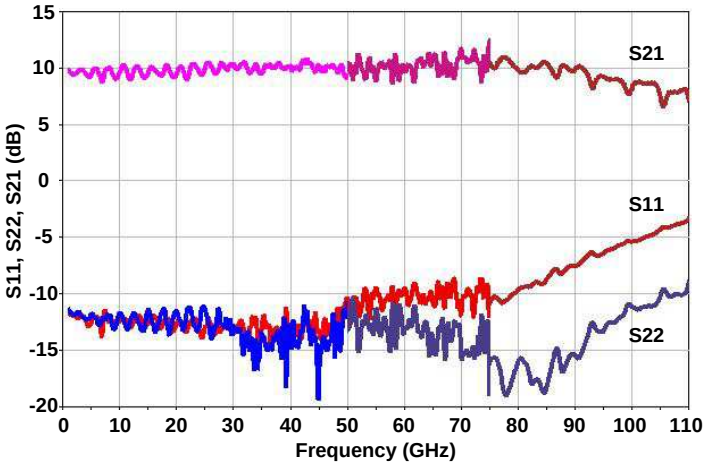


Figure 2.15: Measured TIA s-parameter results DC-to 110 GHz [25]

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Detailed two-stage TIA schematics are as shown in figure 2.14 (a) and the two stage core layout are shown in figure 2.14 (b). The two photodiodes are directly connected to the TIA inputs (in the experiments, short bonding-wires are used for PIC to EIC connections). A V_{EE} of -5.2 V with a total current of 70 mA are supplied for the TIA. The s-parameters for the TIA IC has been measured using three-network xanalyzer setups: 100 MHz - 50 GHz using an Agilent PNA-X network analyzer, 50 to 75 GHz using V-band OML heads with a DC-26 GHz network analyzer, and 75 - 110 GHz using W-band OML heads with the same DC-26 GHz network analyzer. The two-stage differential TIA exhibits 107 GHz 3-dB bandwidth, 9.8 dB gain, and S_{11} and S_{22} below -10 dB from DC-80 GHz (figure 2.15). In large signal measurements, the TIA shows -9.0 and -9.2 dBm 1-dB gain compression points at 10 GHz and 20 GHz respectively. In addition, pseudo-random data patterns (at input voltages of 128 and 134 mV_{pp}) has been

amplified by the TIA and the output eye diagrams (output voltage 357 and 372 mV_{pp}) have been measured. The signals were at 30 Gb/s and 44 Gb/s, and the PRBS sequences were $2^{31}-1$ data patterns long. The output data patterns show the same signal to noise ratio (Q factor) as the input signal (figure 2.16). Detailed descriptions for the TIA are in [25].

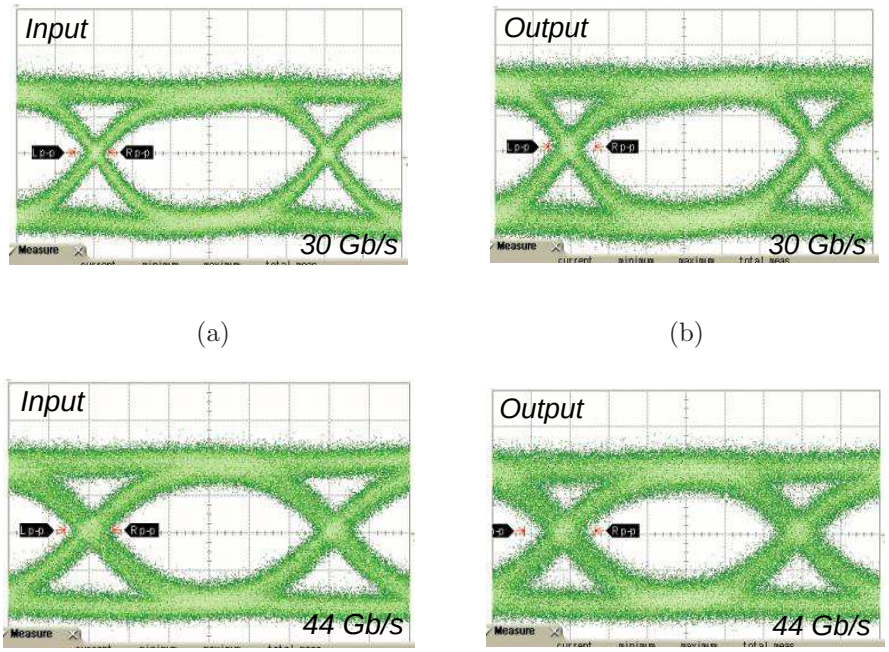
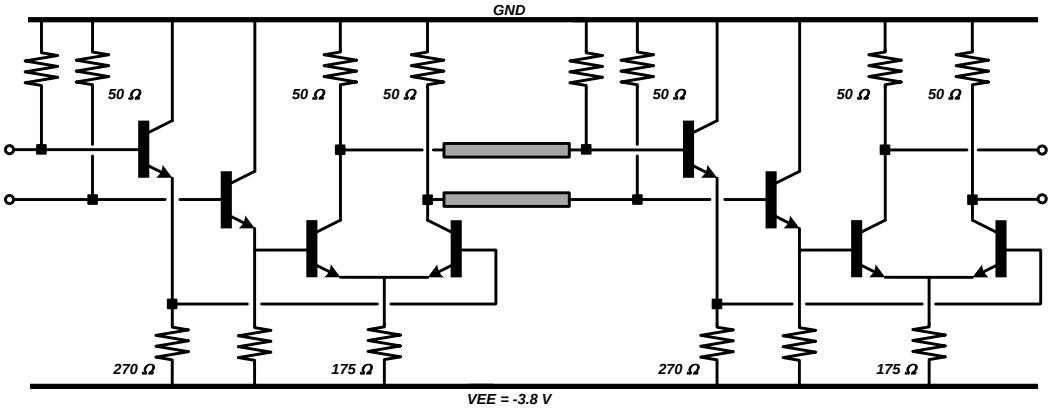


Figure 2.16: Measured eye inputs and outputs through the two stage TIA. Data PRBS ($2^{31}1$) modulated signals of 30 Gb/s and 44 Gb/s have been used for the measurements [25].

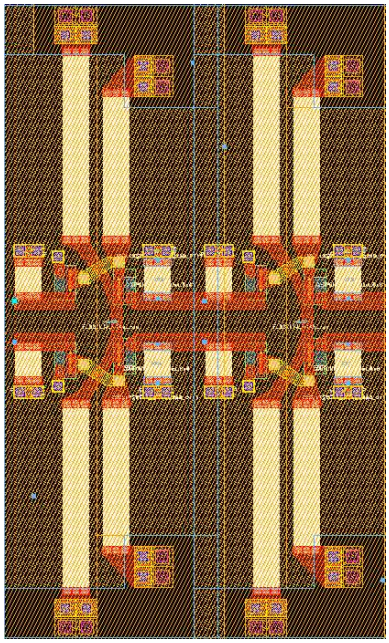
2.4.2 High-Gain Broadband Limiting Amplifiers

Limiting amplifier chains and buffer amplifiers have been designed using basic g_m-blocks and Darlington transistors. This limiting amplifier has been used for al-

most all circuits in the thesis, including homodyne and heterodyne OPLL limiting amplifier chains for digitizing input photodetector signals. Since the photocurrent signal amplitudes depend upon laser gains, input signal amplitudes, and optical waveguide loesses within the PICs variations which would change the OPLL characteristics, the limiting amplifier chains amplify and limit the signals to 0.3 V_{pp}, only storing phase and frequency information. These limiting amplifiers are also used for the WDM receiver ICs as buffer amplifiers in signal distribution. (figure 2.5).



(a)



(b)

Figure 2.17: Two-stage limiting amplifier chains using g_m-blocks and Darlington-transistors. (a) Two-stage schematic with double terminated circuit-to-circuit interconnections, and (b) its layouts as a part of the homodyne OPLL IC, heterodyne OPLL IC, and WDM receiver IC.

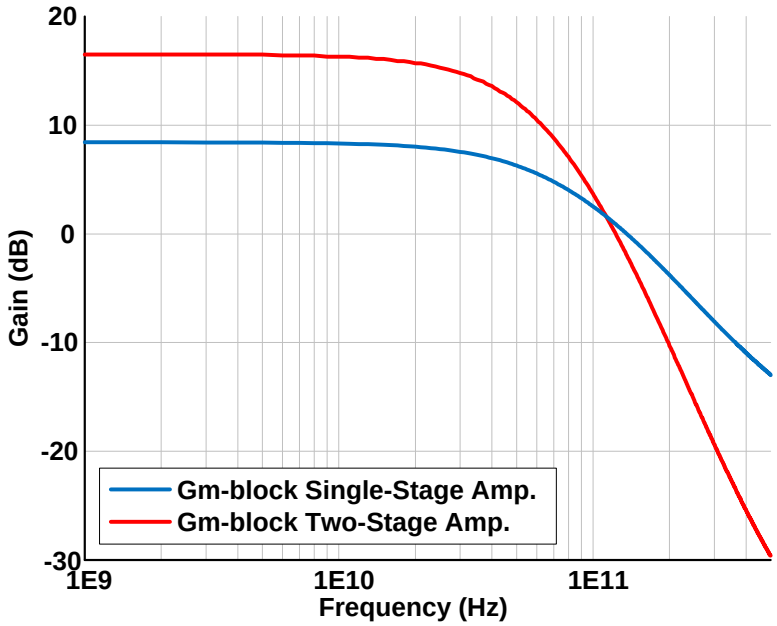


Figure 2.18: Simulation results for a single-stage and two-stage g_m-block limiting amplifiers. The simulation results show ∼8.6 dB gain with 75 GHz f_{3-dB} bandwidth.

Figure 2.17 shows 1-stage and 2-stage resistively-loaded Darlington differential amplifiers. 50 Ω shunt resistors to the ground are double terminated between the two stage amplifier's load and input with 50 Ω transmission lines. Simulation results for these are shown in figure 2.18. The single stage amplifier shows ∼8.6 dB gain with 75 GHz f_{3-dB} bandwidth.

2.4.3 Cherry-Hooper Amplifiers

Broadband limiting amplifiers using the Cherry Hooper amplifier were also designed. This amplifier and the four-stage amplifier chains are used in the WDM receiver ICs for quadrature local oscillator (LO) clock (square-wave) signals and their signal distributions. We targeted LO frequencies up to 70 GHz using the

500 nm InP HBT process. Unlike the Cherry Hooper amplifier shown earlier, this amplifier uses an emitter follower in the negative feedback path. Further, the input g_m-block uses 20 Ω emitter degeneration shunted by 80 fF. This extends the amplifier bandwidth without excess gain peaking. This reduce the extrinsic transconductance G_m of the stage to

$$G_m = \frac{g_m}{1 + g_m \cdot R_{deg}/2}. \tag{2.17}$$

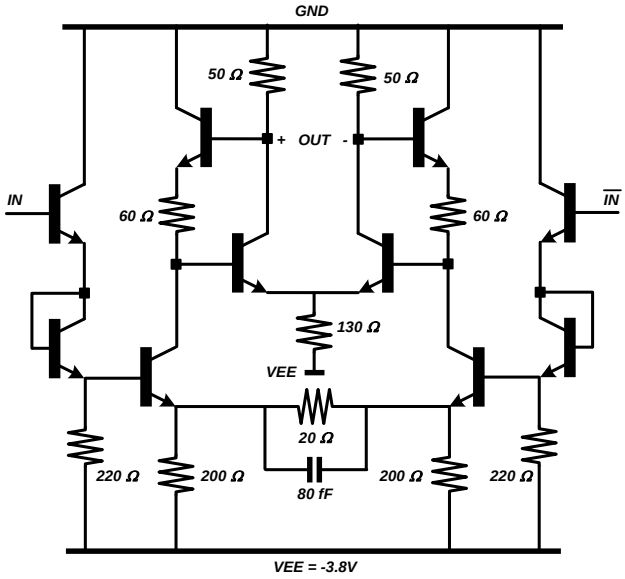
Further, the transimpedance of the second stage is set to 60 Ω. Therefore, following equation 2.15, the voltage gain of this Cherry Hooper amplifier is

$$V_{out}/V_{in} = g_m \times Z_T, \tag{2.18}$$

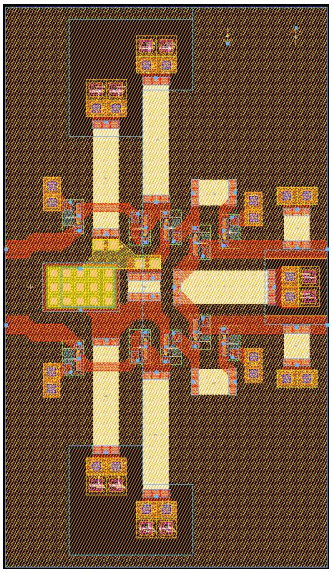
where the voltage gain is 3.3:1 (10.37 dB). The first order time constant for the Cherry Hooper amplifier is

$$a_1 = (C_{be,2} + C_L)/g_{m2}. \tag{2.19}$$

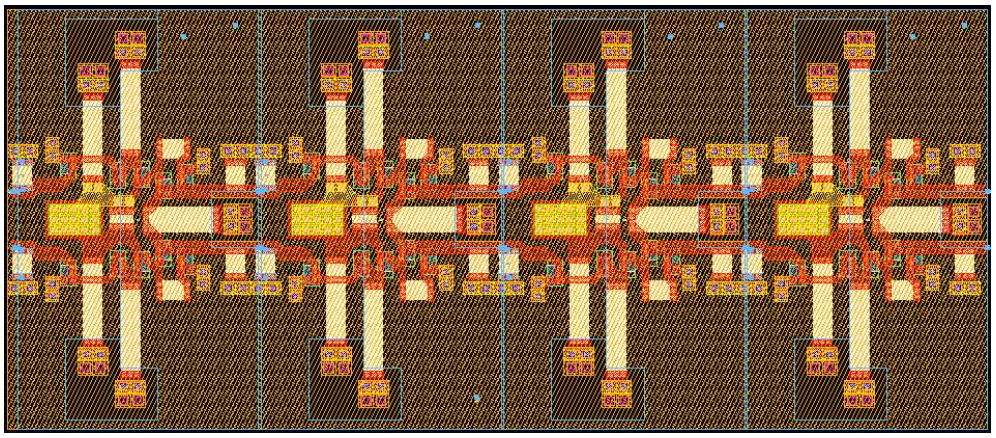
If the C_L is to be similar to the capacitance $C_{be,2}$, the Cherry Hooper amplifier has a dominant pole at ∼150 GHz.



(a)



(b)



(c)

Figure 2.19: Modified differential Cherry-Hooper Amplifier chains for the WDM receiver LO limiting amplifier paths. (a) A single-stage schematic with the degeneration resistor of 20 Ω with high frequency peaking capacitor of 80 fF, (b) a single stage layout, and (C) the layout for the four-stage Cherry-Hooper amplifier chains.

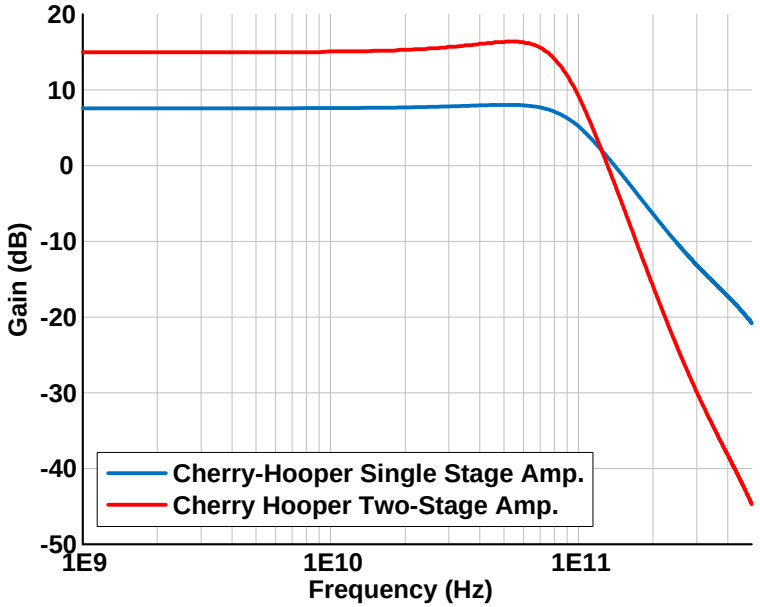


Figure 2.20: Simulation results for a single-stage and two-stage Cherry-Hooper amplifiers. Bandwidth has been extended because of high frequency peaking using the degeneration resistor 20 Ω with 80 fF capacitor.

The schematic of the modified Cherry Hooper amplifier cell is shown in figure 2.19 (a), its single stage layout is shown in (b) and four stage limiting amplifier chains are shown in (c) [37]. For the amplifiers, the characteristics of the single stage Cherry Hooper amplifier and two stage Cherry Hooper amplifier were simulated (figure 2.20). The gain performance is slightly degraded because of voltage dividing at the output load of 50 Ω, and the gain was extended using capacitor peaking with a degeneration resistor, as mentioned above.

2.4.4 Analog Single-Sideband Mixers

A broadband analog single sideband mixer was designed using a Gilbert-cell type mixer as the basic mixer component within a Weaver single-sideband topol-

ogy [38]. This single sideband mixer has been used for a core block of WDM receiver ICs that down-converts RF sub-carriers of either positive or negative frequency offset relative to the optical carrier. This doubles the data capacity and is therefore a key component. A different, digital single sideband mixer was used in the heterodyne OPLL to provide desired positive or negative frequency offsets.

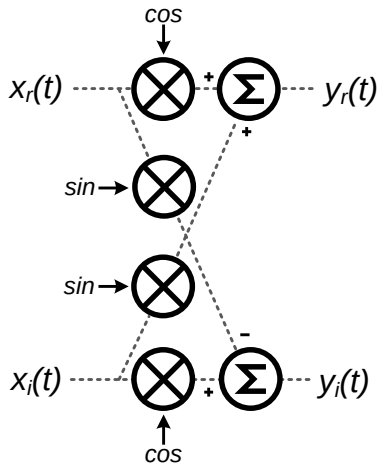


Figure 2.21: Weaver-type broadband analog single sideband mixer. Block-level single-sideband mixer architecture using four mixers with sin and cosin LO signals.

The Weaver single sideband mixer concept is shown in figure 2.21. Input data $x_r(t)$, the real or in-phase signal I', $x_i(t)$, the imaginary or quadrature-phase signal Q', are applied, as are sine and cosine local oscillator signals. Input carrier signals of $x_r(t)$ and $x_i(t)$ are defined as

$$x_r(t) = cos(2\pi f_c t)$$
$$x_i(t) = sin(2\pi f_c t), \tag{2.20}$$

where f_c is the carrier frequency. The two local oscillator (LO) sine and cosine

signals are also defined as

$$cos(2\pi f_{LO}t)$$
$$sin(2\pi f_{LO}t), \tag{2.21}$$

where f_{LO} is the LO frequency. Based on figure 2.21, the outputs of $y_r(t)$ and $y_i(t)$ are

$$\begin{aligned} y_r(t) &= 1/2[cos(2\pi(f_c - f_{LO})t)] + 1/2[cos(2\pi(f_c + f_{LO})t)] \\ &+ 1/2[cos(2\pi(f_c - f_{LO})t)] - 1/2[cos(2\pi(f_c + f_{LO})t)] \\ y_i(t) &= 1/2[sin(2\pi(f_c - f_{LO})t)] + 1/2[sin(2\pi(f_c + f_{LO})t)] \\ &+ 1/2[sin(2\pi(f_c - f_{LO})t)] - 1/2[sin(2\pi(f_c + f_{LO})t)], \end{aligned} \tag{2.22}$$

The single sideband mixer outputs have only down-conversion $f_c - f_{LO}$ outputs. If the input frequency is $-f_c$ or different output connections, then the single sideband mixer has only up-conversion $f_c + f_{LO}$ outputs. If the two different channel data are at both positive and negative frequency of f_c, the single sideband mixer can select only positive or negative channel data. The broadband single sideband mixers are designed for greater than 30 dB alternate sideband suppression (31.6:1 signal to image rejection ratio). The circuit diagram of the mixer is shown in figure 2.22 and the corresponding mask layout is shown in figure 2.23. x_r, x_i, y_r, and y_i are correspond to I', Q', I-data, and Q-data in the schematic and layout, respectively.

figure 2.22

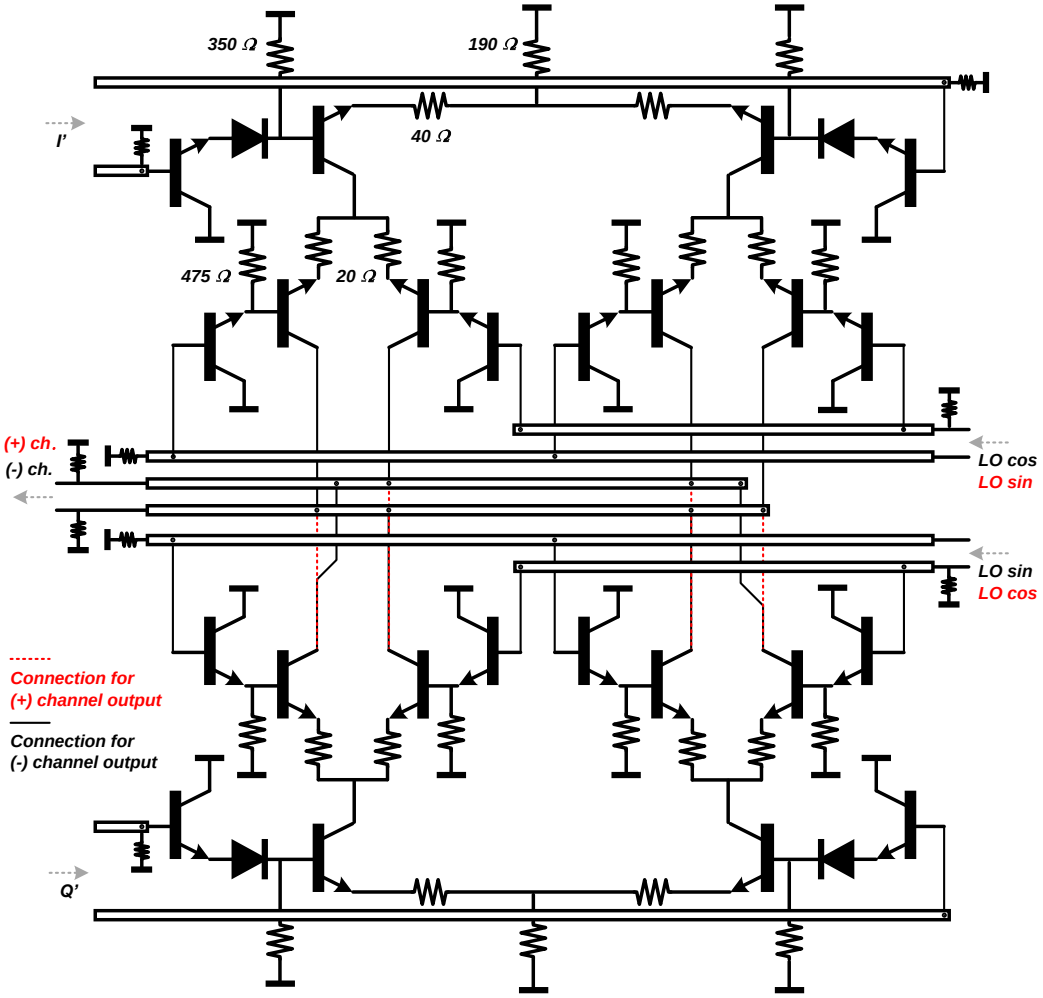


Figure 2.22: A schematic for the Weaver-type broadband analog single sideband mixers.

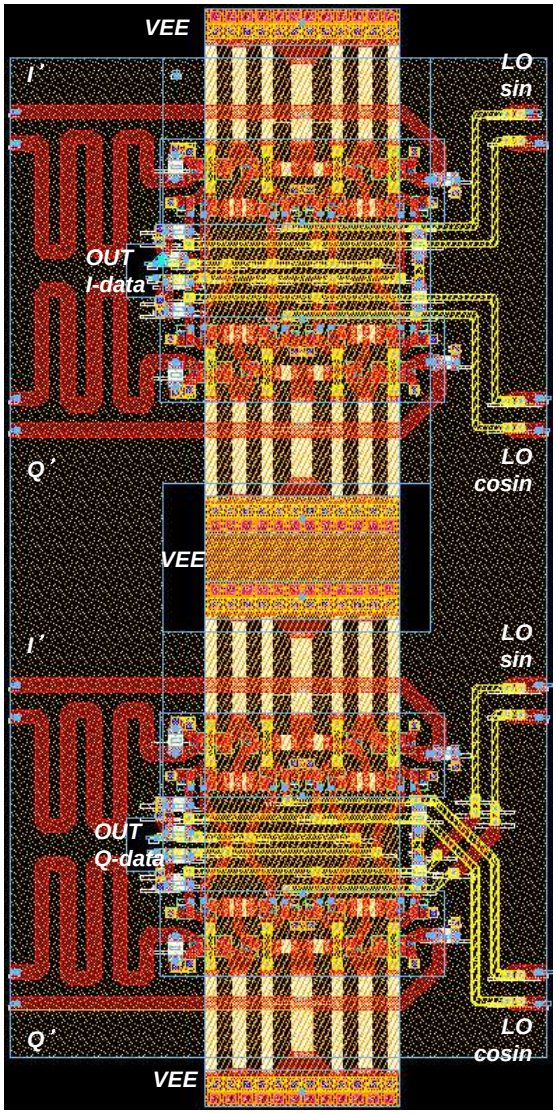


Figure 2.23: A layout for the Weaver-type broadband analog single sideband mixers. The upper section is for I-data outputs and the lower section is for Q-data outputs.

Using this core cells (figure 2.21) with buffer blocks, the both up and down conversion single sideband mixers were designed and simulated. The single sideband mixers exhibited >25 dB rejection ratio over ∼50 GHz (figure 2.24) including full EM simulations for all interconnects.

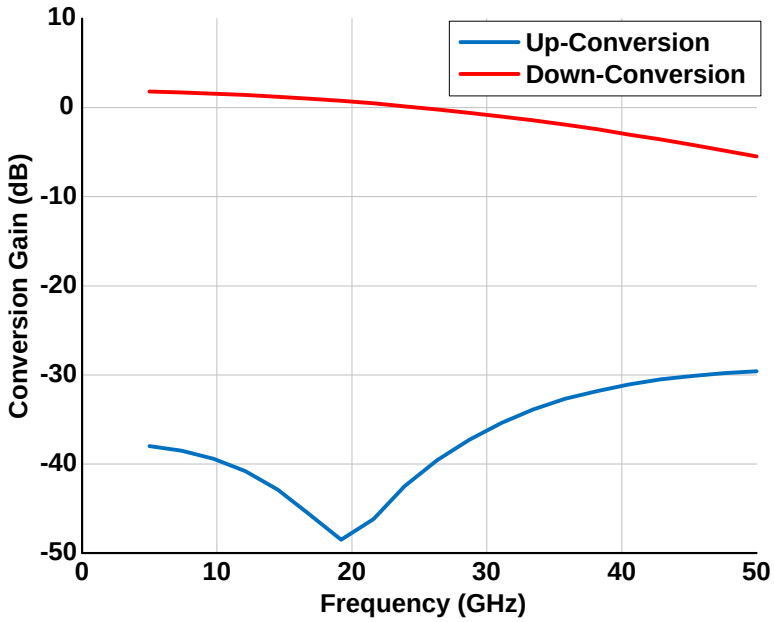
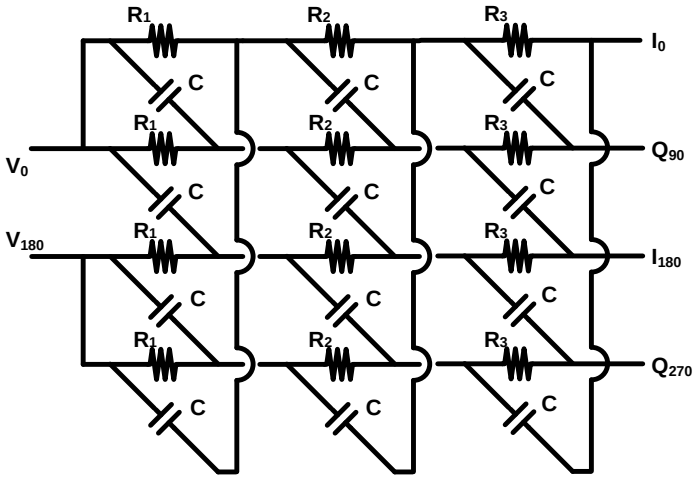


Figure 2.24: Simulation of the single sideband suppression ratio. Weaver single sideband mixer as a function of LO frequency. The simulations use EM models for all interconnects.

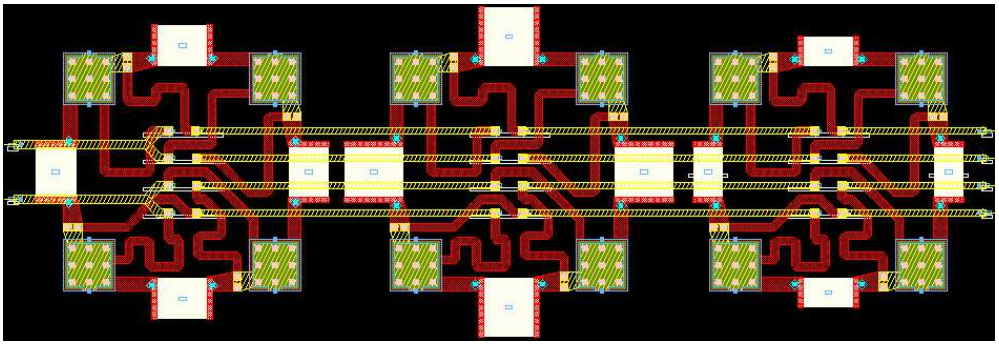
2.4.5 Poly-Phase Filter

A three stage broadband poly-phase filter has been designed to generate the quadrature LO signals needed for the single sideband mixers in the WDM receiver ICs. Theory of such filters is given in [39, 40], while the circuit diagram is in figure 2.25. In the circuit diagram of figure 2.25, with capacitances 68 fF and resistance 44.1 Ω, the center frequency (in rad/sec) $\omega_0 = 2\pi \times 37.5$ GHz satisfies the relationship $RC\omega_0 = 1$. The cascaded three section poliphase filters have slightly different values of $RC\omega_0 = 1$ in order to obtain close to a 90 degree phase shift over a wide frequency range. The optimized mask layout is shown in figure 2.25 [40]. The simulation results including EM simulation of interconnects

show less than 0.5 degree phase difference over 30 GHz (26-57 GHz) as shown in figure 2.26.



(a)



(b)

Figure 2.25: A three-stage poly-phase filter schematic (a) and layout (b) for quadrature LO signals.

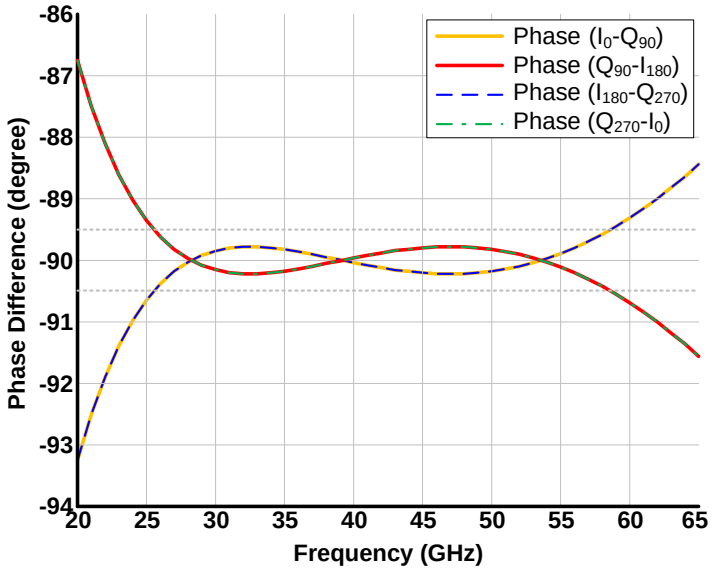


Figure 2.26: Simulation phase difference results for three-stage 37.5 GHz poly-phase filter including EM-simulation of interconnects. The phase error is less than 0.5 degree over a 26-57 GHz bandwidth.

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Chapter 3

Homodyne OPLLs for Short-Link Optical Communications

One of the main goals of this research was to demonstrate stable optical phase locked loops (OPLLs) having wide loop bandwidths, and therefore small loop propagation delay. Through this work, we demonstrated stable OPLLs and many results in data communications [1–7].

I collaborated with M. Lu and E. Bloch from March 2012 to September 2012 to demonstrate stably operating OPLLs. Through this research, we used integrated photonics and integrated electronics to build OPLLs with very low loop delay, which was the key weakness of previous published OPLLs [1–4,8–16]. Using our homodyne OPLL, as a key achievement, we demonstrated a 40 Gb/s coherent optical receiver using an optical Costas loop [17–19]. This was the first highly integrated optical Costas loop that has high loop bandwidth, which permits the OPLL to track fast laser phase variations, and that the OPLL was compact and simple.

The homodyne OPLL was realized on a compact AlN single carrier board, and all components of 1) the photonic integrated circuit (PIC) designed by Mingzhi Lu [4, 20], 2) the electrical integrated circuit (EIC) designed by Eli Bloch [6, 7], and 3) the loop filter are highly integrated within a compact size of $10 \times 10\ mm^2$. To ensure stable operation, several key concepts were implemented: 1) limiting amplifier chains and binary phase and frequency detection improve the OPLL stability against to the external variations such as photocurrent fluctuations and temperature variations. 2) Integration of both electronic and photonic circuits reduce the interconnection delay while implementing multi-stage amplifications and phase and frequency detection functions of in a small IC footprint. 3) A dual-path (feed-forward) loop filter minimizes effective loop delay for higher frequencies and significantly extends the loop bandwidth.

In this chapter, I will describe design of the homodyne OPLL using Costas loop. I will also describe experiments which demonstrate the OPLL performance and which demonstrate the OPLL recovering BPSK data. I will also describe design of the high speed integrated circuits using InP HBTs, will describe the simulation of the feedback loops using Matlab and Simulink.

3.1 Motivation and Background

Since 1980s, coherent fiber optical communication has been interested because of long signal reach and high data capacity [5, 8, 21]. To increase the reach, PSK homodyne coherent detection was widely studied in 1980-1990s because of its superior receiver sensitivity, and its capability for multi-bits/symbol transmission

using multi-level I-Q constellations, i.e. QPSK, 8-PSK, 16-QAM and 64-QAM. However, the interests in homodyne coherent detection in 1990 declined due to the Erbium-doped fiber amplifier (EDFA), which significantly extended the signal reach without requiring coherent detection. Further, with the introduction of wavelength division multiplexing (WDM), the communication bit rates could be increased by the number of wavelength division channels [8, 21].

Recently, coherent detection has become a topic of interest again because of the exponentially increasing demands on data capacity (high spectrum-efficiency) [22, 23]. Intradyne detection, a form of digital coherent detection, uses analog-digital-convertors (ADCs), and digital signal processing (DSP) to recover the carrier. Intradyne system also uses DSP to correct for polarization-mode dispersion (PMD) and chromatic-mode dispersion (CMD) to increase both the communication distance and data capacity [24–26]. Intradyne detection technique is widely used in long-haul optical communications.

In short distance optical communications, i.e. Ethernet accesses, metropolitan links, data-cener links, PMD and CMD are negligible, and the ADCs and DSPs used in the intrdyne links would serve only to recover the phase of the transmitted optical signal. Such short-range links would be much cheaper if the ADC and DSP could be eliminated. Although intensity modulation and direct detection (IMDD), widely used in current short link optical communications, is simpler and lower-power than intradyne because if does not require ADC and DSP ICs, this short-link optical communication has limited spectral efficiency. Demonstrated intensity-modulated links include 100 Gb/s 4-PAM links using VSCEL transmitters and equalizers [27, 28]. As an alternative, homodyne detection based

on OPLLs can be a promising solution, because it has a simple configuration, high data rate per frequency bandwidth by QPSK and QAM modulations and high data rate per power consumption.

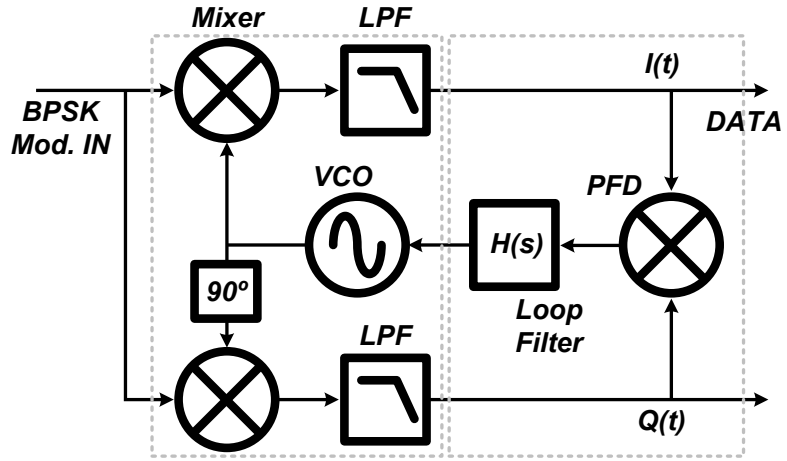
In the past, OPLL (Costas loop) based homodyne detections have been regarded as challenging because of long loop delay and laser linewidth. The size of optical circuits were composed of bulk components and implementations of many complicated electrical circuits, i.e. TIA, limiting amplifiers, phase and frequency detector, including a loop filter on a printed circuit board take a very long interconnection delay [8, 10]. This long loop delay limits the loop bandwidth, which determines frequency suppression ranges for LO laser phase / frequency noise and track-hold ranges for an input reference laser (a transmitted carrier). Due to these interconnection delays, an ultra-stable and narrow linewidth laser source, such as very narrow linewidth external cavity lasers [29–32] for both the LO and transmitted lasers, were required for stable OPLLs which had relatively narrow loop bandwidth.

Recently, many OPLL results have been reported; A homodyne OPLL using a high speed FET for a small delay loop filter with a loop bandwidth of 300 MHz [9], a heterodyne OPLL using an RF exclusive-OR (XOR) as a phase detector with loop delay of 1.8 ns [10], and a highly integrated heterodyne OPLL using an integrated single side band mixer and a phase frequency detector (PFD) with delay of 0.2 ns and closed loop bandwidth of 550 MHz [16] have been published. OPLL based coherent optical receivers have been also developed. Costas receivers using homodyne OPLLs with below 10 Gb/s [18, 19, 32–34], decision-driven loops including sub-carrier modulation scheme [35, 36], and a digital OPLL using a

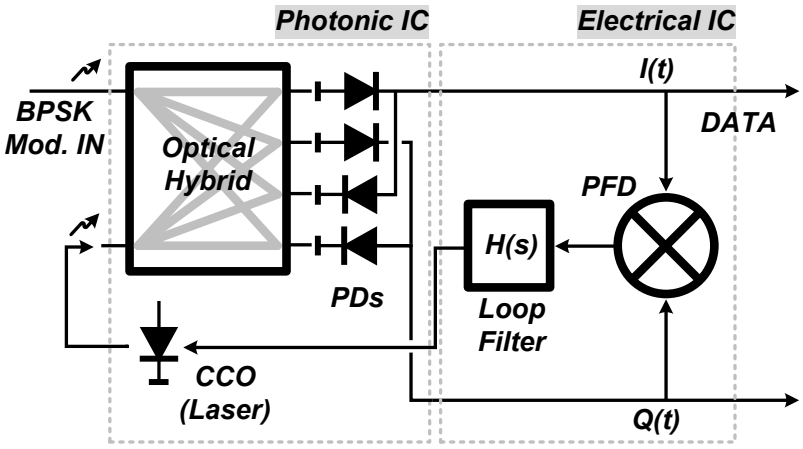
sampled $I - Q$ signals with slow DSP for homodyne reception of PSK 40 Gb/s [30] have also been published. However, the receivers still require a very narrow linewidth on the LO and transmitting lasers due to a narrow loop bandwidth, and they may need additional blocks such as VCO, MZM, optical filter, even ADCs and DSPs to recover the carrier signal.

In this chapter, I will show a stably working 40 Gb/s coherent optical receiver based on the homodyne OPLL (the Costas loop). In section 2, the basic Costas loop concept for both electrical and optical systems will be briefly explained. In section 3, all PIC and EIC devices are characterized and the feedback loop will be fully analyzed to optimize the OPLL systems with a novel loop filter design topology. In section 4 OPLL implementations and their experimental results will be described in detail. Mainly, the OPLL is realized within a compact size of 10 $\times$ 10 mm^2, and it exhibits a closed loop bandwidth of 1.1 GHz and loop delays of 120 ps. In addition, the digitally operating electrical circuits make the OPLL more robust against component variations, and the PFD extends phase-lock and frequency pull-in ranges. As a result, a stable OPLL and binary phase shift keying (BPSK) coherent receiver exhibits error-free (BER less than 10^{-12}) up to 35 Gb/s and BER less than 10^{-7} for 40 Gb/s are achieved.

3.2 BPSK Coherent Receivers Based on Costas Loops

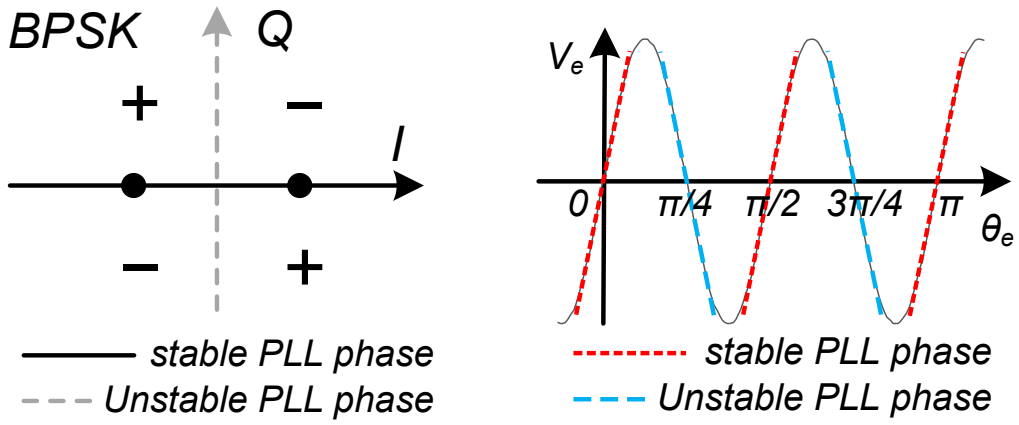


(a)



(b)

Figure 3.1: Costas loop receivers for BPSK modulated signals. The Costas loop using electrical components only (a) and the Costas loop using optical components (hybrid, PDs and laser) and electrical components (mixer as a PFD and loop filter)(b).



(a) (b)

Figure 3.2: Stable phase locked loop conditions. The stable conditions of 0 and 180 degrees in the $I-Q$ constellations (a), and the same results with (a) in the sinusoidal plot $sin(2\theta_e)$ of the voltage error V_e vs. phase error θ_e (b).

To design BPSK coherent detection based on homodyne OPLLs, we selected Costas loop concept as shown in figure 3.1. Such loops were widely used in 1970s and 1980s electrical communication prior to the widespread adoption of phase locked loop (PLL) frequency synthesizers [37]. This is well-known as simple and inexpensive phase synchronous receiver architecture and has a superior signal-to-noise performance. Many versions of the Costas loop have been applied for QPSK, 8-PSK and M-QAM modulation formats [38].

Figure 3.1 (a) shows general electrical circuit configurations of a Costas loop receiver for BPSK modulated signals [17]. As shown in figure 3.1 (a), this structure consists of voltage-controlled-oscillators (VCO), down-conversion mixers on I and Q paths, low-pass filters (LPF), XOR-type phase (also frequency) detector and loop filter. The VCO as local oscillator (LO) can track a transmitted carrier within binary phase modulated signals without losing locks. The Costas loop with $I-Q$

mixing keeps two stable phase lock conditions of 0 and 180 degrees. Therefore, the Costas loop can recover original BPSK data without the DSP which has a carrier phase and frequency estimation function.

Using its simple configuration, we can build an optical coherent detector using the Costas loop concept as shown in figure 3.1 (b). The optical Costas loop consists of optical components of a laser as an optical local oscillator (LO), optical hybrid and photodiodes, and electrical components of phase detector and loop filter. The optical components down-convert optical BPSK modulated input signals to the electrical domain with I and Q signals. The electrical components may requires high speed operations.

I will now explain the principles of both electrical and optical Costas loops. The input transmitted BSPK signal is defined as

$$TX(t) = m(t) \cdot cos(2\pi f_c t + \theta_{BPSK}) \tag{3.1}$$

where the BPSK data $m(t)$ has values of only ± 1, the carrier frequency is f_c, and the carrier phase is θ_{BPSK}. This transmitted signal is mixed with the LO signal $LO(t)$ of

$$LO(t) = 2cos(2\pi f_c t + \theta_{LO}) \tag{3.2}$$

where the LO phase is θ_{LO} (at present we assume that the LO frequency is the same as the carrier frequency). After the $TX(t)$ and $LO(t)$ are mixed, the $I(t)$ and $Q(t)$ signals are derived through the low path filters as

$$\begin{aligned} I(t) &= m(t) \cdot cos(\theta_e) \\ Q(t) &= m(t) \cdot sin(\theta_e) \end{aligned} \tag{3.3}$$

where the phase error is $\theta_e = \theta_{BPSK} - \theta_{LO}$. Then, $I(t)$ and $Q(t)$ are multiplied (mixed) by the XOR gate to extract the phase error

$$I(t) \cdot Q(t) = 1/2[m(t)]^2 \cdot sin(2\theta_e). \tag{3.4}$$

Since $[m(t)]^2$ in equation 3.4 is always 1 (the binary-PSK signal being ± 1), this $sin(2\theta_e)$ represents the measurement of phase error. Equation 3.4 is simply expressed as figure 3.2 using I and Q constellations (a) and voltage error vs. phase error (b). Equation 3.4 and figure 3.2 both show that the Costas loop has two stable phase-locked conditions of 0 and π in a single period 2π. The Costas loop will therefore operate with BPSK data without losing phase-lock. The BPSK data is recovered through the I-path. The phase of the BPSK data has a $\pm$ ambiguity, because of the two stable conditions of 0 and π, but this issue will be solved by differential encoding for input signals and differential decoding for output signal. This will be discussed in detail in the section of the data reception experiments.

In this section, I did not include loop delay and device parasitics in the OPLL (Costas loop) analysis. In the following sections, I will show each device characteristics and parasitics as loop parameters to build stable feedback loop systems (OPLL). Then, I will show our OPLL design procedures within the loop parameters.

3.3 Device Characteristics and OPLL Designs

A homodyne OPLL has been designed using the optical Costas loop concept as the schematics shown in figure 3.3. It consists of three main blocks of a photonic integrated circuit (PIC), an electrical integrated circuit (EIC), and a dual-path

loop filter. Each device has been carefully characterized through measurements and simulations, and considered in feedback loop designs for a stable and well-working OPLL.

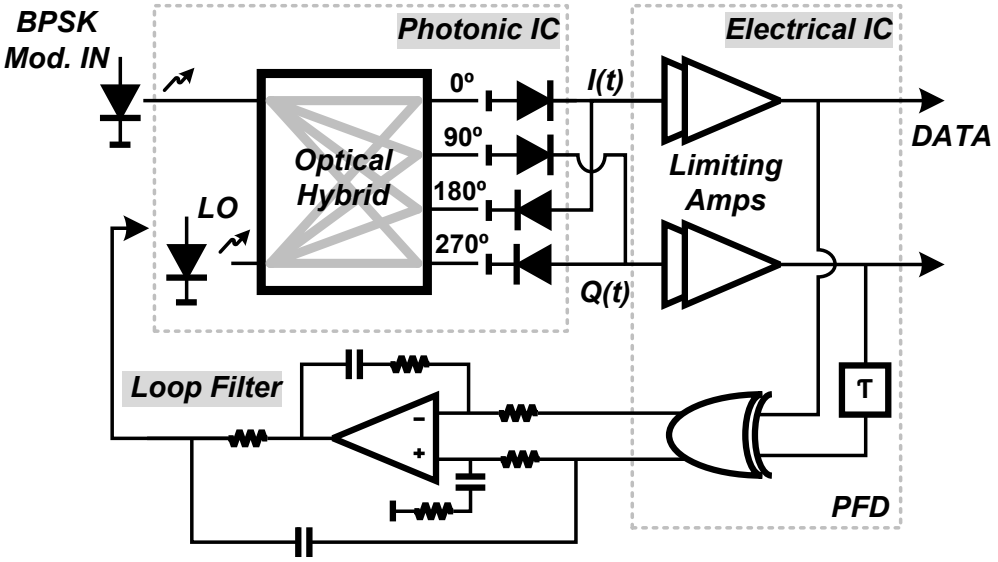


Figure 3.3: A concept schematic for a homodyne OPLL structure using a Costas loop which consists of three main parts of the PIC, EIC and loop filter.

3.3.1 Photonic Integrated Circuit

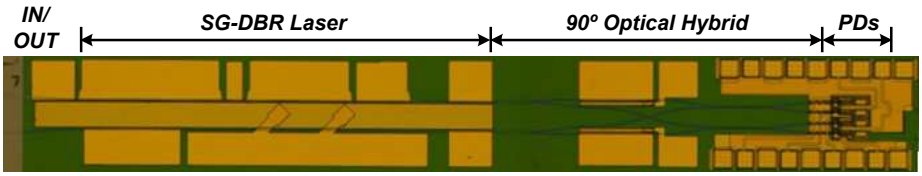


Figure 3.4: Photo image for the fabricated PIC in the UCSB facility, courtesy of M. Lu [4, 20].

The PIC (figure 3.4) is fabricated based on the InGaAsP/InP platform using the UCSB NNIN nano-fabrication facility. This PIC includes a widely tunable

sampled grating distribute Bragg reflector (SG-DBR) laser which can tune over a 40 nm wavelength span (>5 THz) by current injection into front and back mirrors and a phase tuning section diode. The PIC also has a 90 degree optical hybrid and four single-ended uni-traveling carrier (UTC) photodiodes for mixing the optical fields of input transmitted signal and optical LO signal and for down-converting quadrature ($I-Q$) photocurrents in the electrical domain. Detailed PIC process flows and device characteristics are explained in [4, 20]. In order to build a stable OPLL, I will describe the PIC device characteristics and its balanced detection operation using several equation steps [39].

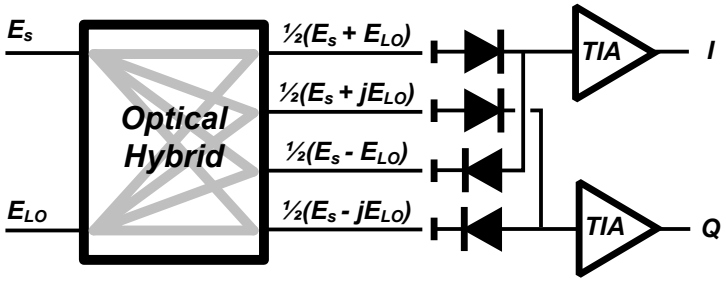


Figure 3.5: Balanced detection using the 90 degree optical hybrid, four photodiodes and electrical trans-impedance amplifiers (TIAs).

The input optical signal field $E_s(t)$ and optical LO field $E_{LO}(t)$ are

$$E_s(t) = \sqrt{P_s(t)} \cdot e^{j(\omega_s(t)+\theta_s(t))}$$
$$E_{LO}(t) = \sqrt{P_{LO}(t)} \cdot e^{j(\omega_{LO}(t)+\theta_{LO}(t))} \tag{3.5}$$

where $P_s(t)$, $\theta_s(t)$ and $\omega_s(t)$ are input power, phase and frequency, respectively, and $P_{LO}(t)$, $\theta_{LO}(t)$ and $\omega_{LO}(t)$ are the LO power, phase and frequency, respectively. The optical input and LO fields E_s and E_{LO} are mixed in the optical hybrid, and four optical fields of $1/2(E_s + E_{LO})$, $1/2(E_s - E_{LO})$, $1/2(E_s + jE_{LO})$

and $1/2(E_s - jE_{LO})$ are obtained at the hybrid outputs. These four output fields (powers) are down-converted through the four UTC photodiodes as

$$\begin{aligned}
I_{I+}(t) &= R/2(P_s(t) + P_s(t)) + R\sqrt{P_s(t) + P_s(t)}\cdot cos[(\omega_s - \omega_{LO})t + \theta_s(t) - \theta_{LO}(t)] \\
I_{I-}(t) &= R/2(P_s(t) + P_s(t)) - R\sqrt{P_s(t) + P_s(t)}\cdot cos[(\omega_s - \omega_{LO})t + \theta_s(t) - \theta_{LO}(t)] \\
I_{Q+}(t) &= R/2(P_s(t) + P_s(t)) + R\sqrt{P_s(t) + P_s(t)}\cdot sin[(\omega_s - \omega_{LO})t + \theta_s(t) - \theta_{LO}(t)] \\
I_{Q-}(t) &= R/2(P_s(t) + P_s(t)) - R\sqrt{P_s(t) + P_s(t)}\cdot sin[(\omega_s - \omega_{LO})t + \theta_s(t) - \theta_{LO}(t)]
\end{aligned} \tag{3.6}$$

where the I-differential current outputs are $I_{I+}(t)$ and $I_{I-}(t)$, the Q-differential current outputs are $I_{Q+}(t)$ and $I_{Q-}(t)$, and R is photodiode responsivity $[A/W]$. The currents $I_+(t)$ and $I_-(t)$ and are subtracted by the balanced PDs as shown in figure 3.5, forming AC differential current outputs $\Delta I_I(t)$ and $\Delta I_Q(t)$, which are

$$\begin{aligned}
\Delta I_I(t) &= 2R\sqrt{P_s(t) + P_s(t)}\cdot cos[(\omega_s - \omega_{LO})t + \theta_s(t) - \theta_{LO}(t)] \\
\Delta I_Q(t) &= 2R\sqrt{P_s(t) + P_s(t)}\cdot sin[(\omega_s - \omega_{LO})t + \theta_s(t) - \theta_{LO}(t)].
\end{aligned} \tag{3.7}$$

(a) (b)

Figure 3.6: Two different balanced-types of the photodiode connections with TIAs: (a) balanced PDs and single-ended TIA and (b) single-ended PDs and differential TIA.

In figure 3.6 (a), the DC currents are subtracted by the series photodetector connection from GND to V_{EE}, and only the AC current of $2\Delta I(t)$ is an input

to the single-ended TIA circuit. In figure 3.6 (b), the balanced single-ended photodetectors can also be directly connected to differential inputs at a TIA, with proper ∼-2 V DC biases for both the photodiodes and the TIAs. In our OPLL design, we used the parallel single-ended PD connections with the differential TIA operation (figure 3.6 (b)), as this simplified the PIC fabrication.

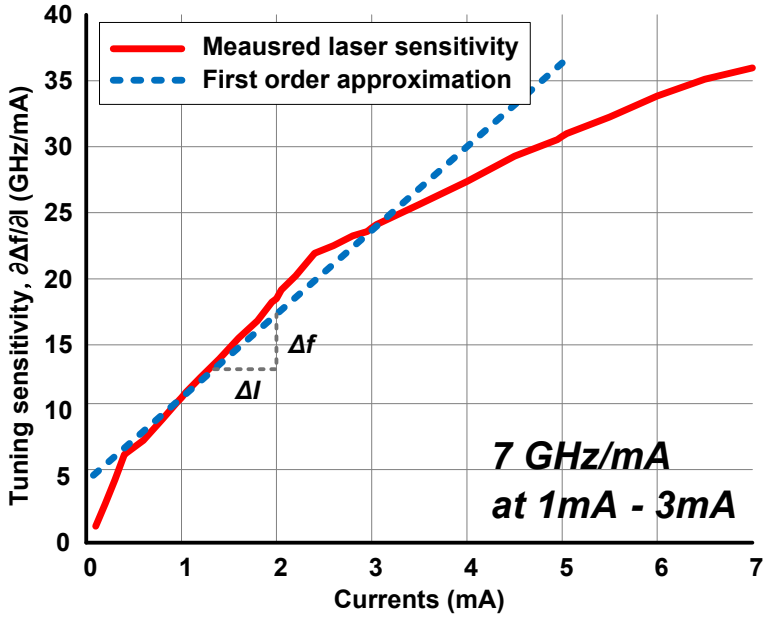
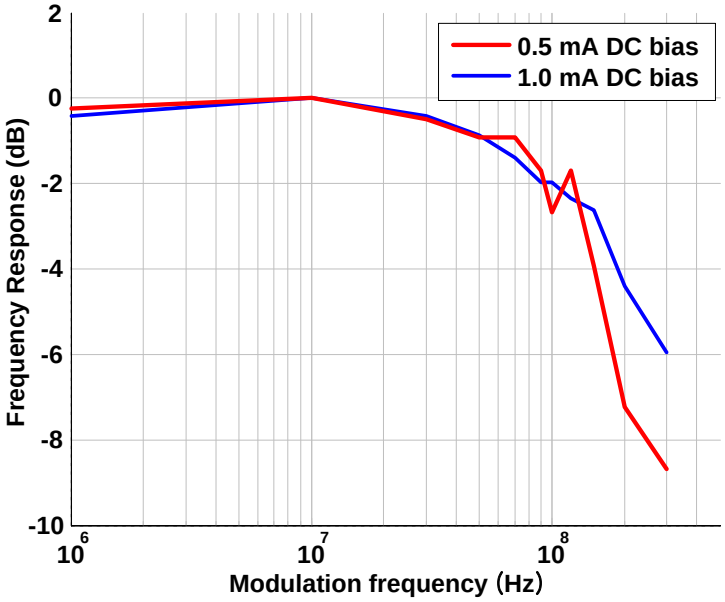


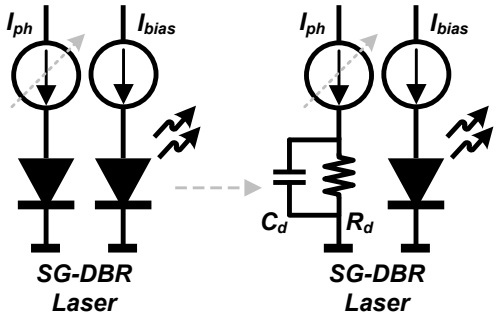
Figure 3.7: Measured SG-DBR laser tuning sensitivity and its first order approximation between 1-3 mA bias ranges, courtesy of M. Lu.

The PIC device characteristics have been measured for the OPLL feedback loop design. First, the frequency tuning sensitivity of the widely tunable SG-DBR laser was measured. The measured result is shown in figure 4.3. The laser tuning sensitivity is approximated by the first order slope of $K_{CCO} = 2\pi \times 7\ GHz/mA = \sim 4.4 \times 10^{13}[rad/sec/A]$ at a DC current bias of 1-3 mA (this initial current condition of 1-3 mA was used in our OPLL system experiment). This K_{CCO} plays a comparable role in OPLL design to the VCO sensitivity K_{VCO} $[rad/sec/V]$ in

electrical PLL design.



(a)



(b)

Figure 3.8: The frequency response for laser tuning section diode. The measured frequency response has a single pole at approximately 100 MHz (a). Simple diode R_d and C_d model for the frequency response (R_d ~10 Ω and C_d ~160 pF) (b), courtesy of M. Lu.

Another important PIC device characteristic is the frequency tuning response at the SG-DBR laser phase tuning. The laser wavelength is tuned by varying the current injection. However, the resulting laser frequency tuning response is re-

tarded because of the minority carrier life time. This phenomenon is represented by a single-pole frequency response $1/(\tau_{tunes}s+1)$ with a pole frequency at approximately 100 MHz in the SG-DBR laser, as shown in figure 3.8 (a). The response is simply modeled as the R_dC_d parallel shown in figure 3.8 (b). This capacitance is the diode diffusion capacitance and is measurable. The diode resistance R_d of 10 Ω is measured, and therefore, C_d of approximately 160 pF is extracted. This parasitic factor might be easily neglected in the OPLL loop design. However, the effect of this laser tuning resposne must be considered in the OPLL feedback loop designs, if the OPLL requires wide loop bandwidth. This 100 MHz pole would introduce 5.7 degree phase variance in a 10 MHz loop and 45 degree phase variation in a 100 MHz loop.

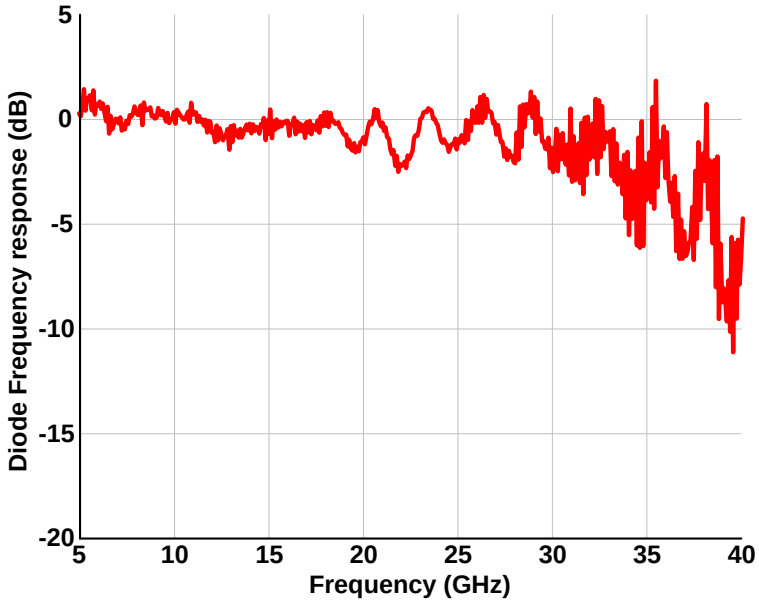


Figure 3.9: Measured PD 3-dB bandwidth. More than 30 GHz bandwidth has been achieved. Courtesy of M. Lu [4, 20].

The third PIC device characteristic is the photodetector's 3-dB frequency

bandwidth, as shown in (figure 3.9). The photodetector bandwidth is limited by the photodetector output capacitance C_{PD} and the TIA's 50 Ω input impedance. The four-element arrays of single-ended UTC PDs were designed and fabricated by M. Lu [4, 20]. The photodetectors exhibited greater than 30 GHz 3-dB bandwidth, measured by an Agilent PNA-X network analyzer (N5247B). This 3-dB bandwidth can also be modeled as a single pole $1/(\tau_{PD}s + 1)$. However, this device characteristic was ignored in the OPLL feedback loop designs, because the pole frequency is far enough from the target loop bandwidth of >500 MHz. This bandwidth does however limit the tuning range of the offset PLLs reported later in this thesis.

After considering physical delay including electrical and optical waveguide length and the transit delay in the laser, hybrid and photodetectors, the total PIC delay τ_{d-PIC} of ∼40 ps was determined by M. Lu. This small delay results from the PIC integration.

The PIC open loop transfer function $T_{PIC}(s)$ including all the above PIC device characteristics is

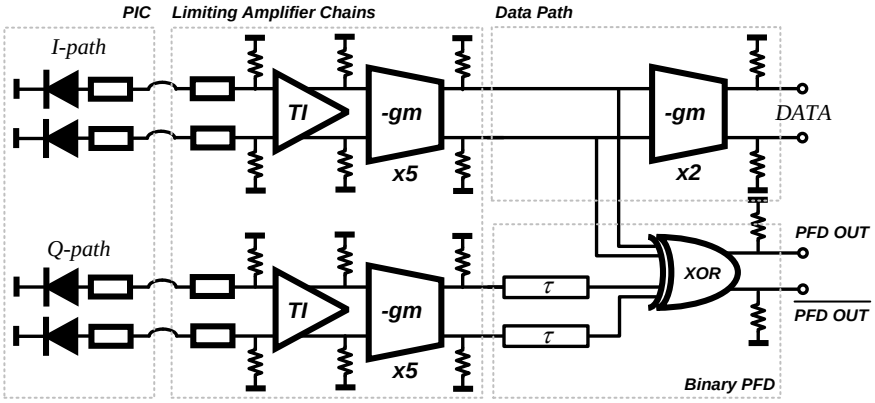
$$T_{PIC}(s) = \frac{K_{CCO}}{s(\tau_{tunes}s + 1)} \cdot e^{(-\tau_{PIC}s)}. \tag{3.8}$$

Table 3.1 gives a summary of the photonic IC device characteristics for the OPLL designs.

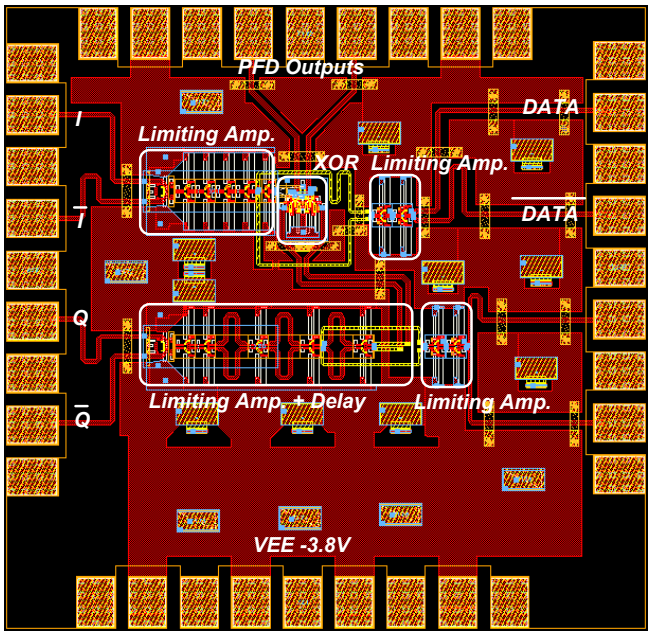
Table 3.1: Summary of the PIC device parameters for the homodyne OPLL design

Parameters	Value	Unit	Descriptions
	1/s	sec/rad	Phase/frequency: $\Theta(s) = F(s)/s$
K_{CCO}	$2\pi \times 7 \times 10^{12}$	rad/A	Laser tuning sensitivity
τ_{tune}	$1/(2\pi \times 100 \times 10^{6})$	sec	Tuning frequency responsivity
τ_{PD}	$1/(2\pi \times 35 \times 10^{9})$	sec	Photodetector 3-dB pole frequency
τ_{d-PIC}	40	ps	Total PIC delay

3.3.2 Electrical Integrated Circuit



(a)



(b)

Figure 3.10: The EIC schematic (a) and layout (b) for the binary phase and frequency detection with BPSK data outputs. TI: trans-impedance (current to voltage conversion), g_m-blocks as limiting amplifiers, and XOR gate with a delay line for PFD functions, courtesy of E. Bloch and T. Reed [7].

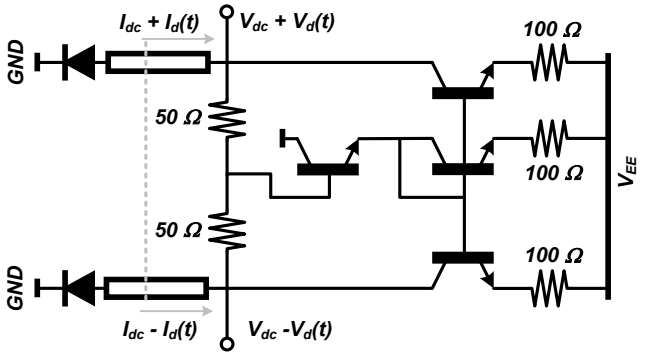


Figure 3.11: The biasing circuit to supply -2 V to the single-ended PDs [7].

We describe an EIC for phase-locked BPSK receivers. The EIC has high-speed binary phase and frequency detector and binary PSK data outputs. Teledyne's 500 nm InP HBT process which has 300 GHz f_τ and f_{max} [40] and four metal stack layers were used for the EIC designs. Block-level IC schematic and layout are shown in figure 3.10. The EIC has $I-Q$ signal paths generated by the PIC. These two 90 degree out-of-phase $I-Q$ signals are amplified and limited (digitized) by five-stage g_m-block limiting amplifier chains. The binary I and Q signals are then mixed in an XOR phase detector with a delay line (10 ps). The combination of the two optical mixers (the photodetectors), plus the XOR gate and delay line, forms Quadri-correlator PFD [41]. The BPSK data are amplified and are output through the I output data path. In detail, the EIC has several key blocks. The input biasing circuit (figure 3.11) was designed to provide a negative DC bias of around -2 V for each single-ended PD and a proper 50 Ω termination for the photodiode AC outputs. Using transistor current mirrors to bias the diodes, the photodiodes are biased at -2 V for the photodiode's DC currents of 0.3-1.5 mA. Thus, the photodiode voltage bias condition is set by the input DC circuit from

the photodetectors as

$$V_{PD}(s) = V_{EE} + V_{DC} \cdot 100\Omega + 2 \cdot V_{EE}, \tag{3.9}$$

where the supply voltage of V_{EE} is -3.8 V and transistor (diode) turn-on voltage V_{BE} is approximately 0.8 V. If the DC currents from the two detectors are equal, the connection point of the two 50 Ω resistors is a virtual ground and the AC signals $\Delta I(t)$ are equally terminated by 50 Ω loads.

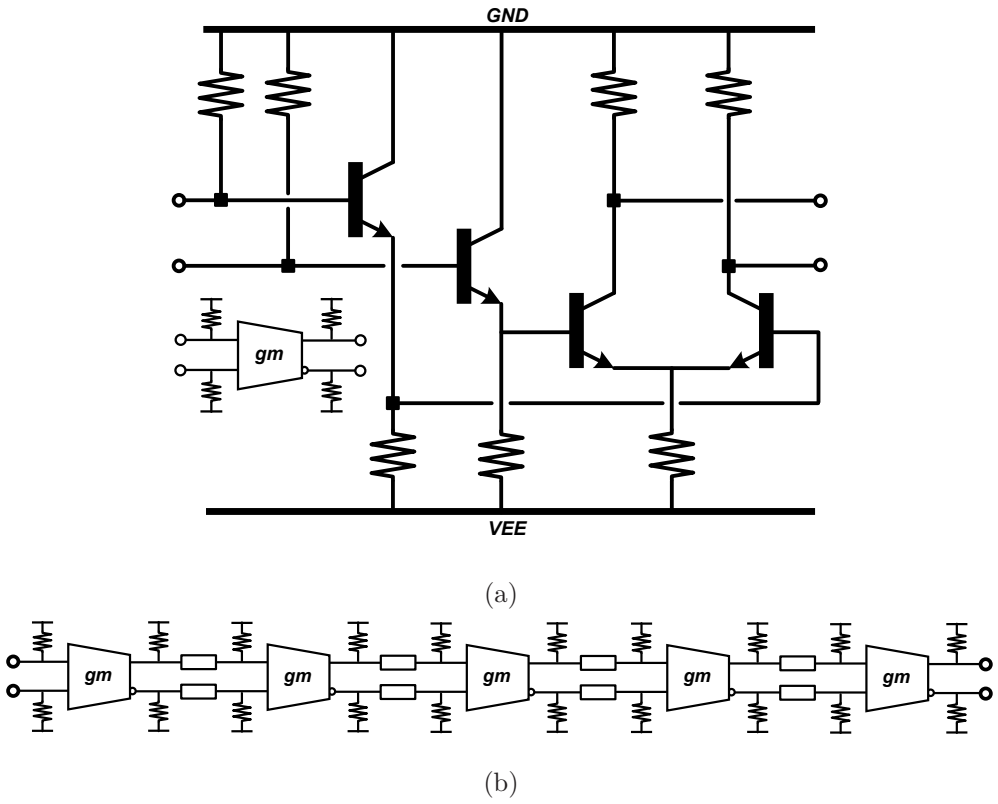


Figure 3.12: g_m-block amplifiers for limiting amplifier chains (a) and five-stage limiting amplifier chains (b) [7].

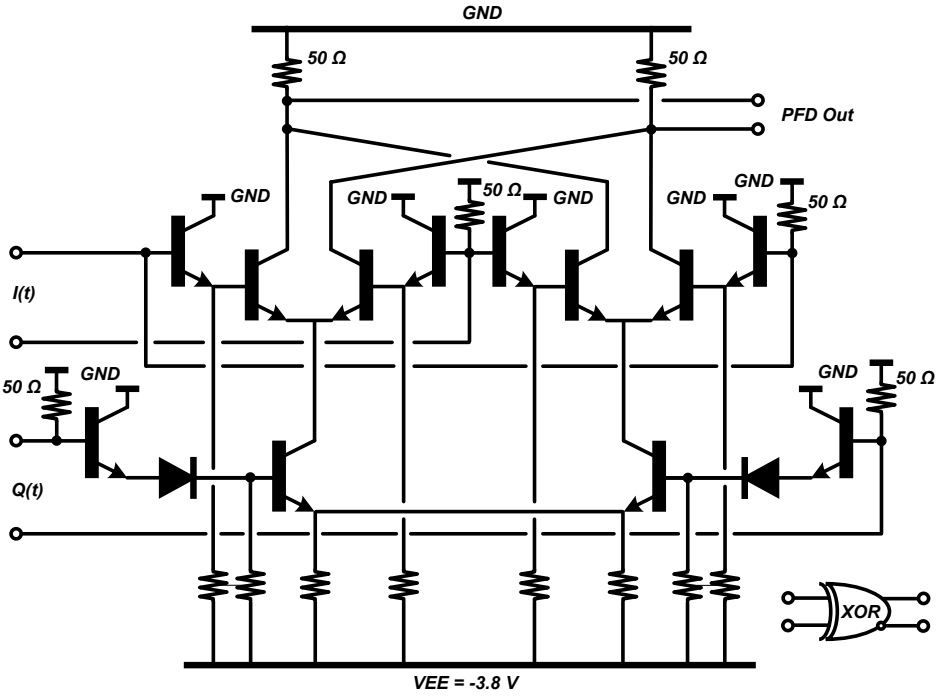
The EIC includes limiting amplifiers, designed by the modified Darlington (ECL-type) g_m-blocks (figure 3.12 (a)). The limiting amplifiers limit the photocurrent ranges of 0.3-1.5 mA to 0.3 V_{pp} digitized signals only carrying phase and

frequency information. This limiting scheme is important for stable OPLL operation. The photocurrent amplitude fluctuations are suppressed by the five-stage limiting amplifier chains of figure 3.12 (b). Five-stage differential g_m-amplifier blocks and the double-terminated interconnections were used for the limiting amplifier chains. Each stage has a voltage gain of approximately

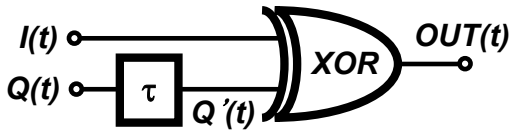
$$V_{out}/V_{in} \approx (qI_c/nKT)\cdot 25\ \Omega, \tag{3.10}$$

where the DC bias current for the differential tail $2I_c$ is 12 mA, a thermal voltage KT/q is 25 mV, an ideality factor n is approximately 2.2 and 50 Ω double terminated interconnection has a total of 25 Ω output resistance. Thus, a single stage has a voltage gain of approximately 2.7:1 (8.71 dB) (Teledyne's HBT are operated at a lower current density (2.4 $mA/\mu m^2$) condition than that optimum (6.0 $mA/\mu m^2$) for the highest f_τ and f_{max} [40]).

A PFD is designed using a Gilbert-cell-mixer (ECL-type XOR-gate) with a 10 ps delay-line. This structure detects both phase and frequency errors. Due to using 10 ns delay, as we will show, this PFD will ideally have a 50 GHz frequency pull-in range ($\omega_n\tau = \pi$). The ECL XOR circuit diagram is shown in figure 3.13 (a) and the Quadri-correlator PFD block is shown in figure 3.13 (b).



(a)



(b)

Figure 3.13: ECL-XOR gate schematic for the PFD design (a) and Quadri-correlator PFD structure including the XOR and delay-line (b) [7].

The inputs $I(t)$ and $Q(t)$ of the PFD are derived from the photodetector outputs as equation 3.7. They can be analyzed as sinusoidal waveforms with

$$I(t) = A{\cdot}cos(\omega_e t + \theta_e)$$
$$Q(t) = A{\cdot}sin(\omega_e t + \theta_e), \tag{3.11}$$

where A is a signal amplitude, ω_e is the frequency difference between the two

lasers, θ_e is the phase difference (the time variation of θ_e is neglected). The $Q(t)$ is delayed by the time delay τ (10 ps in our OPLL design), and Q'(t) is

$$Q'(t) = A{\cdot}sin(\omega_e(t-\tau)+\theta_e). \tag{3.12}$$

Then, the two inputs of $I(t)$ and $Q(t)$ are multiplied by the XOR gate, and the PFD output $OUT(\omega_e, \theta_e)$ is derived as

$$OUT(\omega_e,\theta_e) = 1/2(A)^2{\cdot}sin(2\omega_e t+\omega_e\tau+2\theta_e)+1/2(A)^2{\cdot}sin(\omega_e\tau). \tag{3.13}$$

Here we have treated the XOR gate as a product device and have neglected its limiting characteristics. The signal $OUT(\omega_e, \theta_e)$ is plotted in figure 3.14. This result shows stable locking conditions: phase errors at 0 rad and $\pm\pi$ with a positive slope from blue to red, and a frequency error at 0 Hz with a positive slope from blue to red.

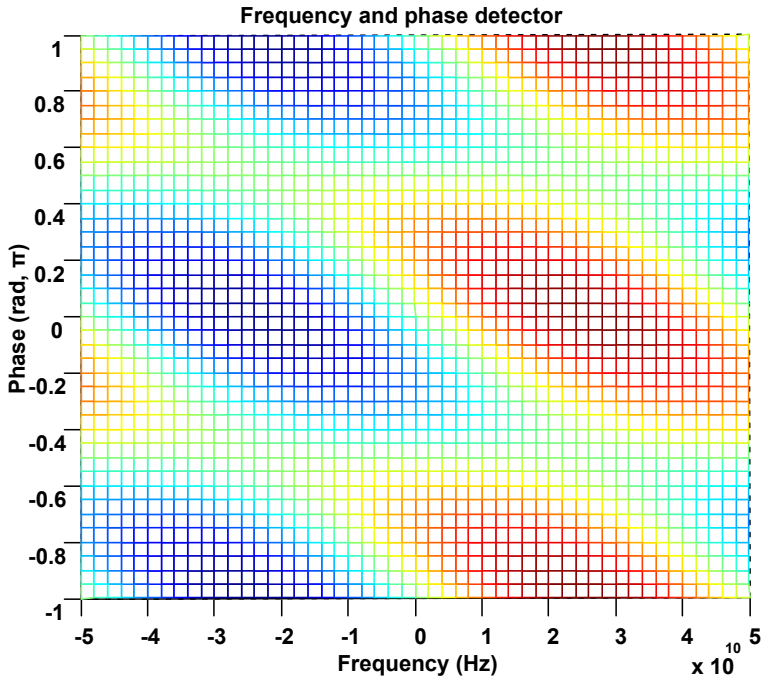


Figure 3.14: 3-D frequency and phase detection plot: voltage error vs. frequency (-50 GHz to 50 GHz) and phase (-π to π). Dark red corresponds to a 0.5 V output and dark blue to -0.5 V output. Phase detection and frequency detection slopes must have the same sign for negative feedback loop operation.

This Quadri-correlator PFD is simply analyzed with two separate conditions of frequency detection mode (frequency error $f_e \neq 0$) and phase detection mode (frequency error $f_e = 0$). If the frequency error is non-zero, $OUT(t)$ is derived as

$$OUT(\omega_e) = 1/2(A)^2 \cdot sin(\omega_e \tau). \tag{3.14}$$

This $OUT(\omega_e)$ represents a measure of the frequency error. The detection range is determined by the length of the delay line, and is ideally $1/(2\tau)$.

If the frequency error is zero, the $OUT(\theta_e)$ is

$$OUT(\theta_e) = 1/2(A)^2 \cdot sin(2\theta_e). \tag{3.15}$$

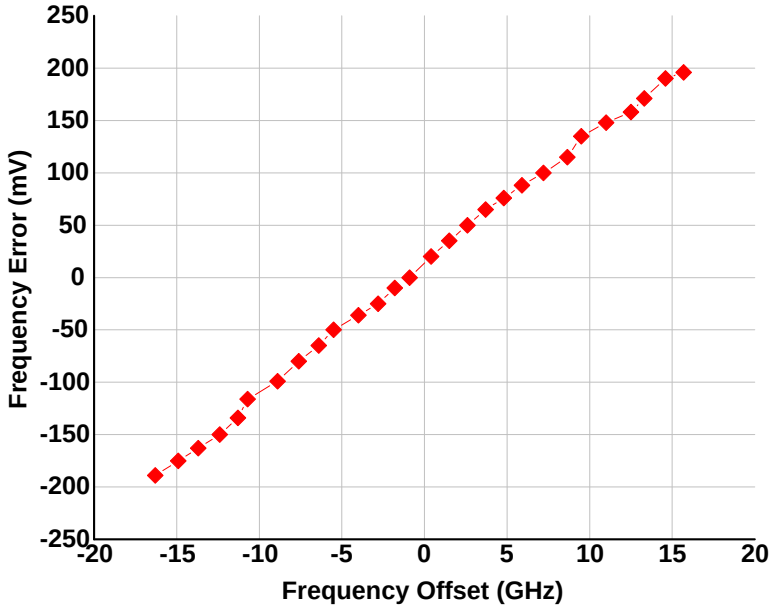


Figure 3.15: Measured frequency detection results through the PIC and EIC.

In our EIC, the digitized I and Q signals with V_{pp} of 0.3 V are used for our PFD operations as a binary PFD. In the frequency detection mode, I and Q' (time delayed) signals are mixed by the XOR gate, and $OUT(\omega_e)$ have different duty cycles, depended on ω_e. Then, the mean values of the different duty cycles represent a linear triangular waveform

$$OUT(\omega_e) = 0.15 \int sgn[sin(\omega_e \tau)] d\omega_e. \tag{3.16}$$

The frequency detection mode was measured through the PIC and EIC, and the measured results are shown in figure 3.15. In the phase detection mode, the phase detection becomes binary

$$OUT(\theta_e) = 0.15 sgn(2\theta_e). \tag{3.17}$$

This binary phase detection has a strong non-linear characteristic, and it requires different feedback loop analysis, compared with linear and sinusoidal phase

detections. In our OPLL design, I have simplified the binary non-linear phase detection characteristics to an equivalent linear function of $0.2 - 0.5$ $[V/rad]$. It has been simulated and compared to Matlab Simulink simulation using the non-linear phase detector. The details of the OPLL design and simulations will be discussed in the next section.

As shown in figure 3.10, the EIC has output paths for BPSK I-phase and Q phase data. In the middle of te limiting amplifier chains, the signals were fanned-out 2:1 and were amplified with two-stage vg_m-block limiting amplifiers. The EIC has been designed with a compact size of 1.30×1.20 mm^2 and has a propagation delay τ_{d-EIC} of 50 ps including HBT circuit delays. This delay has been verified using ADS circuit simulation including EM simulation. The detailed EIC designs and results can be found in [7].

The EIC open loop transfer function $T_{EIC}(s)$ for the phase error is

$$T_{EIC}(s) = K_{PD} \cdot e^{-\tau_{d-EIC} s}, \tag{3.18}$$

where the key parameters are as follows.

Table 3.2: Summary of the EIC device parameters for the homodyne OPLL design

Parameters	Value	Unit	Descriptions
K_{PD}	0.2-0.5	V/rad	Linear equivalent phase detection gain
K_{FD}	$0.3/(2\pi \times 50 \times 10^9)$	V/rad/sec	Linear frequency detection gain
τ_{d-EIC}	50	ps	Total EIC delay

3.3.3 Hybrid Loop Filter

Given the PIC and EIC device characteristics in Table (1) and (2), two design goals were set for a stable OPLL: 1) the open loop bandwidth $\omega_n/2\pi$ of greater than 500 MHz to track the phase noise (linewidth) and to hold the LO's 10's (100's) MHz frequency drifts, and 2) hence, total (effective) loop delay of less than ∼200 ps to meet the absolute stable condition between loop bandwidth vs. delay [42]. Since the total delay in the PIC and EIC is ∼90 ps, the loop filter should be designed with small loop delay and stable loop conditions. A second order type-II PLL including an active loop filter was selected for our OPLL designs, because of its simple configuration and powerful working with a non-steady state error for phase error [43, 44].

Feedback loop analysis starts with the open loop transfer function $T(s)$ including the critical loop delay

$$T(s) = K_{PD} \cdot K_{CCO} \cdot \frac{F(s)}{s} \cdot e^{-\tau_d s}, \tag{3.19}$$

where $F(s)$ is a loop filter transfer function. Then, a closed loop transfer function $H(s) = T(s)/(1 + T(s))$ is

$$H(s) = \frac{K_{PD} \cdot K_{CCO} \cdot \frac{F(s)}{s} \cdot e^{-\tau_d s}}{1 + K_{PD} \cdot K_{CCO} \cdot \frac{F(s)}{s} \cdot e^{-\tau_d s}} = \frac{2\varsigma\omega_n s + {\omega_n}^2 \cdot e^{-\tau_d s}}{s^2 + 2\varsigma\omega_n s + {\omega_n}^2 \cdot e^{-\tau_d s}}, \tag{3.20}$$

where ς is a damping factor, ω_n is a natural loop bandwidth, and τ_d is the total loop delay [43, 44]. Given all the device characteristics in the tables (1) and (2), the final loop transfer function should be similar with equations 3.19 and 3.20. Then, the loop filter $F(s)$ for the second order type-II should be carefully designed including the loop delay and additional parasitics, i.e. laser slow tuning response

of τ_{tune}. In general, the loop filter for the second order type-II PLL consists of one pole and one zero as

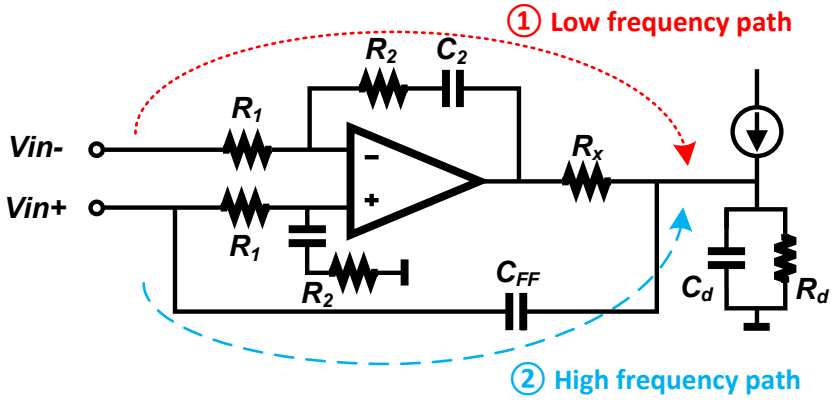
$$F(s) \approx \frac{\tau_2 s + 1}{\tau_1 s}. \tag{3.21}$$

This transfer function is determined by the phase detector gain K_{PD}, laser (or VCO) tuning sensitivity K_{CCO}, and the loop bandwidth ω_n. However, it is more complicated if the feedback loop requires to consider long loop delay, other parasitics, and wide loop bandwidth (targeted for more than 500 MHz), may require many additional design consideration such as the laser slow tuning response, the loop delay for each device, and the poles of the op-amplifier. As discussed in the previous section, the laser pole frequency is approximately 100 MHz, and a zero $(1 + \tau_{zero}s)$ must be added to compensate the laser parastic pole.

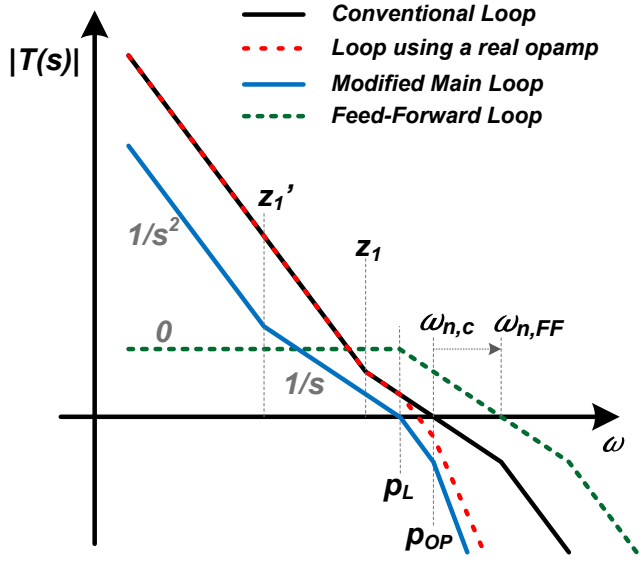
Loop filter design using commercial op-amplifiers has several design challenges: 1) op-amplifier unity gain frequency is small (less than 200 MHz) even on parts labelled as GHz op-amplifiers, and 2) total loop delay through the op-amplifier package including leads is not known or easily measured. In summary the fastest voltage feedback op-amplifier having small DC offset commercially available has only 200 MHz unity gain bandwidth and the second and third pole (the first pole being at DC) at the OPLL transfer function will be located at approximately 200 MHz [45]. This makes broadband OPLL impossible using commercial op-amplifier with the classic loop filter transfer function $F(s)$ of equation 3.21.

To solve these issues, I have proposed a new loop filter-type for our wide loop bandwidth OPLL. To meet design requirements, two basic PLL design constraints have been followed: 1) high gain at DC and low frequencies to suppress laser phase noise, and 2) large phase and gain margins including the additional poles and loop

delay. To achieve the two basic PLL design approaches, we developed a modified dual path loop filter. This approach, used to reduce the size of the compensation capacitor in IC design, is here adopted to minimize high frequency delay and to extend the loop bandwidth in an OPLL.



(a)



(b)

Figure 3.16: Dual-path loop filter schematic with low frequency path and high frequency path (a), and the conceptual bode gain plot open loop transfer function $T(s)$. The feed-forward loop significantly enhances the loop bandwidth $\omega_{n,FF}$ compared with the conventional loop $\omega_{n,c}$ (b).

A schematic of the modified dual-path loop filer is shown in figure 3.16 (a). This loop filter consists of two paths: 1) a low-frequency main signal path having an integrator for DC and low frequencies, giving gain with an $1/s^2$ slope, and 2) a

short, high-frequency passive feed-forward path for high frequency signals which will set the phase margin. Due to this modified loop, the feedback loop keeps the second-order $1/s^2$ phase noise suppression capacity by the high gain at low frequencies and yet gives almost no added delay through the feed-forward path. The dual feed-forward loop is modeled by two independent paths (figure 3.8 (b)). As a result, the total loop delay at high frequencies is not largely impacted by the loop filter, and the loop bandwidth is limited by the PIC and EIC delays.

The integrator path includes a first order active loop filter with integrator time constant $\tau_1 = R_1 C_2$, the op-amplifier internal second pole τ_{OP}, a resistor R_x as voltage to current conversion, and the op-amplifier delay τ_{d-OP}. The differentiator has a zero of time constant $C_{FF}R_d$ and a path gain determined by the capacitor value C_{FF}, given the laser and phase detector gains. Figure 3.16 (b) shows the detail open loop transfer function $T(s)$. The dual-path loop must avoid a 180 degree phase difference between the two paths to prevent an amplitude notch at the gain crossover frequency. In addition, the laser tuning response τ_{tune}, the laser tuning sensitivity K_{CCO}, the integrator arising from frequency to phase conversion $1/s$, and the total effective loop delay τ_{d-eff} are all included in the feed-forward path.

Based on all loop parameters, the final open loop response $T(s)$ is expressed as

$$T(s) \approx K_{PD} \cdot K_{cco} \cdot \frac{1}{\tau_{tune} s + 1} \cdot \left(\frac{\tau_2 s + 1}{\tau_1 s} \cdot \frac{1}{\tau_{OP} s + 1} \cdot \frac{1}{R_x} \cdot e^{-\tau_{dOP} s} + \frac{C_{FF}}{2} \right) \cdot e^{-\tau_d s}, \tag{3.22}$$

where a linear equivalent phase detection gain $K_{PD} = 0.2 - 0.5\ V/rad$, a laser frequency tuning sensitivity $K_{CCO} \approx 5.0 \times 10^{13}\ rad/sec/A$, and a laser slow tuning

response τ_{tune} gives a single pole at 100 MHz. The active loop filter has a pole time constant τ_1 and a zero time constant τ_2 with frequencies at 0.17 MHz and 2.2 MHz, respectively. The op-amplifier second parasitic pole time constant τ_{OP} is at 200 MHz, the resistor R_x is 500 Ω, and the op-amplifier delay τ_{d-OP} of ∼200 ps. The coupling capacitor on feed-forward path C_{FF} is 1.0 pF, and a total effective loop delay τ_d is 120 ps. Based on the equation 3.2, the Bode diagram of the open loop response $T(s)$ is as shown in figure 3.17. The total loop response follows the main path at low frequencies and the feed-forward path at high frequencies. From the response, the feedback loop response shows a natural frequency ω_n of 4.4×10^9 rad/sec (700 MHz) and 65 degree phase and >7 dB gain margins.

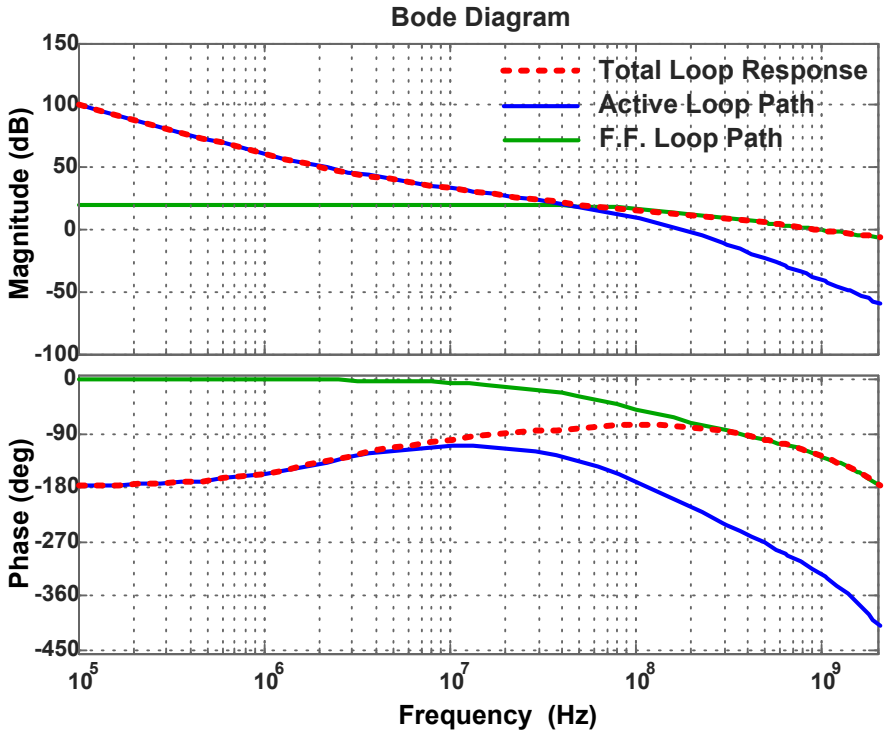


Figure 3.17: A Bode diagram for the OPLL open loop response $T(s)$.

This linear transfer function $T(s)$ is simulated in the Matlab Simulink. In this simulation the phase detector was modeled as a nonlinear limiting element as shown in figure 3.18. Note that the gain of the PFD is given a high value and the output is truncated by a limiter to $V_{pp} = 0.3\ V$. Also, the loop filter has dual paths and the delay of the feed-forward path is ignored. The laser section includes the laser tuning response, and a total effective time delay of 120 ps is included.

A phase step is simulated. The OPLL feedback loop tracks the phase step within 2 ns, corresponding to a reasonable settling time $\approx 4/\varsigma\omega_n$ (figure 3.19 (a)). The phase detector output show digital switching because of the use of the binary PFD. Figure 3.19 (a) is the phase detector limiting amplifier output and figure 3.19 (b) is the modified dual-path loop filter output.

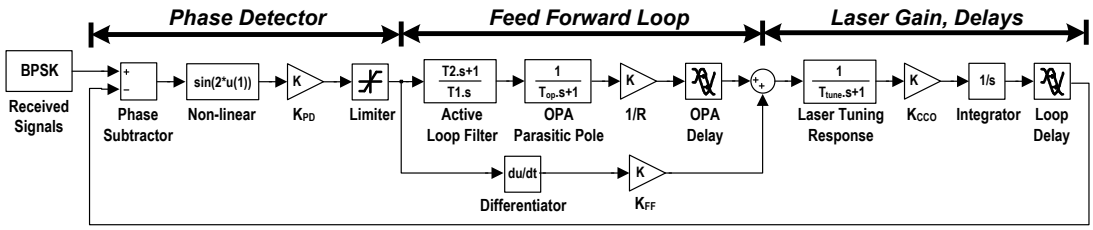
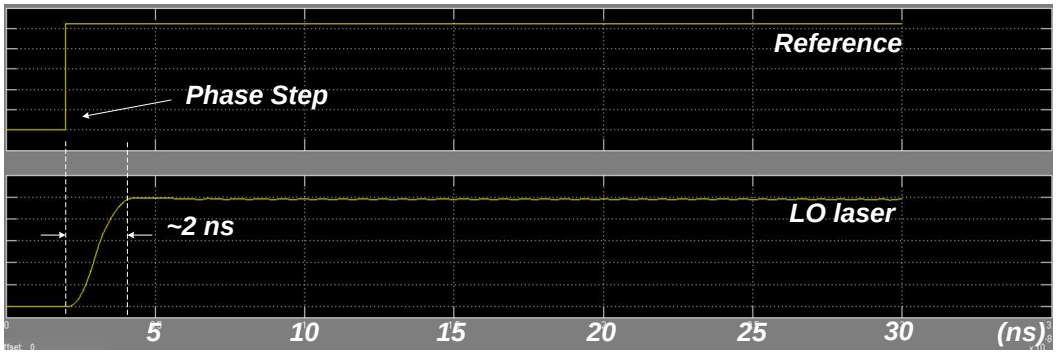
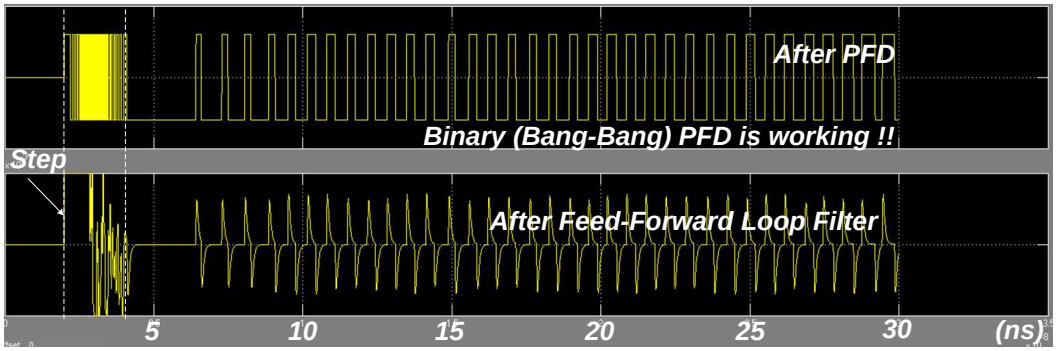


Figure 3.18: Matlab Simulink simulation including the binary PFD, laser device characteristics, feed-forward loop filter and the total effective loop delay.



(a)



(b)

Figure 3.19: Matlab Simulink simulation results for the phase step jump. (a) The phase step jump in the reference and the LO laser's phase acquisition through the designed feedback loop, and (b) Binary (bang-bang) PFD output and the modified loop filter output.

Table 3.3: Summary of the loop filter parameters for the homodyne OPLL design

Parameters	Value	Unit	Descriptions
τ_1	9.5×10^{-7}	sec/rad	Active loop filter pole, R_1C_2
τ_2	7.2×10^{-8}	sec/rad	Active loop filter zero, R_2C_2
τ_{OP}	8.0×10^{-10}	sec/rad	OP-amp parasitic pole (second pole)
τ_{d-OP}	2.0×10^{-10}	sec	OP-amp delay (assumed as relatively big number)
τ_d	1.2×10^{-10}	sec	Total effective loop delay (high frequency path)
R_x	500	Ω	Voltage to current conversion
C_{FF}	1.0	pF	Feed-forward coupling capacitor

3.4 Implementation and Experimental Results

3.4.1 OPLL Integration

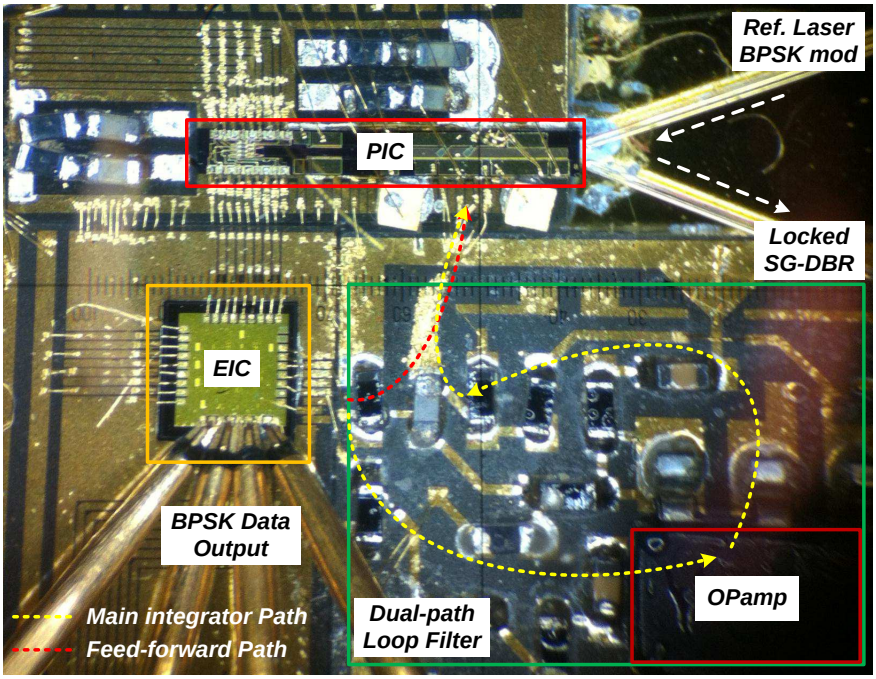


Figure 3.20: The OPLL hybrid integrations including the PIC, EIC, and hybrid loop filter. Red: short feed-forward path through the single capacitor C_{FF}, yellow: long integrator-path through the commercial op-amplifier.

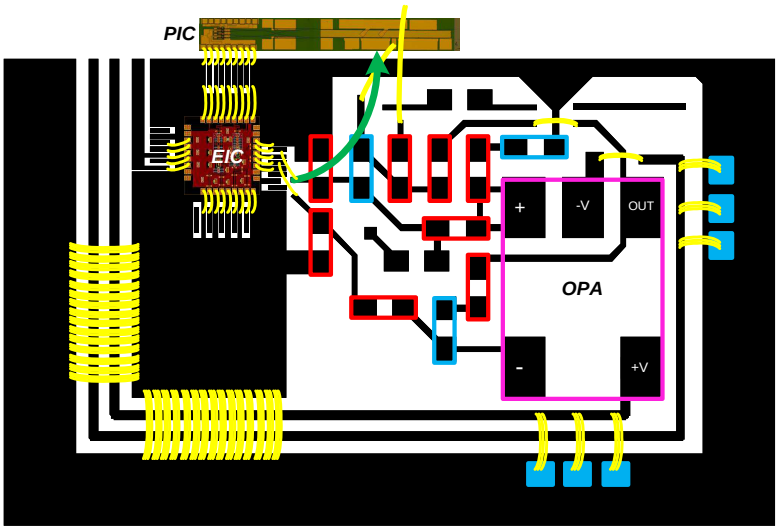


Figure 3.21: The mask layout, discrete component soldering and wire-bonding locations.

The OPLL for the Costas loop receiver is realized as shown in figure 3.20. The fabricated PIC is at on the top of the image, the EIC on the bottom left, and the hybrid loop filter on the bottom right. These are mounted on a single AlN substrate ($\epsilon_r = 9$, thermal conductivity $= 140 - 180\ W/m/K$) within a total size of $10{\times}10\ mm^2$. The ICs are interconnected by wire-bonds and transmission lines. The feed-forward path (red-dots in figure 3.20) is kept shunt to decrease the interconnection delay. The main integrator path (yellow dots in figure 3.20) passes through an op-amplifier to have a high gain but long loop delay. The loop filter uses a commercial voltage-feedback op-amplifier, Texas Instruments LMH6609, which has a 70 dB open loop gain and a 200 MHz unity gain bandwidth [45]. Together with discrete chip capacitors and resistors, the active loop transfer function (equation 3.22) is realized. The mask layout, component placement and wire-bond connections are also shown in figure 3.21.

3.4.2 Homodyne OPLL Experiments

To verify the homodyne OPLL performance, several OPLL tests were performed.

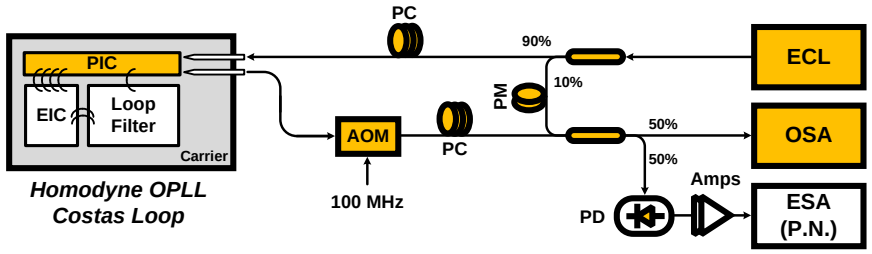


Figure 3.22: The test setup for the first homodyne OPLL experiment to measure the beating spectrum between the reference laser and the locked SG-DBR laser. ECL: external cavity laser, PC: phase controller, OSA: optical spectrum analyzer, and AOM: acousto-optical modulator.

We tested the beat spectrum between the reference laser and the locked SG-DBR laser, measuring its phase noise performance. We used a tunable Agilent or Koshin laser, which have 100 kHz linewidth, as a reference laser, and the locked SG-DBR laser output is shifted by 100 MHz using an acousto-optical modulator (AOM). This shifts the beat note away from DC. A test setup for both two measurements is shown in figure 3.22. The beat signal, which arises from multiplication in time domain, is

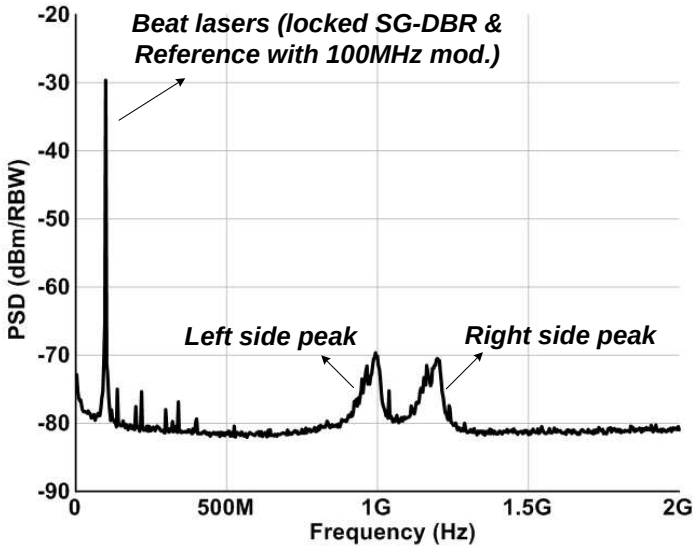
$$cos(\omega_{ref}t + \theta_{pn_{ref}}(t)) \cdot cos(\omega_S t + 2\pi(100MHz)t + \theta_{pn_{RF}}(t) + \theta_{pn_S}(t)) \qquad (3.23)$$

where ω_{ref} is the reference laser frequency, $\theta_{pn_{ref}}(t)$ is the reference phase noise, ω_S is the SG-DBR laser frequency, $\theta_{pn_{RF}}(t)$ is the AOM modulator phase noise, and $\theta_{pn_S}(t)$ is the SG-DBR laser phase noise.

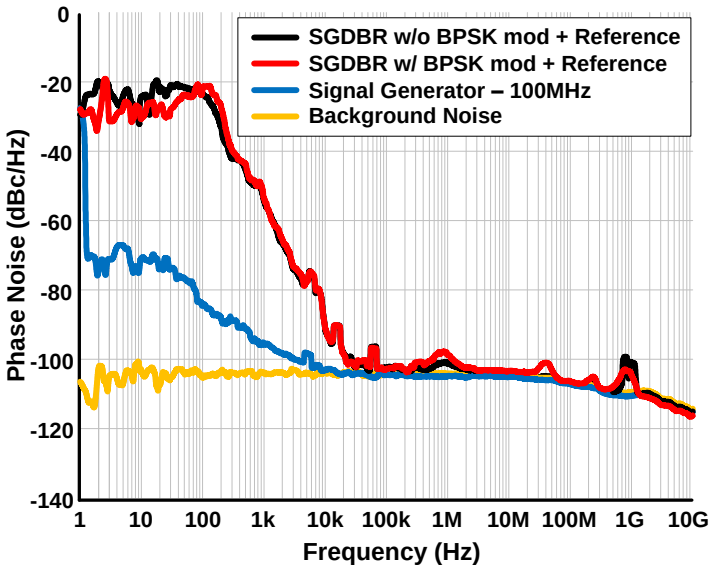
$$cos(2\pi(100MHz))t + \theta_{pn_{RF}}(t) + \theta_{pn_{SGDBR}}(t) - \theta_{pn_{ref}}(t)) \qquad (3.24)$$

where homodyne lokcing forces $\omega_{ref} = \omega_s$, and where we assume that the path lengths between the two lasers are matched. As shown in equation 3.24, the beat spectrum shows the relative phase noise at the homodyne OPLL and the phase noise of the RF signal source. The latter is very small compared with the noise of the SG-DBR laser. Given an ideal PLL, the noise of the locked laser will be following the phase noise of the reference laser.

Using the test setup in figure 3.22, the measured beat spectrum between the two lasers is as shown in figure 3.23 (a). The peak is at 100 MHz, with two side peaks at 1 GHz and 1.2 GHz. These correspond to noise peaks at the OPLL at $\pm\omega_n/\pi$. This result shows that the SG-DBR is stably locked at the same wavelength of the reference laser, and that the closed loop bandwidth is a 1.1 GHz. The beat spectrum between the two lasers (figure 3.23 (a)) was directly connected to the phase noise analyzer to measure the relative phase noise of the two lasers. This was measured for 1 Hz to 10 GHz offsets and compared to the the phase noise of the RF signal source and the background noise of the two broadband amplifiers. The measured single sideband phase noise is below -100 dBc/Hz at offsets 20 kHz, and shows two side peaks at approximately 1 GHz, indicating gain peaking near the loop bandwidth.



(a)



(b)

Figure 3.23: The homodyne OPLL performance.Beating lasers through the external photodiode to the electrical spectrum analyzer (ESA). Peak tone at 100 MHz and side tones at 1.0 and 1.2 GHz (a). Phase noise performance for the beating lasers and compared with the self-beating reference laser, RF signal phase nosie, and background noise through the amplifiers for the external PD thermal noise and shot noise (b).

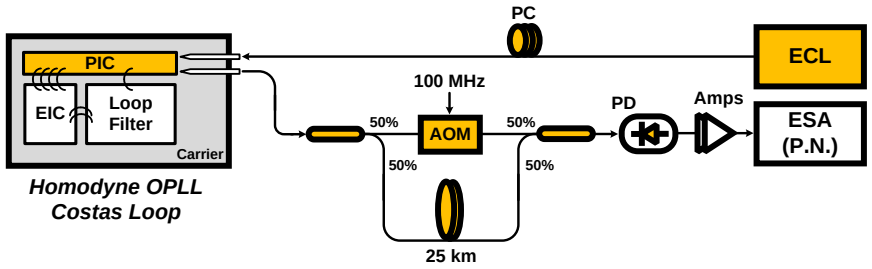


Figure 3.24: The test setup for the homodyne OPLL linewidth measurement experiments (self-heterodyne linewidth measurement technique) [46, 47].

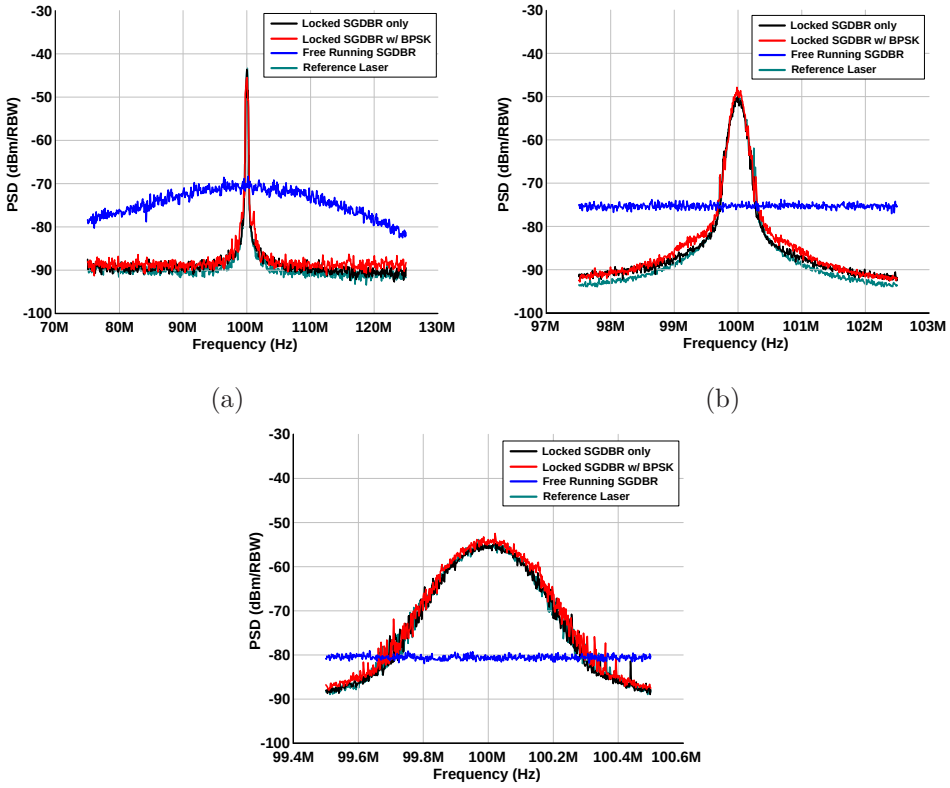


Figure 3.25: The homodyne OPLL linewidth measurement experiments. Self heterodyne linewidth measurements for the locked SG=DBR laser (black), locked SG-DBR laser with BPSK modulated input signals (red), free-running SG-DBR laser (blue), and reference laser (green):(a) RBW 20 kHz and span 50 MHz, (b) RBW 10 kHz and span 5 MHz, and (c) RBW 3 kHz and span 1MHz.

The second measurement of the homodyne OPLL performance is a linewidth measurement of the locked SG-DBR laser using the self-heterodyne linewidth measurement technique [46, 47]. This is shown in figure 3.24, and the linewidth result (black) is compared with the locked SG-DBR laser with a 25 Gb/s BPSK modulated signal (red), the reference laser (green) and a free-running SG-DBR laser (blue). As shown in figure 3.25, the free-running SG-DBR laser measured with the self-heterodyne technique shows approximately 10 MHz linewidth, while the locked SG-DBR laser shows $\sim$ 100 kHz linewidth. This is the same linewidth as the $\sim$100 kHz reference laser (figure 3.25). The locked SG-DBR laser can strongly track the reference in the homodyne OPLL. The result again verifies stable OPLL operation. To check stable operation, the homodyne OPLL was left running for over two hours during which time it maintained phase lock. Linewidth results with different spans and resolution bandwidths (RBWs) are shown in figure 3.25 (a)-(c).

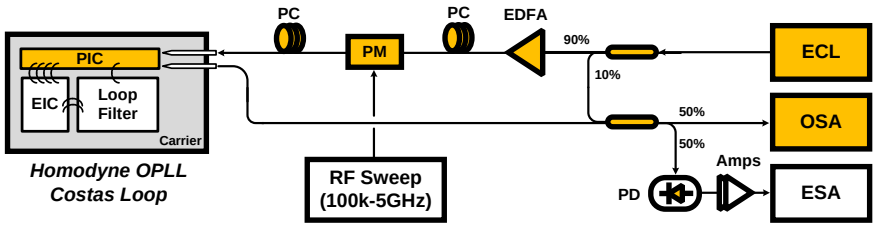


Figure 3.26: The test setup for the homodyne OPLL closed loop bandwidth measurement experiment using the phase modulation.

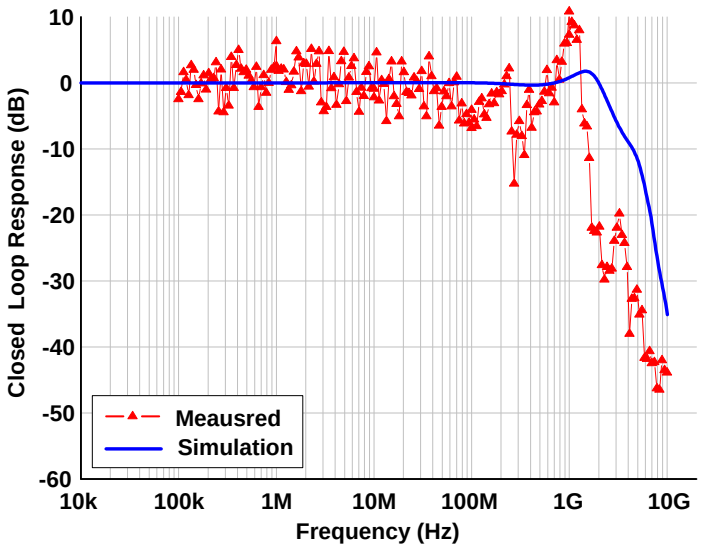


Figure 3.27: The homodyne OPLL closed loop bandwidth measurement experiment. Simulated and measured loop bandwidth results are shown and the results show $\sim$ 1 GHz closed loop bandwidth.

The third measurement of the homodyne OPLL performance is a closed loop bandwidth test using the setup of figure 3.26. In this experiment, the reference laser is phase modulated using a 40 GHz bandwidth optical phase modulator (PM). This response has been measured from 100 kHz to 5 GHz by monitoring the phase modulation using an electrical spectrum analyzer (ESA). The measured result is shown in figure 3.27. The frequency response was compared with the simulations of the closed loop response $H(s) = T(s)/(1+T(s))$. A slightly underdamped closed loop response is observed and the 3-dB frequency bandwidth of $H(s)$ is approximately 1 GHz.

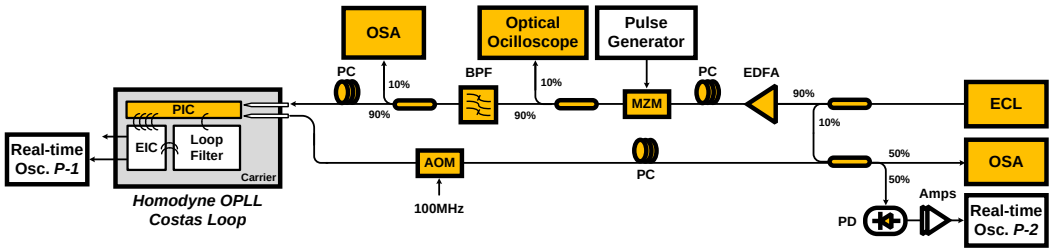
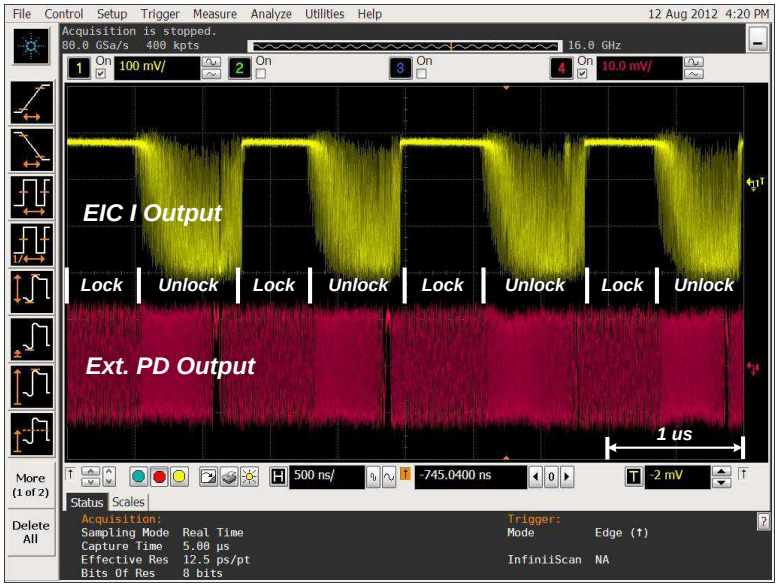
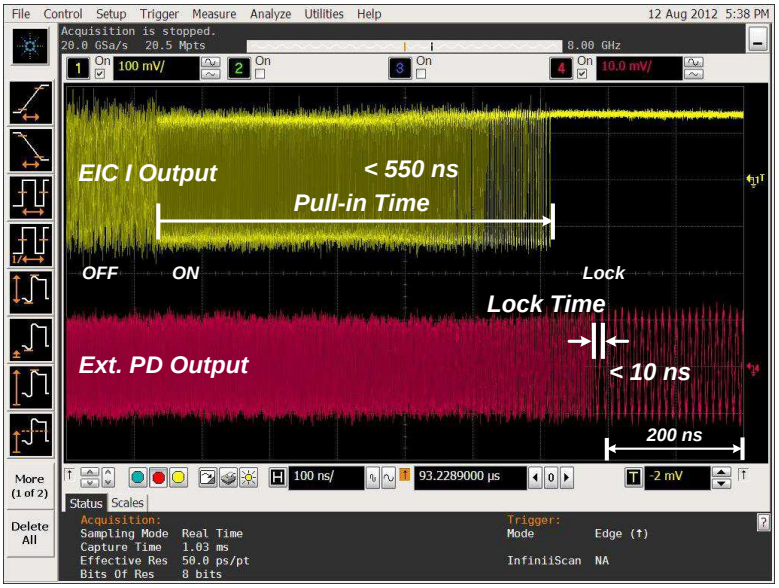


Figure 3.28: The test setup for the homodyne OPLL lock time experiments.



(a)



(b)

Figure 3.29: The homodyne OPLL lock time experiments. (a) Automatic phase lock acquisition monitoring through the real time oscilloscope for the on-off-keying reference input, and (b) pull-in time and lock-time monitoring for the worst measurement result.

Finally, the locking (settling) speed of the OPLL was measured. For this, we used a fast on-off-keying (OOK) modulator (40 Gb/s) with low speed modulation (1 MHz) on the reference laser path to turn on and off the transmitted BPSK-modulated reference signal. The data stream was modulated as a ∼1 MHz rate. This forces the OPLL to lose lock, and then acquire lock at this 1 MHz rate. Figure 3.28 shows the test setup, and figure 3.29 shows the outputs measured on a real time oscilloscope (DSO-X91604A - 40 GSa/s). The yellow trace is the EIC I-data output. Under the locked condition, the I-data output shoud be a logic high level, while under unlocked conditions this output rapidly alternates between binary 1 and binary 0. The red trace is the output of and external photodiode carrying the beat note between the reference laser and the locked laser. This beat note is modulated at 100 MHz using an acousto-optic modulator. Consequently, when the loop is locked, this will be a 100 MHz sinusoidal signal, while when the OPLL is not locked the signal will rapidly fluctuate in frequency and will appear as noise. As shown in figure 3.29 (a), the locked and unlocked condistions are repeated with a period of 1 μs. Figure 3.29 (b) shows a zoomed-in measurement of the worst-case locking time among various measurments. The frequency pull-in time is $\sim$ 550 ns, while the phase lock time is less than 10 ns. We estimate that the frequency deviation before locking is 3-4 GHz.

As the above measurements show, the homodyne OPLL suppresses the SG-DBR laser's free-running phase and frequency noise over a broad frequency range and extends the track and hold ranges against the received (reference) carrier frequency drift. Given the phase-frequency difference detection, the OPLL can maintain phase- and frequency-lock given an initial frequency offset of at least 3-4

GHz.

3.4.3 BPSK Receiver Experiments

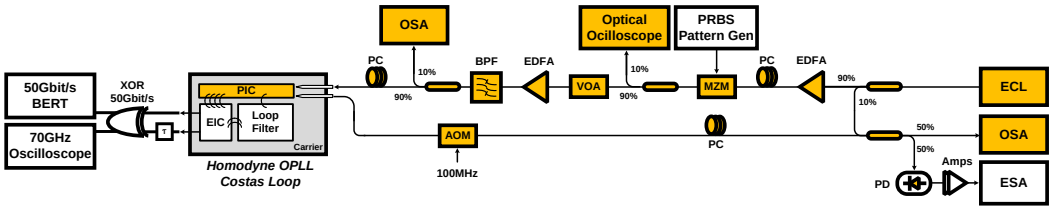


Figure 3.30: The test setup for the optical Costas loop receiver BER vs. OSNR experiments.

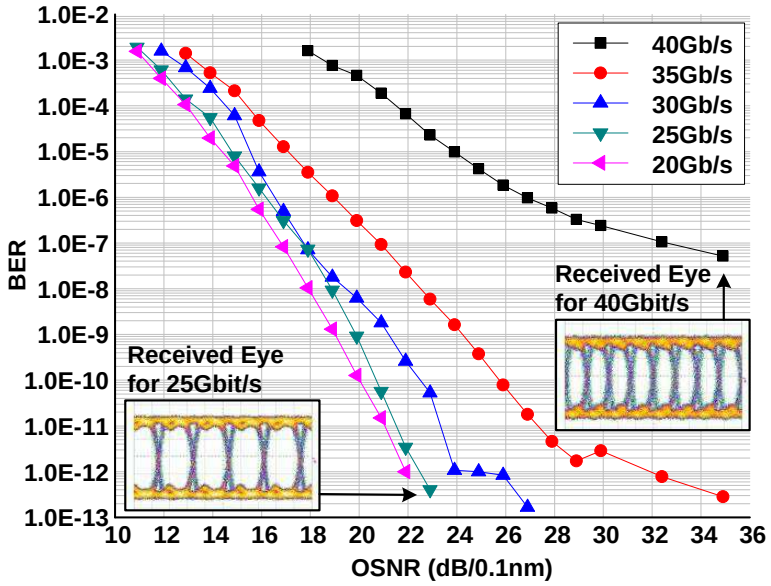


Figure 3.31: The measurement BER vs. OSNR results for the optical Costas loop from 10 Gb/s to 40 Gb/s. The eye diagrams for 25 Gb/s and 40 Gb/s are shown in the polot and they are measured directly to the sampling oscilloscope without the external 40 Gb/s XOR and phase shifters for the differential de-coding.

This homodyne OPLL can be used as a coherent optical receiver for binary PSK-modulated data. To demonstrate the BPSK coherent optical receiver performance, the bit-error-ratio (BER) vs. optical signal to ratio (OSNR) was measured using the test setup shown in figure 3.30. A PRBS $2^{31}-1$ pulse pattern generator and MZM are used for BPSK optical data modulation up to 40 Gb/s. The OSNR was controlled by a variable optical attenuator (VOA) at the input to before the Erbium doped fiber amplifier (EDFA), and optical band pass filter (BPF). Differential I-outputs from the EIC are connected a 50 Gb/s BERT measurement system through an external differential decoder formed from a high speed XOR gate and a 1-bit delay. This differential decode resolves the 180 degree phase ambiguity of the Costas loop, preventing a continuous stream of errors if the loops slips 180 degrees in phase. During this measurement, the lock status of the SG-DBR was monitored with an ESA.

The BER vs. OSNR was measured from 10 Gb/s to 40 Gb/s, as shown in figure 3.31. The coherent BPSK receiver exhibits nearly error-free operation (BER less than 10^{-12}) up to 35 Gb/s operation. It shows less than 10^{-7} error rate for 40 Gb/s operation. In addition, open received eye outputs were measured for 25 Gb/s and 40 Gb/s operation. This measurement used a 70 GHz sampling oscilloscope, was measured with a high OSNR, and was measured without using the external differential decoder. The demonstrated coherent optical receiver can demodulate up to 40 Gb/s BPSK data in real-time without the DSP and latency.

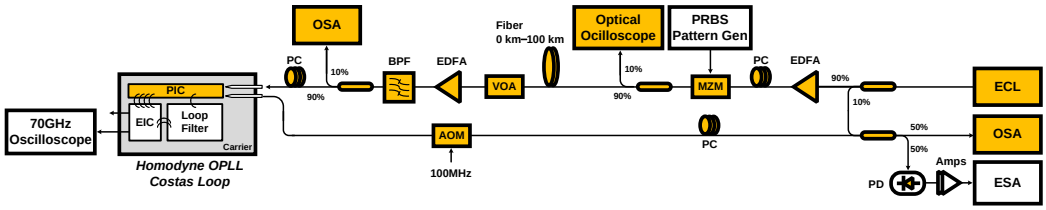


Figure 3.32: The test setup for the homodyne OPLL long-haul data reception experiments for the fiber lengths of 0 km to 100 km and the data rate of 10 Gb/s to 40 Gb/s.

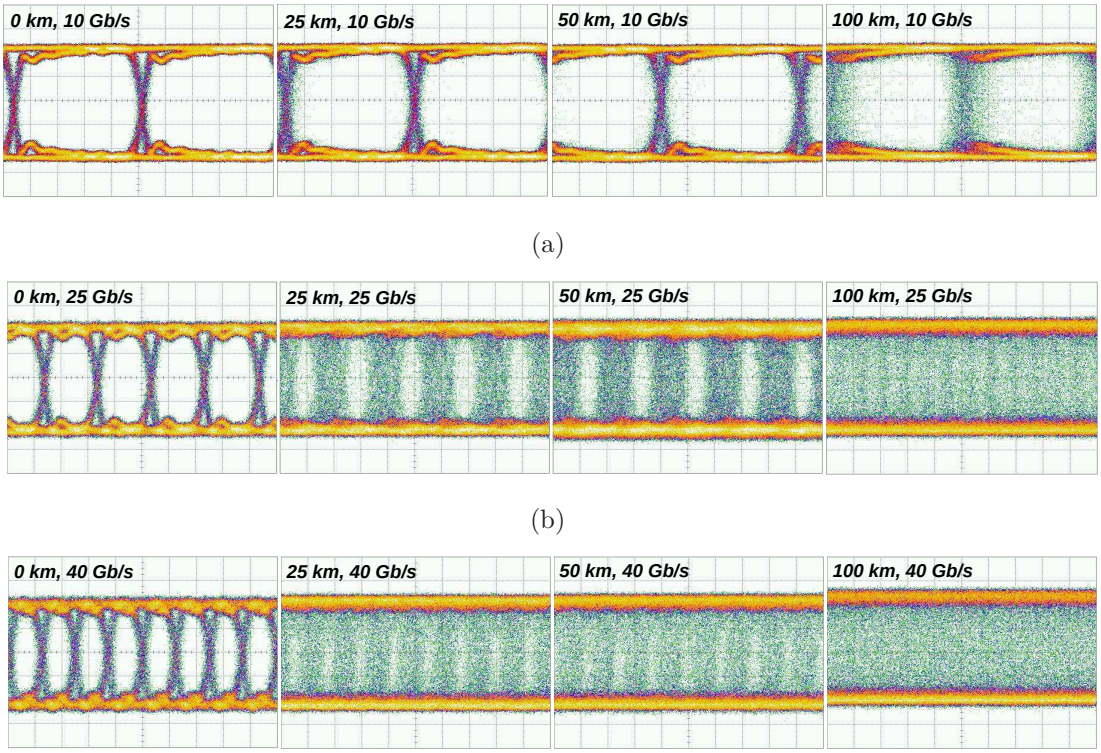


Figure 3.33: The eye-diagrams for the homodyne OPLL long-haul data reception experiments for the fiber lengths of 0 km - 100 km. (a) 10 Gb/s eye diagrams, (b) 25 Gb/s eye diagrams, and (c) 40 Gb/s eye diagrams.

Finally, long distance fiber dispersion effects on the optical homodyne OPLL and the Costas loop receivers were studied using the test setup shown in fig-

ure 3.32. The eye-diagrams were measured for BPSK modulated signals with varying bit rates from 0 Gb/s to 40 Gb/s, and with varying fiber distances of 0 km to 100 km. Figure 3.33 shows measured results. The chromatic dispersion is less than 18.0 ps/(nm·km) Corning's SMF-28e+ commercial optical fiber [48]. The effects of dispersion become more serious as data-rate and fiber length increase. At a short distance of 25 km with low bit-rates of 10 Gb/s eye-diagrams are still open. On the other hand, at high bit-rates of 40 Gb/s with even 25 km transmission, the eye-diagrams close. The signifcant result here is that the homodyne OPLL has kept phase lock even given serious fiber dispersion. This means it may be possible to use simple analog dispersion compensation filters between the PIC's PD outputs and the EIC's TIA inputs. Then, a high data rate of more than 40 Gb/s for the short-link up to 100 km is feasible with the coherent heterodyne OPLL scheme using the Costas loop.

3.5 Conclusion

In this chapter, a highly integrated homodyne OPLL based coherent optical receiver was demonstrated using a Costas loop. The photonic circuits and electrical circuits were designed and fabricated using UCSB facility for optical ICs and the Teledyne InP HBT process for electrical ICs, this giving a high data rate and small loop delay. The PIC and EIC were fully characterized for the OPLL feedback loop design, and their OPLL operation was examined in detail. Key features include the PIC's balanced detection with quadrature current outputs, the EIC's binary phase detection and linear frequency detection, and the novel feed-forward

dual-path loop filter. With these a stable OPLL has been demonstrated within a compact size $10 \times 10\ mm^2$ module. Measured characteristics include a closed loop bandwidth of 1.1 GHz, 120 ps effective loop propagation delay through the feed-forward loop path, 100 kHz locked SG-DBR laser linewidth (the same as the reference laser linewidth), a frequency pull-in time of 550 ns, and less than 10 ns lock-in time. The homodyne OPLL based coherent BPSK optical receiver exhibits error-free (BER less than 10^{-12}) up to 35 Gb/s and BER less than 10^{-7} for 40 Gb/s. The receiver consumes less than 5 W power (PIC: 0.5 W, EIC 4.2 W and loop filter: 0.1 W).

Future work would include demonsatration of improved homodyne OPLL architectures QPSK modualtion, possibly 16-QAM modulation, dispersion compensation in the analog signal path after the OPLL, and polarization insensitive OPLLs.

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Chapter 4

Heterodyne OPLLs for Wavelength Synthesis

This chapter describes my work at UCSB in collaboration with M. Lu and E. Bloch. This work was supported by the DARPA Photonic Integration for Coherent Optics program (PICO). M. Lu and I had worked many long hours in Prof. L. Coldren's lab in an attempt to demonstrate our first OPLL. An initial result with locking turned out to be not due to electrical phase-locking but due to optical injection locking. In the course of these experiments, we discovered that the OPLL failed to operate because of large DC and signal imbalances from the photodetectors on the PIC, and from the low optical power levels. We were able to suppress the DC imbalances, and demonstrate a working OPLL, by adding four RF-chokes at the signal connections between the EIC and PIC, these chokes short-circuiting the ports at DC and thereby suppressing the DC imbalance. This result was the first highly integrated heterodyne OPLL for which the offset frequency

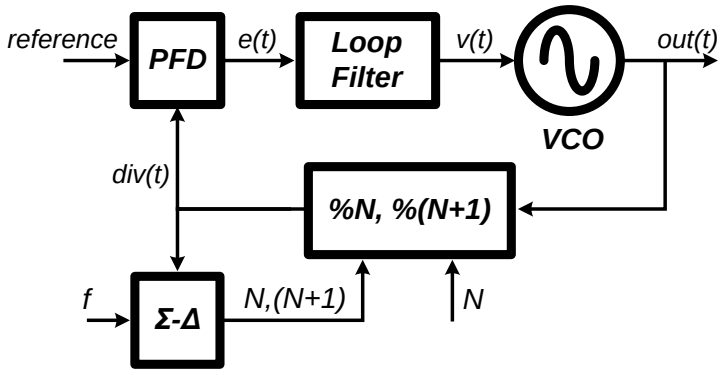
sign could be controlled. This heterodyne OPLL provided over ±1.5 GHz to ±9 GHz frequency tuning range.

Following this first result, we improved the PIC, and the OPLL, allowing a wider frequency tuning range. Frequency offsets from ∼ ±1 GHz to ±20 GHz can be produced by changing only the RF offset generator frequency. No laser bias tuning is required similar to the previous chapter describing the homodyne OPLL, many key techniques were developed to demonstrate a stably-operating heterodyne OPLL. These include 1) EICs with an all digital single sideband mixer (D-SSBM) with Quadri-correlator phase-frequency detector (PFD), developed by Eli Bloch [1,2], 2) enhanced PIC designs giving larger output currents and better signal balance, fabricated by M. Lu [3–8], and 3) a dual-path (feed-forward) loop filter within a highly integrated OPLL. Many experiments [7, 8] were performed using this system.

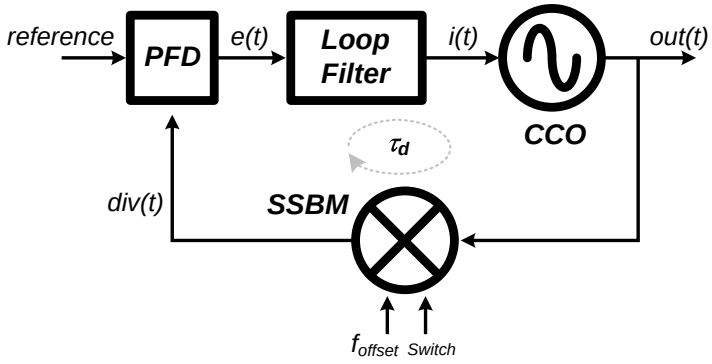
In this chapter, we describe our development and demonstration of a stably operating heterodyne OPLL having a wide frequency offset locking range of over ±25 GHz. In section 2, I will briefly describe optical frequency synthesizers and compare these to PLL based electrical frequency synthesizers. In section 3, I will briefly describe component characteristics of our heterodyne OPLL designs. The EIC, and its digital single sideband mixers (DSSBM) and Quadri-correlator PFD will be described in detail. In section 4, I will describe the dual-path loop filter and describe how to reduce the OPLL feedback loop propagation delay. In section 5, I will show the heterodyne OPLL implementation and experimental results. I will also describe the OPLL's phase noise. Finally, I will summarize this chapter by describing several possible future research directions.

4.1 Motivation and Background

Phase locked loops (PLLs) have been widely used in electrical systems as frequency synthesizers, and for clock recovery in wireline and wireless communications, radar, computers, and other applications [9–17]. PLLs in electrical systems are generally integrated, use a crystal oscillator as a reference oscillator, and precisely set and rapidly tune frequencies under complicated digital controls as shown in figure 4.1 (a).



(a)



(b)

Figure 4.1: Block diagrams for frequency synthesizers. An electrical PLL using the fractional-N divider using a sigma-delta modulator (a), and a direction selectable heterodyne optical PLL (OPLL) using a single sideband mixer (SSBM) and an external RF signal (b).

On the other hand, optical phase locked loops (optical PLLs or OPLLs) have not yet fully matured. Optical phase lock loops would enable many coherent optical applications, including coherent optical communications, high resolution image sensing in LIDAR, THz-signal generation, and optical phased arrays [18–22]. Since the OPLLs were proposed in 1965 [23], they have been an important area of research. Research demonstrations include stable OPLLs with narrow-linewidth external-cavity lasers [24–28], packaged OPLLs using micro-optics [29], loops using a combination of optical injection-locking and electrical phase-locking [18], homodyne OPLL using discrete high speed FETs in the loop filter [30], and a highly integrated heterodyne offset locking using an exclusive-OR (XOR) for a phase detection [19]. Early OPLL research in, the 1980's and 1990's was target towards developing sensitive coherent (phase sensitive) optical receivers to extend the reach of optical fiber communications [31–33].

In this prior work, it was noted that OPLL design is challenging [4–8, 18–21, 29–31, 34], despite the simple structure of a heterodyne OPLL (figure 4.1 (b)). One critical consideration is the loop bandwidth. If the loop has a long propagation delay, then the loop bandwidth must be narrow. A narrow loop bandwidth can suppress phase and frequency noise only over a narrow frequency range, and has limited frequency tracking ranges and tracking speed. Much OPLL research has focused on minimizing the feedback loop delay. It is difficult to reduce this delay because of long path lengths in free-space optics [29], and long interconnection delays in electrical circuits constructed on printed circuit boards [19]. The OPLL feedback loops can also be sensitive to optical intensity fluctuations caused mechanical vibrations and optical frequency drifts caused by temperature changes.

To address these issues, in this work we implemented highly integrated heterodyne OPLLs within a compact size of $10 \times 10\ mm^2$ using a photonic integrated circuit, an electrical integrated circuit, and a hybrid loop filter. The total effective loop delay of the OPLL was reduced to less than 200 ps. This can enable at least 500 MHz loop bandwidth. A novel all-digital single-sideband mixer (D-SSBM) with a quadri-correlator phase and frequency detector (PFD) was designed [1, 2] using Teledyne's 500 nm InP HBT IC technology. The D-SSBM allows optical frequency synthesis with control of the sign of the frequency offset between the two lasers, while the PFD provides a wide frequency acquisition range. A dual-path (feed-forward) loop filter minimizes the loop delay and to allow us to realize even 500 MHz bandwidth loops with op-amplifiers of relatively limited bandwidth. As a result, our heterodyne OPLL operates stably, has a wide frequency tuning range of ±25 GHz, and exhibits phase noise of -80 dBc/Hz and -110 dBc/Hz at 10 kHz and 10 MHz offsets from carrier. The PIC device characteristics have been discussed in the previous chapter and in [3–5]. Therefore this chapter will primarily focus on describing the EIC, the dual-path (feed-forward) loop filter analysis, and the design of the full heterodyne OPLL.

4.2 Basic Heterodyne OPLLs and Design Challenges

However, loop configurations and critical design issues of electrical optical PLLs differ. A classic frequency synthesizer (figure 4.1 (a)) consists of a phase and frequency detector (PFD), a loop filter, a voltage-controlled-oscillator (VCO),

and a frequency divider modulated under sigma-delta for frequency tuning under digital control. In an electrical PLL a second-order feedback loop is commonly used because of relatively simple topology and because of zero static phase error even when tuned in frequency. For such a second-order loop, the loop transfer function $T_{PLL}(s)$ is

$$T_{PLL}(s) = K_{PD} \cdot K_{VCO} \cdot \frac{F(s)}{s}, \tag{4.1}$$

where K_{PD} is the phase detector gain $[V/rad]$, K_{VCO} is the VCO tuning sensitivity $[rad/sec/V]$, the integration term $1/s$ arises from frequency to phase conversion $[sec]$, and $F(s)$ is the loop filter voltage gain. Given that the VCO provides the first loop integration, the loop filter transfer function $F(s)$ for a second order loop is

$$F(s) \approx \frac{\tau_2 s + 1}{\tau_1 s}, \tag{4.2}$$

where τ_1 is the filter integrator time constant and τ_2 is the time constant associated with the compensation zero which is required for a stable second-order loop. The closed-loop transfer function $H_{PLL}(s)$ is then

$$H_{PLL}(s) = \frac{K_{PD} \cdot K_{VCO} \cdot \frac{F(s)}{s}}{1 + K_{PD} \cdot K_{VCO} \cdot \frac{F(s)}{s}}. \tag{4.3}$$

A heterodyne OPLL used in an optical wavelength synthesizer presents several design challenges not present in an electrical PLL. As shown in figure 4.1 (b), an OPLL has a frequency-tunable laser. This laser is an integrated tunable laser in our OPLL designs, and is a current-controlled-oscillator (CCO). Other OPLL components include a single sideband mixer (SSBM) to introduce a frequency offset with controlled (+ or -) sign, a high-speed PFD, and a wide bandwidth loop filter. The frequency of the optical local oscillator (LO) laser, at ∼194 THz (1550

nm wavelength), is much higher than the VCO frequency in common mobile RF frequency synthesizers at 500 MHz - 2 GHz [9,10,13–16,16,17]. Therefore, initial frequency offsets, the frequency drifts, and the oscillator phase-noise bandwidths are all much larger than with electrical oscillators. For example, the integrated tunable lasers used in the OPLLs have ∼5 MHz linewidth and several 10's or even 100's of MHz of frequency drift [3,4]. Hence, the OPLL design needs to have a wide loop bandwidth $\omega_n/2\pi$, c.a. 500 MHz in our integrated OPLL designs. A small OPLL loop delay τ_d is therefore critical. As mentioned in the chapter describing the integrated OPLL, the loop bandwidth sets the bandwidth over which the LO laser noise is suppressed, and sets the frequency lock-in range and pull-in speeds. Hence, though challenging to attain, wide loop bandwidths are necessary.

The phase shift θ_e introduced by the loop delay τ_d at the loop bandwidth ω_n is

$$\theta_e = \tau_d \times \omega_n. \tag{4.4}$$

For a stable feedback loop this phase shift must be at most $\theta_e < 0.736$ when other poles in the loop transfer function are considered [35]. Delay less than 1.0 ns and 100 ps are required for loop bandwidths of 100 MHz and 1 GHz, respectively. The propagation loop delay must be minimized, and the effects of the loop delay must be carefully considered in the design of the OPLL .

The OPLL loop transmission is

$$T_{OPLL}(s) = K_{PD} \cdot K_{CCO} \cdot \frac{F_{OPLL}(s)}{s} \cdot e^{-\tau_d s}, \tag{4.5}$$

where K_{CCO} is the laser tuning sensitivity $[rad/sec/mA]$, $F_{OPLL}(s)$ is the OPLL loop filter transfer function $[A/V]$, and $e^{-\tau_d s}$ arises from the loop delay. The closed

loop response $H_{OPLL}(s) = T_{OPLL}/(1 + T_{OPLL})$ is

$$H_{OPLL}(s) = \frac{K_{PD} \cdot K_{CCO} \cdot \frac{F_{OPLL}(s)}{s} \cdot e^{-\tau_d s}}{1 + K_{PD} \cdot K_{CCO} \cdot \frac{F_{OPLL}(s)}{s} \cdot e^{-\tau_d s}}. \tag{4.6}$$

In the following sections, more OPLL design will be described in detail. Due to the wide loop bandwidth, many minor parasitics must be carefully considered. Key parameters in the PIC, EIC, and loop filter will be carefully characterized

4.3 Heterodyne OPLL Architecture

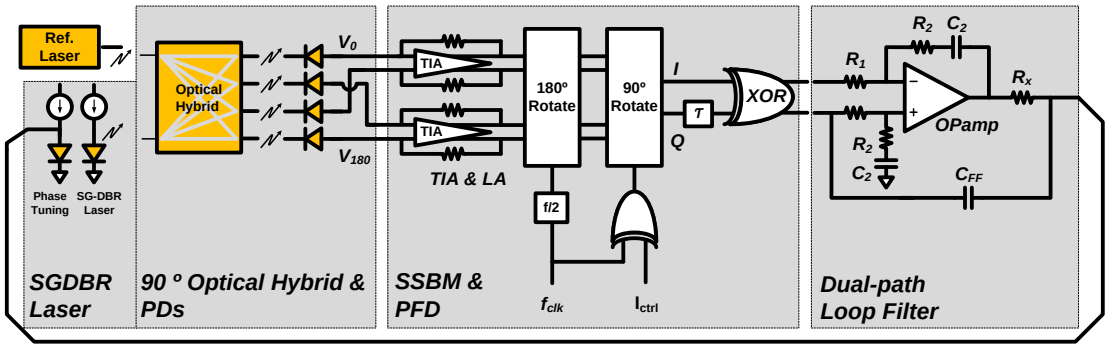


Figure 4.2: A full heterodyne OPLL architecture including three main blocks of the PIC, EIC and loop filter. (SG-DBR: sampled grating-distributed Bragg reflector, TIA: trans-impedance amplifiers, LA: limiting amplifiers, SSBM: single side band mixer, and PFD: phase and frequency detector)

The full architecture of the heterodyne OPLL is shown in figure 4.2. It consists of three main blocks: a photonic integrated circuit (PIC), an electrical integrated circuit (EIC), and a dual-path loop filter. In this section, the detailed device characteristics will be described and the feedback loop will be analyzed. Goals for our heterodyne OPLL design include: less than total 200 ps propagation loop delay, wider than 500 MHz loop bandwidth, a sign-selectable frequency offset

controlled by the EIC, frequency synthesis by an RF signal source, frequency synthesis over as wide a frequency tuning range as possible, a highly integrated OPLL in a single carrier board, and stable operation.

4.3.1 The Photonic IC

The PIC in turn consists of three main blocks: a sampled grating-distributed Bragg reflector (SG-DBR) laser, a 90 degree optical hybrid, and four single-ended uni-traveling carrier (UTC) photodiodes (PDs) as shown in 4.2. The SG-DBR laser wavelength is widely tunable over 40 nm (>5 THz band) in wavelength by injecting current into to the laser front mirror, back mirror and phase-tuning diode sections. The front and back mirrors are used for rough wavelength tuning, and only the phase-tuning section is controlled by the OPLL feedback loop.

This PIC operation is simply analyzed with following equations. The reference laser field $E_{ref}(t)$ is defined as

$$E_{ref}(t) = A_{ref} \cdot cos(\omega_{ref} t + \theta_{ref}), \tag{4.7}$$

where A_{ref} is the intensity of the reference laser, ω_{ref} is the laser frequency, and θ_{ref} is the laser phase. As similar, the LO laser (SG-DBR laser) field $E_{LO}(t)$ is also defined as

$$E_{LO}(t) = A_{LO} \cdot cos(\omega_{LO} t + \theta_{LO}), \tag{4.8}$$

where A_{LO} is the intensity of the LO laser, ω_{LO} is the laser frequency, and θ_{LO} is the laser phase. The two optical fields of equations 4.7 and 4.8 are mixed by the 90 degree optical hybrid and down-converted through the single-ended PDs

to obtain four quadrature phase photocurrents $I_0(t)$ - $I_{270}(t)$ as

$$\begin{aligned} I_0(t) &= I_{DC} + R{\cdot}cos[(\omega_{ref} - \omega_{LO})t + \theta_{ref} - \theta_{LO}] \\ I_{90}(t) &= I_{DC} + R{\cdot}sin[(\omega_{ref} - \omega_{LO})t + \theta_{ref} - \theta_{LO}] \\ I_{180}(t) &= I_{DC} - R{\cdot}cos[(\omega_{ref} - \omega_{LO})t + \theta_{ref} - \theta_{LO}] \\ I_{270}(t) &= I_{DC} - R{\cdot}sin[(\omega_{ref} - \omega_{LO})t + \theta_{ref} - \theta_{LO}] \end{aligned} \tag{4.9}$$

where I_{DC} is a DC photocurrent which is proportional to the intensities of both laser powers, R is the amplitude of the AC current outputs, and depends upon the laser intensities and the PD responsivity, $\omega_{ref} - \omega_{LO}$ is the frequency offset between two lasers, and $\theta_{ref} - \theta_{LO}$ is a phase error. In our OPLL design, the current I_{DC} will be removed by subtraction in the EIC differential amplifiers. Further, the AC outputs will be converted to binary levels (digitized) by limiting amplifier chains in the EIC to make the IC operation insensitive to intensity fluctuations from the PIC. The frequency and phase information in the limited square wave signals will be used by the OPLL feedback loop. It is necessary to have the both quadrature $I - Q$ current outputs (equation 4.9) to operate the single-sideband mixers for sign-selective (+ or -) frequency synthesis.

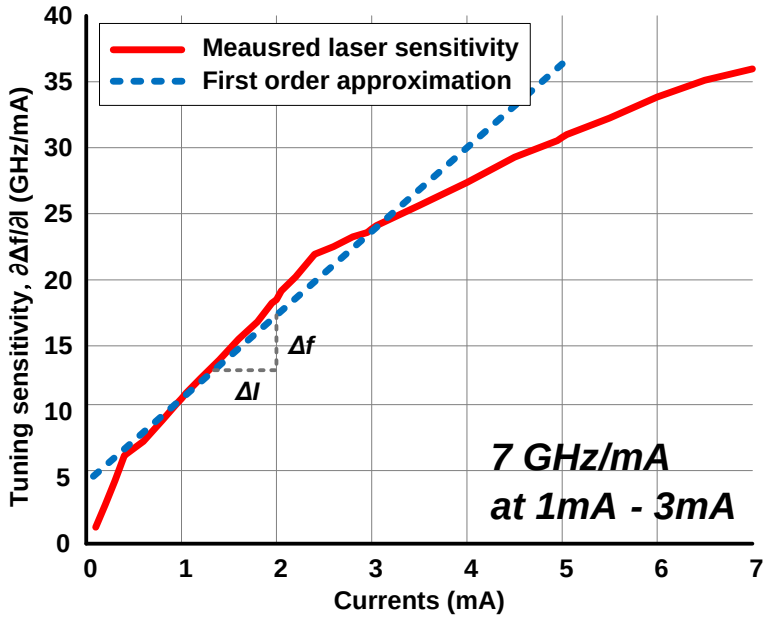


Figure 4.3: Measured SG-DBR laser tuning sensitivity of 7 GHz/mA ($2\pi \times 7 \times 10^{12}$ $[rad/sec/A]$). The first order approximated laser tuning gain has been obtained the DC bias ranges 1-3 mA.

To build a stable OPLL feedback loop, the PIC was carefully characterized. The SG-DBR laser can tune over a wide wavelength range, and hence has a large tuning sensitivity (tuning gain), as is shown in figure 4.3. The laser tuning gain of $K_{CCO} = 2\pi \times 7 \times 10^{12}$ $[rad/sec/A]$ is determined from this measurement (figure 4.3) for DC bias currents of 1-3 mA. the laser wavelength responds only slowly to tuning currents in the phase tuning section diode, as a results of the minority carrier transient time τ_{tune}. This tuning characteristic can be represented as a single pole frequency response as

$$\frac{1}{1 + \tau_{tune} s}. \tag{4.10}$$

The corresponding measured pole frequency, is approximately 100 MHz [5]. Since this pole frequency lies inside of the target loop bandwidth of 500 MHz, this

laser parasitic pole frequency must be considered, and compensated for the OPLL feedback loop design. Adding one zero ($1+\tau_{zero}s$) to the loop filter will compensate the laser pole if $\tau_{zero} = \tau_{tune}$.

As noted in prior chapters, the UTC PD has more than 30 GHz 3-dB bandwidth. While this is vastly larger than the target loop bandwidth, this parameter does limit the OPLL tuning range. By integrating all optical components into a single InP/InGaAs platform, total PIC delay is small at ∼40 ps.

We again give a summary of the PIC characteristics, this being the same PIC that was used in the homodyne OPLL of the previous chapter.

Table 4.1: Summary of the PIC device parameters for the heterodyne OPLL design

Parameters	Value	Unit	Descriptions
	1/s	1/sec	Phase/frequency: $\Theta(s) = F(s)/s$
K_{CCO}	$2\pi \times 7 \times 10^{12}$	rad/A	Laser tuning sensitivity
τ_{tune}	$1/(2\pi \times 100 \times 10^6)$	sec	Tuning frequency responsivity
τ_{PD}	$1/(2\pi \times 35 \times 10^9)$	sec	PD 3-dB pole frequency
τ_{d-PIC}	40	ps	Total delay in the PIC

4.3.2 EIC: Digital-Single Sideband Mixers (D-SSBM) and Phase Frequency Detector (PFD) operation

The EIC integrates high speed analog and digital circuits and minimizes critical interconnection delay, while providing the loop's key high speed electrical features. The EIC has been designed in Teledyne's 500 nm InP HBT technology (300 GHz f_τ and f_{max}). The EIC includes several key blocks. Input biasing circuits supply a negative voltage bias of around -2 V to the arrays of single-ended

PDs and terminate these connections in 50 Ω. Five-stage Darlington g_m-block limiting amplifiers are cascaded to amplify the in-phase I (V_0) and quadrature-phase Q (V_{90}) signals and to limit these to binary values at 0.3 V_{pp} amplitude paths. The digitized square-wave signals are insensitive to fluctuations in the PIC output current, either short-term or due to component fabrication variations. This limiting technique makes the OPLL robust with regard to chip-chip variations in the power levels and photocurrents within the PIC. Given this limiting, the output signals carry only phase and frequency information. The quadrature outputs of the differential limiting amplifier chains $V_0(t)$ and $V_{90}(t)$ become

$$\begin{aligned} V_0(t) &= 0.3sgn[(\omega_{ref} - \omega_{LO})t + \theta_{ref} - \theta_{LO} + \pi/2] \\ V_{90}(t) &= 0.3sgn[(\omega_{ref} - \omega_{LO})t + \theta_{ref} - \theta_{LO}], \end{aligned} \tag{4.11}$$

where the function sgn is a sign function, i.e. $sgn(x) = 1$ for $x > 1$ and $sgn(x) = 0$ for $x < 1$.

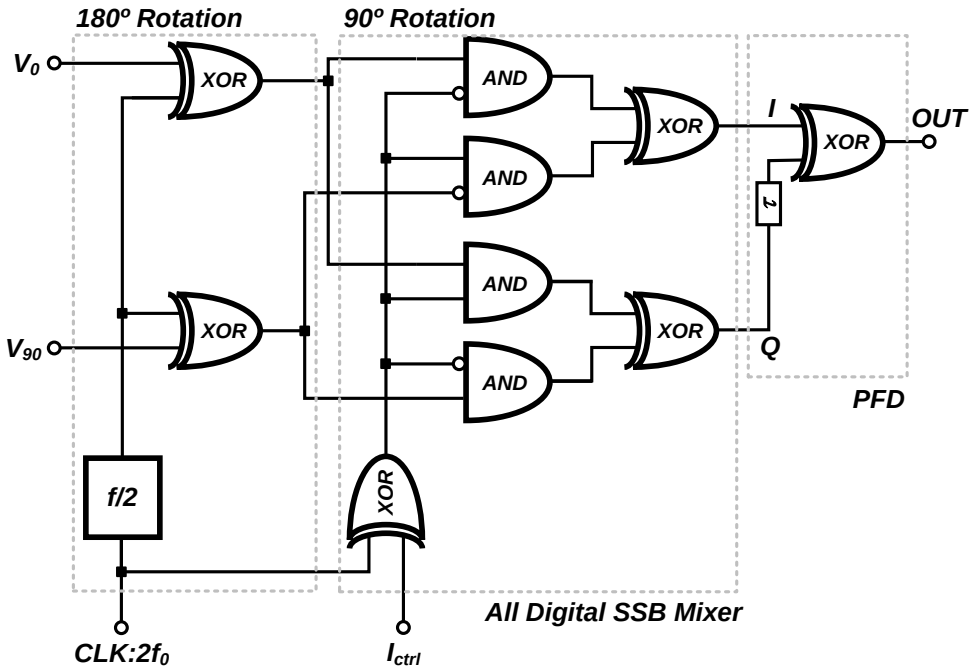
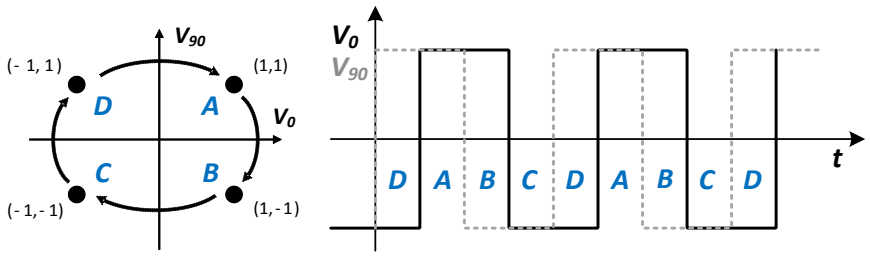


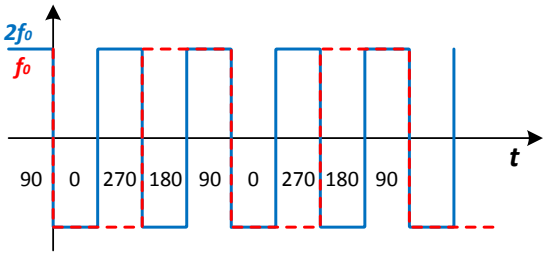
Figure 4.4: The core blocks of the EIC including the Digital-single sideband mixer (D-SSBM) and Quadri-correlator PFD. Courtesy of E. Bloch [1, 2]

To process these digitized signals (equation 4.11), all circuits within the digital single side-band mixer (D-SSBM) and the phase-frequency detector were designed with using high-speed emitter-coupled-logic (ECL) gates. Design of this IC was by Bloch *et al.* [1, 2]. The D-SSBM (figure 4.4) consists of two main blocks, a 180 degree rotation block using two XOR gates with a $2f_0$ clock signal, and a 90 degree rotation block using a combinations of (N)AND and XOR gates with f_0 clock signal input.



(a)

f0	2f0	Rotation
0	0	0°
0	1	90°
1	1	180°
1	0	270°



(b)

Figure 4.5: The logic status for the DSSB operations: (a) The limiting amplifier outputs of V_0 and V_{90}. The 90 degree out-of-phase output signals have four different status. (b) The RF offset frequency inputs (f_0 and $2f_0$) have the DSBBM rotation status. Courtesy of E. Bloch.

The phase state of the input digital signals $V_0(t)$ and $V_{90}(t)$ are represented as only four states, represented by A-D in figure 4.5. Similarly, and the phase of the RF frequency offset signal applied from the synthesizer (f_0 and $2f_0$) can also be represented, to two-bit precision, as four status conditions of 0-270 degree rotations. In the IC design, the delay between the two clock frequency paths at $2f_0$ and f_0, and the two blocks of 180 degree and 90 degree rotation blocks must to carefully matched. The single sideband frequency offset sign (direction) is determined by a control bit I_{ctrl} port in the $2f_0$ path through an XOR gate.

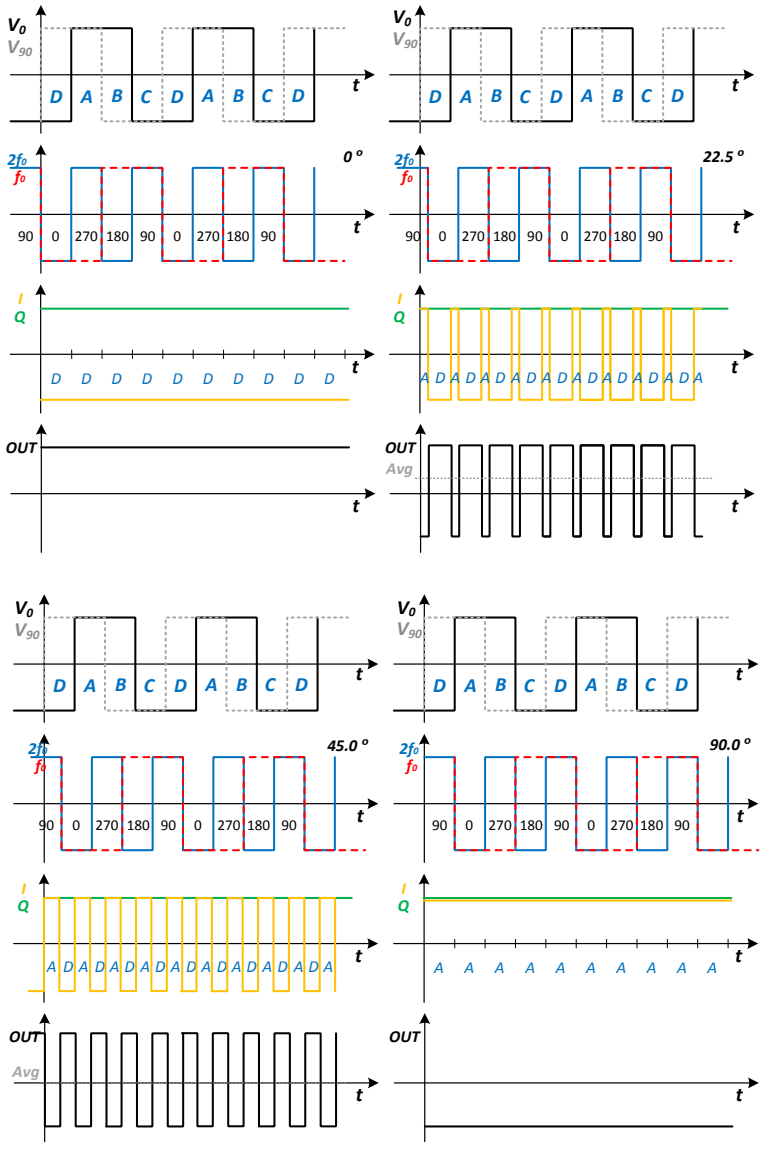


Figure 4.6: The time domain phase detection mode analysis with the D-SSBM and PFD rotation status.

To understand the EIC's phase and frequency detection mode working through the D-SSBM and PFD, digital logic timing diagrams are used to analyze the operation of each block, as shown in figures 4.6 and 4.8. Figure 4.6 analyzes the

phase detection mode if $f_0 = (\omega_{ref} - \omega_{LO})/2\pi$. To compared the outputs, the phase of the RF offset (clock) frequencies f_0 and $2f_0$ are shifted from 0 degree (first), 22.5 degree (second), 45 degree (third) to 90 degree (fourth), and the phases of the input signals $V_0(t)$ and $V_{90}(t)$ are now fixed for this analysis. In the I and Q results, while the phase of RF offset (clock) frequencies are shifted from 0 degree to 90 degree, the I-output changes its sign from (-) to (+) with different duty cycles and the Q-output has a fixed condition of (+). This means the status of the $I - Q$ outputs alternate between the D and A states. If the RF offset (clock) frequency is shifted from 90 degree to 180 degree phase, the $I - Q$ outputs oscillate between the A and B states, as well. Thus, the PFD outputs OUT have varying duty cycles of from 0% (first), 25% (second), 50% (third) and 100% (fourth), respectively. The time-averaged PFD output thus varies, and has a linear variation with the phase of the RF offset clock signal. Using the results (figure 4.6) and its expansion (0 to 2π), the heterodyne OPLL has stable phase lock conditions of the phase difference $\theta_{ref} - \theta_{LO} - \theta_0 = 45$ or 225 degrees. On the other hands, the phase differences 135 and 315 degrees are unstable positive loop conditions. Note in particular that the PFD output signal is independent of the amplitude of the photocurrents produced by the PIC.

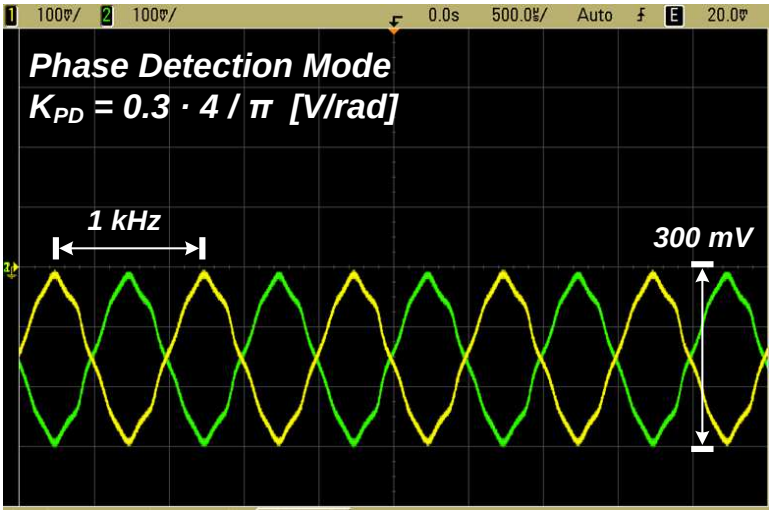


Figure 4.7: The measurement results for the phase detection mode. The results show a 0.3 V_{pp} periodic triangular waveform with a cycle of π. Courtesy of E. Bloch

Measured operation of the EIC in phase detection mode as shown in figure 4.7 using very low frequency offset $(\omega_{ref} - \omega_{LO} - \omega_0)/2\pi$= 1 kHz. The EIC output was electrically low-pass filtered and then measured on a digital sampling oscilloscope. The measurement shows a nearly linear variation in output with phase difference between 0 and 90 degrees, with a periodic triangular waveform with a cycle period of π, and a linear phase detection gain of $K_{PD} = 2 \times 0.3 \times 4/\pi$ $[V/rad]$ between 0 - 90 degrees. This phase detection result is represented as

$$OUT(\theta_e) = 0.3 \int sgn[sin(2\theta_e)]d\theta_e, \tag{4.12}$$

where $\theta_e = \theta_{ref} - \theta_{LO} - \theta_0 - \pi/8$. This result is similar to the characteristics of an XOR-gate phase detector [11, 12].

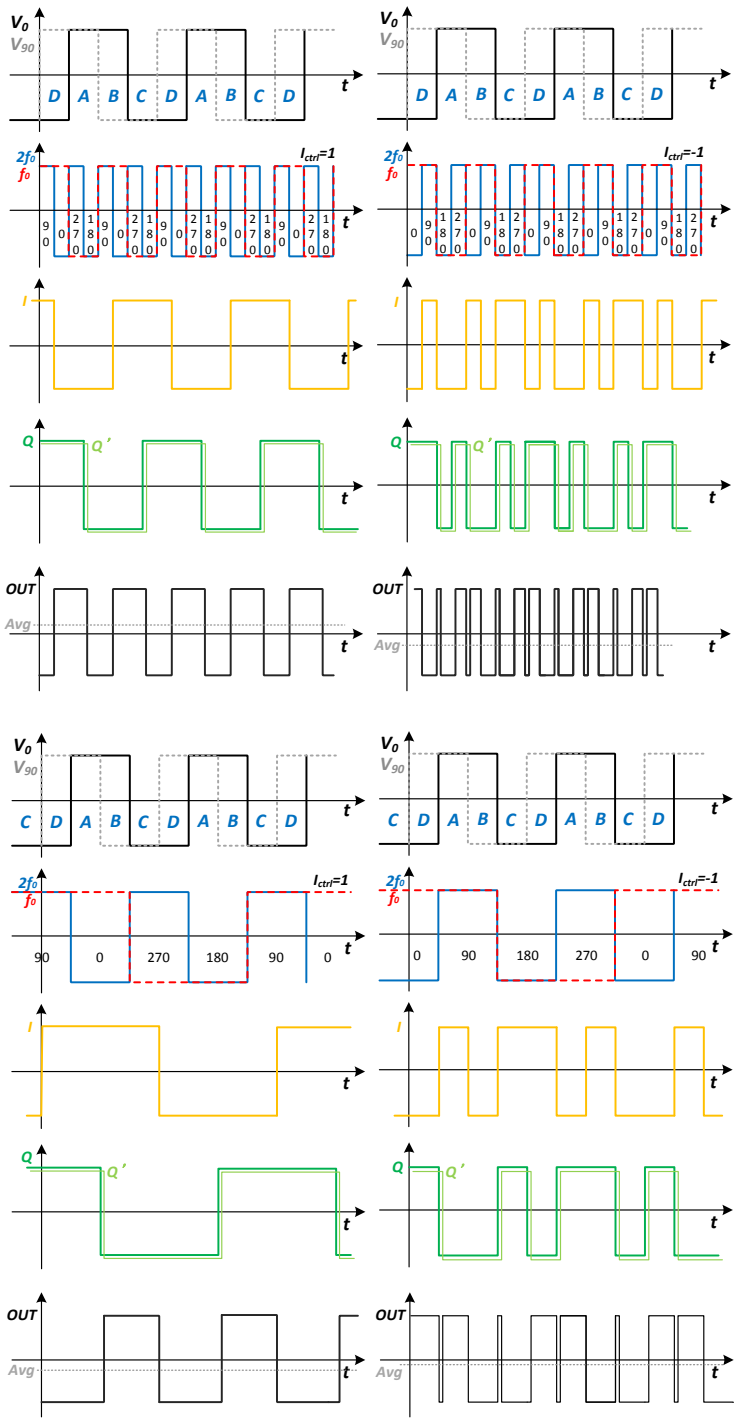


Figure 4.8: The time domain frequency detection mode analysis with the DSSBM and PFD rotation status.)

Operation in frequency detection mode is analyzed and shown in figure 4.8, when $f_0 \neq (\omega_{ref} - \omega_{ref})/2\pi$, and four different detection conditions are graphically analyzed: 1) $f_0 = 2 \times (\omega_{ref} - \omega_{LO})/2\pi$ with (+) I_{ctrl}, 2) $f_0 = 2 \times (\omega_{ref} - \omega_{LO})/2\pi$ with (-) I_{ctrl}, 3) $f_0 = 1/2 \times (\omega_{ref} - \omega_{LO})/2\pi$ with (+) I_{ctrl}, and $f_0 = 1/2 \times (\omega_{ref} - \omega_{LO})/2\pi$ with (-) I_{ctrl}. The D-SSBM I and Q outputs show single sideband operation as expected: 1) $2 \times (\omega_{ref} - \omega_{LO})/2\pi - f_0$, 2) $2 \times (\omega_{ref} - \omega_{LO})/2\pi + f_0$, 3) $1/2 \times (\omega_{ref} - \omega_{LO})/2\pi - f_0$, and 4) $1/2 \times (\omega_{ref} - \omega_{LO})/2\pi + f_0$, and I and Q outputs still have digital and quadrature outputs. Using the quadri-correlator PFD (the Q output is delayed in time by τ, producing the signal Q'. This produces a phase shift of $\omega_e\tau$, which is proportional to the frequency error ω_e. The delayed Q' output and the I output are then multiplied by a high speed XOR gate. The output of the XOR gate has a duty cycle which then varies in proportion to the frequency error f_e. In frequency detection mode, the phase-detector output is

$$OUT(f_e) = 0.3 \int sgn[sin(2\pi f_e \tau)] df_e, \tag{4.13}$$

where the delay τ of 10 ps is set in the EIC designs, and therefore, this PFD has a 50 GHz frequency detection range. As shown in figure 4.8 (first) and (third), the average PFD output is varies with the difference between the RF synthesizer frequency and the laser beat-note frequency. The PFD output is zero is when $f_e = 0$ with the phase error $\theta_e = 0$ or 180 degrees.

Operation of the frequency difference detector was measured with the PIC and EIC connected together with offset (clock) frequencies of f_0 = -12 GHz, +6 GHz, +12 GHz and +20 GHz as shown in figure 4.9. The results show proper frequency detection to within a ~0.5 GHz error. Because this frequency error is less than the OPLL phase lock-in range of ~3:1 times loop bandwidth ω_n [11, 12], the loop

will reliably acquire lock. Due to this frequency detection mode, frequency pull-in and hold-in ranges are significantly extended (to, ideally, 50 GHz), making OPLL operation more robust.

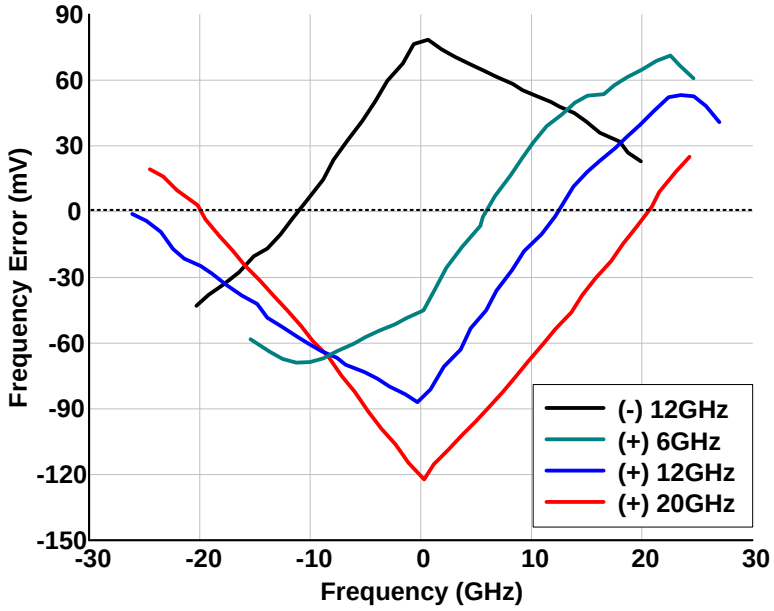


Figure 4.9: The measurement results for the frequency detection mode. The results show a 0.3 V_{pp} periodic triangular waveform with a cycle of ∼50 GHz.

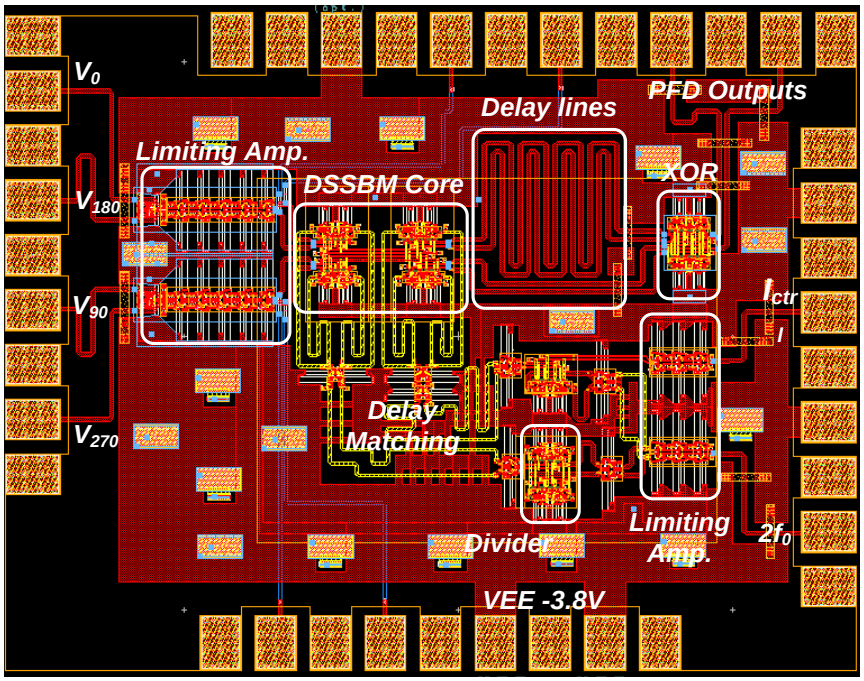


Figure 4.10: The EIC layout designed using Teledyne 500 nm HBTs with the IC size of 1.55 × 1.15 mm^2. Courtesy of Eli Bloch [1, 2].

Final layout of the EIC is shown in figure 4.10. The EIC includes several limiting amplifier chains, the two-stage digital single sideband mixer blocks, the XOR gate with the delay section for the phase frequency detector, plus frequency dividers and delay matching networks.

The total signal propagation delay of the EIC is minimized by integration to less than 100 ps, even though the EIC contains a larger number of analog and digital circuit blocks. This delay should be compared to that of an XOR-type phase detector constructed on a printed-circuit board [19]. The total delay of the PIC and EIC is ∼140 ps.

The table below gives a summary of the EIC device characteristics for the heterodyne OPLL feedback loop design.

Table 4.2: Summary of the EIC device parameters for the heterodyne OPLL design

Parameters	Value	Unit	Descriptions
K_{PD}	$0.3 \times 4/\pi$	V/rad	Linear phase detector gain
K_{FD}	$0.3/(2\pi \times 50 \times 10^9)$	V/rad/sec	Linear frequency detector gain
τ_{EIC}	100	ps	Total delay in the EIC

4.3.3 Hybrid Loop Filter: Dual-Path (Feed-Forward) Loop Filter

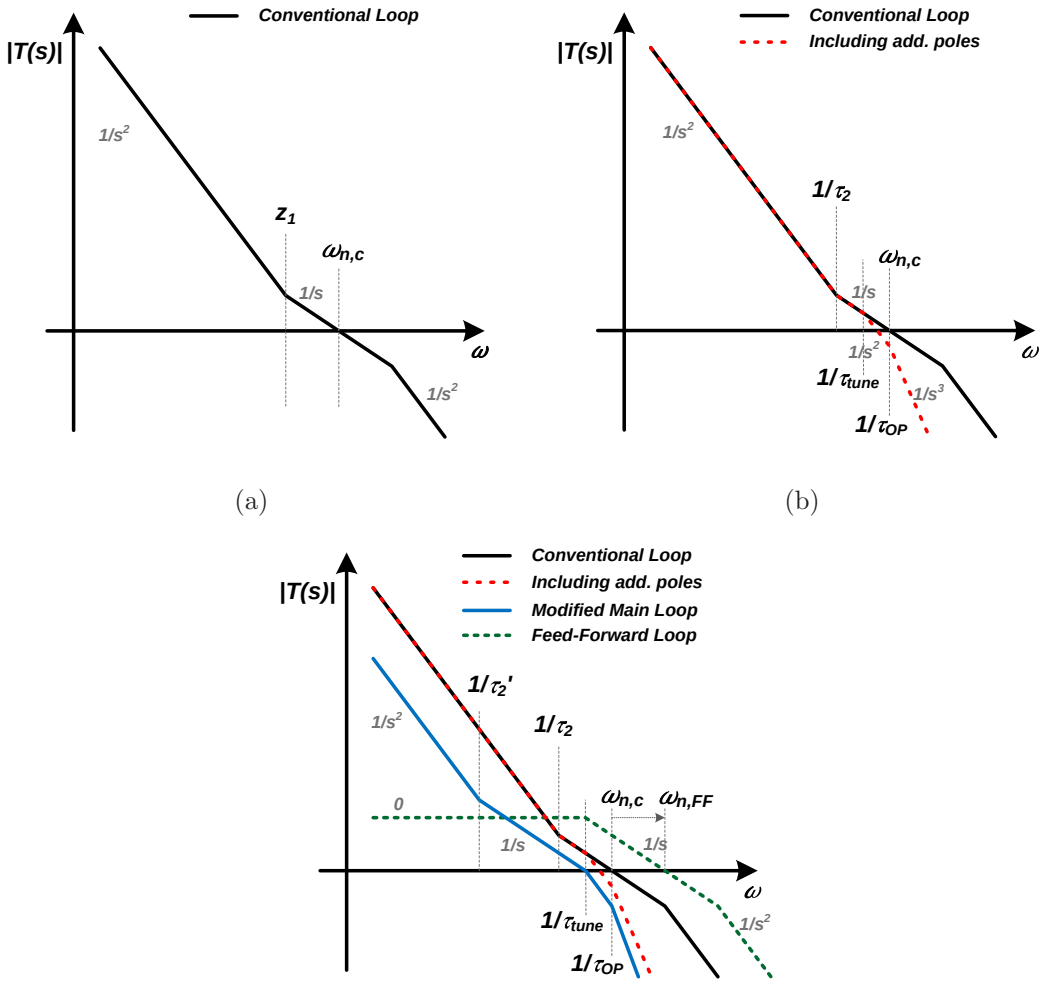


Figure 4.11: The OPLL feedback loop analysis including the feed-forward idea to extend the loop bandwidth. (a) The conventional second-order type-II loop, (b) the conventional loop with the parasitic poles which make the OPLL unstable or may decrease the loop bandwidth, and (c) the modified loop with additional novel feed-forward path to minimize the effective loop delay and extend the loop bandwidth.

Finally, the loop filter was designed for a stable locking with as wide as possible a loop bandwidth. The EIC PFD outputs are differential voltage signals terminated by 50 Ω. An active filter based second-order type-II loop is selected. This uses a commercial high-speed and high-gain op-amplifier. A conventional type-II PLL open loop transfer function including one pole and one zero is shown in figure 4.11 (a). This loop is targeted around 500 MHz loop bandwidth with 65 degree phase margin and 10 dB gain margin. However, to obtain low DC offset voltage, we have used high-speed voltage-feedback op-amplifiers, as opposed to the commercial current feedback op-amplifiers which have wider bandwidth but smaller low-frequency gain and larger DC offset voltages. These voltage feedback op-amplifiers have only ∼200 MHz unity gain bandwidth and have additional poles in their transfer function slightly above 200 MHz. Further, additional phase shift is introduced by the size of the op-amplifier package and from lead lengths on the circuit board connecting to the IC. This adds excess phase to the loop transfer function $T(s)$ (the red dotted trace in figure 4.11 (b)). Together with the additional poles in the transfer function, the τ_{OP} degrades the phase margin and the OPLL loop becomes unstable. In the figure, the basic feedback loop characteristics, shown by the black solid line, include the critical delay (equations 4.4-6), and the op-amplifier loop delay τ_{d-OP} ∼200 ps. The contributions of additional poles are included in the red trace. The OPLL open loop transfer function is then

$$T_{OPLL}(s) = K_{PD}\cdot K_{CCO}\cdot\frac{1}{s(1+\tau_{tune}s)(1+\tau_{OP}s)}\cdot F_{OPLL}(s)\cdot e^{-(\tau_d+\tau_{d-OP})s}. \quad (4.14)$$

Including all the above parasitics, the OPLL feedback loop becomes unstable and the target loop bandwidth of ∼500 MHz cannot be attained. The target loop bandwidth must be reduced or other loop design must be proposed.

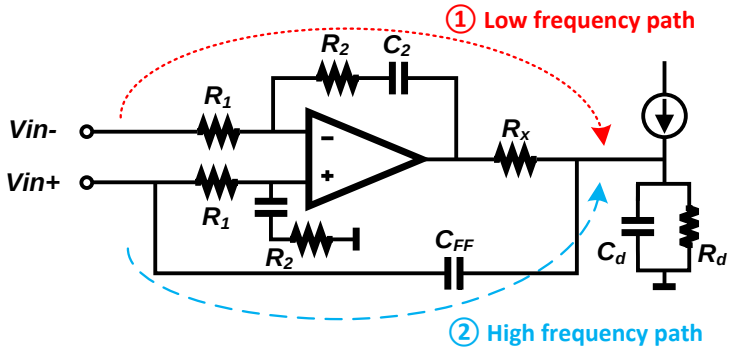


Figure 4.12: The dual-path loop filter schematic including the feed-forward path: 1) the low frequency path with an integrator, and 2) the high frequency path with the passive capacitor C_{FF}.

To address the issue of loop delay, again we use a feedforward (two-path) loop design (figure 4.11). The loop must 1) have high gain and DC and low-frequencies to suppress the laser's phase noise at low frequencies, and 2) must have low excess phase shift at high frequencies to provide high bandwidth yet high phase and gain margins. The dual-path loop filter shown in figure 4.12 satisfies both these conditions and provides a stable open loop transfer function as shown in figure 4.11 (c). The first-order conventional active loop filter has been slightly modified (blue solid-line in figure 4.11 (c)) and a short feed-forward path using a single passive capacitor C_{FF} as one zero at DC is added between $V_{in}+$ to the phase tuning section diode. The transfer function for this signal path is indicated by a green dotted line. Including all loop parameters, the main path still has $1/s^2$ integrator slope at low frequencies, but the integrator time constant and the zero time constant have been modified to τ_1' and τ_2'. Due to additional feed-forward capacitor C_{FF}, the total loop gain through the feed-forward path has constant gain at DC and low frequencies and a first order $1/s$ slope at the

laser tuning frequency of $1/(1+\tau_{tune}s)$ until 0 dB gain (gain crossing point). Since R_1 and R_x are relatively large, this path can be analyzed independently from the input voltage at (+) input node to a current conversion into the phase tuning section diode modeled as a parallel connection of R_d and C_d via the series feed-forward capacitor C_{FF}. Measured the R_d is relatively small at ∼10 Ω. From this, the necessary value of C_d capacitor determined to be ∼160 pF. Therefore, the expression for the gain of the feedforward path can be simplified (see the Appendix) to

$$T_{FF}(s) = K_{PD}{\cdot}K_{CCO}{\cdot}\frac{s{\cdot}0.5{\cdot}C_{FF}}{s(1+\tau_{tune}s+\tau_{FF}s)}{\cdot}e^{-\tau_{d-eff}s}, \tag{4.15}$$

where the time constant of the feed-forward pole is τ_{FF} by $R_d{\cdot}C_{FF}$ and where the effective loop delay through the feed-forward path is $\tau_{d-eff} \approx 200$ ps. The transmission-line delay through the PIC and EIC is less than 140 ps and the interconnection delay with the feed-forward capacitor C_{FF} is less than 60 ps. We will later neglect τ_{FF} because $\tau_{tune} \gg \tau_{FF}$.

The path length in the feedforward path is almost negligible. The feed-forward path gain is determined by the feed-forward capacitor C_{FF} as $0.5{\cdot}K_{PD}{\cdot}K_{CCO}{\cdot}C_{FF}$. This path keeps a constant gain up to the 100 MHz laser pole frequency. Beyond the laser pole frequency, the open loop transfer function has a first order slope $1/s$. Therefore, the loop bandwidth is automatically determined by the feed-forward loop gain multiplied by the laser pole frequency, i.e. 20 dB feed-forward gain corresponds to 1 GHz loop bandwidth. The phase margin is determined by the total effective loop delay τ_{d-eff}, i.e. the first order slope $1/s$ and 200 ps at 1 GHz correspond to 72 degree phase variance. In summary, the OPLL's loop bandwidth is determined by the DC gain of the feed-forward path $0.5{\cdot}K_{PD}{\cdot}K_{CCO}{\cdot}C_{FF}$, and the

phase margin PM is determined by the total effective loop delay τ_{d-eff} through the feed-forward path and the loop bandwidth ω_n as

$$PM = \pi/4 - \omega_n \times \tau_{d-eff}. \tag{4.16}$$

Due to this feed-forward loop filter, the loop delay has greatly reduced to less than 200 ps. The total loop delay is only limited by the PIC and EIC, with no contributions from the loop filter. This allows significantly increased loop bandwidth, being the difference $\omega_{n,c} \rightarrow \omega_{n,FF}$ (figure 4.11 (c)).

The wire-bond connection to the capacitor C_{FF} introduces 0.5 to 1 nH inductance. This introduces second-order poles above 4 GHz. The component values of C_{FF}, L_{wire}, together with the 50 Ω termination resistors, were chosen to damp this resonance. As shown in (figure 4.11 (c)), the feed-forward path (green dotted line) is summed with the main-path (blue-line) which has been slightly modified τ_1' and τ_2' to avoid a 180 degree out-of phase condition between these two signal paths at the gain crossing point, as this would otherwise produce a notch in the summed transfer function. Finally, wideband and yet stable open loop transfer $T_{OPLL}(s)$ is attained

$$\begin{aligned} T_{OPLL}(s) &= K_{PD} \cdot K_{CCO} \cdot \frac{1}{1+\tau_{tune}s} \\ &\quad \cdot \left(\frac{1+\tau_2' s}{\tau_1' s^2 (1+\tau_{OP}s) R_x} e^{-\tau_{d-OP}s} + \frac{C_{FF}}{2} \right) \cdot e^{-\tau_{d-eff}s}. \end{aligned} \tag{4.17}$$

This feedback loop gain $T_{OPLL}(s)$ has been simulated in MATLAB. A Bode plot of gain and phase is shown in figure 4.13. The modified dual-path loop gain $T_{OPLL}(s)$ shows a much wider loop bandwidth, more than ∼400 MHz, with a phase margin of more than 60 degrees and a gain margin of more than 7.5 dB. As seen in

figure 4.13, the modified main-path has a high gain of $1/s^2$ and this gain curve smoothly transitions to the feed-forward path at around 50 MHz without the a notch at the crossover frequency. As noted above, the proposed loop has high gain at DC and at low frequencies through the main integrator path, and has a greatly extended loop bandwidth without additional significant delay through the short passive feedforward path. As a result, the total loop delay can be approximated as the effective loop delay τ_{d-eff} of less than 200 ps (PIC: 40 ps, EIC: 100 ps, others: less than 60 ps) only for the high frequency.

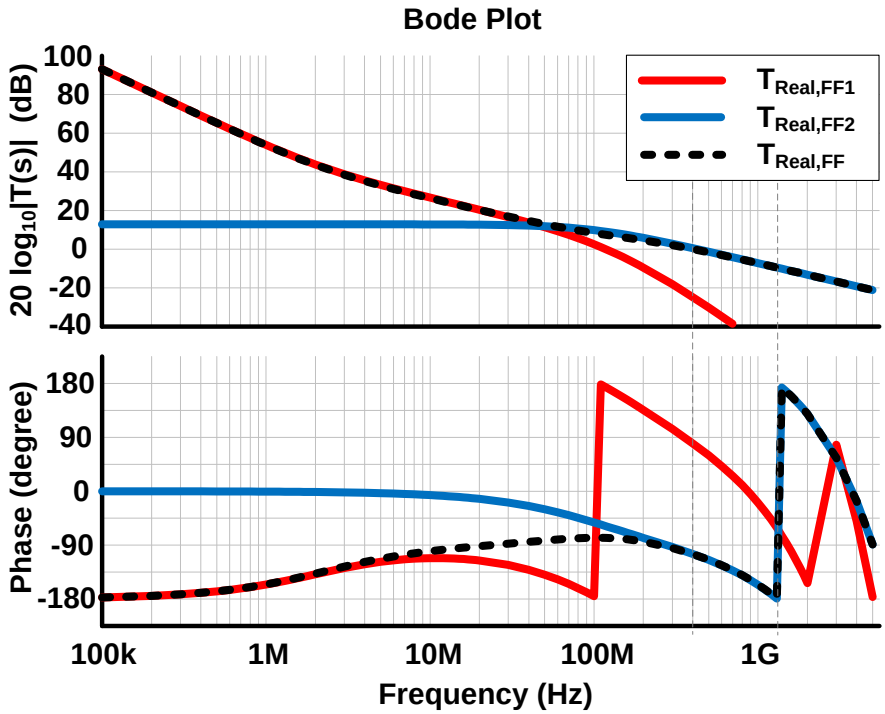


Figure 4.13: The OPLL bode-plot including the feed-forward loop: The open loop bandwidth ω_n ~400 MHz, the phase margin of more than 60 degree, and the gain margin of more than 7 dB.

Parameters of the loop filter are summarized in the table:

Table 4.3: Summary of the loop filter parameters for the heterodyne OPLL design

Parameters	Value	Unit	Descriptions
τ_{d-eff}	200	ps	Effective loop delay
τ_1'	2100 Ω $\times$ 470 pF	sec	Modified pole time constant
τ_2'	160 Ω $\times$ 470 pF	sec	Modified zero time constant
τ_{OP}	$1/2\pi/200$ MHz	sec	Op-amplifier second pole frequency
τ_{dOP}	150	ps	Op-amplifier delay
τ_{other}	$\sim$50	ps	Interconnection delay (T.L. and wire)
C_{FF}	1.0	pF	Feed-forward capacitor C_{FF}
R_x	500	Ω	Voltage to current conversion (V/A)

4.4 OPLL Implementation

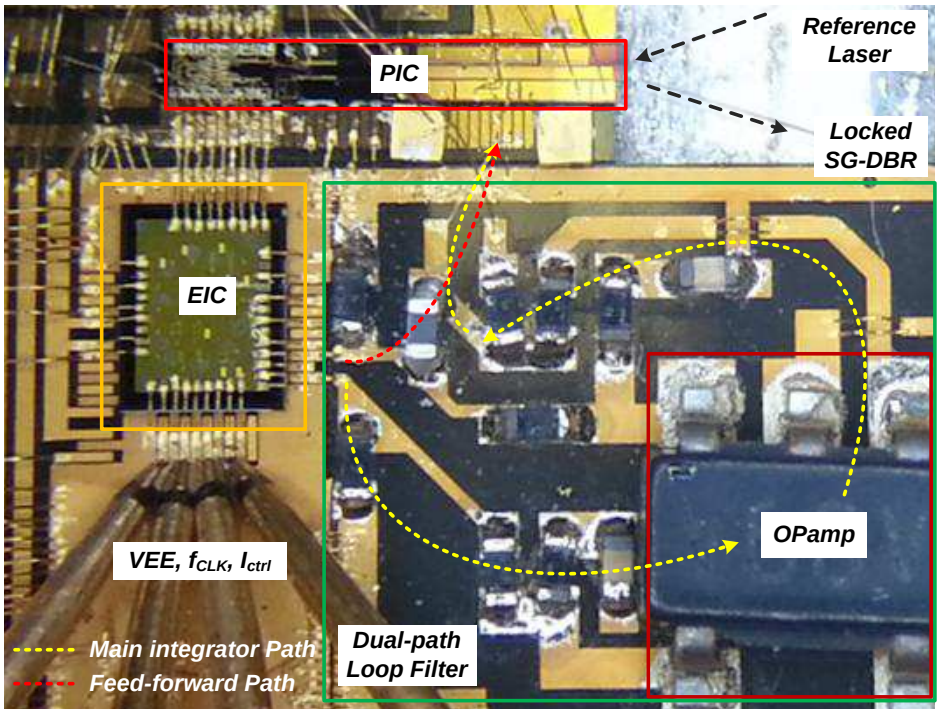


Figure 4.14: The photograph of the heterodyne OPLL: The PIC, EIC and loop filter are highly integrated in a single carrier board within $10 \times 8\ mm^2$.

Based on the loop analysis, our heterodyne OPLL has been realized on a single AlN ($\epsilon_r = 9.0$) carrier board as shown in figure 4.14. All components are integrated within the a compact core of $10 \times 8\ mm^2$. Masks for all AlN carrier boards were fabricated in UCSB's facilities by M. Lu, and all devices and discrete components are mounted using solder paste and conducting silver epoxy. Wirebonds are used for electrical connections between devices to devices and boards to boards, and the lengths of the wires are as short as possible to minimize the length of lines. Many wire-bonds are made between the IC and carrier ground planes.

The PIC and EIC were designed and tested on-wafer and after mounting on the

board. The hybrid loop filter was designed using the commercial TI's LMH6609 voltage feedback op-amplifier which a high DC gain of 70 dB, unity gain bandwidth of more than 200 MHz, a low DC-offset of less than 1 mV. The supply voltage supplies are ± 3.3 and ± 6 V. Loop poles and zeros are realized using 0201 inch discrete R and C surface-mount components.

As shown in figure 4.14, the distance between the PIC and EIC was kept as short as possible to minimize the interconnection loop delay and to maintain the high frequency interface of more than 50 GHz. In addition, the length of the feed-forward path (red arrow dot in figure 4.14) was kept as short as possible to again minimize the loop delay and wire-bond inductance, which is critical to the OPLL stability. Additionally, vertical DC power supply bypass capacitors are connected adjacent to DC paths.

We have carefully considered many implementation issues and successfully achieved stable heterodyne OPLLs, which show widely synthesizing frequency offsets of up to ± 20 GHz. Various experimental results will be shown in the following sections.

4.5 OPLL Experiments and Measurement Results

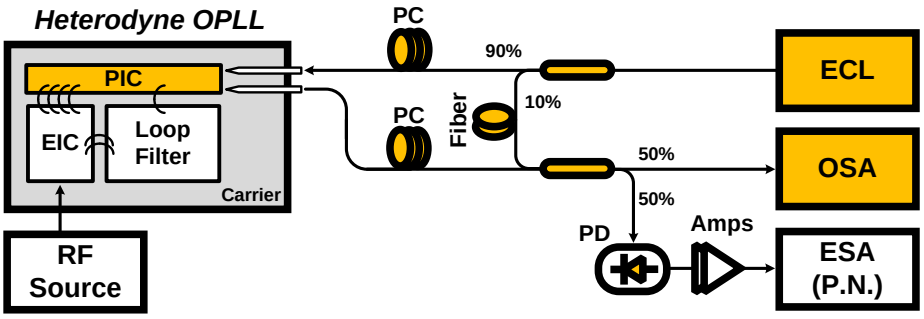


Figure 4.15: A test setup for the heterodyne OPLL for the performance of the locked SG-DBR laser (frequency synthesis and phase noise measurements). EDFA: Erbium doped fiber amplifier, PC: polarization controller, OSA: optical spectrum analyzer, and ESA: electrical spectrum analyzer.

To verify the heterodyne OPLL performance, frequency offset locking at ±6 GHz was performed using the test setup of figure 4.15. An Agilent external-cavity laser, with a wavelength at 1550 nm and ∼100 kHz linewidth, is used as the reference laser. This reference light signal is coupled into the PIC through a 90 % - 10 % optical divider and a polarization controller (PC). The OPLL's locked SG-DBR laser output is coupled out, the two laser signals are monitored through an optical spectrum analyzer (OSA), and the lasers are combined together and mixed on a 40 GHz photodiode. This allows the relative phase noise between the two lasers, and their frequency offset, to be measured by an electrical spectrum analyzer. An RF signal source at twice the clock frequency ($2f_0$) is applied as frequency offset signal to D-SSBM within the EIC, and the sign (+ or -) of the frequency offset is controlled by the EIC's I_{ctrl} port.

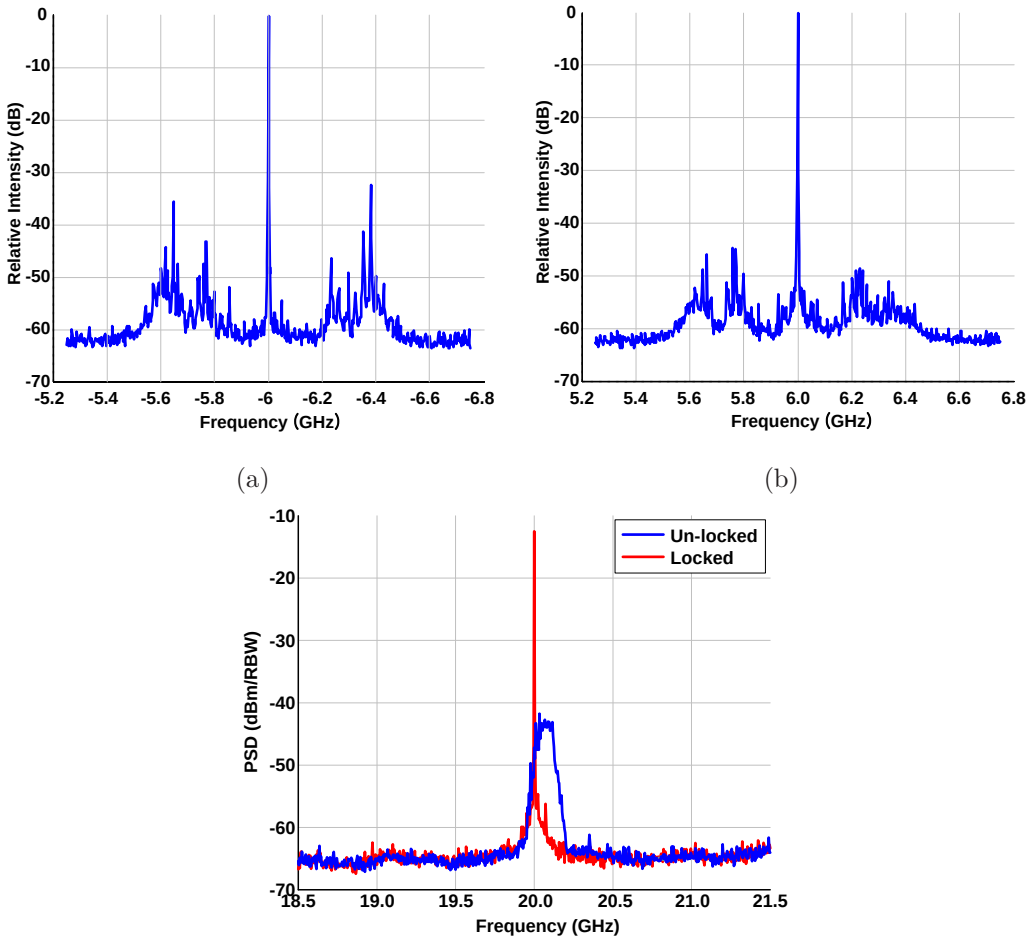


Figure 4.16: The beating spectra between the locked SG-DBR laser and the reference laser. (a) An offset frequency lock at (+) 6 GHz, (b) offset frequency lock at (-) 6 GHz, and (c) offset frequency offset lock at 20 GHz and unlock (free-running) near 20 GHz frequency offset.

In the first offset-locking experiment, the heterodyne OPLL showed stable frequency locking at ±6 GHz offset frequencies from the reference laser frequency. The beat-note spectrum between the locked SG-DBR laser and the reference laser is shown in figure 4.16 (a) and (b). Since the difference frequency between two lasers is ±6 GHz, the main peak tone of the beat note is at 6 GHz. The side

peaks at 350 MHz offset correspond to OPLL phase noise peaking at the OPLL loop bandwidth.

The above results were obtained using the first PICs fabricated. Subsequent development efforts by M. Liu improving the PIC performance. Using these improved PICs, frequency synthesis with the heterodyne OPLL was extended up to 20 GHz tuning range (figure 4.16 (c)). The figure shows measurement of the spectra of both the locked SG-DBR laser at +20 GHz frequency offset (red) and the un-locked SG-DBR laser, again near 20 GHz offset (blue). With the feedback loop, the locked SG-DBR laser in the heterodyne OPLL has the desired frequency offset, has a narrow linewidth, and tracks the reference laser carrier with the 20 GHz frequency offset set by the RF frequency signal source.

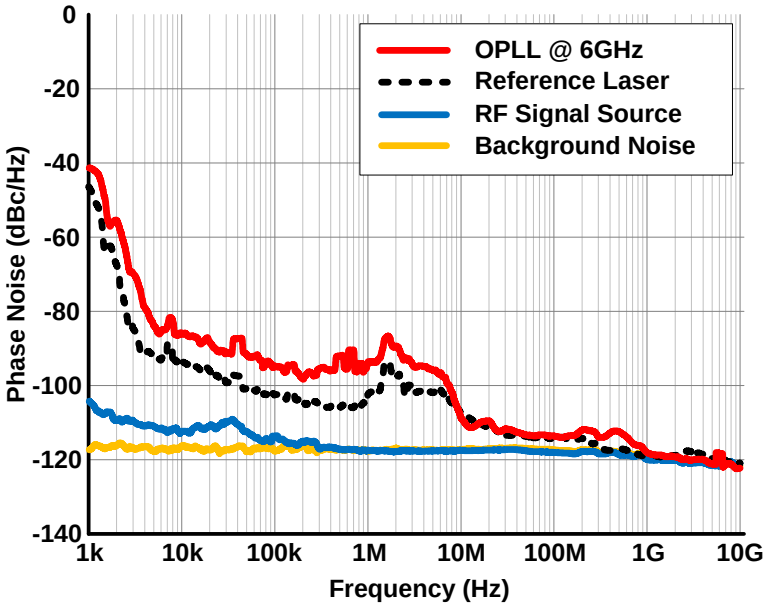


Figure 4.17: The phase noise measurement results for the beating spectrum in figure 4.16 (a), and the compared phase noise results of the reference laser, RF signal source, and background noise.

To further examine the OPLL performance, the beat signal between the two lasers (figure 4.16 (a)) is directly connected to a phase noise analyzer and the single-sideband (SSB) phase noise of the locked SG-DBR laser is measured at offsets from 1 kHz to 10 GHz (figure 4.17). The OPLL phase noise is then compared with the phase noise of the reference laser (homodyne-beat with a 100 MHz AOM modulator), the phase noise of the RF signal source, and the background noise, the latter including thermal and PD shot noise and the noise figure and gain of amplifiers. The measured phase noise of the locked laser is only slightly larger than that of the reference laser source. The heterodyne OPLL exhibits a phase noise of -80 dBc/Hz and -110 dBc/Hz at 50 kHz and 10 MHz offsets, respectively. Phase noise variances extracted by the phase noise show $\sim$0.03 rad^2 in a integration from 1 kHz to 10 GHz offset from carrier.

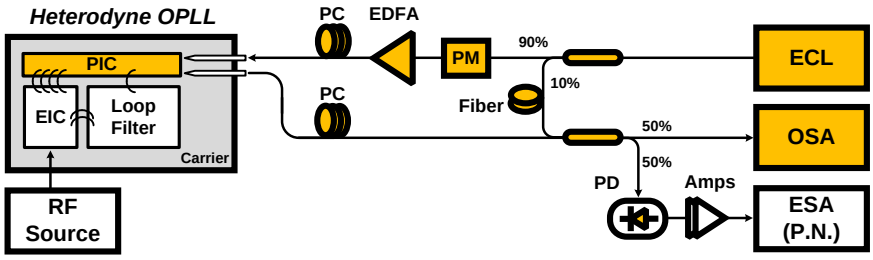


Figure 4.18: A test setup for the heterodyne OPLL for the closed loop frequency response measurements (figure 4.19 and figure 4.20 (b)).

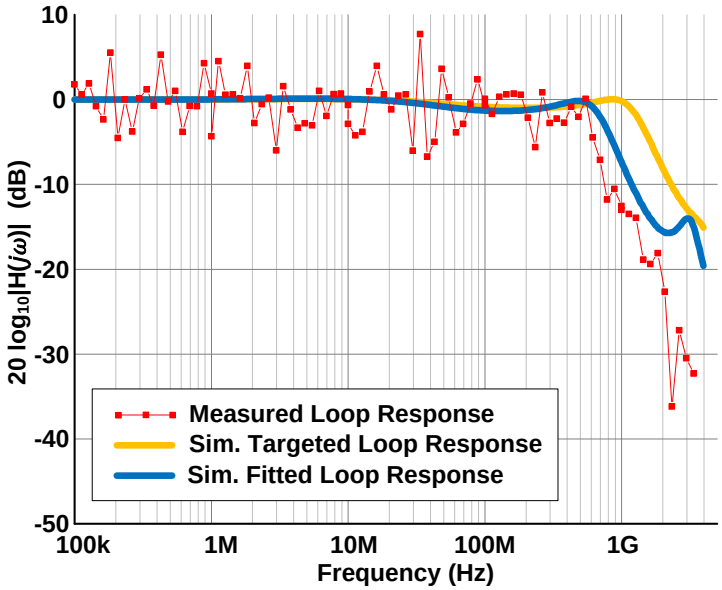
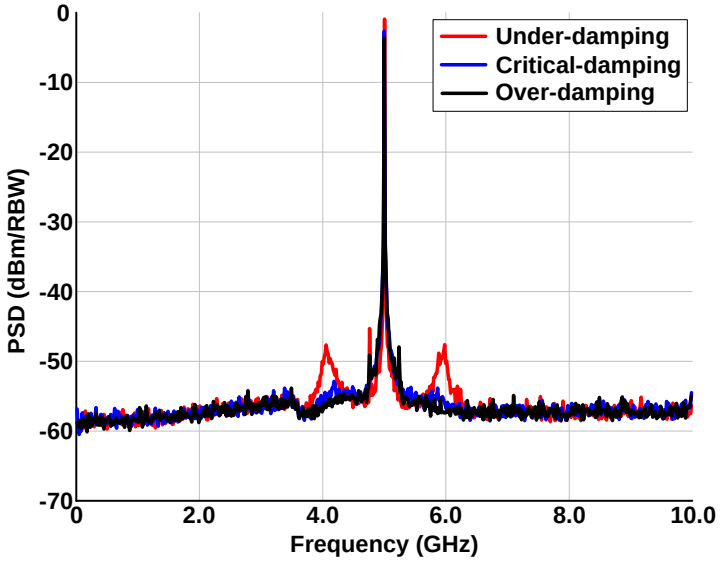
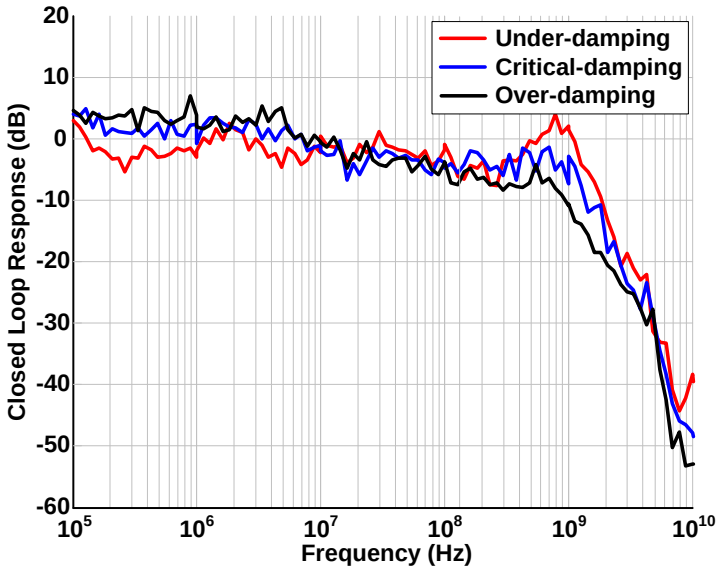


Figure 4.19: The closed loop frequency response for the heterodyne OPLL (red line-dot), and comparison results of simulated closed loop frequency response for the open-loop response T_{OPLL} (yellow) and fitted frequency response for the measured result (blue).

The closed-loop frequency response $H(s) = T(s)/(1 + T(s))$ of the heterodyne OPLL was measured using the test setup shown in figure 4.18. With the heterodyne OPLL is operating, reference laser is phase modulated. The resulting frequency response measurement is shown in figure 4.19 (red dotted line). The measured frequency response is compared with simulation (yellow line) using the OPLL's open loop response T_{OPLL}. A response (blue line) fitted to the measurement is used to estimate the OPLL open loop bandwidth. The closed loop bandwidth of ∼550 MHz is measured, and the open loop frequency response of ∼270 MHz is extracted from the fitted closed response. The target open loop bandwidth in the previous simulation is set at around 400 MHz, and the realized OPLL has slightly lower bandwidth than designed.



(a)



(b)

Figure 4.20: The measured beating spectra (a) and the closed loop frequency responses (b) at the frequency offset of 5 GHz. The values of the feed-forward capacitor are varied with 0.5, 1.0 and 1.5 pF, and the different loop responses are measured.

Additionally, using the previous test setup for the frequency response, we

examined adjusting the loop damping. As discussed previously in the loop filter and OPLL feedback loop analysis, the loop bandwidth is determined by the feed-forward gain, $K_{PD} \times K_{CCO} \times 0.5 C_{FF}$ with the laser pole at τ_{tune}. This means that the gain is easily controlled by the value of the feed-forward capacitor C_{FF} and that the OPLL damping factor is also easily adjusted. A capacitance of $C_{FF} =$ 1.0 pF was used in the initial OPLL design. This was then varied from 0.5 pF to 1.5 pF. The closed-loop frequency response was measured for these cases, giving different loop bandwidths and loop damping conditions. The results are shown in figure 4.20. The OPLL feedback loop shows an over-damping ($\varsigma > 0.707$) with $C_{FF} = 0.5$ pF, a critical damping with $C_{FF} = 1.0$ pF, and an under-damping ($\varsigma < 0.707$) with $C_{FF} = 1.5$ pF. In figure 4.20 (a), the under-damped result shows higher noise-enhancement peaks at around 500 MHz offset from the 5 GHz carrier. In contrast, the over-damped result shows lower noise-enhancement at around 300 MHz offset. The closed loop bandwidth results in figure 4.20 (b) represent the same performance results as figure 4.20 (a).

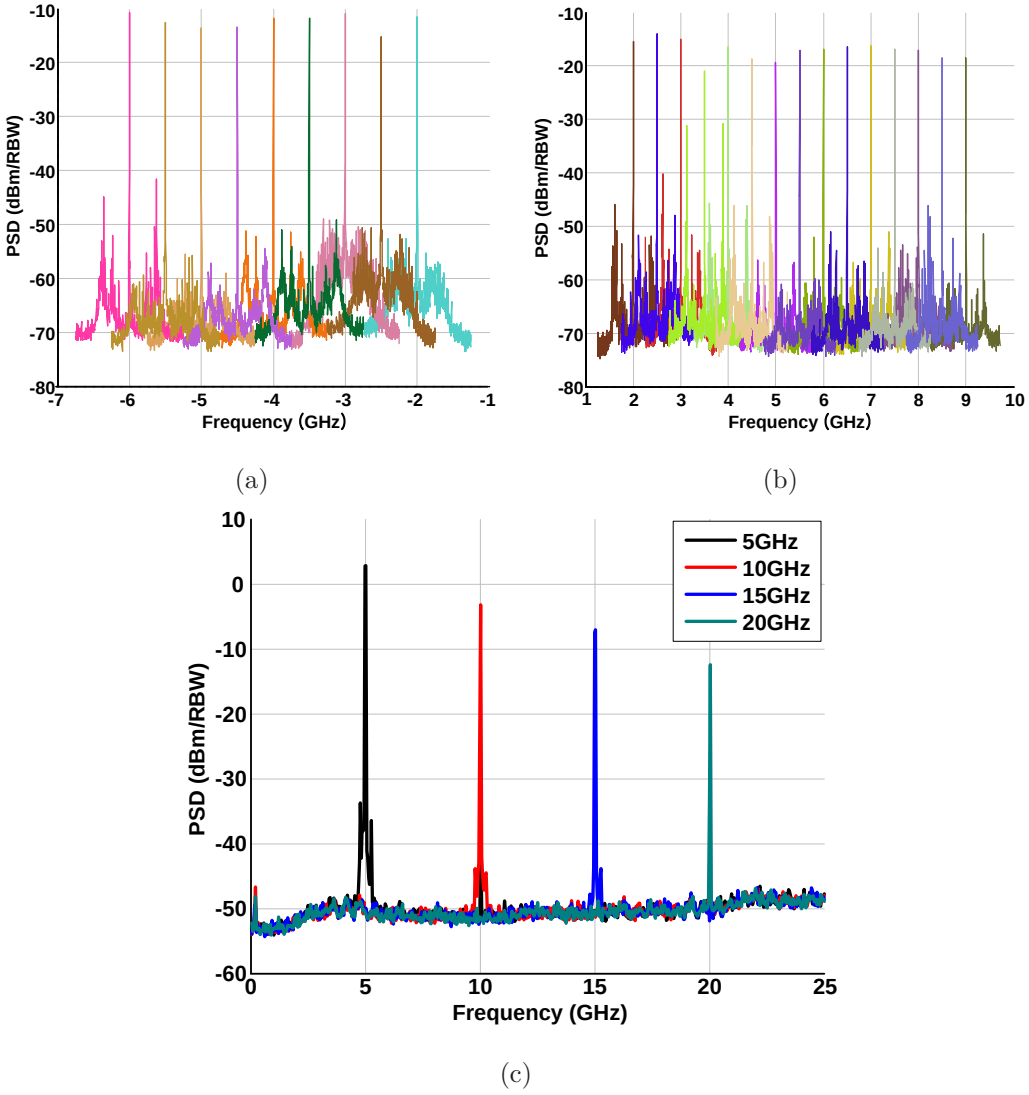


Figure 4.21: The frequency synthesis experimental results. (a) The negative frequency sweeps from -6 to -2 GHz with $I_{ctrl} = (-)1$ in the EIC, (b) The positive frequency sweeps from 2 to 9 GHz with $I_{ctrl} = (+)1$ in the EIC, and (c) The wide frequency sweep range up to 20 GHz using the improved OPLL.

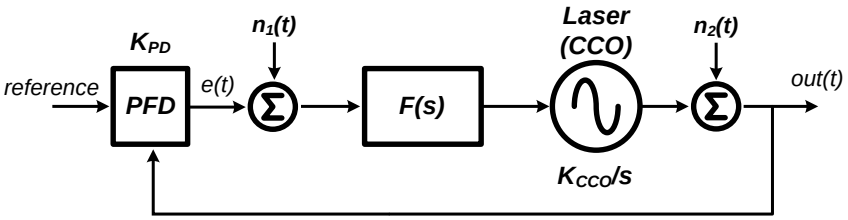
Finally, broadband frequency synthesis experiments have been performed as shown in figure 4.21. Simply, the frequency offset is determined the RF signal source of $2f_0$ and the direction is selected by the I_{ctrl} bits (-1 or 1) in the EIC.

The initial heterodyne OPLL exhibits frequency offset synthesis ranges of -6 GHz to -2 GHz (figure 4.21 (a)) and +2 GHz to +9 GHz (figure 4.21 (b)). Using the improved heterodyne OPLL, much wider frequency synthesis ranges of up to 20 GHz (figure 4.21 (c)) are demonstrated.

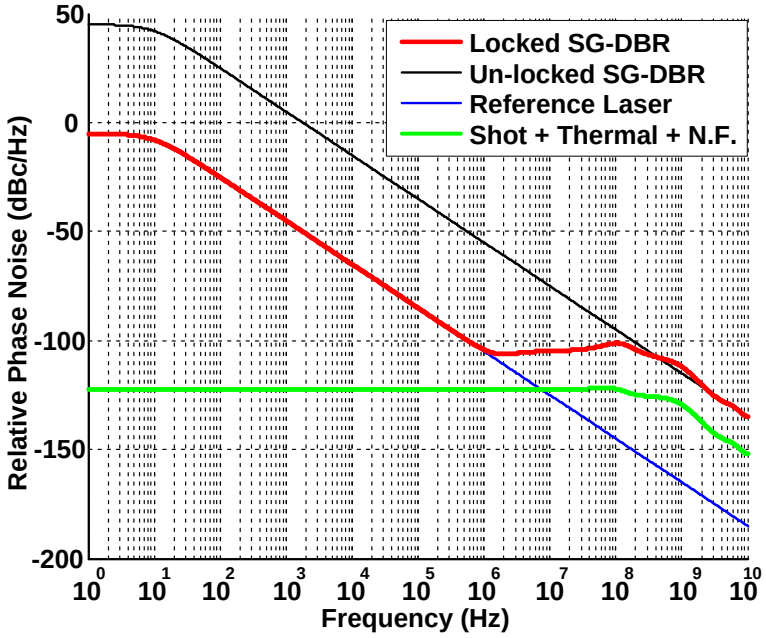
4.6 Conclusion

A new highly integrated heterodyne OPLL was demonstrated using a photonic IC, an electrical IC, and a feed forward loop filter. The design challenges for stable and wide bandwidth OPLLs were discussed, and a full architecture for the heterodyne OPLL was introduced. The loop characteristics for each block and total loop responses were analyzed including practical characteristics such as the loop delay and the limited operational bandwidth from the electrical circuits. Based on the loop architecture and analysis, the heterodyne OPLL was built on a single carrier board with the compact size of $10 \times 8\ mm^2$. In addition, by using a feed forward loop filter, a total loop delay of approximately 200 ps at high frequencies is obtained. The OPLL exhibits a unity gain bandwidth of 270 MHz and the 3-dB closed loop bandwidth of 550 MHz. Moreover, the locked SG-DBR laser at 6 GHz offset frequency shows phase noise of -110 dBc/Hz at 10 MHz offset and -80 dBc/Hz above 10 kHz, respectively.

4.7 Additional Analysis-I: Phase Noise Analysis



(a)



(b)

Figure 4.22: Laser phase noise analysis. Optical PLL system diagram including the noise sources of input reference, $n_1(t)$ of shot and white noise including an amplifier noise figure, and $n_2(t)$ of laser (oscillator) noise (a), and phase noise (dBc/Hz) vs. frequency from 1 Hz to 10 GHz.

Phase noise of the OPLL was analyzed using our dual-path feedback loop system of $T_{OPLL}(s)$ in equation 4.17. The typical phase lock loop system diagram is modeled as figure 4.22 (a) and three noise sources are defined in this loop [36,37].

The first noise source of $n_1(t)$ includes photodetector shot noise $S_s(f) = 2qI_p$ and thermal noise $S_T(f) = 4K_BT/R_L$ including amplifiers' noise figure NF in the OPLL system and they are assumed as -149 dBc/Hz, -153 dBc/Hz, and ∼22 dB at the photodetector current output conditions of ∼1 mA [38, 39]. The second noise source of $n_2(t)$ is from the free-running SG-DBR laser and it is assumed as 1 MHz linewidth laser and its $1/f^2$ noise slope extrapolated to 1 Hz. The third noise source is the input reference laser which is modeled using a Lorentzian linewidth of $1/\pi \cdot \Delta v/(\Delta v^2 + f^2)$ and total phase error variation are set to have 10 Hz with ∼0.01 rad^2 which is derived by integrations of the spectral density. The output of the locked SG-DBR laser in the feedback loop has been derived as

$$\begin{aligned} OUT(s) &= Ref(s) \cdot \frac{K_{PD} \cdot F(s) \cdot 1/s \cdot K_{CCO}}{1 + K_{PD} \cdot F(s) \cdot 1/s \cdot K_{CCO}} \\ &+ N_1(s) \cdot \frac{F(s) \cdot 1/s \cdot K_{CCO}}{1 + K_{PD} \cdot F(s) \cdot 1/s \cdot K_{CCO}} \\ &+ N_2(s) \cdot \frac{1}{1 + K_{PD} \cdot F(s) \cdot 1/s \cdot K_{CCO}}, \end{aligned} \tag{4.18}$$

As shown in figure 4.22 (b), the SG-DBR laser's phase noise is suppressed through the feedback loop $T_{OPLL}(s)$ and cloned to the reference laser until ∼10 Hz. The first order loop by the main path and the feed-forward loop are smoothly mixed and transited. The total closed loop bandwidth of ∼1 GHz are noticed. The noise limits of -131.7 dBc/Hz are derived from the shot, thermal noise including noise in the feedback loop system. Total phase error variation of ∼0.011 rad^2 (as similar as the reference laser) in the locked SG-DBR laser is obtained.

In summary, the integrated SG-DBR laser source, which, without phase-locking is not suitable for coherent multi-order constellations and very sensitive sensors, becomes a very narrow coherent laser source when phase-locked by a

wideband OPLL [40]. Using this system, there will be many applications such as high spectral efficiency coherent data transmission and reception, narrow line-width mm-wave and sub-THz signal generation, and in high resolution LIDAR imaging and sensing systems.

4.8 Additional Analysis-II: Dual-path (Feed-forward) Loop Filter Analysis

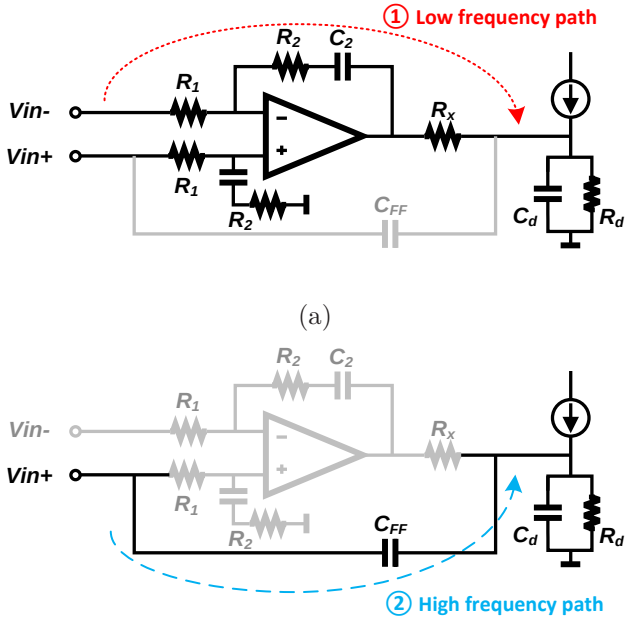


Figure 4.23: Dual-path (feed-forward) loop filter analysis. The circuit schematic for low frequency path including an integrator and pole and zero (a), and the circuit schematic for high frequency path through the feed-forward capacitor C_{FF} as a zero (b).

In the OPLL designs, we have targeted as wide a loop bandwidth ω_n as feasible. The loop delay a the critical parameter limiting this bandwidth. Given the loop delay by the PIC and EIC, a loop filter design using a high gain active loop filter with commercial op-amplifiers has been challenging because of the op-amplifiers' long delay and their limited bandwidth. As mentioned, in this reason, we could not target a loop bandwidth of even 100 MHz. Therefore, we adopted the dual-path concept in the electrical PLLs. This technique had earlier been introduced to decreasing the size of capacitors in ICs [11, 12]. We have used this concept to separate a low-frequency path and a high-frequency path. The low frequency path including an integrator through the op-amplifier has high gain but long loop delay. The high frequency path including only a passive capacitor has a zero with a coupling factor but short delay. Then, the two paths are smoothly combined by controlling the loop parameters. The main path figure 4.23 (a) has pole τ_1' and zero τ_2' frequencies of

$$\begin{aligned} \tau_1' &= R_1 C_2 \\ \tau_2' &= R_2 C_2. \end{aligned} \tag{4.19}$$

In our feedback loop design, the values of τ_1' and τ_2' are not designed for the optimum loop characteristics for the second order type-II feedback loop. The values are set to avoid the 180 degree output-of-phase (which will produce a gain notch) at the gain crossing point, when the main path gain is the same as the feed-forward path. Then, the main path loop filter transfer function $F_{main}(s)$ is set as

$$F_{main}(s) = \frac{I_{out}}{V_{in-}} = \frac{\tau_2' s + 1}{\tau_1' s} \cdot \frac{1}{R_x}, \tag{4.20}$$

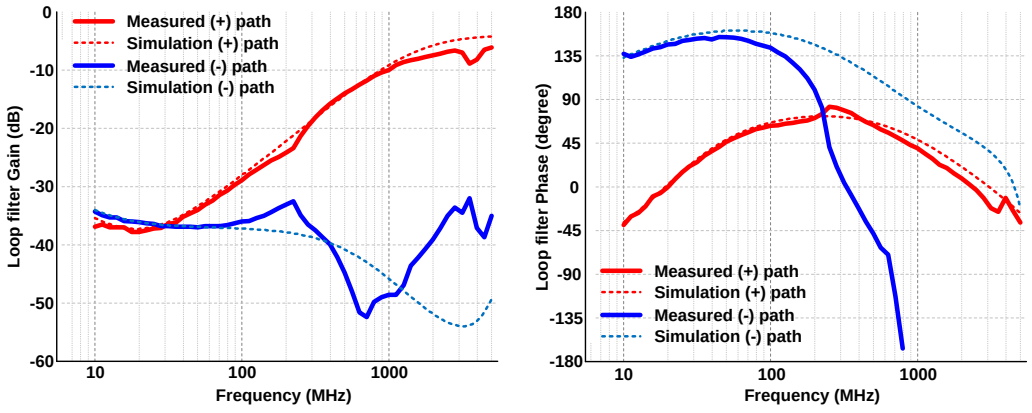
and the feed-forward path loop filter transfer function $F_{FF}(s)$ is

$$F_{FF}(s) = \frac{I_{out}}{V_{in+}} = \frac{sC_{FF}(1 + sC_dR_d)}{1 + s(C_dR_d + C_{FF}R_d)}. \tag{4.21}$$

The feed-forward loop filter path has two zero at 0 and C_dR_d and one pole at C_dR_d+$C_{FF}R_d$. Because of $C_dR_d \gg C_{FF}R_d$, the feed-forward path loop is assumed as

$$F_{FF}(s) \approx sC_{FF}. \tag{4.22}$$

The feed-forward loop filter has only one zero with the feed-forward coupling factor value, and the total feed-forward loop has a constant gain including laser pole $1/s$, laser gain K_{CCO}, and phase detector gain K_{PD}. As mentioned in the main chapter, I have used the first order slope using the laser slow tuning response at the phase tuning section diode τ_{tune} at around 100 MHz, and the phase margin and loop bandwidth is properly determined by the total effective loop delay τ_{d-eff} through the feed-forward path.



(a) (b)

Figure 4.24: Dual-path (feed-forward) loop filter simulation and measurement results from 10 MHz to 5 GHz. Gain curves (a) and phase curves (b) from V_{in-} port of the main path and V_{in+} port of the feed-forward path.

Loop filter characteristics have been simulated and measured from 10 MHz to 5 GHz for each loop filter port of the V_{in+} and V_{in-} as shown in figure 4.23. The V_{in+} path include the both main path and feed-forward path, but the feed-forward path is more dominant at the high frequency. The V_{in-} path includes only the main path. The simulation setup for the op-amplifier does not consider the op-amplifier's additional second and third poles and delay. The measurement and simulation results for the feed-forward path are nearly matched. However, the main path of (-) path represents additional poles and delays.

In summary, because of to the feed-forward path, the loop bandwidth performance of the OPLL is not limited by the loop filter and only limited by the PIC and EIC delay. As a result, a wide loop bandwidth of ∼550 MHz and total effective loop delay >200 ps are achieved in the heterodyne OPLLs, and thus, we have demonstrated stably operating OPLLs and state of the art ±20 GHz frequency synthesis.

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Chapter 5

Flexible Compact WDM Receiver

This chapter describes my third research topic at UCSB, for which I collaborated with M. Piels and E. Bloch. The results of this work have been reported in conference and journal publications [1–3]; this chapter includes recent additional, unpublished experimental results. We have proposed a new wavelength division multiplexing (WDM) receiver concept which uses cascaded optical and electrical signal frequency down-conversion. Initial design began with WDM receiver ICs and their sub-IC blocks using Teledyne's 500 nm InP HBTs [4], and later, the sub-block ICs were tested and system-level WDM receiver experiments were successfully demonstrated. In this work, I have only considered first system demonstrations using our high speed ICs. I have not considered other key system parameters including power consumption, noise, chip size, dynamic range, and bit rate.

In this chapter, I will introduce our proposed WDM receiver concept and compare it with a conventional WDM receiver architecture. The WDM receiver ICs

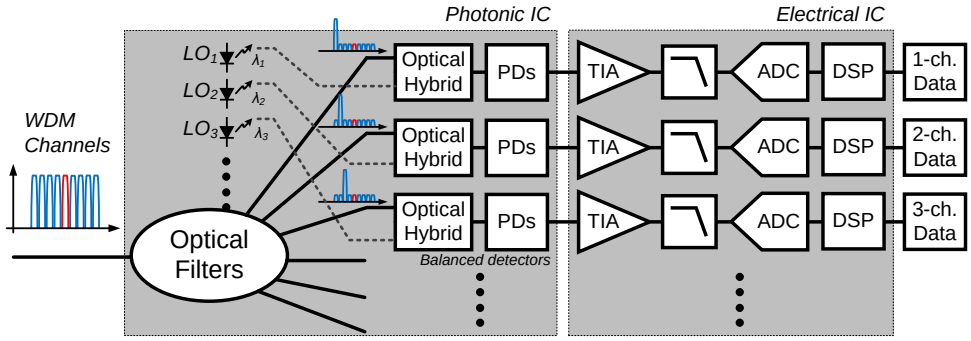
using high speed IC sub-blocks (discussed in chapter 2) will be examined, and simulation and measurement results will be described. I will then show three system experiments to demonstrate the proposed WDM receiver. The first experiment tests an image rejection within the WDM receiver. The second measures adjacent channel interference and its suppression. From this we to find a maximum spectral efficiency. The third experiment tests a 6-channel data reception using a core analog single-sideband mixer (SSBM) IC. In the conclusion chapter, I will briefly discuss several alternative (advanced) receiver architectures and IC designs using silicon-based processes for future research.

5.1 Motivation and Background

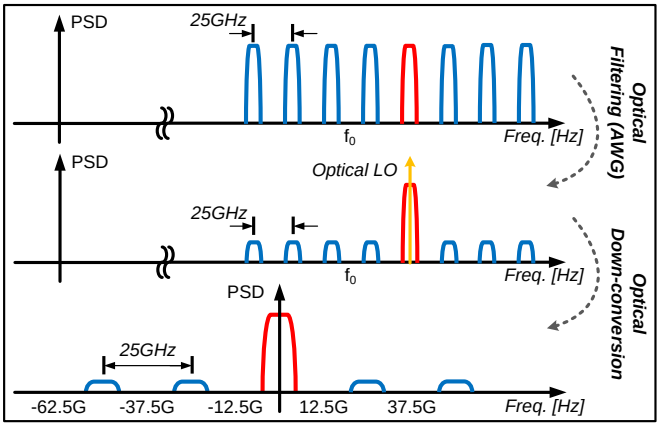
High spectral efficiency and high channel capacity wavelength division multiplexing (WDM) systems such as Tb/s super-channels [5–10] are needed to meet future demands for high data rate transmission. For these systems, simple hardware and low DC power consumption are both desirable. Moreover, WDM systems with elastic and flexible channel allocations have been proposed to aid in adapting to variations in network traffic and conditions [11, 12]. A conventional coherent WDM receiver consists of a fixed- or flexible-grid optical de-multiplexing filter and an array of coherent receivers, as is shown in figure 5.1 (a) [5–10]. The photonic IC (PIC) is complex, containing the optical filter and an array of coherent receivers. Each coherent receiver contains a local oscillator (LO) laser, a 90 degree optical hybrid, and a pair of balanced photodiodes (PDs). Each pair of PICs and electronics requires its own high-speed electrical interface [5, 8]. The

large number of components and interfaces can increase manufacturing costs and decrease manufacturing yield. The number of PIC components can be reduced by high-speed and high-resolution analog-digital-converters (ADCs) and digital-signal-processors (DSPs), but this imposes a large power penalty and comes at the cost of reduced optical reach [8].

As shown in recovering flows in figure 5.1 (b), the optical filter (i.e. arrayed waveguide grating (AWG)) demultiplexes a desired channel from received multi-channels, the balanced detector down-converts the desired channel (still in an optical domain) to an electrical domain, and the receiver chain recovers original data through the TIA, LPF, ADC, and DSP.



(a)



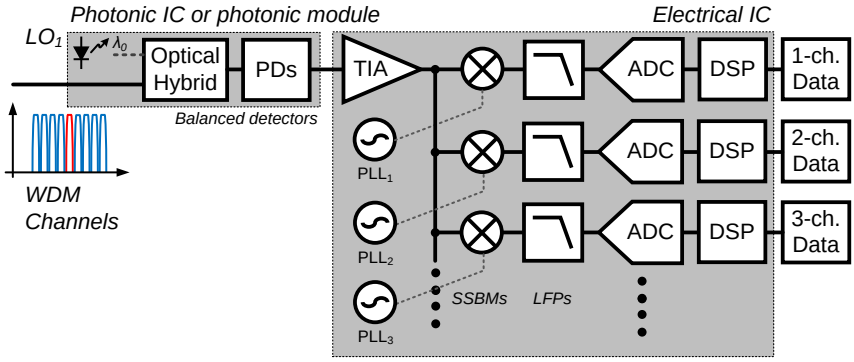
(b)

Figure 5.1: The conventional WDM coherent receiver concept, (a) block diagrams: optical filters (AWG) for wavelength channel de-multiplexing (b) optical to electrical de-multiplexing flows.

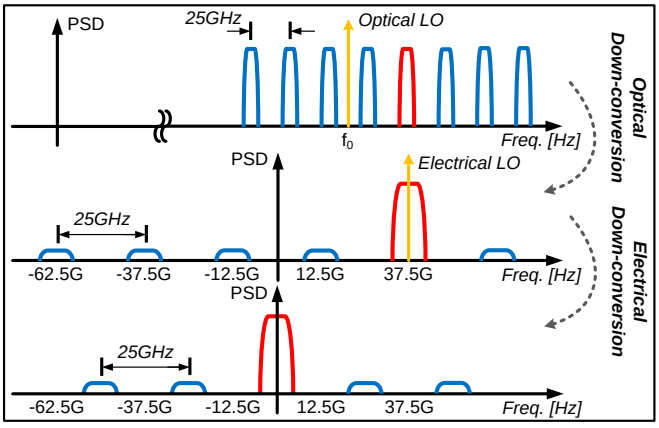
In this work, we have proposed and demonstrated a new coherent WDM receiver architecture (figure 5.2 (a)) which can scale toward Tb/s operation while using only a pair (I and Q phases) of optical detectors to recover multiple wavelength channels. The proposed receiver has a simple circuit configuration, can provide high spectral efficiency, and accommodates a flexible range of channel spacing and data modulation formats. The complexity of the required PIC is greatly reduced, removing the optical filter and leaving only one set of balanced

detectors and an LO laser. Most of the signal processing is instead performed in electrical integrated circuits (EICs). Sets of optical WDM channels are recovered in the EIC using single-sideband (SSB) mixers and their associated LOs as frequency down-converters. The EIC requires only a single broadband trans-impedance amplifier (TIA). Figure 5.2 (b) shows the proposed concept of two step optical and electrical down-conversions. All optical channels are down-converted to the electrical domain as RF sub-carriers and each channel is selected by single-sideband mixers (SSBMs) with the electrical LOs. The rest of section from the outputs of the SSBMs are the same as the conventional WDM receiver.

The channel capacity in the proposed receiver is ultimately limited by the bandwidth of the photodiodes (PDs) and of the de-multiplexing EIC. Very wide bandwidths are now feasible for these components. Uni-travelling carrier (UTC) PDs with 3-dB bandwidth higher than 300 GHz [13] and high-speed InP hetero-junction bipolar transistors (HBTs) having power-gain cutoff frequencies f_{max} greater than 1 THz have both been reported [14–16]. Even silicon-based transistors have attained 500 GHz f_{max} [17, 18]. Amplifier EICs operating above 670 GHz have been reported [19–22]. Given such components, the proposed receiver architecture can scale beyond 1Tb/s capacity using >125 GHz bandwidth PDs and EICs together with dual optical polarizations and 16-QAM modulation. Using 300 GHz photodiodes [13] and transistor amplifiers [23], a single EIC receiver could process 24 WDM channels at 25 GHz channel spacing. Further, in the proposed receiver, the optical channel wavelength allocation can be adjusted dynamically by tuning LO frequencies within the electrical frequency conversion circuits.



(a)



(b)

Figure 5.2: The new proposed WDM receiver concept, (a) block diagrams: a single photonic IC and channel de-multiplexing in the electrical domain (b) optical and electrical two-step de-multiplexing flows.

In this chapter, I will describe (section 2) a new architecture for the coherent multi-channel WDM receiver using cascaded optical and electrical down-conversions. I then describe (section 3) WDM receiver ICs in detail, i.e. each channel WDM receiver ICs for ±12.5, ±37.5, and ±62.5 GHz channels and a full 6-channel WDM receiver IC (25 GHz with 6 channels - DC to 75 GHz bandwidth). To prove the new WDM concept, (section 4) I will describe demonstrations of im-

age rejection and of adjacent channel interference using the two-channel receiver IC and six-channel data reception demonstrations using the broadband analog single sideband mixer. I have successfully demonstrated the proposed concepts using simulation and experimental results, and I will also propose several future directions in section 5.

5.2 A Single-Chip Multi-Channel WDM Receiver Concept

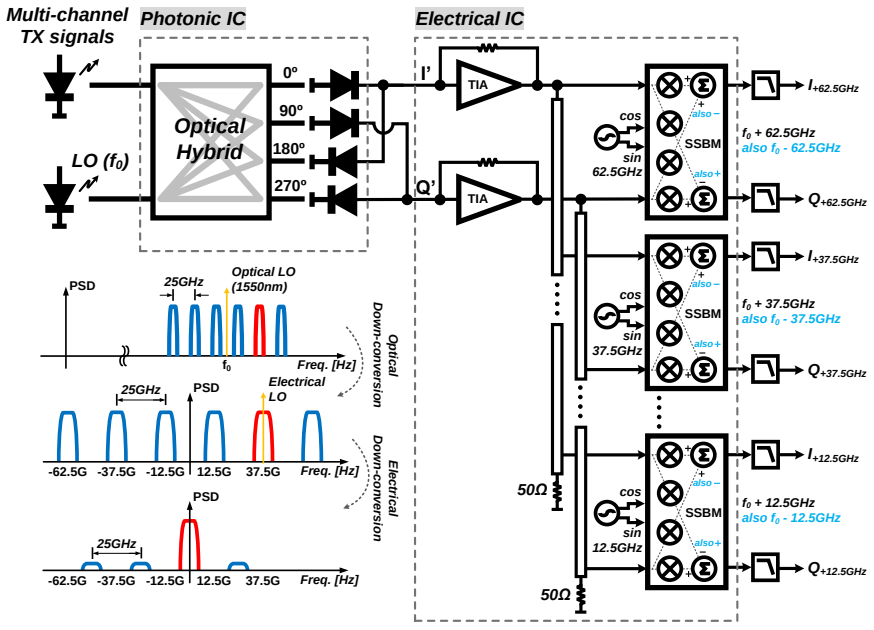


Figure 5.3: A concept schematic diagram for a coherent single-chip multi-channel WDM receiver and its de-multiplexing flows for six modulated channels.

Figure 5.3 shows a six-channel WDM receiver configuration with 25 GHz channel spacing (block diagram level). The receiver de-multiplexes the six channels si-

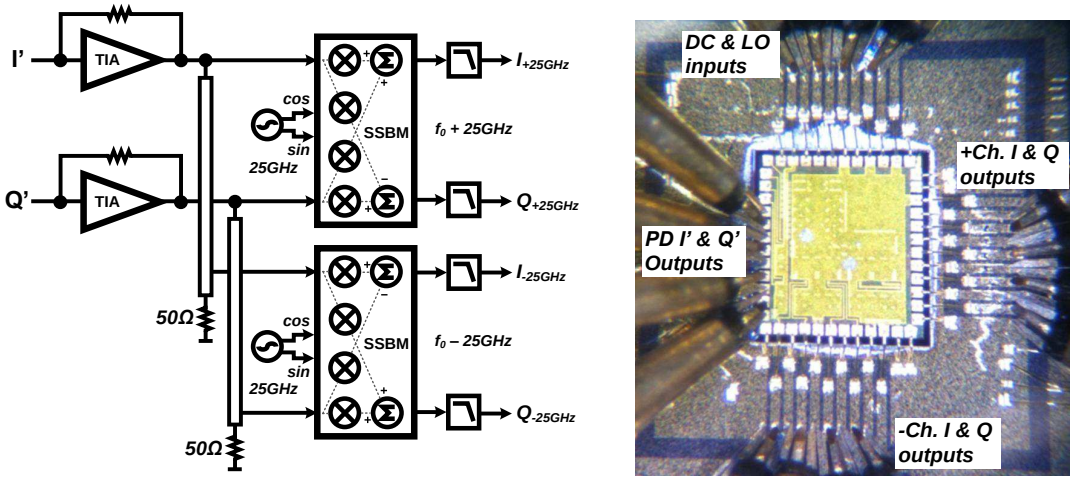
multaneously using a single but broadband PIC and a single but complex EIC. The PIC only includes one standard coherent balanced detector. The EIC includes a broadband TIA, clock and RF signal distribution networks, and broadband analog SSB mixers. Use of single-sideband (SSB) mixers permits the receiver to recover, without crosstalk, WDM channels lying both above and below the frequency of the optical LO. This SSB mixing therefore doubles number of the optical WDM channels which can be recovered within a given EIC and PD analog bandwidth.

De-multiplexing of the six WDM carriers proceeds as follows: 1) An optical hybrid combines the six modulated WDM channels with a relatively strong optical LO (f_0) mixing these together on balanced photodiodes. In this optical down-conversion, the WDM channels become six electrical RF sub-carriers with 25 GHz spacing (at $\pm$12.5 GHz, $\pm$37.5 GHz, and $\pm$62.5 GHz). 2) Each RF sub-carrier is then down-converted to a baseband using the SSB mixer. This signal has both the outputs of I and Q components of the optical modulation. Independent SSB mixers independently recover the ($\pm$12.5 GHz, $\pm$37.5 GHz, and $\pm$62.5 GHz) sub-carriers. 3) Low-pass filters in the I and Q outputs suppress interference from adjacent channels. Data can then be recovered through standard ADC and DSP. Note that if the optical wavelength separations in the WDM transmitter are set by optical wavelength synthesis [3], then the WDM channel frequency separations are determined by the precision of the microwave synthesizers used to set the optical frequency offsets. In this case, the SSB mixers can use stable but asynchronous local oscillators with the resulting LO phase and frequency errors corrected by electrical differential phase-shift-keying demodulation [24–26].

5.3 IC Designs for the Single-Chip 6-Channel WDM Receiver Systems

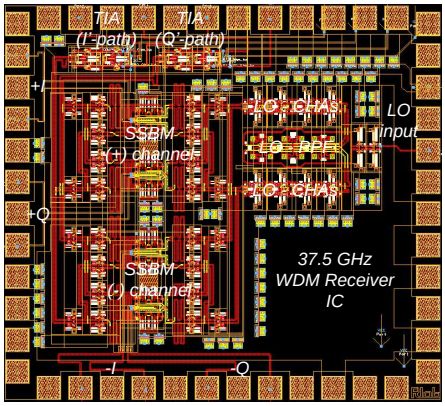
To prove the proposed WDM receiver concept, four different WDM receiver ICs have been designed as two-channel receiver ICs for ±12.5 GHz, ±37.5 GHz, ±62.5 GHz layout, and full six-channel WDM receiver IC using Teledyne's 500 nm InP HBT processes. The HBTs have 300 GHz f_τ and f_{max} and 4.5 V breakdown voltage and four metal layer stacks have been provided for 50 Ω transmission lines for high speed circuit-to-circuit interconnections (figure 2.2) [4].

5.3.1 Two-channel Receiver IC Designs

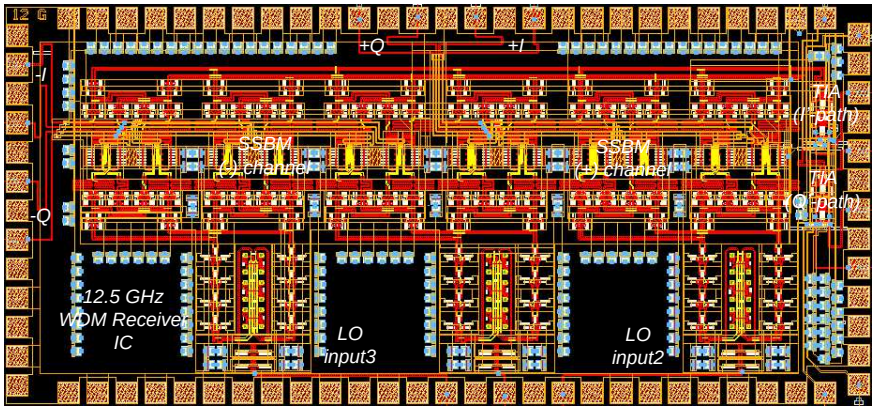


(a) (b)

Figure 5.4: (a) Two-channel WDM receiver circuit schematic for ± 37.5 GHz and ± 62.5 GHz channels, (b) Photo image for the two-channel IC and its probing. PD I' and Q' outputs are connected with the direct probing and others are wire-bonded.



(a)

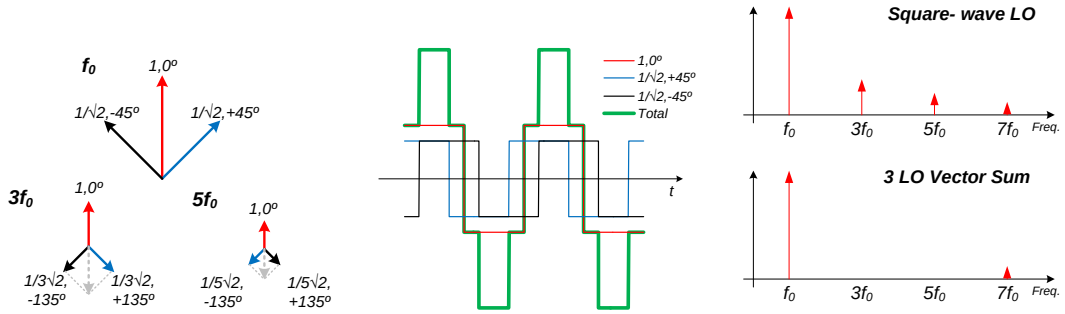


(b)

Figure 5.5: Two-channel WDM receiver circuit layouts for ± 37.5 GHz and ± 62.5 GHz channels (a) and for ± 12.5 GHz channels including three electrical LOs for a harmonic rejection vector summation scheme (b).

As parts of the full channel WDM receiver, three different two-channel WDM receiver ICs were designed for ±12.5 GHz, ±37.5 GHz, and ±62.5 GHz channels as shown in figures 5.4 and 5.5. The receivers consist of a pair of differential broadband resistive feedback TIAs for the input stage, a pair of single-sideband mixers to recover the (+) and (-) channels simultaneously, and LO signal distribution circuits including a single-to-differential amplifier, three-stage poly-phase filters for

sine and cosine signals for single sideband operation, four-stage Cherry-Hooper amplifier chains, and buffers with microstrip line-type signal distributions. Figure 5.4 (a) is a block level IC schematic and (b) is a die photograph taken during testing. The IC layouts shown in figure 5.5 also include a (a) ±37.5 GHz receiver IC and (b) ±12.5 GHz receiver IC including a harmonic rejection technique.



(a) (b) (c)

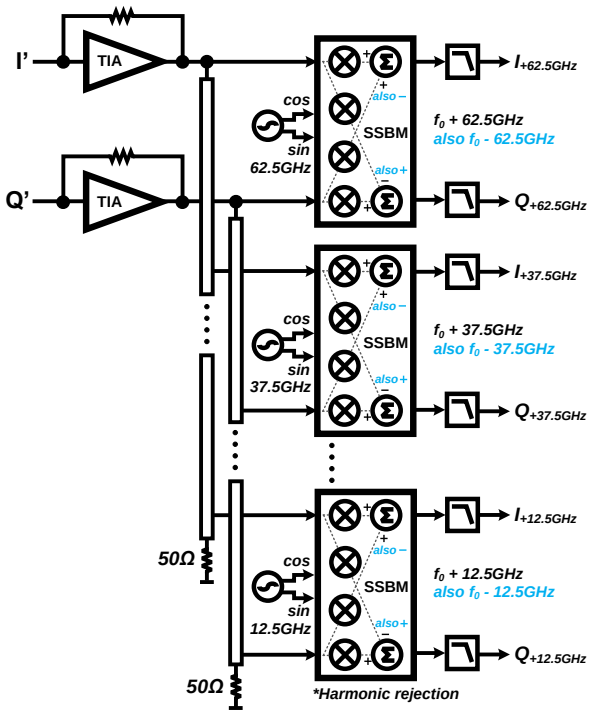
Figure 5.6: Harmonic rejection mixer scheme. (a) The vector sums for the fundamental frequency f_0, the third order harmonic frequency $3f_0$, and the fifth order harmonic frequency $5f_0$, (b) Time domain signal sum for the three vectors, 1 amplitude with 0 degree, $1\sqrt{2}$ amplitude with +45 degree, and $1\sqrt{2}$ amplitude with -45 degree, and (c) Therefore, the 3 LO vector sum shows no harmonic components at $3f_0$ and $5f_0$. [27]

The ±12.5 GHz channel receiver IC differs from receiver ICs for ±37.5 GHz and ±62.5 GHz channels. Since the RF sub-carrier frequencies are again set at ±12.5 GHz, ±37.5 GHz which is 3 × 12.5 GHz, and ±62.5 GHz which is 5 × 12.5 GHz, the down-converted channel, mixed from the 12.5 GHz electrical LO, receivers interference from the other sub-carrier channels at 37.5 GHz and 62.5 GHz, because of the harmonic components of $3f_0$ and $5f_0$ from the 12.5 GHz square wave LO input signal. This is a well-known issue in broadband DTV turner (receiver) ICs and the harmonic rejection mixer scheme can solve this issue

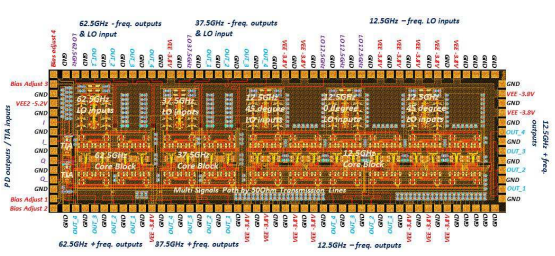
as shown in figure 5.6 [27–30]. This harmonic rejection scheme requires three mixers with 1 (0 degree), $1\sqrt{2}$ (+45 degree), and $1\sqrt{2}$ (-45 degree) vector output summations (figure 5.6 (a)). The fundamental f_0 signals are summed, and the third $3f_0$ and fifth $5f_0$ harmonic signals are canceled. As seen in figure 5.6 (b) and (c), in the time domain, the total summed signal (green) looks more nearly sinusoidal (b), and in the spectral domain, there will be no $3f_0$ and $5f_0$ spectral components after the harmonic vector summations (c). The layout is shown in figure 5.5 (b). Compared with the 37.5 GHz channel receiver IC, the three mixers and three LOs have been used in this 12.5 GHz frequency channel receiver IC.

These two-channel receiver ICs are tested and exhibited more than 25 dB single sideband suppression ratio over the poly-phase filter bandwidth (∼20 GHz). Using the two-channel receiver ICs, image rejection tests and adjacent channel interference tests have been performed as a part of the full six channel WDM receiver ICs. The system experiments and measured results will be discussed in the next sections.

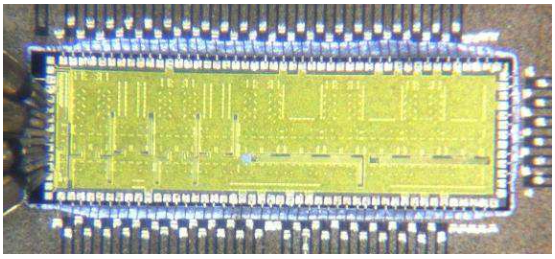
5.3.2 Six-Channel Receiver IC Designs



(a)



(b)



(c)

Figure 5.7: A proposed six-channel WDM receiver IC schematic (a), a layout for the six-channel receiver IC and its port assignments (b), and a photo image of a 6-channel WDM receier IC with wire-bonding on carrier board (c).

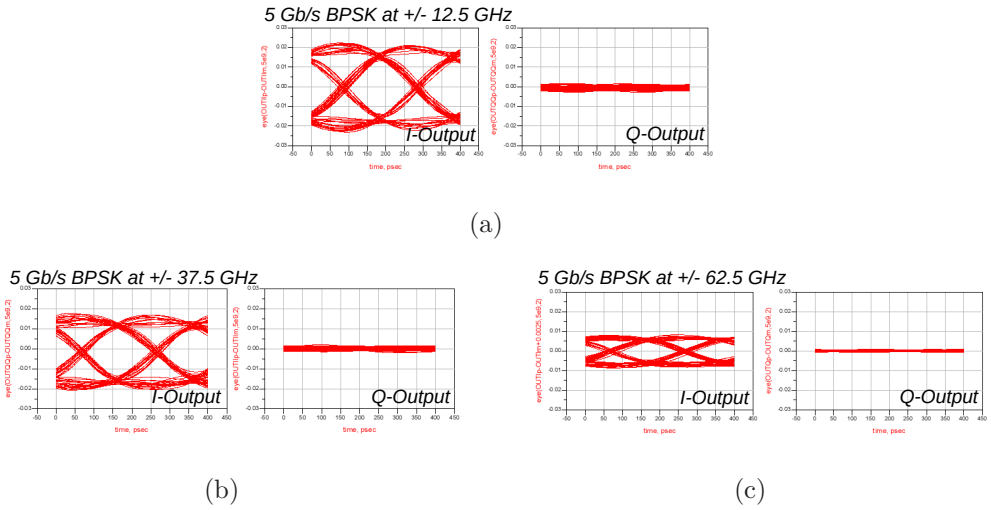
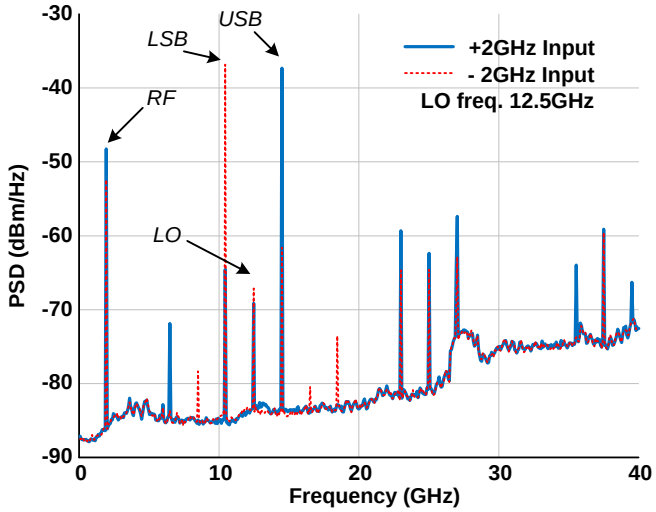


Figure 5.8: Simulation results for the 6-channel WDM receiver ICs. 5 Gb/s BPSK for 6-channels (in total 30 Gb/s) are applied as the inputs signals. The 5 Gb/s BPSK eye diagrams on both ±12.5 GHz I- and Q-outputs (a), 5 Gb/s BPSK eye diagrams on both ±37.5 GHz I- and Q-outputs (b), and 5 Gb/s BPSK eye diagrams on both ±62.5 GHz I- and Q-outputs (c). The eye heights are getting smaller because of the bandwidth EIC bandwidth (limited by the multiple buffer stages).

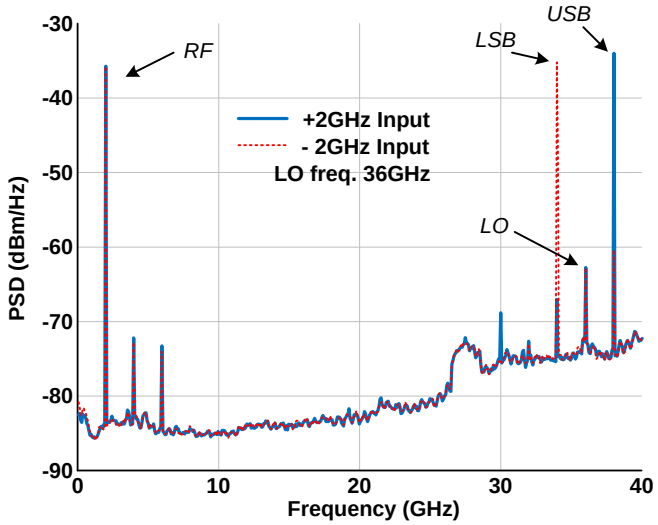
The full six-channel WDM receiver IC has been also designed to receive six WDM data channels simultaneously. The WDM receiver IC schematic, layout and photo image are shown in figure 5.7 (a) block-level schematic, (b) layout with pin information, and (c) IC photo image showing signal wire-bonds, respectively. The WDM receiver IC includes many blocks. A pair of extremely broadband TIAs for the I and Q signal paths are at the input [3]. A double-terminated transmission-line-based network (figure 2.6) distributes the electrically down-converted RF-sub-carriers to each of the receivers. Because of the high conductor losses for the high frequency receiver, the ±62.5 GHz channel receiver is located close to the TIAs. The distributed signals are again distributed using buffered amplifiers with the transmission lines to each core ICs of the single sideband mixers

(SSBM). All transmission lines and their conductor losses and mismatches have been characterized by ADS 2.5-D Momentum electro-magnetic (EM) simulations and included in the circuit and system simulations. The LO signal distribution paths have constructed in a form similar to the input signal distribution networks. The single-ended LO signal is converted to a differential signal for the quadrature sine and cosine signal generation through poly-phase filters. The sinusoidal LO signal is then limited through four stage Cherry-Hooper amplifier chains, as described in previous sub-sections. The square-wave LOs are distributed with the same buffered amplifiers with distributed networks as the input to match the delay and phase of the signals.

In system-level simulations, 5 Gb/s BPSK data, hence a total 30 Gb/s for the six-channels, is successfully performed, and the results of open eye diagram outputs for each channel are shown in figure 5.8. In addition, the designed WDM receiver IC also recovers 2.5 Gb/s QPSK data for all six channels. Higher-order, multi-level constellations and higher bit rates were not simulated because of limited CPU and memory performance in our servers. It is clear that the down-converted I and Q outputs retain their phase and amplitude information. High symbol rates up to 12.5 GHz, the Nyquist channel bandwidth, can be supported. In addition, the bit rates, multiplied by higher symbol rates, i.e. BPSK-1 bit/symbol, QPSK-2 bits/symbol, 8-PSK-3 bits/symbol, and 16-QAM-4 bits/symbol, are feasible, depending on the systems' signal-to-noise ratio (SNR) and bit-error-ratio (BER) tolerance.



(a)



(b)

Figure 5.9: Full six-channel receiver IC measurement results in the electrical spectrum analyzer (ESA). (a) Two-channel results at ±12.5 GHz are shown for the single-sideband suppression and the SSB result of more than 25 dB for both channels, and (b) Two-channel results at ±36 GHz (because of 40 GHz ESA range) are shown for the single-sideband suppression and the SSB result of ∼30 dB for both channels. I could not measure the 62.5 GHz channel because of measurement equipments' bandwidth limits (ESA, signal source, and RF probes.

The six-channel WDM receiver IC was tested as shown in figure 5.9. Single sideband suppression tests for all channels (12.5 GHz and 36.0 GHz LOs) have been performed, and all channels work properly with more than 25 dB single sideband suppression ratio, as predicted from simulation. In this measurement, the proposed harmonic rejection schemes for the 12.5 GHz channel spacing WDM receiver also work properly. The output signals and image suppression capability are changed by changing the phases of LO signals. However, this receiver IC was not used for system-level experiments because of its extremely high DC power consumption of more than 20 W within the small chip size of $5.0 \times 1.3\ mm^2$. This high DC current generates a great deal of heat dissipation, and therefore, the IC performance was degraded. Many buffer blocks for signal distributions, core single sideband mixers and LO distribution chains must be optimized to decrease the IC power consumption and decreasing the IC size. Therefore, the whole system demonstrations for multi-channel WDM receivers have been performed using the core single-sideband mixer (SSBM) ICS with sweeping the LO signals with 10 GHz channel spacing. The detailed experiments will be shown in the next section.

5.4 System Demonstrations and Experimental Results

To demonstrate the WDM receiver system, using the two channel receiver IC (figure 5.4), 1) we have measured image rejection for the two modulated carriers at f_0 $\pm$25 GHz and thus $\pm$25 GHz electrical sub-carriers, and 2) we also have measured adjacent channel interference using three modulated carriers with

channel spacing varying from 5 GHz to 20 GHz. Moreover, we have generated 6-modulated channels with 2.5 Gb/s BPSK data with 10 GHz channel spacing (because of system equipment of an optical modulator analyzer's frequency bandwidth limit), and we have recovered original data for the 6-modulated channels using the single sideband mixer core IC and the different LO frequency from +5 GHz to +25 GHz.

5.4.1 Image Rejection Experiment

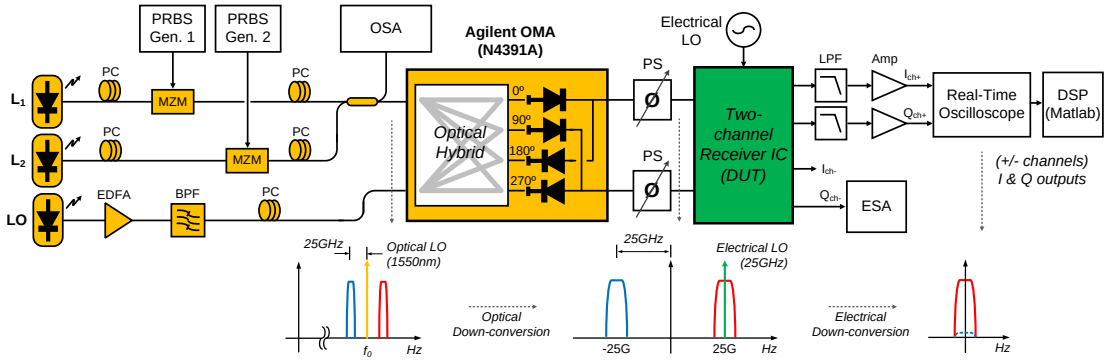
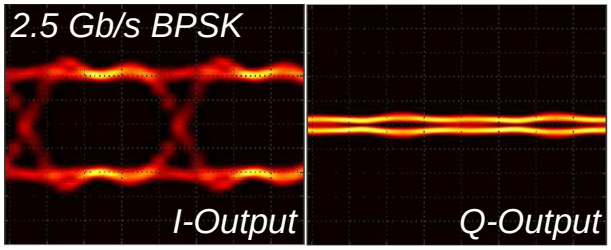


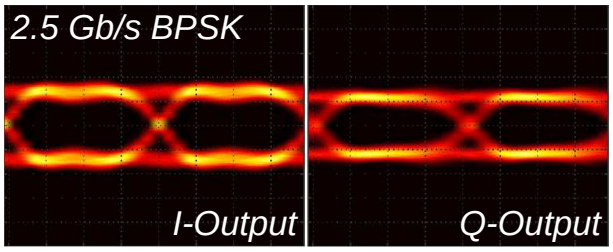
Figure 5.10: Test setup for image rejection using two wavelength channels.

To double the number of WDM channels processed, the single sideband mixers are used in the receiver IC, independently recovering signals both below and above the optical LO frequency. Figure 5.10 shows a test configuration of the image rejection experiment. Three free-running distributed feedback (DFB) lasers, which have a narrow linewidth and low relative intensity noise (RIN), are used: L_1 as a transmitter carrier laser #1 at optical carrier frequency f_0 +25 GHz, L_2 as a transmitter carrier laser #2 at frequency f_0 -25 GHz, and L_3 as the LO laser at frequency f_0. The carrier lasers L_1 and L_2 are modulated using 2.5 Gb/s

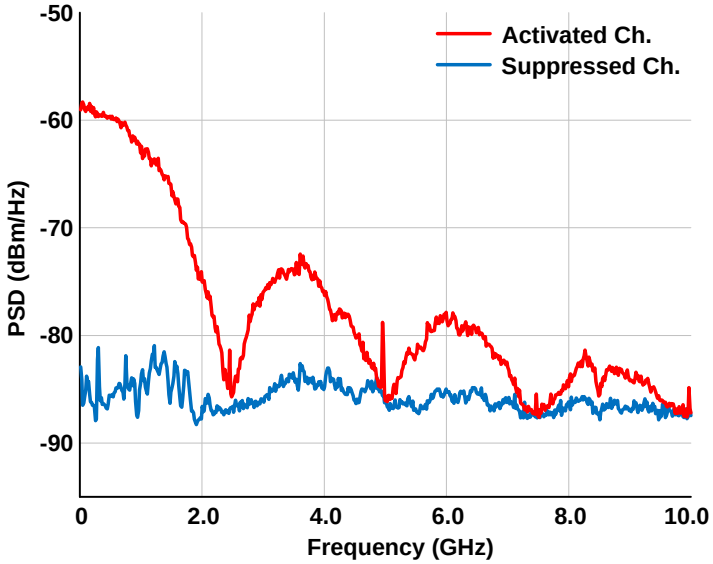
binary-phase-shift-keying (BPSK) data with two pseudo-random-binary-sequence (PRBS) pattern generators and Mach-Zehnder modulators (MZMs). PRBS of lengths $2^{31}-1$ and $2^{15}-1$ are applied to lasers L_1 and L_2 in this test. The modulated channels are combined in a 50/50 optical directional coupler and coupled to the optical signal port of the receiver, with the LO laser L_3 connected to the receiver LO port.



(a)



(b)



(c)

Figure 5.11: Experimental results for image rejection measurement: The eye diagrams for the activated (+) channel and the suppressed (-) channel with a single modulated carrier (a), the eye diagrams for the (+) and (-) channels with two modulated carriers (b), and the measured output spectra when the signal and the adjacent (crosstalk) channels are active. Crosstalk suppression is ∼25dB (c).

In this experiment, we have used a free-space 90 degree optical hybrid and balanced PDs contained in an Agilent optical modulation analyzer (OMA) N4391A. The balanced PDs have more than 33 GHz 3-dB-bandwidth. The relative delays of the I-channel and Q-channel cables between the OMA and the two-channel receiver IC were carefully matched within 50 ps by adjusting RF cable lengths and using phase shifters. This delay mismatch limits the bit rate to no more than 2.5 Gb/s, but this mismatch issue can be solved by the hybrid integration of PIC and EIC. The EIC was contacted using multi-finger GGB RF probes. The two-channel receiver IC has I and Q outputs for both the $\pm$25 GHz channels. One pair of I_{ch+} and Q_{ch+} outputs was low-pass filtered, amplified, and stored in an Agilent real-time oscilloscope (DSA-X 92004A). Frequency and phase errors were corrected by DSP (in this work, we used a simple phase error estimation technique using a Matlab code), thereby recovering the $I-Q$ transmitted data streams, as shown in figure 5.11 (a)-(b). The second pair of I_{ch-} and Q_{ch-} outputs are connected to an electrical spectrum analyzer (ESA) to monitor the suppression of adjacent-channel interference in the frequency domain. Figure 5.11 (c) shows the spectra measured from the EIC output, comparing the cases when one of the lasers L_1 and L_2 is active (or suppressed).

Figure 5.11 (a) show the recovered data outputs on (+) and (-) channels using a single 2.5 Gb/s BPSK modulated carrier (L_1 is on and L_2 is off) without the 50/50 directional coupler. After the post signal processing, figure 5.11 (a)-left shows fully activated (open) eye diagram on the (+) channel, and figure 5.11 (a)-right shows suppressed (closed) eye diagram on the (-) channel. Figure 5.11 (c) indicates that there is about 25 dB (18:1 in voltage) image rejection ratio between

the activated and suppressed channels. This is typical of that expected for well-designed SSB mixers. Regarding two 2.5 Gb/s BPSK modulated carriers (L_1 is on and L_2 is on), both (+) and (-) channels show open eye diagrams, as shown in figure 5.11 (b). The slightly degraded eye diagrams in this test are most likely because the input power to the two-channel receiver IC is 2:1 lower than that in the experiment involving only a single modulated carrier.

5.4.2 Adjacent Channel Interference Experiment

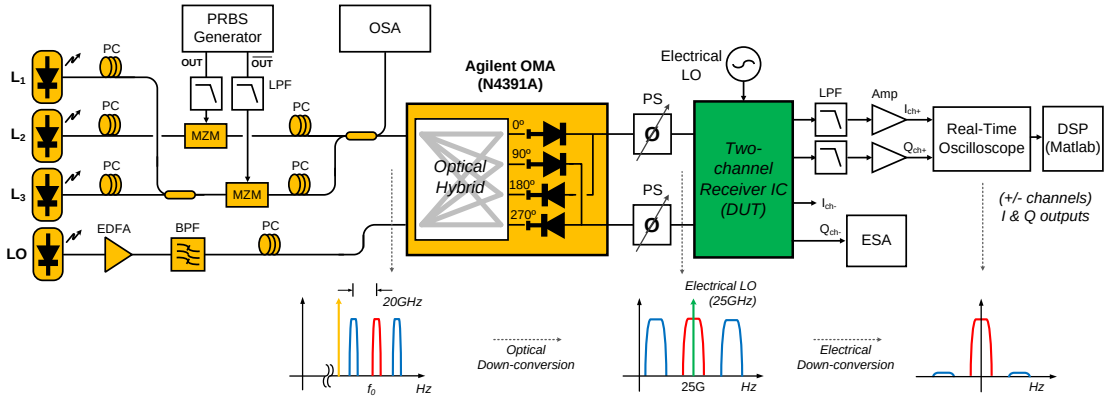
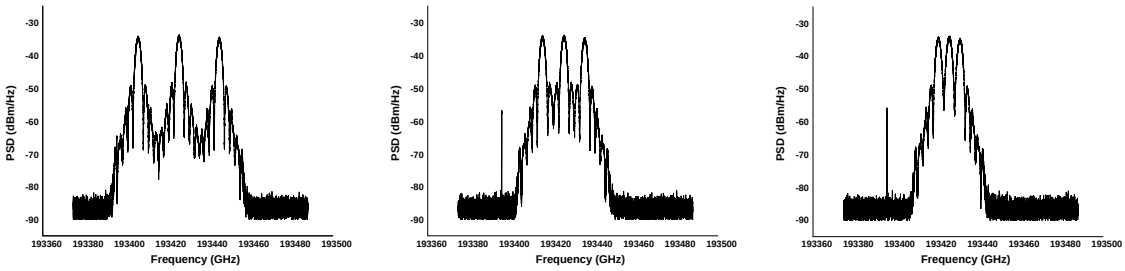


Figure 5.12: Test setup for adjacent channel interference measurements using three wavelength channels.



(a) (b) (c)

Figure 5.13: Measured optical spectra for different channel spacing: (a) 20 GHz, (b) 10 GHz, and (c) 5 GHz. The narrow band tone visible in (b) and (c) is from the LO laser.

To measure receiver crosstalk from adjacent channels and to determine the maximum spectral efficiency given the minimum channel grid spacing, three-channel experiments have been performed using the test configuration shown in figure 5.12. Three DFB lasers and a Koshin (LS-601A) tunable laser, which also have a narrow linewidth and low RIN, are used: L_1 as a transmit carrier laser #1 at an optical frequency variable from f_0 +5 GHz to f_0 +20 GHz, L_2 as a fixed transmit carrier laser #2 at an optical frequency f_0 +25 GHz, L_3 as a transmit carrier laser #3 at an optical frequency variable from f_0 +30 GHz to f_0 +45 GHz, and L_4 as a fixed LO laser at frequency f_0. Again, three channels of 2.5 Gb/s BPSK data are modulated on the carrier lasers of L_1, L_2 and L_3 using differential outputs of a PRBS $2^{31} - 1$ pattern generator and two MZMs as shown in figure 5.12. The two patterns are de-correlated using a path length difference of about one meter. The three modulated channels are combined using 50/50 directional couplers and the power of each channel is equalized and monitored through an APEX high-resolution optical spectrum analyzer (OSA). Figure 5.13 shows the measured spectrum of the three optical modulated channels with channel grids of

(a) 20 GHz, (b) 10 GHz and (c) 5 GHz, the final case having no frequency guard band.

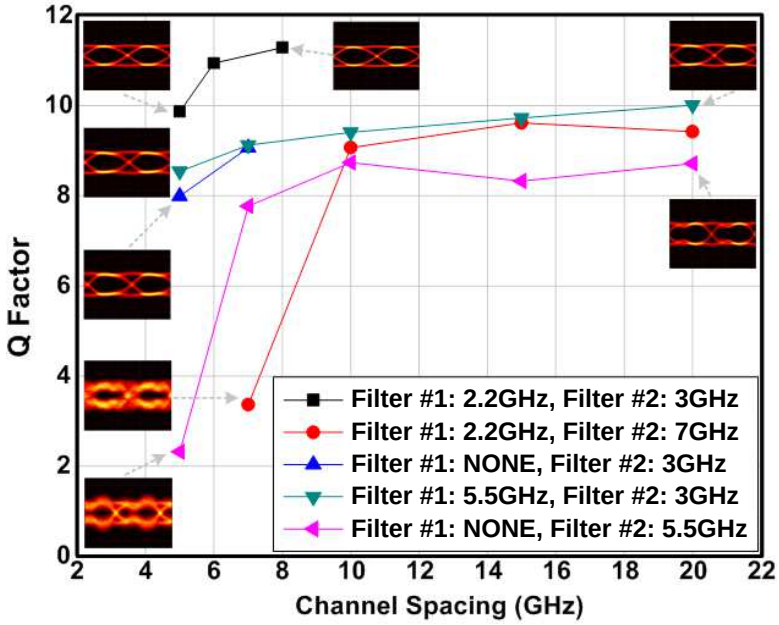


Figure 5.14: Measured eye diagram qualities for the different channel spacing and filter combinations (filter #1 before the optical modulators, and filter #2 after the EIC).

In this experiment, the quality of the recovered data were measured and compared in figure 5.14 for the different channel spacing and differing combinations of input and output low-pass filter bandwidths. Here filter #1 is low pass filters (LPFs) located before the optical modulators (MZMs) to suppress spectral side lobes in the transmitted optical spectrum, while filter #2 is LPFs located at the two-channel receiver IC outputs to suppress adjacent channel interference. With 2.2 GHz LPFs in the transmitter and 3 GHz LPFs in the receiver, even with a 5GHz channel spacing, corresponding to no frequency guard band, a signal-to-noise including interference ratio (Q-factor), extracted from eye diagram outputs,

of approximately 10:1 is measured. Note that $Q = 6$ corresponds to 10^{-9} BER given Gaussian statistics.

As figure 5.14 demonstrates, the receiver IC operates with high signal/crosstalk ratios even when channels carrying 2.5 Gsymbol/second modulation are spaced in frequency by only 5 GHz; the proposed WDM receiver system provides high spectral efficiency.

5.4.3 6-Channel Data Reception Experiment

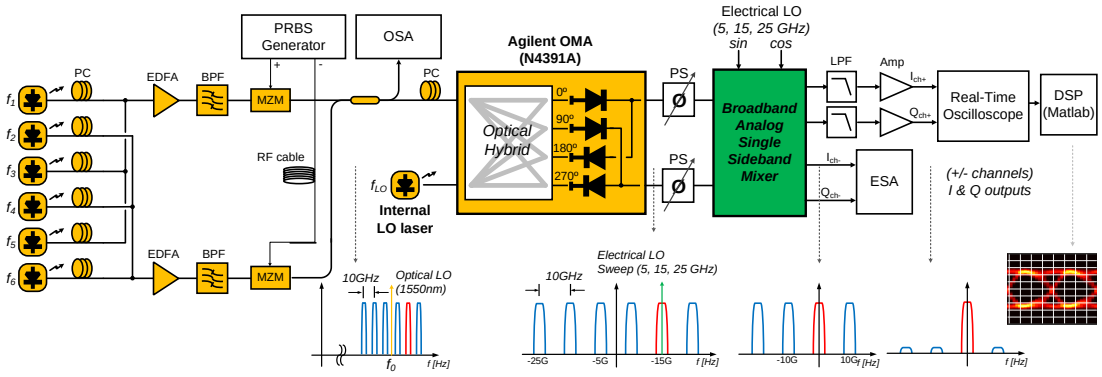


Figure 5.15: Test setup for 6-channel data reception measurements using the core analog single-sideband mixers.

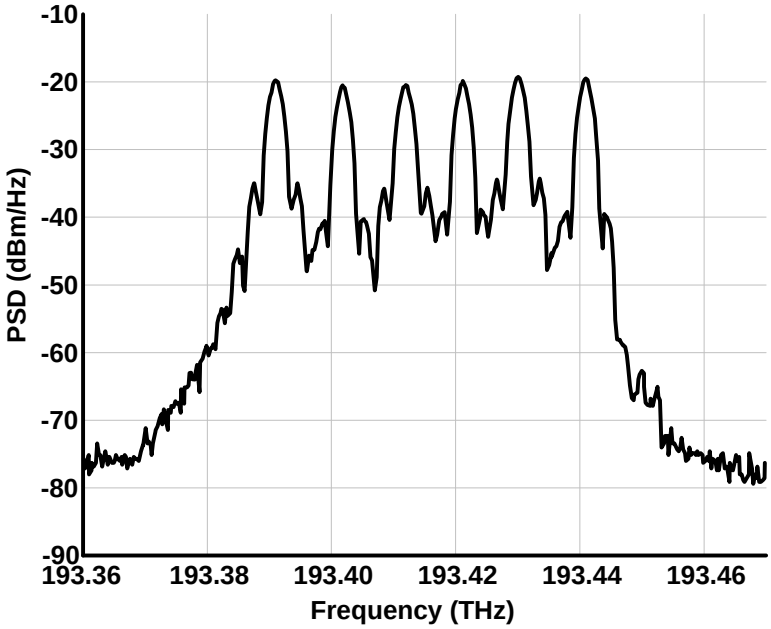
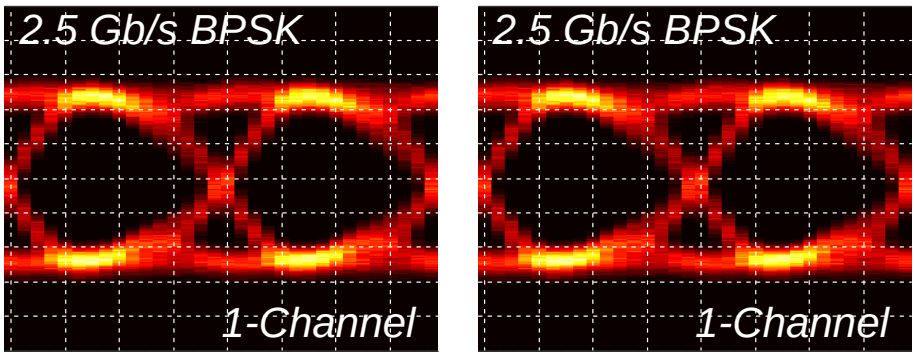


Figure 5.16: Six-modulated channels using six-independent laser sources, two high speed Mach-Zehnder modulators (MZMs), and one-differential PRBS pattern generator.

Finally, to verify our proposed concept of the single-chip multi-channel WDM receiver, the 6-channel experiments were performed using a test configuration shown in figure 5.15. The key blocks, the broadband analog single-side-band mixers (A-SSBMs), 6 modulated channels, a single fixed-frequency optical LO laser, and a widely swept electrical LO (±25 GHz, ±15 GHz, and ±5 GHz) were used in the tests. The 6-independent lasers (three DFB, two Agilent tunable and one Koshin tunable lasers) are used as carriers for the 6 modulated WDM channels: each laser source from f_1 - f_6 are set with 10 GHz channel spacings and 2.5 Gb/s BPSK modulated data using the differential 2.5 Gb/s PRBS $2^{31}-1$ patterns with different lengths of the RF cables (more than 1 m length difference) to de-correlate the data patterns in each channel. Due to the limited number of BPSK modulators

available at UCSB, two high speed Mach-Zehnder modulators (MZMs) have been used to generate the 6 modulated channels. To separate the channel data from the adjacent channels, the lasers f_1, f_3 and f_5 are combined, then passed through one modulator, and the lasers f_2, f_4 and f_6 are combined and passed through the second modulator. Each data extinction ratio has been measured through an optical sampling oscilloscope, and then, the total 6-modulated channels has been observed in the Apex's optical spectrum analyzer as shown in figure 5.16. The optical signal intensity has been carefully adjusted within less than 1 dB power for the all-modulated channels. Again, the Agilent's optical modulation analyzer (OMA-N4391A) has been replaced by the coherent balanced detector (90 degree optical hybrid and high speed photodetectors), and the photodetectors show more than 33 GHz 3-dB bandwidth. An internal local oscillator (LO) laser in the Agilent OMA was used and the LO frequency is set and adjusted to the middle of f_3 - f_4 lasers.



(a) (b)

Figure 5.17: Single-sideband suppression tests using the core SSBM ICs. (a) The eye-diagram with single-channel 2.5 Gb/s BPSK modulated data, and (b) The eye-diagram with two modulated channels (± 5 GHz).

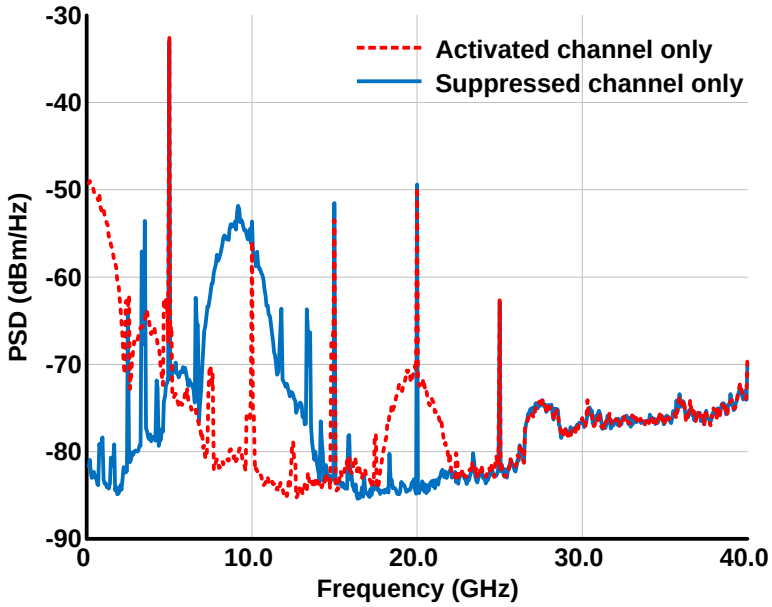


Figure 5.18: Down-converted spectra to measure the single-side suppression ratio (>30 dB) - measured through the ESA.

In this 6-channel experiment, I have successfully demonstrated (recovered) all 6-channel data, not simultaneously, but one by one with sweeping the electrical LO from 5 GHz to 25 GHz. As learned from the previous 3-channel data recovery experiments, the 3 GHz electrical filters prior to the optical modulators and after the EIC have been used for optimum data reception. I also used the same Matlab code (corresponded to the DPS functions) for the all 6-channel 2.5 Gb/s BPSK data recovery.

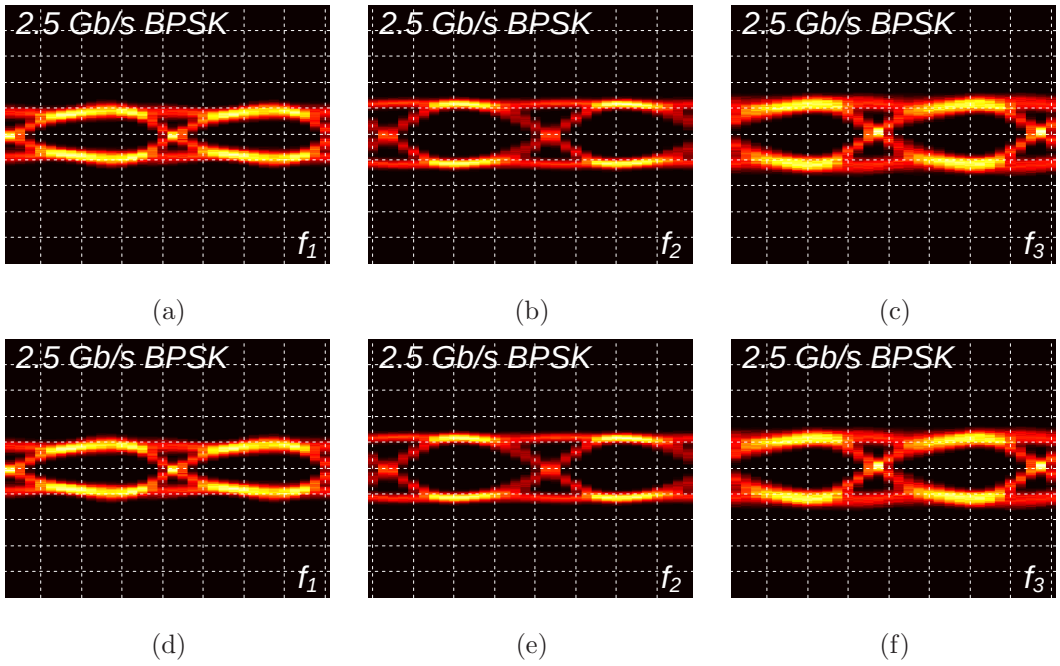


Figure 5.19: Six-channel eye outputs: the modulated channels (f_3 and f_4) close to the LO laser show more opened eye outputs than other channels.

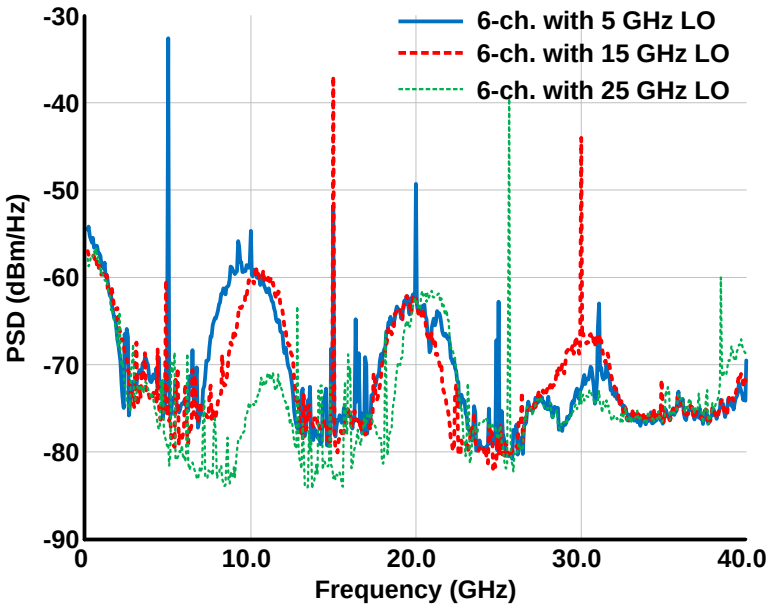


Figure 5.20: Six-channel down-converted spectra with the 5, 15 and 25 GHz electrical LOs.

First, the single sideband image rejection experiment was repeated using two-channel modulated signals (at ± 10 GHz). Fully open eye diagrams were obtained, as shown in figure 5.17. The wideband frequency spectrum results up to 40 GHz show high single-sideband image rejection ratios of more than 30 dB for both the activated channel and the suppressed channel with ± 10 GHz electrical LOs (figure 5.18). After proving the 2-channel system, I then applied all 6 channels, forming the spectrum shown in figure 5.16. These signals were applied to the receiver IC (analog single sideband core) through the OMA, and the output of the receiver IC was captured on an oscilloscope and processed off-line with Matlab code. This recovered fully open BPSK eye diagrams as shown in figure 5.19. Due to the limited bandwidth of the photodetectors in the OMA and the electrical ICs, the signal-to-noise ratio (SNR) in the eye diagrams are slightly degraded for the channels (i.e. f_1 and f_6) which are far in frequency from the optical LO signal (i.e. the high-frequency RF sub-carriers). Figure 5.20 shows the EIC's output spectrum as the electrical LO frequencies are changed (5, 15 and 25 GHz). The power of the down-converted signal near DC again is slightly reduced because of their higher frequency RF sub-carriers.

It would have been preferable to demonstrated the 6-channel receiver with all data channels recovered simultaneously using the full-six channel WDM receiver IC. As mentioned, since the WDM receiver ICs for the six-channel consumed over 20 W DC power, heat dissipation was excessive, and such system-level experiments were not possible. The above experiments and their results fully verify that the electrical multi-channel WDM receiver is feasible.

5.5 Conclusion

We have demonstrated a WDM receiver using cascaded optical and electrical down-conversion to recover multiple optical wavelength channels. Given the demonstrated bandwidth of modern photodiodes and EICs, the receiver can readily scale to a large number of WDM channels using only a single (I and Q) pair of optical coherent detection channels. Three full demonstrations indicate high image rejection, low adjacent channel interference, and full data recoveries within the multi-modulation channels.

Using the proposed concepts with optimized IC designs, it is possible to decrease the receiver complexity, the power consumption, IC size, and cost, and to increase the spectral efficiency. In this receiver, the channel bandwidth allocations and symbol rate are flexible. More than 1 Tb/s receivers using the single multi-channel electrical IC may be feasible.

5.6 Additional Analysis-I: RF Sub-Carrier Generations for Circuit Simulations

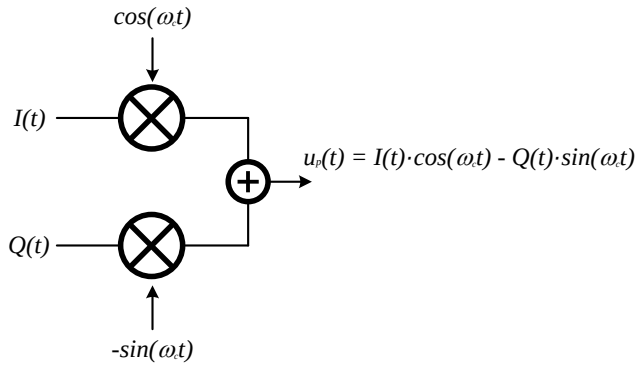


Figure 5.21: Optical I-Q modulation concept. $u_p(t)$ is the up-converted $I-Q$ modulated signal, and the multi-channels are generated with different frequencies ω_c.

I have generated multi-channel RF sub-carriers for ADS circuit simulations. As $I-Q$ modulations, two independent $I(t)$ and $Q(t)$ are modulated using a carrier frequency of ω_c (1550 nm, ∼194 THz for optical fiber communications) as shown in figure 5.21. Data $I(t)$ is mixed by the $cos(\omega_c t)$, another data $Q(t)$ is mixed by the quadrature $-sin(\omega_c t)$ and two up-converted signals are added in the optical domain as

$$u_p(t) = I(t)\cdot cos(\omega_c t) - Q(t)\cdot sin(\omega_c t). \tag{5.1}$$

The optically phase modulated signal $u_p(t)$ is optically mixed with an optical local oscillator (LO), $cos(\omega_{LO} t)$, in an optical hybrid and down-converted by the arrays of photodiodes for 90 degree output of phase signals in the electrical domains as shown in figure 5.22. Here is an important assumption. The intensity (power)

of the optical LO $cos(\omega_{LO}t)$ must be much higher (i.e. 100:1) than the optical channels to avoid cross modulation between the WDM channels. In this condition, the down-converted electrical photocurrent outputs I'(t) and Q'(t) are derived as

$$I'(t) = (u_p(t) + cos(\omega_{LO}t))^2 \approx 2u_p(t) \cdot cos(\omega_{LO}t)$$
$$Q'(t) = (u_p(t) - sin(\omega_{LO}t))^2 \approx 2u_p(t) \cdot sin(\omega_{LO}t), \quad (5.2)$$

where the high frequency components of $(u_p(t))^2$ and $(sin(\omega_{LO}t))^2$ are filtered out and ignored in this equation. The first optically down-converted data I'(t) and Q'(t) as the RF sub-carriers should consider both $I(t)$ and $Q(t)$ components on I'(t) and also Q'(t). Therefore, the test setups for the electrical circuit simulations are as shown in figure 5.23. To generate the direct RF sub-carriers in our circuit simulations, the PRBS $I(t)$ and $Q(t)$ modulated signals are up-converted by $cos(\omega_{LO2}t)$ and $sin(\omega_{LO2}t)$, where $\omega_{LO2} = \omega_c - \omega_{LO}$, and summed and band-pass filtered as shown in figure 5.23. The final I'(t) and Q'(t) are derived as

$$I'(t) = 1/2I(t)cos(\omega_{LO2}t) - 1/2Q(t)sin(\omega_{LO2}t)$$
$$Q'(t) = 1/2I(t)sin(\omega_{LO2}t) + 1/2Q(t)cos(\omega_{LO2}t), \quad (5.3)$$

where the high frequency components are filtered out. The other RF sub-carrier channels are generated using different frequencies with independent PRBS seed values and root raised cosine filters (matched filter) for each frequency.

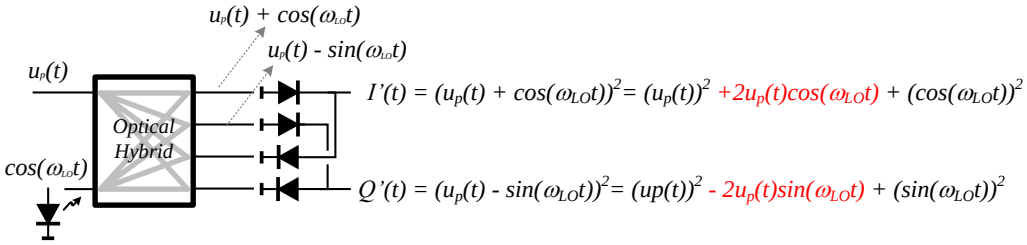


Figure 5.22: Optical to electrical down-conversions through the optical hybrid and by photodiodes. Outputs of photodiodes are $I'(t)$ and $Q'(t)$.

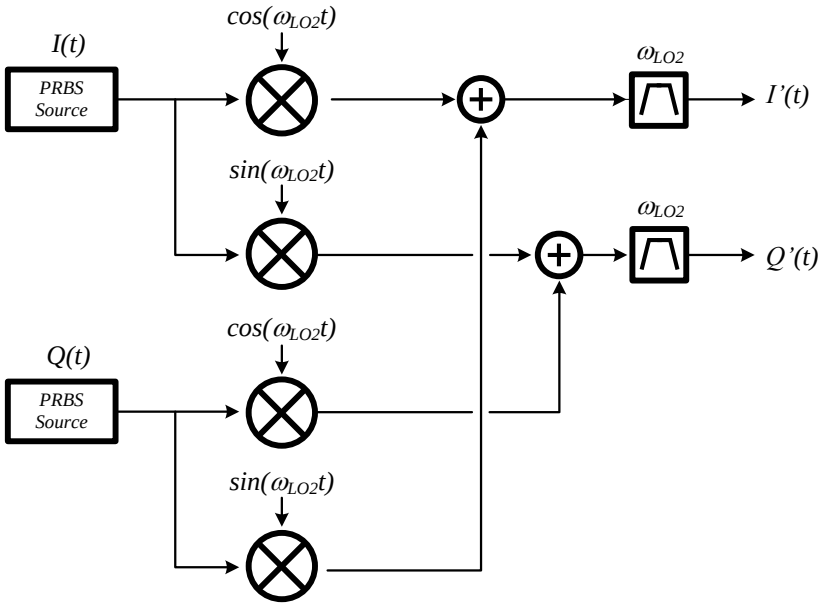


Figure 5.23: ADS circuit simulation setup for the modulated channel sources of the WDM receiver ICs. All-channels are independently modulated by different seeds for the PRBS $I-Q$ sources and ω_{LO2} is RF-subcarrier frequencies, i.e. $\omega_{LO2} = \pm 12.5$ GHz, ± 37.5 GHz and ± 62.5 GHz) .

5.7 Additional Analysis-II: Local Oscillator (LO) Laser Power

One of the main concerns in WDM receiver systems is a system efficiency, and total required optical local oscillator (LO) power is one of the critical issues in the proposed WDM receiver design. In this analysis, I have compared the LO power requirements of a conventional WDM receiver array with that of the proposed WDM receiver. Simply, the conventional receiver array with N wavelengths requires N LO lasers, while the proposed electrical WDM receiver requires only a single LO laser. At first examination, it would appear that considerably smaller total LO power is required. Yet, optical cross-modulation in the proposed electrical/optical WDM receiver somewhat increases the necessary LO power for this topology. The total LO power remains well below that of the conventional WDM receiver array.

I will first calculate how much LO power and input signal power are required for a maximum signal-to-noise ratio (SNR) including shot and thermal noise. Then, I will compare how much LO power and input signal power are required for a maximum SNR and signal-to-interference ratio (SIR), with the interference resulting from optical intermixing between adjacent channels.

First, the optical signal field is defined as

$$E_s(t) = \sqrt{P_s} \cdot exp(j\omega_s t + \phi_s)$$
$$E_{LO}(t) = \sqrt{P_{LO}} \cdot exp(j\omega_{LO} t), \tag{5.4}$$

where E_s, P_s, ω_s, ϕ_s are input signal field, power, frequency, and phase, respec-

tively, and E_{LO}, P_{LO}, and ω_{LO} are LO signal field, power, and frequency. The photocurrent $I_{PD}(t)$ produced by the combined optical signal and LO is

$$I_{PD}(t) = \eta \frac{q}{h\nu} \cdot P_{opt}(t) + I_n, \tag{5.5}$$

where η is a quantum efficiency $[A/W]$, q is the electron charge 1.6×10^{-19} $[Coulombs]$, h is Planck's constant 1.05×10^{-34} $[J-s]$, ν is the optical frequency 1.94×10^{14} $[Hz]$, P_{opt} is $[E_s(t) + E_{LO}(t)]^2$, and I_n includes shot and thermal noise. $I_{PD}(t)$ also can be expressed by power and current terms as

$$\begin{aligned} I_{PD}(t) &= \eta \frac{q}{h\nu} [P_s + P_{LO} + 2\sqrt{P_s \cdot P_{LO}} \cdot sin(\phi_s)] + I_n \\ &= I_s + I_{LO} + 2\sqrt{I_s \cdot I_{LO}} \cdot sin(\phi_s) + I_n. \end{aligned} \tag{5.6}$$

The current noise spectral density $S_n(f)$ includes shot noise and thermal noise as

$$S_n(f) = 2qI_{DC,PD} + \frac{4KTF}{Z_0}, \tag{5.7}$$

where $I_{DC,PD}$ is a photocurrent DC component, KT is a product of the Boltzmann constant K and temperature T, F is the electrical amplifier noise factor, and Z_0 is the TIA termination impedance. Because $I_s \ll I_{LO}$ in general, the noise spectral density $S_n(f)$ is approximated as

$$S_n(f) \approx 2qI_{LO} + \frac{4KTF}{Z_0}, \tag{5.8}$$

the noise power (RMS) is

$$< i_n^2 >= \left(2qI_{LO} + \frac{4KTF}{Z_0} \right) \cdot B \tag{5.9}$$

and the RMS signal power $i_{sig,rms}^2$ is

$$i_{sig,rms}^2 = 2I_s \cdot I_{LO}. \tag{5.10}$$

Therefore, the signal to noise ratio is

$$SNR(W/W) = \frac{I_s}{qB}\frac{1}{1+\frac{2KTF}{qZ_0 I_{LO}}}. \tag{5.11}$$

In order to keep the SNR of $\frac{I_s}{qB}$, a minimum LO photocurrent current (power) of $I_{LO} > \frac{2KTF}{qZ_0}$ is required to keep the SNR within 3dB of the shot-noise limit. If we assume $Z_0 = 50\ \Omega$ and $F = 1.0$, then the minimum current is 1.04×10^{-2} $[A]$. This corresponds to an LO optical power of 8.30×10^{-3} $[W]$ if we assume 100% quantum efficiency. In order to have minimum SNR above the shot noise, minimum signal photocurrent per WDM optical channel is required as

$$I_{s,min}(t) = Q^2 \cdot q \cdot B, \tag{5.12}$$

where the Q-factor of 6 (SNR=36) is assumed, giving a BER of $< 10^{-9}$ for uncoded BPSK data. Therefore, the minimum input photocurrent is required to have 5.76×10^{-8} $[A]$, where the data bandwidth (bit rate) B is assumed to be 10 Gb/s. The corresponding optical signal power is 4.60×10^{-8} $[W]$.

In summary, the coherent WDM receiver systems require a minimum input signal power of 4.60×10^{-8} $[W]$ and a minimum optical LO power of 8.30×10^{-3} $[W]$. As expected, the LO power is much higher than the input power ($\sim 1 : 10^5$ ratio, five orders of magnitude). For N WDM channels, N greater optical LO power is then required.

Our proposed WDM receiver systems may require also strong LO power to keep high SNR as well as high SIR from WDM channel-to-channel interference. The most critical interference is a second order intermixing between most adjacent channels. For N WDM receiver channels, there are at most $(N-1)$ of intermixing frequency components falling into a desired signal channel, and it is represented

by

$$I^2_{sig,IM2} = 2(N-1)\cdot(DR\cdot I_{s,min})^2. \tag{5.13}$$

Here we have assumed in input signal DR:1 larger than $I_{s,min}$, where DR is the receiver dynamic range. Then, the SIR is derived as

$$SIR(W/W) = \frac{I_{LO}}{(N-1)\cdot I_s}, \tag{5.14}$$

where $I_s = DR\cdot I_{s,min}$. In order to have a minimum SIR against such multi-channel interference, a minimum LO photocurrent $I_{LO,min2}$ is required, where

$$I_{LO,min2}(t) = Q^2(N-1)\cdot DR\cdot I_{s,min}. \tag{5.15}$$

If N is 20 and $DR = 10$, then $I_{LO,min2}(t) = 4.15 \times 10^{-4}$ $[A]$, which is still much less than $N \times I_{LO,min}(t) = 2.08 \times 10^{-1}$ $[A]$.

In conclusion, the optical LO power requirement for our proposed electrical/optical WDM receiver is far below that required for an array of receivers in the conventional WDM architecture.

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Chapter 6

Summary and Future Work

6.1 Summary

Using high speed integrated circuits (ICs), I have improved coherent optical components and communication systems. First, in homodyne optical phase locked loops (OPLLs), integrated sampled grating-distributed Bragg reflector (SG-DBR) lasers have been stabilized by a feedback loop including photonic integrated circuits, high speed electrical circuits and loop filter. The linewidth of the SG-DBR laser exhibited <100 kHz linewidth which is the same linewidth performance of a reference laser. The un-locked SG-DBR laser's linewidth was ∼10 MHz, which is not suitable for coherent local oscillator (LO) laser sources for multi-bits per symbol modulation formats, i.e. QPSK, 16-QAM. Because of the homodyne OPLL, the SG-DBR laser can reduce phase noise for wide frequency ranges and can dynamically track a reference laser carrier frequency and phase as coherent optical BPSK receivers.

The homodyne OPLL was designed using integration of photonic IC (PIC), electrical IC (EIC) and loop filter. It was integrated on a single AlN carrier board, and realized within a compact size of $10 \times 10\ mm^2$. Our homodyne OPLL operated stably with a closed loop bandwidth of 1.1 GHz, propagation loop delay of 120 ps, pull-in time of 0.55 μs, lock time of less than 10 ns, and hold-in range of $\sim$15 GHz. The coherent optical receiver based on the homodyne OPLL exhibited 40 Gb/s BPSK data recovery with BER of $< 10^{-7}$ and 35 Gb/s data recovery with BER of $< 10^{-12}$.

A heterodyne OPLL was also designed by the PIC (the same PIC in the homodyne OPLL), EIC (including a digitally operating single-sideband mixer and a PFD), and loop filter. All ICs were highly integrated in a compact size of 10 $\times$ 8 mm^2. Our heterodyne OPLL operated stably with loop bandwidth of >550 MHz and propagation loop delay of <200 ps. An initial heterodyne OPLL showed frequency synthesis from -6 GHz to -2 GHz frequency offsets and from 2 GHz to 9 GHz frequency offsets. An improved heterodyne OPLL performed frequency synthesis of up to 20 GHz. The improved OPLL has a higher photocurrent and better I and Q signal balance. For the beat spectrum between the locked homodyne OPLL and a reference laser, the measured phase noise performance showed -110 dBc/Hz at 10 MHz offset and -80 dBc/Hz at 5 kHz respectably.

Using our high speed and broadband ICs, a new WDM receiver concept was proposed and designed for digital coherent optical fiber communications. Compared with the conventional WDM receiver, our proposed WDM receiver can be simple, compact, flexible, and inexpensive, because of its simple photonic circuit configuration and high speed broadband electrical circuits. To prove the proposed

WDM receiver concept, I have designed several electrical ICs and demonstrated three main system experiments of image rejections, adjacent channel suppressions and six-channel data receptions. The WDM receiver performed image rejection of >25 dB to double the number of the WDM channels, gridless channel operation to maximize the spectral efficiency, and 6-channel data reception at a total 15 Gb/s (2.5 Gb/s BPSK $\times$ 6-channels).

In addition, many high speed ICs have been designed for our coherent optical fiber communication and systems: 107 GHz 3-dB bandwidth resistive feedback amplifiers as TIAs, modified Darlington-type limiting amplifiers for OPLL inputs, Cherry-Hooper amplifiers for WDM receiver LO clock chains, analog/digital single-sideband-mixers as core blocks for the heterodyne OPLL and the WDM receivers, Quadri-correlator-type PFD, and poly phase filter for broadband I and Q signal generations. All ICs have been properly working as parts of the OPLL and WDM receiver systems.

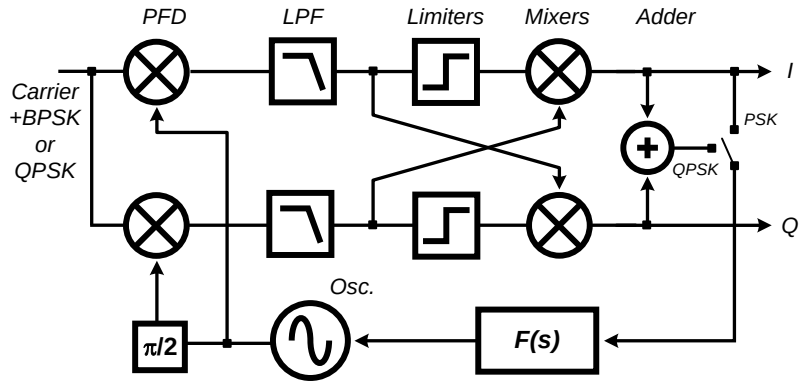
6.2 Future Works

Additional improvements and future works are described in the following subsections.

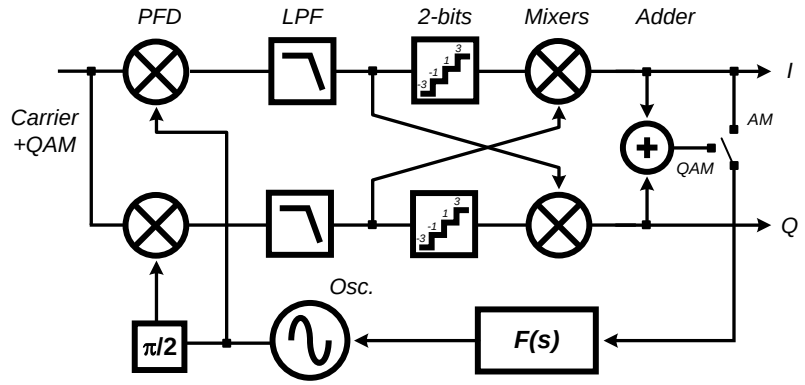
6.2.1 Modified Optical Costas Loop for Higher Bits per Symbol

Our homodyne OPLL is used as cohernet BPSK optical receiver with 1 bit per a symbol, and it performed up to 40 Gb/s data rate. By simple electrical circuit

changes, the homodyne OPLL systems can increase the symbol rates to 2 bits, 3 bits, and even 4 bits per a symbol, and therefore, more than 100 Gb/s data reception is feasible. In electrical systems, a modified Costas loop architectures were proposed [1]. Figure 6.1 (a) shows a modified Costas loop receiver architecture for QPSK modulated signals, and figure 6.1 (b) shows another modified Costas loop receiver architecture for QAM modulated signals. The receiver configurations use limiters and mixers on both $I-Q$ paths, and need an adder to have four stable QPSK lock conditions. Small changes of the electrical circuits can provide 2:1 and 4:1 higher bits per symbol rates, and data rate of >100 Gb/s is feasible using our OPLL concept which does not require a digital signal processing. These architectures can be one of the promising solutions for the short range optical communication systems which require simple configuration, high data rate, low cost, and low power consumption. DC and AC signal imbalances and phase mismatch in the PIC and EIC need to be considered for stable OPLL based receiver designs.



(a)



(b)

Figure 6.1: Concept schematics for modified Costas loops. QPSK or PSK (a) and QAM or AM (b) [1].

6.2.2 Polarization Insensitive OPLLs

Optical fields rotate and disperse in fibers because of fibers' birefringence effect, which is one of the critical challenges to use OPLLs in commercial systems. The OPLLs may lose phase locks because of the dynamically rotating optical fields. Compared to polarization mode dispersion in long haul fiber communications, a slowly rotating polarization is an issue for short-link optical fiber communications. This rotation can be compensated with simple and slowly operating analog circuits

or ADCs and DSPs with OPLLs. A polarization insensitive OPLL for a single polarized signal was introduced in [2] and a slightly modified OPLL for QPSK receivers are shown in figure 6.2. The rotating single polarized optical field is split by a polarization beam splitter (PBS) at input, and two separate optical fields by the PBS are down converted to electrical domains as $I_1(t)$, $Q_1(t)$, $I_2(t)$ and $Q_2(t)$. By summing each I and Q components, the original $I(t)$ and $Q(t)$ are dynamically restored by $I(t) = I_1(t) + I_2(t)$ and $Q(t) = Q_1(t) + Q_2(t)$. The $I(t)$ and $Q(t)$ are fed back to the laser through the EIC QPSK function and a loop filter. This polarization insensitive OPLL receiver has capability of 2-bits/symbol and 4-bits/symbol for QPSK and 16-QAM modulation formats, respectively.

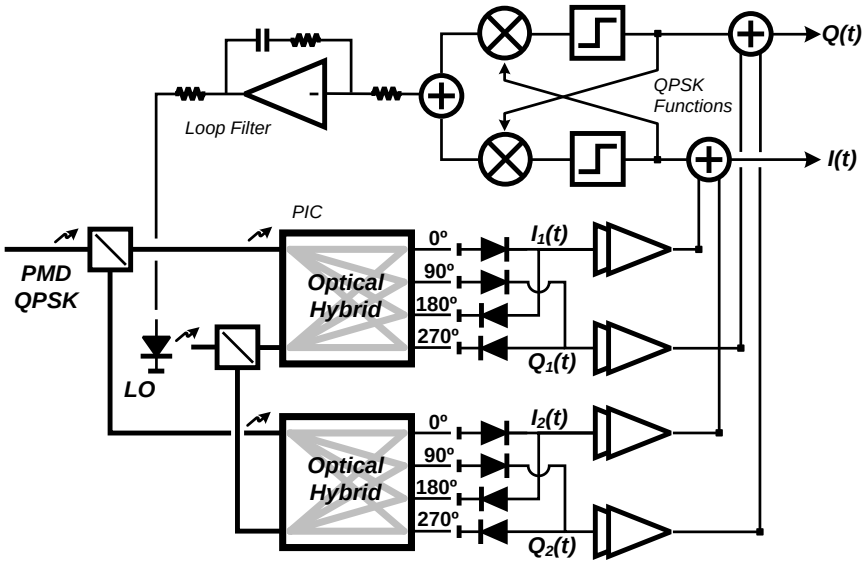


Figure 6.2: Polarization insensitive OPLL architecture for a single polarized input and a QPSK modulation format (2-bits/symbol).

For the dual polarization division multiplexing (PDM), a new polarization insensitive OPLL architecture has been proposed to double the spectral efficiency. The compensation concept has been adopted based on digital coherent detections

[3–5]. Since the polarization rotation is a slow mechanism (several MHz or 10's MHz), the polarization rotations can be compensated by low speed and low power analog/digital circuits (ADCs and DSPs) with 4:4 analog matrix with broadband variable gain amplifiers (VGAs) as shown in figure 6.3. For example, constant modulus algorithm (CMA) or least mean square (LMS) algorithm can be used for the dynamic polarization compensation. Using the CMA, four complex coefficients p_{xx}, p_{xy}, p_{yx} and P_{yy} for the 4:4 analog matrix can be derived as

$$\begin{aligned}
p_{xx} &= \int \mu(1-(I_X^2+Q_X^2))(I_X+jQ_X)(I_x+jQ_x)^* dt \\
p_{xy} &= \int \mu(1-(I_X^2+Q_X^2))(I_X+jQ_X)(I_y+jQ_y)^* dt \\
p_{yx} &= \int \mu(1-(I_Y^2+Q_Y^2))(I_Y+jQ_Y)(I_x+jQ_x)^* dt \\
p_{yy} &= \int \mu(1-(I_Y^2+Q_Y^2))(I_Y+jQ_Y)(I_y+jQ_y)^* dt,
\end{aligned} \tag{6.1}$$

where I_x+jQ_x and I_y+jQ_y are before compensations, I_X+jQ_X and I_Y+jQ_Y are after the compensations, and μ is a feedback gain factor. The complex coefficients are dynamically varying to manage the polarization rotation, and therefore, the transmitted dual-polarization I_X+jQ_X and I_Y+jQ_Y data are recovered through an EIC (QPSK receiver) and a loop filter (figure 6.3).

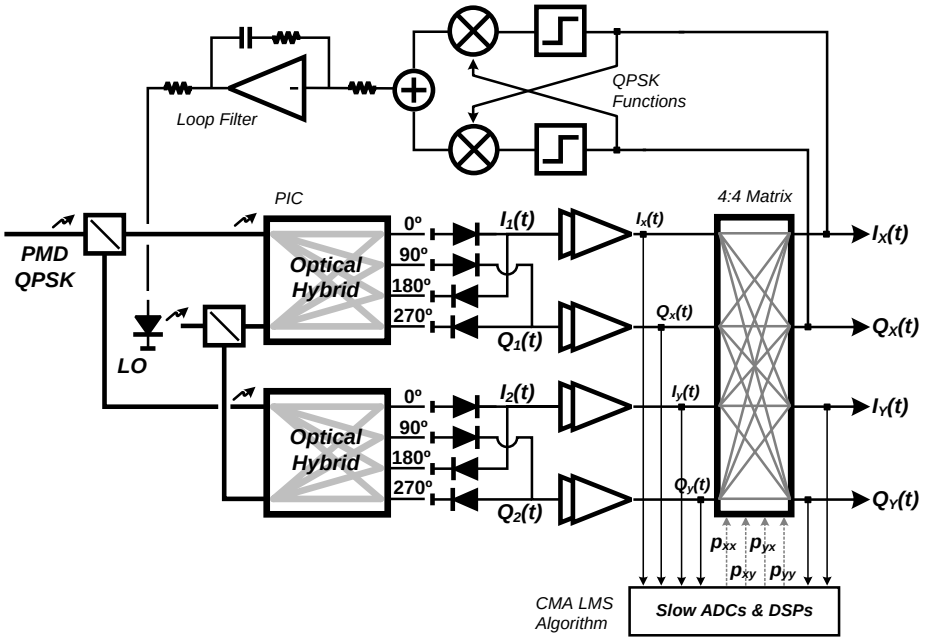


Figure 6.3: Proposed polarization insensitive OPLL architecture for dual polarized inputs and QPSK modulation formats (4-bits/symbol).

6.2.3 Silicon Based Low Power, Compact High Speed IC Designs

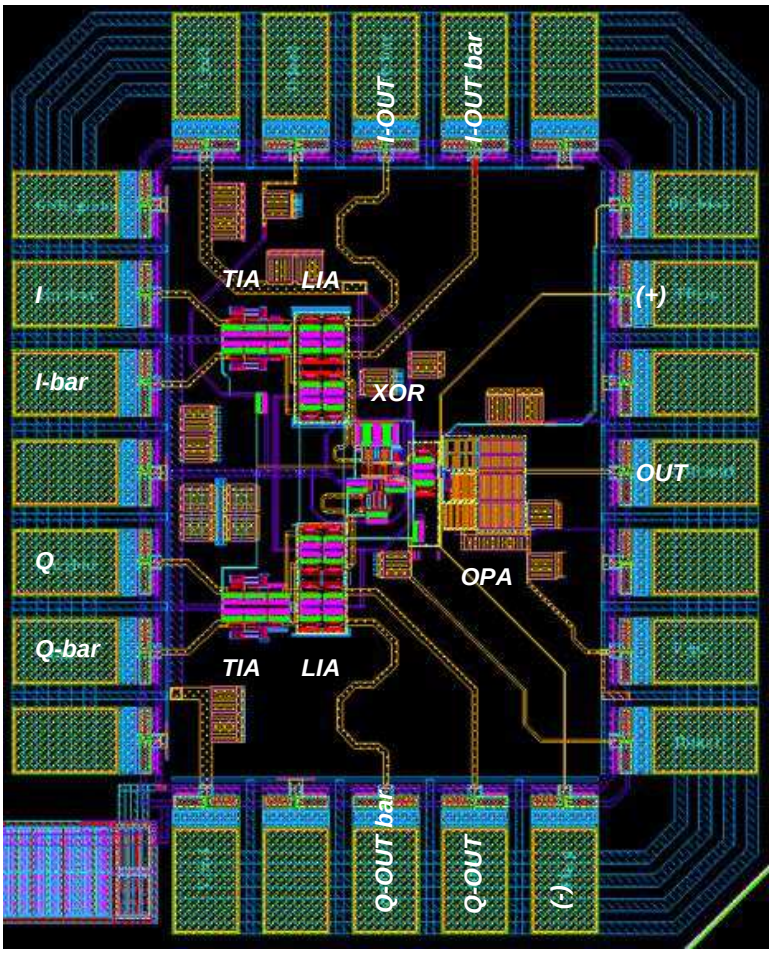


Figure 6.4: The advanced 65 nm CMOS IC designs for BPSK optical Costas loop receiver including an op-amplifier to realize more compact receivers, wider loop bandwidth, and less power consumption.

Two additional ICs have been designed using 65 nm CMOS processes which has ∼200 GHz f_τ and f_{max}. One of the IC designs is a BPSK receivers including an op-amplifier as shown in figure 6.4. The regulated Cascode structure is used

for high speed trans-impedance amplifiers (TIAs), limiting amplifiers and XOR type phase detector are applied for this designs. Conventional rail-to-rail op-amplifier has been included in this IC with the performance of >60 dB gain and 50 MHz unity gain bandwidth. The data bandwidth of BPSK 25 Gb/s has been targeted. The core IC has a chip area of 0.42 mm^2 and low DC power consumption of <0.5 W (InP HBT based BPSK receiver IC: <2.2 W). Compact and power efficient coherent optical Costas loop receiver is possible using this IC, and the loop bandwidth of more than 1 GHz with loop delay of <100 ps is feasible using the chip-to-chip integration.

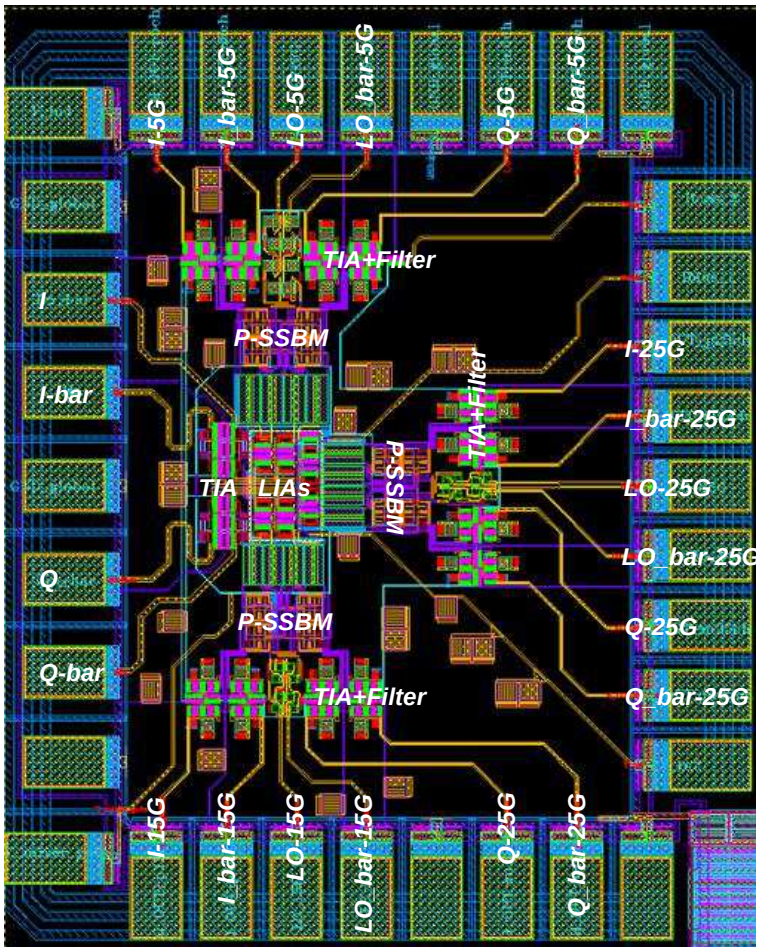


Figure 6.5: The advanced 65 nm CMOS IC designs for dense WDM receiver. 10 GHz channel spacing with 6-WDM modulated channels.

Another IC is for a dense WDM (10 GHz channel spacing) receiver and the layout is shown in figure 6.5. The regulated Cascode structure is also used as high speed trans-impedance amplifiers (TIAs), and passive type single sideband mixer with TIAs (5 GHz bandwidth) are applied for this IC designs. Total six-WDM channels are targeted in this design. The WDM receiver IC has a compact die areas of 0.72 mm^2 and it has small power consumption of >0.65 W (c.f. our previous InP HBTs design: die area of ∼5.0 mm^2 and power consumption of >20

W). The maximum data rate of 30 Gb/s for BPSK, 60 Gb/s for QPSK, and 120 Gb/s for 16-QAM are feasible in this receivers.

6.2.4 Advanced WDM Receiver Concepts

The previous proposed WDM receiver in this chapter can be improved using the proposed concepts as shown in figures 6.6 and 6.7. The first WDM receiver architecture is a modified structure using analog filter chains. This architecture can reduce the trans-impedance amplifiers' overheads such as dynamic range, bandwidth, noise contribution, and power consumption. Highest frequency channel (f_N) only passes through a capacitor C_1, the next frequency channel (f_{N-1}) comes out through L_1 and C_2, L_2 and C_3, ..., and L_{N-1} and C_N. The selected/filtered channels are amplified by narrow band trans-impedance amplifiers, and they are down-converted by each electrical LO (f_N, f_{N-1}, f_{N-2}, ..., and f_1).

More advanced version of the second architecture uses multiple high speed samplings with different delays of ϕ_1, ϕ_2, ϕ_3 ..., and ϕ_N. Then, an analog summing matrix as an analog FFTs selects and extracts the desired channels. The similar concepts have been proposed and demonstrated in the low frequency wireless communication systems as soft-defined radio (SDR) or cognitive radios (CRs), and have many advantages of impedance matching, rejection of blocker at LO harmonics and low noise contributions [6–8]. The numbers of channels, total data rate, and channel bandwidth can be determined by high frequency clocks and numbers of samplings.

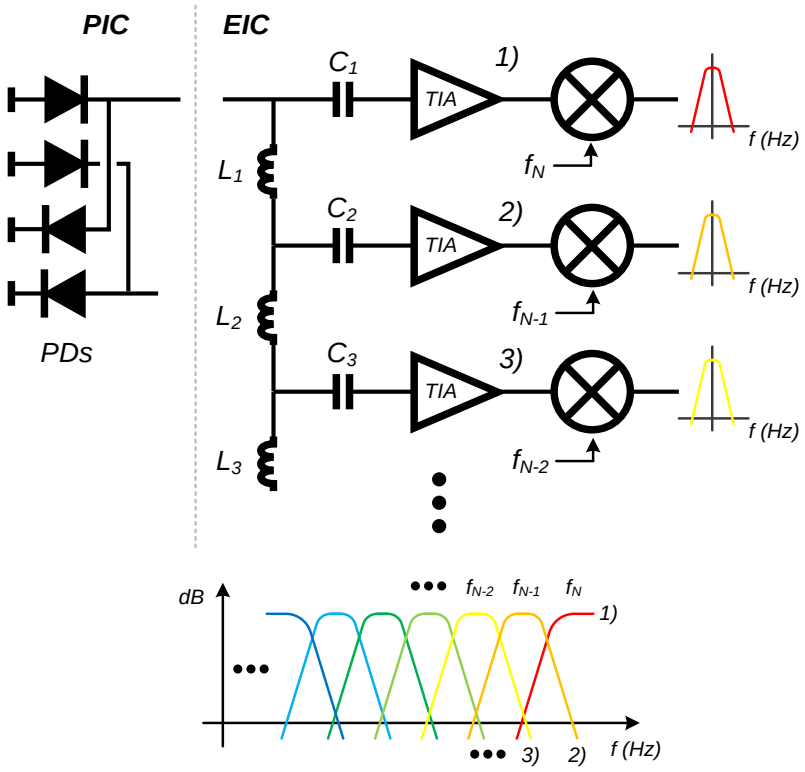


Figure 6.6: Advanced WDM receiver concept using analog filter chains.

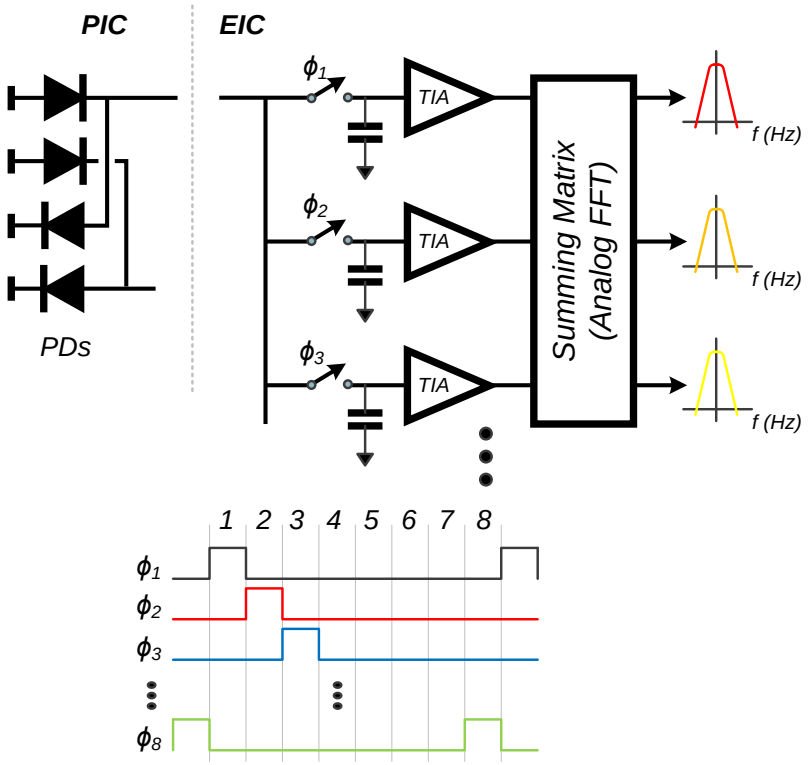


Figure 6.7: Advanced WDM receiver concept using high speed digital sampling with summing matrix and analog FFTs.

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