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Ion Beam Drift Compression Technology for NDCX Phase II
Final Report
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Prepared for:

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1. Summary

The overall objective of this STTR program (Phases I and II) was to develop and demonstrate the efficacy of the Fast Inductive Energy Corrector (FIEC) for the correction of the longitudinal energy distribution of the Neutralized Drift Compression eXperiments (NDCX) ion beam at Lawrence Berkeley National Laboratory (LBNL). The goal is to regulate the ion energy with sufficient accuracy to allow the beam to be compressed axially by a factor of 100 during neutralized drift. The Phase I effort established the basic feasibility of the Fast Inductive Energy Corrector (FIEC) by developing the preliminary design for this system. The feasibility demonstration was extended in Phase II by developing, constructing, and testing much of the FIEC system. The Phase II objectives were to: (1) the design, construct and test a Fast Agile Solid-state Modulator (FASM) to drive the FIEC with a 20 kV output voltage into a 25 Ω load in pulses that were 50 ns long with pulse rise and fall times of about 15 ns; (2) design, construct, and test the induction accelerator module for the FIEC; (3) construct and test a 10-module FASM assembly to drive the induction accelerator module; and (4) demonstrate the FIEC with the NDCX at LBNL. Tasks corresponding to objectives 1 and 2 and part of 3 were completed. The results achieved under objective 4 were limited to preliminary experiments and modeling by LBNL to optimize the utility of the FIEC concept. The equipment developed under objectives 1 - 3 was delivered to LBNL for further evaluation at the conclusion of the project.

2. Introduction

Background

The heavy ion beams produced by modest energy accelerators can be a useful tool for creating strongly coupled plasmas. To achieve the energy density required to drive a sample to the desired plasma state, these beams must be initially formed at high line-charge density and then further compressed both longitudinally and radially to near the emittance limit of the beam. The longitudinal energy distribution of the ion beam must be precisely regulated to achieve these beam compression goals. Since it is not feasible to maintain the required degree of ion energy control throughout the length of the accelerator, it will be necessary to correct the ion energy prior to the start of the final beam compression. This project focuses on the development of an advanced accelerator module to apply the required energy correction to the ion beam.

The Warm Dense Matter (WDM) regime of High Energy Density Physics (HEDP) [1,2,3] encompasses a class of plasmas with high density and pressure and moderate temperature (kT), in which the Coulomb interaction energy between plasma particles exceeds kT. This regime is rich with potential for important scientific discoveries. Many astrophysical systems (e.g., brown dwarfs, and giant planets) and inertial confinement fusion plasmas in the beginning stages of compression fall into this regime. However, these strongly coupled plasmas are difficult to study analytically or by numerical simulation and there exists a large parameter space of temperature and density where data is currently limited or non-existent.

Facilities in which WDM can be created and its properties accurately measured would provide an opportunity to improve our understanding and develop models of this regime. Numerous types of energy deposition devices are capable of producing WDM conditions at various temperatures, pressures, and sample sizes. The challenge is not how to create these conditions, but to create them so that their fundamental properties can be best studied. Towards this end, it will be important to maintain precise control and uniformity of energy deposition in the sample. It will also be critical for the WDM sample size to be large compared to diagnostic resolution volumes.

Modest energy accelerator-produced heavy ion beams offer the potential for producing large samples of very uniform WDM. Multi-stage accelerators with agile voltage waveform control can be used to precisely tailor the longitudinal energy distribution of ion beams, and therefore manipulate the energy deposition and pressure profiles in targets. Recent research in the Heavy Ion Fusion (HIF) program has defined how the use of heavy ion beams with energies just above the Bragg peak in dE/dx (ion energy loss per unit range) can maximize heavy ion deposition power density and uniformity simultaneously [4]. "Typically, ion focal spot radii of approximately 1 mm are expected, which is large enough that the beam heating can be uniform radially within a few hundred microns of the axis where local target properties can be measured" [5]. At modest energy, the ion range in solid target foils would limit the sample thickness to a few microns and would require an ion pulse length ~100 ps to limit the effects of hydrodynamic expansion during the measurements. However, thicker targets composed of low average density

foam or wire-array targets, can be 10 to 100 times thicker for the same ion range and pulse energy, with correspondingly longer hydro-expansion times. "Use of low-density foam targets would provide the opportunity to begin warm dense matter research with pulses initially as low as 1 J and then upgrade the accelerator pulse energy in steps up to about 100 J"[5].

The Heavy Ion Fusion Virtual National Laboratory (HIF-VNL) has a program underway at Lawrence Berkeley National Laboratory (LBNL) that is designed to exploit the unique capabilities of accelerator-produced heavy ion beams for driving matter into the WDM regime. This sequence of three accelerator and beam compression experiments based on induction technology, called the Neutralized Drift Compression eXperiments (NDCX series) is shown in Figure 1. This program starts by examining the underlying physics of the three critical beam manipulations; neutralized drift compression, transverse confinement, and high line-charge density injection, using existing NTX facilities in the first phase, NDCX-I. The second phase, NDCX-II, will be a unified ion beam compression and focusing experiment, but at parameters scaled from the user facility that would be constructed in NDCX-III. The work described in this SBIR/STTR project is intended to support both NDCX-I and NDCX-II. NDCX-III will be a user facility employing a high repetition rate ion accelerator, ~1 Hz, supplying compressed ion bunches to multiple experimental chambers, which will be available to researchers in a number of disciplines, for HEDP experiments.

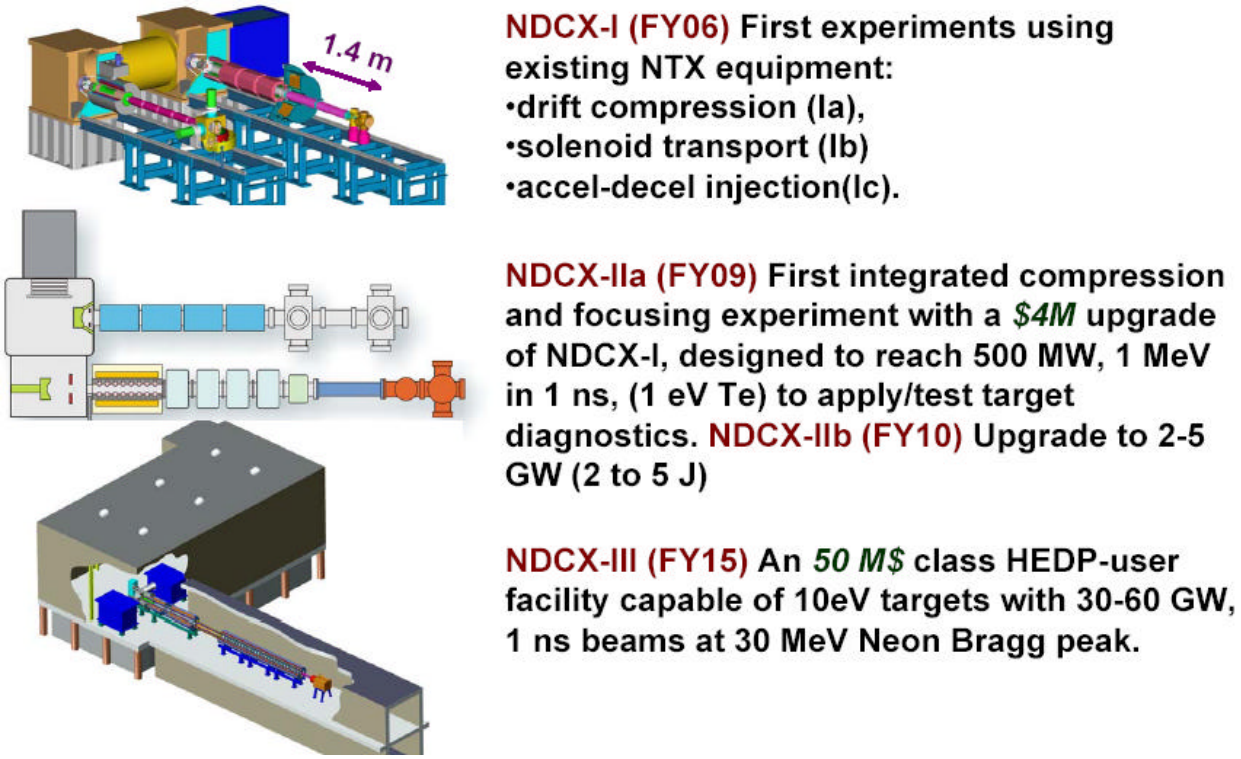


Figure 1. The NDCX sequence of neutralized drift compression experiments with increasing capability for WDM experiments that are underway at LBNL [5].

The goal of NDCX-II is to deposit ~1 J of ion beam energy in 1 ns into an ~1 mm diameter spot. Although the specific parameters of NDCX-II have not yet been finalized, pending the results of NDCX-I experiments, the general features of the system are illustrated in Figure 2. A beam of ions (He^+ is shown in the illustration, but Li^+ is now considered a preferred species), with a total current of ~1 A and a pulse length of ~1 μs, will be formed and accelerated to a nominal energy just above the peak of the Bragg curve (2.44 MeV for Li^+). During acceleration, the addition of energy tilt (increasing the energy of the tail of the beam more than the beam head) will cause the beam to bunch. In combination with the increased ion velocity, the beam duration will be reduced to 100 ns. Solenoidal focusing will be used to maintain transverse confinement of the beam during injection and acceleration. The beam will then be neutralized and allowed to drift, during which time the energy tilt will cause the pulse length to contract to 1 ns. A final focus will radially compress the beam to 1 mm.

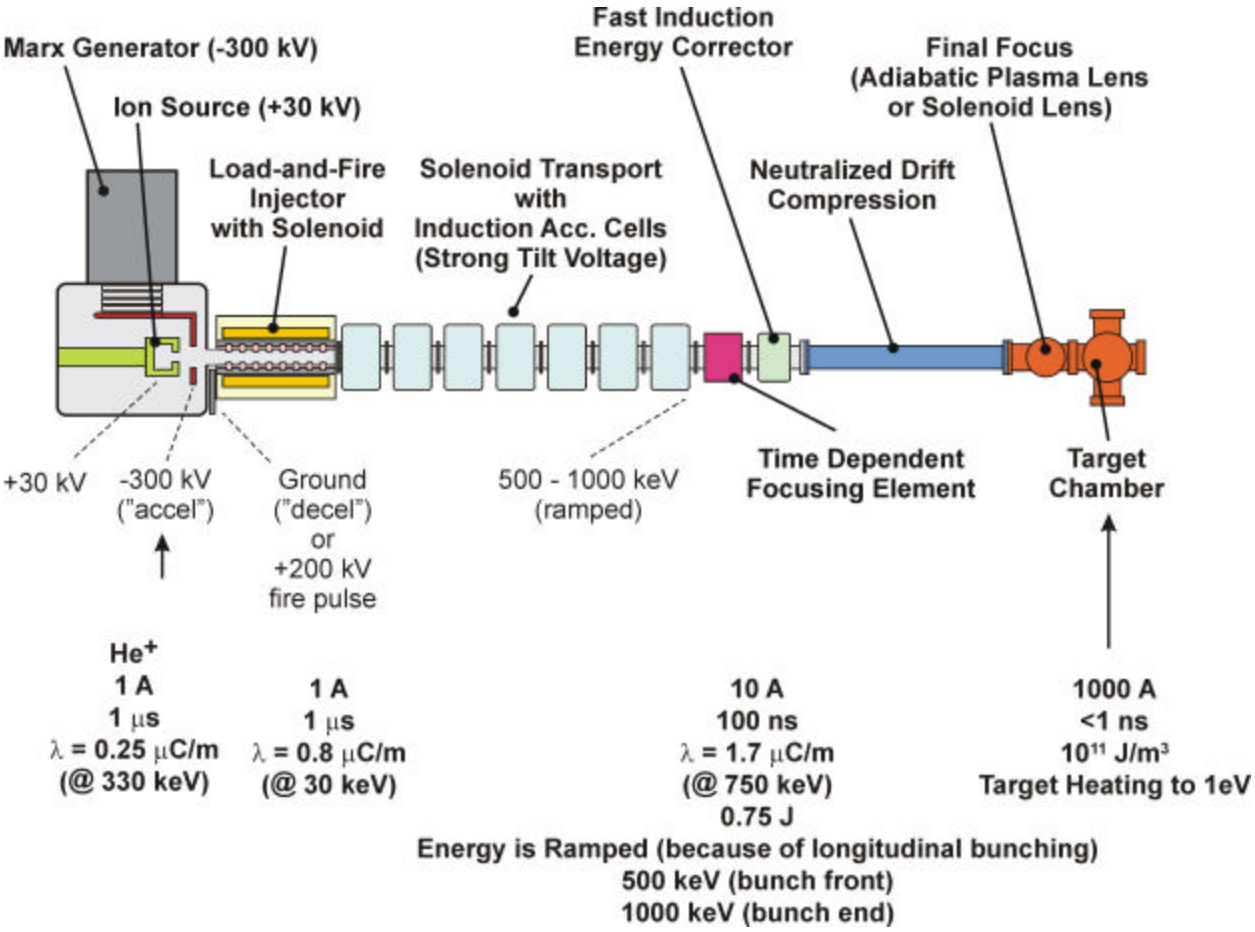


Figure 2. Illustration of the NDCX-II (courtesy of Matthaeus Leitner, LBNL).

With the neutralization of the space-charge forces, the longitudinal compression of the beam is controlled by the distribution of ion axial energy. The ideal ion energy distribution as a function of time, *E(t)*, is given by:

$$E(t) = E_o \left[\frac{1 - \frac{h}{2}}{1 - \left(\frac{h}{1 + 0.5h} \right) \left(\frac{t}{t_p} \right)} \right]^2$$

where, E_o is the energy at the center of the beam, t_p is the total beam length, and h is the total velocity tilt (the difference between the tail and head velocity divided by the beam center velocity). This ideal distribution would produce infinite compression, the beam would be reduced axially to a point, barring coupling from transverse emittance. More realistically, the beam compression limits will be dominated by the beam emittance and field errors in the transverse and longitudinal compression forces.

Of particular concern are acceleration field errors that will cause the longitudinal energy distribution to deviate from the ideal form given by the above equation. Several sources for these errors will exist in the NDCX. These include errors in acceleration voltage waveforms, timing errors, and coupling of transverse emittance into longitudinal emittance.

A certain amount of error in the energy distribution can be tolerated. Expressed as momentum spread, $\delta p/p$, the maximum allowable error for 100X compression is $|\delta p/p| < 1\%$ [7]. However, to allow for unanticipated beam perturbations during the neutralized drift, it should be reduced to less than this value prior to the start of drift compression. A value of $|\delta p/p| < 0.5\%$ is reasonable, this corresponds to an energy error, $|\delta E/E| < 1\%$. Note that this error is evaluated relative to the ideal at a specific point in the beam. With velocity tilt in the beam for compression, the beam head energy is less than the tail energy; therefore, a smaller absolute energy error can be tolerated in the beam head than tail.

As an example, consider the NDCX-II point design; Li^+, E_{ave}= 2.44 MeV, $|E_{tilt}/E_{ave}| \leq 20\%$. The ideal energy at the beam head is 1.95 MeV and at the tail it is 2.93 MeV. Hence, the energy errors should be kept to less than ±19.5 keV at the head and ±29.3 keV at the tail.

Technical Approach

It should be possible to prevent errors in the longitudinal energy distribution by carefully regulating each manipulation of the ion beam from formation to the entrance to the drift compression region. However, the NDCX program has adopted an alternative approach that will provide the same regulation of the final beam energy at a lower cost.

Certain classes of errors that will affect the beam energy are random in nature, e.g. timing jitter. Random errors occurring repeatedly, for example passing the beam through several acceleration modules, will cancel on average. Therefore, the maximum error in the longitudinal beam energy distribution due to random errors will be, on average, smaller at the entrance to the neutralized drift compression region than at the individual acceleration modules at which the errors occurred.

In general, the cost to reduce energy errors, i.e. reduce timing jitter or improve accelerator voltage waveform regulation, scales inversely with the magnitude of the error at a rate much faster than linear. For example, the cost to reduce an error by 1%, from 2% to 1%, will almost certainly be much higher than to reduce it a by 1%, from 10% to 9%.

In recognition of the foregoing, the approach that LBNL has adopted for NDCX is to apply modest regulation to each acceleration waveform and accumulate errors in the beam energy along the length of the accelerator. Then just upstream from the neutralized drift compression region, apply an energy correction to cancel the residual errors that were induced during acceleration of the beam. By maintaining modest energy regulation in the preceding acceleration stages, the maximum error that must be offset by this energy correction can be kept to a minimum. This will minimize the cost for the energy correction system. By applying the highly regulated correction at a single location, the cost of all other modulators can be minimized as well.

The Fast Inductive Energy Corrector (FIEC) is being developed under this project to apply the required energy correction to the NDCX ion beam. The FIEC is based on an induction accelerator topology. This allows the correction waveform voltage to be superimposed on the beam energy, adding or subtracting the exact energy of the correction, regardless of the initial beam energy.

To correct the errors in the NDCX beam, the FIEC must fulfill four requirements; the maximum energy must exceed the maximum energy error in the beam, the energy resolution must be better than the maximum allowable energy error in the NDCX beam, the "bandwidth" must be sufficiently high to allow the correction to accurately reproduce the time dependent error, and the correction waveform must be agile so that it can be changed to match changes in the errors of the NDCX beam when experiment parameters are altered.

The maximum energy error that must be corrected in the NDCX beam is not precisely known. However, a reasonable estimate can be made. The maximum beam energy for the Li^+ point design for NDCX-II, 2.93 MeV, might practically be achieved in six acceleration stages of ~0.5 MeV each. It is realistic to expect each acceleration stage to maintain ±10% accuracy, ±50 keV. Allowing that some of the energy errors may be additive between stages, the FIEC should be able to correct a somewhat larger error, ±100 keV is a reasonable value.

To achieve effective compression of the beam, the energy errors should be reduced to $|\delta E/E| < 1\%$. Inserting the values for the Li^+ point design for the NDCX-II suggests that the FIEC must be able to regulate ion energy errors to less than ±19.5 keV. Therefore, the energy resolution of the FIEC should be better than this, ±10 keV is a practical value.

The energy errors that accumulate on the beam are characterized not only by voltage, but also by their time-dependence. Clearly, the correction applied by the FIEC must be able to slew in voltage to approximate this time dependence. The beam will be 1 μs initially and reduced to 100 ns at the FIEC through a combination of increased average velocity and compression. Thus, the time dependence of the accelerating voltages, and their errors, can be characterized by times in the range of 10's to 100's of ns. It can be concluded that the FIEC correction voltage should be

able to slew substantially on ns time scales to effectively correct potential energy errors in the NDCX beam, ~10 kV/ns should be effective.

The time dependence of the ion energy errors in the NDCX beam will not be known until the time dependent beam energy is measured. Further, it is anticipated that the time dependent energy errors will vary with changes in the system parameters. Therefore, the FIEC must possess the waveform agility to generate a wide range of time dependent energy corrections. The FIEC must approximate a high voltage arbitrary waveform generator that can be programmed to create a precisely controlled, complex waveform at the output that can be applied to correct the beam energy distribution.

During Phase I of this STTR an approach to meet the foregoing requirements was identified by FPSI. This system consists of an induction acceleration module that contains ten independent primary assemblies each of which is powered by an advanced solid-state pulse modulator. The modulators employ a FPSI patented technology. The preliminary design for the induction acceleration module and the pulse modulators was completed in Phase I of this STTR project. This provided the foundation for development and demonstration of the technology in Phase II.

Project Objectives

The overall objective of the Phase I and II projects was to develop and demonstrate the efficacy of the Fast Inductive Energy Corrector (FIEC) for the correction of the longitudinal energy distribution of the Neutralized Drift Compression eXperiments (NDCX) ion beam. The goal is to regulate the ion energy with sufficient accuracy to allow the beam to be compressed axially by a factor of 100 during neutralized drift. The Phase I effort established the basic feasibility of the Fast Inductive Energy Corrector (FIEC) by developing the preliminary design for this system. The goal of the Phase II project was to complete the demonstration of this technology by constructing the FIEC and testing it on the NDCX at LBNL. The specific technical objectives of the Phase II were to:

1. Design, construct and test the Fast Agile Solid-state Modulator (FASM). The goal of this objective is to develop the advanced pulse modulator that will be used in the FIEC on the NDCX. The goal parameters for this device are; 20 kV output voltage, 15 ns voltage rise and fall times, and an agile programmable pulse width ranging from 15 ns to 50 ns (fwhm), into a 25 Ω load. The preliminary design for this modulator was developed under the Phase I effort.

2. Design, construct and test the FIEC induction acceleration module for the NDCX. The goal of this objective is to develop an induction acceleration module that can regulate the longitudinal energy distribution of the NDCX ion beam with sufficient accuracy to achieve 100X axial drift compression. The performance target for this device is to apply an optimally shaped correction waveform within the energy range of ±100 kV during the 100 ns duration of the beam. The preliminary design for this induction module was developed under the Phase I effort.

3. Construct and test the FASMs for the FIEC. The goal of this objective is to produce the agile waveform control modulators that will power the FIEC induction module. The preliminary FIEC design, developed under the Phase I effort, requires 10 modulators.

4. Demonstrate the FIEC on the NDCX. The goal of this objective is to use the FIEC to regulate the longitudinal energy distribution of the NDCX ion beam. The objective is to experimentally demonstrate the regulation of the NDCX ion beam longitudinal energy distribution to the accuracy required to reduce the axial length of the beam by 100X during neutralized drift compression.

3. Task 1 - Design, Construct and Test the FASM

The basic schematic circuit diagram for the FASM is shown in Figure 3. It is formed from 20 series modules; each module generates a 1 kV output that is controlled by a 1200 V MOSFET. A single-turn transformer on each module joins the modules. The transformer secondary, referred to as the stalk due to the physical arrangement, of each module is joined in series with the next to produce the 20 kV output. There are 12 parallel switch elements in each module to provide the required current capability, 20kV/25Ω = 800 A.

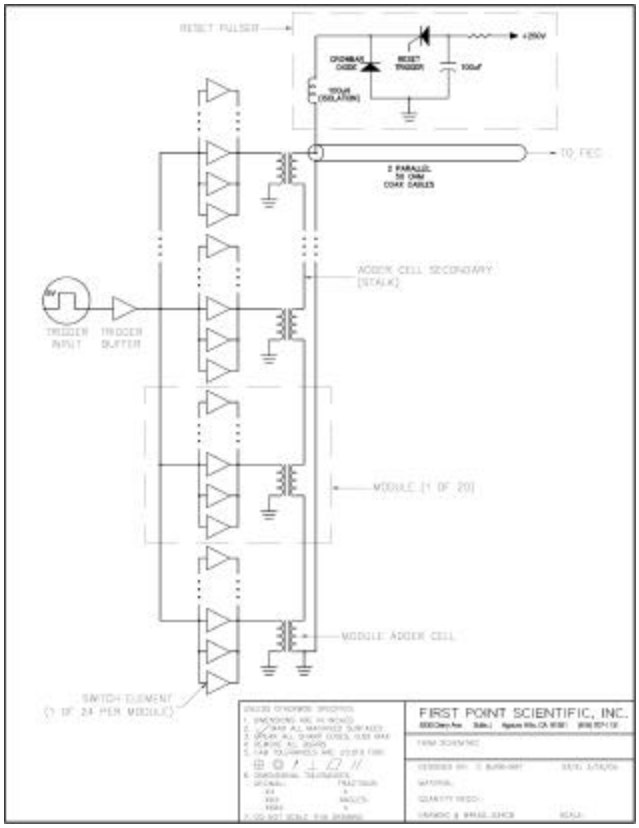


Figure 3. The schematic diagram of the FASM.

The steps in the development of the FASM design consisted of:

Basic Modulator Development and Testing

A preliminary design for the FET driver circuit for the modulator board was developed and bench tested. The circuit employed 12, 1.2 kV power MOSFETs from Advanced Power Technologies as the power switches. A fiber optic circuit for triggering the board was developed and bench tested. Based on the results from these tests a prototype modulator PC board with 12 FETs was designed. This board was intended to test the FET driver and trigger circuits and employed a resistive load instead of a ferrite core for simplicity.

Three prototype boards were fabricated by Sierra Proto Express. The boards were stuffed by J.P. Systems. In order to facilitate testing, the 12 power MOSFETS were initially omitted. These components were added individually during testing. The completed board with all MOSFETS installed is shown in Figure 4.

The boards were tested using the setup shown in Figure 5. A trigger pulse was generated by an Agilent 33250A waveform generator, and was coupled fiber-optically to the test board. The output waveforms were measured using a Tektronix TDS220 digital storage oscilloscope and downloaded to a laptop computer over an RS232 interface for analysis.

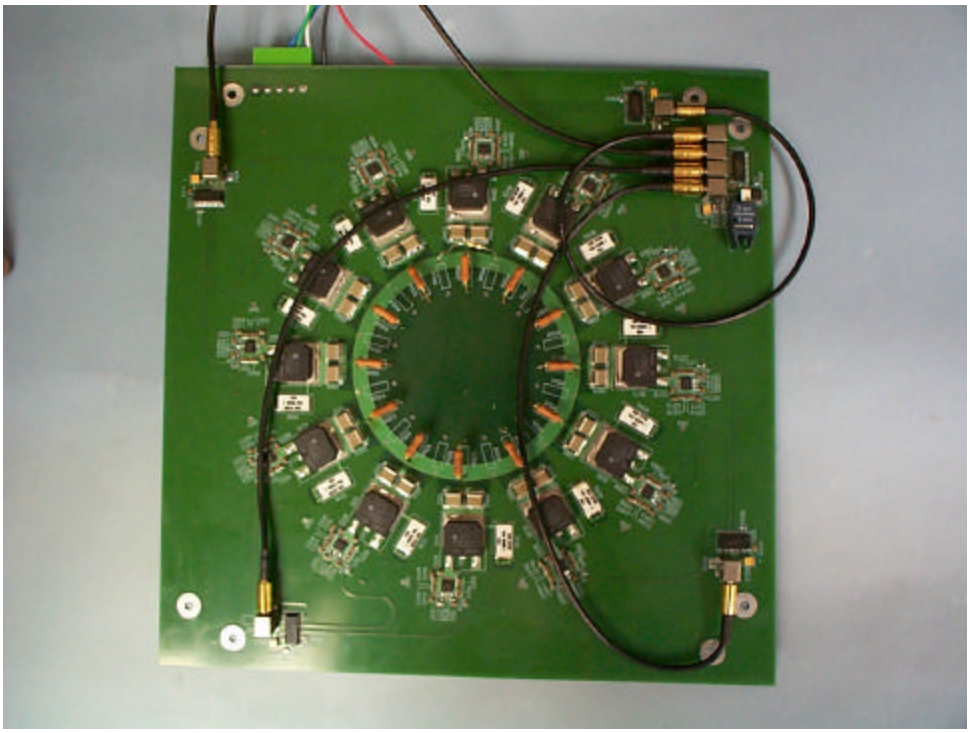


Figure 4. Completed FIEC prototype modulator board with all MOSFETs installed.

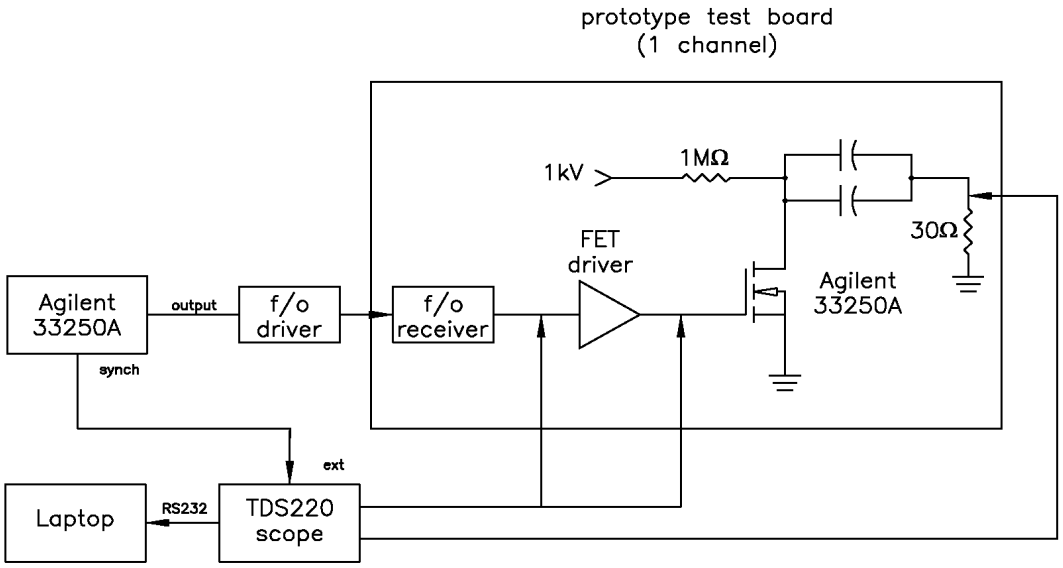


Figure 5. Layout for the testing of the FIEC prototype modulator board.

Typical input and output waveforms for the driver are shown in Figure 6. The input trigger is shown in Figure 6(a) and the input to the FET driver is shown in Figure 6(b). The ~22 ns delay between these pulses is caused by the fiber optic coupling circuit. Figure 6 (c) shows the output from the FET driver without a FET connected. This component is biased for bipolar operation between –15V and +20V to improve the FET switching characteristics. The ~30 ns delay is due to the switch on time of the driver. The rise time of the FET driver output is ~4 ns (10% to 90%) without a load.

Figures 6(d) and (e) show the output from an APT 1201R4SFLL power FET driven by the output shown in (c). The rise time from Fig 6(d), which was measured using a 100x Tektronix scope probe) is 8.4 ns (10 to 90%), while the rise time in Fig. 6(e) (which was measured using a 1000x Tektronix scope probe) is 10.1 ns. The fall times are 15.7 and 17.0 ns (10 to 90%), respectively. Once all the output FETs were connected, the rise and fall times improved significantly as shown in Figure 7. In this case the rise time was reduced to 5.0 ns and the fall time to 5.5 ns.

Timing measurements were made to determine jitter in the system. Two types of timing errors were investigated: (1) shot to shot jitter (one channel) and (2) timing discrepancies between channels. Figures 8(a) and (b) show histograms of the trigger times for the first 12 channels. The data in 8(a) were measured at the input to the FET driver and the data in (b) were taken at the output (no load). The centroids and standard deviations for these data are plotted in Figures 9(a) and (b) respectively. The shot to shot jitter for any given channel is roughly the same for all channels, ~75 to 85 ps, both at the input and the output of the FET drivers. For the input signals, channel-to-channel variances are roughly of the order of the single channel jitter. However, for the output, variations are much larger (~1 ns) presumably reflecting chip-to-chip variations introduced during manufacturing.

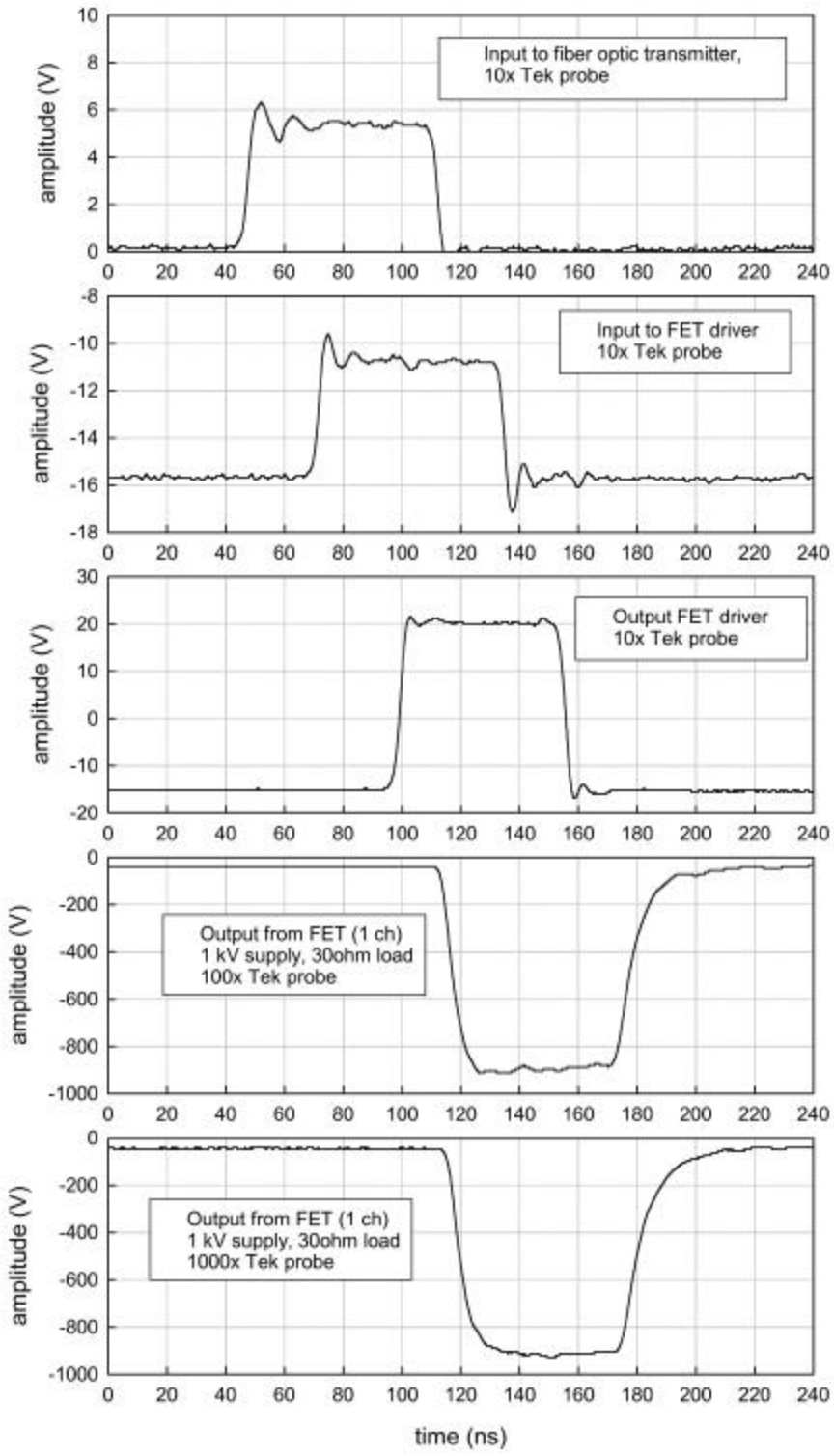


Figure 6. Waveform timing. (a) Input to the fiber optic driver; (b) input to the FET driver on the prototype board; (c) output from the FET driver (no FET connected); (d) circuit output into 30 ohms with 1 kV supply, measured using a 100x Tektronix probe; (e) circuit output measured using a 1000x Tektronix probe.

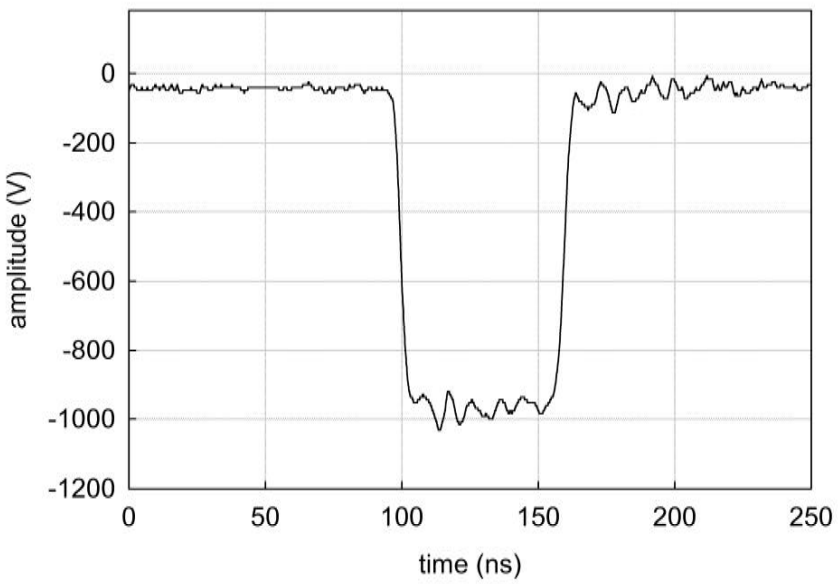
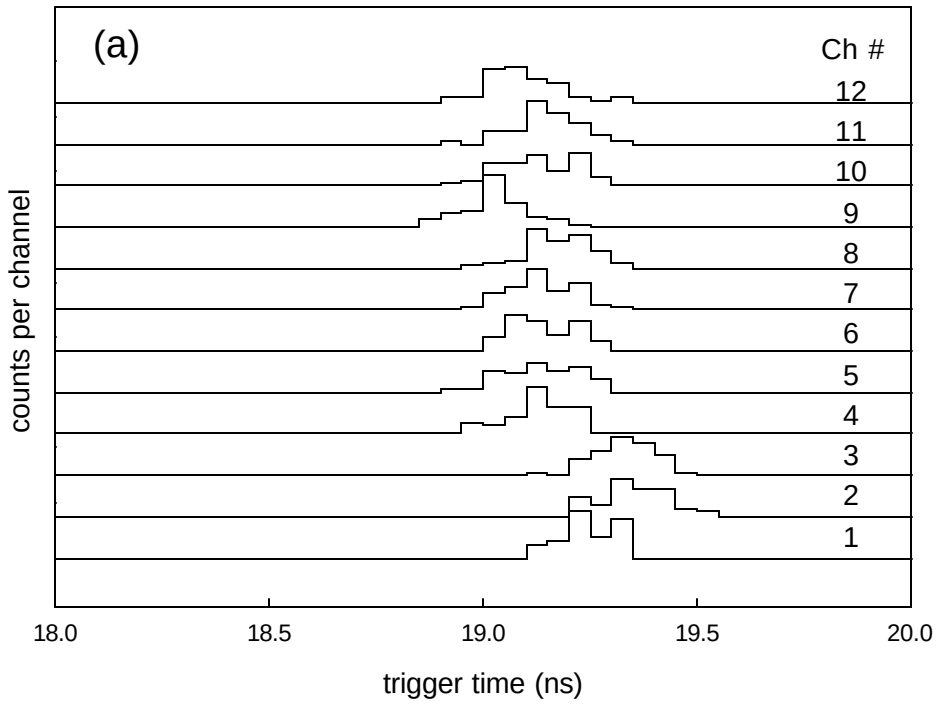


Figure 7. High voltage output waveform with 12 output FETS connected.

The measured rise and fall times are well within the 15 ns design specification. The arrival times of the trigger pulses at the FET drivers are well within the specified 0.5 ns dispersion window. However, there appears to be a chip-to-chip variation of ~1 ns in the switch-on time of the IXDN404 FET driver. If each FET and its driver were mounted on a separate daughter board, it should be possible to correct for this delay by characterizing it during testing, and mounting daughter boards with similar delays on the same motherboard. The relative offset for each motherboard can be compensated for either in the fiber optic driver, or adjusting the reference voltage to the comparator in the fiber optic receiver on each motherboard. This reference voltage is provided by a trimpot; tests with the current test board show that several nanoseconds of timing adjustment can be obtained in this way. Based on these considerations, redesign to incorporate the daughter board concept was undertaken.

In conclusion, the basic circuit for the FIEC modulator board has been successfully tested. Rise and fall times for the high voltage output pulse are significantly better than specifications. Timing jitter is estimated to be around 1 ns which is somewhat larger than the specified value of 0.5 ns. This will lead to an increase in rise and fall times of around 1 ns. However, the measured rise and fall times are significantly less than the specified values. Also, consideration of switch-on delays resulted in redesign to mount each MOSFET and its driver on a separate daughter board. This design also has the advantage that failed components can be easily replaced.



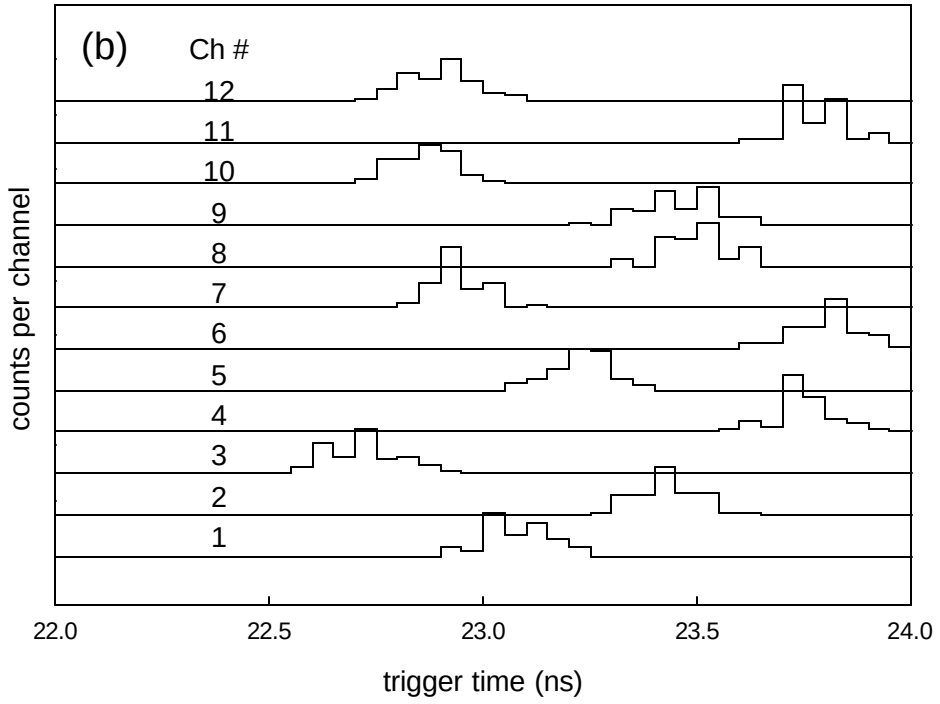


Figure 8. Histograms of trigger times for the first 12 channels at (a) the input to the FET driver, and (b) the output of the FET driver.

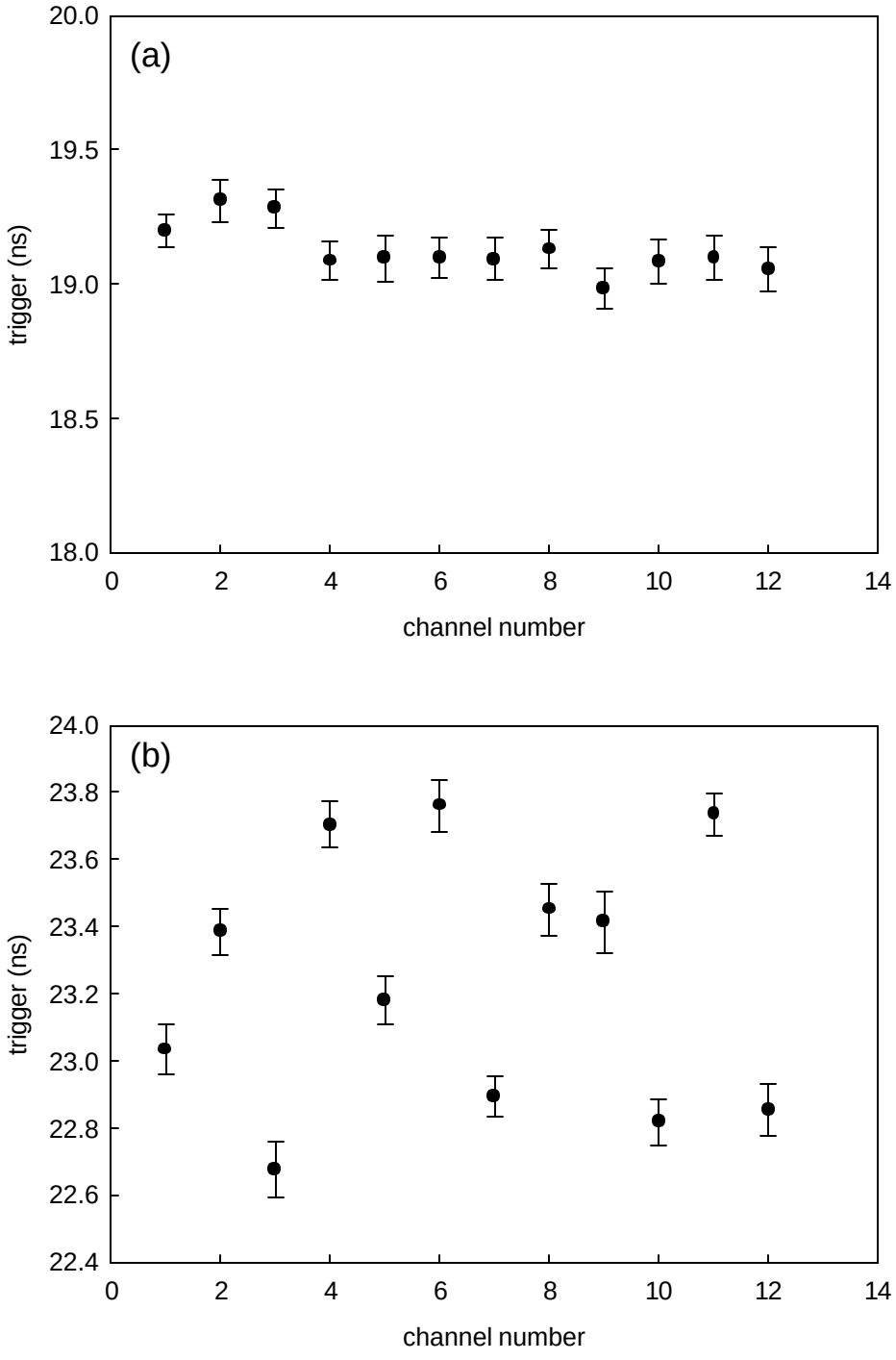


Figure 9. Centroid and standard deviation data from Figure 8.

Selection of the Ferrite Core Material for the Modulator Mother Boards

Isostatically pressed and fired CN20 (a NiZn Ferrite) from Ceramic Magnetics was chosen for use in the FASMs because of its favorable mechanical and electrical properties, as well as cost factors. FPSI considered various options for fabricating the primary transformer winding, a single turn winding encircling the core. The most attractive approach involved copper plating the cores on three sides.

The technique for attachment of the ferrite cores to the motherboard was developed in which they were directly soldered to the motherboard. In order to test this approach, 5 cores were copper plated to a thickness of 0.003". A custom heater that clamps the core to the board has been developed. Solder paste was applied before mounting the ferrite. The only problem that was encountered during the tests was delamination of the copper plating on the inner surface of the core. This will be avoided by increasing the plating thickness to 0.010" on this surface.

Each ferrite core requires a copper-plated jacket with a gap on one face. A technique for producing the required pattern by masking the cores prior to plating was developed in collaboration with ArtCraft Plating in Burbank, CA.

Each modulator consists of 20 boards with one ferrite core per board. These boards are assembled by stacking them in series. Each core must be electrically connected to the adjacent board. Previous FPSI designs have made these connections using a planar contact assembly that required considerable force to assemble the entire stack of boards. For the current design, a simpler and more robust solution was developed in which each board has a ring-shaped spring assembly made of a standard beryllium-copper finger stock from Bal Seal. A simple jig was designed to permit the finger stock to be soldered to each board in a simple and quick procedure while maintaining the required tolerances. This spring fits over the ferrite core of the adjacent board so that no axial force is required to hold the assembled boards in place.

Design and Testing of the Mother Board/daughter Board Concept

As discussed in A, based on the experience with the first prototype board, the decision was made to redesign the board on a modular basis. For this modular design, each FET together with its driver is mounted on a separate daughter board. The daughter boards are plugged into a motherboard on which the Ferrite core is mounted, together with the timing distribution circuit. This approach facilitates achievement of better pulse shapes, simplified assembly and troubleshooting, and will permit faulty components to be readily replaced. The design of the daughter board was completed (Figure 10), together with a small test board to verify operation of the new board (Figure 11).

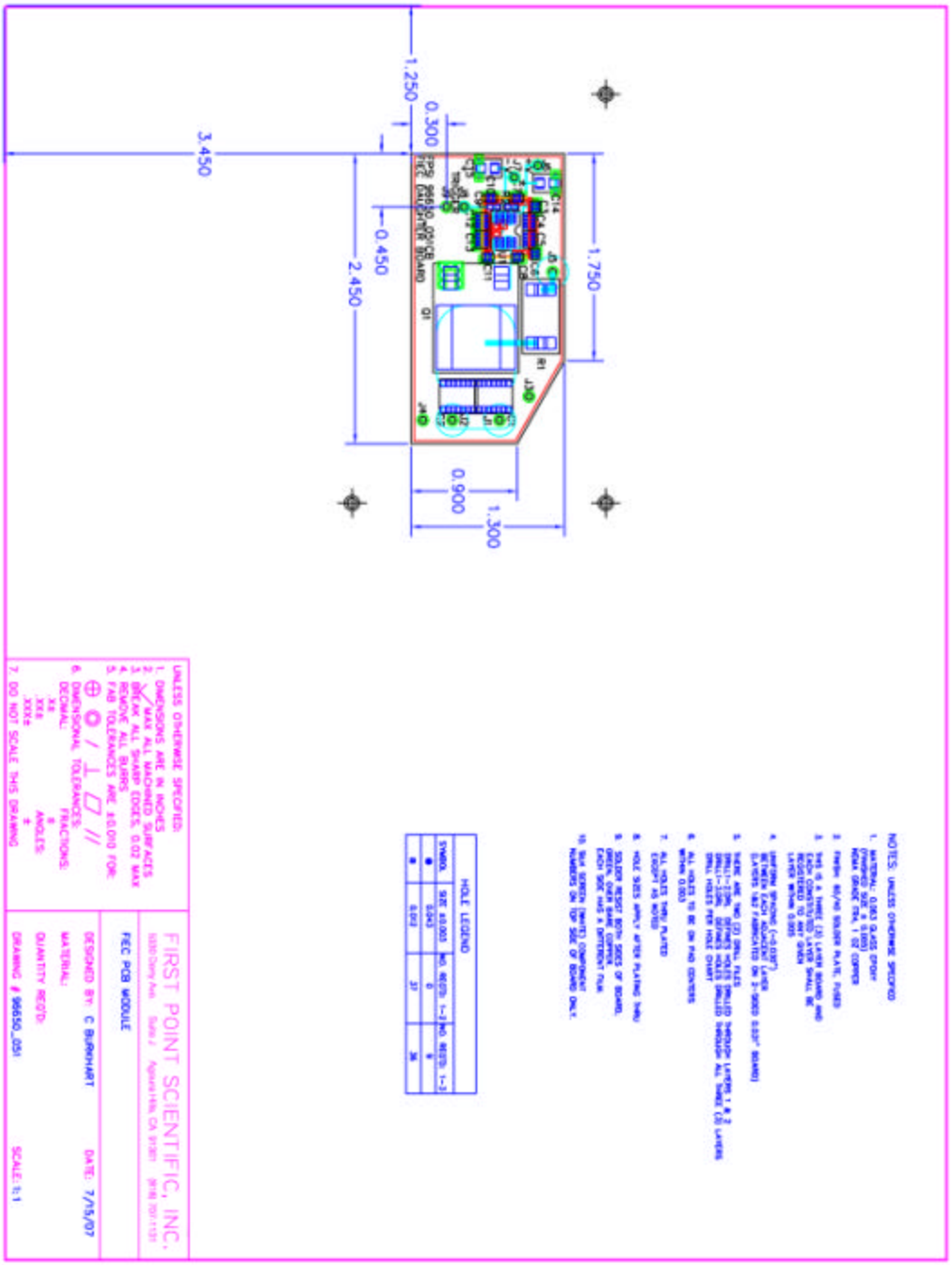


Figure 10. Design of the daughter board.

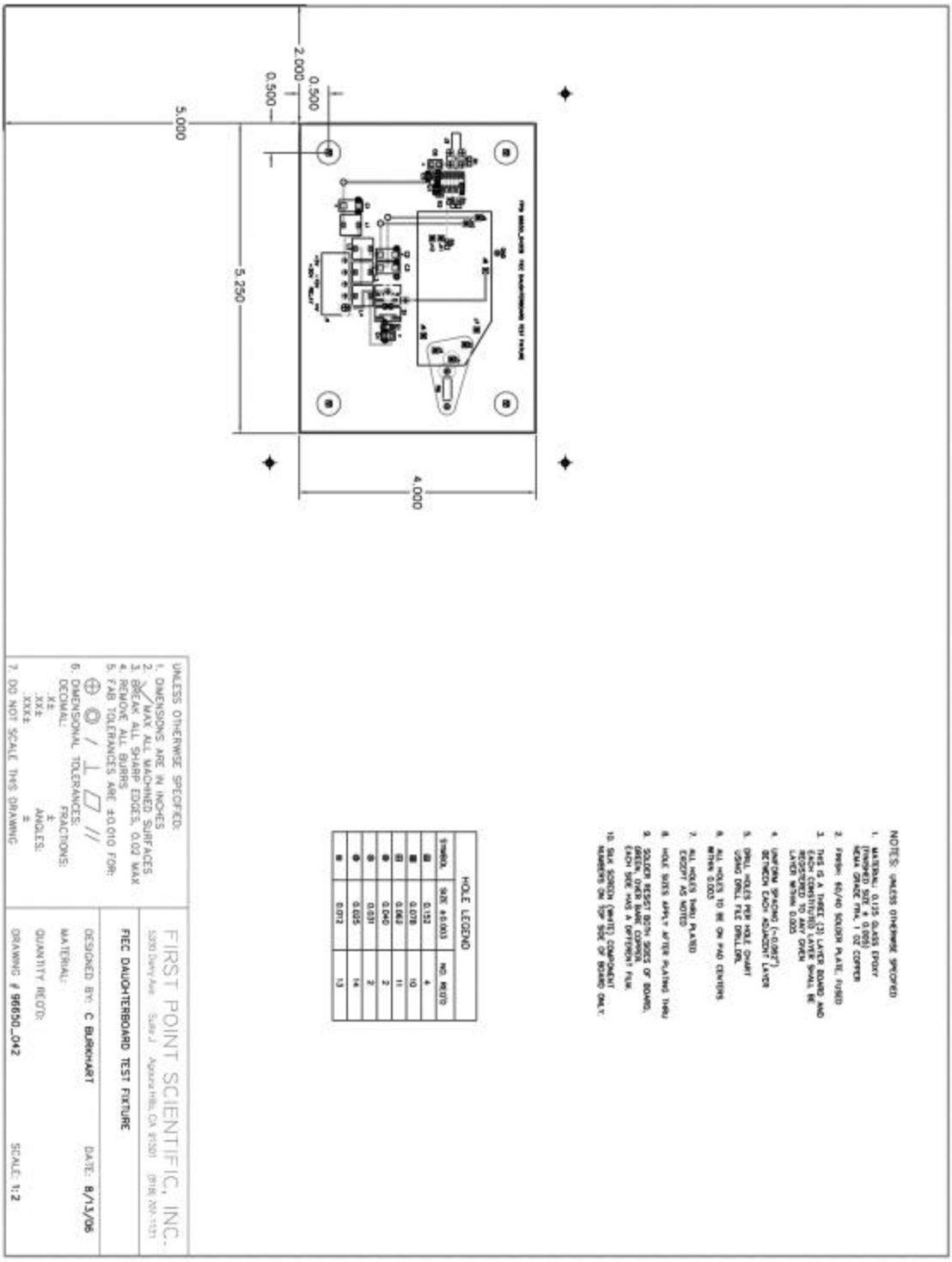


Figure 11. Test board.

Figure 12 shows the completed daughter board, and Figure 13 shows the daughter board mounted on the test board.

Figure 12. Detailed view of the daughter board.

Figure 13. Test board with daughter board in place.

Pulse testing was carried out using the setup shown in Figure 14. Input pulses were generated by a HP 33250A arbitrary waveform generator operated as a pulse generator. Pulses of 0 to 5 volts with a pulse width of 50 ns and a rise time of less than 5 ns were fed to the input of the daughter board mounted on the test board. The output of the daughter board was detected by a 100x high voltage probe and recorded on a Tektronix TDS 210 digital storage oscilloscope triggered on the waveform generator. A typical output waveform is shown in Figure 15. From this figure, it can be seen that the rise and fall times are less than 8 ns (10 to 90%), which are well within the required specifications. Further improvements are likely once the daughter boards are mounted in parallel on the motherboard.

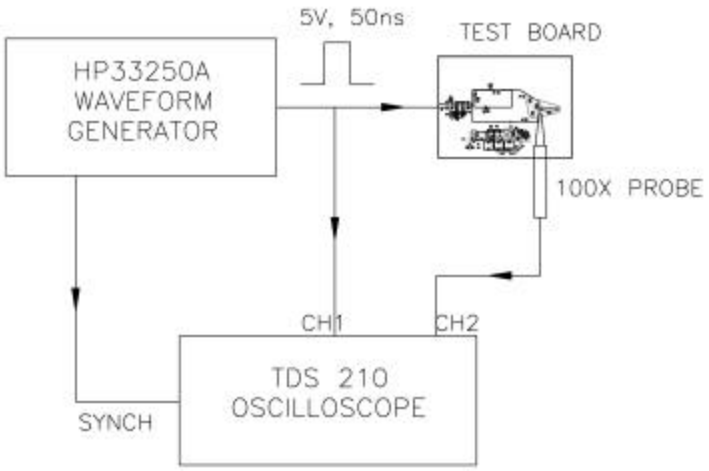


Figure 14. Test circuit for the daughter board.

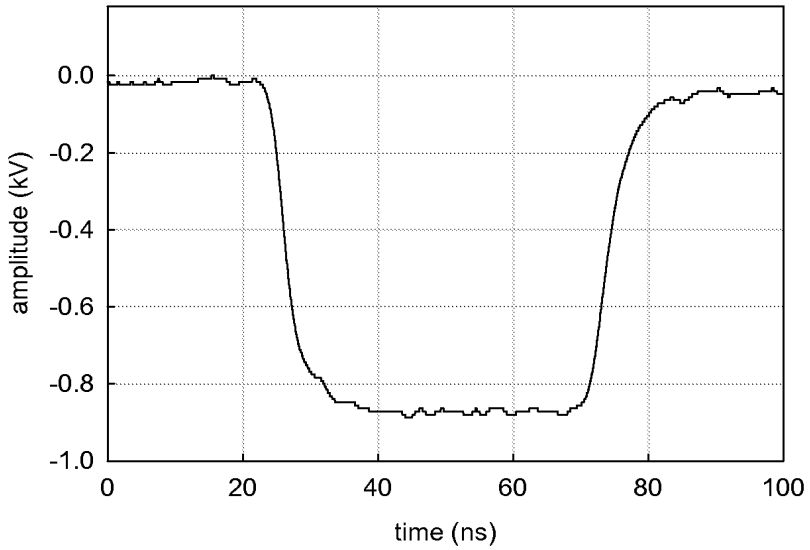


Figure 15. Typical output waveform from the daughter board showing rise and fall times of <8 ns.

In addition to pulse shape measurements, the board-to-board jitter was also measured for the 4 boards that were fabricated. A typical set of timing histograms is shown in Figure 16 for each of the 4 daughter boards. This figure shown that the shot to shot jitter for each board is less than 400 ps, while the board-to-board scatter contributes an additional 200ps. These figures are well with the required specifications.

Based on these results, the efficacy of the daughter board/mother board was demonstrated.

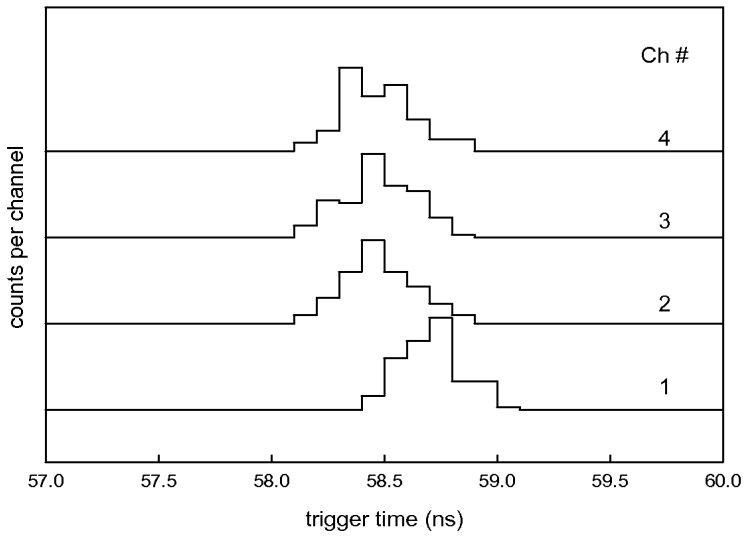


Figure 16. Timing histograms for the 4 daughter boards tested.

The print for the mother boards is shown in Figure 17.

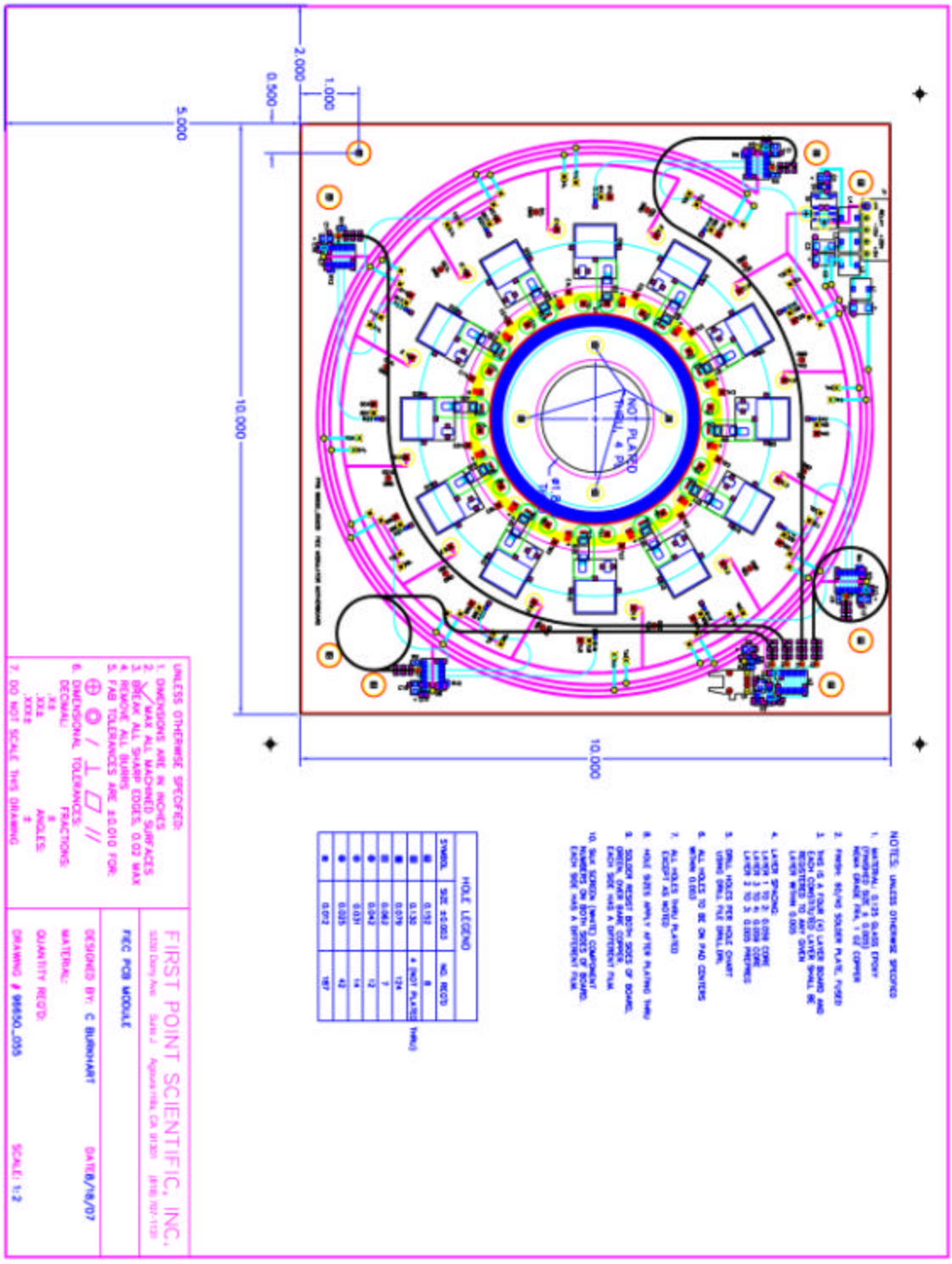


Figure 17. Mother board.

Following finalization of modulator mother board and daughter board designs, construction of the first FASM was undertaken. The first batch of boards (25 motherboards and 260 daughter boards) were fabricated by Sierra Proto, and stuffed by JP Systems. Figures 18 and 19 show a completed mother board with 12 daughter boards attached. Testing of the board was then performed.

The assembly design for the FASM is shown in Figure 20. The 20 modulator boards are mounted on an aluminum base plate. The assembly is enclosed in an aluminum batch can that provides a sealed environment within which an atmosphere of sulfur hexafluoride is maintained. All electrical, gas and fiber optic connections are made through the base plate so that the cover can be easily removed for servicing the assembly.

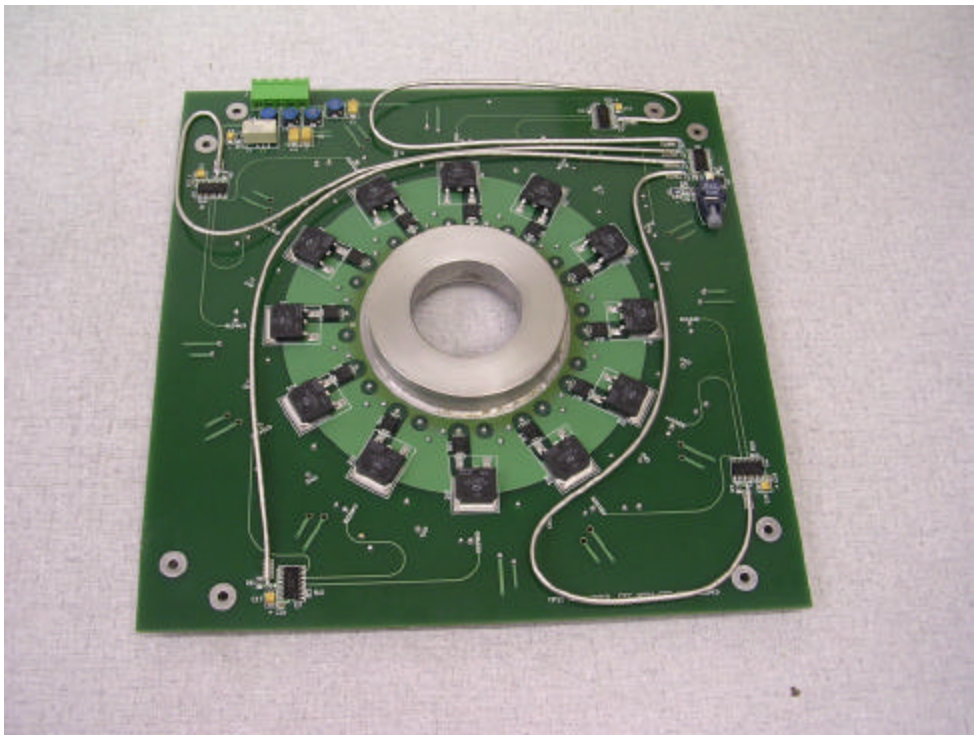


Figure 18. Completed modulator board. Lower side showing ferrite in center and semirigid coax cables for signal distribution.

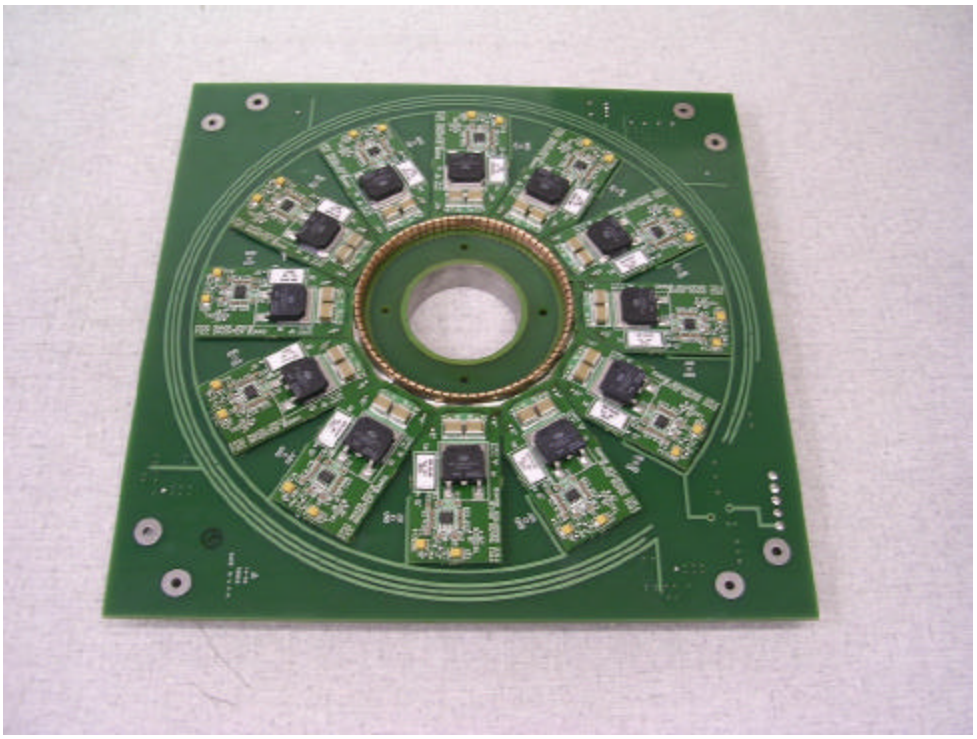


Figure 19. Completed modulator board. Upper side showing the 12 daughter boards, each mounting one FET, and the fingerstock ring used to connect to the adjacent board.

Figure 20. FASM assembly drawing.

Figure 21 shows the test setup for single boards. The output load consisted of twelve 30 ohm Caddock resistors connected in parallel to form and effective 2.5 ohm load resistor. The output was measured across the load resistor or across the FET output using a x100 high voltage Tektronix probe. The input waveform was produced by a HP33250A waveform generator and was optically coupled to the motherboard.

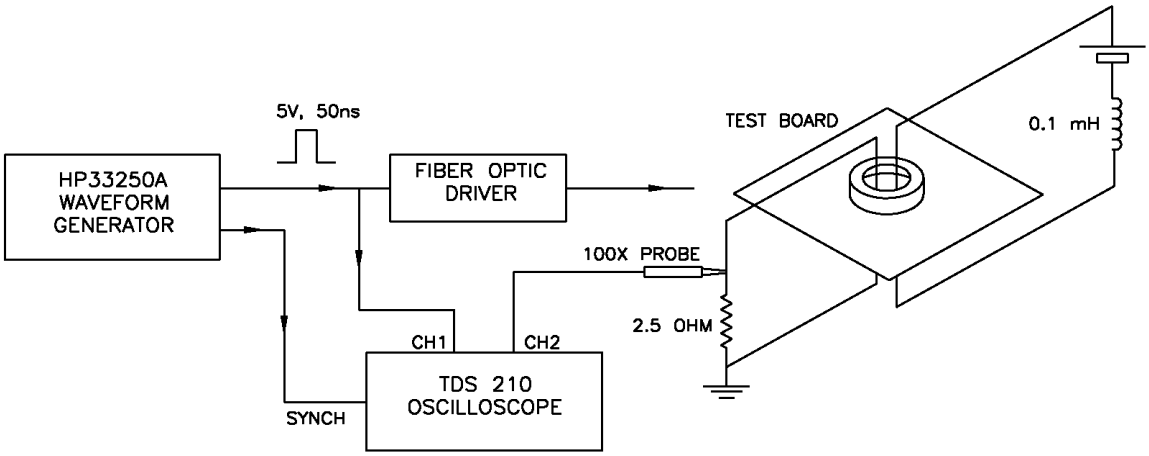


Figure 21. Schematic for testing single boards for the FIEC modulator

Figure 22(a) shows typical output waveforms (FET output) for various values of input voltage. As can be seen from these waveforms, there is significant ringing on the trailing edge of the pulse waveform as the FET supply voltage is increased due to increasing core saturation. For supply voltages above 850V, FET failure occurs reproducibly. The inclusion of a snubber circuit on the FET output was not able to mitigate this problem. This was resolved by implementing a simple DC reset, as shown in Fig. 21. This consisted of an additional circuit to drive a DC current through the secondary in series with a 100μH inductance. The resulting output waveform for a supply voltage of 1000V (as measured at the load) is shown in Fig. 22(b). FET supply voltages up to 1100 V were tested without a single FET failure.

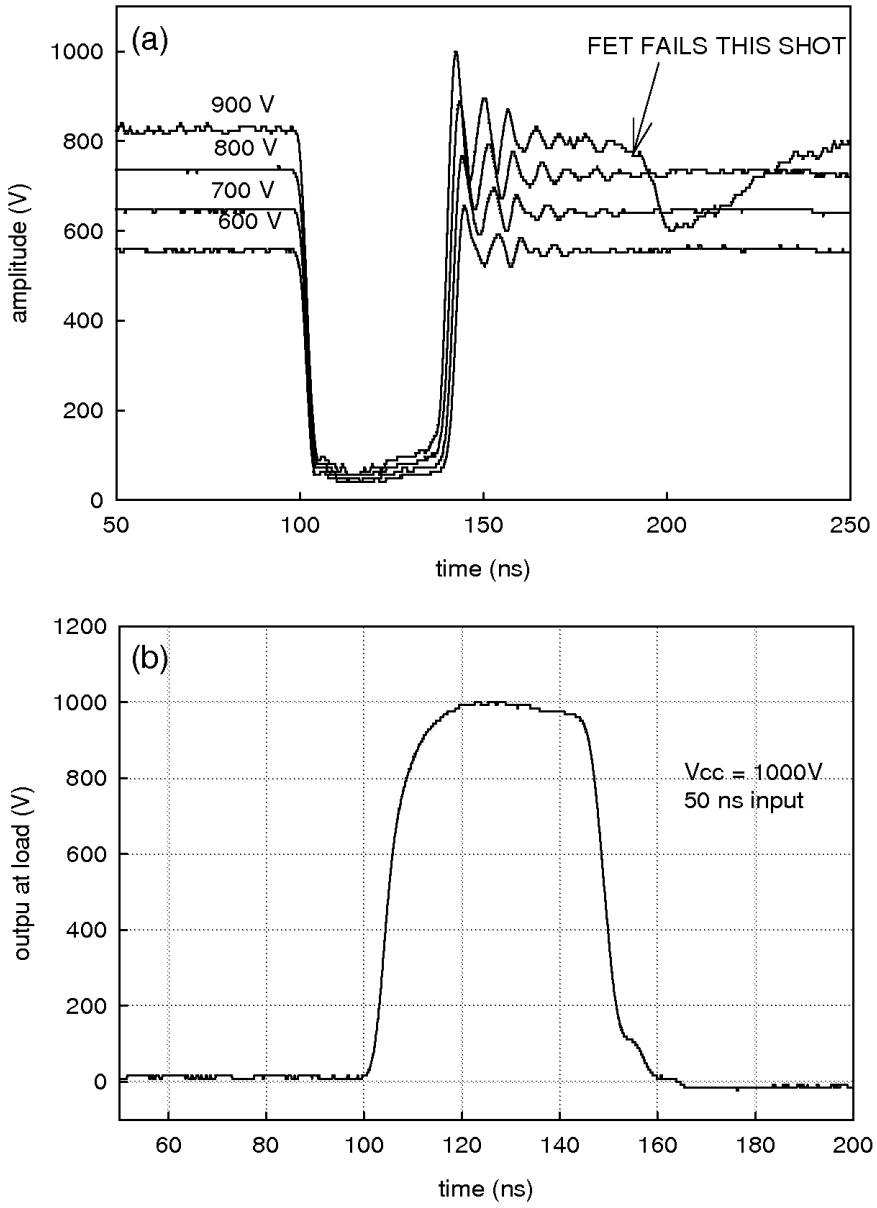


Figure 22. (a) Output waveforms without core reset as measured at the FET output for various values of FET supply voltage showing ringing on the trailing edge of the pulse. (b) Output waveform with reset as measured at the load with DC reset of 8A.

Assembly and Testing of the FASM

Construction of the first modulator has been completed. Figure 23 shows the completed stack of 20 motherboards mounted on the base plate. Figure 24 shows the shows the complete modulator together with the enclosure for containing the sulfur hexafluoride insulating gas.

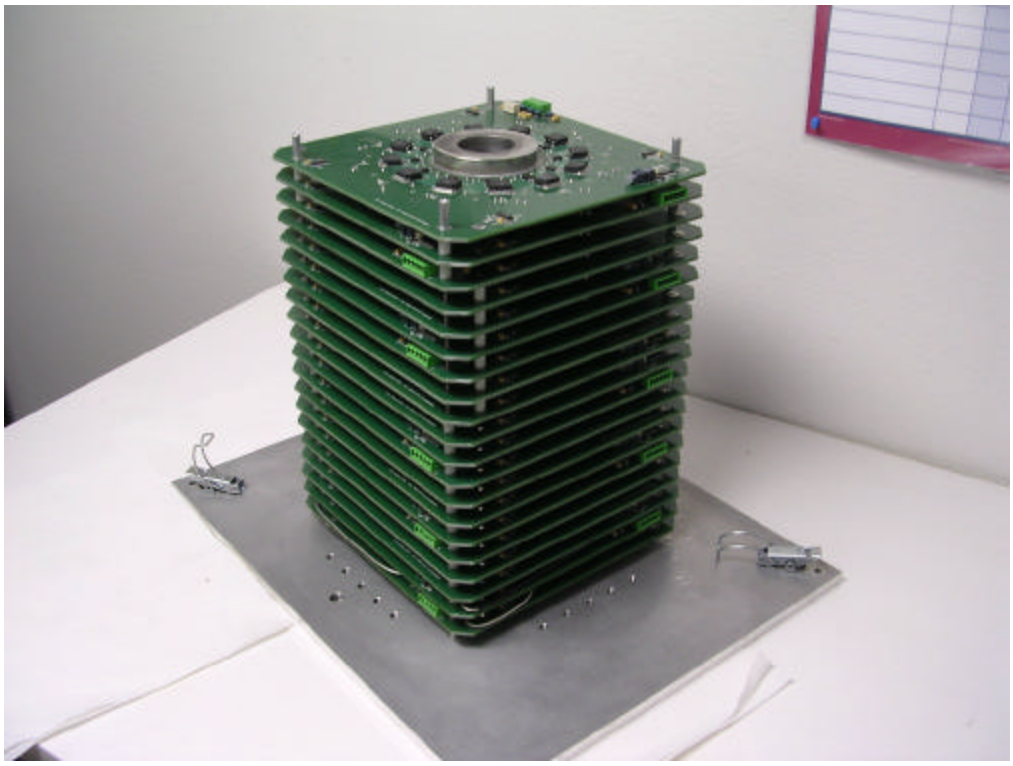


Figure 23. Assemble board stack for the first FASM.

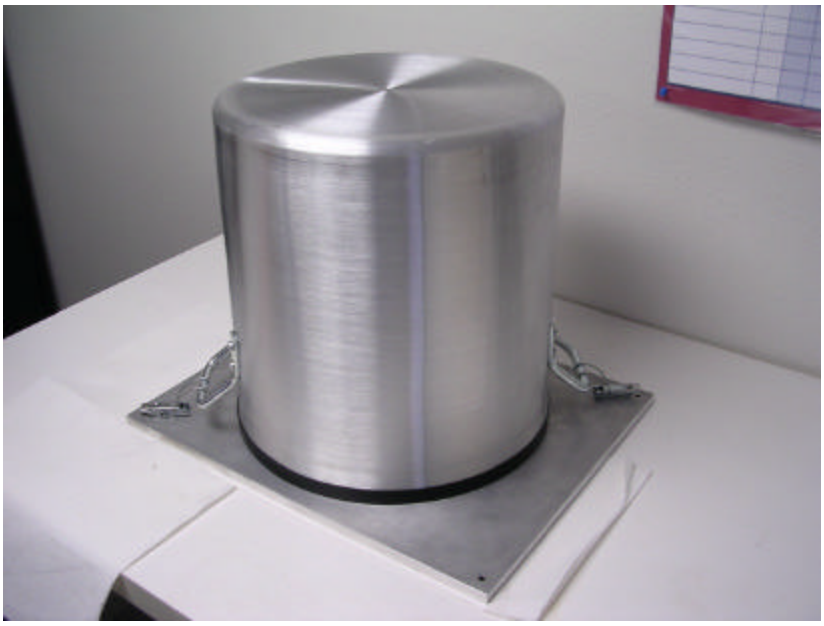


Figure 24. modulator with enclosure for sulfur hexafluoride insulating atmosphere.

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Tests of the assembled stack were performed using the setup shown in Fig. 25. This is essentially the same configuration as shown in Fig. 22 except that the load resistance was increased to 50 ohm. To limit risk of damage to the FETs prior to delivery to the customer, the

system was not tested at full voltage and only limited tests using reset were performed. Preliminary tests were conducted with 10 boards with FET supply voltages up to 500V (i.e. 50% of the design voltage). Subsequent tests were performed with all 20 boards with FET supply voltages up to 300V.

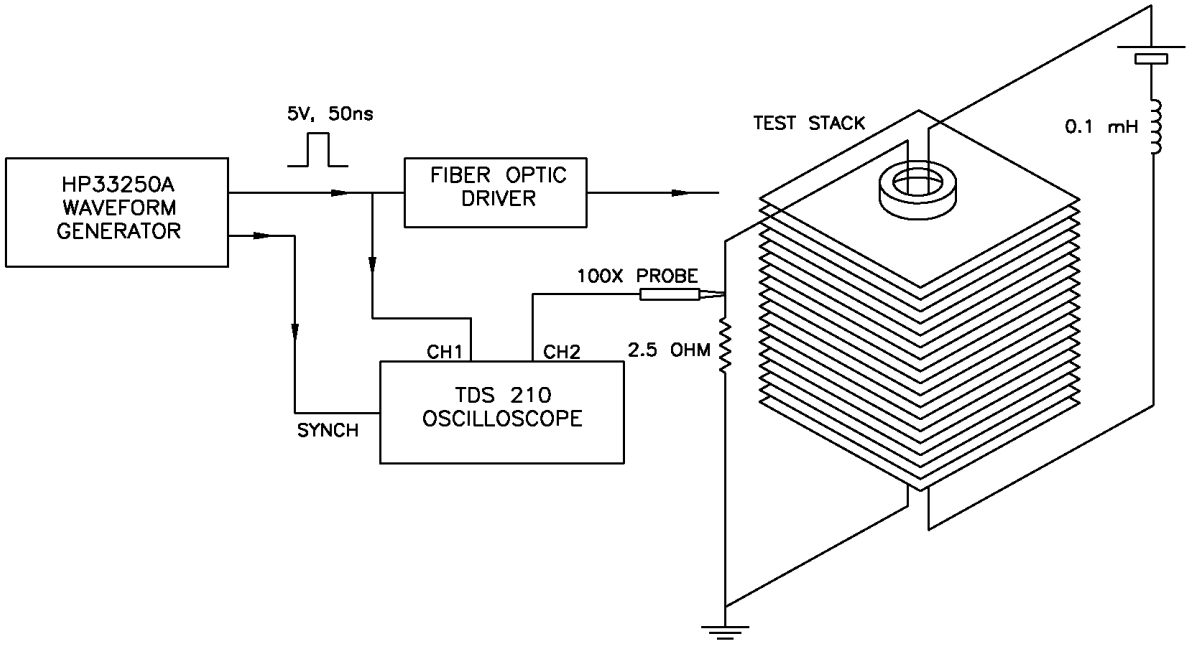

Figure 25. Test setup for the full stack of 20 modulator boards.

For output voltages up to 2 kV, the Tektronix 100x probe was used to measure the output. For voltages above this, a HP 1000x probe was used. Some problems were experienced with the 1000x probe. The output waveforms showed significant transients and the waveforms were found to be strongly dependent on placement of the leads. For this reason the waveforms measured using the 1000x probe are considered to be of less value in accurately representing the shape of the waveform, although the amplitude is likely to be correct. Figure 26(a) shows typical output waveforms, as measured at the load

For operation at higher voltages, the 1000x probe was used. Typical waveforms for FET supply voltages up to 300V are shown in Fig 26(b). The data show rise and fall times of 5 to 6ns which is well with the required specification.

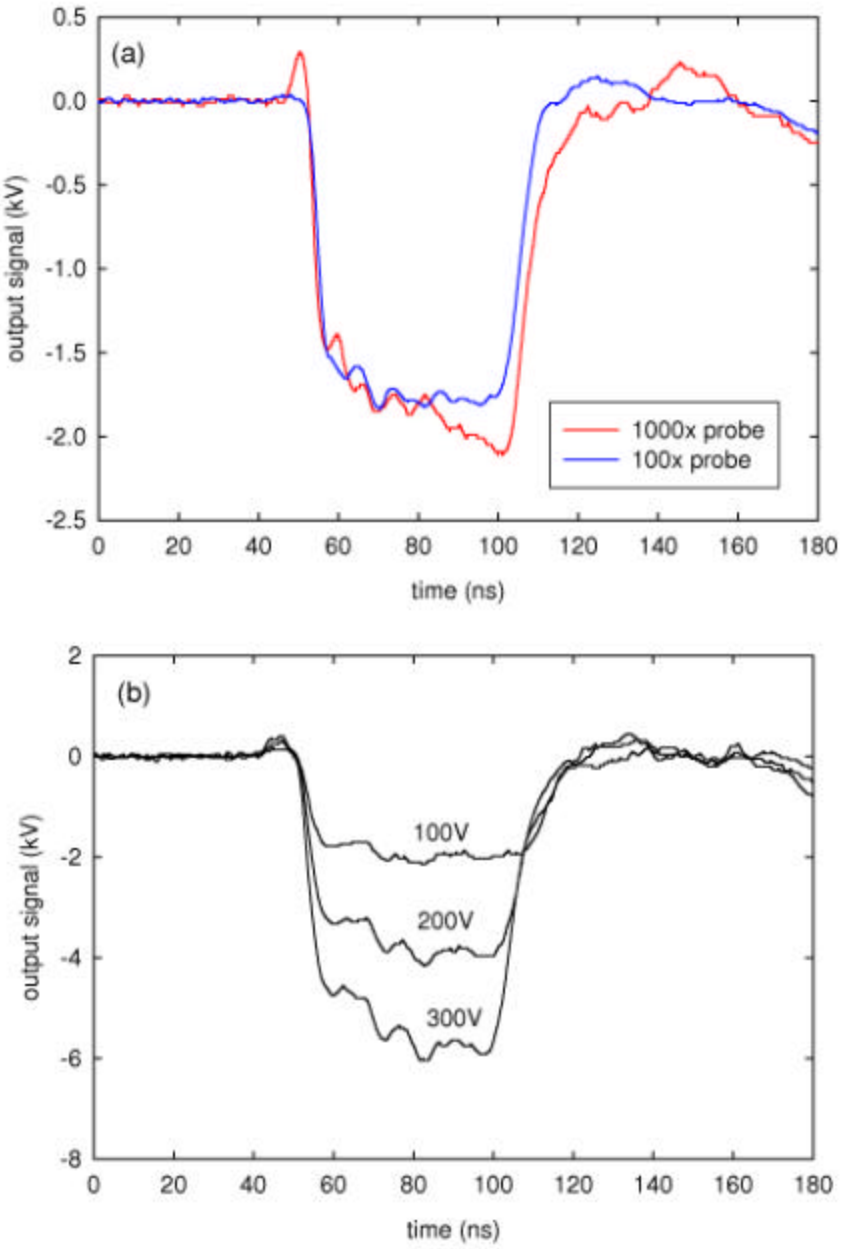

Figure 26. Output waveforms for the full stack of 20 modulator boards (a) output waveforms for a FET supply voltage of 100 V as measured using two different oscilloscope probes. (b) output waveforms for three values of FET supply voltage measured using the 1000x probe.

4. Task 2 - Design, Construct and Test the FIEC Induction Acceleration Module

Design Discussion

The layout drawing of the FIEC induction acceleration module is shown in Figure 27. An inductive adder approach has been employed, which incorporates ten independent Induction Cell Primary Assemblies (ICPAs). The correction applied to the ion beam at the acceleration gap is the sum of the corrections generated by each ICPA. Resultantly, the maximum modulator voltage swing is reduced from 200 kV (±100 kV) to 20 kV. Neutralization of the ion beam can be applied immediately downstream of the acceleration gap. Therefore, transverse confinement fields only need to extend up into the acceleration module, not through its length.

The use of the inductive adder configuration for the FIEC greatly simplifies the requirements for the modulators to power the accelerator and also adds substantial flexibility to the waveform corrections that can be applied to the ion beam by the accelerator. The preliminary design calls for five of the 10 ICPAs to be powered by +20 kV modulators and five to be powered by –20 kV modulators, providing the capability to generate a correction voltage in the range of ±100 kV. However, the FIEC could be reconfigured if NDCX requirements change, for example, +20 kV modulators could be applied to all 10 ICPAs and provide energy correction in the range of 0 to +200 kV.

The complex waveforms to correct energy errors in the NDCX ion beam will be generated by adding the contributions of each ICPA. Each of the cells will be capable of generating a pulse, or pulses, of fixed amplitude, 20 kV, but variable duration during the passage of the NDCX ion beam. By varying the duration of each ICPA pulse and the relative timing between ICPAs, a step-wise approximation to almost any waveform between ±100 kV could be generated. However, as the rise and fall time of ICPA pulse will be ~15 ns, the step feature of many of the waveform transitions will be eliminated, further improving the accuracy of the correction. With the capability of ramping each ICPA to 20 kV in 15 ns, the FIEC will be capable of slewing at up to 13 kV/ns.

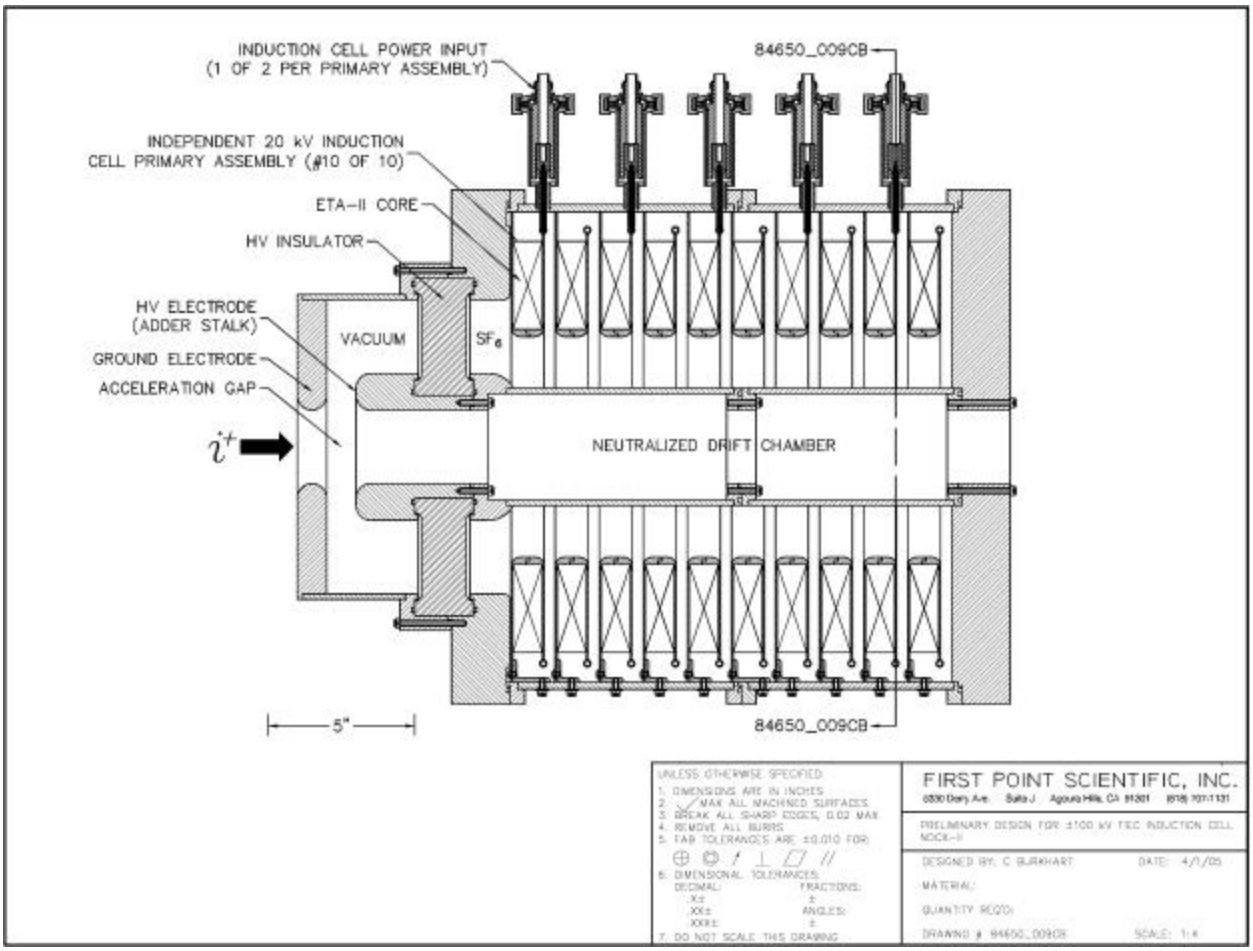

Figure 27. Sectional drawing (r-z plane) of the FIEC induction module.

A further improvement in the energy resolution of the FIEC could be achieved by applying a voltage lower than 20 kV to one or more of the ICPA. However, this would reduce the maximum energy correction that could be generated. The energy resolution required for the NDCX-II Li^+ point design is ±19.5 keV. Given that a resolution of ±10 keV or better can be achieved with the application of 20 kV, such an approach would not be required for that configuration. However, it is a possible option if requirements change.

As the FIEC is an induction accelerator, there will be a maximum volt-seconds, $\int V \cdot dt$, that can be applied to each ICPA before the magnetic core saturates. Since the intent of the FIEC is only to correct errors, not make a net addition or subtraction to the total beam energy, on average the time integral of the correction should be about zero. This implies that an integrated pulse length of 50 ns in either the positive or negative polarity should be sufficient to correct the 100 ns beam.

Each ICPA houses a high permeability ferrite core to inductively couple the primary voltage to the acceleration gap. The cores are 35.6-cm-OD X 20.3-cm-ID X 2.54-cm-HT and made of TDK PE-11BL material. This is the same core used in the ETA-II accelerator at Lawrence

Livermore National Laboratory where it was extensively characterized. The characterization of these cores in ETA-II provided a sound basis on which to estimate the performance of the ICPA.

The ETA-II induction cells contained 8 cores, to which a 125 kV pulse of 45 ns duration was applied, producing dB/dt = 8 X 10^6 T/s and DB = 0.36 T. Under these conditions the circuit response of the cores is very well modeled by a resistance of 200 Ω. The core in the ICPA will operate under similar conditions. At the maximum voltage, 20 kV, and pulse width, 50 ns, the flux swing will be, DB = 0.51 T and the rate of flux change, dB/dt = 1 X 10^7 T/s. The most significant change from the ETA-II parameters is the increased flux swing, which is still much less than the maximum for the material, DB = 0.65 T. Further, because the shape of the FIEC waveform is expected to be much more complex than a "square" 20 kV by 50 ns pulse, under most conditions both dB/dt and DB will be less than the maximum values calculated above and closer the ETA-II values.

The geometric variation in ferrite impedance is effectively modeled by $Z \propto A_c / l_m$ [8]. In reducing the load from the eight cores in the ETA-II cell to the single core in the ICPA, the core area, A_c, is reduced by a factor of 8 while the mean magnetic path length, l_m, stays the same. Therefore, the estimated impedance of the ICPA was 200/8 = 25 Ω (tests performed in this project actually indicated that 50 Ω provides a better match).

The ICPA core is encased in the primary winding. This provides several benefits as compared to a strap-type winding often employed in induction accelerators. First, it provides the mechanical support for the core. The winding is constructed of 304 stainless steel to provide mechanical strength. The skin resistance is sufficiently low, <1 mΩ, that it will not distort the applied waveform. Second, this provides a minimum inductance configuration for the primary winding. The inductance of the primary lead is a leakage inductance in series with the primary inductance of the ICPA that will degrade the waveform and hence, should be minimized. Additionally, the primary winding design minimizes electric field enhancements, by eliminating winding "edges" that could cause electrical breakdown in the module. The only edge in the primary winding design is at the outer perimeter where the high voltage leads attach and this is terminated in a corona ring. Lastly, this design allows for multiple waveform inputs on the primary.

One high voltage input is used to power each ICPA. the inputs of adjacent ICPAs are rotated by 180^o to maximize mechanical clearances. The high voltage feedthroughs that connect the drive cables to the ICPA are a proven design. They were developed for use on DARHT at LBNL and have been used subsequently on other projects at LBNL and FPSI.

The ICPAs are enclosed in a common pressure vessel. The housing is designed to operate with up to 5 atm of a SF_6/N_2 (30%/70%) gas mixture to provide high voltage insulation between adjacent ICPAs and between the primaries and the inner module housing (experimentally it was found that air at STP was acceptable).

All of the pressure vessel and vacuum chamber components are fabricated from 304 stainless steel. This material has sufficient strength for the mechanical loading that would result from up to 5 atm gas load and has excellent properties for use in vacuum. Seals between all demountable

joints will be made by elastomeric o-rings. To maintain alignment throughout the assembly, all of the chamber components will be aligned via concentric steps machined into adjacent parts rather than relying on assembly bolts.

The interface between the ICPA pressure vessel and the acceleration gap vacuum chamber is provided by a Rexolite insulator. This material was selected based on a number of favorable mechanical and electrical properties. It offers high dielectric and mechanical strength. The relatively low dielectric constant helps to minimize electric field perturbations at the vacuum/dielectric interface, which simplifies the electrostatic design. Rexolite also has very low out-gassing rates, which helps to minimize contamination of the vacuum system.

The electric fields in the module were examined using a numerical field solver. The results of these calculations are illustrated in Figure 28, an equipotential plot in the critical areas. The fields were calculated for a voltage of 200 kV, rather than 100 kV, to assure a substantial safety factor.

The maximum electric field in the vacuum region, 122 kV/cm, occurs on the high voltage electrode near the vacuum acceleration gap. The estimated electric field to induce breakdown is 300 kV/cm, so this design includes a substantial safety margin. In the SF_6 region, the maximum field, 115 kV/cm, is also on the high voltage electrode, near the high voltage insulator. The breakdown limit in the proposed gas mix is 260 kVdc/cm. For short pulse, <100ns, operation this limit will be higher, but quantitative relationships are not available. Suffice it to say, the design is very conservative.

The field limitation on the high voltage insulator depends on multiple factors. Perhaps most critical are the fields at the triple points, locations where conductor, insulator and vacuum/gas meet. Small gaps between conductor and insulator can produce large electric fields in the gaps that can stimulate electron field emission from the conductor or initiate electrical breakdown in the gas in the gap. The re-entrant electrode design near the triple points is incorporated to minimize the fields at these critical locations. Near the inner diameter of the insulator, the triple point fields are 15 kV/cm and near the outer, 6 kV/cm. Both values are acceptable for short pulse conditions. With the triple points properly accounted for, the maximum electric field that can be supported along the insulator is much higher than predicted by semi-empirical formulas

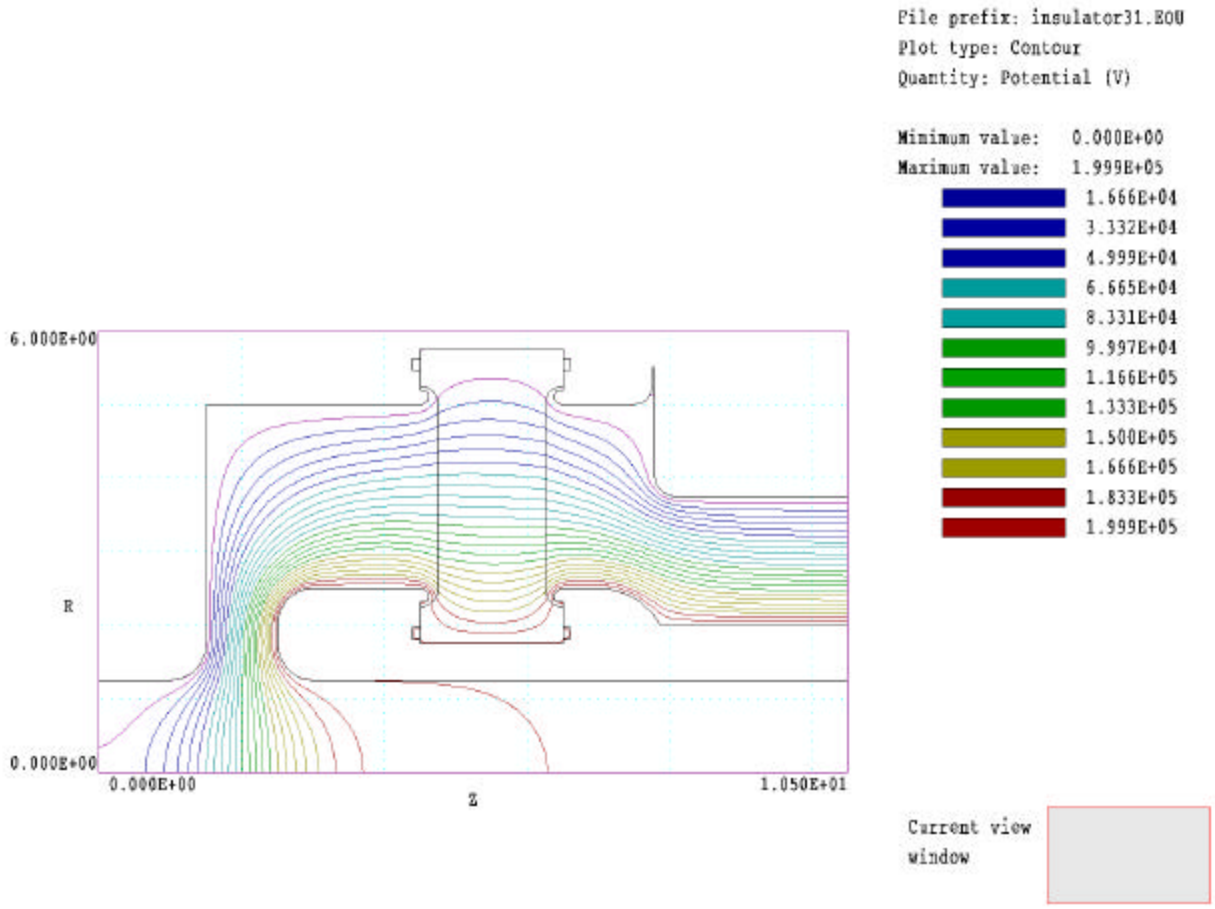

Figure 28. Equipotential plot in the critical high voltage areas of the FIEC induction module for an induced voltage of 200 kV.

that do not specify the triple point conditions. In both vacuum and SF_6 the insulator can easily support 100 kV/cm without breakdown under these short pulse conditions. The maximum calculated field in vacuum is 58 kV/cm and in the SF_6 it is 56 kV/cm. As in all of the other calculated fields, this provides a large safety margin from the breakdown limiting fields.

The capacitances within the induction module can distort the voltage induced at the acceleration gap relative to the ICPA input waveforms. Using the numerical field solver, the capacitance across the acceleration gap (including the area around the Rexolite insulator) was found to be 21 pF. The capacitance between individual ICPAs and the stalk is 3.3 pF. Between any two ICPAs, the capacitance is 80 pF. The manner in which these capacitances affect the output varies between ICPA. If a voltage is applied to ICPA #1, it will induce a field between the stalk and the other 9 ICPAs that must charge a capacitance of (9)(3.3 pF), plus the 21 pF of the acceleration gap and the 80 pF between the ICPA and the chamber wall, a total of 131 pF. The capacitance is a little lower for ICPA #10, the application of a voltage to that cell does not induce a field between the stalk and any of the other ICPAs, and so the total capacitance is 101pF. However, in each case, the ICPA will be driven by a 50 Ω impedance and so the characteristic response time, given by RC, will be 6.6 ns or less, much faster than the rise or fall

time of the pulses that will be applied. Therefore, the capacitances in the preliminary design will have a negligible impact on the performance of the FIEC.

Induction Cell Tests

Early in the project a single ETA-II ferrite core test setup was designed and assembled. Simple electrical tests were performed on one core to assess the basic core characteristics. It was found that the core impedance varied from 160 Ohms to 25 Ohms during a 50 ns pulse. This is more variation than expected as it was originally thought that the impedance would be relatively constant at approximately 25 Ohms. However, this does not include the affects of cell geometry and gap capacitance. However, these tests provided the foundation for proceeding to design and test a Cell Primary Assembly (ICPA), a single 20 kV induction cell that included all aspects of the cell design indicated in Figure 1. The experiment assembled to assess the electrical characteristics of the ICPA is shown in Figure 29.

Figure 29. Experimental assembly for evaluation of the electrical characteristics of the 20 kV induction cell primary assembly of the FIEC induction acceleration module. The chamber contains the cell assembly. The electronics rack contains the charging power supply for the reset circuit which is located in the yellow plastic box. The gas tank is used to pressurize the high voltage spark switch in the 20 kV, 50 ns pulser which is located under the bench. The pulser is charged from the power supply located on the bench next to the chamber.

Tests were performed using a one and two 50 Ω PFLs switched using a spark gap switch. The measurements included measurement of the I-V characteristics of the cell for various values of acceleration gap width (these tests indicated that the design width of 0.375 inches is best – smaller gaps result in more capacitive overshoot and large gaps increase the assembly length). The core was fully reset between pulses using both a low-voltage 1-ms pulser and a dc reset

circuit (in either case resetting to more than 1.2 Oe offered no benefit). Although provision was made to operate the cell in a pressurized insulting gas (30% SF_6, 70% N_2) in order to avoid electrical breakdown of the gap, it was determined that the cell can be operated in room air at up to approximately 25 kV without breakdown.

The voltage waveform of the driver operating with each cable connected to a 50 Ω resistive load is shown in Figure 30. Figure 31 shows the current and voltage waveforms for the ICPA containing ferrite core 6-21-B (one of the ETA-II cores provided by LBNL) when driven by two cables at diametrically opposed locations. The voltage pulse width at 80% of the peak voltage was measured as a function of both pulsed and dc reset currents. It was found to saturate at approximately 30 ns (corresponding to 41 ns fwhm). The integrated VT measured with the cell was 0.89 mV-s.

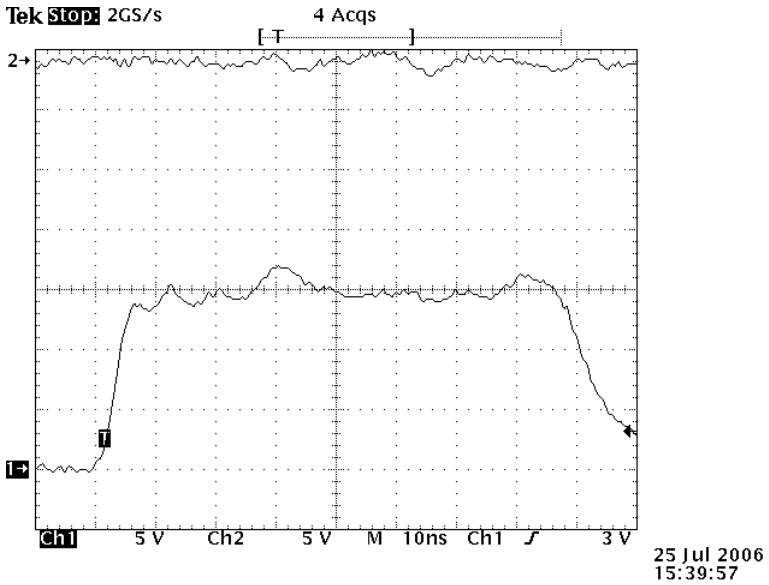

Figure 30. Voltage waveform of the driver operating into 50 Ω load at 4.63 kV/div.

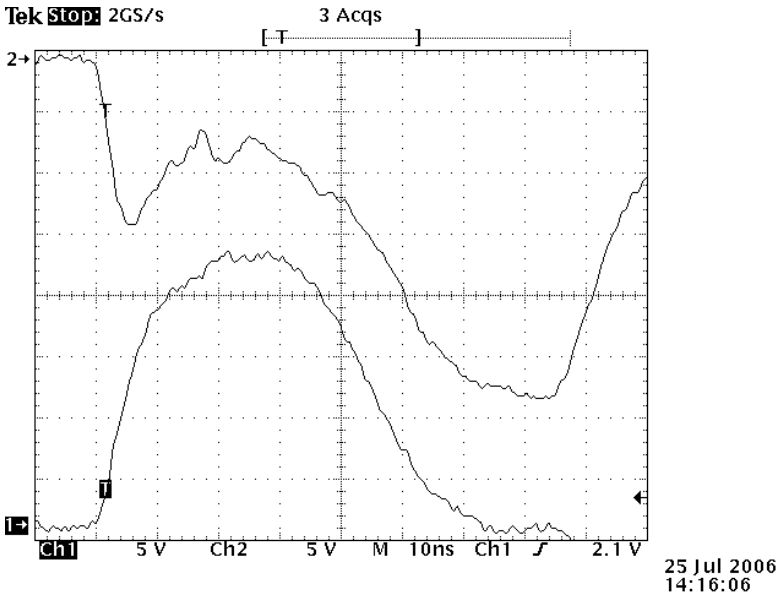

Figure 31. Channel 1 is the cell voltage at 4.63 kV/div measured with a 1:1000 Tektronix HV probe. Channel 2 is the current flowing in one drive cable at 100 A/div as measured with a 0.05 Ω CVR.

A second ferrite (6-16-A) was tested as part of the ICPS with the results shown in Figure 32 for two PFLs and drive cables, and Figure 33 for one PFL and one drive cable. This core performed slightly better than the first. The results are summarized below (Z is the total cell impedance).

t(ns)	I(2 cables, A)/V(kV)/Z(Ω)	I(1 cable, A)/V(kV)/Z(Ω)
10	420/17/40	440/17/39
20	380/20/53	340/20 /59
30	390/20/51	320/20/63
40	400/18/45	360/17/47
50	660/11/17	520/9/17
60	1000/4/4	650/3/5

	2 Cables	1 Cable
V pulse length (@80% peak V), ns	34	30
V pulse length (fwhm)	47	43
V risetime (10-90%), ns	12	15
Integral Vxdt, mV-s	0.93	0.89

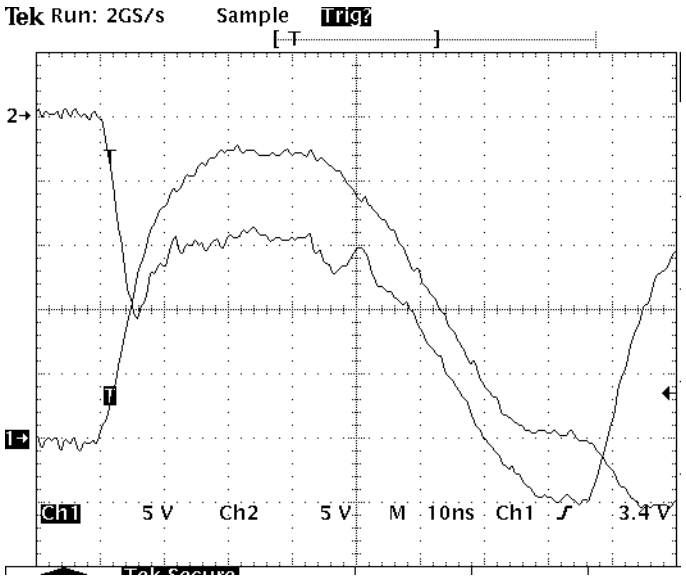

Figure 32. Data with two PFLs and drive cables. Channel 1 is the cell voltage at 4.63 kV/div measured with a 1:1000 Tektronix HV probe. Channel 2 is the current flowing in one drive cable at 100 A/div as measured with a 0.05 Ω CVR.

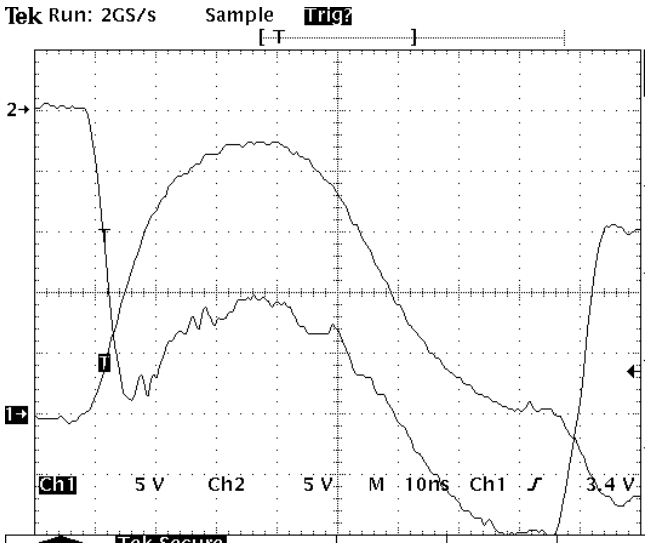

Figure 33. Data with one PFL and drive cable. Channel 1 is the cell voltage at 4.63 kV/div measured with a 1:1000 Tektronix HV probe. Channel 2 is the current flowing in one drive cable at 100 A/div as measured with a 0.05 Ω CVR.

The conclusions of the ICPA tests were:

1. There are small differences between cores. However, the first core was glued into the cell which may have resulted in stresses that changed the B-H characteristics slightly. The second one was not glued.
2. Better driver-cell matching is achieved using a single 50 Ω driver and drive cable with small penalties in V pulse length and rise time as would be expected. This is the preferred approach.
3. The goal parameters for Fast Agile Solid-state Modulator (FASM) are: 20 kV output voltage, 15 ns voltage rise and fall times, and an agile programmable pulse width ranging from 15 ns to 50 ns (fwhm) (corresponding to a maximum VT = 1 mV-s), into a resistive load impedance comparable to the induction cell impedance (thought to be 25 Ω at the time the proposal was written). The cell design has been demonstrated to be compatible with this goal to within approximately 10%.

Based on these results the final piece part fabrication drawings for the FIEC induction module were prepared.

Bids were obtained from three vendors (Huntington Mechanical Labortories, Nor-Cal, and Kurt J. Lesker Co.) for construction of the major components of the FIEC. Huntington was selected based on price; we also had good experience with them in previous projects. We note that the price was $19,645, about 4 times greater than what was originally proposed. The increase was due to the very large inflation in the cost of stainless steel as well as in manufacturing costs since our proposal was submitted in April, 2005.

Photographs of the parts are shown in Figures 34 and 35. The completed FIEC is shown in Figure 36.

Figure 34. Induction cell components.

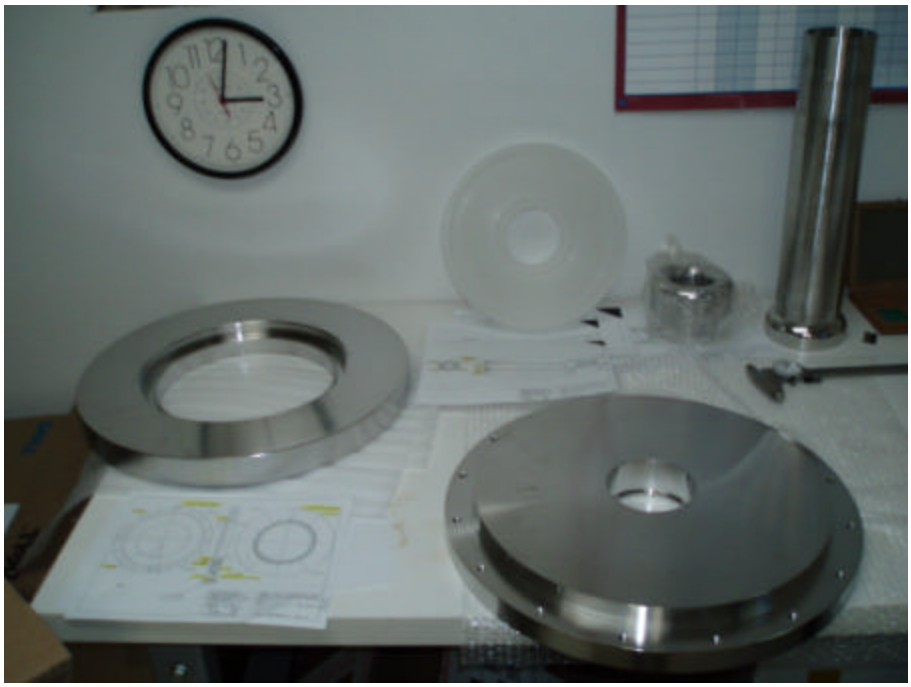

Figure 35. Induction cell Components.

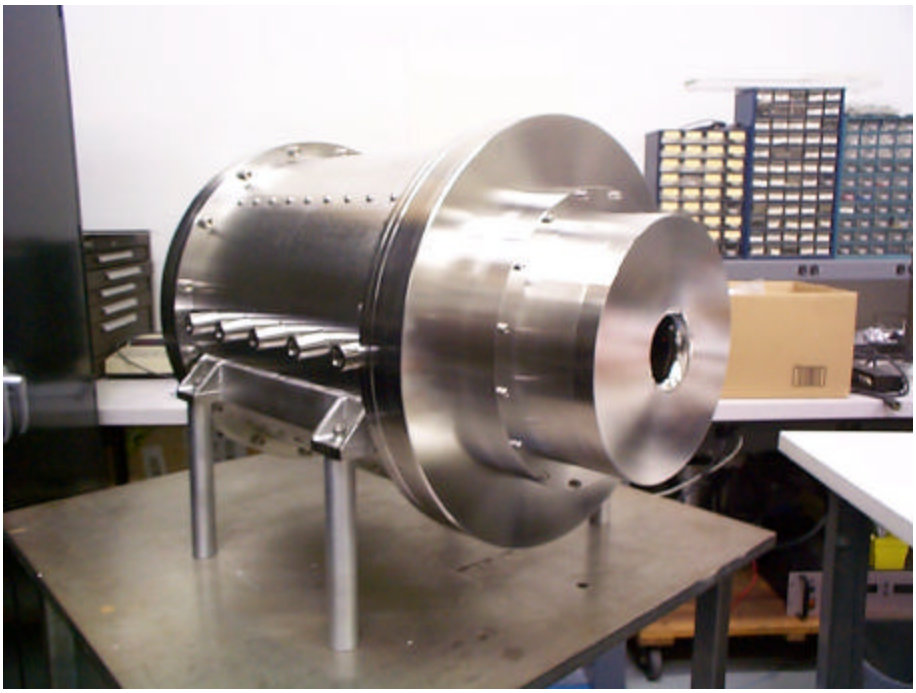

Figure 36. Completed FIEC induction module.

5. Task 3 - Construct and Test the FASMs for the FIEC

The objective of this task was to construct and test the ten FASMs for the FIEC. The status of this task at the conclusion of this project is summarized as follows:

1. One complete FASM has been completed and tested into a resistive load.
2. All major electronic components required to construct 10 FASMs have been ordered and received.
3. The daughter boards and mother boards required to assemble 3 additional FASM modules have been ordered and received.

6. Task 4 - Demonstrate the FIEC on the NDCX

The objective of this task was to demonstrate the FIEC on the NDCX with the goal of using the FIEC to regulate the longitudinal energy distribution of the NDCX ion beam to the accuracy required to reduce the axial length of the beam by 100X during neutralized drift compression.

LBNL Waveform Requirements Estimates

The NDCX-1 beamline is shown in Figure 37. The injected K^+ beam energy of 280-350 keV is established by a Marx generator with a nearly square shape. The corresponding space-charge-limited beam current strikes a current limiting aperture plate, transmitting 20-35 mA beam depending on the Marx voltage setting. Four matching solenoids are used to establish transverse envelope requirements at the entrance to the induction bunching module (IBM). The axial compression is achieved with the IBM inserted after the matching section. Operating the IBM with a voltage swing of ±100 kV, a ±12.5% velocity ramp is imparted to ˜0.5 μs subset of the several-microsecond beam pulse. The beam then drifts through a neutralizing plasma in a drift compression section a few meters in length (L=2.9 m). A ferro-electric plasma source [9] establishes a neutralizing plasma along most of the length of the drift compression section, and cathodic arc plasma sources injected a high-density (˜10^{13}/cm^3) plasma near the focal plane where the beam density is greatest. A short, high-field solenoid (B = 8 Tesla, 10-cm coil length) after the ferroelectric plasma source and before the target plane (Figure 38) imparts a steep convergence angle on the beam before the focal plane. A current amplification of > 50 has been demonstrated in NDCX experiments [10,11,12].

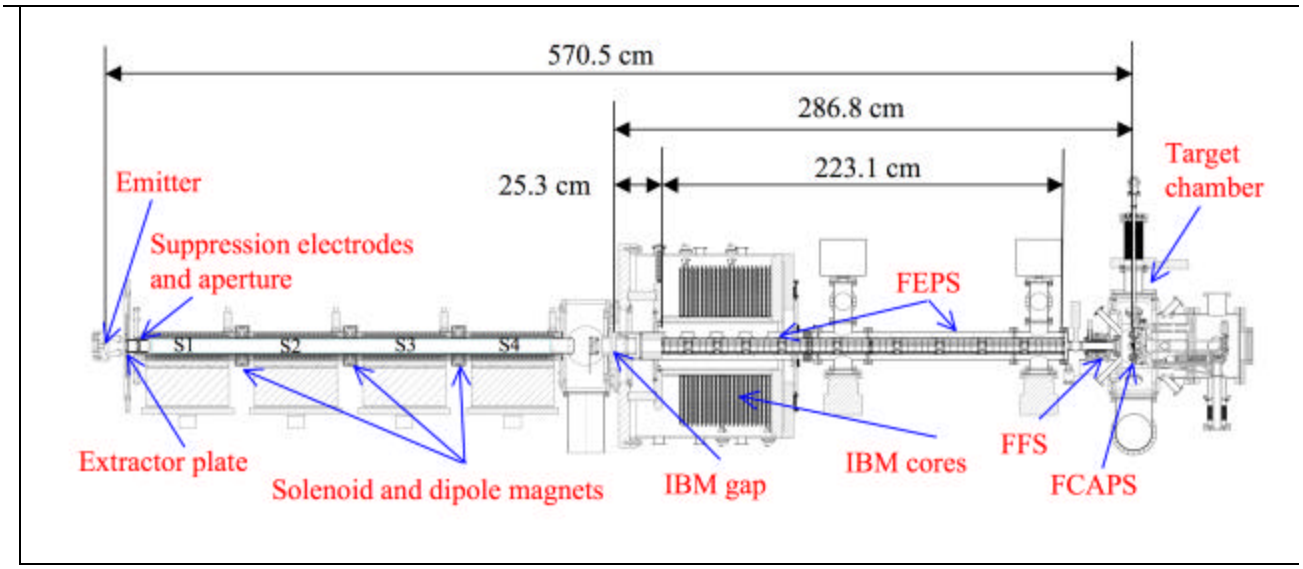

Figure 37. Elevation view of the NDCX-1 beamline.

Figure 38 shows an example of the IBM waveform, compared to the ideal waveform calculated from an analytic model [13] based on a linear velocity ramp to achieve an axial focus at a distance L:

$$\upsilon(t) = \frac{\upsilon_o L}{L - \upsilon_o t}$$

where υ_o the velocity of the leading edge of the bunching beam, and the resulting voltage waveform is:

$$V(t) = \frac{1}{2} m(\upsilon^2(t) - \upsilon_o^2)$$

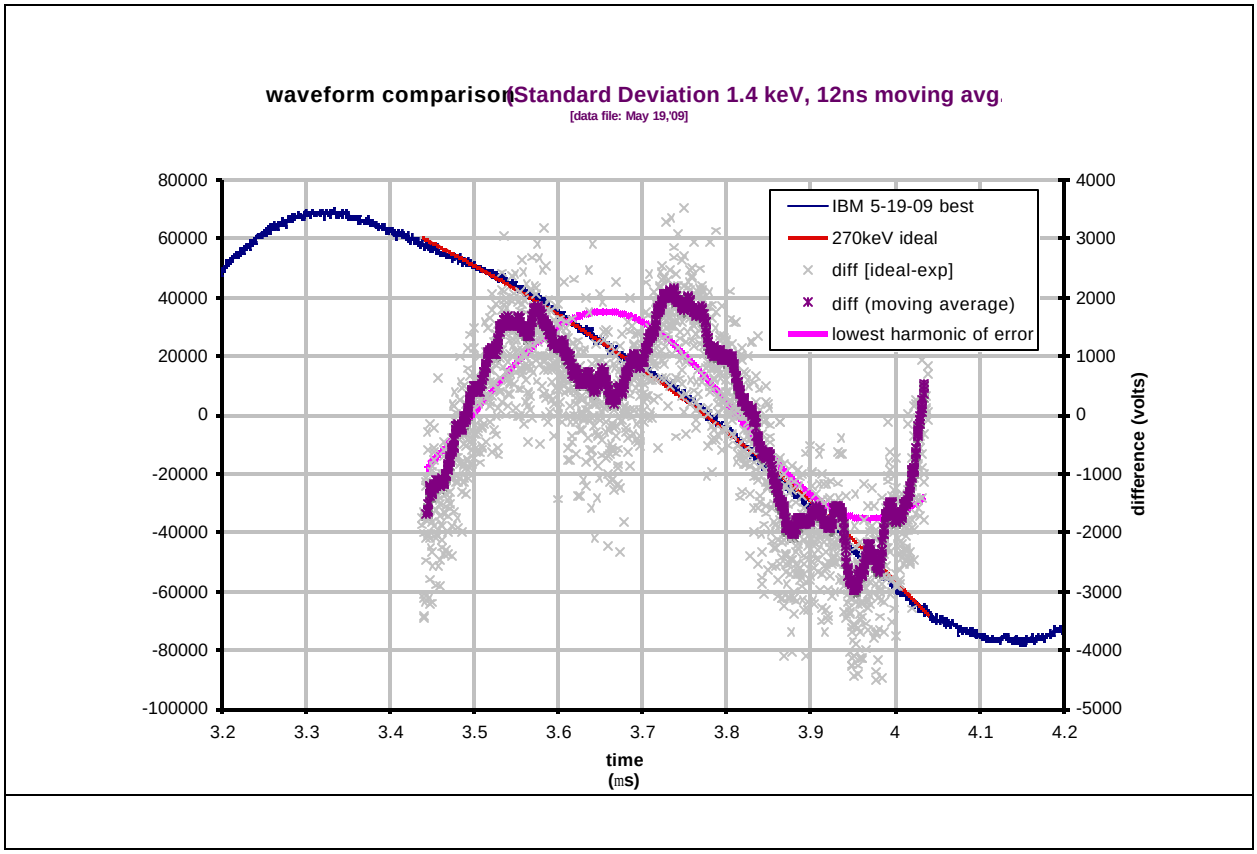

Figure 38. Comparison of IBM waveform (blue) to an ideal waveform (red). The IBM voltage scale is on the left, and the difference between ideal and experimental data is on the right. The magenta curve is moving average (12 ns) of the difference (gray crosses). This average is approximately one-half the transit time through the IBM gap, which would smooth the higher frequency component. The pink curve is a best fit of a sine function to approximate the lowest harmonic in the error.

This model makes the reasonable assumption that the gap is very short compared to the beam length and the drift compression distance. (The gap length is 3 cm and the transit time of 300 keV K+ ions is ~25 ns, while the bunched beam is initially ~0.5 usec, and the travel time from the IBM gap to the target is 2.4 usec.)

Integrating the absolute value of the difference between ideal and experimental waveform yields 753 μV•sec. This is less than the (20 kV) • (50 ns) = 1000 μV•sec for an FIEC module noted in the previous section, so there is adequate volt-seconds in the FIEC module to correct waveform errors such as these.

It would be possible to correct the *lowest* harmonic via a MHz-range ringing circuit (~1.6 MHz is the lowest harmonic in the example waveform of Figure 38 independent of the FIEC, since the time response required to do so is not especially demanding. This would permit using the FIEC to correct longer waveforms with higher fidelity, or enable corrections of waveforms calling for more opposite-polarity module combinations.

Whatever the waveform errors are, they change from shot to shot, as illustrated in Figure 39. We suspect that this may be caused by jitter among the individual trigger pulse generators, or variations in the output voltage of individual induction core modules, and we will test this hypothesis soon. Once the cause has been isolated, we expect that these random errors can be significantly reduced via a combination of noise shielding and trigger threshold adjustments. As shown above, any residual systematic errors are within the correction capability of the FIEC.

As a side note, shot-to-shot waveform error differences could be corrected in a feed-forward circuit with on-board waveform analysis, taking advantage of the relatively low ion velocity ($\beta = v/c = 4 \times 10^{-3}$ on NDCX-I, and 2.5×10^{-2} on NDCX-II). Note that feed forward is a concept that may not be practical on NDCX-I or NDCX-II due to their short length. However, it is of interest in longer induction linacs which afford more time to feed the correction to a downstream location.

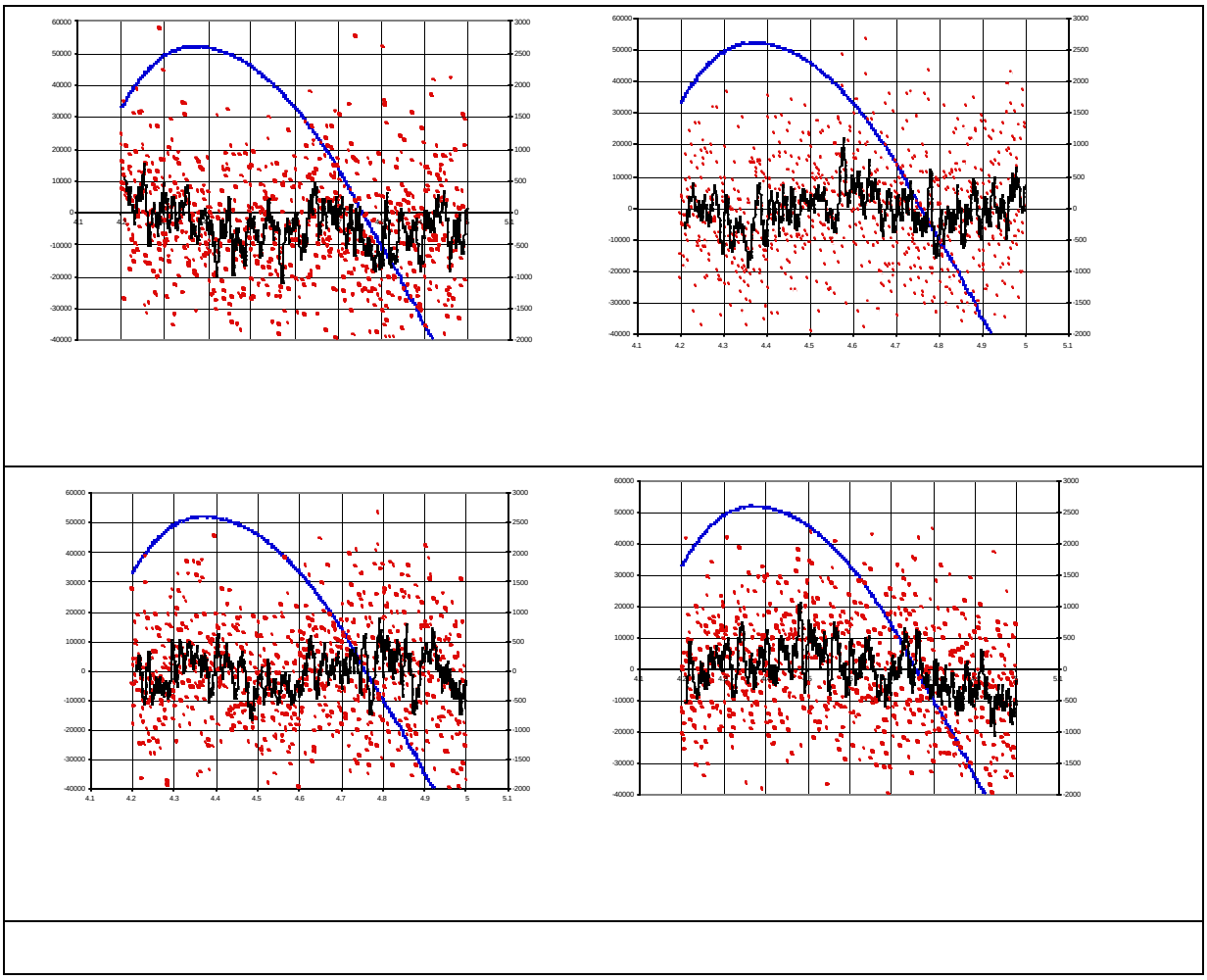

Figure 39. Four successive IBM shots illustrate the variation in waveform errors from shot to shot. The left scale is the IBM waveform voltage (blue curves). The right scale is the voltage difference (red data points) between the ideal waveform and the measured waveform. The black curve is a 10-ns moving average of the raw difference. (The data were recorded in August 2009 with the new IBM and the first voltage monitor.)

FPSI Deliveries to LBNL

FPSI delivered the assembled induction cell assembly (ETA cores and drive current feedthroughs, beam tube, acceleration gap and insulator, provision for SF-6 insulation) along with one (of 10) assembled inductive adder modulators. Most of the long lead time and high value components (PC boards, FETs, capacitors, FASM cores for all remaining nine modules) were also delivered.

LBNL Testing

A random subset of module components have been inspected at LBNL. Electrical tests of the assembled inductive adder modulator were carried out at FPSI. LBNL plans to repeat these electrical tests, finish assembling the remaining 3 modulators for which boards have been supplied by FPSI,

finishing the remaining 6 modules for which electrical components but no boards have been supplied, and test the system with realistic correction waveforms.

Testing the FIEC on NDCX-I would require completing these tasks and addressing the following issues: (1) assemble the remaining FIEC modulators with the FIEC induction module; and (2) machine the mating flanges in order to mate with the NDCX-I beamline.

The limited bore diameter requires space-charge neutralization in the FIEC. However, the presence of neutralizing plasma is not compatible in the ~19 centimeter region in the vicinity of the acceleration gap. Thus the beam will be somewhat defocused due to space charge, for which compensation would be required in upstream focusing elements. The tune window and envelope dynamics are already constrained by the beam tube dimensions in the neutralized drift compression section, so detailed modeling will be required to derive a workable envelope solution which allows clearance for beam halo and beam centroid offsets.

Waveform correction will occur at a different axial location from the IBM gap. Thus the correction waveform will not be a simple canceling of the errors in Figures 39 and 40, but modified by the drift compression of the beam. Since the minimum axial displacement between the IBM gap and a downstream corrector gap would be ~1 m (axial extent of the IBM module), the beam will have compressed by a factor 0.64, a modest change in beam length. Modeling this, including the space-charge waves induced by the waveform errors will be helpful.

Testing on NDCX-I will depend on scheduling the effort to be synergistic with the current programmatic goals.

7. Conclusions

This project achieved many of its objectives. Great difficulty was encountered in demonstrating a practical and workable FASM design. This led to increased costs for the FPSI portion of the project. Attempts to obtain a modification to the STTR grant, in which part of the funds originally allocated to LBNL were expended at FPSI in order to compensate for the increased costs, took a great deal of time but, in the end, proved fruitless.

At the conclusion of the project major components of the FIEC system were delivered to LBNL where they will be tested and incorporated in the NDCX experimental system for evaluation in the future.

Based on the work performed in the Phase II project it appears that the subject technology is technically and economically feasible. However, full demonstration could not be achieved within the funding and programmatic constraints of the program.

It is expected that the Fast, Agile, Solid-state Modulator (FASM) systems, when fully developed, will greatly improve performance, reduce costs, and serve as enabling technology for numerous commercial and Government pulse modulator applications in a variety of areas. Potential applications for the FASM include:

1. Induction accelerators including: HIF linear accelerators, induction synchrotrons and high power electron accelerators for radiation processing.
2. Pulsed lasers including: CO_2, excimer, copper vapor, nitrogen and YAG.
3. Low voltage ion accelerators and plasma ion implantation (PII) systems for ion surface modifications and semiconductor ion implantation.
4. Pulsed neutron generators for radiography, activation analysis and medical isotope production.
5. Two-beam electron accelerators for high-energy physics research.
6. Rf modulator drivers for radar and high-energy accelerators.

Many of the aforementioned applications will have uses in Government-sponsored research and development programs as well as in the commercial arena. The combination of tight regulation and low cost envisioned for the FASM relative to other modulator designs may enhance existing processes and be enabling to new applications.

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