Title

Design of a Wide Bandwidth Phase Modulator and Modeling of Polar Transmitters with Split-band Envelope Modulation

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Publication Date

2013

Peer reviewed|Thesis/dissertation

University of California

Los Angeles

Design of a Wide Bandwidth Phase Modulator and Modeling of Polar Transmitters with Split-band Envelope Modulation

A thesis submitted in partial satisfaction

of the requirements for the degree

Master of Science in Electrical Engineering

by

Sameed Hameed

2013

Abstract of the Thesis

Design of a Wide Bandwidth Phase Modulator and Modeling of Polar Transmitters with Split-band Envelope Modulation

by

Sameed Hameed

Master of Science in Electrical Engineering

University of California, Los Angeles, 2013

Professor Sudhakar Pamarti, Chair

High bandwidth and spectral efficiency requirements in today's wireless communication systems require innovative architectures to maintain high transmitter efficiency. Polar transmitters with a high efficiency switching power amplifier offer a promising solution to this problem. Such architectures require phase and envelope modulators with wider bandwidths than their Cartesian counterparts. This work presents a open loop phase modulator with 12 physical bits which is designed to operate at a carrier frequency of 1.25GHz with a phase bandwidth of up to 125MHz. The system was implemented in 65nm commercial CMOS process and a prototype IC achieved 8-bit linearity with pre-distortion and was modulated with PSK signals at 20.83MS/s while consuming 27mW of power. Separately, the problem of envelope modulation with a split-band envelope modulated system is considered. A MATLAB/Simulink model was developed to analyze trade-offs between efficiency, dynamic range and error in such a system.

The thesis of Sameed Hameed is approved.

Babak Daneshrad

Mau-Chung Frank Chang

Sudhakar Pamarti, Committee Chair

University of California, Los Angeles

2013

To my parents,

for their unconditional love and support

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Acknowledgments

I am extremely grateful to my advisor Prof. Sudhakar Pamarti, without whose help and support this thesis could not have been written. His depth of knowledge and patience has always amazed me and went a long way in helping me during this work. I would also like to thank Prof. Babak Daneshrad and Prof. Frank Chang for agreeing to be a part of my committee. I am also indebted to Prof. Asad Abidi and Prof. Behzad Razavi for their comprehensive IC design courses which further improved my understanding of basic principles in electronic circuits and systems.

I am deeply indebted to Ryan Jaewook Shin for his constant help during this research project. I learned a lot about IC design and testing from him and I don't think I would have had a better tutor for IC layout than him. I am also grateful for the discussions I had with Manas Bachu, Abhishek Ghosh, Jeffrey Lee and others who worked on other aspects of the project with me. My other group members including Neha Sinha and Nitin Nidhi were a great source of help during the tape out of the design as were my roommates Shailesh, Hitesh, Pranay and Chetan who helped keep my spirits high in those difficult times. Last, but not the least, I would like to express my deep gratitude towards my parents, family and friends for their constant love, encouragement and support during my time at UCLA.

CHAPTER 1

Introduction

1.1 Motivation

Data requirements have been increasing tremendously over the past decades, especially for consumer portable devices. To keep up with this increasing demand, scarce wireless spectrum has to be used with high spectral efficiency which has led to the usage of increasingly wider bandwidths and complex modulation schemes such as orthogonal frequency division multiplexing (OFDM) in modern communication systems such as LTE and WiFi which minimize guard bands in frequency domain [1, 2]. One particular downside to this shift has been the increase in the peak to average power ratio of wireless signals [3]. Increasing amount of work has been done on reducing this critical ratio [4] but such systems still require extreme linearity in power amplifiers (PA). Hence low efficiency in conventional transmitter architectures involving quadrature up-conversion is inevitable with usage of highly-linear and power hungry class-A/AB PAs running with huge back-offs from peak power driving the antenna. Thus, usage of novel power efficient transmitter architectures is of utmost importance, especially in power limited applications such as battery operated portable devices.

This thesis looks at an alternative transmitter architecture called the polar transmitter architecture which seems to offer a promising solution to the problem of transmitter efficiency. However significant challenges exist in a practical implementation of this architecture. The sections below describe the architecture

in detail and the challenges it poses such as wide bandwidth envelope and phase modulation. Various options are considered to deal tackle these issues while maintaining the benefits of the architecture. A practical wideband phase modulator is implemented and demonstrated to achieve good performance. A promising solution to wideband envelope modulation is also considered and modeled to realize its requirements and trade-offs.

1.2 The Polar Transmitter Architecture

Polar transmitter architectures, also known as Envelope Elimination and Restoration (EER) attempt to deal with this problem by eliminating the envelope signal from the input of the PA, thus operating it at its peak output power and hence highest efficiency at all times [5]. The envelope is then reintroduced through a separate envelope modulation input to the PA which is usually done by modulating its supply. The basic scheme is shown in Fig. 1.1 and relies on the rectangular to polar coordinate transformation shown in Eq. 1.1. Such a scheme allows the usage of switching PAs such as Class-E PAs which have much higher efficiency at peak output power compared to linear PAs [6]. This scheme also has several advantages over conventional Cartesian architectures such as absence of LO feed through or IQ mismatch.

$$I + jQ = Ae^{j\theta} \Rightarrow A = \sqrt{I^2 + Q^2} \quad \theta = tan^{-1}\left(\frac{Q}{I}\right) \tag{1.1}$$

However, polar architectures pose significant challenges in the design of the transmitter. It is well known that delay mismatch between the envelope and phase paths can cause significant spectral re-growth as well as EVM reduction in the transmitted signal [7]. Hence a way to calibrate the delays in both paths is required to cover inevitable variations over process, voltage and temperature (PVT). Another important drawback of polar architecture is the significant band-

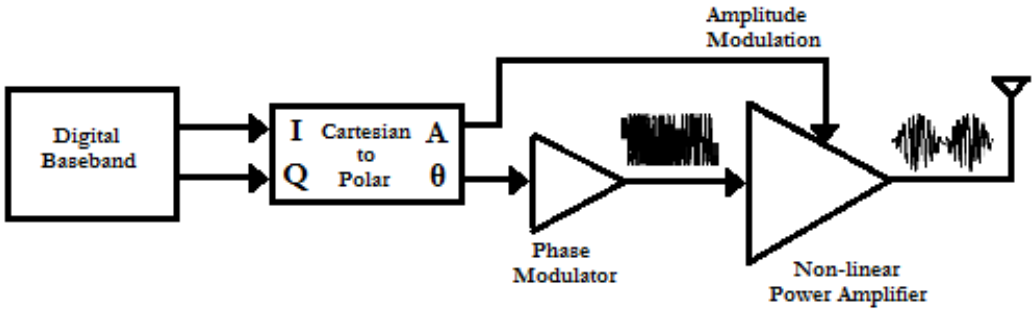

Figure 1.1: Polar Transmitter Architecture

width extension caused by the non-linear Cartesian to polar transformation. As an example, the Fig. 1.2 shows the power spectral density (PSD) of the signal in Cartesian form $(I + jQ)$ of a typical WiFi OFDM signal while Fig. 1.3 and Fig. 1.4 shows the PSDs of its corresponding amplitude (A) and phase $(e^{j\theta})$ signals, respectively. It is clear that while the spectrally efficient modulation scheme limits the bandwidth in Cartesian form, the bandwidth of the amplitude and phase signals are much higher. The bandwidth of the phase path is significantly higher with up to five times the Cartesian bandwidth being considered normal for OFDM signals.

1.3 Wideband Phase and Amplitude Modulation

Various architectures exist for achieving wide bandwidth phase modulation. One of the promising solutions is open-loop phase modulation [8, 9, 10]. In such modulators, different phases of the carrier signal, obtained using a delay-locked loop (DLL) or by dividing a high frequency signal is used along with a phase mixer or interpolator to achieve granular phase control. Hence a direct digital to phase conversion occurs which is easily amenable to digital pre-distortion techniques.

Envelope modulation at higher bandwidths is a significant problem. Supply

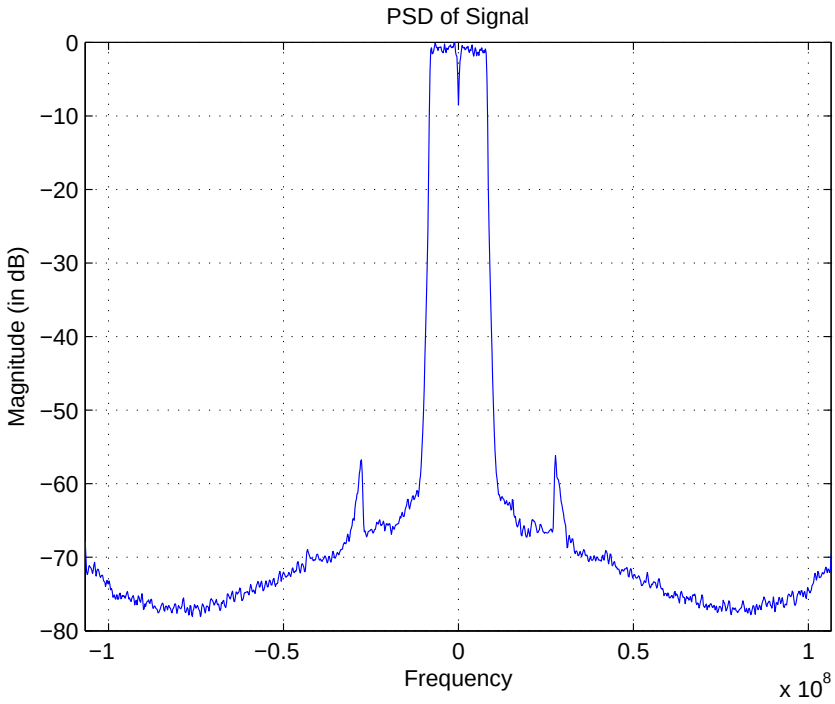

Figure 1.2: PSD of Signal in Cartesian Form $(I + jQ)$

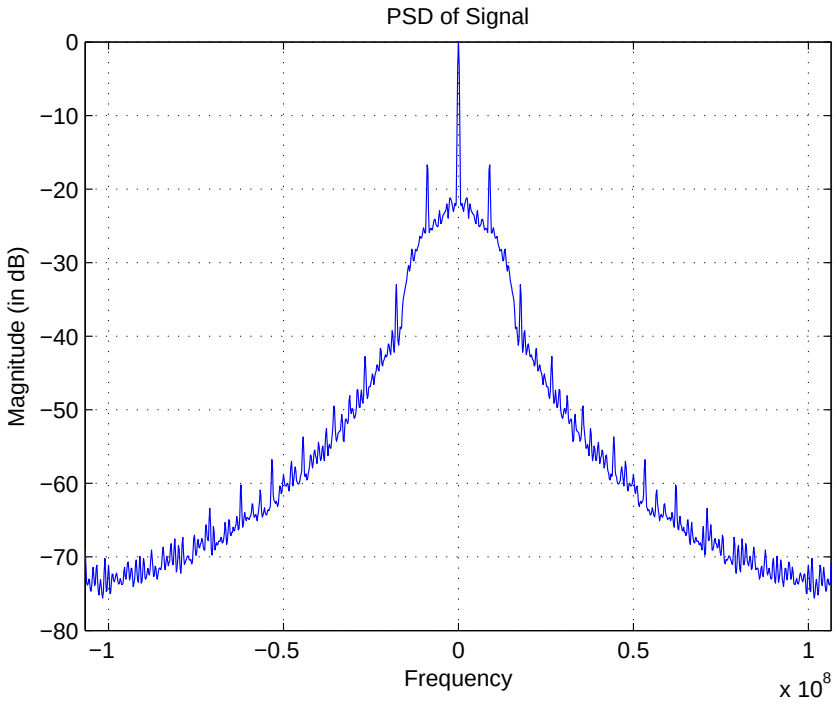

Figure 1.3: PSD of Amplitude Signal (A)

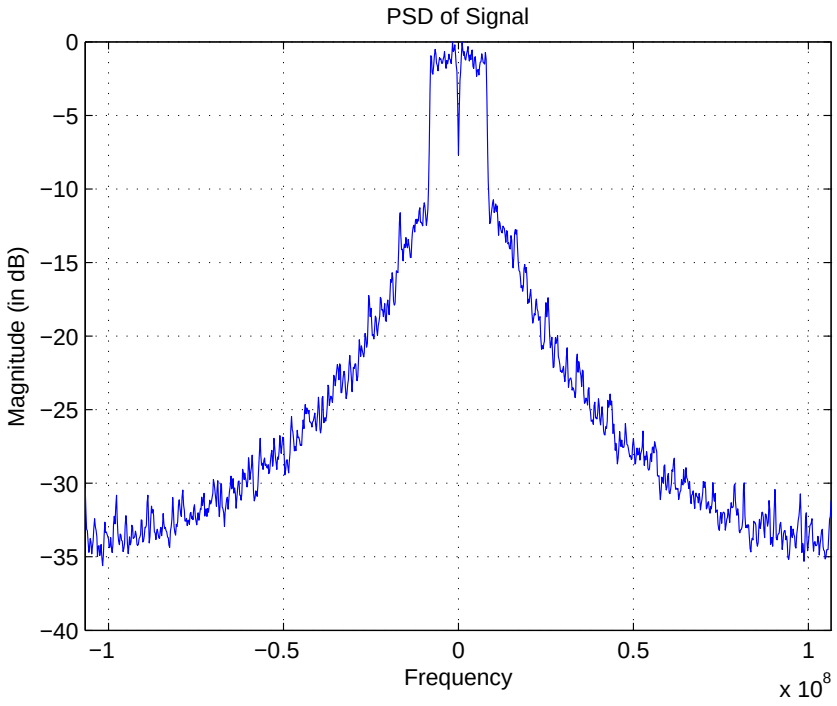

Figure 1.4: PSD of Phase Signal ($e^{j\theta}$)

regulation using switching DC-DC converters such as buck converters is highly efficient but is usually limited to a few MHz of bandwidth for reasons of efficiency and switching noise [11, 12]. Higher classes of supply modulators such as Class S supply modulators exist but are limited to a few tens of MHz of bandwidth. However the usage of switched mode PAs in polar transmitters allow additional degrees of envelope control such as controlling the duty cycle of the waveform driving the PA [13]. Such controls have been proved to be efficient even with back-off, using schemes such as contour modulation [14], but are usually limited in dynamic range due to difficulties in degenerating very fine small duty cycle waveforms at high carrier frequencies. Split-band envelope modulation, which splits the envelope data into different bands to be handled by highly optimized solutions for each band [15, 16] is an interesting solution to this problem but require careful optimization for dynamic range and efficiency of each block.

1.4 Organization of the Thesis

Chapter 2 describes various architectures to perform phase modulation in a transmitter. Their advantages and downsides are considered and open-loop phase modulation is shown to be a viable option.

Chapter 3 details the circuit implementation of an open-loop phase modulator and its ancillary circuits.

Chapter 4 discusses the testing of a prototype integrated circuit (IC) of the implemented phase modulator and details the performance metrics achieved by the design.

Chapter 5 presents details regarding a MATLAB/Simulink model to study the tradeoffs in a split-band envelope modulated system. Some results obtained are also discussed.

Finally **Chapter 6** concludes the thesis with some discussion on future work.

CHAPTER 2

Phase Modulator Architectures

Phase modulation involves varying the phase of a carrier signal usually as a function of the baseband signal. Various architectures have been published in the literature for wideband phase modulation. This chapter describes a few of them and discusses their advantages and drawbacks. Then the architecture of the open-loop phase modulator which is implemented is detailed.

2.1 Cartesian Phase Modulator

A Cartesian phase modulator consists of two DACs which generate two quadrature phase inputs which are then up-converted by using mixers to the required RF frequency [17]. This simple scheme is shown in Fig. 2.1. The DACs and the mixers can be combined together in a single stage as shown in Fig. 2.2 which is called a digitized Cartesian phase modulator [18].

Though very simple, this architecture suffers from various problems arising from gain and phase mismatches in the two arms and inaccurate quadrature phases from the local oscillator (LO). For higher bandwidths, the problems are more severe with increasing frequency dependent mismatches in the two branches. Mismatches can also cause parasitic amplitude modulation which if clipped by a non-linear PA, can cause significant spectral re-growth.

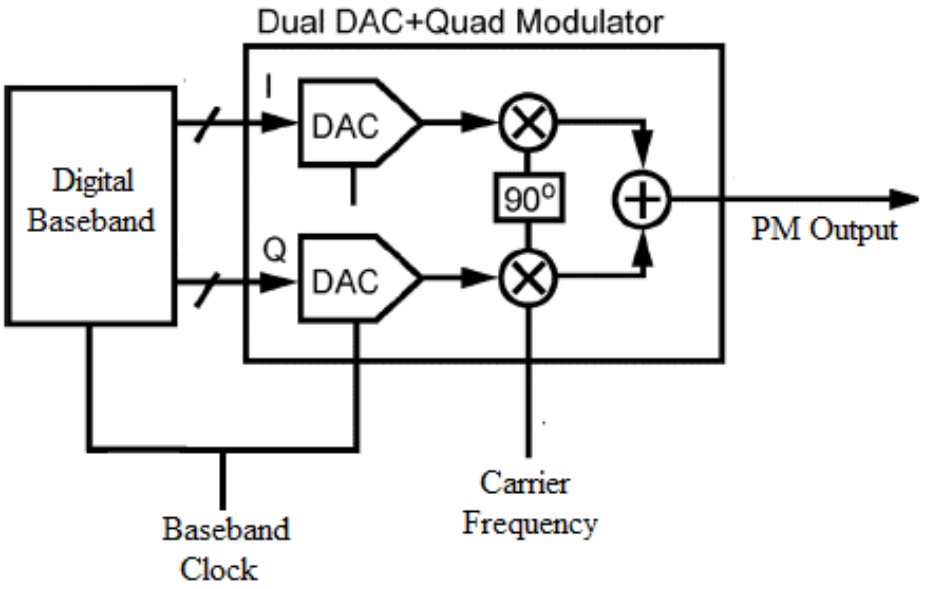

Figure 2.1: Cartesian Phase Modulator

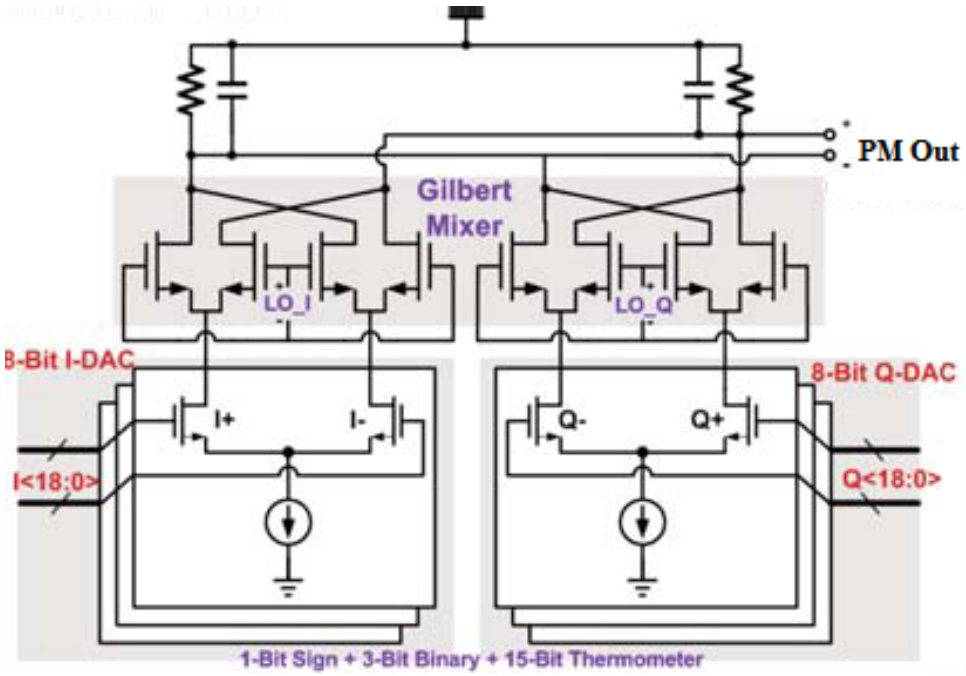

Figure 2.2: Digitized Cartesian Phase Modulator

2.2 Offset PLL

An offset PLL uses phase-locking in phase-locked loop (PLL) to perform phase modulation on a carrier signal. Such a PLL behaves like a frequency up-converter in the radio transmitter and are known as frequency translational loops (FTL) [19, 20]. The architecture is shown in Fig. 2.3. The I and Q represent quadrature base-band signals corresponding to a constant-envelope modulation scheme that are first up-converted to an intermediate frequency (IF). This signal is compared with a down-converted version of the PLL output signal. Hence in steady state, the PLL output signal will be phase-modulated according to the IF signal. In such an architecture the noise present at the modulator output is filtered by the PLL for frequency offsets in excess of the loop bandwidth from the RF carrier which can eliminate the need for any additional filtering.

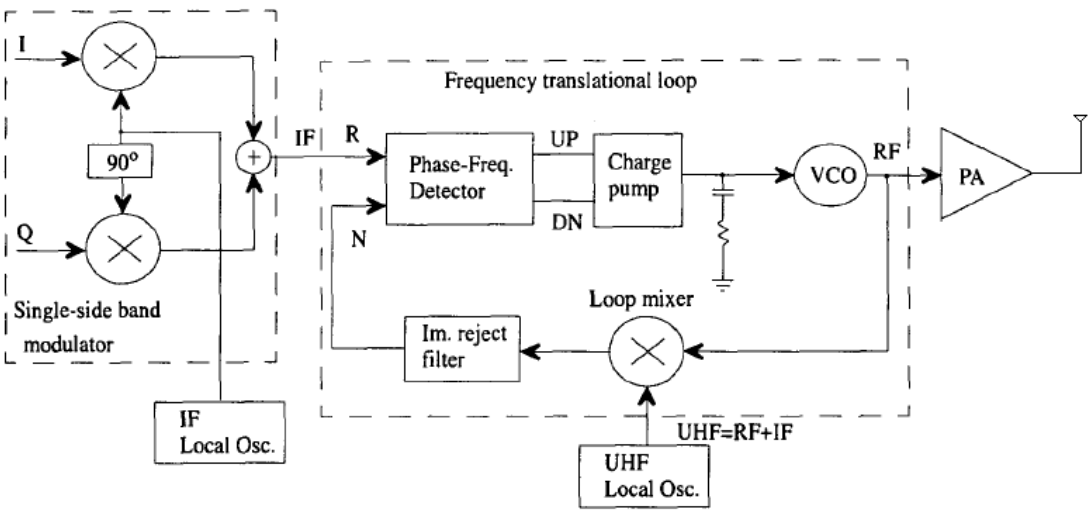

Figure 2.3: Offset PLL

Clearly, such a system can generate phase modulated signals with a bandwidth less than the loop-bandwidth of the PLL. However, PLL loop-bandwidths are generally confined to less than 1/10th of the IF frequency which is usually a few MHz for reduced power consumption and mismatch requirements. Hence, phase

modulation bandwidth achievable is extremely limited. Additional requirements of this architecture are analog components for generating the IF signal such as DACs and mixers and generation of the IF and LO signals which require additional frequency synthesizers.

2.3 Fractional-N PLL

A fractional-N PLL uses a programmable divide ratio in the feedback path of a PLL to achieve output frequencies which are a fractional multiple of the input frequency. Usually the divide ratio is controlled using a digital $\Delta\Sigma$ modulator such that the average divide ratio in the feedback path is the required fractional value. This allows usage of reference frequencies which are much higher than the channel spacing in a wireless standard (unlike in an integer-N PLL) and also allows a larger loop-bandwidth. To perform phase modulation on the carrier signal generated by a fractional-N PLL, the digital input to the $\Delta\Sigma$ modulator can be varied so that the output frequency and hence the phase is modulated as required [21]. This concept is shown in Fig. 2.4.

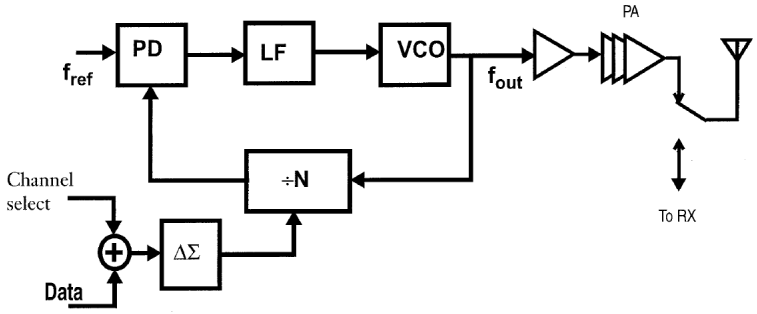

Figure 2.4: Fractional-N PLL

The advantage of such a system over an offset PLL is that analog components are not required except those used in the frequency synthesizer itself. Also additional synthesizers required for generating the IF and LO frequencies in an offset PLL are not needed. Hence power consumption is greatly reduced. The phase

modulation bandwidth is still limited by the loop-bandwidth [22] which is usually about a few MHz so as to reduce the quantization noise from the $\Delta\Sigma$ modulator appearing at the output phase. Also, fractional spurs which are caused due to the $\Delta\Sigma$ modulation pose a significant problem, especially as the loop-bandwidth is increased. Hence wideband modulation is not achievable.

2.4 Two-Point Modulation

As seen in the case of the fractional-N PLL, the phase modulation bandwidth is usually limited by the loop-bandwidth of the PLL. The two-point modulation technique circumvents this problem by splitting the phase modulation into two and sending a portion directly through the VCO by modulating its control voltage while the other is passed through the $\Delta\Sigma$ modulator as in a regular fractional-N PLL [23]. The band pass phase transfer characteristic from the VCO input to the output phase thus allows phase modulation beyond the loop-bandwidth. This is illustrated in Fig. 2.5.

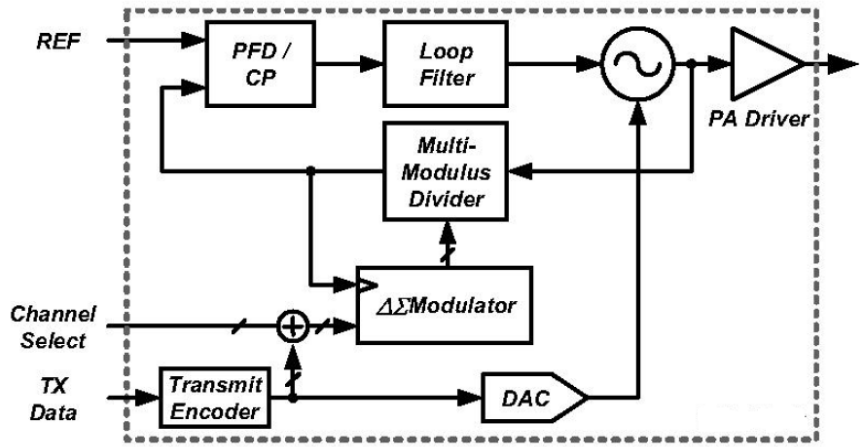

Figure 2.5: Fractional-N PLL with Two Point Modulation

This achieves much higher modulation bandwidths independent of the loop-bandwidth. Hence loop-bandwidth is decoupled from the modulation bandwidth

and can be optimized to minimize noise contributions from for example the $\Delta\Sigma$ modulator. However, like in any system with multiple parallel paths, such a system requires gain and delay matching between the two paths which becomes increasingly difficult at higher phase bandwidths and over PVT and so requires extensive calibration [24]. Also, the VCO gain non-linearity adversely affects achievable phase modulation accuracy. Hence the bandwidth is typically limited to below 5MHz.

2.5 All-Digital PLL

The two-point modulation technique described above can be easily implemented in all all-digital PLL as well for further increase in the modulation bandwidth. In an all-digital PLL, the VCO control is also a digital input and hence modulation data can be added digitally similar to the input of the $\Delta\Sigma$ modulator [25]. Hence digital calibration of gain and phase mismatches between the two paths is easier. Fig. 2.6 shows an all-digital PLL modified for two-point modulation.

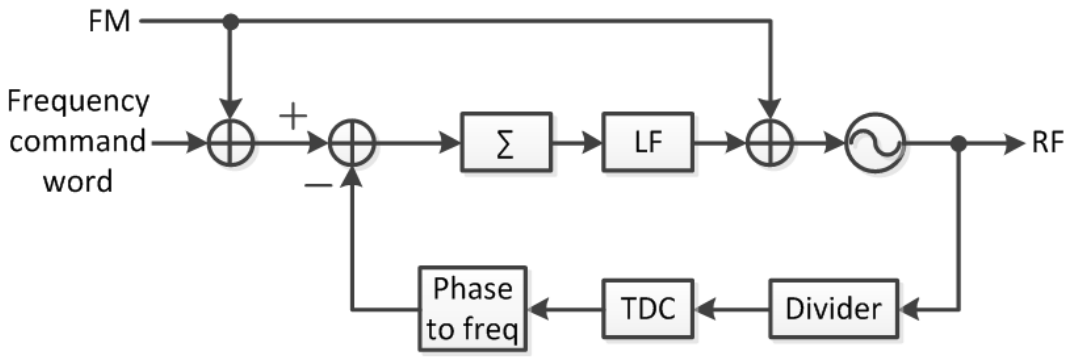

Figure 2.6: All-Digital PLL with Two Point Modulation

The all-digital PLL is a robust solution which scales well with technology and the digital implementation of the two-point modulation invites easier digital calibration for gain and timing mismatches in the two paths. The DCO gain

non-linearity has to be carefully calibrated too to achieve high phase modulation accuracy [26]. Achievable bandwidths are typically below 20MHz.

2.6 Open-loop Phase Modulator

Figure 2.7 shows a conceptual open-loop phase modulator [9]. It generates an output phase modulated waveform depending on the input phase codes it receives and so it acts as a digital to phase converter. Essentially, M different phases of a carrier signal are generated using a PLL or using phase interpolation on various phases of the carrier signal and then the required output phase is selected based on the input phase codeword [10].

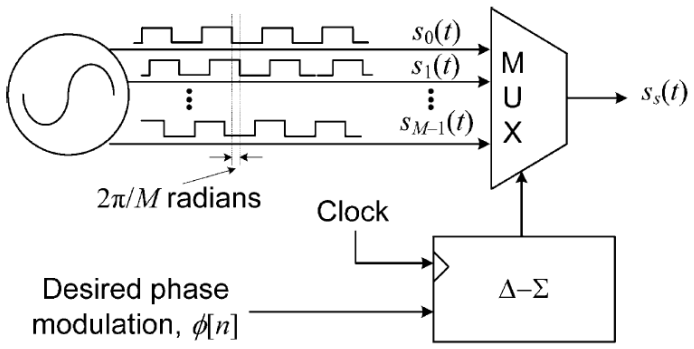

Figure 2.7: Open-loop Phase Modulator

Clearly by limiting to M different output phases, usually spaced $2\pi/M$ radians apart, the phase data is quantized introducing phase quantization noise (PQN) which can violate the spectral mask of the wireless standard if M is too small. To reduce this noise, oversampling with interpolation or $\Delta\Sigma$ modulation can be applied on the input phase code words before being supplied to the phase modulator [8]. However $\Delta\Sigma$ modulation while improving in-band EVM, can significantly degrade out of band spectral emissions which must be suppressed by additional filtering. Images at frequency offsets from carrier frequency which are multiples of the phase modulator clocking frequency also need to be sufficiently attenuated

for meeting the emission mask of any wireless standard.

2.7 Open-loop Phase Modulation with PQN Cancellation

One of the limitations of open-loop phase modulation is the introduction of phase quantization noise (PQN) due to the quantization of the phase data when the number of output phases possible M is small. To reduce PQN, one obvious method is to increase M, but this comes at significantly higher power consumption and matching requirements. An interesting technique to cancel PQN while not changing M is detailed in [9]. A block diagram of the system is shown in Fig. 2.8.

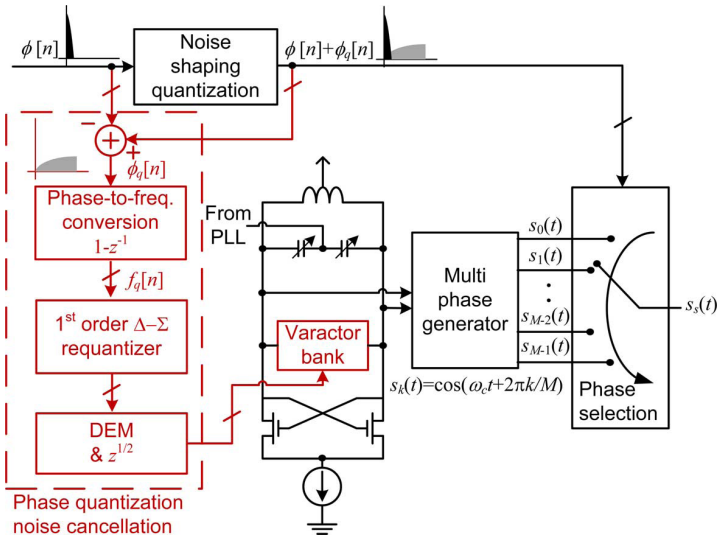

Figure 2.8: Open-loop Phase Modulator with PQN Cancellation

The technique essentially involves calculating the phase quantization noise produced and cancelling it by introducing it through an additional control port in the VCO which generates the carrier signals for the phase selector. If the output phase of the VCO is advanced or retarded by the exact opposite amount as the quantization noise, perfect cancellation is achieved. About 7dB of PQN cancellation is demonstrated in [9] while a theoretical 12dB of cancellation is predicted in case of perfect VCO gain estimation.

CHAPTER 3

Implementation of the Phase Modulator

3.1 Phase Modulator Architecture

The architecture chosen for this work was an open-loop phase modulation architecture due to its inherent higher achievable bandwidth, its convenience in controlling delay mismatch between phase and amplitude modulation paths and for being easily amenable to digital pre-distortion. The architecture of the phase modulator designed [27] is shown in Fig. 3.1.

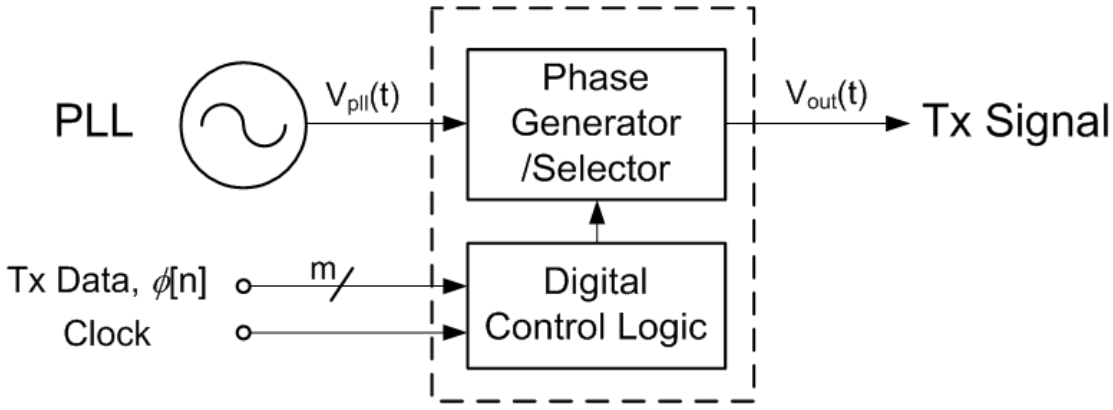

Figure 3.1: Open-loop Phase Modulator Architecture

The open-loop phase modulator consists of phase generator (and/or selector) and digital control logic. The phase generator/selector receives a clean signal at the carrier frequency from phase-locked loop (PLL), and generates multiple sub-phases and selects one of them to make phase modulated output signal under

the control of digital logic which decodes transmission data ($\phi[n]$) at the clock frequency.

The phase generator and selector is composed of frequency dividers and multiplexers. As discussed in Chapter 2, the number of output phases which can be generated sets the floor on phase quantization noise. $\Delta\Sigma$ modulation can be used to improve in-band noise floor but significantly degrades out-of-band noise which may require additional output filtering which will significantly reduce transmitter efficiency. Ring oscillator or delay line can also used as multiple phase generation circuits, but they have inherently high phase noise. Thus, they are not suitable for high resolution phase modulators.

To generate much finer resolution phase steps, the concept of phase interpolation is used. Figure 3.2 (a) shows a conceptual phase interpolator whose output phase is dependent on the current control X, where the value of X is between 0 and 1. The output phase ϕ varies from ϕ_1 to ϕ_2 as X increases from 0 to 1 (Fig. 3.2 (b)). Such a structure is suitable for fine phase control and immune to common mode noise sources due to its fully differential structure.

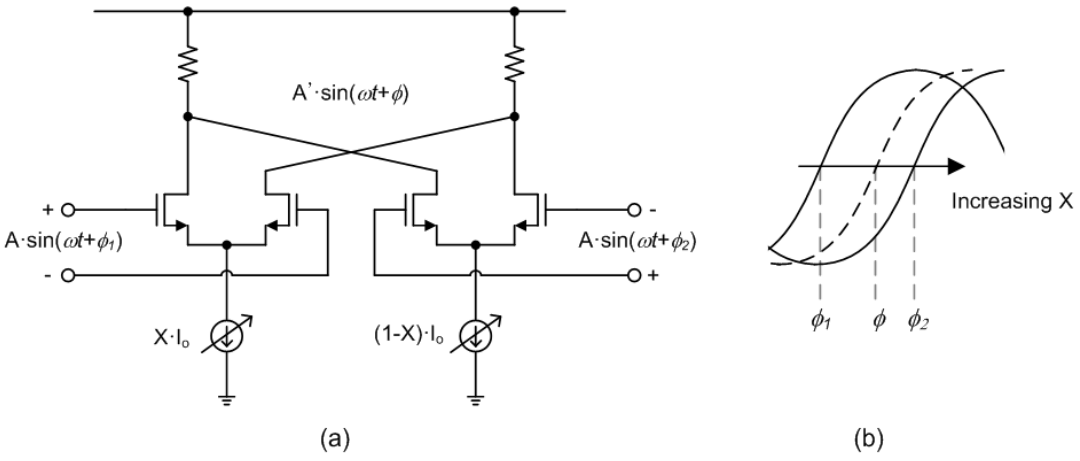

Figure 3.2: Conceptual Phase Interpolator

Output phase linearity of the phase interpolator in Fig. 3.2 (a) is highly dependent on the input phase difference $\Delta\phi(= \phi_1 - \phi_2)$. Figure 3.3 compares

calculated differential non-linearity (DNL) of output phase when $\Delta\phi$ is 45^0 and 90^0. DNL varies between -0.09 and 0.05 for 45^0 and -0.36 and 0.27 for 90^0. Clearly, a lower $\Delta\phi$ improves the linearity of the interpolator but drastically increases the complexity of the phase generator block. Lower $\Delta\phi$ implies a higher frequency carrier signal needs to be generated and divided down to generate the required number of phases which increases power consumption. Hence in this work 45^0 input phase difference is selected.

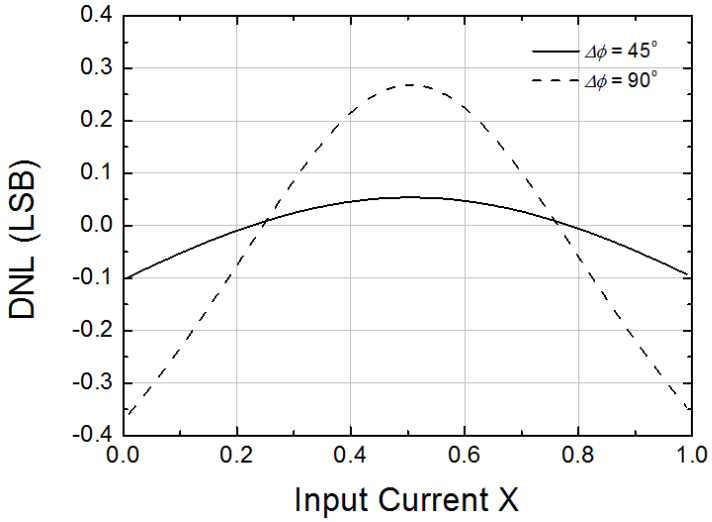

Figure 3.3: Phase Interpolator Linearity vs. $\Delta\phi$

The block diagram of the implemented open-loop phase modulators is shown in Fig. 3.4. A clean high-frequency carrier signal at 10GHz is obtained from a PLL or an external source. This signal is divided down to the desired carrier frequency by a two-stage CML divide-by-2 stage which generates octant phase signals which are at 45^0 phase offset intervals. These signals are passed through amplitude and phase tuning buffers to correct for mismatches in various paths and then are passed to two coarse 8-to-1 MUXs which perform octant phase interpolation based on the 3 MSBs of the digital phase selection signal. The two selected signals (ϕ_1 and ϕ_2) are then passed to the sub-octant phase interpolator which is controlled by the 9 LSBs of the phase selection signal to obtain the required output phase.

The phase modulated signal at the phase interpolator output is then converted to a CMOS level output which drives the final output inverter chain buffer.

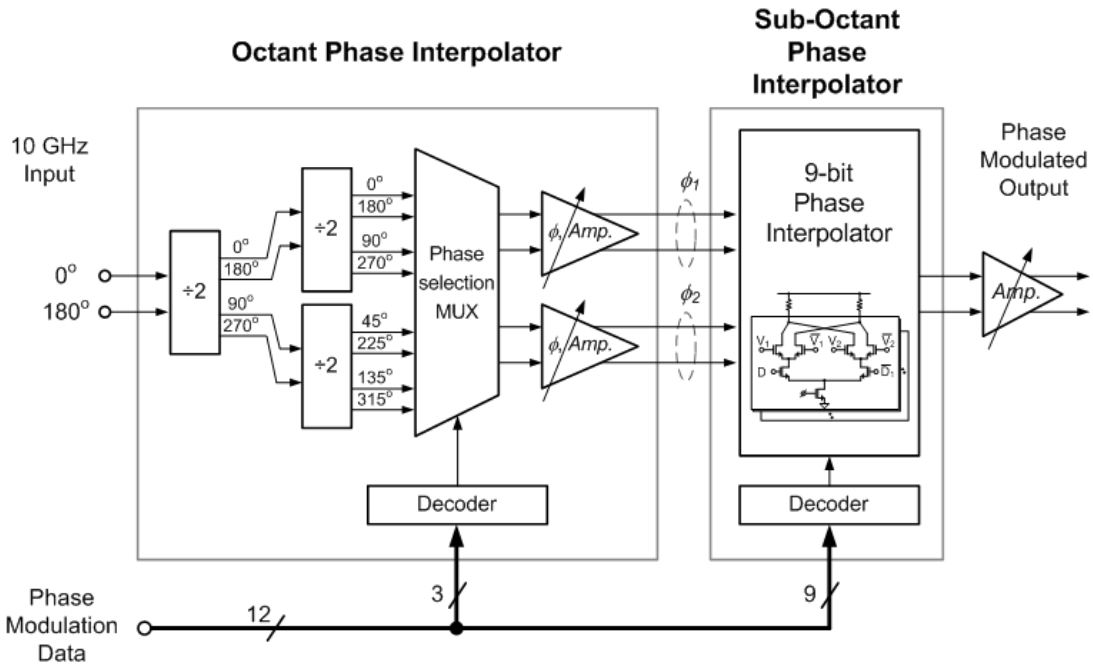

Figure 3.4: Block Diagram of the Phase Modulator

3.2 Circuit Design

3.2.1 Phase Interpolator

Figure 3.5 shows the unit interpolator circuit in 9-bit sub-octant phase interpolator. Following the concept shown in Fig. 3.2(a), it has two differential pairs controlled by the input V_1 and V_2 which corresponds to phases ϕ_1 and ϕ_2 respectively. The tail current source is a constant current source which feeds either of the two differential pairs based on the additional input D and its complement $\bar{D}$. To realize phase interpolation, the current weight X in Fig. 3.2(a) should be updated at the clock frequency. In this work, NMOS switches M_1 and M_2 present in all the interpolator units receive digital data which set the steering ratio X.

The shared source of the two NMOS switches (M_1 and M_2) improves the speed of current switching since the tail current source is never turned-off. Limited amplitude control is achieved at the output using tail current control which is primarily used for amplitude control over PVT.

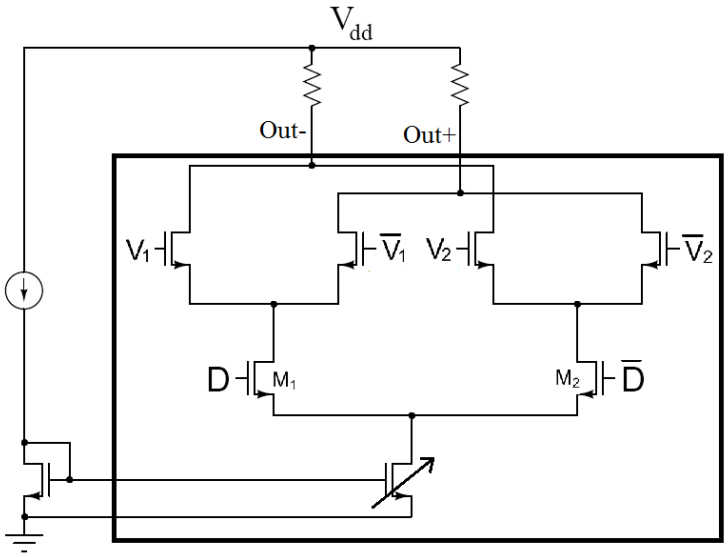

Figure 3.5: Phase Interpolator Unit Cell

To achieve 9-bits of phase interpolation, 512 equally sized unit cells could be used which can be controlled with a 9-bit input which can be decoded to activate required number of unit cells for current steering. Ideally, all bits could be used for thermometer control to guarantee phase monotonicity with digital input but in the interest of minimizing area (as 1-bit wider binary to thermometer code conversion requires twice as many digital gates) while maintaining performance, 5 bits of thermometer control for the MSBs and 4 bits of binary control for the LSBs was chosen. Hence the thermometer controlled unit cells could be grouped together to form new unit cells which are more compact but carry 16 times the current of a unit cell controlled by the LSB.

Overall the phase interpolator is grouped into 31 unit cells carrying 16 times the LSB unit current, one unit carrying 8 times unit current, one carrying 4 times,

one carrying 2 times and two carrying an LSB unit current to totally carry 512 LSB units of current. The 31 unit cells carrying 16 times the LSB unit current are controlled using thermometer code derived from the 5 MSBs of the digital data input which the 4 LSBs control the remaining binary sized unit cells.

The sizing and careful layout is critical for the linearity of the phase interpolator in the presence of mismatches. The sizing of the basic unit cell was decided based on careful Monte-Carlo simulation on the unit cell. The most critical sizing is that of the tail current source as any mismatch in the tail current source directly translates to different non-linearity (DNL) in the interpolator output phase. Also, larger the tail current source, smaller the mismatch but larger the area of the interpolator. Increasing the nominal value of tail current improves the linearity as well but at the cost of extra power consumption. Hence the size was set such that the standard deviation of the unit cell current is less than 0.1 LSB with a total phase interpolator power consumption of 2mA from a 1V supply. To randomize the effect of mismatch, the unit cells placement was carefully chosen in layout. The phase interpolator layout is shown in Fig. 3.6 and occupied an area of $300\mu m \times 150\mu m$ after layout.

3.2.2 Multi-phase Carrier Generation

The phase modulator receives a 10GHz carrier input from an on-chip PLL with an option to receive up to 20GHz input from an external source. To generate octant phase signals, the carrier signal is divided down by CML divide-by-2 stages. Each stage consists of two CML latches, shown in Fig. 3.7. connected in feedback with each other as shown in Fig. 3.8.

The capacitive load and output frequency determines the resistive load. Hence current consumption determines the output swing of the divider which needs to exceed a certain threshold for reliable operation of the divider. To minimize

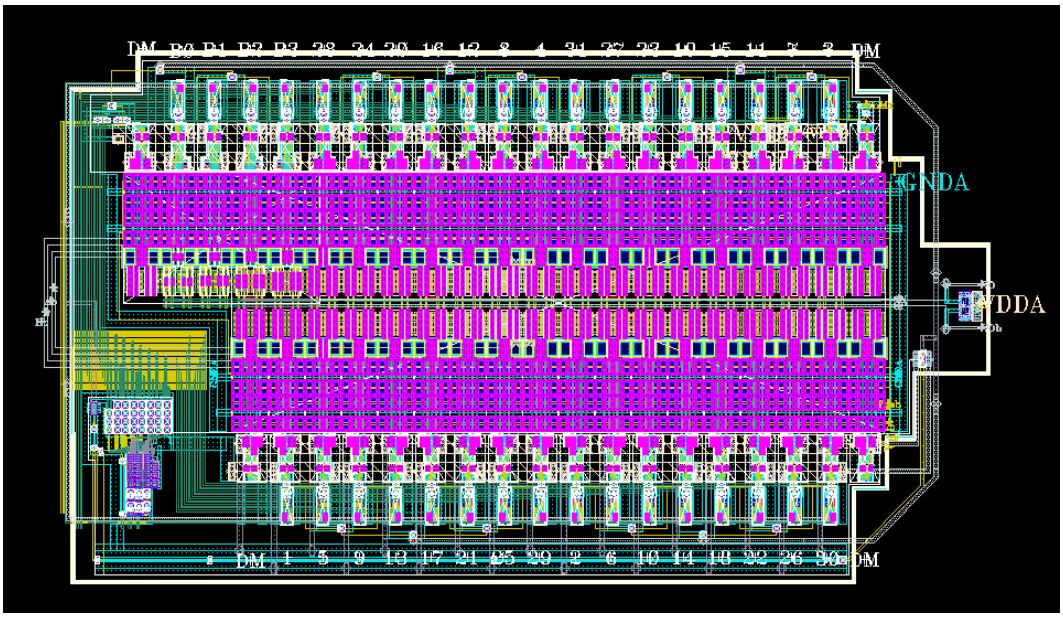

Figure 3.6: Phase Interpolator Layout

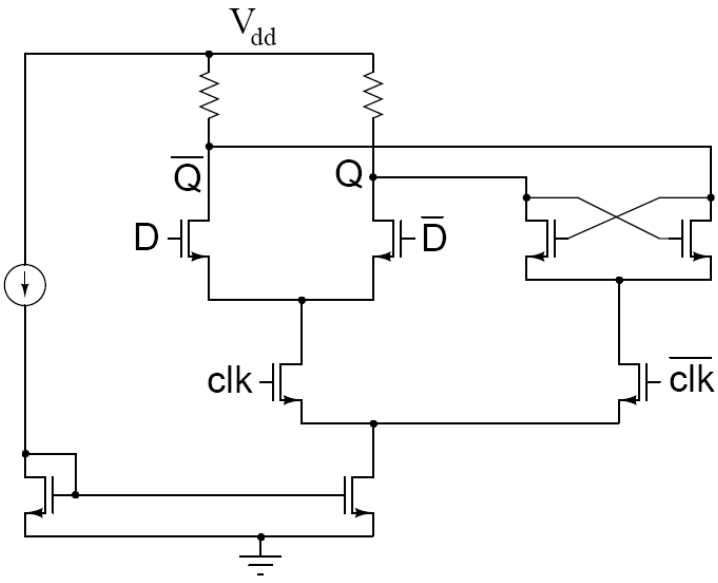

Figure 3.7: Basic CML Latch

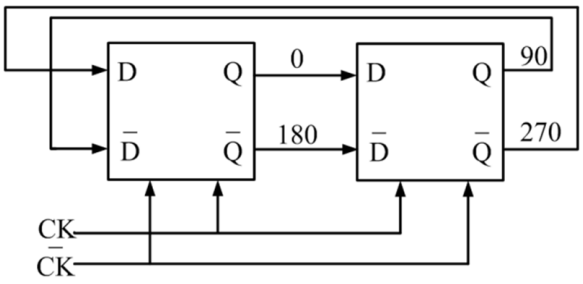

Figure 3.8: CML Divide-by-2 Stage

power consumption, the dynamic operation of the high-speed divider circuit has to be carefully looked at as shown in [28]. Each CML latch in the 10GHz to 5GHz divider, which is designed to operate up to 20GHz input consumed 5mA of current from a 1V supply. The latches in the subsequent stages consume about half that of the previous stage due to halving of the output frequency. Hence the latches in the 5GHz to 2.5GHz divider and 2.5GHz to 1.25GHz divider consume 2.5mA and 1.25mA respectively. The layout of the divider chain is shown in Fig. 3.9 and the outputs at various stages of the divider chain after post-layout extraction is shown in Fig. 3.10.

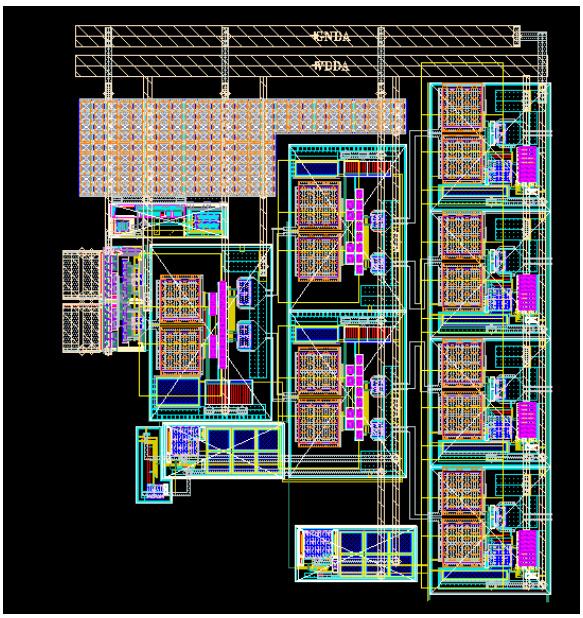

Figure 3.9: Divider Chain Layout

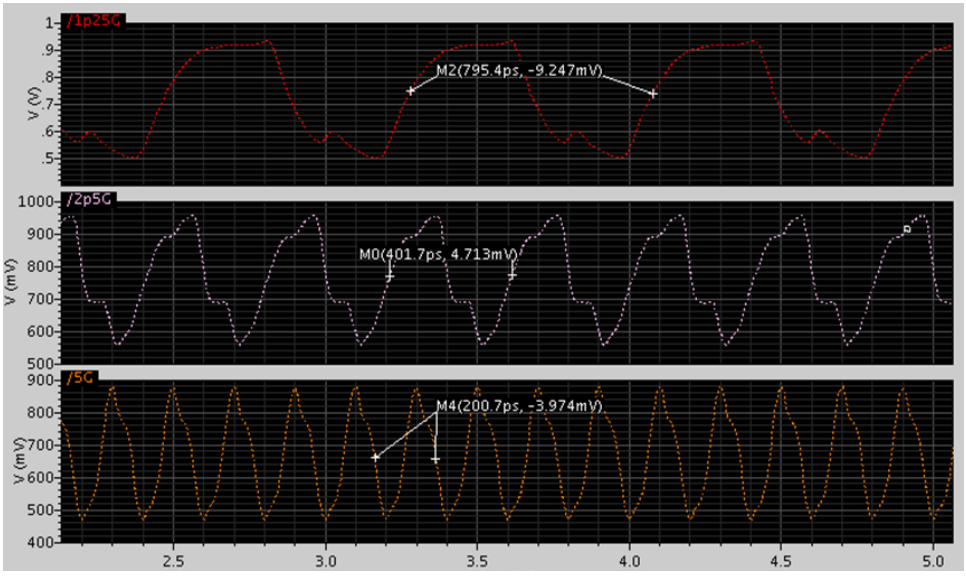

Figure 3.10: Divider Chain Output

3.2.3 Octant Phase Interpolation

The octant phase interpolation is done using two 8-to-1 MUXs which generate the signals X_1 and X_2 for the 9-bit phase interpolator. The MUX consists of 8 differential pairs, which are driven by the 8 differential signals corresponding to the octant phases as shown in Fig. 3.11. The tail current is switched into one of these differential pairs based on switches which are enabled based on the 3-bit MSB of the phase select digital data. Limited amplitude control is achieved at the output of the MUXs using tail current control which is primarily used for amplitude control over PVT.

3.2.4 Amplitude and Phase Control Buffers

The amplitude at the input of the 8-to-1 MUX and the 9-bit phase interpolator affects the linearity achieved by these blocks. The 8-to-1 MUX performs better with a higher swing at its input. Figure 3.12 shows the variation of the DNL at an 8-bit level introduced at the MUX output for various input amplitudes. In

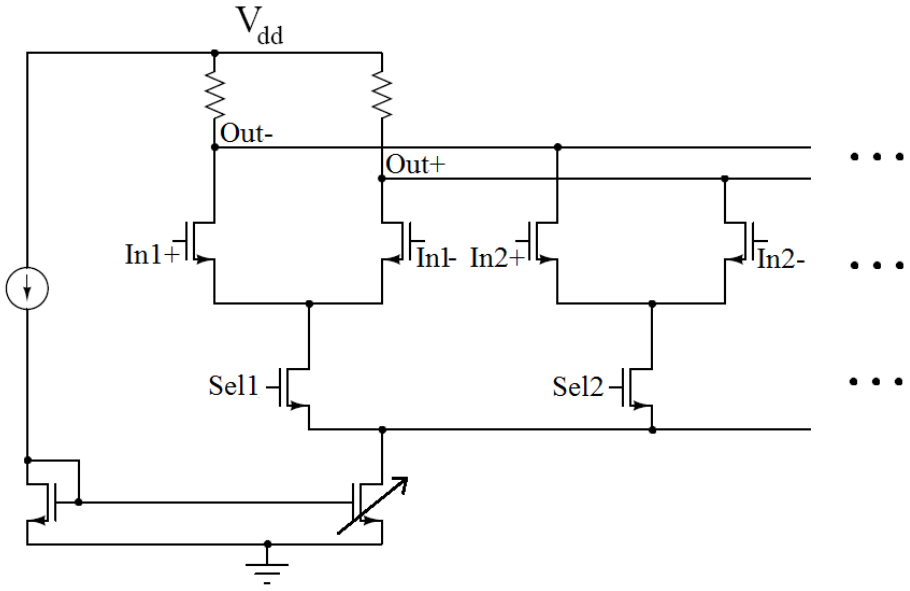

Figure 3.11: CML 8-to-1 MUX

case of the 9-bit interpolator, the linearity improves with a lower swing due to the nature of the phase interpolation operation being smoother with a lower slope in the input waveforms. As seen in Fig. 3.13, the DNL at an 8-bit level improves with lower input amplitude. Hence amplitude control, especially over PVT is crucial for linearity. Amplitude control buffers, which are essentially differential pairs with tail current control as shown in Fig. 3.14 precede both these critical blocks.

The presence of parallel paths means the phase of the waveforms at the inputs of the MUXs may vary due to mismatches and layout errors. These can lead to large phase jumps at the octant boundaries in the phase modulator output. To alleviate this problem, the phase variation is alleviated using phase tuning buffers before the MUXs. By varying the capacitive loads at the outputs of differential pairs as shown in Fig. 3.15, slight changes in output phase is achievable. Cascading many such stages allows enough range in phase tuning to compensate for expected mismatches. However this case lead to amplitude imbalances in the output which is reduced by stages of amplitude control buffers after phase tuning.

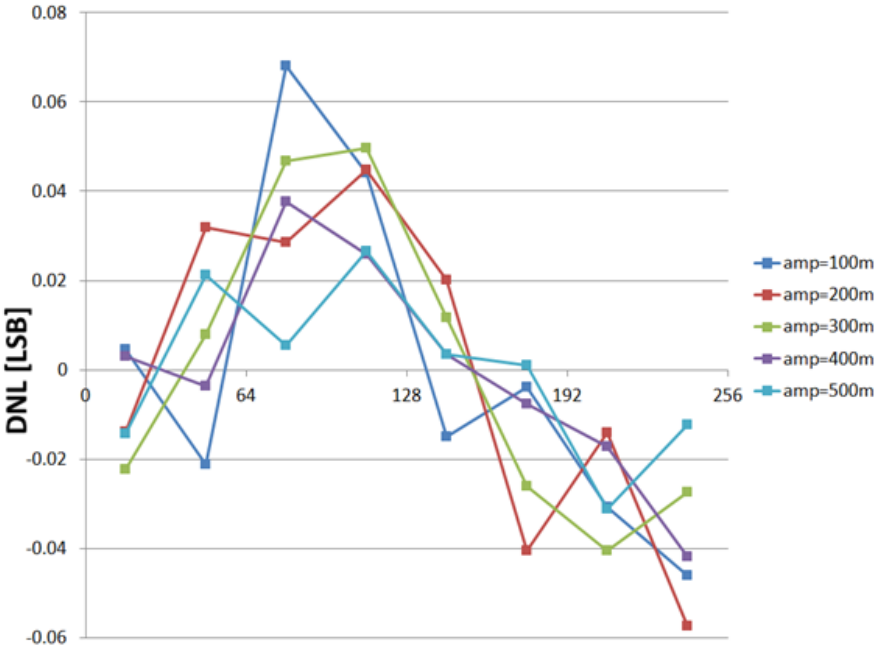

Figure 3.12: 8-to-1 MUX DNL vs. Input Amplitude

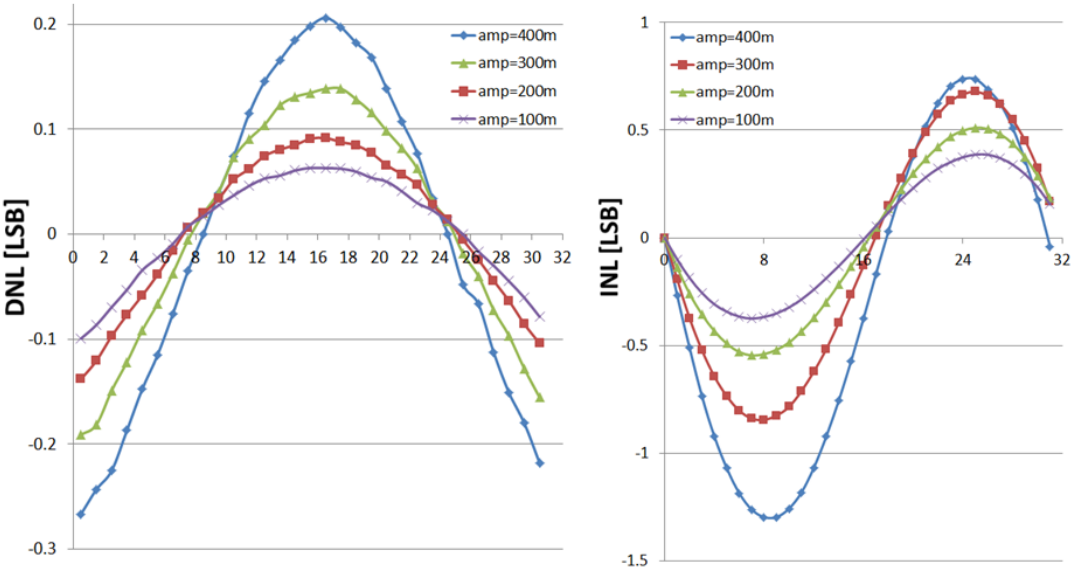

Figure 3.13: Phase Interpolator Linearity vs. Input Amplitude

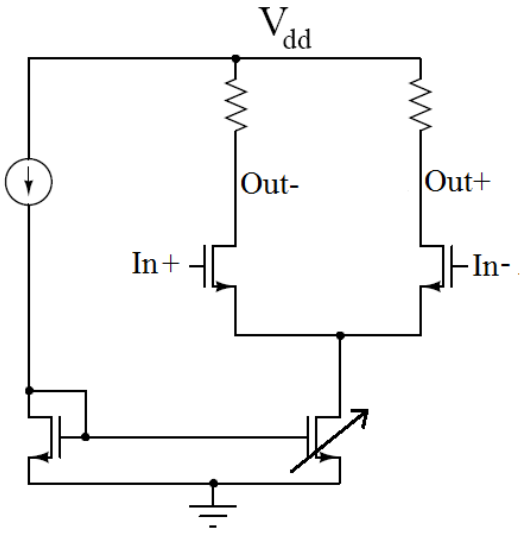

Figure 3.14: Amplitude Control Buffer

Figure 3.16 shows the output of a chain of five phase tuning buffers in series for different codes. Each phase step is about 4ps for a total phase control range of about 60ps.

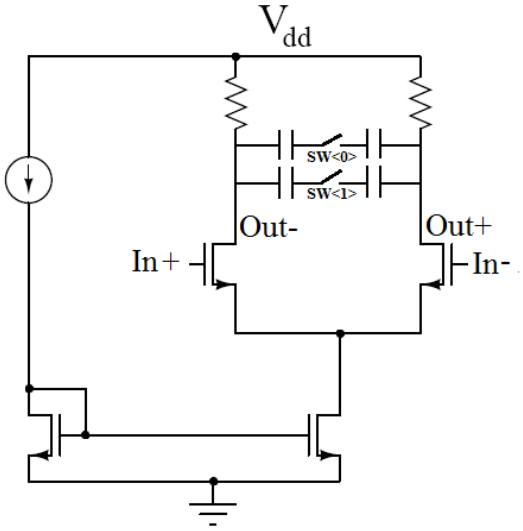

Figure 3.15: Phase Tuning Buffer

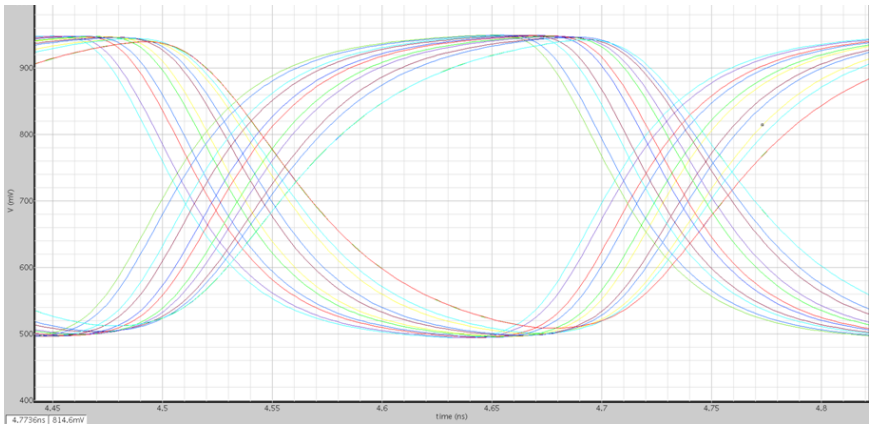

Figure 3.16: Phase Tuning Buffer Chain Output

3.2.5 CML-to-CMOS Level Converter

The phase interpolator output is converted to CMOS levels before it drives the output buffer chain. The linearity of this converter is extremely important to preserve the overall linearity of the system. The converter consists of a moderate gain differential pair followed by inverters with resistive feedback which provides enough gain to convert the differential signal to two pseudo-differential outputs at CMOS levels which drive the output buffer as shown in Fig. 3.17. The output of the converter for various phases at its input is shown in Fig. 3.18. To ensure that the output of the converter has 50% duty cycle over PVT, the size of the NMOS device can be varied. This is necessary to allow for accurate phase modulation at lower frequencies.

3.2.6 Phase Modulation at Lower Carrier Frequencies

To allow for the phase modulated output to be at carrier frequencies which are binary fractions of 1.25GHz, the architecture in Fig. 3.19 is used. The code words to the various MUXs being used is obtained from the MSBs of the digital phase selection code to the phase modulator while the LSBs are passed to the main 12-bit phase modulator. Hence, for example to obtain 12-bit phase modulation at

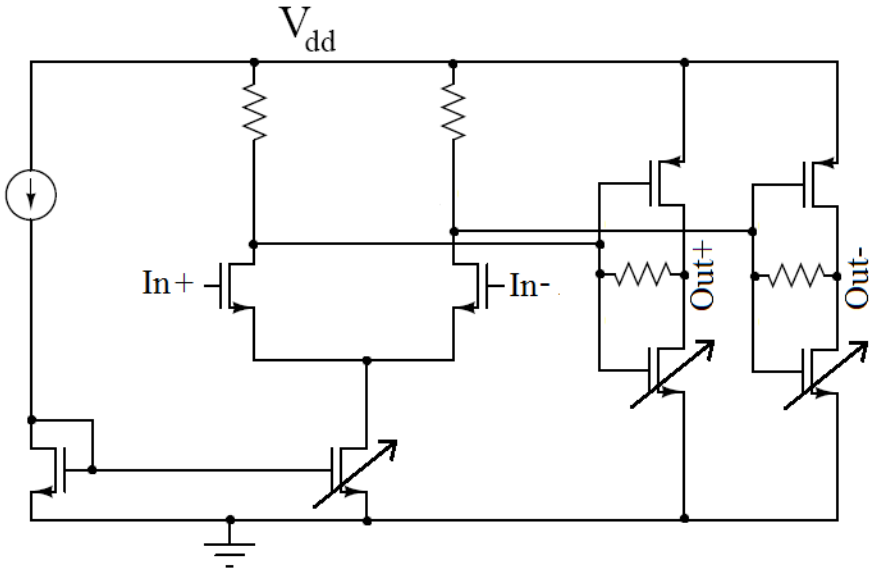

Figure 3.17: CML-to-CMOS Level Converter

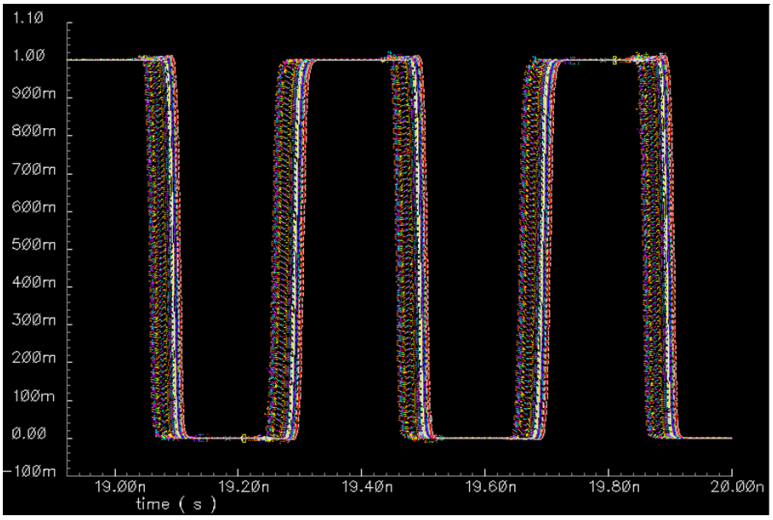

Figure 3.18: CML-to-CMOS Level Converter Output

312.5MHz, the 2 MSBs are used to select between the divided phase modulator outputs and their complements, while the 10 LSBs are used as the 10 MSB bits in the 12-bit phase modulator, while setting its 2 LSBs to 0.

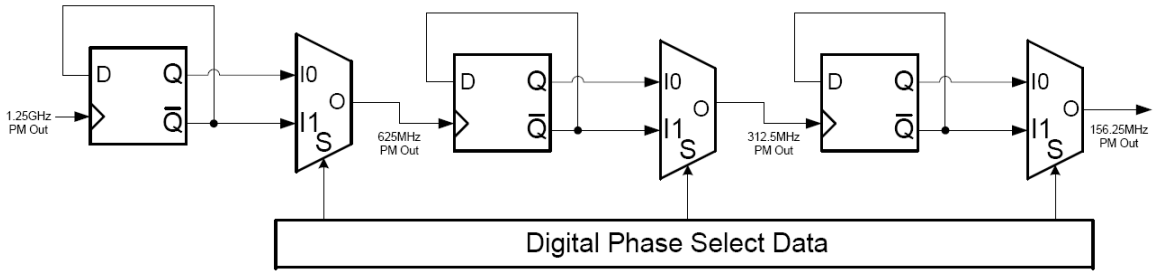

Figure 3.19: Phase Modulation at Lower Carrier Frequencies

3.2.7 Output Buffer Chain

The output buffer consists of a 3.3V inverter chain preceded by a 1V to 3.3V level converter as shown in Fig. 3.20. The buffer was designed to drive 10pF of load at 1.25GHz output frequency and its layout is shown in Fig. 3.21.

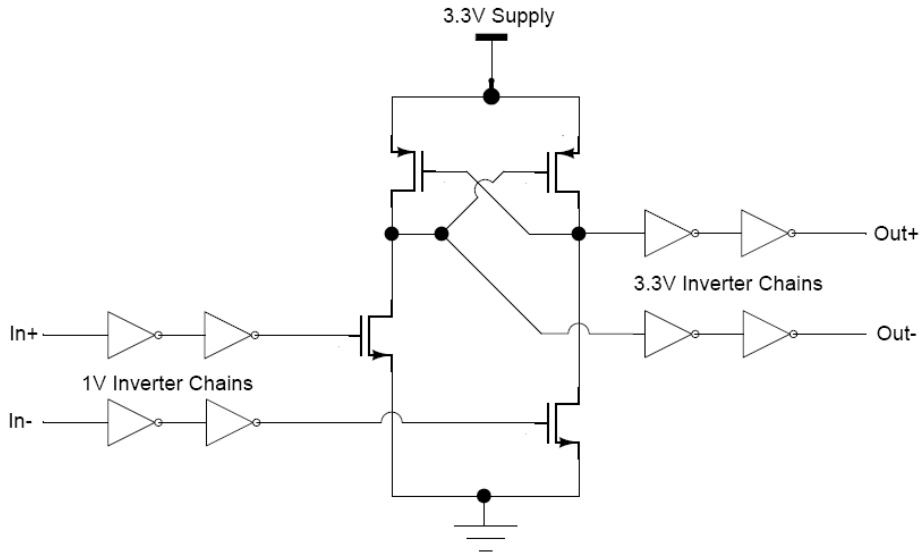

Figure 3.20: Output Buffer Chain

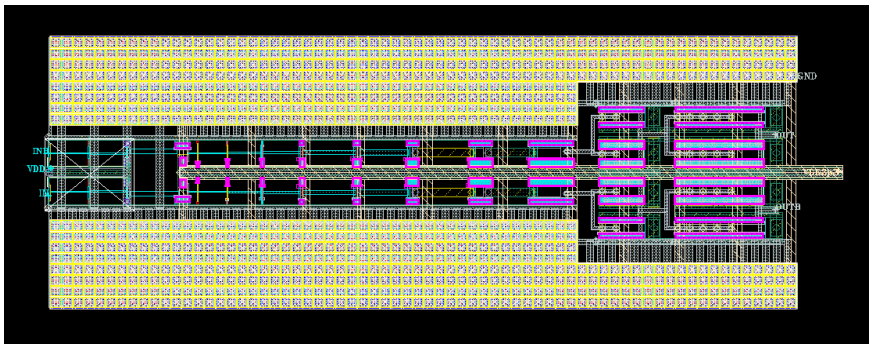

Figure 3.21: Output Buffer Chain Layout

3.3 IC Layout

The phase modulators were designed as part of a larger system which required five such phase modulators driven by a common multi-phase carrier generation divider chain. The divider chain input was selectable between an on-chip 10GHz PLL output and an external source. The layout of the phase modulators and ancillary circuitry in the chip is shown in Fig. 3.22.

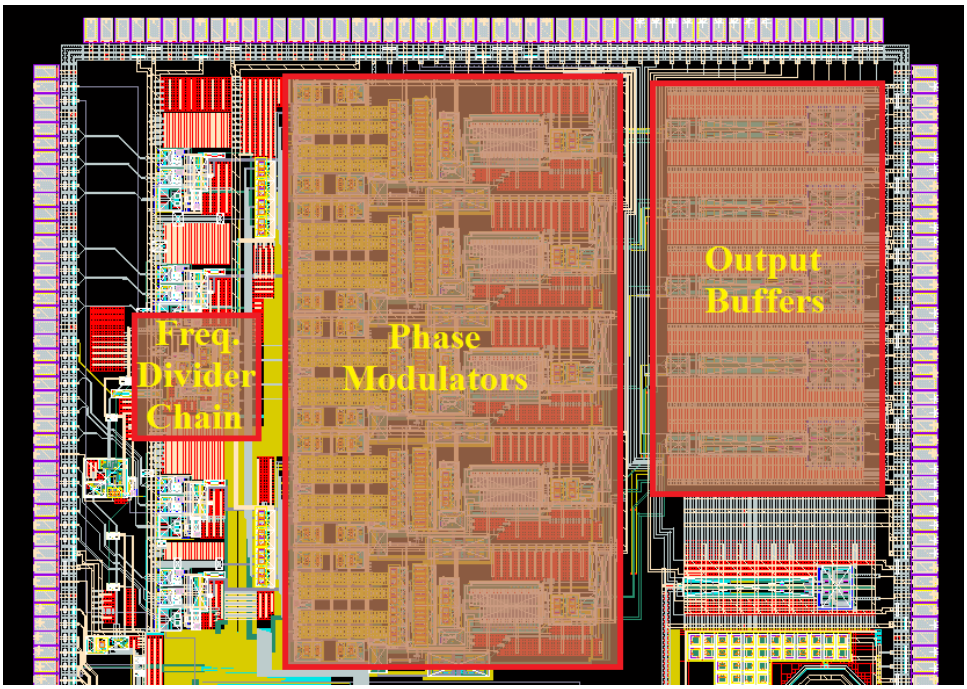

Figure 3.22: IC Layout

CHAPTER 4

Testing and Measurement Results

4.1 IC Characteristics

The IC designed in 65nm CMOS process was fabricated by TSMC. The chip micrograph is shown in Fig. 4.1. The IC contains 5 phase modulators driven by a common multi-phase carrier generator which can accept a 10GHz carrier signal from an on-chip PLL or from an external source.

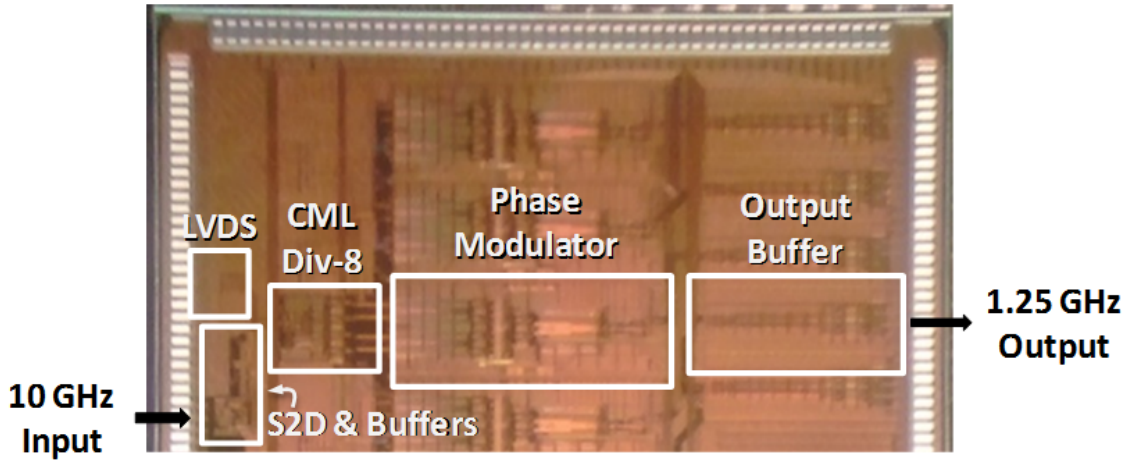

Figure 4.1: Chip Micrograph

The IC was mounted on a PCB using the chip-on-board (COB) technique, thus avoiding a package. The measurement setup is shown in Fig. 4.2. For setting various calibration bits, an on-chip USART was used which was programmed through a laptop with MATLAB.

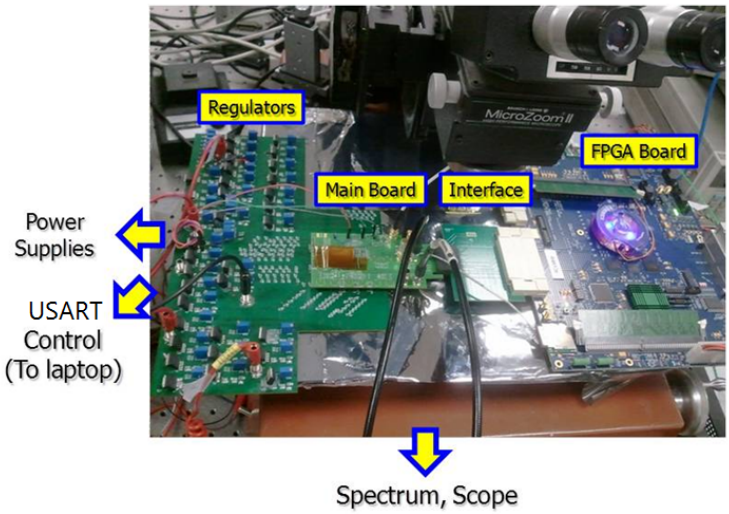

Figure 4.2: Measurement Setup

4.2 Static Characteristics of the Phase Modulator

The major static measurements required to characterize the IC are:

- The static non-linearity curve of the phase modulator.
- The phase noise at the phase modulator input and output.
- The DC power consumption of the circuit.

4.2.1 Non-linearity

For measuring the static non-linearity curve, i.e. the DNL of the phase modulator, the phase modulator input code was set to a constant value using the USART and the phase of the output was measured. By sweeping the input code and measuring the corresponding output phase, the DNL of the phase modulator with code was obtained. Due to limitations of the test equipment, only 9 MSBs of the input code was swept. The output phase was measured using the Tektronix TDS6154C oscilloscope. An example output waveform is shown in Fig. 4.3(a) and the output spectrum is shown in Fig. 4.3(b). As seen from the output spectrum, the main

tone at 1.25GHz is at least 50dB above any other spurious tones in the output.

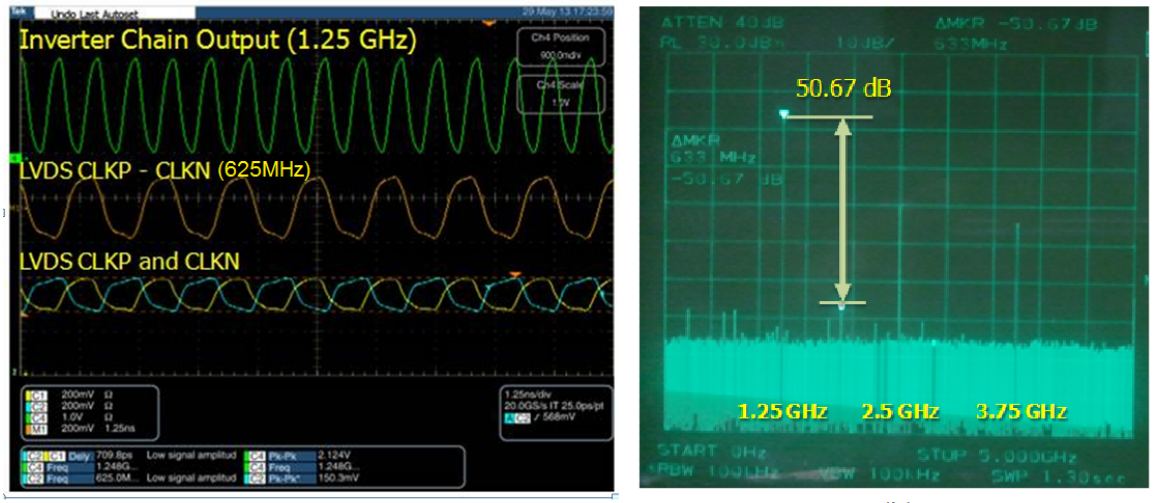

Figure 4.3: Phase Modulator and LVDS Clock Outputs

The measured DNL characteristic of the phase modulator is shown in Fig. 4.4(a). A full octant (64-phase) and transition point between 1st and 2nd octants were measured because DNL performance will be repeated in each octant. The worst-case DNL is measured at the octant transition points as expected and the DNLs are 2 and -14 LSB at codes of 64 and 128, respectively.

The 9-bit measurement was then used to achieve 8-bit linearity by selecting a 9-bit code which gave the required output phase for an 8-bit input, thus pre-distorting the input of the phase modulator. This improves the linearity of the phase modulator with DNL reduced to below 0.5 LSB as shown in Fig. 4.4(b).

4.2.2 Noise Performance

The phase noise spectrum of the 10GHz carrier input and 1.25GHz output of the phase modulator for a constant digital code were measured using a spectrum analyzer to measure the maximum phase resolution achievable by the phase modulator. Figure 4.5(a) and Fig. 4.5(b) show the phase noise spectrum at the input

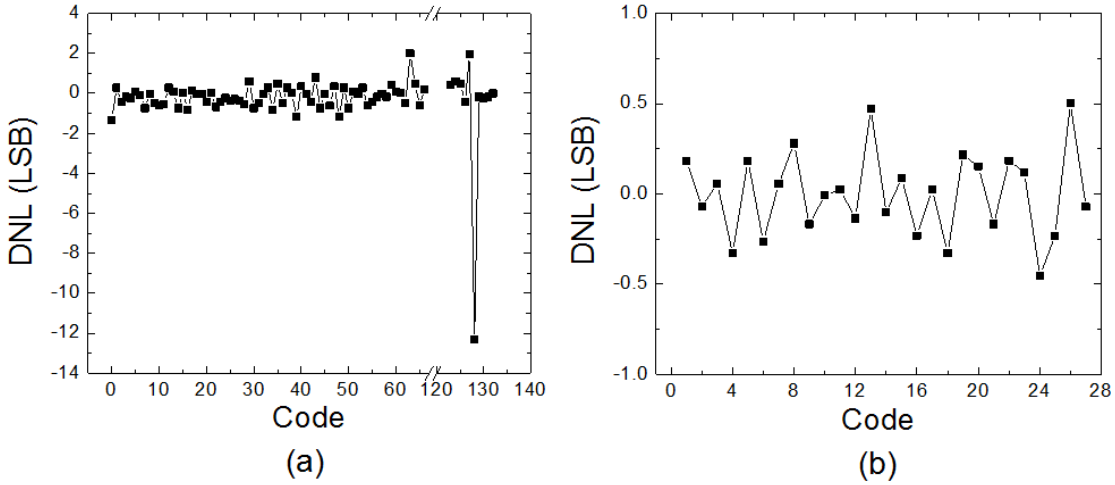

Figure 4.4: Measured DNL of the Phase Modulator (a) Before Pre-distortion and (b) After Pre-distortion

and output, respectively, of the phase modulator.

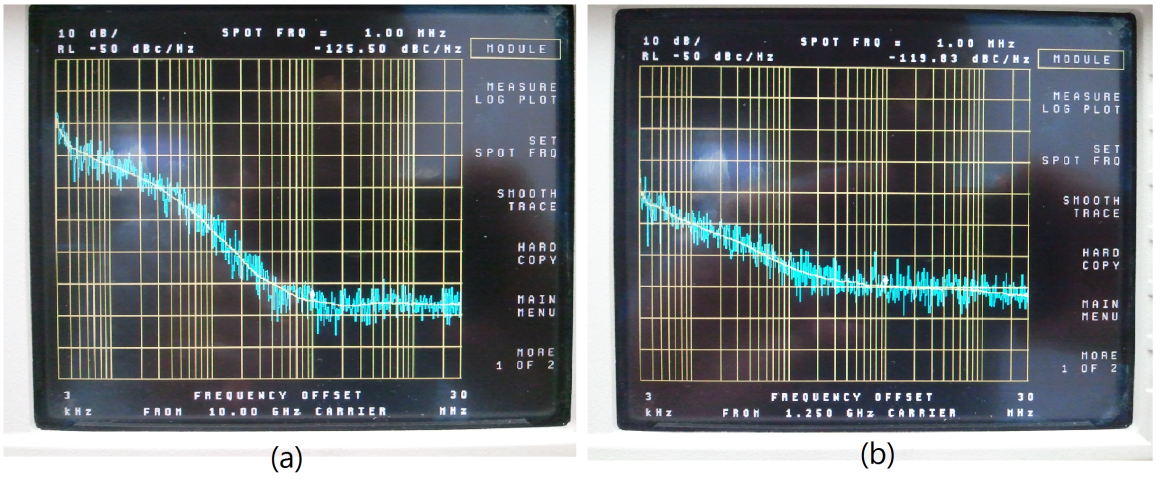

Figure 4.5: Phase Noise Spectra of the Phase Modulator (a) Input and (b) Output

Figure 4.6(a) and Fig. 4.6(b) show the integrated phase noise again at the input and output, respectively. From the integrated phase noise, the effective resolution achievable at the output of the phase modulator is given by $.4061^0$ which corresponds to an ENOB=$20log_{10}(360/.4061) = 59dB = 9.5$ bits.

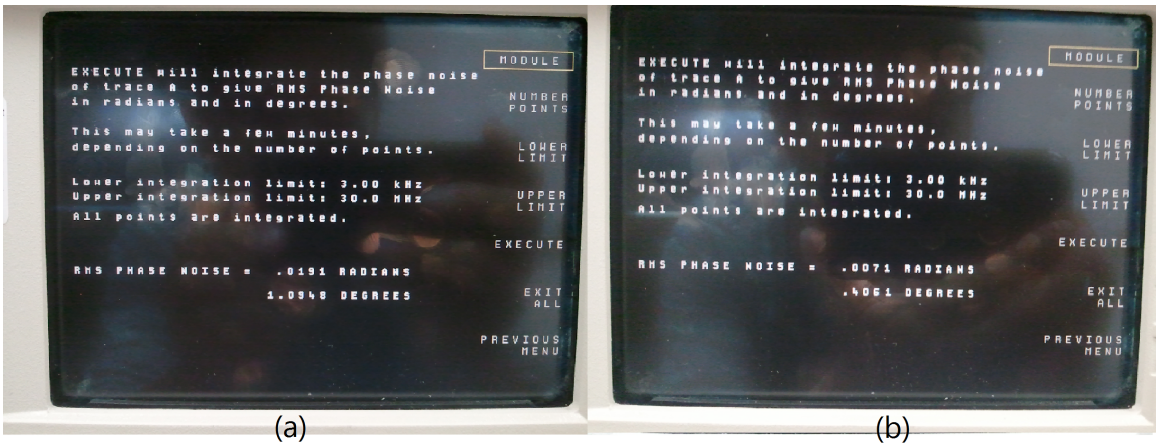

Figure 4.6: Integrated Phase Noise of the Phase Modulator (a) Input and (b) Output

4.2.3 Power Consumption

Current consumption of a single phase modulator, which includes octant interpolator, sub-octant interpolator, and output differential-to-single converter, is 22.5mA from 1.2V supply (27mW power consumption). Input CML divider chain consumed 10mA from 1.2V supply. The output stage inverter chain consumes 100mA from 3.3V supply.

4.3 Dynamic Characteristics of the Phase Modulator

To measure the dynamic performance of the phase modulator, pre-distorted digital data was generated from a Xilinx Virtex 5 based FPGA called ROACH [29] which allows programming using a Simulink interface. An example program to generate 8PSK data with pre-distortion is shown in Fig. 4.7.

The ROACH generates two differential outputs at up to 200MS/s through its ZDOK connectors which are received at the chip and then decoded and demultiplexed to 12 bits of phase control digital data. Hence the data rate at the phase modulator is 1/6th that of the FPGA.

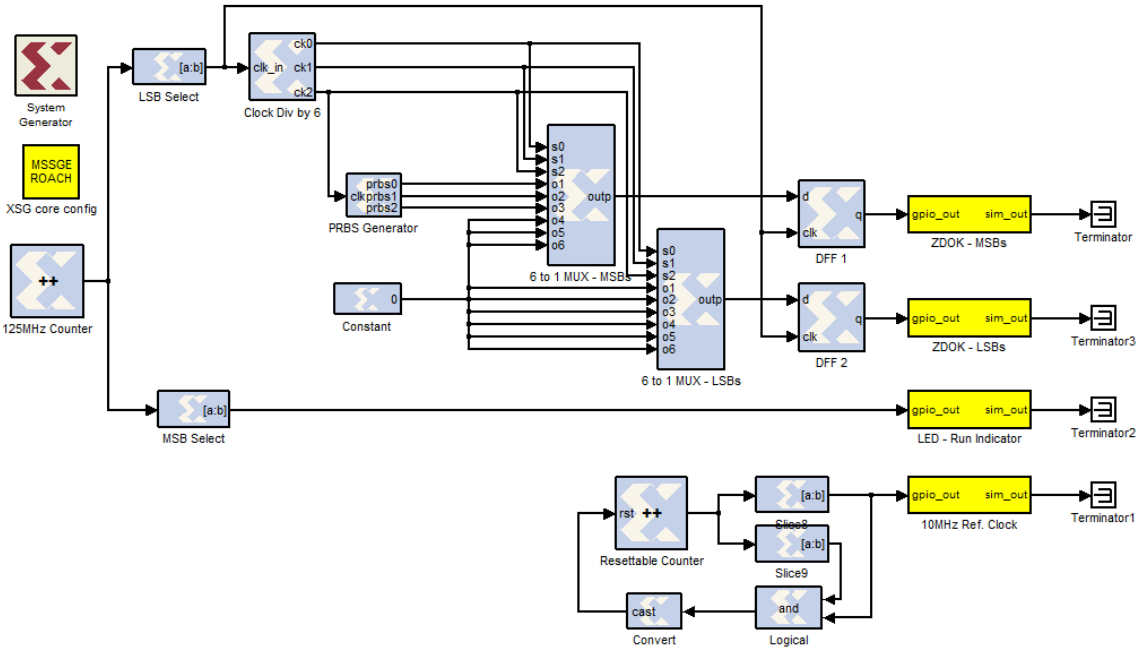

Figure 4.7: ROACH Setup for Generating 8PSK Data

To synchronize the FPGA and the phase modulator clocks, the 10MHz reference clock for carrier generation for the phase modulator has to be derived by dividing the FPGA system clock by an integer fraction. Since the demultiplexer clock is generated by dividing down the 1.25GHz carrier input of the phase modulator, the ROACH clock rate has to be obtained by a integer division of 1.25GHz. Hence the fastest FPGA clock rate that could be used was 125MS/s which means the fastest modulation bandwidth achievable was 125/6=20.83MS/s. For an 8PSK modulation input to the phase modulator, the output spectrum obtained is shown in Fig. 4.8.

The time domain output for a BPSK modulation input is shown in Fig. 4.9 and its demodulated constellation is shown in Fig. 4.10. The achieved error vector magnitude (EVM) is about -22.6dB.

Similarly, the time domain output for an 8PSK modulation input is shown in Fig. 4.11 and its demodulated constellation is shown in Fig. 4.12. The achieved

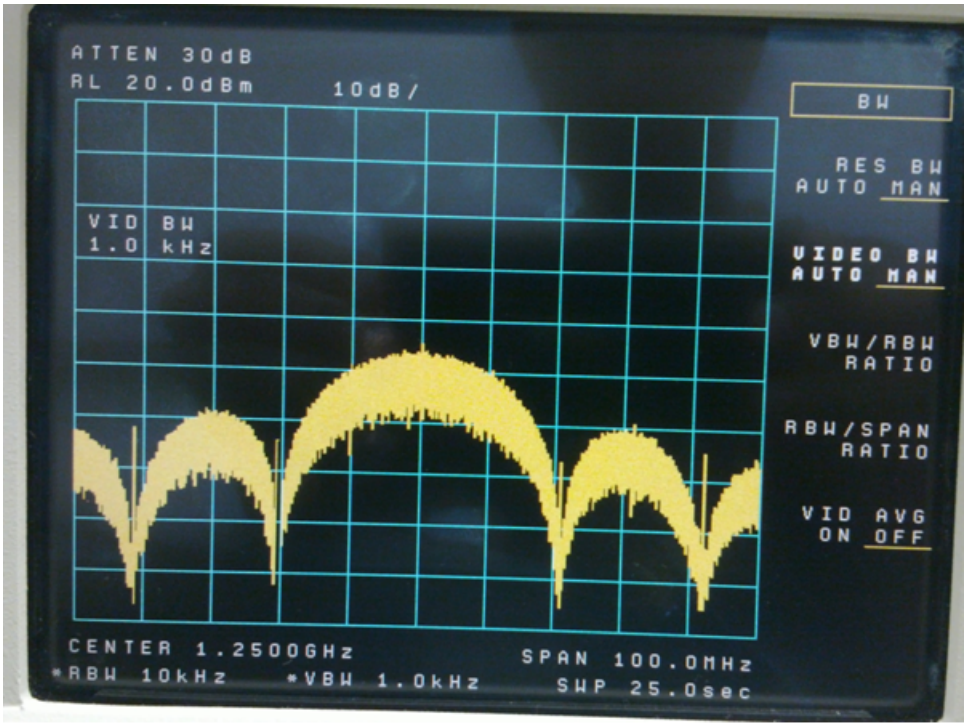

Figure 4.8: Measured Spectrum of 8PSK Modulated Output

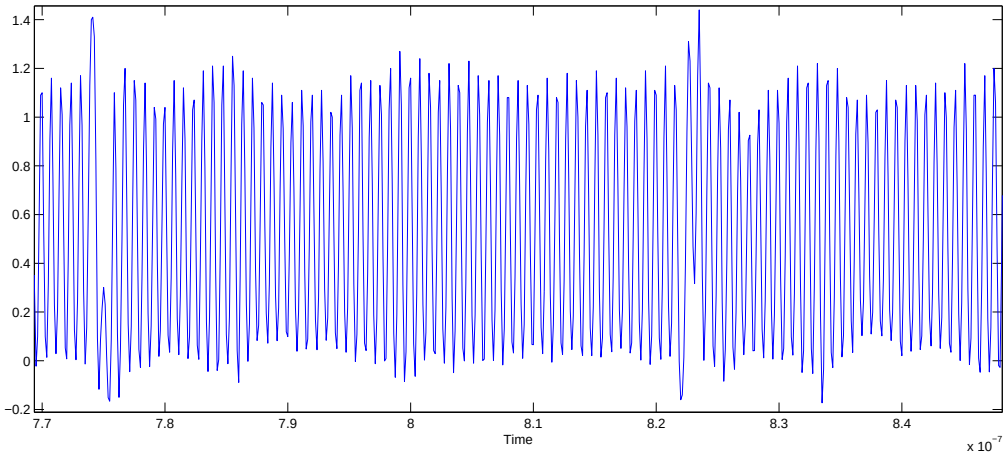

Figure 4.9: BPSK Modulated Output

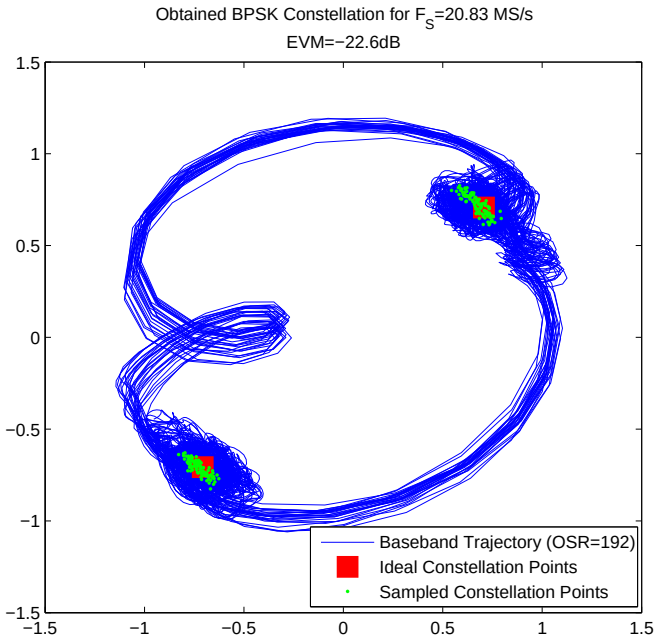

Figure 4.10: Demodulated BPSK Constellation

is about -16.6dB.

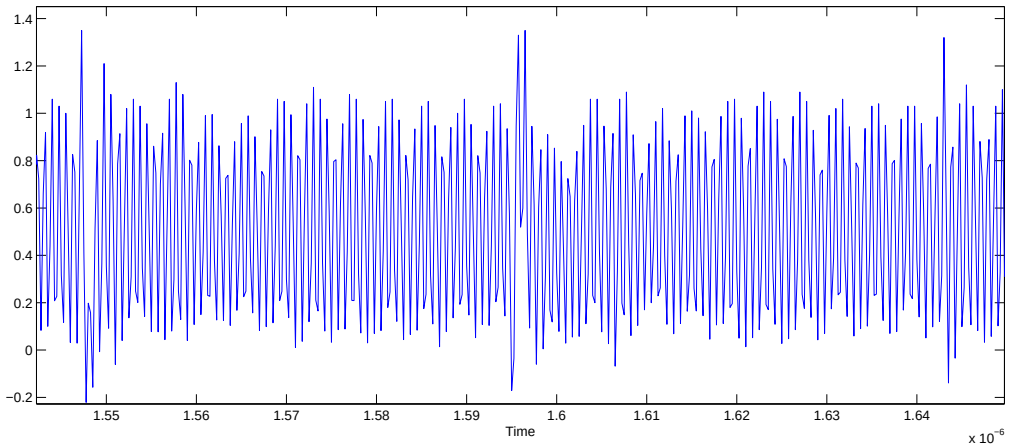

Figure 4.11: 8PSK Modulated Output

The achieved EVM is largely limited by the large supply and ground bounce on the output inverter buffer chain caused by unwanted but avoidable problem of switching in the output buffer, especially after a phase change which limits

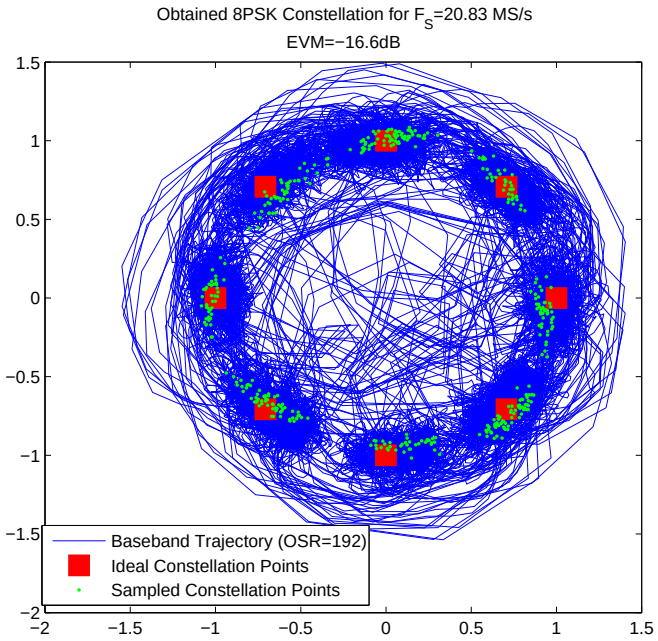

Figure 4.12: Demodulated 8PSK Constellation

achievable bandwidth at a good EVM. The performance could be improved by using a differential output buffer instead of a hard switching buffer such as an inverter chain.

CHAPTER 5

Modeling of Split-band Envelope Modulation

Wide bandwidth envelope modulation at high efficiency is a significant problem. Wide bandwidths of the order of hundreds of MHz with high dynamic range is prohibitively power hungry and inefficient with supply modulators. Supply regulation using switching DC-DC converters such as buck converters is highly efficient only to about a few MHz of bandwidth [11, 12] and performance degrades for higher bandwidths due lower switching efficiency and noise. Higher classes of supply modulators exist but are limited to a few tens of MHz of bandwidth. Other ways of modulating the envelope signal, such as duty cycle modulation of the driving waveform in a switching PA [13] have typically high bandwidths and techniques such as contour modulation [14] help with improving efficiency under back-off but still are limited in dynamic range.

5.1 Split-band Envelope Modulation

Split-band envelope modulation is proposed as a solution to this problem. In this scheme, the envelope signal is split into different bands to be handled by highly optimized solutions for each band. For example, the envelope signal within a bandwidth of a few MHz can be applied through a high-efficiency buck converter [16] or Class-S supply modulator while the higher bandwidth envelope modulation can handled by a linear power amplifier as in Fig. 5.1 [15] or duty cycle modulation in a switching amplifier. Appropriate choice of the bands should result in higher efficiency and comparable performance with respect to a single block designed

to handle the entire envelope signal [30]. This becomes even tougher when the number of parallel paths in the envelope modulator is more than two.

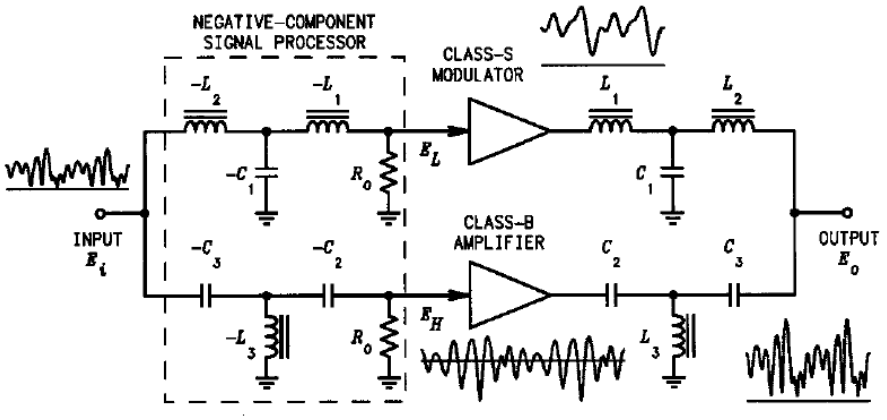

Figure 5.1: Split-band Envelope Modulation

5.2 Model for Split-banding

To look at aspects related to efficiency and dynamic range from a system level, a model was created in MATLAB/Simulink which is shown in Fig. 5.2. The input data (which is randomly generated) is first passed through a QAM constellation before applying pulse shaping using a Gaussian filter. For example, a QAM16 signal at 100MS/s is up-sampled 10 times and filtered by a Gaussian filter with a BT product of .64 which gives an EVM of -34dB at the output while suppressing out-of-band spectral content as shown Fig. 5.3.

The pulse-shaped output is converted into polar form with the phase data being handled by a wideband phase modulator. As for the envelope path, it is split into three segments using Gaussian filters. For example, when the BT products of the low band and mid band Gaussian filters are set to .0032 and .032, respectively, the spectra of the various output bands are shown in Fig. 5.4. The spectrum of the final PA output with an ideal phase modulator is shown in Fig. 5.5.

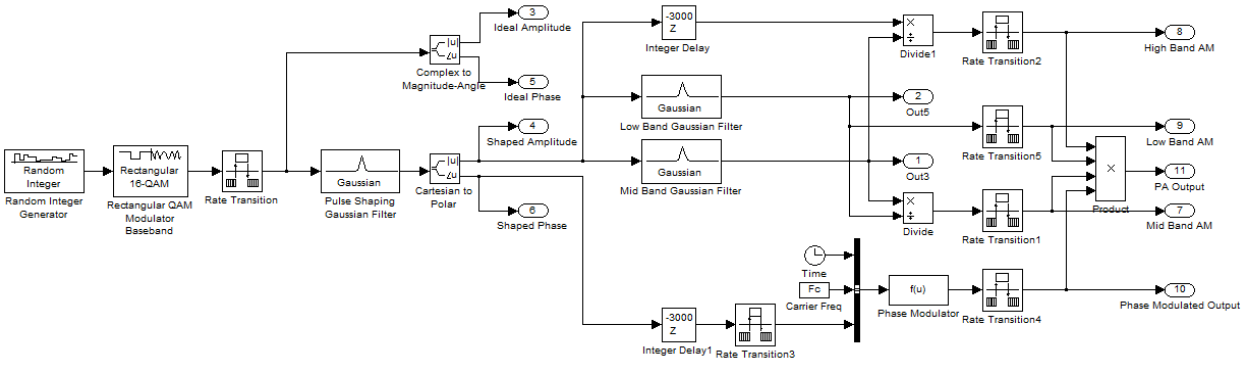

Figure 5.2: Simulink Model for Split-band Envelope Modulation

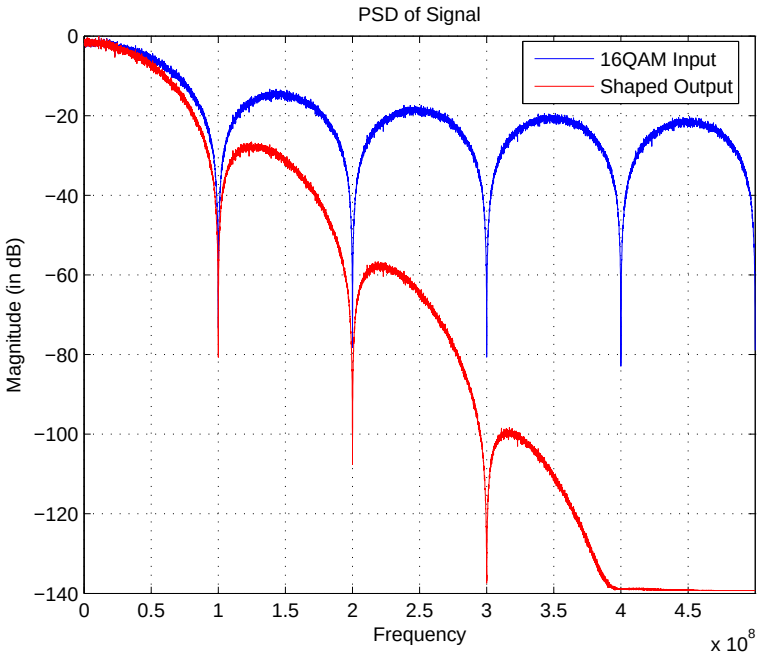

Figure 5.3: PSD of Shaped 16QAM Output

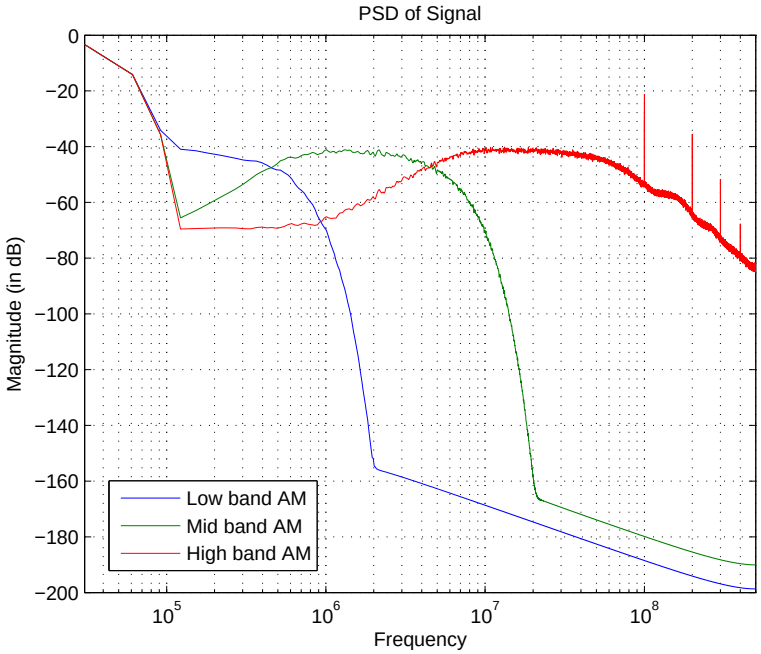

Figure 5.4: PSD of Split-band AM Outputs

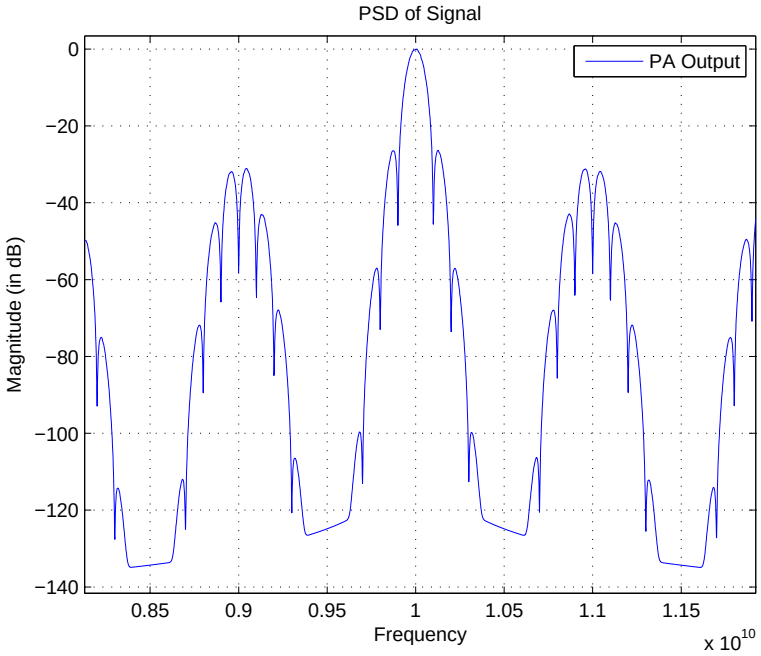

Figure 5.5: PSD of Final PA Output

5.3 System Trade-offs

This model can be used to evaluate the dynamic range requirements for each of the paths given constraints on EVM. For example, in one set of simulations, the low band filter BT product is kept constant at .0032 and the mid band filter BT product is set as $.032\alpha$. By varying α, the bandwidth handled by the mid band and high band envelope modulators are varied. Figure 5.6 and Fig. 5.7 shows the effect of varying α on the peak-to-average power ratios (PAPR) and peak-to minimum power ratios (PMPR) of the mid and high band envelope modulators, respectively. Figure 5.7 shows up the interesting result that the PAPR and PAMR of the high band signal increases for a certain range when the bandwidth handled by that path is reduced (i.e. α is increased).

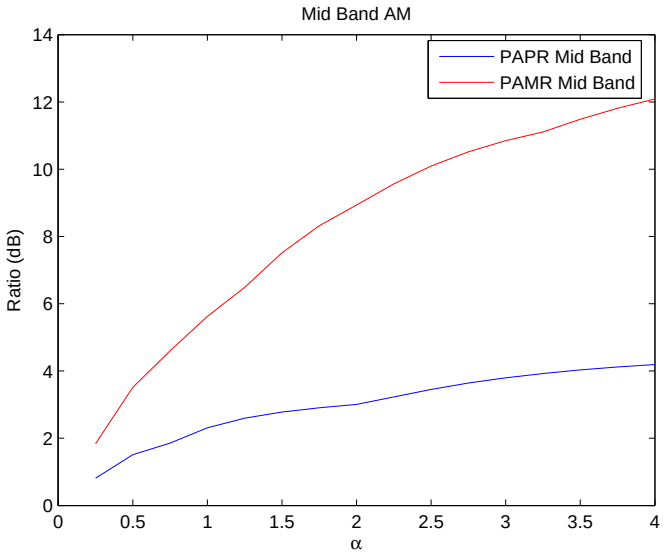

Figure 5.6: PAPR and PAMR of Mid Band AM Signal

The limited dynamic range of various blocks can be modeled as clipping in its output. In Fig. 5.8, the dynamic range of the high band modulator is fixed to some value and the output EVM is plotted with varying α. The result follows as an outcome of Fig. 5.7 with EVM worsening for a certain range even if the bandwidth handled by that path is reduced (i.e. α is increased). This seems to

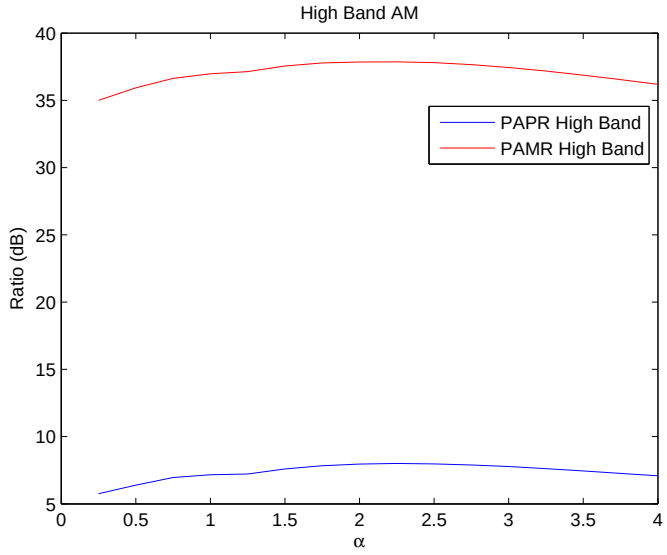

Figure 5.7: PAPR and PAMR of High Band AM Signal

suggest that frequency band based signal division is not the ideal way to process the envelope signal if the dynamic range of certain blocks are limited.

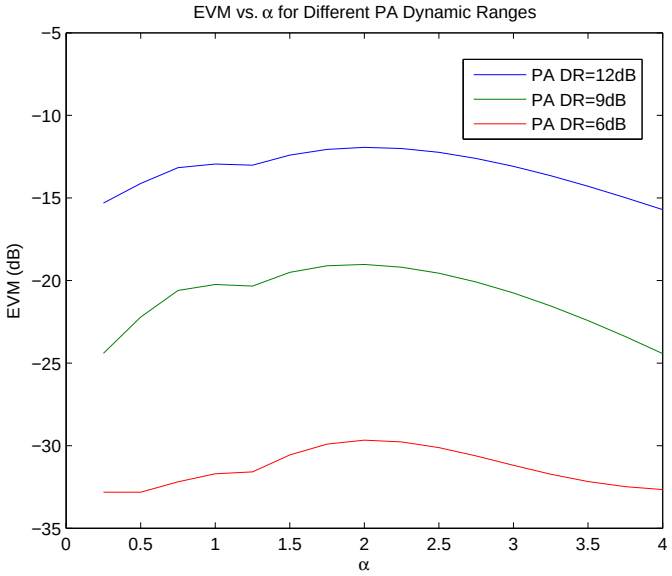

Figure 5.8: Variation of EVM vs. PA Dynamic Range

Such plots show how design decisions can be made in a split-band system. Efficiency of each path is a function of the input. Hence a simple one-dimensional

look-up-table (LUT) can be used to find instantaneous efficiencies and hence average efficiency. In case different blocks impact efficiencies of each other, multi-dimensional LUTs may be required. Hence efficiency can be factored into design decisions.

CHAPTER 6

Conclusion

6.1 Summary

In this thesis, an open-loop phase modulator was designed with the aim of achieving wideband phase modulation on a 1.25GHz carrier signal. A prototype IC implementing the designed open-loop phase modulator was fabricated in 65nm CMOS process.

Table 6.1: IC Performance Summary

Technology	TSMC 65nm CMOS
Area	$300\mu m \times 300\mu m$(Frequency Divider Chain) $1000\mu m \times 300\mu m$/Phase Modulator Core
Core V_{DD}	1.2V
Core Current Consumption	10mA (Frequency Divider Chain) 22.5mA/Phase Modulator Core
Buffer V_{DD}	3.3V
Buffer Current Consumption	100mA/Chain
Carrier Frequency	1.25GHz
Max. Modulation Rate	20.83MS/s
EVM	-22.6dB (BPSK) -16.6dB (8PSK)

Table 6.1 summarizes the performance metrics measured. Table 6.2 compares this work with other published works on open-loop phase modulation. The results show that open-loop phase modulation is a viable architecture for wideband phase modulation.

Table 6.2: Comparison with Previous Work

Reference	[8]	[9]	This Work (Simulated)	This Work (Measured)
Process (nm)	180	180	65	65
Core Voltage (V)	1.4	1.8	1.0	1.2
Power (mW)	8.82	62.1	25	39
Area (mm^2)	0.47	2.5	0.39	0.39
EVM	4.1% (2FSK) 11.6% (GFSK)	7.6% (GFSK)	-	7.4% (BPSK) 14.8% (8PSK)
Carrier Frequency	380MHz	2.4GHz	2.5GHz	1.25GHz
Modulation Rate	6MS/s	60MS/s	125MS/s	20.83MS/s

A MATLAB/Simulink model was also developed to analyze some of the trade-offs in a split-band envelope modulated polar transmitter system and some interesting results were obtained as a result. Hence both the envelope and phase paths in a wideband polar transmitter were dealt with in this thesis.

6.2 Future Work

The performance of the CMOS IC was limited by the switching inverter chain output buffer chain. Hence, it is desirable to replace it with a differential output buffer to better measure the limitations of the phase modulator. An FPGA with a higher data rate will also be required to test such a setup.

The MATLAB/Simulink model can easily be extended to account for efficiencies of various blocks and their interdependencies. Moreover, to account for non-linearities, pre-distortion can also be performed to the inputs of each block, but requires detailed models for block-level performance.

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