UC San Diego

UC San Diego Electronic Theses and Dissertations

Title

W-band phased array systems using silicon integrated circuits

Permalink

https://escholarship.org/uc/item/8zz9v532

Author

Kim, Sang Young

Publication Date

2012

Peer reviewed|Thesis/dissertation

eScholarship.org Powered by the California Digital Library
University of California

UNIVERSITY OF CALIFORNIA, SAN DIEGO

W-band Phased Array Systems using Silicon Integrated Circuits

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Sang Young Kim

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor James Buckwalter
Professor Gert Cauwenberghs
Professor William S. Hodgkiss
Professor Lawrence E. Larson

2012

Copyright
Sang Young Kim, 2012
All rights reserved.

The dissertation of Sang Young Kim is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

_____

_____

_____

_____

_____

Chair

University of California, San Diego

2012

DEDICATION

To my parents, Jin Heung Kim and Jin Hwan Choi,
and my brother and sister-in-law, Jae Young Kim and YoonMi Lee.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

First and foremost, I would like to sincerely thank my dissertation advisor Prof. Gabriel M. Rebeiz for his guidance and unlimited technical and moral support throughout my doctoral studies at University of California, San Diego (UCSD). His questing mind and endless enthusiasm for the research always inspired me and those were the strong motivation in my research whenever I fell into a slump. With his very well-maintained state-of-the-art labs and his expertise in the fields of the electro-magnetic wave, antenna and wireless communication, and remarkable insight on the phased arrays provided the best environment for top-notch research and the most efficient experiments and measurements. I learned so much from him - not only the academic lessons, but also valuable life lessons I will cherish for the rest of my life. Without his advice and support, all this work could not be finished. It was a great pleasure to know him and work with him, and it is a great honor for me to be one of his students.

Next, I would like to thank my dissertation committee members, Prof. Lawrence E. Larson, Prof. James Buckwalter, Prof. Gert Cauwenberghs and Prof. William S. Hodgkiss for their time, interest, and valuable comments. The distinguished faculty is the strongest driving force that makes UCSD one of the top engineering school in the world.

I would like to thank Dong-Woo Kang, Kwang-Jin Koh, Ozgur Inac, Choul-Young Kim and Donghyup Shin for their contribution to the work in this thesis. Additionally, I must thank my fellow graduate students for their support and friendship. My thanks go to all of the TICS group including Byung-Wook Min, Jeonggeun Kim, Bonhyun Ku, Yusuf Atesal, Berke Cetinoneri, Woorim Shin, Jason May, Sang-June Park, Michael Chang, Tiku Yu, Chris Galbraith, Carson White, Balaji Lakshminarayana, Mohammad El-Tanani, Isak Reines, Alex Girchner, Jung-Mu Kim, Ramadan Alhalabi, Chirag Patel, Kevin Ho, Mehmet Uzunkol, Jennifer M. Edwards, Yu-Chin Ou, Yi-Chyun Chiou, Chih-Chieh Cheng, Dr. Rashed Mahameed and Hojr Sedaghat Pisheh, Fatih Golcuk.

My special and deepest appreciation go to my family to whom I owe so much. Completing my PhD would not have been possible without support and encouragement of my family. My parents, Jin Heung Kim and Jin Hwan Choi, have always inspired me as spiritual mentors. I know that they are always there whereever/whenever I need them. I can never forget their support, dedication and never-ending love throughout my life. My elder brother, Jae Young Kim, is the reliable buttress of our family inspiring us all. And brother's wife, YoonMi Lee, I really appreciate her great support and careful concern. Without my family this work would have never existed, I would like to express many thanks to them.

The material in this dissertation is based on the following papers which are either published, or under final process for publication.

Chapter 2, is based on and mostly a reprint of the following papers:

- Sang Young Kim, D.-W. Kang, K.-J. Koh and G. M. Rebeiz,"An Improved Wideband All-Pass I/Q Network for Millimeter-Wave Phase-Shifters," submitted to *IEEE Transactions on Microwave Theroy and Techniques*, April 2012 (accepted).

Chapter 3, is based on and mostly a reprint of the following papers:

- Sang Young Kim and G. M. Rebeiz,"A 4-Bit Passive Phase Shifter for Automotive Radar Application in 0.13 μm CMOS," *IEEE Compound Semiconductor IC Symposium (CSICS)*, Oct. 2009, pp. 1-4.

Chapter 4, is based on and mostly a reprint of the following papers:

- Sang Young Kim and G. M. Rebeiz,"A Low-Power BiCMOS 4-Element Phased Array Receiver for 76-84 GHz Radars and Communication Systems," *IEEE Journal of Solid-State Circuits*, Feb. 2012, pp. 359-367.

Chapter 5, is based on and mostly a reprint the following papers:

- Sang Young Kim, Ozgur Inac, C.-Y. Kim and G. M. Rebeiz,"A 76-84 GHz 16-Element Phased Array Receiver with a Chip-Level Built-In-Self-Test System,", accepted for publication in *IEEE Radio Frequency Integrated Circuits Symp. Dig.* 2012.
- Sang Young Kim, Ozgur Inac, C.-Y. Kim and G. M. Rebeiz,"A 76-84 GHz 16-Element Phased Array Recevier with a Chip-Level Built-In-Self-Test System," will be submitted to *IEEE Transactions on Microwave Theroy and Techniques* 2012.

Appendix A, is based on and mostly a reprint of the following papers:

- Sang Young Kim, K. V. Buer and G. M. Rebeiz,"An 18-20 GHz Subharmonic Satellite Down-Converter in 0.18μm SiGe Technology," *IEEE Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan. 2009, pp. 1-4.

The dissertation author was the primary author of the work in these chapters, and co-authors (Prof. Gabriel M. Rebeiz, Dr. Dong-Woo Kang, Dr. Kwang-Jin Koh, Dr. Choul-Young Kim, Mr. Ozgur Inac, Mr. Donghyup Shin, Kenneth V. Buer) have approved the use of the material for this dissertation.

Sang Young Kim

La Jolla, CA

June, 2012.

VITA

1998 - 2003	B. S. in Electrical Engineering, Seoul National University, Seoul, Republic of Korea
2003 - 2005	M. S. in Electrical Engineering, University of Southern California
2005 - 2012	Ph. D. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego

PUBLICATIONS

Sang Young Kim, K. V. Buer and G. M. Rebeiz,"An 18-20 GHz Subharmonic Satellite Down-Converter in 0.18μm SiGe Technology," *IEEE Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan. 2009, pp. 1-4.

Sang Young Kim and G. M. Rebeiz,"A 4-Bit Passive Phase Shifter for Automotive Radar Application in 0.13 μm CMOS," *IEEE Compound Semiconductor IC Symposium (CSICS)*, Oct. 2009, pp. 1-4.

Sang Young Kim and G. M. Rebeiz,"A Low-Power BiCMOS 4-Element Phased Array Receiver for 76-84 GHz Radars and Communication Systems," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 359-367, Feb. 2012.

Ozgur Inac, Sang Young Kim, D. Shin, C.-Y. Kim and G. M. Rebeiz,"Built-In Self Systems for Silicon-Based Phased Arrays," *IEEE Int. Microwave Symp. Dig.*, June 2012, accepted.

Sang Young Kim, Ozgur Inac, C.-Y. Kim and G. M. Rebeiz,"A 76-84 GHz 16-Element Phased Array Receiver with a Chip-Level Built-In-Self-Test System," *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, June 2012, accepted.

Sang Young Kim, D.-W. Kang, K.-J. Koh and G. M. Rebeiz,"An Improved Wideband All-Pass I/Q Network for Millimeter-Wave Phase-Shifters," accepted for publication in *IEEE Transactions on Microwave Theory and Techniques*, 2012.

Sang Young Kim, Ozgur Inac, C.-Y. Kim and G. M. Rebeiz,"A 76-84 GHz 16-Element Phased Array Receiver with a Chip-Level Built-In-Self-Test System," will be submitted to *IEEE Transactions on Microwave Theory and Techniques*, 2012.

G. M. Rebeiz, K.-J. Koh, T. Yu, D.-W. Kang, C.-Y. Kim, Y. Atesal, B. Cetinoneri, S. Y. Kim, D. Shin,"Highly dense microwave and millimeter-wave phased array T/R modules and Butler matrices using CMOS and SiGe RFICs," *IEEE Int. Symp. Phased Array Sys. and Tech.*, pp. 245-259, Oct. 2010.

G. M. Rebeiz, K.-J. Koh, T. Yu, D.-W. Kang, C.-Y. Kim, Y. Atesal, B. Cetinoneri, S. Y. Kim, K. Ho, D. Shin, "Highly dense microwave and millimeter-wave phased array T/R modules using CMOS and SiGe RFICs," *IEEE Wireless and Microwave Technology Conference*, pp. 1-5, Apr. 2011.

ABSTRACT OF THE DISSERTATION

W-band Phased Array Systems using Silicon Integrated Circuits

by

Sang Young Kim

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2012

Professor Gabriel M. Rebeiz, Chair

This thesis demonstrates the silicon-based on-chip W-band phased array systems. An improved wideband I/Q network to minimize the capacitive loading problem is presented, and its implementation in a 60–80 GHz active phase shifter using 0.13 μm SiGe BiCMOS process is demonstrated. In addition, a 67–78 GHz 4-bit passive phase shifter using low-pass π-network and 0.13 μm CMOS switches is demonstrated. By adding amplifiers to the passive phase shifter with the architecture of alternating amplifiers and phase shifter cells, a low-power BiCMOS 4-element phased array receiver for 76–84 GHz applications are presented. Lastly, a 76-84 GHz 16-element phased array receiver, designed differentially in order to reduce the sensitivity to packaging effect such as ground inductance, is presented.

This thesis presents the silicon-based on-chip W-band phased array systems. An improved quadrature all-pass filter (QAF) and its implementation in 60–80 GHz active phase shifter

using 0.13 μm SiGe BiCMOS technology is presented. It is demonstrated that with the inclusion of an R_s/R in the high Q branches of C and L, the sensitivity to the loading capacitance, therefore the I/Q phase and amplitude errors are minimized. This technique is especially suited for wideband millimeter-wave circuits where the loading capacitance (C_L) is comparable to the filter capacitance (C). A prototype 60–80 GHz active phased shifter using the improved QAF is demonstrated. The overall chip size is 1.15 $\times$ 0.92 mm^2 with the power consumption of 108 mW. The measured S_11 and S_22 are $<$ -10 dB at 60–80 GHz and 60–73 GHz, respectively. The measured average power gain is 11.0–14.7 dB at 60–79 GHz with the rms gain error of $<$ 1.3 dB at 60–78 GHz for 4-bit phase states. And the rms phase error is $< 9.1^\circ$ at 60–78.5 GHz showing wideband 4-bit performance. The measured NF is 9–11.6 dB at 63–75 GHz and the measured P_{1dB} is -27 dBm at 70 GHz.

In another project, a 67–78 GHz 4-bit passive phase shifter using 0.13 μm CMOS switches is demonstrated. The phase shifter is based on a low-pass π-network. The chip size is 0.45 $\times$ 0.3 mm^2 without pads and consumes virtually no power. The measured S_{11} and S_{22} is $<$ -10 dB at 67–81 GHz for all 16 phase states. The measured gain of 4-bit phase shifter is -19.2 $\pm$ 3.7 dB at 77 GHz with the rms gain error of $< 11.25^\circ$ at 67–78 GHz. And the measured rms phase error is $<$ 2.5 dB at 67-78 GHz. The measured P_{1dB} is $>$ 8 dBm and the simulated IIP3 is $>$ 22 dBm.

A low-power 76–84 GHz 4-element phased array receiver using the designed passive phase shifter is presented. The power consumption is minimized by using a single-ended design and alternating the amplifiers and phase shifter cells to result in a low noise figure at a low power consumption. A variable gain amplifier and the 11° phase shifter are used to correct for the rms gain and phase errors at different operating frequencies. The overall chip size is 2.0 $\times$ 2.7 mm^2 with the current consumption of 18 mA/channel with 1.8 V supply voltage. The measured S_{11} and S_{22} is $<$ -10 dB at 70–88 GHz and 74–88 GHz, respectively. The measured average power gain is 10.1–18.9 dB at 76–84 GHz with the rms gain error of $<$ 0.6 dB at 76–77 GHz, $<$ 0.8 dB at 79–81 GHz and $<$ 1.1 dB at 81–84 GHz. The measured rms phase error is $< 3.9^\circ$ at 76–77 GHz, $< 7.2^\circ$ at 79–81 GHz and $< 10.4^\circ$ at 81–84 GHz. The measured NF is 10.5 $\pm$ 0.5 dB at 80 GHz and the measured input P_{1dB} is -26.7 dBm to -23 dBm at 77–80 GHz depending on the gain setting. The on-chip coupling is $<$ -30 dB between adjacent channels.

Finally, a 76–84 GHz 16-element phased array receiver in a 0.13 μm SiGe BiCMOS process is presented. All circuits are designed differentially to result in less sensitivity to packaging effect and high channel-to-channel isolation. The overall chip size is 5.0 $\times$ 5.8 mm^2 with the

power consumption of 500–600 mA from 2 V supply voltage. The measured S_{11} and S_{22} for all 16 phase states is $<$ -9 dB at 72–88 GHz and 73–86 GHz, respectively. And the measured average power gain (S_{21}) is $>$ 10 dB for 76.4–90 GHz with the rms gain error of $<$ 1 dB for 74–84.2 GHz. The measured rms phase error is $< 11^{\circ}$ for 73.6–83.6 GHz. In order to optimize the rms gain and phase errors, the VGA and 11° phase shifter are used. The measured reverse isolation (S_{12}) $>$ -45 dB. The measured NF is 11.2–13 dB at 77–87 GHz at the maximum gain state. And the measured input P_{1dB} is -20 dBm at 77 GHz and -25.8 dBm at the 83 GHz. The measured coupling between channels is $<$ -48 dB because of the relatively high substrate resistance and the long distance between channels.

Chapter 1

Introduction

1.1 Phased Array Systems

Phased array systems are widely used in defense applications such as radars and communication systems to achieve beam forming and beam scanning [1]. Mechanically-controlled phased array systems uses many motors and gears to rotate and elevate the antennas. However, because this technique is slow and difficult to control accurately, electronically-scanned phased array has been developed. With this technique, the high-speed and high-precision beam forming and scanning can be achieved [2].

Phased arrays are an array of antennas in which relative phase of the each element is varied in such a way that the signal of the desired direction is added constructively and the signals of the undesired direction are suppresed. By increasing the number of the antenna and changing the signal amplitude of the each antenna, the beam pattern can be shaped (Fig 1.1(a)). Also, by controlling the phase shifter of each antenna, the beam pattern can be steered (Fig. 1.1(b)). Fig. 1.2 shows the block diagram of the 8-element phased array system receiver. The incoming signal from the angle θ arrives at each antenna with a phase difference of $\triangle\phi$,

$$\triangle\phi = kd\cos\theta, \quad k = \frac{2\pi}{\lambda} \tag{1.1}$$

where, d is the distance between the antenna elements, θ is the incident angle, and λ is the wavelength. By compensating the phase and amplitude difference between the antenna by the phase shifter and the variable gain control block, the incoming signals are added constructively in the desired direction and suppressed in the other directions.

One of the benefits of the phased array systems is that the effective Signal-to-Noise-

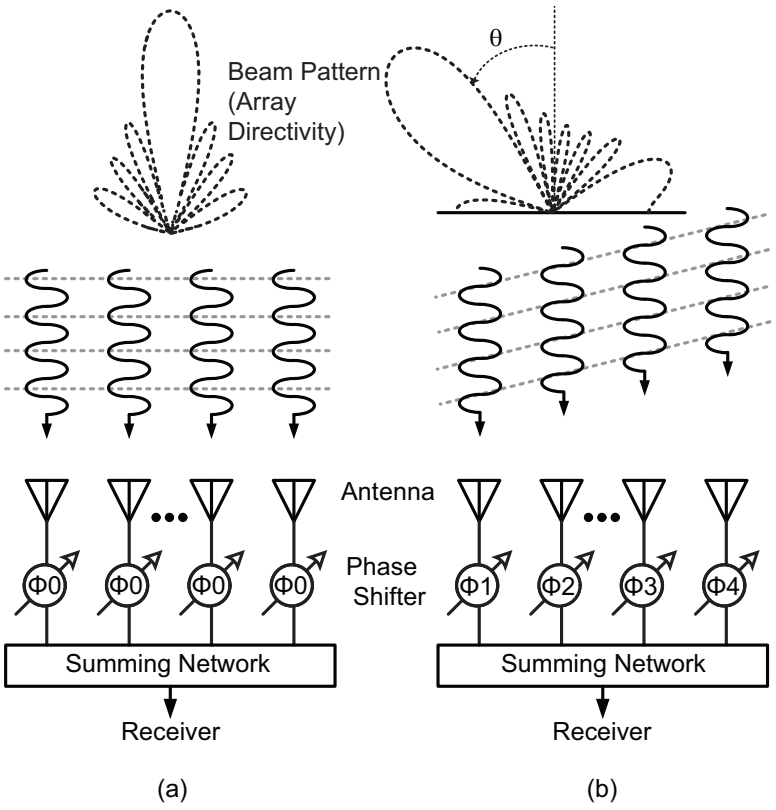


Figure 1.1: (a) Beam forming and (b) Beam steering.

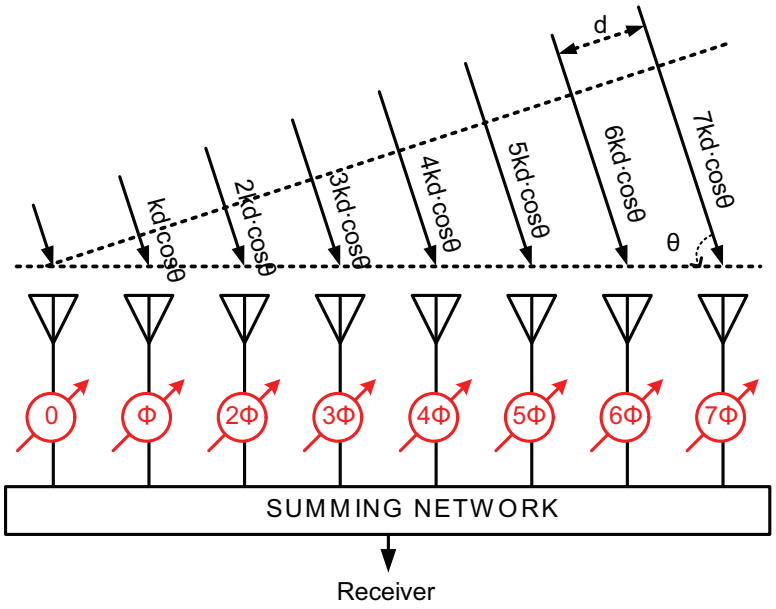


Figure 1.2: Block diagram of an 8-element phased array.

Ratio (SNR) at the output of the receiver can be improved by 10log(N) compared the single antenna element. As can be seen in Fig. 1.3(a), the incoming signals at each antenna are amplified by the system power gain and combined "coherently" at the output. However, the input noise at each antenna are amplified by the same gain and then combined "incoherently". Therefore, the SNR at the output of the phased array receiver is improved. In addition, any interference from different direction can be placed in the null of the beam pattern so that the spectral efficiency is increased by spatial filtering (Fig. 1.3(b)).

1.2 Phased Array Architectures

The phase shifting to compensate for the phase difference between the antennas can be realized in the RF, IF, LO and digital domain (Fig. 1.4). The RF phase-shifting architecture (Fig. 1.4(a)) has been widely used because the interferers at the system are combined and suppressed at the RF domain, thus the required linearity of the following mixer can be relaxed. Also, because the RF phase-shifting needs only one mixer at the receiver, it can be scalable to large arrays with low power consumption. Recently, the IF- or LO-based phase-shifting architectures were realized (Fig. 1.4(b),(c)) because these archtectures can remove the RF phase shifters which can be lossy at millimter-wave. However, they requires the LO distribution network, which requires complex layout for large arrays. Also, they require one mixer for every channel and this will make the system complex with high power consumption. In the digial beam-forming (DBF) architecture (Fig. 1.4(d)), the signals are first digitized and the phase shifting is done in the digital domain. The DBF can achieve the highest performance. However, the DBF consumes high power because it requires the largest number of components including A/D converters and digital signal processor (DSP). Therefore, all RF phase-shifting architecture is chosen in this thesis.

1.3 77 GHz Automotive Radars

One of the application that phased arrays have been used is the automotive radars. Over the past decades, an intense research effort has been put on the automotive radar systems, including parking aids, blind-spot detection, lane change and adaptive cruise control (ACC). Especially, long-range radars (LRR) for the ACC require the narrow beamwidth and the beam steering capabilities in order to detect the distance and the relative speed of the vehicles in the range of 100-150 meters. Therefore, the 76-77 GHz band is preferred because it can have large arrays of

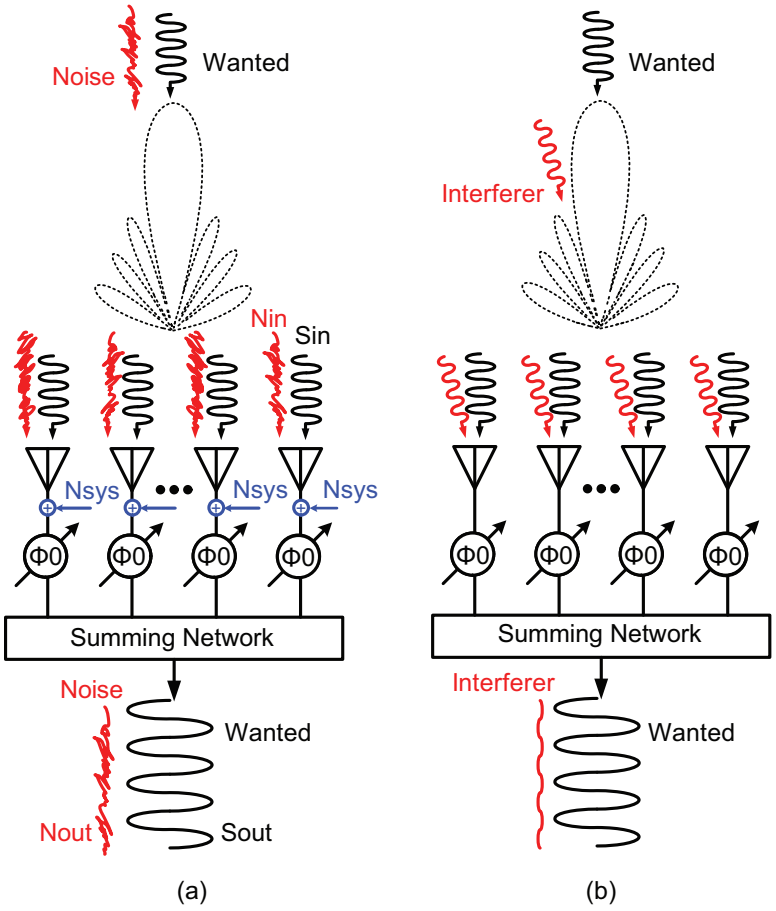


Figure 1.3: (a) SNR improvement and (b) interference rejection, in an All-RF phased array architecture.

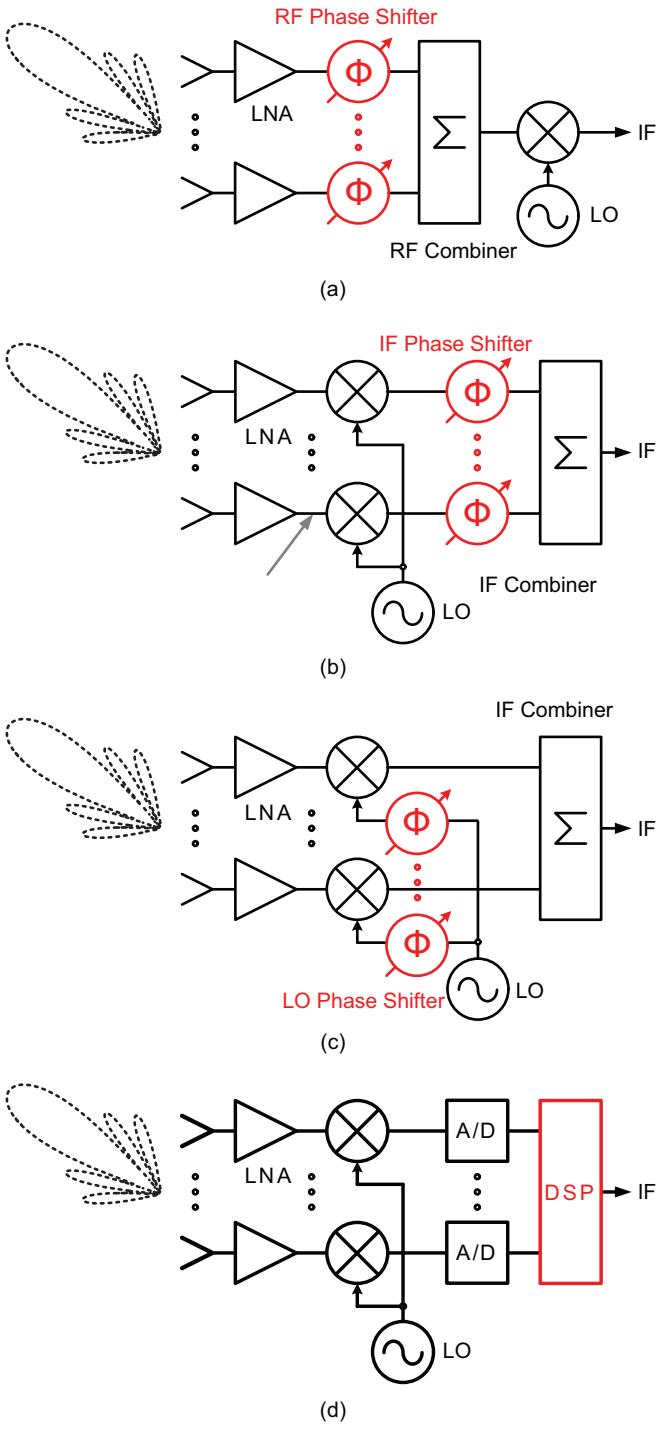


Figure 1.4: Block diagram of the phased array architecture (a) RF phase-shifting, (b) IF phase-shifting, (c) LO phase-shifting and (d) digital beam-forming.

antenna with compact size.

At millimter-wave frequency, these phased array systems have been implemented with GaAs or InP based on discrete modules, resulting in high cost and low integration density. However, recent developement in silicon technology has led to the silicon-based single-chip phased array in order to reduce the cost. SiGe implementations of the automotive radars were particularly successful due to their low phase noise performance and reliability over a range of temperature.

1.4 Thesis Overview

Chapter 2 presents the design and analysis of an improved wideband I/Q network and its implementation in a wideband phased-array front-end. It is found that the addition of two resistors (Rs) in the all-pass I/Q network results in improved amplitude and phase performance versus capacitance loading and frequency, which is essential for wideband millimeter-wave applications. A prototype 60-80 GHz phased array front-end based on 0.13 μm SiGe BiCMOS is demonstrated using the improved QAF and with 4-bit phase shifting performance at 55-80 GHz. Application areas are in wideband millimeter-wave systems.

Chapter 3 demonstrates a 67–78 GHz 4-bit passive phase shifter using CMOS switches available in the 0.13 μm SiGe BiCMOS process. The phase shifter is based on a low-pass π–network and CMOS passive transistors. The phase shifter achieves -19.2 $\pm$ 3.7 dB of gain including pad loss at 77 GHz. The RMS phase error is less than 11.3° and the RMS gain error is less than 2.5 dB over the 67–78 GHz range. The total chip size is 450 $\times$ 300 m^2 (0.135 mm^2), excluding pads, and the chip consumes virtually no power. The measured P1dB is $>$ +8 dBm at 77 GHz and the simulated IIP3 is $>$ 22 dBm, making it possible to precede this design with a high gain LNA without loss of system linearity or input power handling.

Chapter 4 presents a 76–84 GHz low-power 4-element phased array receiver built using a 0.13 μm BiCMOS process. The power consumption is reduced by using a single-ended design and alternating the amplifiers and phase shifter cells to result in a low noise figure at a low power consumption. A variable gain amplifier and an 11° trim bit are used to correct for the rms gain and phase errors at different operating frequencies. The phased array consumes 32 mW per channel and results in a gain of 10–19 dB at 76–84 GHz, a noise figure of 10.5 $\pm$ 0.5 dB at 80 GHz and an rms gain and phase error $<$ 0.8 dB and $<$ 7.2°, respectively, up to 81 GHz, and $<$ 1.1 dB and 10.4° up to 84 GHz. The phased array also shows a channel to channel coupling of $<$ -30 dB up to 84 GHz. The alternating amplifier/phase shifter topology consumes less power than

a vector modulator approach, and can be extended to a differential topology. To our knowledge, this work presents state-of-the-art on-chip performance at W-band frequencies.

Chapter 5 presents a 76-84 GHz 16-element phased array receiver built using a 0.13 μm BiCMOS process. The chip is built with fully differential circuits in order to avoid the ground inductance effect from packaging (bond-wire, stud-bump, etc.). A variable gain amplifier and an 11° calibration bit are used to correct for the rms gain and phase errors. Each channel consumes 60 mW and results in an average gain of 9–17 dB, S_{11} and S_{22} of $<$ -10 dB at 76–84 GHz, a noise figure of 11–13.5 dB at 76–85 GHz, a input P_{1dB} of -21 dBm at 77 GHz and an rms gain and phase error $<$ 1 dB and $< 11^\circ$, respectively, at 76–83 GHz. The measured phased-array including the 16:1 summer and I/Q mixer shows a voltage conversion gain of 28–33 dB in a 1 kΩ IF load (V_{outIF}/V_{inRF}), and I/Q imbalance $<$ 1 dB at 76–84 GHz ($<$ 0.5 dB at 76-81 GHz), a 3-dB IF bandwidth of DC–5 MHz with a controllable IF gain range of 20 dB (for FMCW radars). The required LO power is -4 dBm at 37-44 GHz and is provided using an external source. The phased array also shows a channel to channel coupling of $<$ -40 dB up to 84 GHz.

Appendix A presents the design and implementation of a 18–20 GHz satellite down-converter receiver with a 10.5 GHz local oscillator. The circuit design is single-ended for minimal area and current consumption, and for compatibility with a GaAs low-noise pre-amplifier and a coaxial output transmission-line. The RF, LO and IF ports are ESD protected using on-chip diodes. The down-converter results in a measured gain of 35–40 dB, an output P_{1dB} of +2.4 dBm, and a noise figure of 4.8–9.8 dB for an input frequency of 18–20 GHz (IF of 3–1 GHz). The required LO power is 2–3 dBm. The chip consumes 31.5 mA from a 2.5 V supply, and 55 $\%$ of the current is used for the output 50 Ω driver (17.3 mA). The chip size is 1.1 $\times$ 0.7 mm^2 including all pads and is built using a commercial 0.18-μm SiGe technology.

Chapter 2

An Improved Wideband All-Pass I/Q Network for Millimeter-Wave Phase-Shifters

2.1 Introduction

Electronic phase shifters are essential for phased-arrays, and have been implemented using passive and active networks in CMOS and SiGe technologies [3–21]. The active approach is based on an in-phase/quadrature-phase (I/Q) network and, phase interpolation is achieved by adding the I/Q signals with appropriate amplitudes and polarities (Fig. 2.1) [13–21]. A low-loss accurate I/Q network is therefore an important circuit element of the active approach for precise phase shifting. To circumvent the loss in traditional R-C-based passive quadrature generators such as RC–CR bridge or R–C polyphase filters, a new quadrature all-pass filter (QAF) based on an L–C series resonator was proposed in [14]. The QAF utilizes a second-order series resonance and provides a wideband quadrature signal with maximum 3 dB voltage gain, and has been implemented in several wideband phased-array chips [14–16, 18, 19, 21].

However, at millimeter-waves, the QAF loading capacitance due to the vector modulator can be comparable to the internal QAF capacitance, and this results in significant I/Q errors. In fact, this problem was known in [14], and it was recommended that the loading capacitance (C_L) be chosen to be 0.1–0.2 of the filter capacitance (C) for reduced phase errors. At millimeter-wave frequencies, this is not possible in many cases, and therefore, an improved QAF network which is not sensitive to the loading capacitance is required. This paper presents the analysis of such a

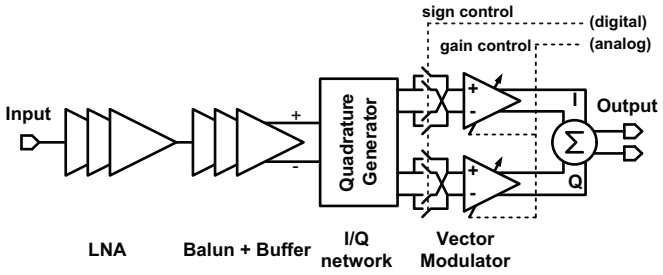


Figure 2.1: The active phase shifter architecture.

network, and its implementation in a wideband 60–80 GHz phased–array front–end.

2.2 Design

2.2.1 Architecture

The active phase shifter architecture is presented in Fig. 2.1. An I/Q network and two variable gain amplifiers (VGAs) are used in a differential mode for sign reversal, and the VGA outputs are summed in the current domain to create the final vector with arbitrary phase shift. The output phase relies on the gain *ratio* between the I- and Q-paths, and this results in a robust design against process, supply voltage and temperature variations. Phase synthesis based on the interpolation of quadrature vectors is a linear operation and is independent of frequency, guaranteeing wideband operation. The fundamental limitation of the phase accuracy and the operating bandwidth is given by the quadrature network.

Analysis Of Phase Synthesis Based On Signal Interpolation

To investigate the effect of the amplitude and phase errors in the quadrature network on the output phase accuracy, define a quadrature signal set as S_{IQ} = $\{V_I, V_Q\}$ = $\{A\angle 0°, A\Delta A\angle(90+\Delta\theta)°\}$, where ΔA and $\Delta\theta$ are the I/Q amplitude mismatch and phase imbalance of the basis I/Q vectors V_I and V_Q, respectively. The linear combination of the reference vectors is V_{out} = $G_I A\angle 0°$+$G_Q A\Delta A\angle(90+\Delta\theta)°$, where G_I and G_Q are amplitude weights determined by the output phase θ_{out} = $\tan^{-1}(G_Q/G_I)$. The phase error (θ_{error}) and amplitude error (M_{error}) of the output signal are given by (2.1) and (2.2), respectively ([22]):

$$\theta_{\text{error}}|_n = \tan^{-1}P_n - \tan^{-1}\left(\frac{P_n\Delta A\cos\Delta\theta}{1-P_n\Delta A\sin\Delta\theta}\right)(\deg). \tag{2.1}$$

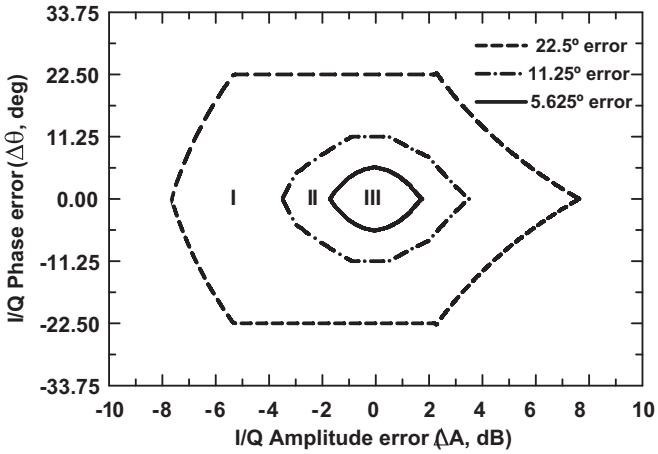


Figure 2.2: The contour plot of I/Q errors (quadrature phase error, $\Delta\theta$, and amplitude mismatch, ΔA) in a quadrature network for 3-bit (region I, $\theta_{error} < 360°/2^4 = 22.5°$), 4-bit (region II, $\theta_{error} < 360°/2^5 = 11.25°$) and 5-bit (region III, $\theta_{error} < 360°/2^4 = 5.625°$) operation.

$$\mathrm{M_{error}}|_n = 10\log\left(\frac{1+(\mathrm{P_n}\Delta\mathrm{A})^2 - 2\mathrm{P_n}\Delta\mathrm{A}\sin\Delta\theta}{1+\mathrm{P_n^2}}\right)\ (\mathrm{dB}). \tag{2.2}$$

where P_n=$(G_Q/G_I)_n$=$\tan^{-1}(n360°/2^N)$, with N=number of phase bits; and n=0, 1, 2, …, 2^N-1 ($0 \le P_n \le \infty$, P_n=0 for θ_{out}=0°, P_n=1 for θ_{out}=45° and P_n=∞ for θ_{out}=90°).

When P_n=∞ (+90° phase bit), θ_{error}=$\Delta\theta$ and M_{error}=20logΔA, respectively, consistent with intuition ($\tan^{-1}x \simeq \pi/2$-1/x, if $x \gg 1$). θ_{error} should be $<360°/2^{N+1}$ to avoid any phase overlap between different phase bits, guaranteeing N-bit phase resolution. Fig. 2.2 ([22]) presents contour plots of ΔA and $\Delta\theta$ for several cases of θ_{error}. To achieve 3-bit, 4-bit and 5-bit accuracies the I/Q errors should be inside region I, II and III, respectively. For example, for 5-bit phase accuracy, $|\Delta\theta|$ needs to be less than 5° with a maximum of $\pm$1.5 dB of I/Q amplitude error in the quadrature network.

2.2.2 Quadrature Signal Generation

2.2.3 R-C-based and L-C Resonator Quadrature Generators

The traditional RC-CR network has been widely used for narrowband quadrature signal generation (Fig. 2.3(a)). To extend the operation bandwidth, multi-stage R-C polyphase filter of which a single stage is shown in Fig. 2.3(b) has been used. However the limitation of these I/Q networks is the loss which tends to increase significantly with the number of stages for wideband

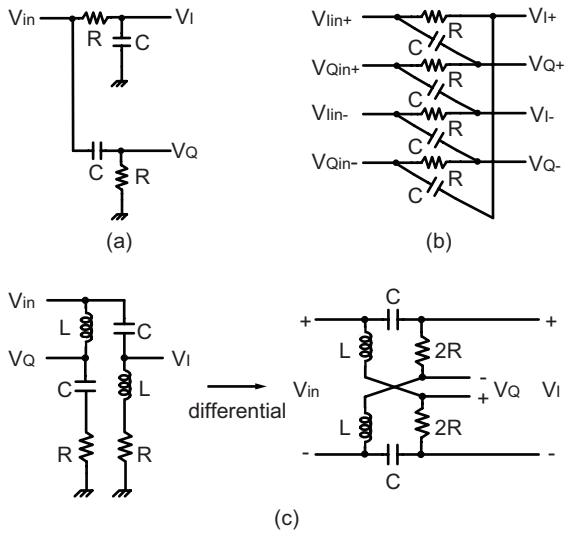


Figure 2.3: (a) Typical R-C-based lumped passive quadrature networks: RC-CR network, (b) R-C polyphase filter (one-stage) and (c) L-C resonance-based quadrature networks. The differential version is called as quadrature all-pass (QAF) filter.

operation. Therefore the main applications of these networks are in high signal routes such as LO or IF rather than the RF path [23–25].

Quadrature signals can also be generated without any voltage loss using an L-C resonance technique, which is shown in Fig. 2.3(c) for the single-ended version (where R=$\sqrt{L/C}$ {Q=$\sqrt{L/C}$/R=1} and ω_o=1/$\sqrt{LC}$). The transformation to a differential all-pass network having equal I/Q amplitude for all ω, called a quadrature all-pass filter (QAF), is described in [14]. The transfer function of the QAF ([22]) is

$$\begin{bmatrix} V_{I\pm} \\ V_{Q\pm} \end{bmatrix} = V_{in} \times \begin{bmatrix} \pm\dfrac{s^2+\frac{2\omega_o}{Q}s-\omega_o^2}{s^2+\frac{2\omega_o}{Q}s+\omega_o^2} \\ \mp\dfrac{s^2-\frac{2\omega_o}{Q}s-\omega_o^2}{s^2+\frac{2\omega_o}{Q}s+\omega_o^2} \end{bmatrix} \tag{2.3}$$

where *s*=*j*ω. For practical applications with $0.8 \leq Q \leq 1$, the QAF results in 2-3 dB voltage gain over a wideband frequency range (3:1) which is much better than the R-C-based I/Q networks [14]. The QAF can generate any phase difference between two outputs by changing the resistor value (R) in Fig. 2.3(c): i.e., in general, the replacement of 2R with 2R$\times\xi$ will generate $2\times\tan^{-1}(1/\xi)$ of phase difference between the output ports.

Performance Comparison

Fig. 2.4 ([22]) shows the performance comparison between the polyphase filters and the QAF, when driven by ideal voltage source and with no capacitance loading. For a fair comparison, the polyphase filters are also driven in an all-pass mode where the quadrature-phased differential input, $V_{Qin\pm}$, is tied to the in-phase differential input, $V_{Iin\pm}$ in Fig. 2.3(b), resulting in equal I/Q amplitude for all ω and quadrature phase splitting at the pole frequency (=1/RC) [25]. The poles of each stage in the 2- and 3-stage polyphase filters are also set at the same value. The 3-stage polyphase filter shows the widest I/Q phase bandwidth at the expense of high loss. The I/Q phase error characteristic of the QAF is equivalent to that of the second-order polyphase filter but the QAF achieves 6 dB higher voltage gain than the second-order polyphase filter. The QAF can achieve more than 100% bandwidth with an I/Q phase error $< 5^\circ$ and with $>$ 2.6 dB of voltage gain. Another difference between the polyphase filters and the QAF is that the QAF provides real input and output impedances over a wide bandwidth while the input and output impedances of the polyphase filter are capacitive (Fig. 2.5) [14]. Typically input and output return losses of the QAF are $<$ -10 dB over more than 240% bandwidth.

Improvement of the QAF under Loading Capacitance

A parasitic loading capacitance, C_L, will cause I/Q errors in the QAF and these errors are large at mm-wave frequencies since C_L can be comparable to the filter capacitance C [14]. The insertion of a series resistance R_s in the high Q branches of C and L reduces the network Q and its sensitivity to the loading capacitance (Fig. 2.6). In this case, the I/Q transfer function of (2.3) is modified as (2.4) ([22]), and R_s separates the negative real poles farther through decreasing Q by (1 + R_s/R). The R_s does not disturb any zero location. Since the quadrature phase relation is set by the geometry of the zero positions, the I/Q phase characteristics of (2.4) are identical to those of (2.3).

$$\begin{bmatrix} V_{I\pm} \\ V_{Q\pm} \end{bmatrix} = V_{in} \times \begin{bmatrix} \pm\dfrac{s^2 + \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}\left(1 + \frac{R_s}{R}\right)s + \omega_o^2} \\ \mp\dfrac{s^2 - \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}\left(1 + \frac{R_s}{R}\right)s + \omega_o^2} \end{bmatrix} \tag{2.4}$$

Fig. 2.7 ([22]) presents the simulated QAF I/Q phase errors and magnitude mismatches with several values of R_s/R versus C_L/C at ω_o. The I/Q errors are suppressed with the increase of R_s and the QAF is insensitive to the parasitic capacitance when R_s = R at ω_o. The penalty is loss

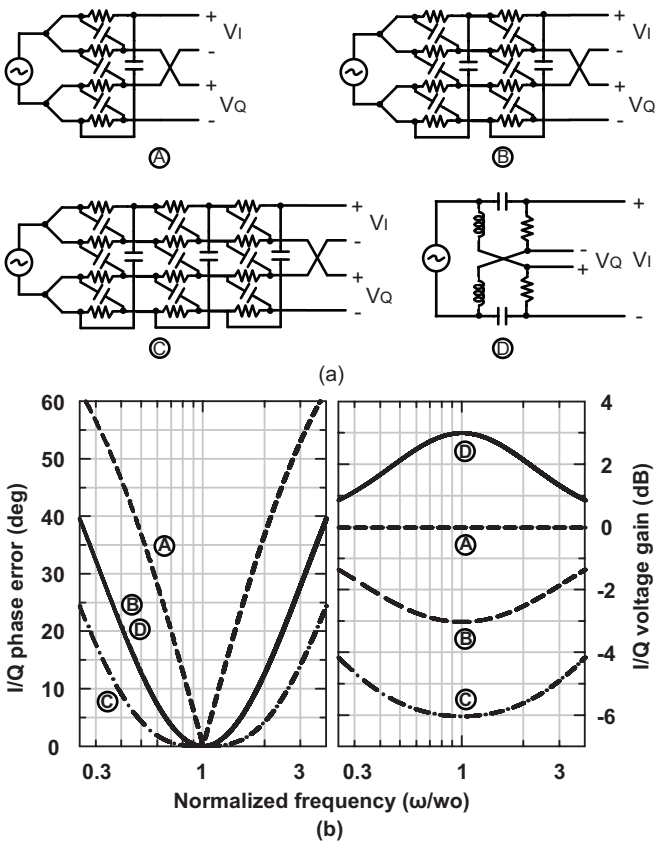


Figure 2.4: Performance comparisons between quadrature networks: (a) R-C one-, two- and three-stage polyphase filters (Ⓐ, Ⓑ and Ⓒ) and QAF (Ⓓ), (b) quadrature phase error and gain characteristics versus normalized angular frequency for the QAF and polyphase filters. R = 20 Ω, C = 113.68 fF, L = 45.47 pH and f_o = 70 GHz.

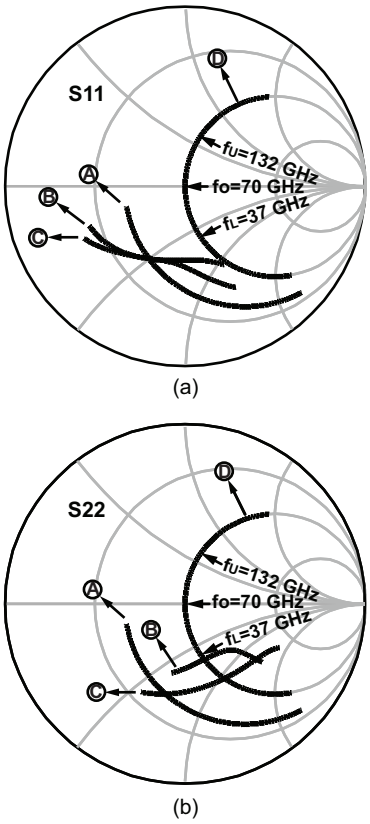


Figure 2.5: Input and output impedance of the I/Q networks shown in Fig. 2.4: (a) input differential impedance, (b) output differential impedance for one of the I/Q outputs. For QAF, S_{11} < -10 dB and S_{22} < -10 dB at 37 GHz ($0.53\,f_o$) to 132 GHz ($1.88\,f_o$).

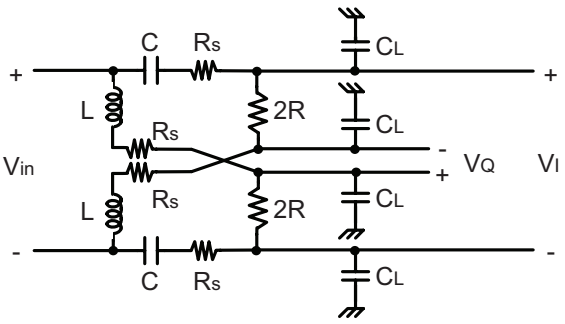


Figure 2.6: Q reduction in the QAF using R_s to desensitize the loading capacitance C_L.

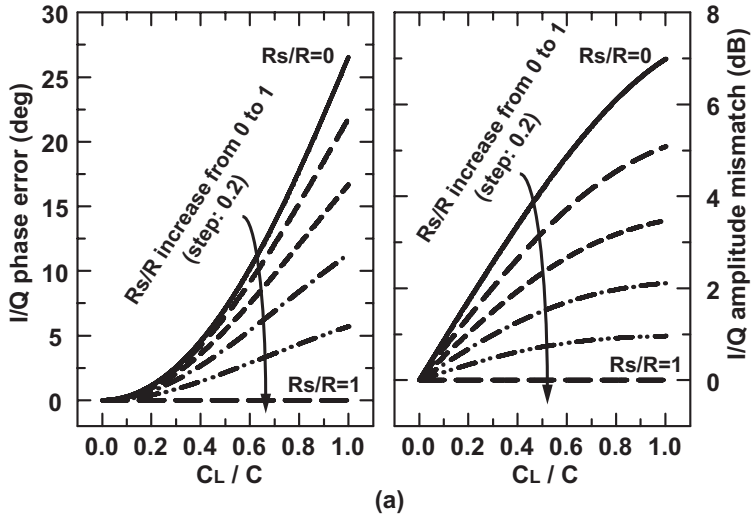


Figure 2.7: I/Q errors (phase errors and amplitude mismatches) in the QAF under capacitive loading, C_L, with several values of R_s in Fig. 2.6

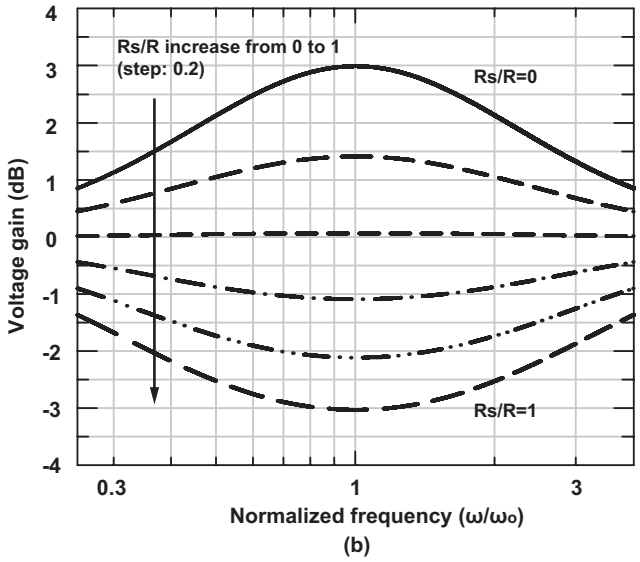


Figure 2.8: Amplitude response of the improved QAF vs. R_s.

as shown in Fig. 2.8 ([22]), and the maximum loss to desensitize C_L at ω_o is 6 dB when R_s = R (Fig. 2.8 is done for C_L/C = 0). The added benefit of R_s is that it increases the QAF input impedance by (1 + R_s/R) and increases the load impedance on the previous amplifier stage (thus lowering its power).

An in-depth look at the frequency response of the QAF with a loading capacitance and the corresponding effect of R_s is shown in Fig. 2.9. The simulations are done for a QAF with a natural Q = 1, that is, C_L = 0 and Rs = 0. It is seen that the phase mismatch between the I and Q outputs for C_L = 0.5 C is the same as C_L = 0 but with a shift in frequency due to the C_L loading (Fig. 2.9(a)). The addition of an R_s serves to de-Q the network and widen the frequency response at the expense of loss as shown in Fig. 2.9(b). In effect, the I/Q response can be re-centered for a specific C_L value and an R_s is not really needed. However, the amplitude mistmatch between the I and Q output is greatly affected by the C_L loading (Fig. 2.9(c)) and the addition of R_s/R = 0.67 to the network improves the mismatch to $<$ 1.5 dB (from 4–5 dB) over a wide frequency range (Fig. 2.9(d)), and allows the design of wideband 5-bit phase shifters. In reality, the choice of R_s depends on C_L/C and can be minimized with proper scaling of the QAF impedance together with optimizing the loading transistor size.

2.2.4 Wideband 60–80 GHz Phase Shifter Design

The active phase shifter is designed using a 0.13 μm SiGe BiCMOS process (IBM 8HP). The IBM 8HP supports seven metal layers including two thick metal layers, AM (= 4 μm) and LY (= 1.25 μm), for low loss the RF routing (Fig. 2.10). The SiGe npn transistors with a peak cutoff frequency (f_T) of 200 GHz, Metal-Insulator-Metal (MIM) capacitors (1 fF/μm^2) and spiral inductors are provided in the design kit, but in this work, coplanar-waveguide (CPW) transmission lines are used as the inductors using shorted stubs. The transition between the 50 Ω transmission line and the G-S-G pad is designed using an electromagnetic simulator (Sonnet [26]) to provide a 50 Ω impedance and $<$ -25 dB reflection coefficient.

The active phase shifter circuit is shown in Fig. 2.11. First, the single-ended RF input signal is amplified by a three-stage low-noise amplifier (LNA), and then converted to a differential signal using an active balun. Next, the differential quadrature signals are generated using a QAF loaded with Rs and the I/Q signals are sent to a vector modulator. One output of the vector modulator is terminated in 50 Ω for single-ended S-parameter measurements.

A common-emitter topology is adopted for the LNA to provide low-noise matching and 50 Ω input matching (Fig. 2.11). The first stage is biased at 1.0 mA/μm which is the middle

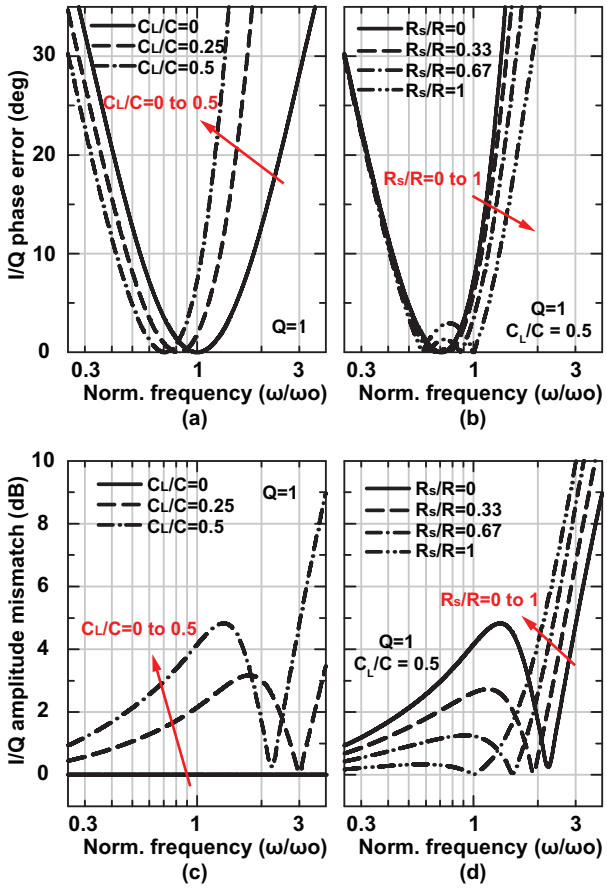


Figure 2.9: (a) I/Q phase error when C_L/C increases ($R_s = 0$), (b) I/Q phase error when R_s/R increases ($C_L/C = 0.5$), (c) I/Q amplitude mismatch when C_L/C increases ($R_s = 0$), (d) I/Q amplitude mismatch when R_s/R increases ($C_L/C = 0.5$).

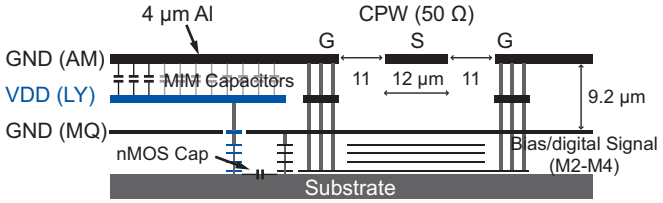


Figure 2.10: IBM 8HP metal stack-up.

bias point between the lowest noise figure and the maximum power gain. The input matching is done using a single shunt inductor at the gate for the minimum chip area. The second and third stages are biased to maximize the gain. The LNA consumes 9.3 mA from 1.5 V supply (14 mW) and achieves a simulated voltage gain of 19 dB at 70 GHz, and with S_{11} < -10 dB at 55.5–73.0 GHz. The simulated noise figure is 8 dB and 1-dB compression point (P_{1dB}) is -19 dBm (when simulated with a 50 Ω output port).

The active balun is realized using a two-stage differential amplifier by grounding one of the differential inputs of the first stage. In order to provide additional common-mode rejection, resistors are placed at the drain of the current source transistors (Fig. 2.11). Simulations indicate that the output signal has an amplitude imbalance of 0.7 dB and the phase error of 2.2° at 70 GHz. The simulated balun voltage gain is 7.9 dB at 70 GHz for a current of 11.2 mA.

After a buffer stage with a simulated voltage gain of -1.3 dB at 70 GHz, the differnetial quadrature signals are generated by the improved QAF network (Fig. 2.11) with L =35.14 pH, C =103.4 fF, and R = 20 Ω. This results in Q = $\sqrt{L/C}$/R = 0.92. In this design, the estimated loading capacitance is C_L = 50–80 fF, which results in C_L/C = 0.5–0.8 which causes an I/Q phase error of 18° and an amplitude mismatch of 6 dB at the center frequency (see Fig. 2.7). By choosing R_s = 20 Ω (Rs/R=1), the gain decreases to -3 dB, but I/Q errors are greatly minimized and the input impedance doubles to 40 Ω.

The vector modulator is composed of two Gilbert-cell type VGAs [14, 15] and the desired phase signal is synthesized by adding the current-domain I/Q signals with the proper gains at the output nodes (Fig. 2.11). The 180° phase shifting is done by switching the tail current (sw_I+/sw_I- and sw_Q+/sw_Q-) and the variable gain function is done by changing the bias current of the I/Q branches (Ibias and Qbias). The vector modulator consumes 11.6 mA from a 3 V supply with a voltage gain including the QAF of -3.2 dB at 70 GHz.

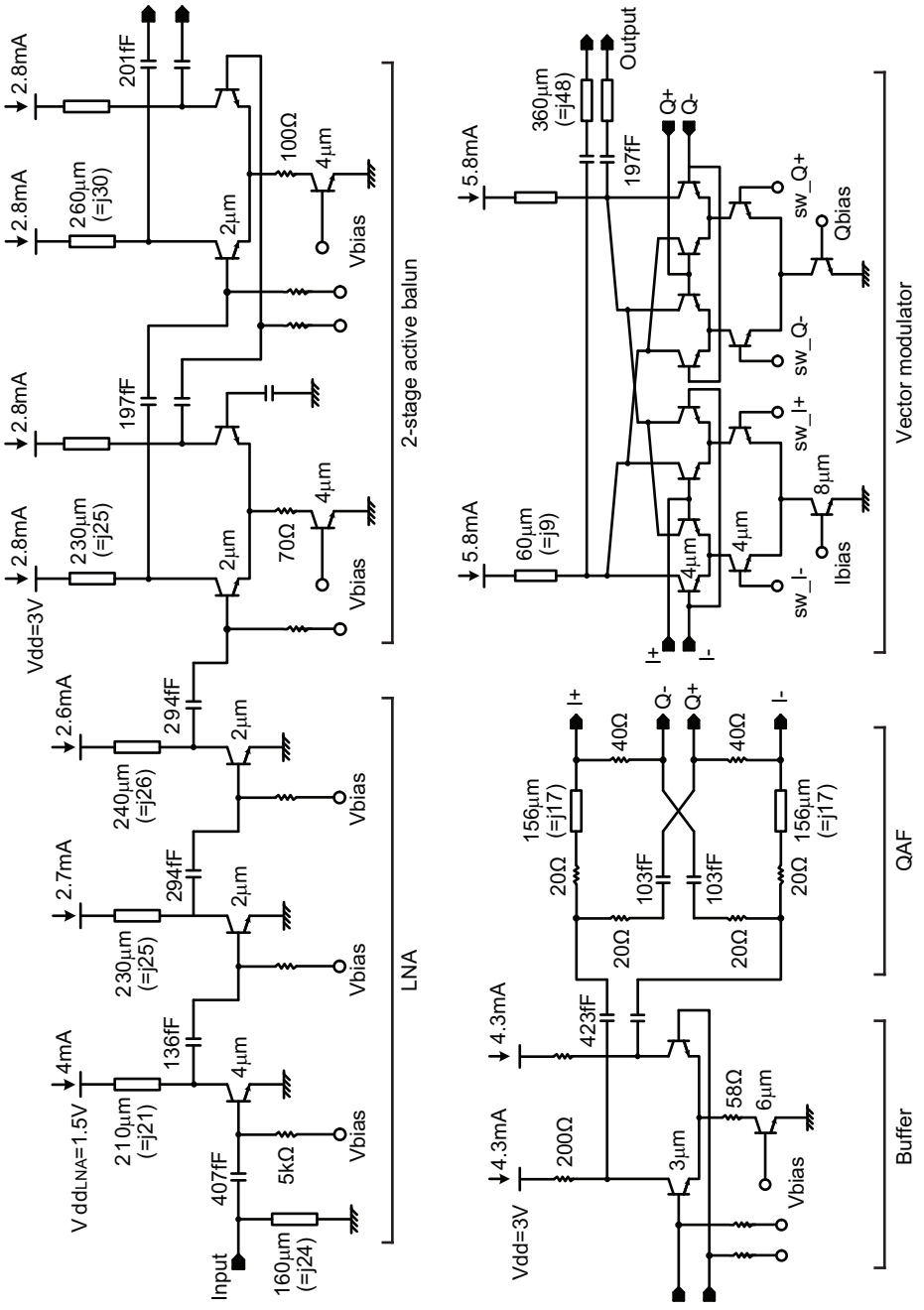


Figure 2.11: Circuit schematics of the wideband millimeter-wave phase shifter front-end.

2.3 Measurements

All measurements are done on-wafer using an Agilent E8361A Vector Network Analyzer with extenders to 110 GHz. A standard Short-Open-Load-Thru (SOLT) calibration to the W-band GSG probe tips is first done using the Cascade 138-357 calibration substrate [27], and the measurements include the GSG pad transition loss. Several chips were measured and resulted in similar measurements.

Fig. 2.12 presents the chip microphotograph of the wideband active phase shifter front-end. The overall chip size is 1.15×0.92 mm^2 including pads with a power consumption of 108 mW (LNA: 9.3 mA, 1.5 V, Balun: 11.6 mA, 3.0 V, buffer: 8.6 mA, 3.0 V, vector modulator: 11.6 mA, 3.0 V). The power consumption is relatively high due to the wideband design of 60-80 GHz and the de-Q resistors. Also, since this was a demonstration circuit for the improved QAF, low power techniques such as interstage transformer neutralization were not used.

Fig. 2.13 presents the measured input and output matching characteristics for 16 phase states. It is seen that S_{11} is $<$ -10 dB at 60–80 GHz, and S_{22} is $<$ -10 dB at 60–73 GHz. The measured S_{22} does not agree well with simulations and this could be due to slight imbalances in the differential output port (one is internally loaded with 50 Ω and the other is connected to the GSG pad). The measured average power gain (S_{21}) is 11.0-14.7 dB at 60–79 GHz and agrees well with simulations. The peak-to-peak gain variation is $\leq \pm2.3$ dB, and the rms gain variation is $<$ 1.3 dB at 60–78 GHz for the 4-bit phase states (Fig. 2.14). Fig. 2.15 presents the measured 4-bit phase responses from 60–80 GHz. The phase shifter results in an rms phase error of $< 9.1^\circ$ at 60–78.5 GHz, and $< 5.6^\circ$ at 70–77.5 GHz, showing wideband 4-bit performance.

An accurate method to measure the QAF performance is to compare the measured 0° and 90° responses of the active phase shifter [14]. Fig. 2.16 shows that the I/Q phase and amplitude error of the improved QAF is $< 9.5^\circ$ and $<$ 0.5 dB for 55–78.5 GHz, respectively, which is a proof that the improved QAF does generate accurate I/Q signals under high capacitive loading. Both follow the response predicted in Fig. 2.9.

The measured noise figure (NF) ranges is 9–11.6 dB at 63–75 GHz and agrees well with simulations (Fig. 2.17). The NF is nearly independent of the phase states because the LNA/active-balun gain is high enough to ignore the NF variation in the vector modulator. The measured 1-dB gain compression point (P_{1dB}) is -27 dBm at 70 GHz (not shown).

Fig. 2.18 presents the measured gain and rms errors at different temperatures up to 67 GHz (limited by the test set-up). The gain drops by $\sim$10 dB from 20° to 110°. In the future, this gain drop can be compensated using Proportional-To-Absolute-Temperature (PTAT) biasing

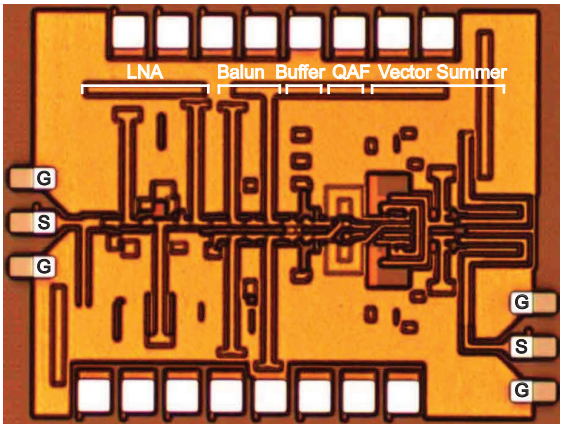


Figure 2.12: Microphotograph of the wideband 60-80 GHz phase shifter front-end (1.15×0.92 mm^2 including pads).

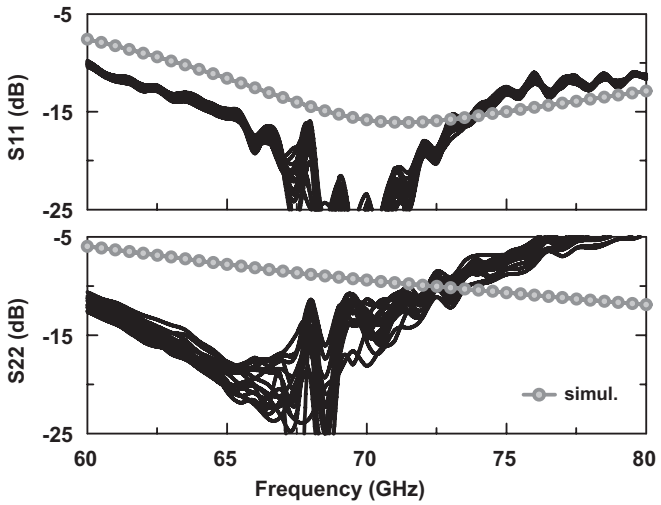


Figure 2.13: Measured and simulated S_{11} and S_{22} for 16 phase states.

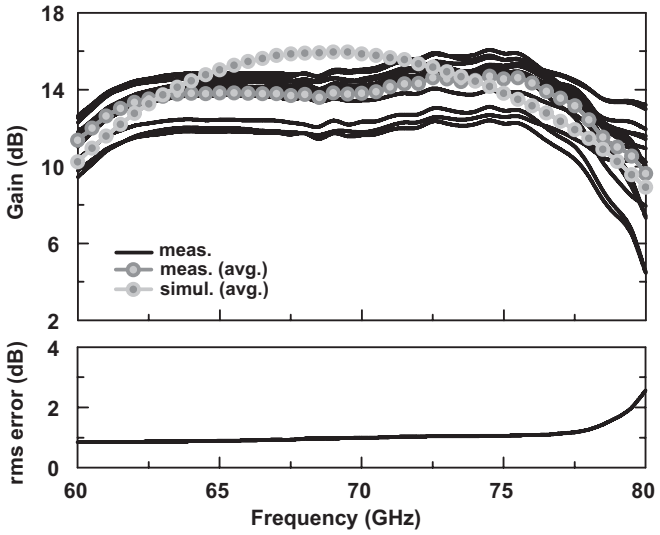


Figure 2.14: Measured and simulated gain response for 16 phase states and rms gain error.

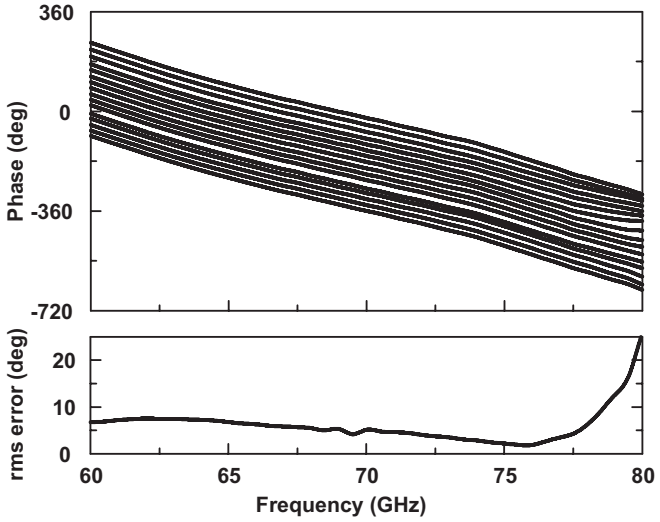


Figure 2.15: Measured phase response and rms phase error.

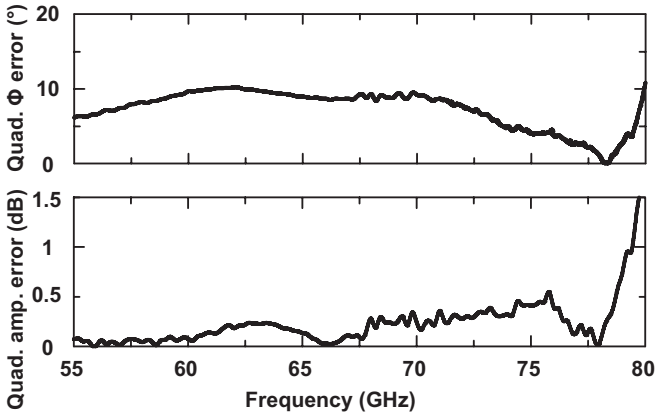


Figure 2.16: Measured quadrature phase error and amplitude error.

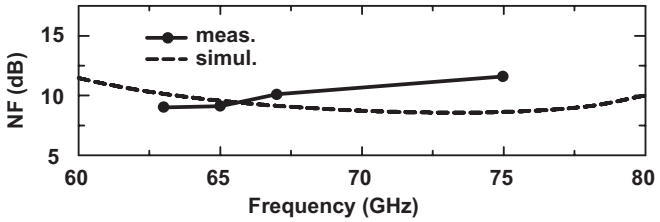


Figure 2.17: Measured and simulated noise figure.

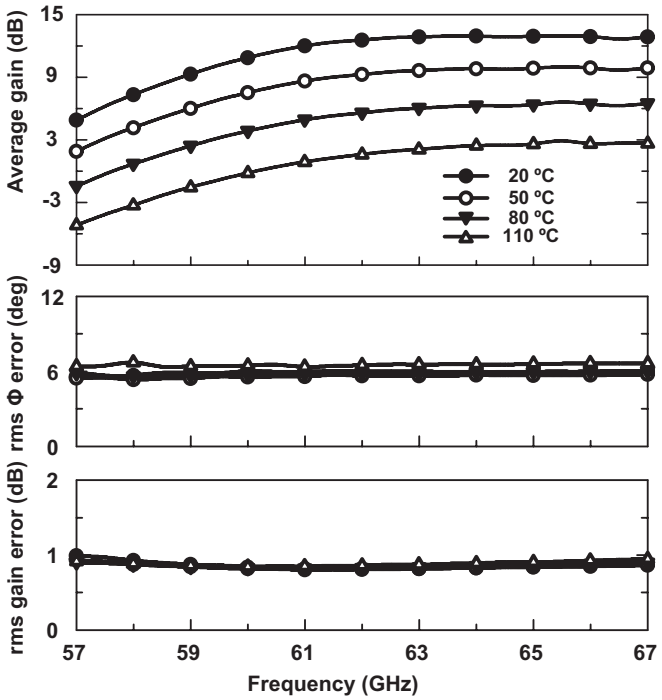


Figure 2.18: Measured gain and rms errors at different temperatures.

circuits as shown in [10]. On the other hand, the rms phase and gain errors remains the same showing that the vector modulator amplifiers track each other over a wide temperature range.

2.4 Conclusion

This paper presents an improved QAF and its implementation in 60–80 GHz active phase shifter using a 0.13 μm SiGe BiCMOS technology. It is demonstrated that with the inclusion of an Rs/R=0.5–1 in the quadrature all-pass filter, the capacitive loading problem is mitigated and the I/Q phase and amplitude errors are minimized. This technique is especially suited for wideband millimeter-wave circuits which naturally result in a high C_L/C values and cannot be tuned using narrowband techniques. A prototype wideband receiver resulted in state-of-the-art I/Q amplitude and phase balance at 55-78 GHz even with a C_L/C loading of 0.5-0.8.

2.5 Acknowledgment

This work was supported by the Toyota Research Institute of North America (TRINA). The authors thank Dr. Jae Lee and Koji Shiozaki, both at Toyota Research Institute of North

America (TRINA), for technical discussions.

Chapter 2 is mostly a reprint of the material as it is submitted for publishing to IEEE Transactions on Microwave Theory and Techniques, 2012. Sang Young Kim; Dong-Woo Kang; Kwang-Jin Koh; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 3

A 4-bit Passive Phase Shifter for Automotive Radar Applications in 0.13μm CMOS

3.1 Introduction

Phased array systems have been widely used in defense applications such as radars and communication systems to achieve electronic beam forming and fast beam scanning [1]. At millimeter-wave frequency, these have been implemented with GaAs and/or InP based discrete modules, resulting in high cost and low integration density. However, recent development in silicon technologies have led to Si-based phased array on a single chip. This does not only reduce the cost but also multiple elements can be integrated on a single chip with excellent uniformity. A major issue in building phased array is the phase shifter design, especially at millimeter-wave frequencies. The phase shifter can be built using a switched delay [7], loaded reflection [28], loaded line [4] and vector modulation [14]. In this paper, low-pass passive networks with MOSFET switches are used [29].

3.2 Design and Implementation

3.2.1 Process, Transmission Line, Capacitor and RF pads

The 4-bit digital phase shifter is designed using CMOS switches available in the IBM 8HP, 0.12 μm SiGe BiCMOS process. All the inductors used in this design are implemented with

transmission lines as shown in Fig. 3.1. The small capacitors are built using two interconnect metal layers in the process stack-up (Fig. 3.1). Each bit of phase shifter is designed with the input and output impedance of 50 Ω and connected using short 50 Ω transmission lines. A tapered transition between G-S-G pad transition and the transmission line is designed to provide 50 Ω input and output impedance. All the design including transmission lines, capacitors, pads and interconnections are simulated using Sonnet [26], a full-wave EM solver.

3.2.2 Phase Shifter

A 4-bit digital phase shifter with 22.5° phase resolution is designed using CMOS passive switches. The digital phase shifter consumes virtually no power and requires simple digital control circuits. Fig. 3.2 presents the schematic of the 4-bit digital phase shifter. Two 90° phase shifters are tied together to build the 180° phase shifting element. Then, 22.5°, 45° and 90° phase shifter are placed afterwards. Each phase shifter is based on a low-pass network which consists of one series inductor and two shunt capacitors [29]. The network can switch between a phase-delay state and a bypass state using CMOS passive switches. When T1 is off and T2 is on, Ls and Cp form a low-pass network which results in a phase delay given by $\phi = \sin^{-1}(\omega_{\circ} \mathrm{L}_s/\mathrm{Z}_{\circ})$. However, when T1 is on and T2 is off, Ls and Cp / 2 has minimal effect on the phase which gives a bypass state [29]. Because the junction capacitors of the shunt CMOS switch (T2) degrades the isolation to ground at the bypass state, a shunt inductor Lr is added in parallel with the shunt switch to resonate out the parasitic capacitor at the desired frequency. This is a standard design and has been implemented before at Ka-band [29]. The challenge in this work is to scale it to W-band using 0.13 μm CMOS transistors.

A large CMOS transistor results in a small series resistance, which is desirable for a small insertion loss. However, as the transistor size increases, the capacitive coupling to the substrate increases due to the increased shunt junction capacitances of the source and drain, resulting in an increase of the signal loss. Therefore, the transistor size must be optimally chosen to minimize the insertion loss at the desired frequency [30]. Simulations show that the insertion loss is minimized at 77 GHz when the gate width is 14 μm. Also, the substrate resistance, (Rsub), between source/drain junction and substrate depends on the size and distance of substrate contact [31]. Therefore, large substrate contacts (81 $\times$ 54 m^2) are placed closely around each transistor to minimize the uncertainty and to ensure that Rsub is close 50 Ω, assumed by the IBM model [32]. Also, the CMOS gate node is biased using a large resistor, Rc = 22 kΩ, which prevents signal leakage and oxide breakdown [33].

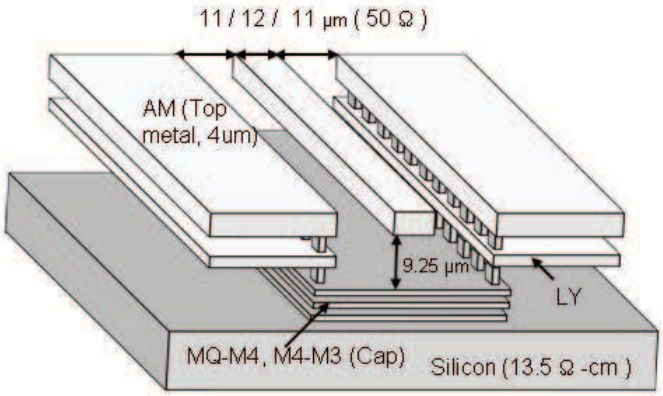


Figure 3.1: The grounded-CPW transmission line and Metal-Oxide-Metal capacitor.

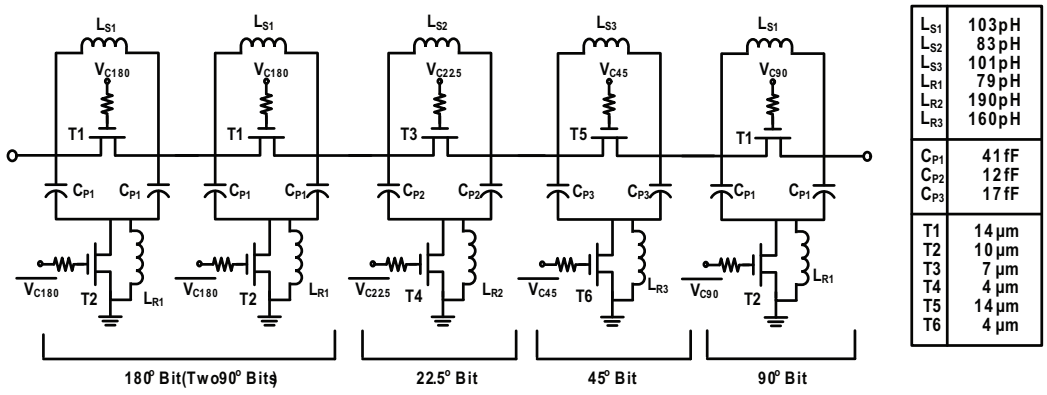


Figure 3.2: Schematic of the 4-bit digital phase shifter.

Fig. 3.3 presents the chip photograph of the designed phase shifter. The values of the inductors are shown in Fig. 3.2 and each is translated to an equivalent short transmission-line stub. The chip size is 450 $\times$ 300 m^2 without pads. The inductors and capacitors are designed using a full-wave electromagnetic simulator and therefore the interconnect and mutual coupling effects are taken into account.

3.3 Measurements

The 4-bit digital phase shifter was measured using an Agilent E8361A 67 GHz PNA with extenders up to 110 GHz. All the measurements were done with SOLT calibration to the probe tips. The probe loss and transition to the CPW line are included in the measurements. Fig. 3.4 presents the measured phase response of the phase shifter for all 16 different phase states over 67-82 GHz. It is seen that 180° and 90° phase shifters result in excellent phase performance. The measured gain of all 16 different states and the average gain are shown in Fig. 3.5. The phase shifter results in -19.2$\pm$3.7 dB of gain at 77 GHz, which includes 1 dB pad loss. The RMS phase error and RMS gain error are 10.8° and 2.4 dB at 77 GHz as shown in Fig. 3.6, respectively. The input return loss is $<$ -10 dB over 67-82 GHz for all 16 states (Fig. 3.7). The output return loss is $<$ -10 dB over 67-81 GHz as shown in Fig. 3.8 for all 16 states. The measured and simulated gain are shown in Fig. 3.9 vs. phase state. One can clearly notice that the transistor insertion loss (or Ron) is not accurately modeled since the measured insertion loss at the 0° state is 5 dB higher than the simulated gain. In this case, all the series transistors are biased ON, and therefore each stage has approximately 1 dB higher insertion loss than simulated. On the other hand, when all the shunt transistors are turned ON, 337° (phase delay state), then the measured and simulated insertion loss are nearly the same. Also notice the measured large insertion loss variation when the 90° state is toggled. This is currently being investigated and is not available in the simulations. The measured 1 dB gain compression point is $>$ 8 dBm as shown in Fig. 4.17 and is limited mainly by the available test power. The simulated IIP3 is $>$ 22 dBm, and is not measured.

3.4 Conclusion

A 67-78 GHz 4-bit passive phase shifter using CMOS switches available in 0.12 μm SiGe BiCMOS process is presented. The RMS phase error is $<$ 11.25° over 67-78 GHz, respectively. The phase shifter must be combined with a 20 dB gain LNA/VGA to compensate for its

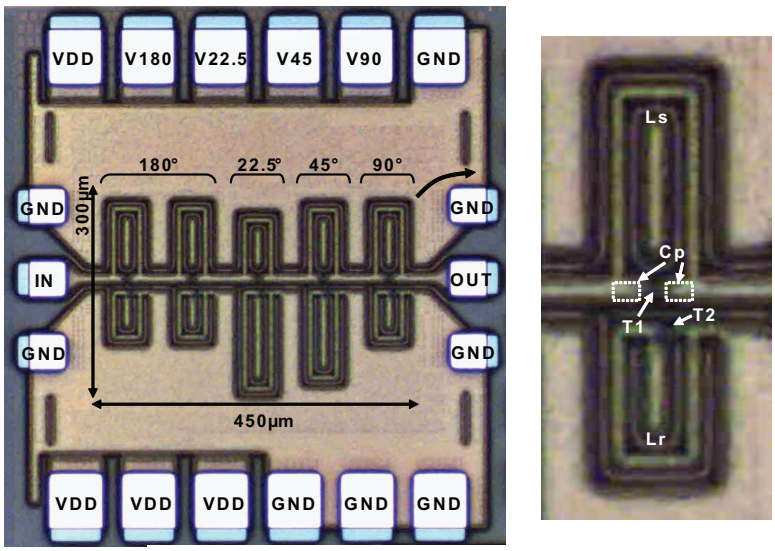


Figure 3.3: Chip photograph of (a) 4-bit digital phase shifter and (b) 90° phase shifter cell.

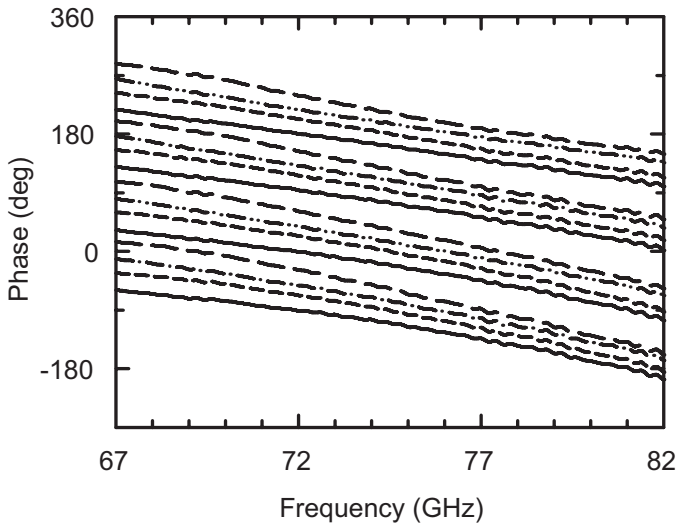


Figure 3.4: Measured phase response of 16 different phase states.

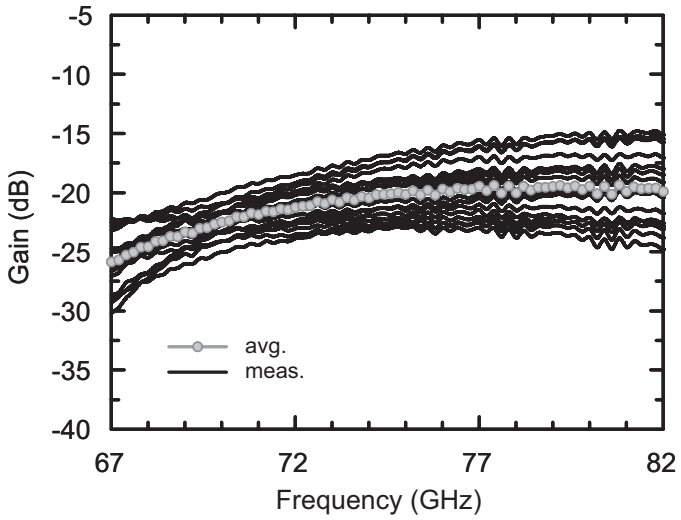


Figure 3.5: Measured gain response of 16 different phase states and average gain.

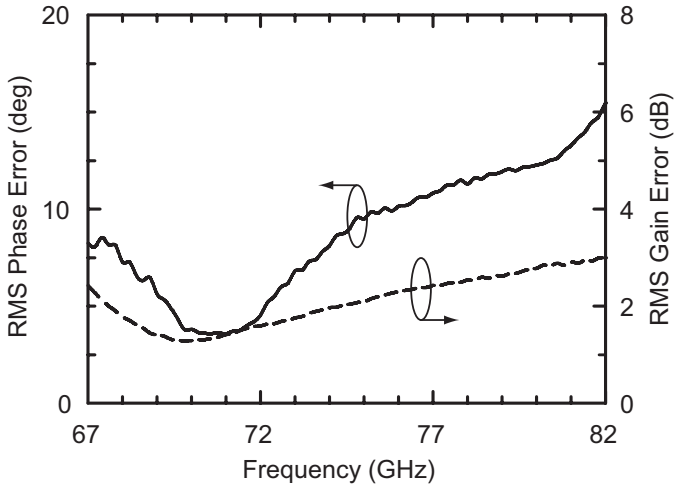


Figure 3.6: RMS phase error and RMS gain error of 4-bit phase shifter.

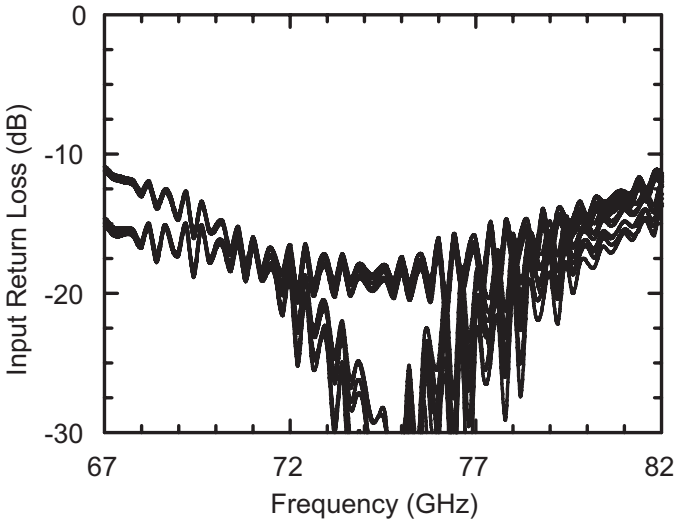


Figure 3.7: Measured input return loss of 16 different phase states.

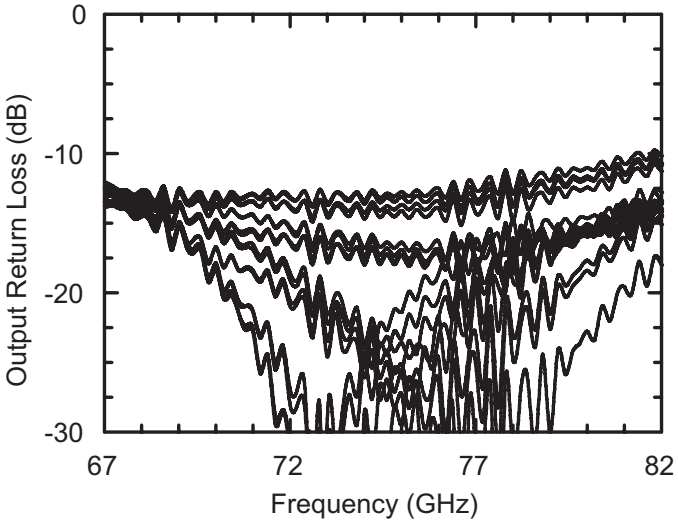


Figure 3.8: Measured output return loss of 16 different phase states.

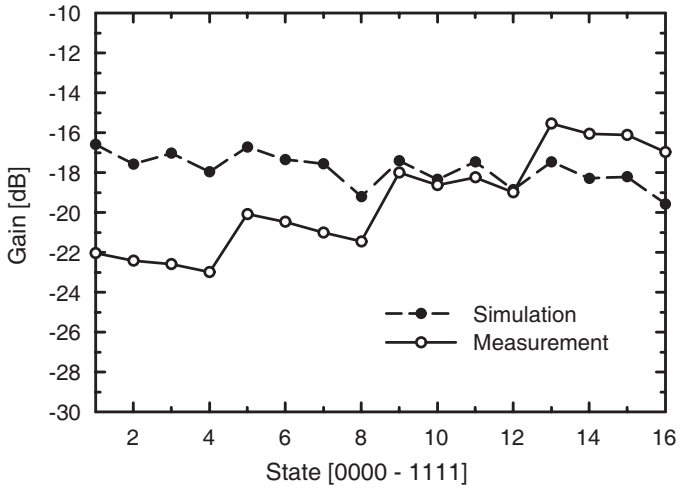


Figure 3.9: Measured and simulated gain vs. phase states.

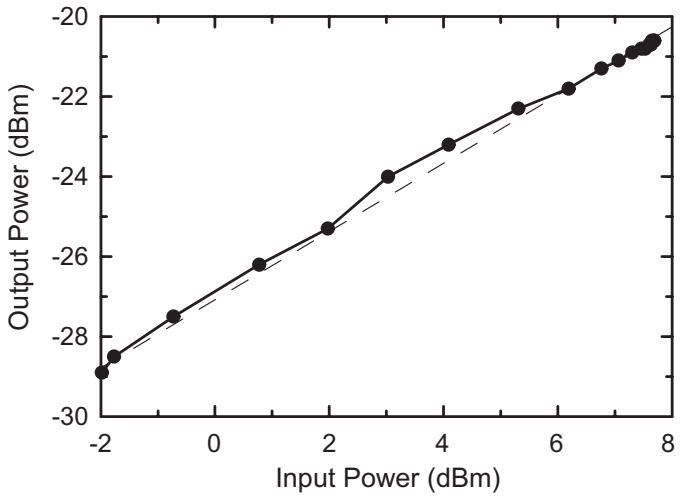


Figure 3.10: Measured output power vs. input power.

loss and gain variation for millimeter-wave applications. The passive phase shifter is very small and is therefore excellent for array applications without taking a lot of space on the RFIC wafer.

3.5 Acknowledgment

This work was supported by the Toyota Research Institute of North America (TRINA), Ann Arbor, Michigan.

Chapter 3 is mostly a reprint of the material as it appears in IEEE Compound Semiconductor Integrated Circuit Symposium, 2009. Sang Young Kim; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 4

A Low Power 4-Element Phased Array Receiver with Single-Ended Passive Phase Shifter for 76-84 GHz Radar and Communication Systems

4.1 Introduction

Millimeter-wave automotive radar chips, both at 77 GHz (mostly FMCW systems) and at 79-81 GHz (pulse based systems), were recently demonstrated using SiGe and CMOS technologies [34–44]. The SiGe implementations were particularly successful due to their low phase noise performance and their operation at temperatures as high as 125°C which is required in automotive applications. There are two radar platforms for automotive applications: 1) Long-range radars for cruise control (1-200 m) implemented at 76-77 GHz and with 200-1000 MHz bandwidth, and 2) short-range radars (0.5-40 m) implemented at 79-81 GHz using $<$ 1 ns radar pulses for blind-spot detection, lane change, and collision avoidance applications. Both applications require that the antenna beam be scanned in space, and this can be done using switched focal plane systems [45–47], digital beamforming [48,49], or phased arrays [16,50]. The phased arrays for the long range radars are particularly challenging since an 8 cm aperture can be replaced by 8-24 antennas (the number of channels depends on the scanning angle and the number of transmit channels [2]), and therefore, it is advantageous to reduce the power consumption per phased-array element.

The 81-86 GHz band is also used in high-data rate point-to-point communication systems with complex modulation [51–54]. In this case, the band can be used entirely in one shot, or can be subdivided into two different band (81-84 GHz, 83-86 GHz, etc.). These systems are currently based on reflector antennas, but phased arrays are proposed to solve the costly alignment issue between two reflector antennas located on towers. In this case, the SiGe phased array must be proceeded by a low noise InP amplifier (one per channel) since the system NF must have a very low NF ($<$ 4 dB) for long distance communications.

Silicon-based phased arrays have been demonstrated at millimeter-wave frequencies using All-RF, LO and IF beamforming architectures [16, 50, 55–59]. This work is based on the All-RF approach which eliminates the I/Q mixers on each element and the LO distribution network. The RF beamforming architecture can be scaled to a large number of elements (16-32) as shown by UCSD, Intel, IBM and Mediatek at 45-65 GHz [16, 55–57]. A single-element chip and a 4-element chip are presented capable of operation at 76-77 GHz, 79-81 GHz, and 81-84 GHz with low power consumption and wide instantaneous bandwidth.

The phased-array receiver design is single-ended and consumes less power than a differential implementation, but on the other hand, it is sensitive to the grounding inductance when packaged with off-chip antennas. One way to solve this problem is to use on-chip antennas as shown in [60] for a 3x3 wafer-scale power amplifier array. In this case, the antenna and the amplifier/phase-shifter share the same ground and there is no ground transition between the chip and the antennas. Another way is to migrate the design presented in this paper to a differential circuit which is robust to ground inductance transitions as shown in [55].

4.2 Design

4.2.1 Architecture

The 4-element phased-array architecture is shown in Fig. 4.1. The design is based on an amplifier/phase-shifter cell/amplifier approach [61], and the outputs of the 4-element array are added together using a two-stage Wilkinson coupler. Wilkinson couplers are passive devices with high linearity and low loss [62], and are ideal at mm-wave frequencies due to their relatively small size and low loss [6, 63]. The amplifiers are implemented using 0.13 μm SiGe transistors with a f_T / f_{max} of 200 / 220 GHz, and the phase shifters are based on switched-LC networks implemented using 0.13 μm CMOS transistors (available in the IBM 8HP process) [32]. The phase shifters show high linearity (IIP3 of $\sim$23 dBm) and zero power consumption, but have a simu-

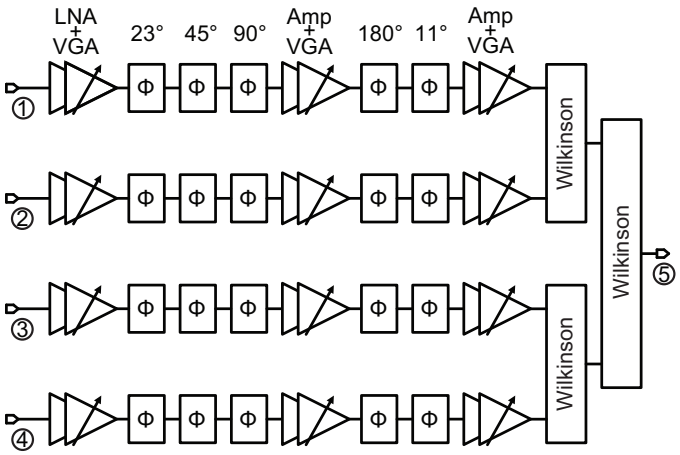


Figure 4.1: W-band 4-element phased-array architecture.

lated loss of 17-20 dB for a 5-bit design due to the channel resistance and parasitic capacitance of the 0.13 μm CMOS transistors [6, 30, 64].

Fig. 4.2 and Table 4.1 compare three different topologies for the phased-array element: Topology 1 is based on a traditional design with an LNA in front followed by a 5-bit phase shifter, topology 2 divides the amplifier into two units, one at the input and one at the output of the phase shifter, and topology 3 distributes the amplifiers and phase shifters throughout the chain. The design is done for an input P_{1dB} of -26 dBm and a gain of 16 dB at 81 GHz. Topology 1 results in the lowest NF but with the highest power consumption due to the 36 dB amplifier gain required to overcome the 20 dB phase shifter loss. This results in an P_{1dB} of +10 dBm at the output of the LNA and high power consumption. Also, due to the potential of substrate coupling, it is not advisable to design 36 dB gain amplifiers in single-ended systems [65]. Topology 2 results in the highest NF, and this is not acceptable. It is seen that topology 3 results in a NF of 11.4 dB and with a power consumption of only 32 mW per channel, roughly quarter of topology 1.

4.2.2 Amplifiers

The 4-element phased array is built using the IBM 8HP process with 7 metal layers and a 4 μm thick top layer (AM) (Fig. 4.3). The coplanar-waveguide (CPW) transmission lines are built using the AM and MQ layers with a 9.2 μm thick interlayer dielectric, and have a simulated loss of 0.75 dB/mm at 80 GHz for a 50 Ω line. Fig. 4.4 presents the simulated f_{max} and f_T for a 5 $\times$ 0.12 μm common-emitter transistor given by the IBM model (reference to M1) and including the full electromagnetic (EM) simulation up to AM layer. It is seen that the EM-simulated f_T

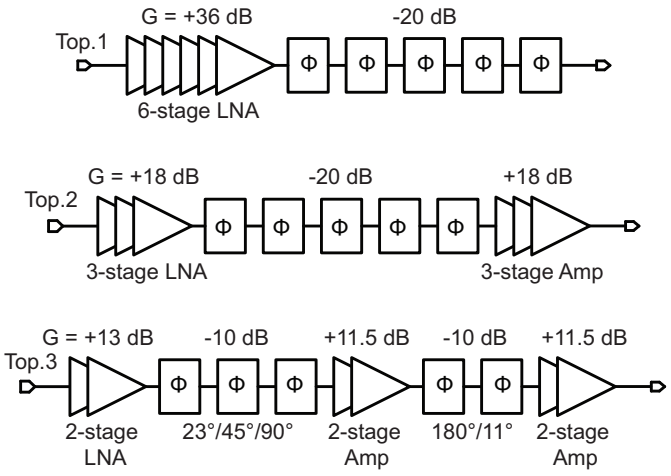


Figure 4.2: Comparison of three different architectures, at 80 GHz.

Table 4.1: Comparison of three different topologies

	Gain (dB)	NF (dB)	IP1dB (dBm)	Power Cons. (mW)
Topology 1	16	8.4	-26	120
Topology 2	16	12.5	-26	32
Topology 3	16	11.0	-26	32

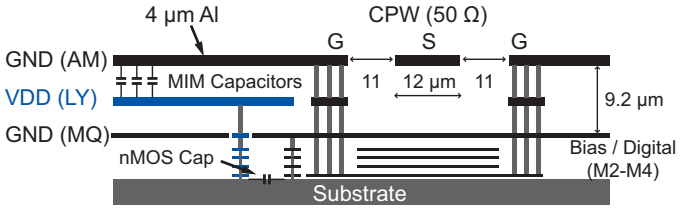


Figure 4.3: IBM 8HP metal stack-up with a presentative 50 Ω CPW line.

and f_{max} are lower than the values obtained using the IBM model. This has significant effect on the gain and NF of mm-wave amplifiers and is therefore essential for accurate circuit design.

A two-stage cascode-based LNA with a center frequency of 81 GHz is used with conjugate inter-stage matching for maximum gain (Fig. 4.5(a)). The second stage is gain controlled using 2-bit current steering (0/-0.2/-2.3/-4.0 dB relative gain). Resistors are placed in shunt with the load inductors in order to widen the 3 dB bandwidth to 19 GHz at the expense of 0.5 dB in additional noise. The inductors are designed using microstrip lines between AM and M1, with a width of 6 μm and Q of 18 at 81 GHz, and are EM modeled by Sonnet [26]. C1 (40 fF) is built using custom capacitors between M3 and M4 with a simulated Q of 40 at 81 GHz. The current bias is done at 0.6 mA/μm to result in the lowest noise figure and is less than the optimal bias current for highest gain as given by the IBM design manual [32]. A simulated gain and noise figure of 9.9-12.2 dB and 8.2-8.8 dB, respectively, are obtained at 76-85 GHz for a total bias current of 6 mA. The amplifier results in a wide impedance match (S_{11}, S_{22} $<$ -10 dB at 72-100 GHz, 74-91 GHz respectively) and a P_{1dB} of -21 dBm. The other variable-gain amplifiers are identical to the two-stage LNA.

An essential design tool at millimeter-wave frequencies is the global analysis and optimization of the two-stage cascode amplifier (Fig. 4.5(b)). In the layout around the transistors, the ground plane is dropped from MQ to M1 to result in a low emitter inductance, and the inductors are based on microstrip-lines using AM and M1 layers. The entire circuit is modeled using Sonnet with internal ports for the base-emitter-collector nodes, and the ports are attached to the IBM transistor models in the Cadence. This takes into account the full-wave electromagnetic effects of the vias around the transistors and any coupling between the inductors in the amplifier. The Sonnet simulation takes 4 hours to analyze the cascode amplifier from 0.1 to 200 GHz on a modern desktop station (Fig. 4.5). The global modeling and optimization technique, while time intensive, results in excellent comparison between simulations and measurements (see Section III).

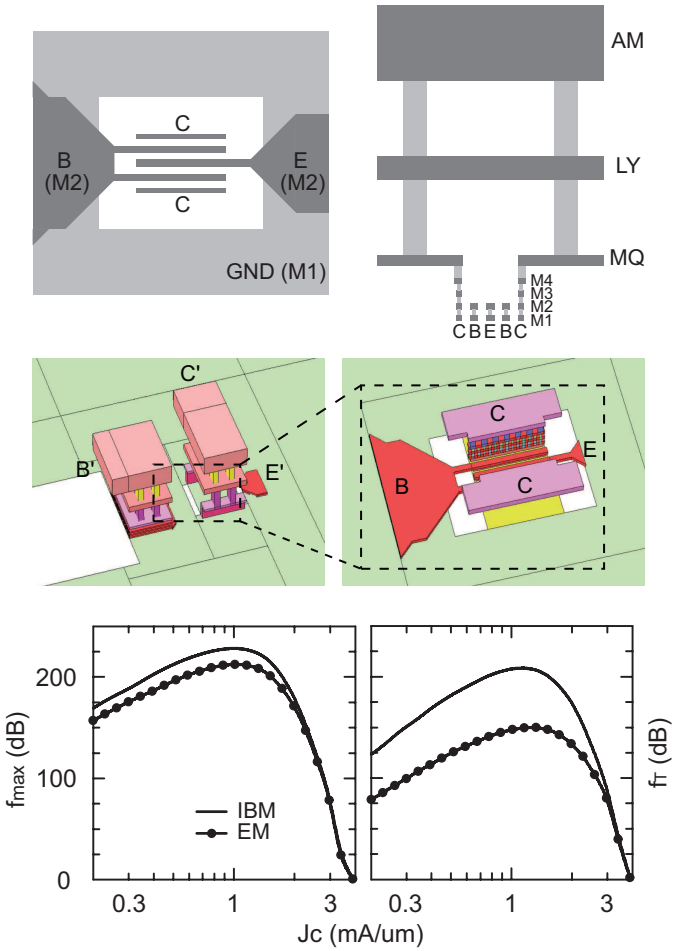


Figure 4.4: Simulated f_{max} and f_T without and with EM simulation (transistor size = 5 μm x 0.12 μm.)

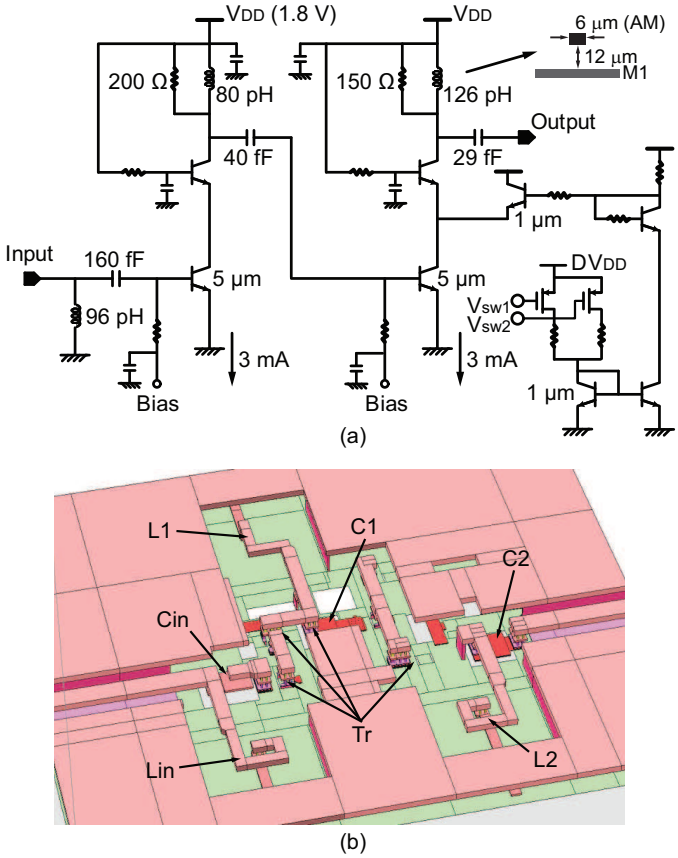


Figure 4.5: (a) Schematic and (b) layout of the 2-stage W-band cascode amplifier with gain control.

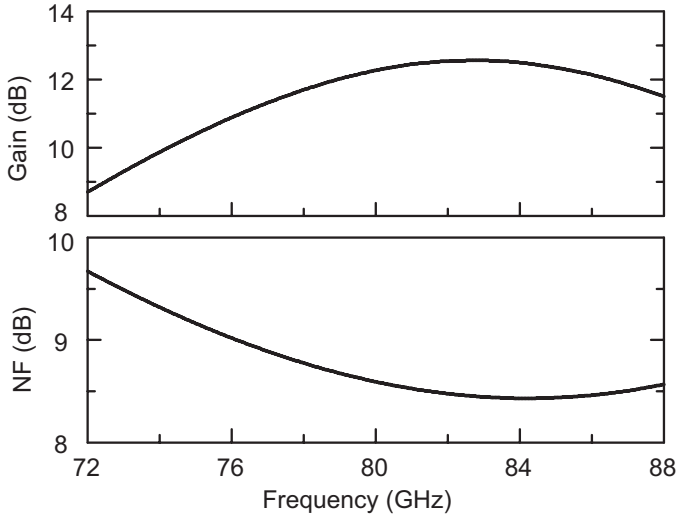


Figure 4.6: Gain and noise figure of the 2-stage W-band cascode amplifier.

4.2.3 Phase Shifter Design

The design of the phase shifter is based on switched 50 Ω low-pass networks for the 11°, 22.5°, 45° and 90° bits, and the 180° bit is built using two 90° bits under the same control voltage (Fig. 4.7) [30]. In the bypass-state, T1 is ON and T2 is OFF, Lr resonates with the off-state capacitance of T2, creates an open-circuit at node A, and port 1 is connected to port 2 using T1. In the phase-delay state, T1 is OFF and T2 is ON, T2 connects point A to ground, and port 1 is connected to port 2 using the low-pass network Cp-Ls-Cp. The phase delay is determined by the choice of Cp and Ls, and is linear with frequency within a ± 10 % frequency range.

The transistors (T1, T2) must be chosen to result in relatively low insertion loss when the transistors are ON, but on the other hand, the 0.13 μm CMOS technology results in a large substrate capacitance which contributes to high insertion loss at 77-85 GHz even when the transistors are off. T1 and T2 are therefore chosen to result in similar insertion loss in the bypass and phase-delay states (see Table 4.2). Fig. 4.8 presents the simulated gain and phase response of the individual phase shifter cells. The 90° bit is challenging due to the large Cp-Ls-Cp values used, and results in an insertion loss of 4.0-4.2 dB (8.2-8.5 dB for the 180° bit) and an S_{11} (or S_{22}) $<$ -11.5 dB from 75-85 GHz in the phase-delay state. In order to alleviate the effect of the S_{11} mismatch, the 90° and the 180° cells are placed next to the central amplifier which is a well-matched 50 Ω impedance block. The inductors are designed using Sonnet and based on high-impedance transmission-lines (Z_o=70.7 Ω, 2 dB/mm, Q=13 at 80 GHz), and global EM simulation is performed (see Fig. 4.7 for the Sonnet EM model). Also, the 22°/45°/90° and the 180°/11° bits are simulated together in Sonnet and Cadence in order to ensure low electromagnetic coupling between the individual bits and a wideband impedance match.

This phase shifter topology results in gain variation over the 16 states due to the loss and impedance variation between the two states of each cell, and the cascade of non-ideal 50 Ω blocks (especially the 45°, 90° cells). Simulations indicate a gain of -17 to -20 dB over the 32 states at 81 GHz. The variable gain amplifiers are therefore essential to compensate for this effect and to result in a low rms gain error.

4.2.4 2-stage Wilkinson Combiner

The 50 Ω Wilkinson combiners are designed using two λ/4 sections of 70.7 Ω CPW lines (Q=13 at 80 GHz) and result in an insertion loss of 0.9 dB and S_{11}/S_{22}/S_{33} $<$ -20 dB at 72-88 GHz (Fig. 4.10). The isolation between the two ports, S_{23}, is $>$ 25 dB at 72-88 GHz. The Wilkinson combiner is wideband and has no effect on the channel S-parameters except for

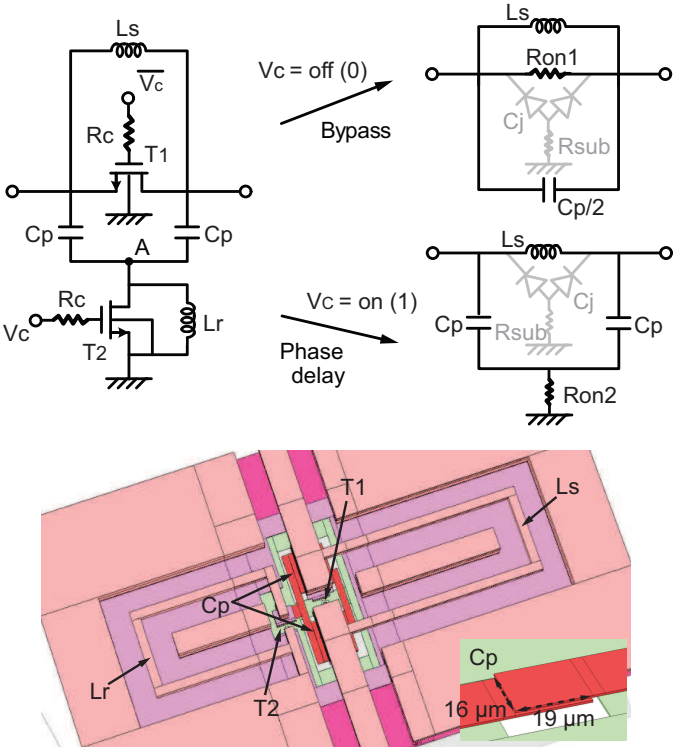


Figure 4.7: Design of switched-delay CMOS phase shifters.

Table 4.2: Phase Shifter Component values.

	11°	22°	45°	90°	180°
T1/T2 (µm)	7/4	7/4	14/4	14/10	14/10
Ls (pH)	65	70	80	74	74
Cp (fF)	12	12	17	41	41
Lr (pH)	117	107	92	62	62
Bypass loss (dB)	2.5	2.9	3.8	4.4	8.7
Delay loss (dB)	1.4	1.6	2.7	4.0	8.3

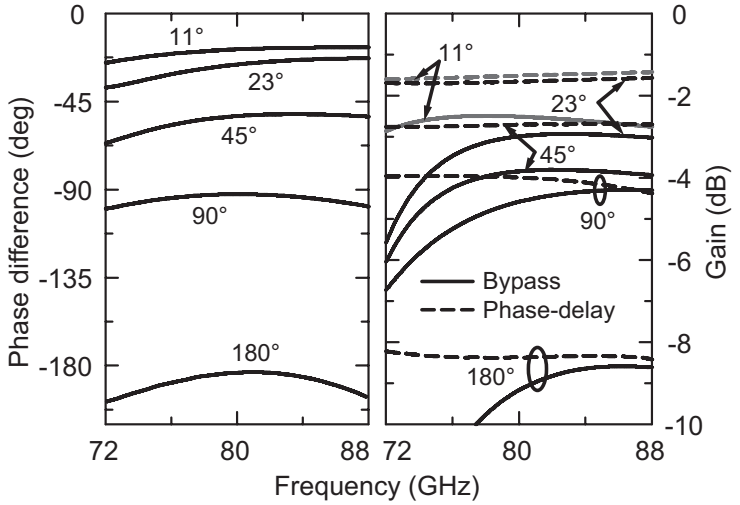


Figure 4.8: Simulated switched-delay CMOS phase shifter cells.

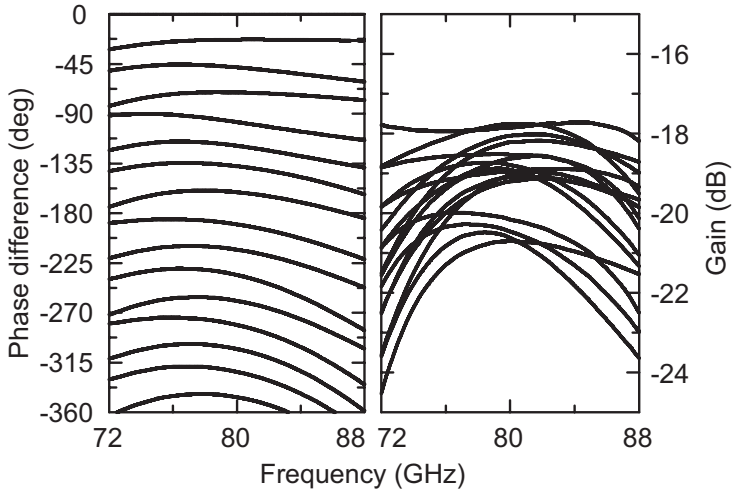


Figure 4.9: Simulated phase difference and gain of the total phase shifters.

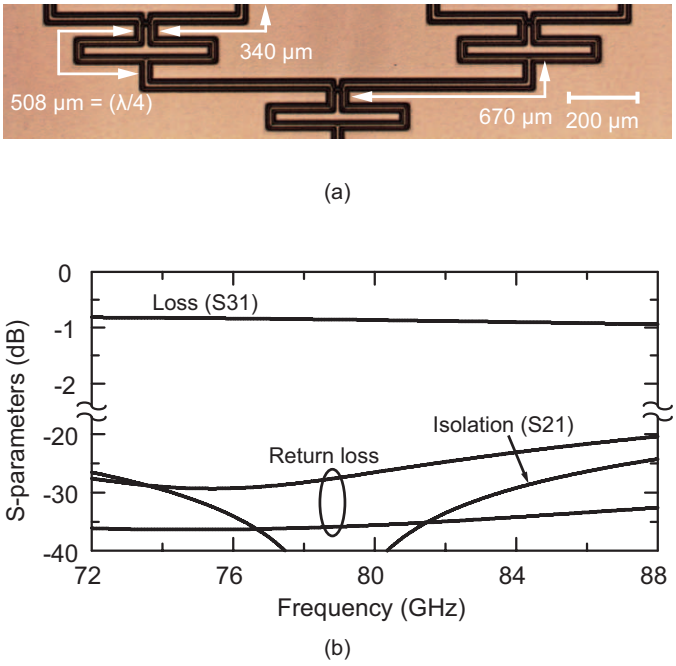


Figure 4.10: Simulated S-parameters of a single-stage Wilkinson coupler.

an additional 0.9 dB loss per stage. Again, the 4:1 Wilkinson combiner is electromagnetically modeled in Sonnet and its S-parameter block is used in Cadence.

4.2.5 Phased Array Simulations

The simulated average gain of a single channel is 16.1 dB at 80 GHz for the 16 phase states, with a corresponding noise figure of 11.1$\pm$0.6 dB, an input P_{1dB} of -27 dBm, and a power consumption of 32 mW (1.8 V, 18 mA). The simulated S_{11} and S_{22} are $<$ -10 dB from 73 GHz to $>$ 90 GHz. The gain can be controlled by 9.5 dB in 1.6 dB steps. An important design aspect is that the channel phase does not change by more than $\pm 4^{\circ}$ over a large gain-control range. This allows the variable gain amplifiers to correct for the gain change vs. phase state without adding additional phase errors. The 4-element array results in a similar performance as a single channel but with an additional 2.4 dB loss at 81 GHz: 1.8 dB loss due to two Wilkinson couplers and 0.6 dB for the added transmission lines.

Since this is a single-ended design, the phased array channels are placed 600 μm from each other, and the area between the channels is filled with Vcc decoupling capacitors (23 pF per channel) and with metal walls which connect the AM metal layer to the substrate. The

input GSG (CPW) pad transition is designed using Sonnet and includes a short high-impedance tapered section to match the pad capacitance at 70-90 GHz, and results in $S_{11} \leq$-20 dB and $S_{21} \leq$ -0.2 dB at 75-85 GHz.

4.3 Measurements

Fig. 4.11 presents microphotographs of a single-channel chip and a 4-element chip. All measurements are done on-wafer using an Agilent E8361A Vector Network Analyzer with extenders to 110 GHz. A probe-tip calibration is first done using the Cascade 138-357 calibration substrate [27], and the measurements include the GSG pad transition loss. Several chips were measured and resulted in similar measurements.

Fig. 4.12 presents the measured gain response of a stand-alone test chip with 23°/45°/90° phase shifters. The measured average gain agrees well with simulations, but has larger variation vs. phase states at $>$ 82 GHz than predicted by simulations. It shows good matching between the simulated and measured average gain of the phase shifters.

Fig. 4.13 and Fig. 4.14 present the measured S-parameters of a stand-alone single channel for 16 phase states and the bias conditions are V_{DD} = 1.8 V and a current of 18.3 mA/channel. A wideband input and output matching is achieved with a rms gain and phase error of 2.2-3.5 dB and $\leq 15^{\circ}$, respectively, at 76-84 GHz. Comparison with simulations indicates excellent match with S_{11}, S_{22} and the average S_{21}, but again with a higher rms gain and phase error. This is attributed to the phase shifter cells which showed higher loss than simulations due to inadequate 0.13 μm transistor models at 75-85 GHz. The measurement also shows 13 dB of gain control with $\leq \pm 4^{\circ}$ phase change over a 10 dB control range (Fig. 4.15). The nominal state in Fig. 4.15 is the gain-state setting which is used for all measurements (S-parameters in Figs. 4.13 and 4.14).

The measured NF and input P_{1dB} were also done on the single channel chip and are shown in Fig. 4.16 and Fig. 4.17. The NF measurements are done at the nominal gain state so as to yield the average NF seen by the phased array channels when the gain control is used. The measured average NF is 10.5 dB at 80 GHz which agrees well with simulations (11.1 $\pm$ 0.6 dB at 80 GHz for all phase states). The measured input P_{1dB} is -26.7 to -23.0 dBm at 77-80 GHz depending on the gain setting and also agrees well with simulations.

The rms gain error can be substantially reduced using the variable gain amplifiers, and the rms phase error can also be corrected using the 11° phase bit as a trim bit. Fig. 4.18 and Fig. 4.19 present the achieved performance at 76-77 GHz (gain control only), 79-81 GHz (gain

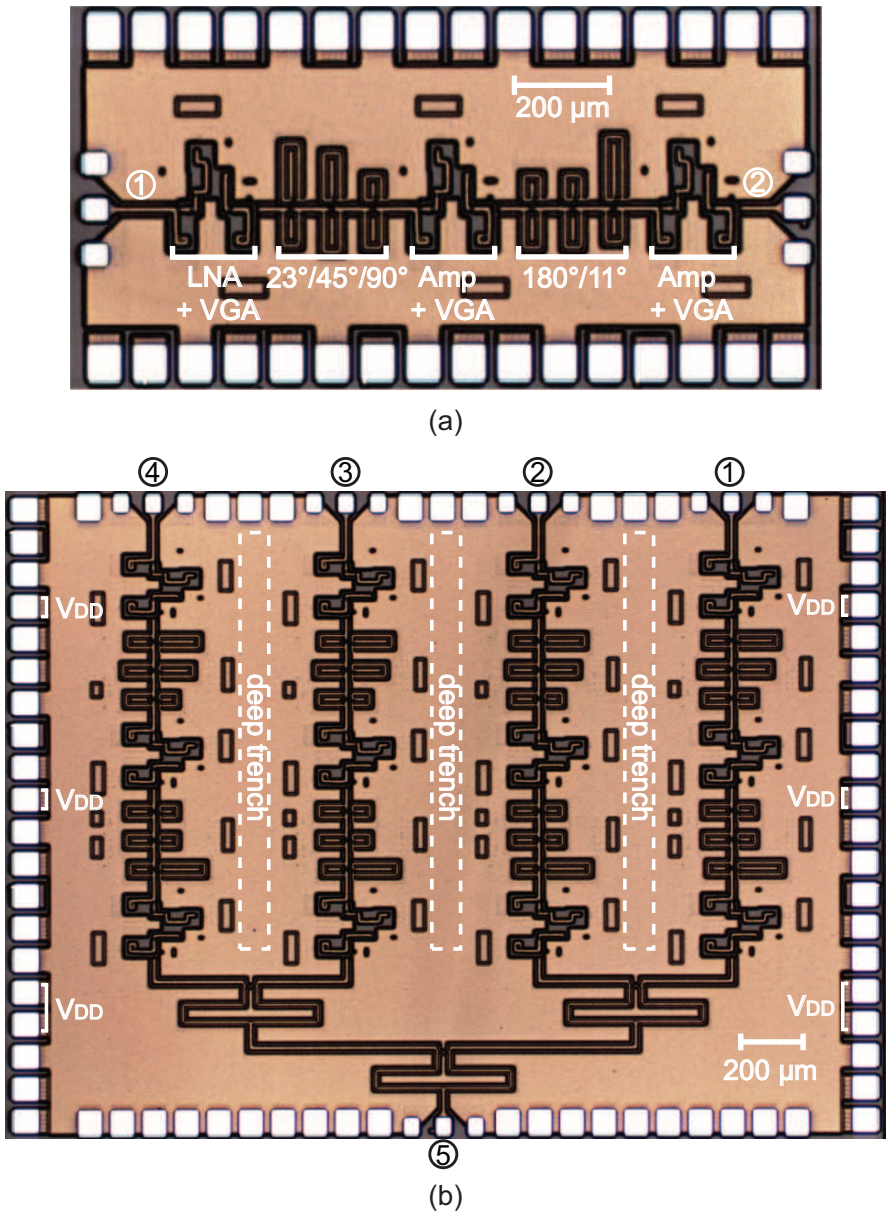


Figure 4.11: Photograph of (a) single channel (1.6×0.8 mm^2) and (b) 4-element phased arrays (2.0×2.7 mm^2).

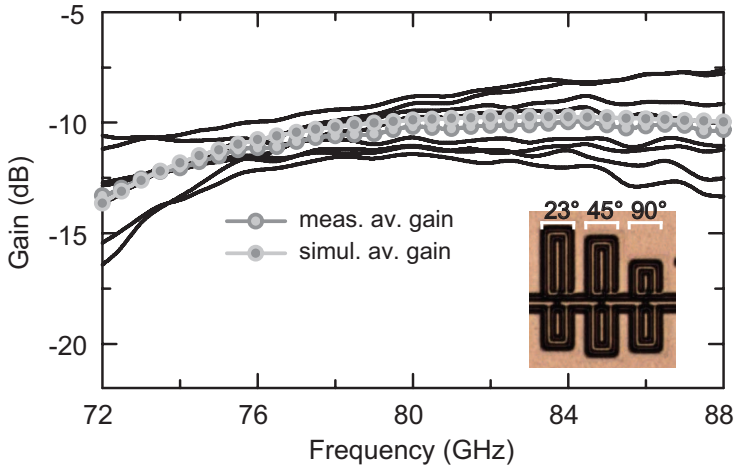


Figure 4.12: Measured and simulated gain of the 23°/45°/90° phase shifter cell.

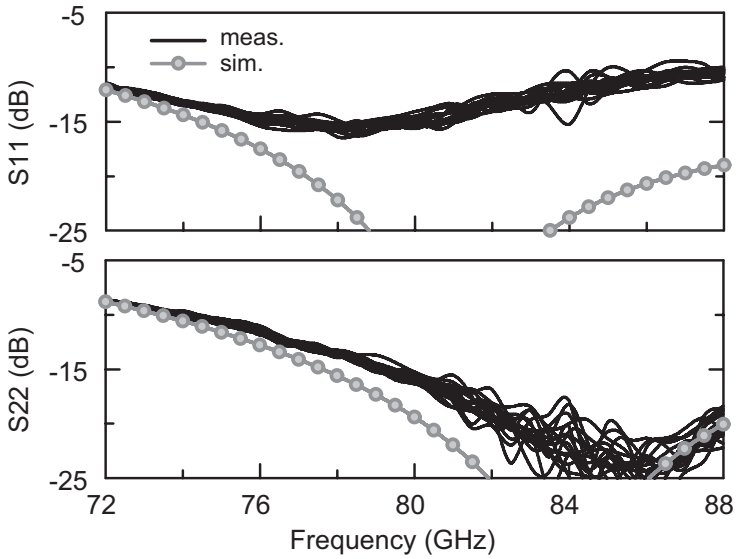


Figure 4.13: Measured S_{11} and S_{22} for 16 phase states.

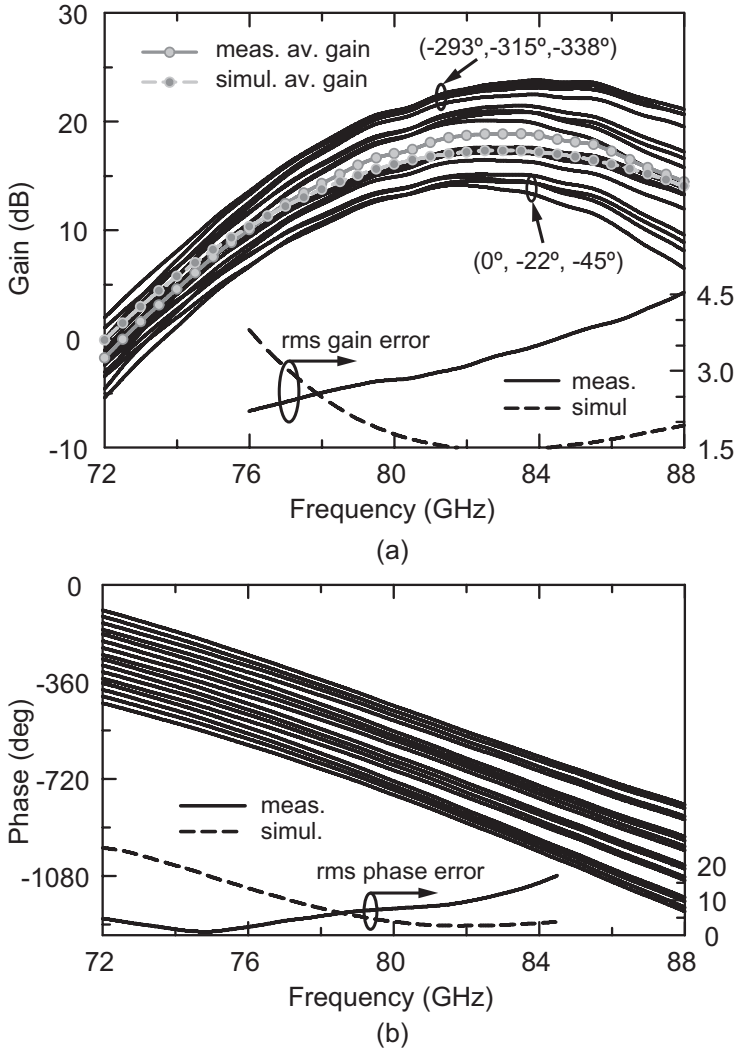


Figure 4.14: Measured (a) gain and (b) phase response vs. 16 phase states.

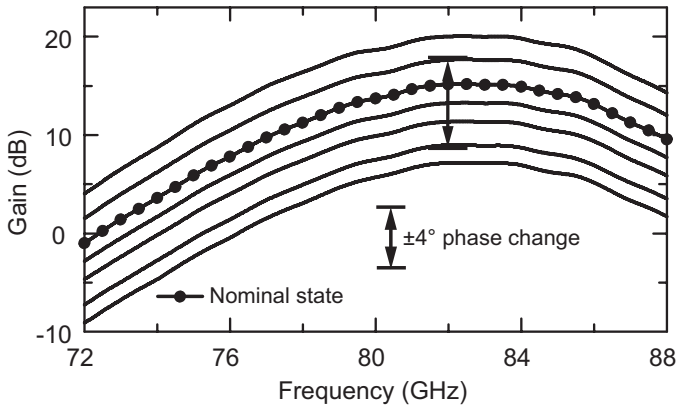


Figure 4.15: Measured VGA operation at the (1,1,1,1) state.

control and 11° phase trim), and 81-84 GHz (gain control and 11° phase trim). In Fig. 4.19, the small phase change between the raw data and the gain control data is due to the variable gain amplifier. The simulated NF under low rms gain and phase states is within ± 0.5 dB of the nominal-state values shown in Fig. 4.16. The phased array can be used in the automotive bands with instantaneous bandwidth of 500 MHz (76.5 GHz) and 2 GHz (79-81 GHz), and is also usable in the 81-84 GHz band.

The 4-element chip consumes 74 mA (V_{DD} = 1.8 V) and results in virtually identical performance to the single element chip except for an additional 2.5-3.8 dB loss at 76-84 GHz due to the Wilkinson network (Fig. 4.23). Note that each channel in the 4-element array results in near identical gain vs. frequency, which is typical of SiGe-based circuits and a symmetrical passive combiner [6].

The measured coupling between the different channels is done using S-parameters first (Fig. 4.24(a)), and then by changing the phase of channels 2, 3, 4 and monitoring the S-parameters on channel 1 (Fig. 4.24(b)) [15, 65]. In this case, channels 2, 3, 4 are left open-circuited which results in a worse-case condition for testing. The on-chip coupling is very low, estimated to be $<$ -30 dB between channels 1 and 2 using the vector addition method. The effect of channel 3 and 4 on channel 1 are negligible ($< \pm 0.1$ dB, $< \pm 1°$).

Fig. 4.25 presents the measured gain vs. temperature at nominal settings. The gain is constant up to 75°C and then drops by 3 dB at 100°C. This is achieved by a simple biasing network which employs a diode in the current reference path and results in an increased bias current vs. temperature. As stated above, the amplifiers are biased at 0.60 mA/μm so as to result in a low NF, and the increase in the bias current results in a near constant gain vs. temperature.

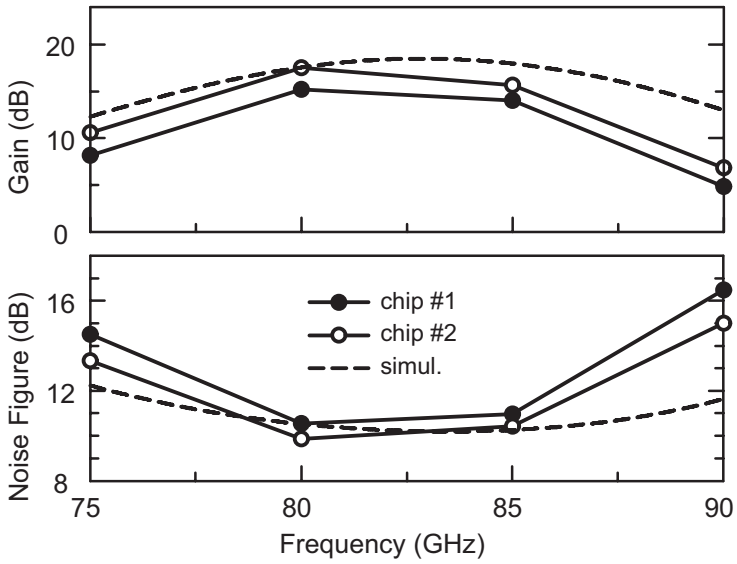


Figure 4.16: Measured gain and noise figure using a hot/cold technique. Gain is set at the nominal state (see text).

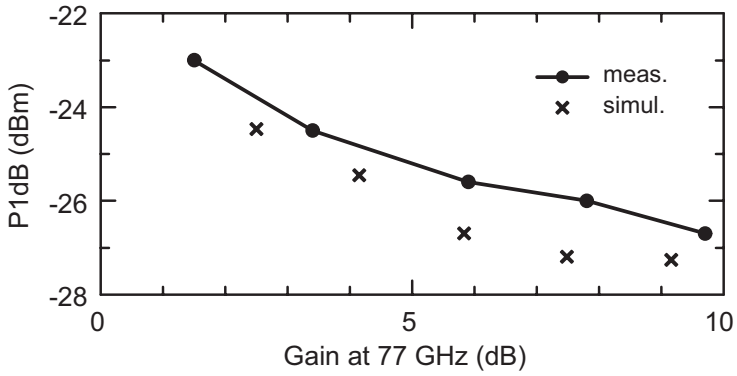


Figure 4.17: Measured input P_{1dB} vs. gain setting at 77 GHz.

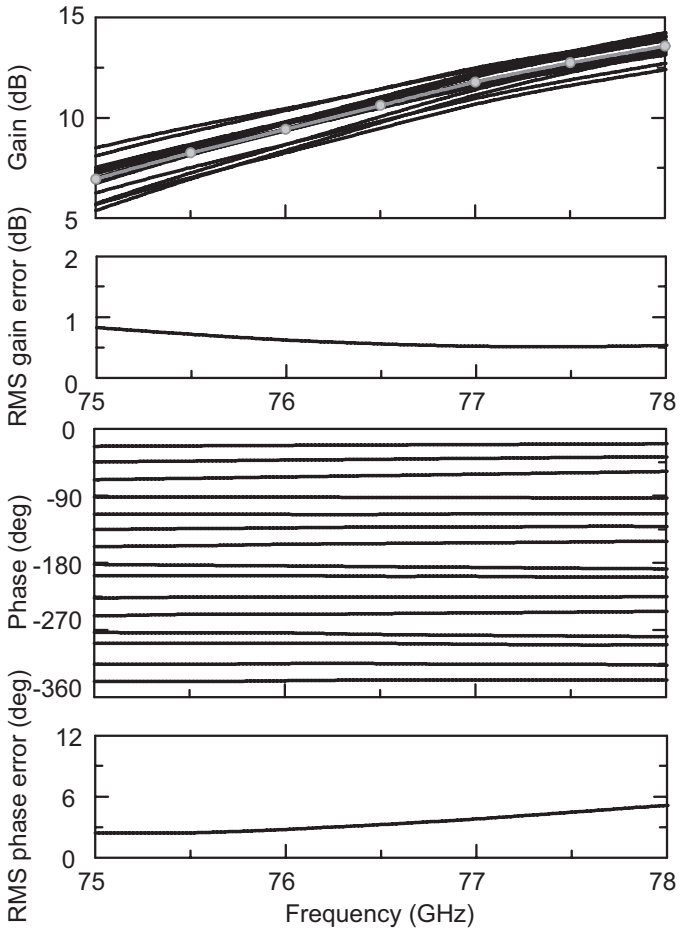


Figure 4.18: Gain, phase, and RMS error after calibration at 76.5 GHz.

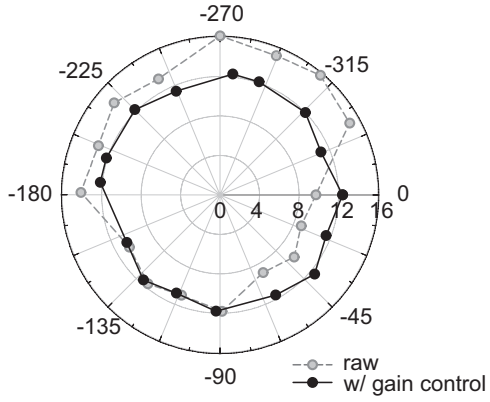


Figure 4.19: Gain and phase correction on a vector chart at 76.5 GHz.

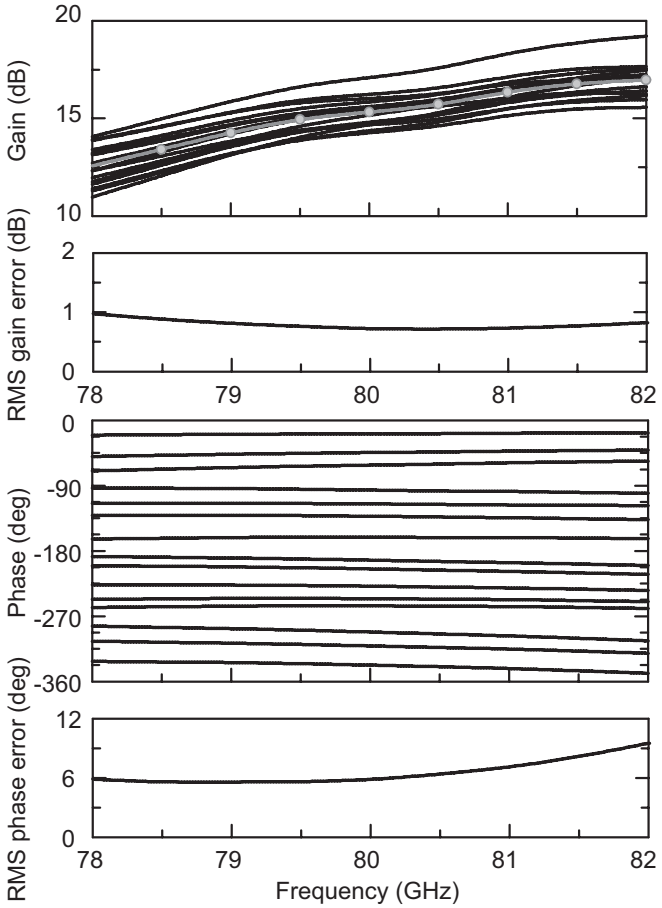


Figure 4.20: Gain, phase, and RMS error after calibration at 80 GHz.

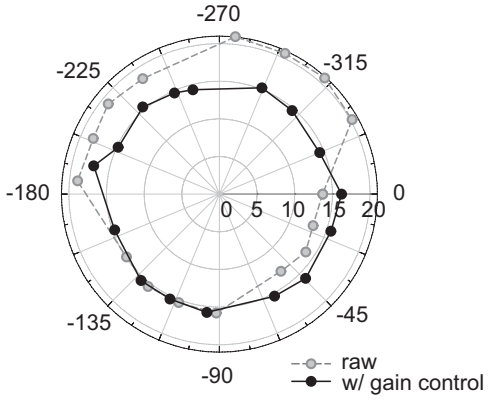


Figure 4.21: Gain and phase correction on a vector chart at 80 GHz.

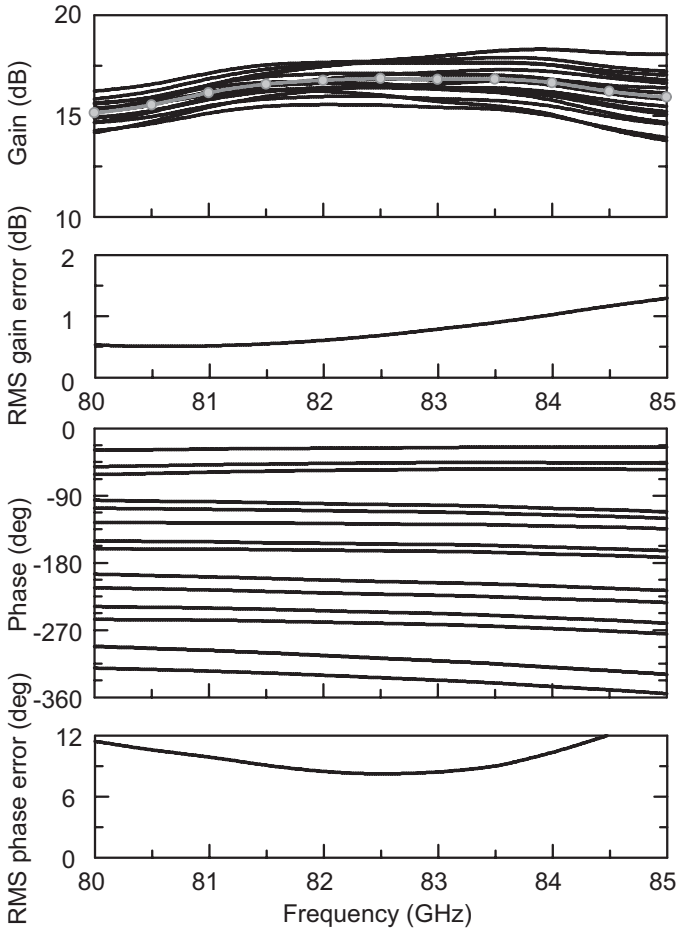


Figure 4.22: Gain, phase, and RMS error after calibration at 82.5 GHz.

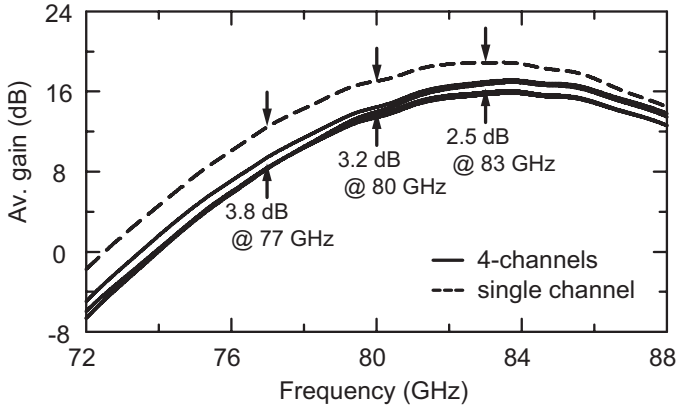


Figure 4.23: Measured average gain of 4-channel phased array chip and single channel chip.

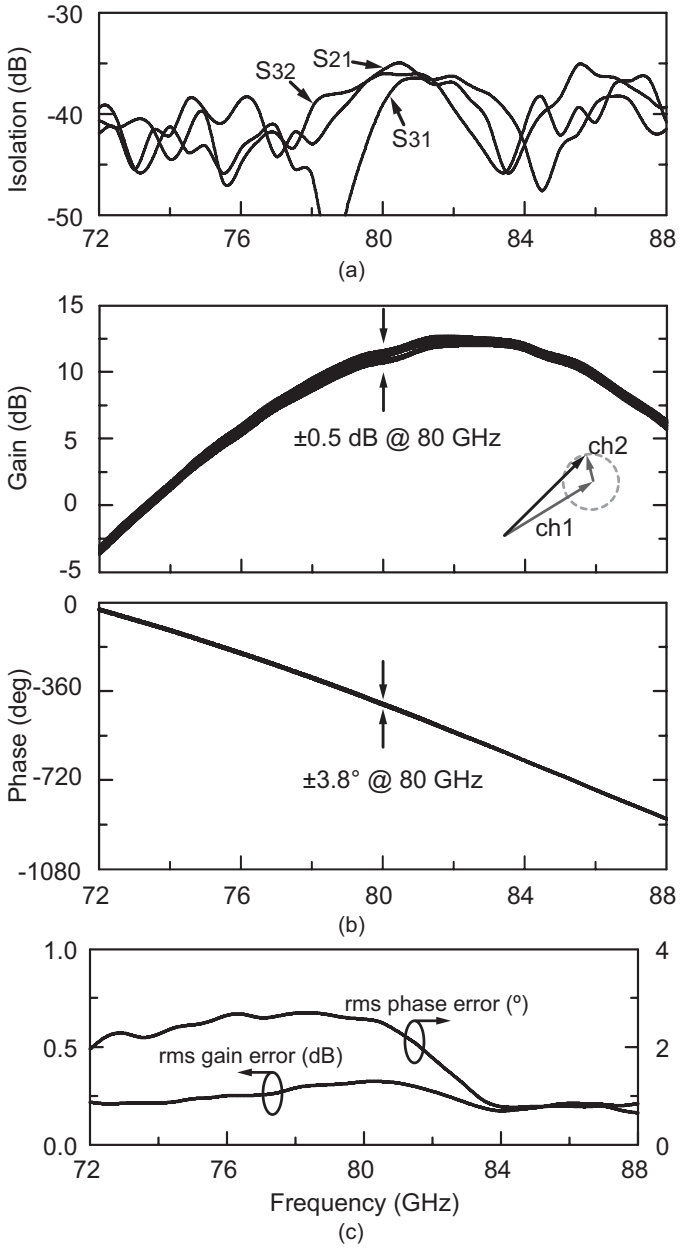


Figure 4.24: (a) Measured S-parameters coupling between the channels, (b) the effect of channel 2 phase change on channel 1, and (c) rms gain and phase error in channel 1 due to the phase change in channel 2.

The phase performance vs. temperature remains essentially unchanged as shown by simulations and as demonstrated in similar circuits at 30-40 GHz [6]. The chip performance is summarized in Table IV.

4.4 Conclusion

A 76-84 GHz 4-element phased array receiver was demonstrated in a 0.13 μm BiCMOS process. The rms gain and phase error were mostly due to inaccuracies in the transistor switch model, but can be corrected using a VGA and an 11° trim bit. Also, the phase shifter loss is high due to the use of the 0.13μm CMOS technology. The results indicate that this topology can be applied at 60-120 GHz using advanced CMOS nodes (65 nm, 45 nm). The single-ended design can be extended to a differential topology which is less sensitive to ground inductance and packaging effects.

4.5 Acknowledgements

This work was supported by the Toyota Research Institute of North America (TRINA). The authors thank Dr. Jae Lee and Koji Shiozaki, both at Toyota, for technical discussions.

Chapter 4 is mostly a reprint of the material as it appears in IEEE Journal of Solid-State Circuits, 2012. Sang Young Kim; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

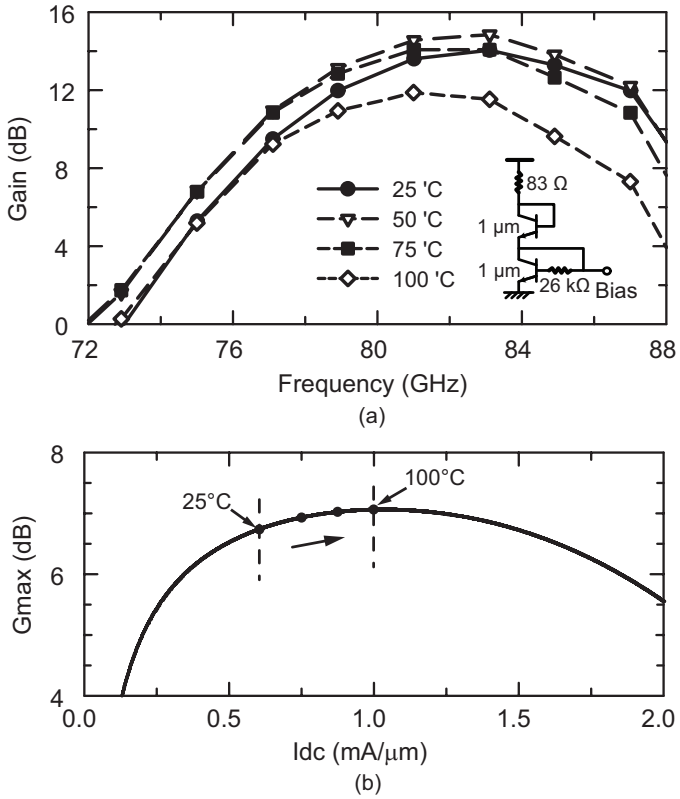


Figure 4.25: (a) Measured gain of a single channel at different temperatures, (b) channel current consumption and bias condition vs. temperature.

Table 4.3: Current consumption vs Temperature

Temp ($^{\circ}$C)	25	50	75	100
Current (mA)	18.5	22.4	26.1	29.3

Table 4.4: Summary of phased array performance.

Technology	0.13 μm SiGe BiCMOS (IBM 8HP)
Frequency band	76-84 GHz
Supply voltage	1.8 V (analog), 1.5 V (digital)
Current consumption	18.0 mA / channel
Chip area	5.4 mm^2 (2.0 x 2.7 mm^2)
Input return loss	-10 dB @ 70-88 GHz
Output return loss	-10 dB @ 74-88 GHz
Power gain (avg.)	10.1 - 18.9 dB @ 76-84 GHz
Phase resolution	4-bit
Gain error (rms)	< 0.6 dB @ 76-77 GHz < 0.8 dB @ 79-81 GHz < 1.1 dB @ 81-84 GHz
Phase error (rms)	< 3.9º @ 76-77 GHz < 7.2º @ 79-81 GHz < 10.4º @ 81-84 GHz
NF	10.5 ± 0.5 dB @ 80 GHz

Chapter 5

A 16-Element 76–84 GHz Differential Phased Array Receiver

5.1 Introduction

This chapter presents a continuation of the design effort presented in Chapters 3 and 4 on millimeter-wave phased array receivers, but using a fully differential circuit topology as opposed to a single-ended topology (chapter 4). The differential topology is less sensitive to packaging effects such as ground plane and V_{DD} inductance and results in very low on-chip coupling. The phased array chip will eventually be packaged either using bond-wires or using flip-chip techniques, and therefore, a differential topology is preferred. However, since the chip is generally pad limited, the inputs are single-ended and the signal is quickly converted to differential mode using an on-chip balun placed directly at the pads.

The 16-element chip is part of a large program which contains a 16-element phased-array front-end, a high linearity receiver including an I/Q mixer and LO distribution, and a novel built-in-self-test (BIST) method. The chapter will report mainly on the phased array front-end and the 16:1 differential Wilkinson combiner since this is the author's work, and will report a bit on the high-linearity receiver and the BIST circuitry.

5.2 Design

5.2.1 Architecture

Fig. 5.1 presents a 76–84 GHz 16-element phased-array chip with a 16:1 passive Wilkinson combiner, an I/Q receiver and a 38-42 GHz local-oscillator (LO) input. The LO signal is first doubled to 76–84 GHz and split into two paths: The BIST and LO paths. When the BIST mode is selected, the cascode active switch connects the BIST signal to a differential transmission-line on the left (Ch. 1-8), right (Ch. 9-16) or both sides of the array. This BIST signal is then fed to the phased-array channels using miniature differential couplers located at the input of each channel. The signal passes by the channels (each with amplitude and phase control), the 16:1 combiner, and is translated to DC I and Q voltages using a homodyne mixing technique. This allows for measuring the phase and amplitude response of individual channels if one channel is turned on at a time. It also allows for measuring an on-chip array factor if several channels are turned on and the phase between them is varied.

Fig. 5.2 presents the phased-array channel based on an alternating amplifier/phase-shifter topology (see [10] for a single-ended design). A passive balun is used for single-ended RF input port and the differential signal is fed into a SiGe cascode LNA+VGA. Switched-LC phase shifters are used for the 11°, 22°, 45° and 90° phase-shifter cells, and a SiGe Gilbert-cell is used for the 180° phase shift.

The 16 channel outputs are then fed to a 16:1 differential Wilkinson combiner with a net gain of 5 dB (12 dB summing gain, 7 dB ohmic loss), followed by an I/Q down-converter based on Gilbert-cell mixers with an input P_{1dB} of -5 dBm, and DC-coupled operational amplifiers. An RF monitor section is also implemented to measure the chip performance without the need of a local oscillator signal. This is done using a 300 Ω -10 dB resistive coupler attached to the main RF line. The chip is controlled using an SPI interface and contains a PTAT biasing circuit. The overall chip size is 5.5 × 5.8 mm^2 with a channel spacing of 700 μm, and consumes 500-600 mA from a 2V supply (1–1.2 W).

5.2.2 Amplifiers

The chip is built using the IBM 8HP SiGe BiCMOS process with a f_T of 200 GHz. It has 7 metal layers with a 4 μm thick top layer (AM) (Fig. 5.3). The 100 Ω differential coplanar-waveguide (CPW) transmission lines (gap-signal-gap-signal-gap = 9-6-10-6-9 μm) are built using the AM and MQ layers with a 9.2 μm thick interlayer dielectric (ε_{eff} = 3.9), and

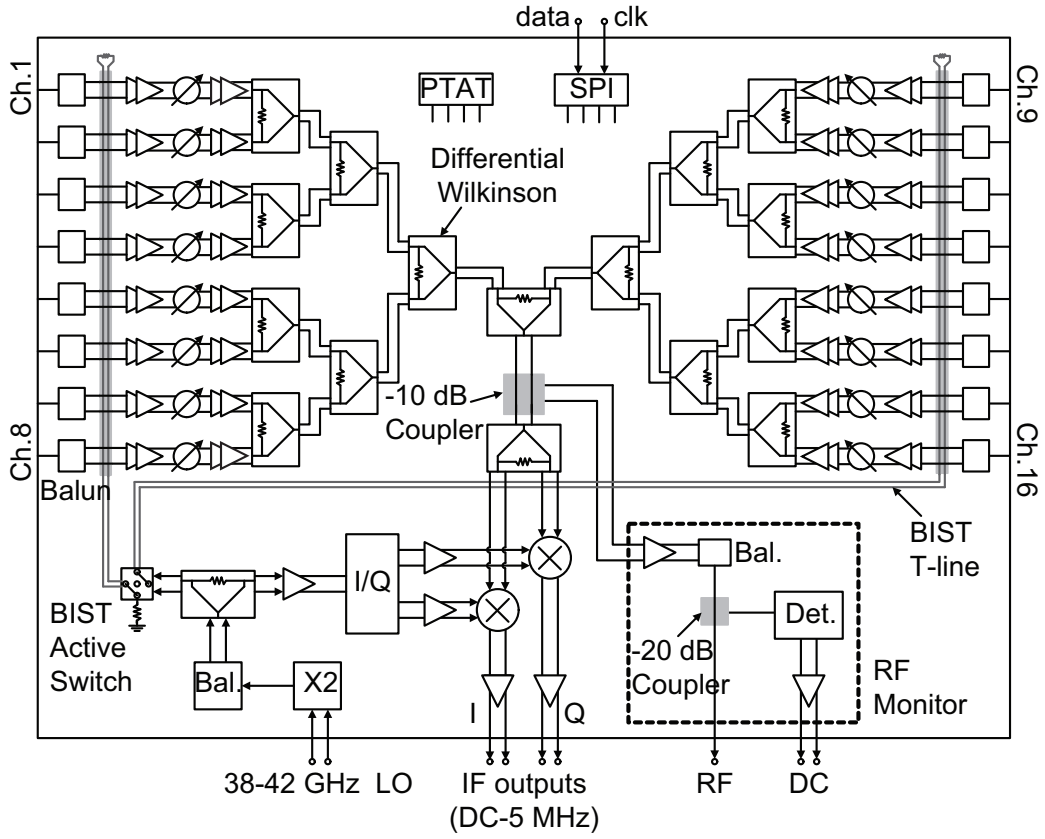


Figure 5.1: Block diagram of the 76-84 GHz 16-element phased array receiver with a chip-level built-in-self-test (BIST) system.

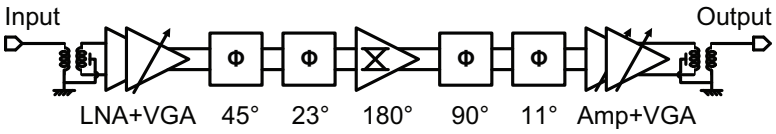


Figure 5.2: Block diagram of single channel

have a simulated loss of 1.05 dB/mm at 80 GHz.

Fig. 5.4 shows a two-stage cascode amplifier with a center frequency of 80 GHz. The first stage is biased at 0.4 mA/μm to result in the lowest noise figure and is less than the optimal bias current for highest gain as given by the IBM design manual [32]. The VGA is implemented by controlling the bias current of the second stage. The inductors are designed using microstrip lines between AM and M1, with a width of 4 μm and Q of 12 at 80 GHz. Capacitors are built using custom Metal-Oxide-Metal (MOM) capacitors between M3 and M4 with a simulated Q of 50 at 80 GHz. Resistors are placed in shunt with the load inductors in order to widen the 3 dB bandwidth to 19.6 GHz at the expense of 0.6 dB in additional noise. A simulated gain and noise figure is 10–11.1 dB and 8.9–9.2 dB, respectivley, at 75–86 GHz for a total bias current of 9 mA. The amplifier results in a wide impedance matching (S_{11}, S_{22} $<$ -10 dB at 66–100 GHz, 73–91 GHz, respectively) and a P_{1dB} of -19.9 dBm.

At millimeter-wave frequency, it is essential to design and model all the metal stacks using electromagnetic (EM) simulation tools. In this design, the entire circuits (the inductors, capacitors and interconnections) are EM-modeled and optimized using Sonnet [26] (Fig. 5.4). The Sonnet simulation takes 5 hours to analyze the cascode amplifier from 0.1 to 200 GHz on a modern desktop station. The global modeling and optimization technique, while time intensive, results in excellent comparison between simulations and measurements.

5.2.3 Phase Shifter

The design of the 11°, 22.5°, 45° and 90° phase shifter is based on switched-delay network and is a differential version of the earlier designs [10,30,64] (Fig. 5.5(a)). In the bypass state (T1 is ON and T2 is OFF), Lp resonates with the off-state parasitic capacitance of T2, and Ls and Cp are in parallel with the on-state resistance (R_{on1}) of T1. As long as R_{on1} is small enough, the Ls and Cp has minimal impact on the insertion phase. In the phase-delay state (T1 is

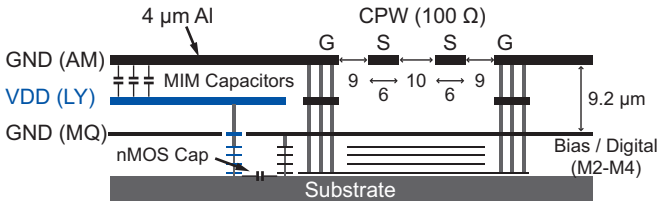


Figure 5.3: IBM 8HP metal stack-up with a representative 100 Ω differential CPW line.

OFF and T2 is ON), the input is connected to the output with the low-pass π network Cp-Ls-Cp. The Ls and Cp values can be chosen to provide the desired phase difference between the bypass and phase-delay states.

Also, the transistors (T1, T2) can be chosen to result in relatively low insertion loss when the transistors are ON, but the 0.13 μm CMOS technology results in a large substrate capacitance which contributes to high insertion loss at millimeter-wave frequency even when the transistors are off. T1 and T2 are therefore chosen to result in similar insertion loss in the bypass and phase-delay states (see Table 5.1). In the previous single-ended design [10], the 180° phase shifter was built by cascading two 90° switched-delay phase shifters, and its insertion loss was too high (8–9 dB). However, in the differential design, the 180° phase shifter can be easily implemented by controlling the quad switches of a Gilbert cell such that gain is achieved rather than loss (Fig. 5.5(b)).

Fig. 5.5(c) presents the simulated gain and phase response of the individual phase shifter cells. The 90° bit results in an insertion loss of 3–4.3 dB and a S_{11} (or S_{22}) $<$ -12.7 dB from 70–83 GHz for the bypass and phase-delay states. The 180° phase shifter results in 2.9 dB gain at 80 GHz, with S_{11} and S_{22} $<$ -15 dB at 71-90 GHz and 76-83 GHz, respectively for both states. By placing the active 180° phase shifter in the center of other phase shifter cells as shown in Fig. 5.2, the effect of the impedance mismatch between two states of the passive cells is minimized due to the high isolation of the active phase shifter (S_{12} $<$ -35 dB). All the inductors and MOM capacitors are designed and optimized using Sonnet, and global EM simulation is performed (see Fig. 5.5 for the Sonnet EM model).

This phase shifter topology results in gain variation over the 16 states due to the loss and impedance variation between the two states of each cell, and the cascade of non-ideal 100 Ω differential blocks (see Fig. 5.6). Simulations indicate a loss of 6.5-9.4 dB over the 16 phase states at 80 GHz. The variable gain amplifiers are therefore essential to compensate for this

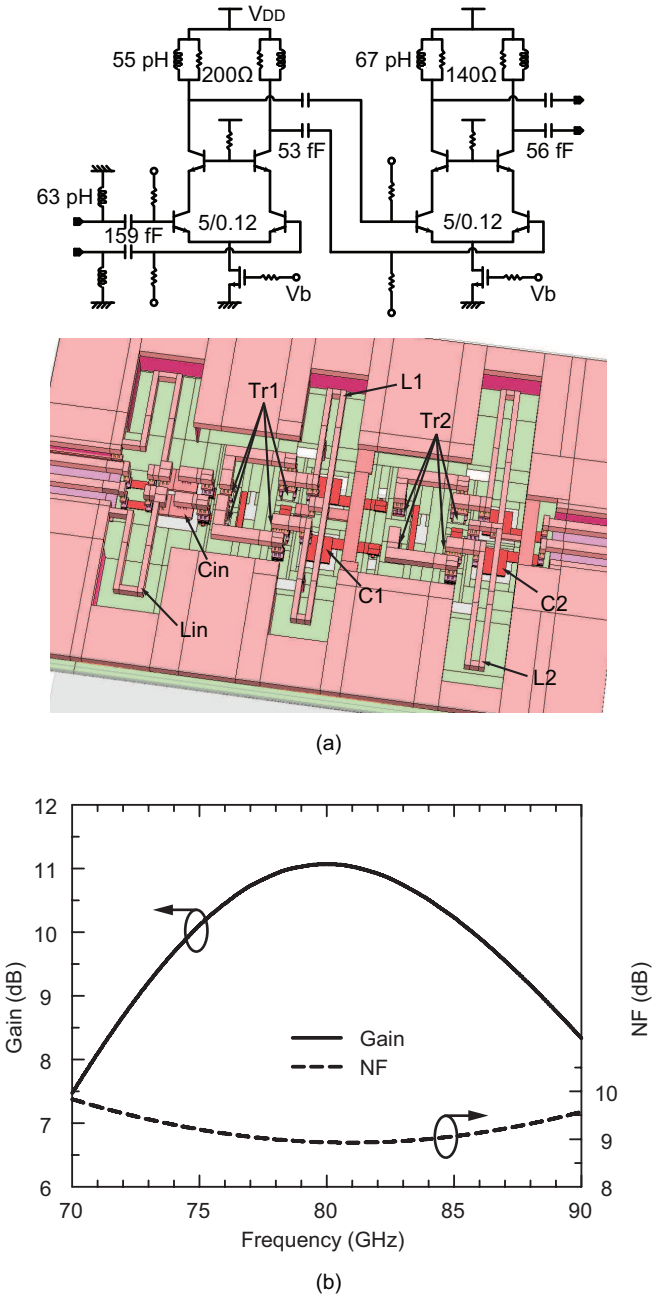


Figure 5.4: (a) Schematic and layout of the two-stage W-band cascode amplifier and (b) its simulated gain and noise figure.

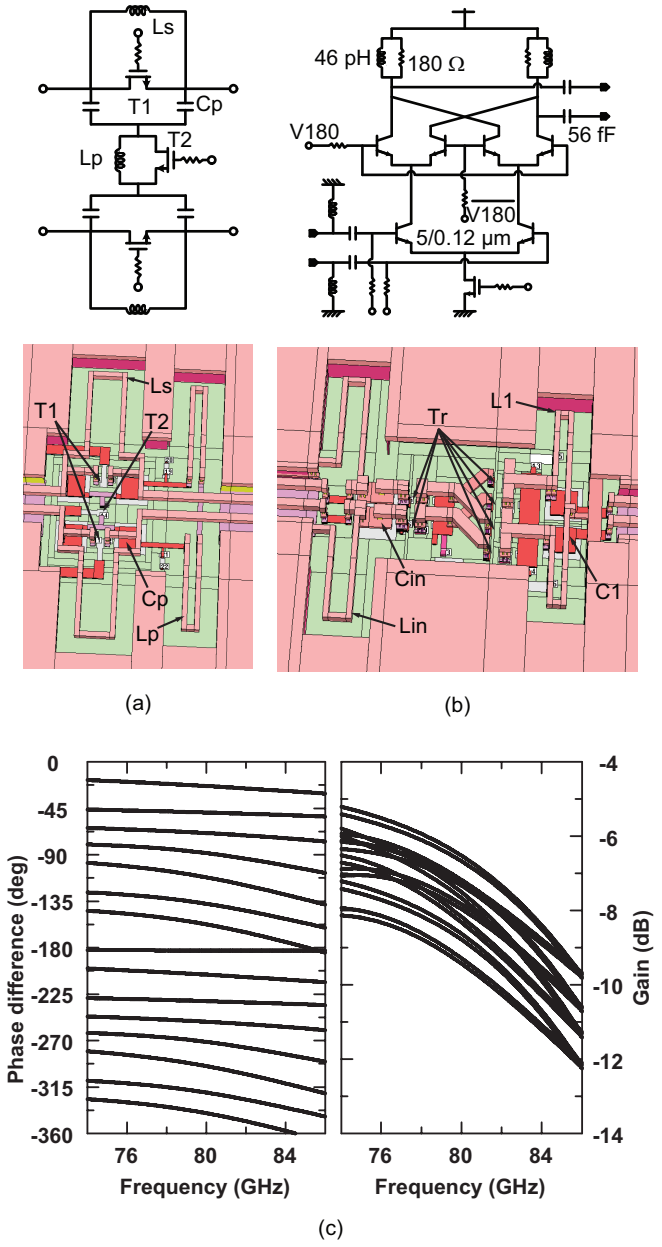


Figure 5.5: Schematic and layout of (a) 180^o phase shifter, (b) 90^o, 45^o, 23^o and 11^o phase shifters and (c) simulated phase difference and gain of each phase shifter.

Table 5.1: Phase shifter component values

	90°	45°	22°	11°
T1 (μm)	14	10	6	2
T2 (μm)	10	6	6	6
Ls (pH)	54	44	52	52
Cp (fF)	43	24	17	17
Lp (pH)	55	85	∞	∞

effect and to result in a low rms gain error. The simulated phase error is $\pm$4.4° at 80 GHz, and is from -12.4° to 20° at 76–84 GHz.

5.2.4 Balun and Differential Wilkinson Combiner/Divider

Fig. 5.7 shows the designed passive balun to convert single-ended signal to differential signal. A passive balun is preferred since it does not consume any DC power and can act as an ESD protector. Also, it is not connected to V_{DD} and therefore, does not couple to the supply. The passive balun is a two-layer design with a primary turn implemented using AM and the secondary turn implemented using LY. The distance to the ground plane is 16 μm on each side and the metal width is 8 μm. A 32 fF series capacitor at the input and a 38 fF shunt capacitors at the output are used for matching and provide a wideband matching (S_{11} $<$ -10 dB for 70–100 GHz). The balun has a simulated loss of 1.2 dB at 80 GHz.

Fig. 5.8 shows the 100 Ω differential Wilkinson combiner/divider, designed using two λ/4 sections of 70.7 Ω CPW lines (Q=13 at 80 GHz) and results in an insertion loss of 0.9 dB and S_{11}/S_{22}/S_{33} $<$ -20 dB at 72–88 GHz. The isolation between the two ports, S_{23}, is $>$ 25 dB at 72–88 GHz. The Wilkinson combiner is wideband and has no effect on the channel S-parameters except for an additional 0.9 dB loss per stage. It also allows for high-power combining with no dc power consumption. Again, the 16:1 Wilkinson combiner is electromagnetically modeled in Sonnet and its S-parameter block is used in Cadence.

5.2.5 Doubler

The 38 GHz FMCW LO input signal is provided externally and is up-converted using an on-chip doubler. The usage of the LO at half the frequency allows for a lower LO distribution loss between the Tx and Rx chip on the Teflon board and for easy flip-chip (or bond-wire) transitions. Also, any LO coupling between the LO ports and the RF ports results in a high IF

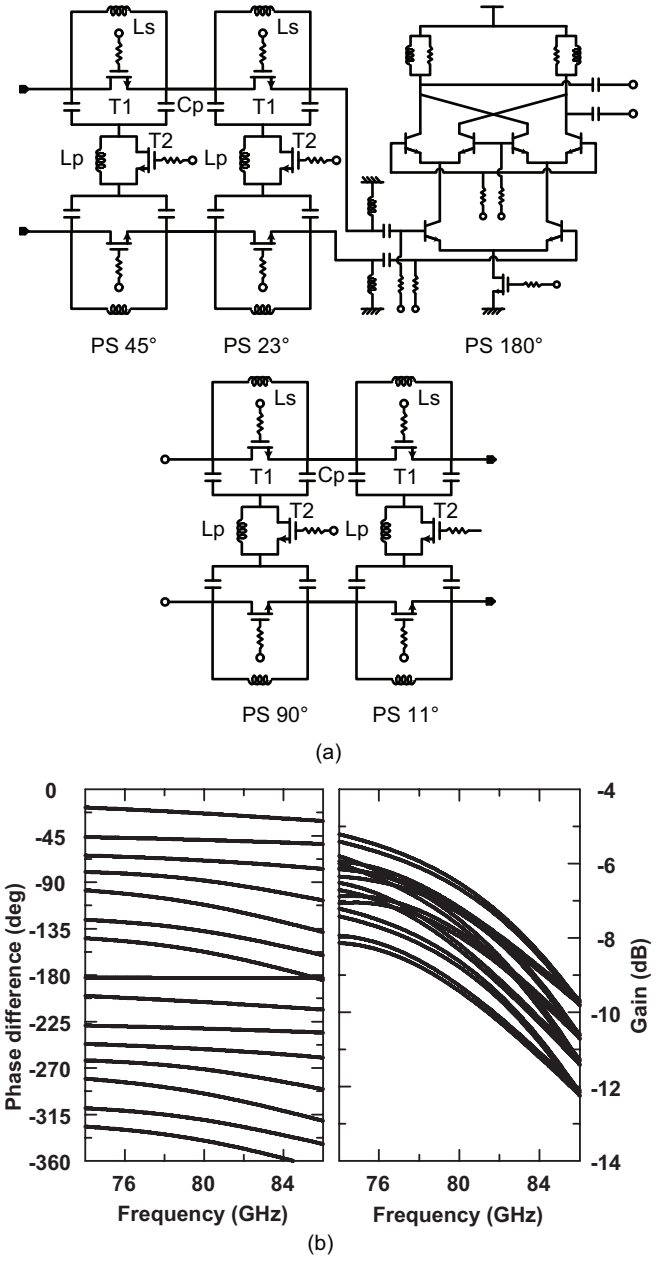


Figure 5.6: (a)Schematic and (b)Simulated phase difference and gain of the total phase shifters.

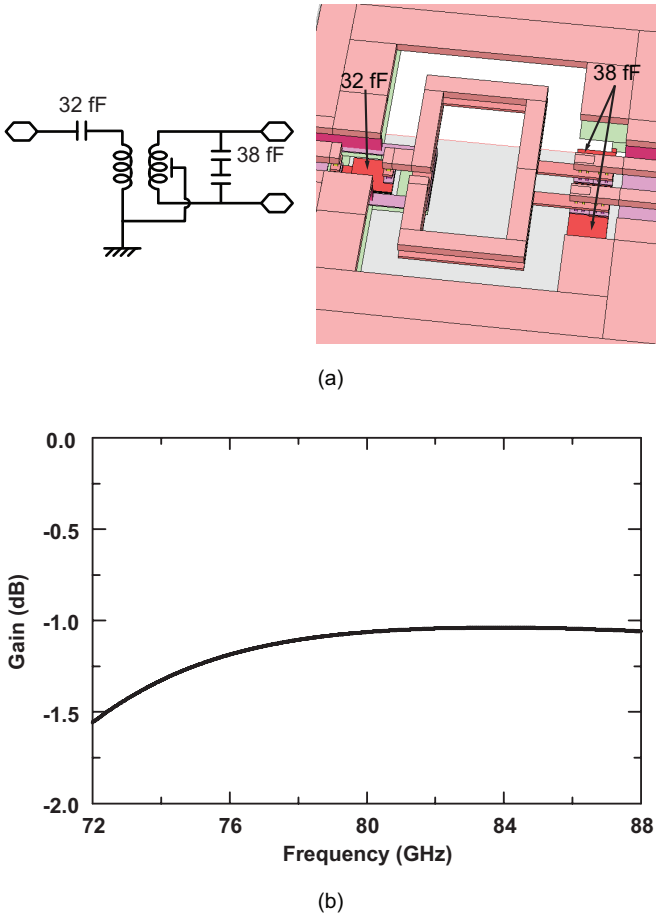


Figure 5.7: (a)Schematic, layout and (b)simulated gain of passive balun.

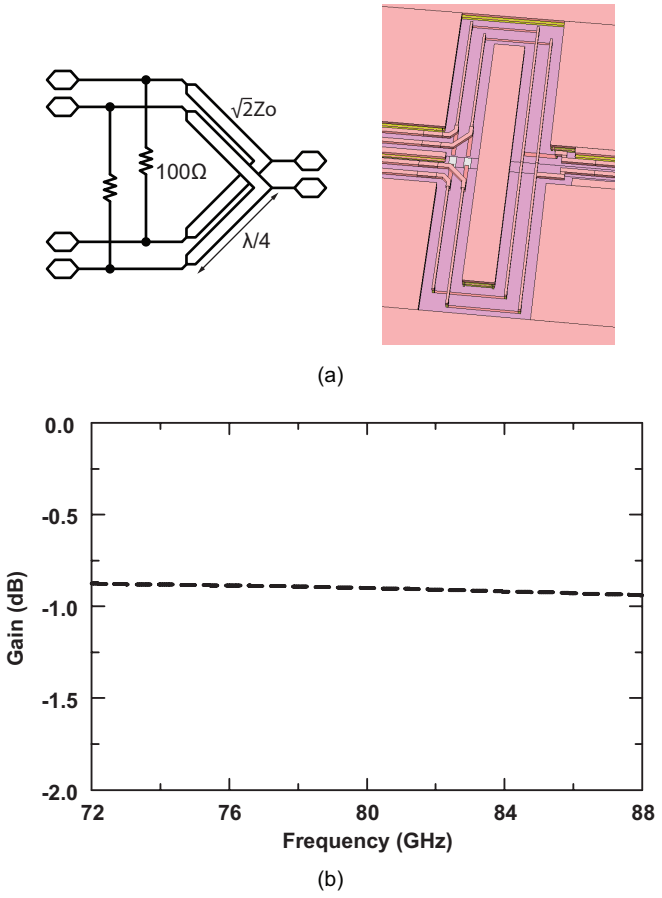


Figure 5.8: (a)Schematic, layout and (b)simulated gain of differential Wilkinson combiner/divider.

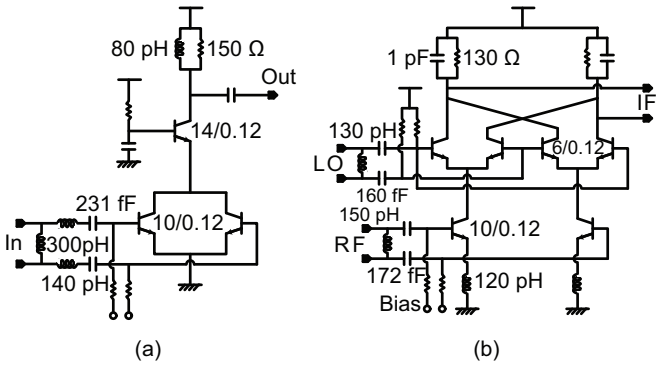


Figure 5.9: Schematic of (a) doubler and (b)double-balanced mixer.

which is filtered by the low-frequency IF amplifiers. The doubler is an active balanced design as shown in Fig. 5.9(a) [66, 67]. The LO input are differential for reduced coupling, and are directly fed into a balanced transistor pair biased near the class-B region in order to generate the second harmonic components efficiently. A cascode stage is added to increase the conversion gain and isolation between input and output. At the fundamental frequency and odd harmonics, the RF signals at the differential drain nodes are out-of-phase, and since the drain nodes are tied together, this creates a short circuit and rejects the fundamental and odd harmonics. At the second and even harmonics frequencies, the input signals are combined in-phase at the drain common nodes. The simulated conversion gain is 0 dB for an input power of -10 dBm with S_{11} and S_{22} $<$ -10 dB at 36–44 GHz and 72–87 GHz, respectively.

5.2.6 LO Path Design

As shown in Fig. 5.1, the doubled LO signal is first converted to a differential signal using a passive balun and then split into two paths using a differential Wilkinson divider: The BIST path and the LO path (Fig. 5.10(a)). In the LO path, a set of I and Q signals are generated using a polyphase filter (Fig. 5.10(b)). A single-stage RC-CR polyphase filter is selected since driving the I/Q mixers requires narrowband quadrature LO signals. Also, this poly-phase filter provides a robust quadrature signal to the I/Q mixer which is more sensitive to the I/Q phase mismatch rather than the amplitude mismatch. In order to compensate the balun, Wilkinson divider and I/Q network loss, Amp1 and Amp2 are added in the LO path which also act as limiting amplifiers for the I/Q mixers (Fig. 5.10(c),(d)).

5.2.7 I/Q Mixer

The active I/Q mixers are based on a standard double-balanced mixer topology (Gilbert cell) (Fig. 5.9(b)). The double-balanced mixer provides high isolation between the LO and IF ports by nature, and therefore relaxes the filtering requirement at the IF output. The RF and LO ports are matched to 100 Ω so that maximum power can be transferred. Standard inductive degeneration is used for high linearity. At the IF output, 130 Ω resistive loads are added for wideband IF operation and 1 pF capacitor is used as a filter to eliminate any RF and LO leakage. The simulated voltage conversion gain is 8 dB for an LO input power of 0 dBm, with a simulated return loss at the RF and LO port of $<$ -10 dB at 70–86 GHz. The simulated NF of the I/Q mixer and the IF amplifier is 21.2 dB and 18.5 dB for a gain setting of 8 dB and 27 dB, respectively.

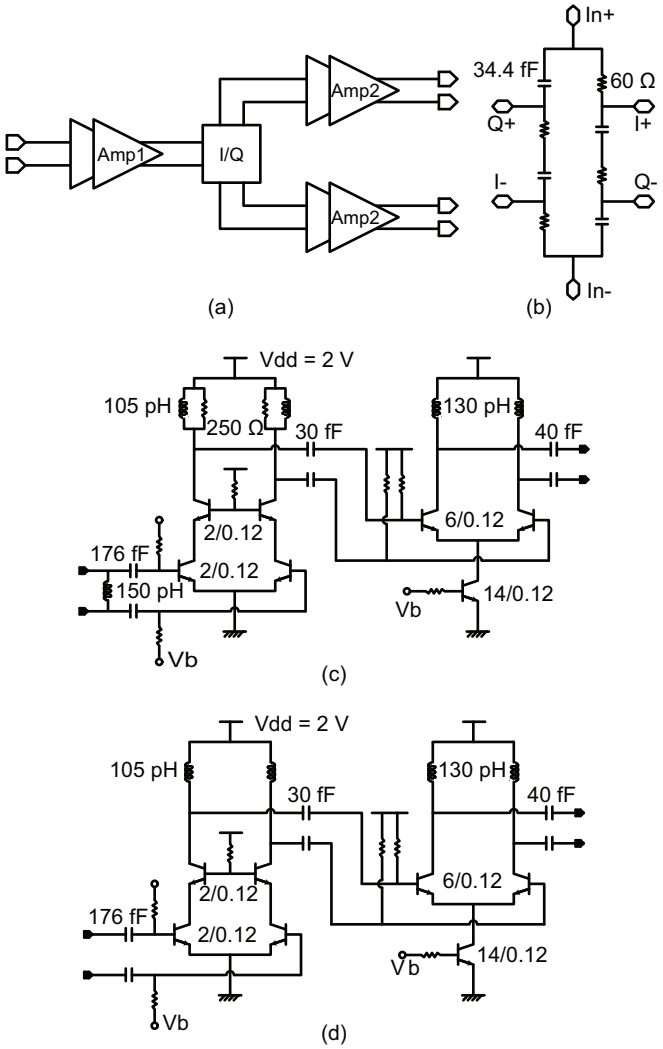


Figure 5.10: (a) Block diagram of LO path, schematic of (b) IQ generator, (c) Amp1 and (d) Amp2.

5.2.8 IF amplifier

Fig. 5.11(a) shows the block diagram of the IF amplifier. The IF amplifier is a RC-compensated 2-stage op-amp (Fig. 5.11(b)), followed by the invert-type buffer (Fig. 5.11(c)) with the 2-bit digital gain control. BJT transistors are used at the input of the op-amp due to its better 1/f noise performance. The inverter-type buffer with resistive feedback is for driving the low impedance output loads. The simulated voltage gain of the IF amplifier is 26/19/12/3 dB when the output is open-circuit, and the gain drops by 9 dB if the output is terminated with a 100 Ω differential load. (The closed-loop output impedance of the IF amplifier is 330 Ω). The total power consumption of the op-amp and buffer is 7.7 mA from a 2 V supply. The closed-loop 3-bandwidth of the amplifier is 7 MHz at highest gain setting.

5.2.9 Built-In-Self-Test System Design

The differential BIST transmission-line and coupler are shown in Fig. 5.12. The BIST line is built using the M3 layer (Z_o = 85 Ω, loss = 4 dB/mm at 80 GHz) and is shielded from the RF line and silicon substrate using the MQ and M1 ground layers. A lumped-element coupler is synthesized at each channel input by locally opening the MQ ground layer, moving up the BIST line to M4, dropping the RF line to MQ, and widening both to 11 $\times$ 12 μm^2, thereby creating a capacitive coupler. The BIST and RF line are coupled at two different positions to ensure an equiphase response at port 2. Full-wave electromagnetic analysis using Sonnet show S_{23}=-26 dB coupling when port 1 is terminated differentially with 100 Ω (i.e. attached to antennas) and -20 dB when port 1 is left open-circuited (i.e. chip test with no external connections). The 6 dB increase is due to the BIST voltage wave coupling to port 1, reflecting at the open circuit and then adding in phase with the BIST voltage wave coupling to port 2. The coupler effect on the RF line is minimal (S_{21} $<$ -0.2 dB, S_{11} $<$ -20 dB at 80 GHz). PUT A FIGURE of the BIST coupler

5.3 Measurements

All measurements are done on-wafer using an Agilent E8361A Vector Network Analyzer with extenders to 110 GHz. A standard Short-Open-Load-Thru (SOLT) calibration to the W-band GSG probe tips is first done using the Cascade 138-357 calibration substrate [27], and the measurements include the GSG pad transition loss. Several chips were measured and resulted in similar measurements.

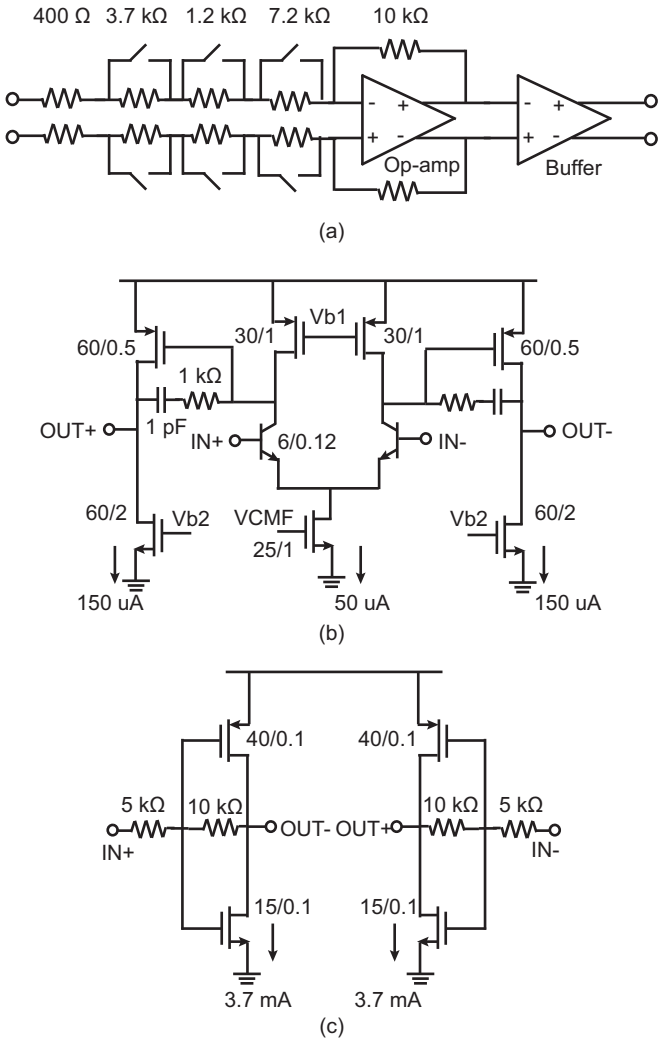


Figure 5.11: (a) Block diagram of the IF amplifier, (b) the schematic of 2-stage op-amp, and (c) the schematic of the buffer.

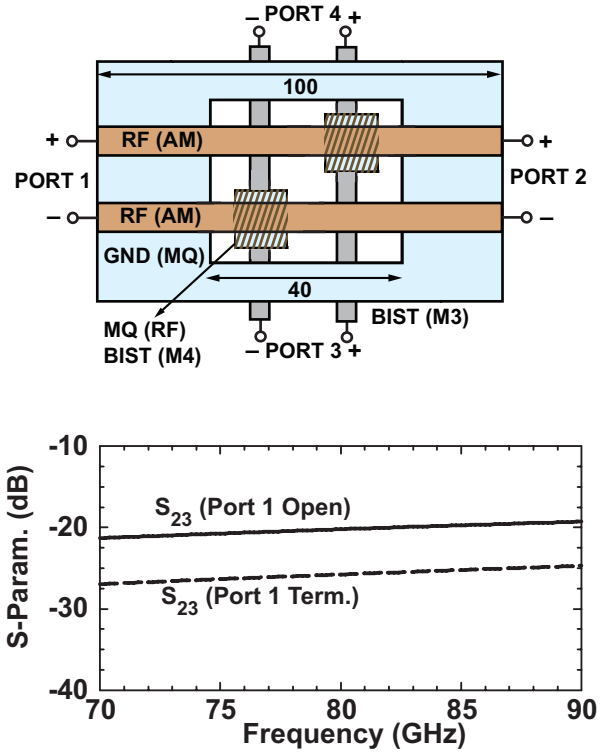


Figure 5.12: BIST coupler and simulated S-parameters of the BIST network.

5.3.1 Single-Element

Fig. 5.13 shows the measured S_{11} and S_{22} for 16 phase states using a single-channel test chip. The single channel consumes the total current of 30 mA from 2 V supply voltage (60 mW). All the digital circuits use a separate supply voltage of 1.5 V. A wideband input and output matching is achieved with S_{11} and S_{22} $<$ -9 dB at 72–88 GHz and 73–86 GHz, respectively. Fig. 5.14 presents the measured gain and phase response of S_{21} and its rms errors for 16 phase states. The measured average power gain (S_{21}) is $>$ 10 dB for 76.4–90 GHz, and its rms gain error is $<$ 1 dB for 74–84.2 GHz. The rms phase error is $< 11^{\circ}$ at 73.6–83.6 GHz. In order to optimize both rms gain and phase errors, the variable gain amplifier (VGA) function and the 11° phase shifter are used. The measured reverse isolation (S_{12}) is $<$-45 dB (not shown).

Comparison with simulations indicates that measured center frequency has shifted up from 78 GHz to 83 GHz. The discrepancy could be due to the inaccurate transistor modeling at W-band frequency together with process variations and errors in the parasitic estimation. In order to match the measured center frequency with simulations, first, the parasitics are decreased, and then the bias current is increased from 25 mA to 30 mA so as to get enough gain at W-band

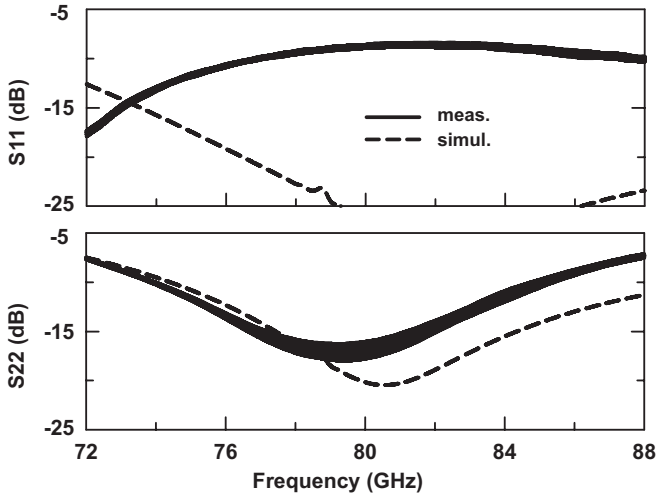


Figure 5.13: Measured and simulated S_{11} and S_{22} for 16 phase states.

to match the measurements (Fig. 5.15).

Fig. 5.16 presents the measured VGA operation with 4-bit digital control. The VGA can be controlled over a 7.3 dB range with $\leq \pm 5.3^{\circ}$ phase change. The noise figure (NF) is measured for several gain states (Fig. 5.17). For the maximum gain state, the NF is 11.2–13 dB at 77–87 GHz and it increases by 1.5 dB at for minimum gain state. Fig. 5.18 presents the measured input P_{1dB} of -20 dBm and -25.8 dBm at 77 GHz and 83 GHz, respectively. The P_{1dB} values are measured at the maximum gain state and almost constant for different gain states.

Fig. 5.19 presents the measured gain vs. temperature. The gain variation is less than 1.9 dB up to 100°. This is achieved by using Proportional-To-Absolute-Temperature (PTAT) bias circuits and results in an increased current as the temperature increases. As demonstrated in [6], the rms gain and phase error remains unchanged at different temperatures.

5.3.2 16-Element Phased Array

In order to have the high angular resolution scanning capabilities, a 16-element phased array is chosen. Simple array factor calculations indicate that a 16-element linear array results in a 6.4° 3-dB beamwidth [2]. Fig. 5.20 presents the chip microphotographs. The overall chip size is 5.0×5.8 mm^2 with a channel spacing of 700 μm, and consumes 500–600 mA from a 2 V supply voltage (1–1.2 Watt). The channel to channel distance (therefore, the chip size) is set by the Printed-Circuit-Board (PCB) design limitation rather than the circuit layout. A total of 8 DC pads are assigned as V_{DD} in order to satisfy the current density requirement. Also, GND pads

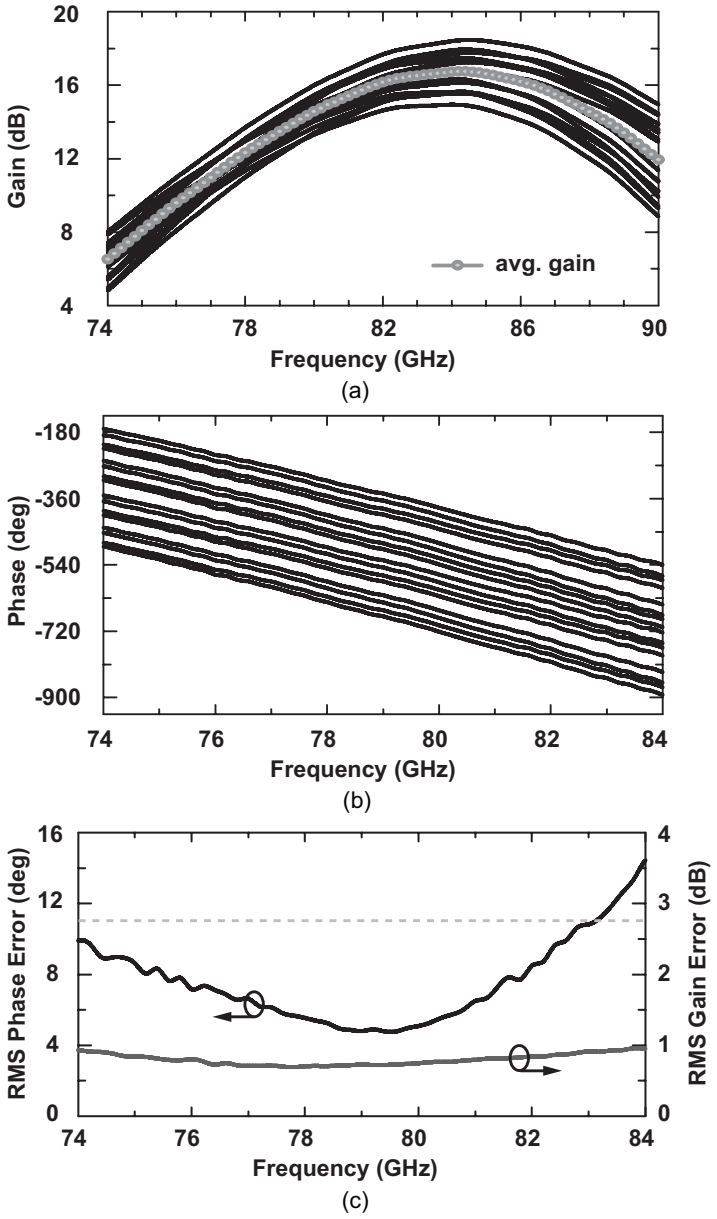
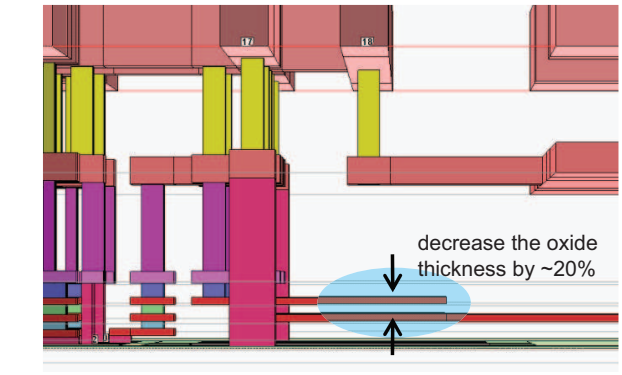
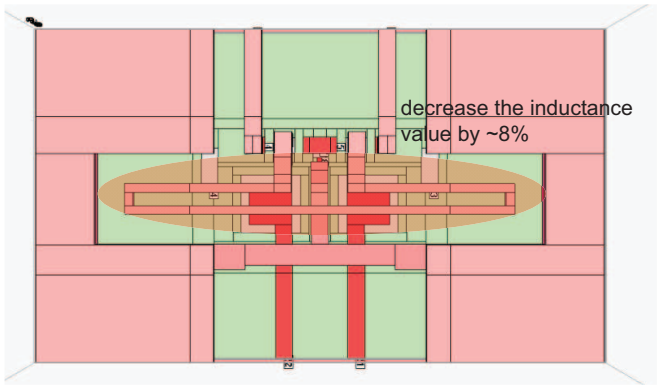


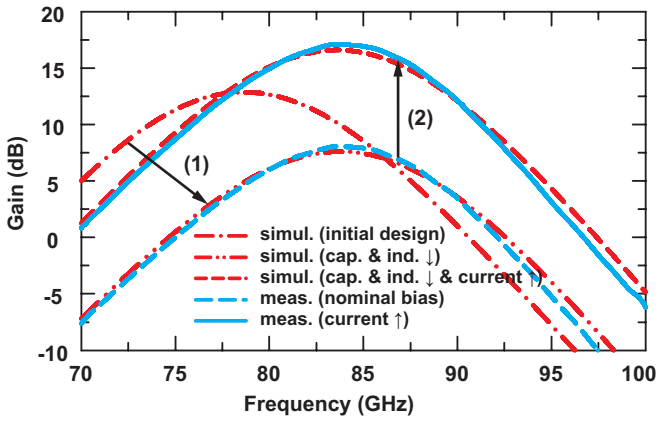
Figure 5.14: Measured (a) gain, (b) phase response and (c) rms gain and phase error for 16 phase states.



(a)



(b)



(c)

Figure 5.15: Average gain fitting by (a) decreasing capacitance by 20% due the oxide thickness variation ($< \pm 23\%$) and (b) inductance by 8%, and increasing current (npn by $+0.6\sigma$.)

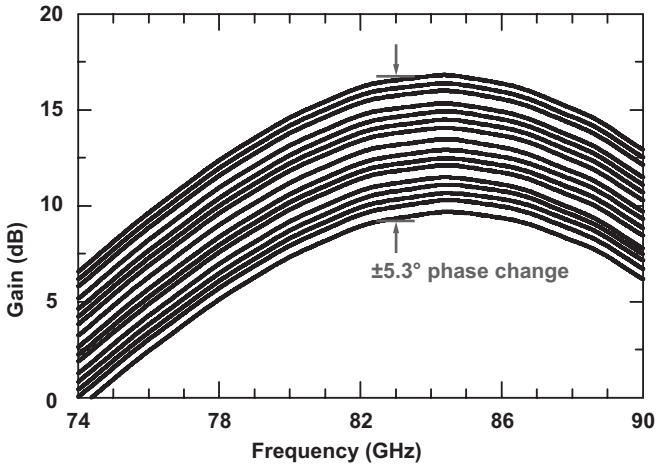


Figure 5.16: Measured VGA operation at 0^o state.

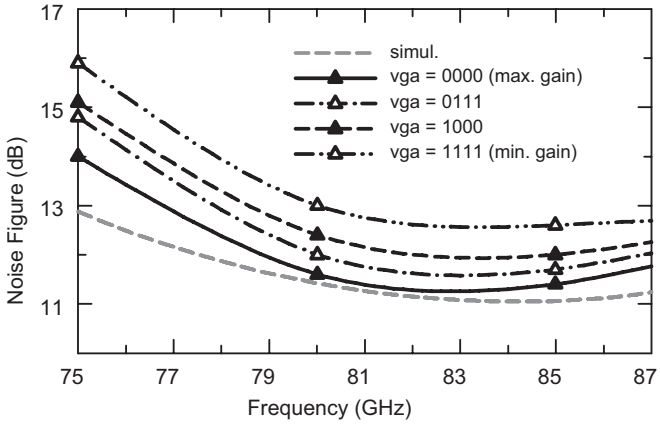


Figure 5.17: Measured and simulated noise figure for different gain setting.

are used all over the chip to minimize the GND inductance when connected to the PCB either with bond-wires or flip-chip technologies.

In phased array systems, the coupling between channels is a major concern [16, 65]. The fully differential design and layout, with a relatively high substrate resistance of the SiGe BiCMOS process (ρ = 11–16 Ω-cm) and the large distance between adjacent channels (700 μm), help reduce the channel-to-channel coupling. In addition, ground barriers (grounded via stack from substrate to MQ metal) are placed between the channels to reduce the coupling further. In this system, the coupling between the channels was determined by measuring the down-converted I/Q voltage with an input at channel 3 and toggling the phase of channel 4, and then fitting the coupling vector, c [65]. A coupling of $|c^2| \sim$ -50 dB was measured at 77 and 83 GHz (Fig. 5.21). Measurements done on different channel combinations result in a coupling of -48 dB to -54 dB, which is insignificant in a phased array.

5.4 Conclusion

A 76-84 GHz 16-element phased array receiver was demonstrated in a 0.13 μm BiCMOS process. All the circuits are designed differentially to result in less sensitivity to ground inductance when packaged. This also results in a very high channel-to-channel isolation due to the excellent rejection of the common-mode substrate coupling. The rms gain and phase errors were mostly due to inaccuracies in the transistor switch model, but can be corrected using a VGA and an 11° trim bit. The overall chip size is 5.0 $\times$ 5.8 mm^2 with the power consumption of 1–1.2 Watt (500–600 mA from a 2 V supply voltage).

5.5 Acknowledgements

This work was supported by the Toyota Research Institute of North America (TRINA). The authors thank Dr. Jae Lee and Koji Shiozaki, both at Toyota, for technical discussions.

Chapter 5 is mostly a reprint of the material as it will be submitted for publishing to IEEE Transactions on Microwave Theory and Techniques, 2012 (or IEEE Journal of Solid-State Circuits, 2012). Sang Young Kim; Ozgur Inac; Choul-Young Kim; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

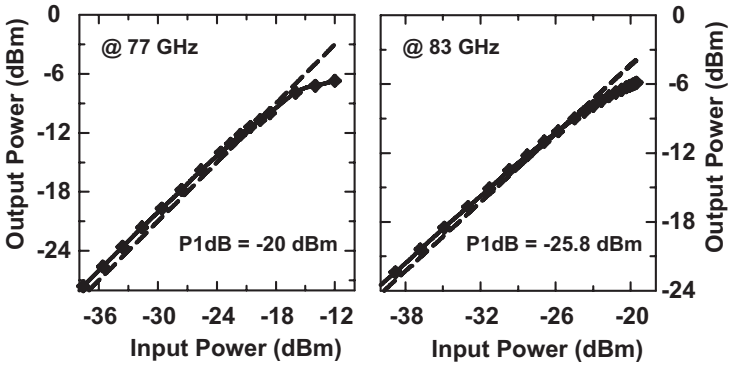


Figure 5.18: Measured P_{1dB} at 77 GHz and 83 GHz for VGA = 0000 (max.).

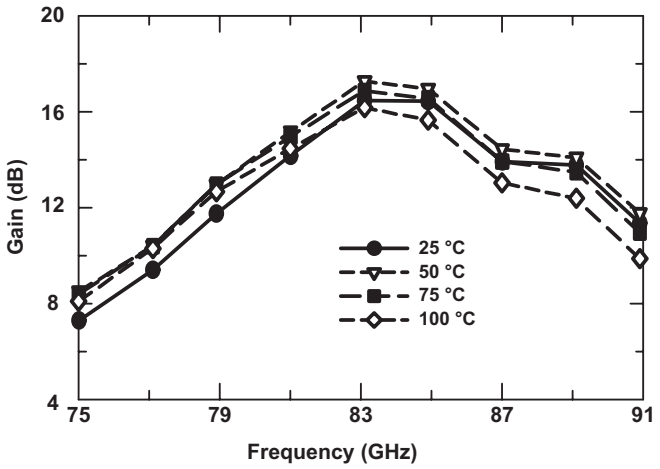
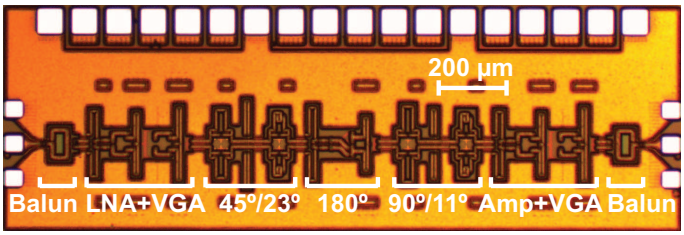
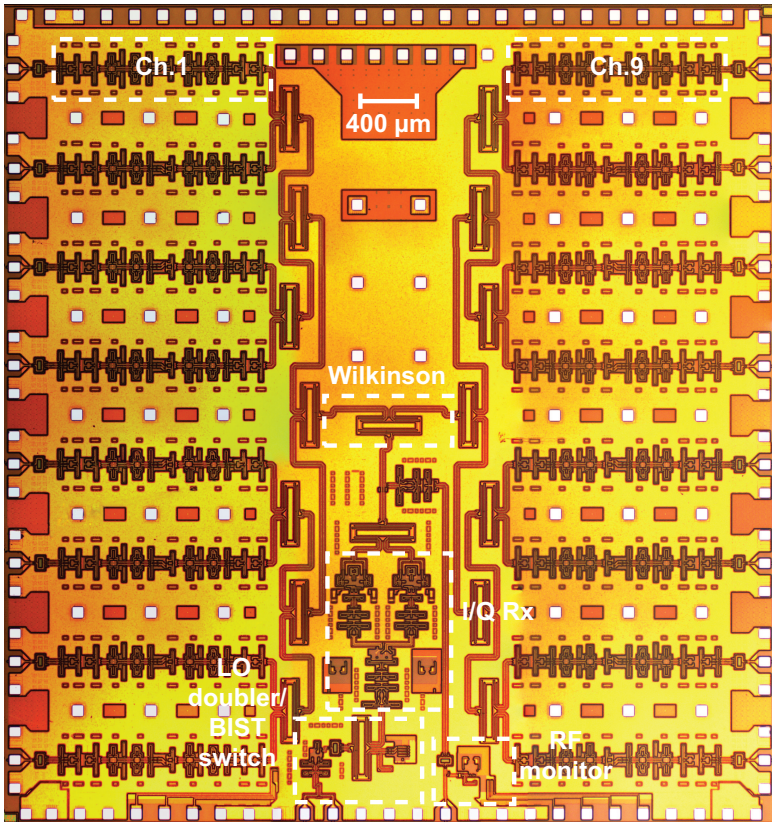


Figure 5.19: Measured gain of a single channel at different temperatures.



(a)



(b)

Figure 5.20: Photograph of (a) single channel (2.0 x 0.65 mm^2) and (b) 16-element phased arrays (5.5 x 5.8 mm^2).

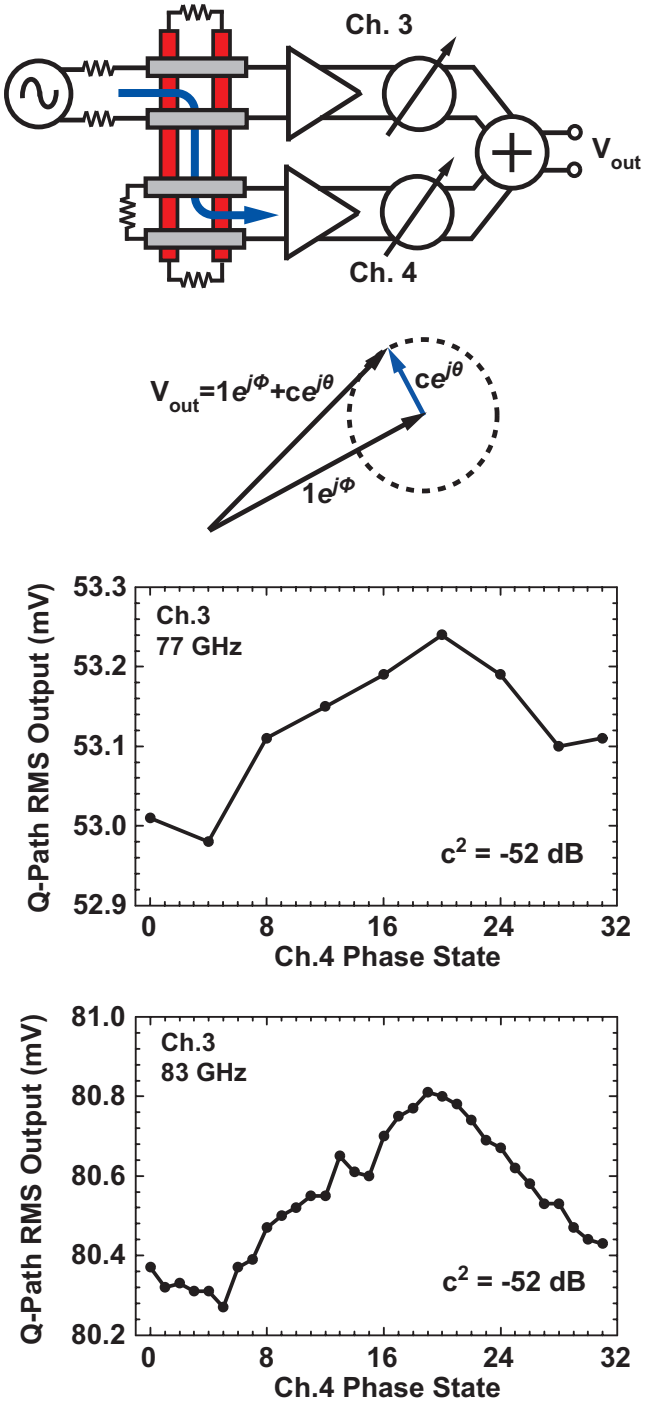


Figure 5.21: Leakage between two channels due to the BIST transmission-line and measured coupling between channel 3 and channel 4.

Table 5.2: Performance Comparison

	IBM	Intel	This Work
Frequency	55-65 GHz	57-66 GHz	76-84 GHz
Number of element	16	32	16
Process	0.13 μm BiCMOS	90nm CMOS	0.13 μm BiCMOS
Gain	70 dB*	13 dB*	30 dB @77GHz 34 dB @83GHz
Gain, Front-end	18 dB	N/A	11 dB @77GHz 16 dB @83GHz
Front-end NF	6.8-7.3 dB	11 dB	11-13 dB
P1dB, (per element)	-28 dBm	-32 dBm	-20dBm @77GHz -26dBm @83GHz
Size	6.1 x 6.2 mm^2	4.4 x 3.3 mm^2	5.0 x 5.8 mm^2
Power	1.8 W	0.5 W	1.2 W

*Includes IF stage

Chapter 6

Conclusion

This thesis demonstrates several silicon-based on-chip W-band phased array systems. An improved wideband I/Q network to minimize the capacitive loading problem is presented, and its implementation in a 60–80 GHz active phase shifter using 0.13 μm SiGe BiCMOS process is demonstrated. In addition, a 67–78 GHz 4-bit passive phase shifter using low-pass π-network and 0.13 μm CMOS switches is demonstrated. By adding amplifiers to the passive phase shifter with the architecture of alternating amplifiers and phase shifter cells, a low-power BiCMOS 4-element phased array receiver for 76–84 GHz applications are presented. Lastly, a 76-84 GHz 16-element phased array receiver, designed differentially in order to reduce the sensitivity to packaging effect such as ground inductance, is presented.

Chapter 2 presents an improved quadrature all-pass filter (QAF) and its implementation in 60–80 GHz active phase shifter using 0.13 μm SiGe BiCMOS technology. It is demonstrated that with the inclusion of an R_s/R = 0.5–1 in the high Q branches of C and L, the sensitivity to the loading capacitance, therefore the I/Q phase and amplitude errors are minimized. The another benefit of putting R_s into the QAF is that the it increases the QAF input impedance by (1 + R_s/R) and increases the load impedance on the previous stage, thus lowers its power consumption. This technique is especially suited for wideband millimeter-wave circuits where the loading capacitance (C_L) is comparable to the filter capacitance (C).

Chapter 3 demonstrates the a 67–78 GHz 4-bit passive phase shifter using 0.13 μm CMOS switches. The phase shifter is based on a low-pass π-network. The chip size is 0.45 $\times$ 0.3 mm^2 without pads and consumes virtually no power. The measured S_{11} and S_{22} is $<$ -10 dB at 67–81 GHz for all 16 phase states. The measured gain of 4-bit phase shifter is -19.2 $\pm$ 3.7 dB at 77 GHz with the rms gain error of $< 11.25^\circ$ at 67–78 GHz. And the measured rms phase error

is $<$ 2.5 dB at 67-78 GHz. The measured P_{1dB} is $>$ 8 dBm and the simulated IIP3 is $>$ 22 dBm.

Chapter 4 presents a low-power 76–84 GHz 4-element phased array receiver using 0.13 μm SiGe BiCMOS process. The power consumption is minimized by using a single-ended design and alternating the amplifiers and phase shifter cells to result in a low noise figure at a low power consumption. A variable gain amplifier and the 11° phase shifter are used to correct for the rms gain and phase errors at different operating frequencies. The overall chip size is 2.0 $\times$ 2.7 mm^2 with the current consumption of 18 mA/channel with 1.8 V supply voltage.

Chapter 5 presents a 76–84 GHz 16-element phased array receiver in a 0.13 μm SiGe BiCMOS process. All circuits are designed differentially to result in less sensitivity to packaging effect such as ground inductance and V_{DD} inductance, and high channel-to-channel isolation due to the excellent rejection of the common-mode substrate coupling. The overall chip size is 5.0 $\times$ 5.8 mm^2 with the power consumption of 500–600 mA from a 2 V supply voltage.

At the moment, a 76–84 GHz 16-element phased array receiver chip, designed fully differentially, has been completed and showed a excellent performance. Most of the published work presents on-chip performance using CPW probes, but this ignores the packaging effect of phased array system, such as ground and V_{DD} inductance effect, coupling between different RF ports due to the wire-bonds, and matching between the antennas and the chip. These effects can degrade the phased array chip performance and make it un-usable in the practical phased array system. Therefore, it is important to demonstrate the performance when the chip is mounted and packaged on-board. Fig. 6.1 shows the PCB board (RO3003, ε_{eff} = 3.0) designed by Bon-hyun Ku at UCSD. The 16-element phased array receiver chip will be mounted on the PCB board and the antenna will be connected to the board to measure the beam-pattern.

All the work, presented in this dissertation, is for an on-chip receiver. In order to improve the performance and reduce the price further, it is necessary to design an integrated on-chip transceiver system. Therefore, a W-band 16-channel phased array transceiver (2x4-channel: receiver, 8-channel: transmitter) with a chip-level BIST is being designed and will be taped-out by Bon-hyun Ku and Ozgur Inac in March 2012 (Fig. 6.2).

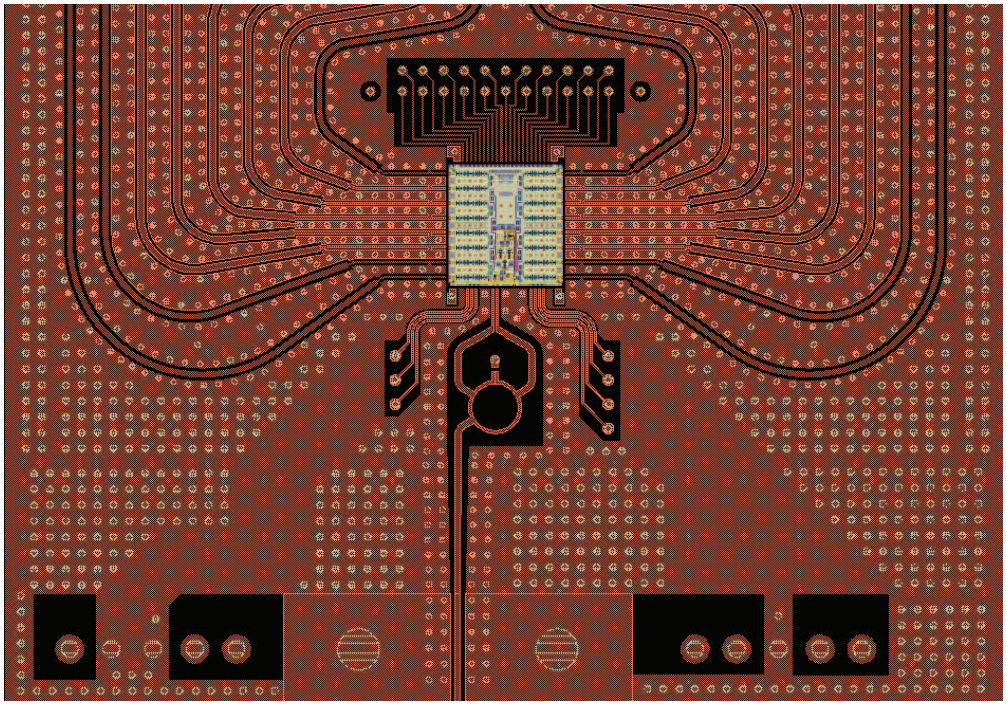


Figure 6.1: PCB board design for measuring the antenna pattern using the designed 76–84 GHz 16-element phased array receiver.

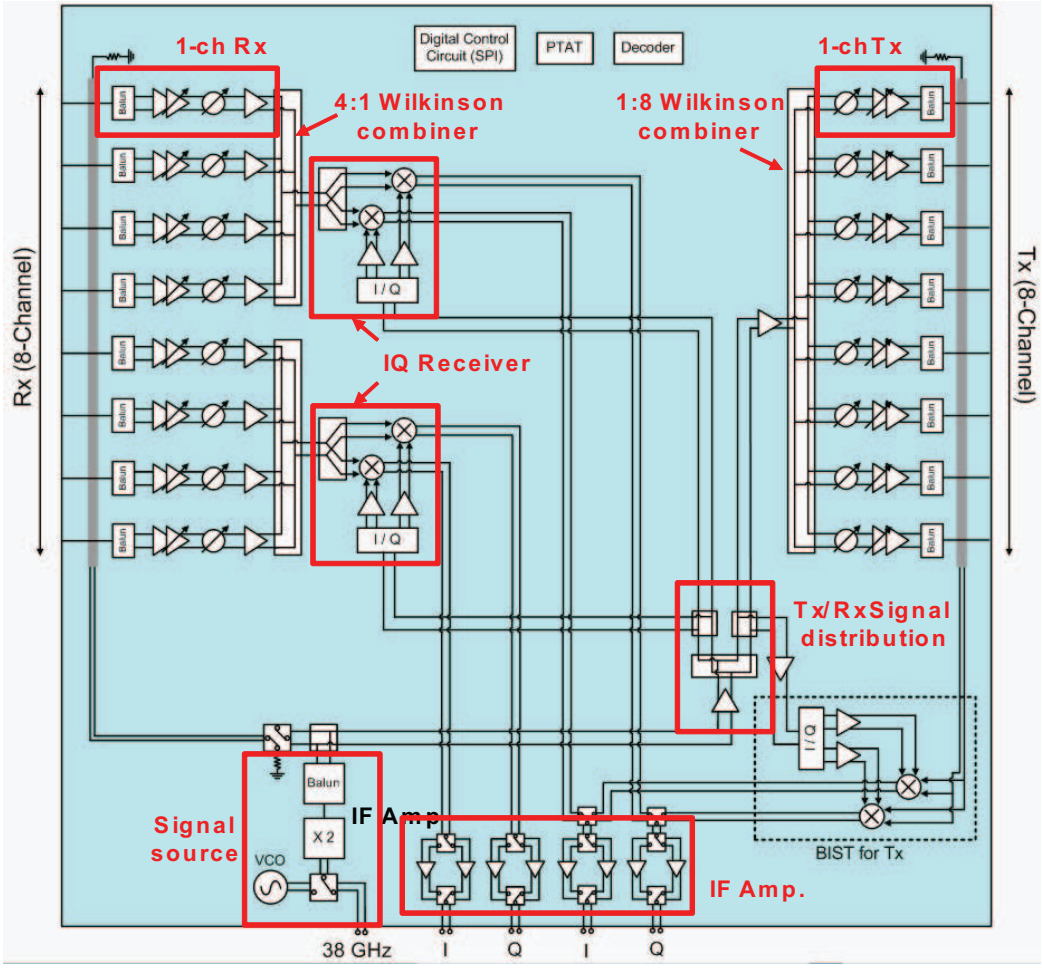


Figure 6.2: PCB board design for measuring the antenna pattern using the designed 76–84 GHz 16-element phased array receiver.

Appendix A

An 18-20 GHz Subharmonic Satellite Down-Converter in 0.18 μm SiGe Technology

A.1 Introduction

Satellite down-converters in the 8-44 GHz band are currently based on GaAs circuits which offer very low noise figure receivers and excellent performance. The GaAs receivers are built using discrete components on low-loss Teflon substrates, and while this is acceptable for 8-14 GHz operation, they require manual tuning in the 20-44 GHz range. Also, a typical 18-20 GHz GaAs down-converter may require as much as 20 different discrete components after the LNA. It is therefore beneficial to replace the entire back-end with a single silicon chip for lower cost and a much smaller package for the LNB (low-noise block) (Fig. A.1) [68]. The silicon chip should have high gain, relatively low-noise figure, and be capable of a high output-P_{1dB} since it will be connected to the long coaxial cable between the LNB and the satellite receiver. The chip should also be single-ended so as to be compatible with the GaAs LNA, the dielectric-resonator-oscillator (DRO) and the coaxial IF output. The single-ended design also ensures minimum circuit area and current consumption. The 18-20 GHz silicon chip can be designed using 90 nm CMOS or using 0.18-μm SiGe technology, both with an f_T of 120-150 GHz. We have chosen the SiGe solution due to its lower cost for small volumes, and due to the required high output P_{1dB} (0-3 dBm) for a 50 Ω output impedance.

A.2 Design

Fig. 1 presents the block diagram of the silicon down-converter. Two stages are used for the RF-stage with a gain of 28 dB at 19 GHz, and another two stages are used at the IF-stage with a gain of 21 dB at 1-3 GHz. The gain is divided nearly equally between the RF- and IF-stages so as to reduce the possibility of oscillations. A subharmonic mixing topology is chosen since it is easier to build a low noise DRO at 10.5 GHz than at 21 GHz. The subharmonic mixer (7 dB conversion loss) requires a differential local oscillator, and an integrated balun is used to convert the single-ended LO into a differential signal. The output IF stage is designed to drive a 50 Ω load with an output P_{1dB} of 0-1 dBm.

The input RF amplifier is based on two cascade stages and a reactive inter-stage matching network (L1=378 pH, C1= 375 fF) (Fig. A.2(a)). The first stage is biased for low-noise and an emitter inductor (Le = 70 pH) is used for near-simultaneous noise and gain match, and the second stage is biased for high-gain. The input matching is done using Lb (220 pH) with a simulated Q of 14 at 19 GHz. An output reactive network acts as a matching circuit between the RF amplifier and the subharmonic mixer (L2=484 pH, C2= 270 fF). The bandwidth of the inter-stage and output matching networks is widened using R1 (300 Ω) and R2 (170 Ω). The simulated gain and noise figure of the RF amplifier is 30-28 dB and 3.3-3.5 at 18-20 GHz, respectively, with an input P_{1dB} of -40 dBm and an input IIP_3 of -26 dBm at 19 GHz. The bias current is 8.7 mA.

The subharmonic mixer is based on a differential LO doubler circuit and an RF transconductance stage with a bias current of 6 mA (Fig. A.2(b)). A resistive load is used and increases the gain bandwidth of the IF-stage (1-3 GHz). A small emitter degeneration resistor (Re = 12 Ω) is present in the RF-stage to increase its linearity. The LO balun was designed using full-wave EM simulations and is built using the M6 and M5 metal layer and results in a simulated loss of 1-1.5 dB. The gain and phase difference of the passive balun are 0.11 dB and 1.1° at 10.5 GHz, respectively. The simulated conversion loss of the subharmonic mixer is 7 dB for an LO power of 1-3 dBm, but this design results in a high NF of 24 dB. The noise figure is simulated for an LO power of 2-9 dBm and is 24-25 dB. This is still acceptable due to the input RF amplifier with a gain of 28 dB. A series choke (L3 = 186 pH, C3 = 308 fF) is added at the mixer output port to short the $2f_{LO}$ leakage signal.

The IF amplifiers are resistively loaded due to the IF bandwidth of 1-3 GHz and the requirement for a very small chip size (a high impedance load with a CLC transformer was not possible). The first cascade stage consumes only 4.1 mA, while the second common-emitter stage

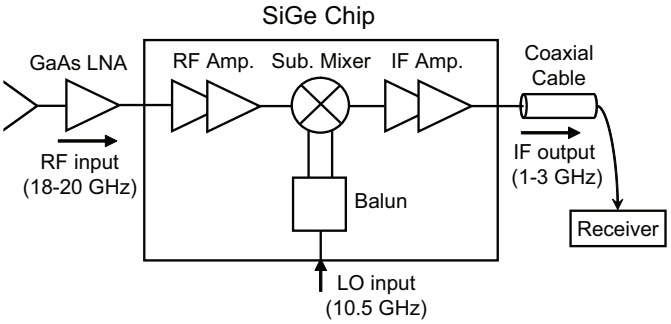


Figure A.1: Block diagram of the 18-20 GHz subharmonic satellite down-converter.

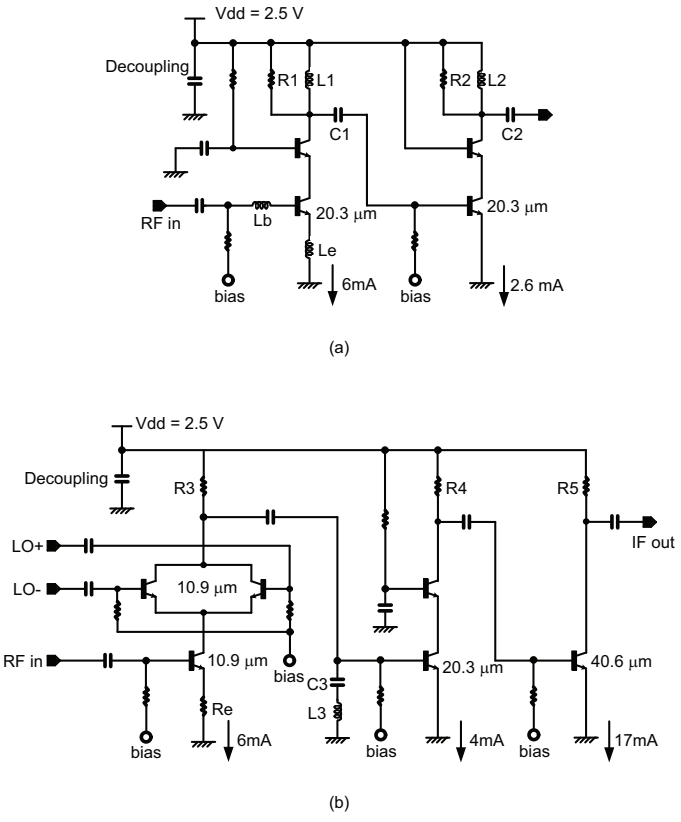


Figure A.2: (a) Input RF amplifier (two stage design), (b) subharmonic mixer and IF amplifier.

consumes 17.3 mA with a collector resistance of 75 Ω. This results in an ouput impedance of 43-j28 Ω when the CPW pad RC model is taken into account. The capacitive output impedance will be cancelled by the IF bonding inductance of 1-2 nH. The simulated IF amplifier gain is 21 dB at 1-3 GHz with an output P_{1dB} of 0-1 dBm.

The chip is built using the Jazz SiGe SBC18HAZ technology which offers a 0.18-μm SiGe transistor (f_T=150-160 GHz), 0.18-μm CMOS (not used), a 6-layer metal process (Fig. A.3) and 5.6fF/μm^2 stacked MIM capacitors between M3/M5 and M4 [69]. A microstrip transmission-line is used with M6 for the signal line and M1/M2/M3/M5 for the ground plane. Also, M4 and M6 are used as VDD plane for easy integrating with decoupling capacitors. DC-20 GHz ESD diodes capable of handling 1.2 KV of human body model and with C = 20.7 fF are placed on the RF, LO and IF ports. Also, ESD diodes with a 3.6 kV breakdown are placed on the bias nodes. The input and output ports are compatible with 150 μm pitch CPW probes and are done with M6. A pad model consisting of a shunt C = 30.8 fF, R = 260 Ω network is taken in the simulations. Inductors and connecting transmission-lines are simulated using Sonnet [26], a full-wave EM-solver. All transistors are biased using current mirrors. The transistor models used are the "nominal process" models and are provided by Jazz.

A.3 Measurements

Fig. A.4 presents the 18-20 GHz subharmonic down-converter with a size of 1.1×0.7 mm^2 including all pads. The supply voltage is set at 2.5 V and the bias current is 31.5 mA which is a bit lower than the simulated value of 36 mA. The chip operated well for an LO power of 1.5-3.5 dBm at 10.5 GHz ($2f_{LO}$ = 21 GHz), and an LO power of 2.5 dBm is used for all the presented data. The measured gain and noise figure are 35-40 dB and 4.8-9.8 dB for an RF of 18-20 GHz (IF of 3-1 GHz), respectively (Fig. A.5 and Fig. A.6). The noise figure increases rapidly for an IF $<$ 1 GHz ($f_{RF} > 20$ GHz) since the subharmonic mixer and IF amplifiers are based on a high-pass design and have low gain in this frequency range. This is clearly seen in the gain from 17-25 GHz for a fixed LO of 10.5 GHz (Fig. A.7). TABLE A.1 presents the measured LO and $2f_{LO}$ leakage at the IF and RF ports for different LO frequencies. It is seen that the LO and 2LO isolation at the RF port is $>$ 50 dB, and is $>$ 14 dB at the IF port. The measured S_{11} is $<$ -9 dB at 18-20 GHz and S_{22} is -15 dB for an IF of 300 MHz to 4 GHz (as expected) (Fig. A.8). All measurements agree well with simulations except for S_{11} (simulated value is -15 dB at 19 GHz). Finally, the measured output P_{1dB} is +2.4 dBm at 1-3 GHz (simulated is 0-1 dBm) and the measured IIP_3 is -36 dBm for a two-tone test at 19 GHz and 19.1 GHz (Fig. A.9). The

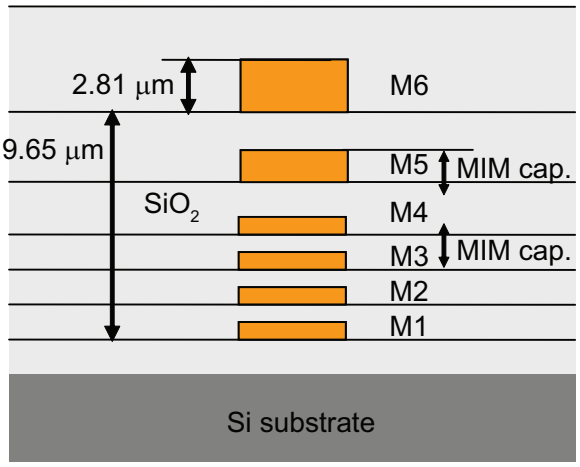


Figure A.3: Metal stack layer of the Jazz SBC18HAZ.

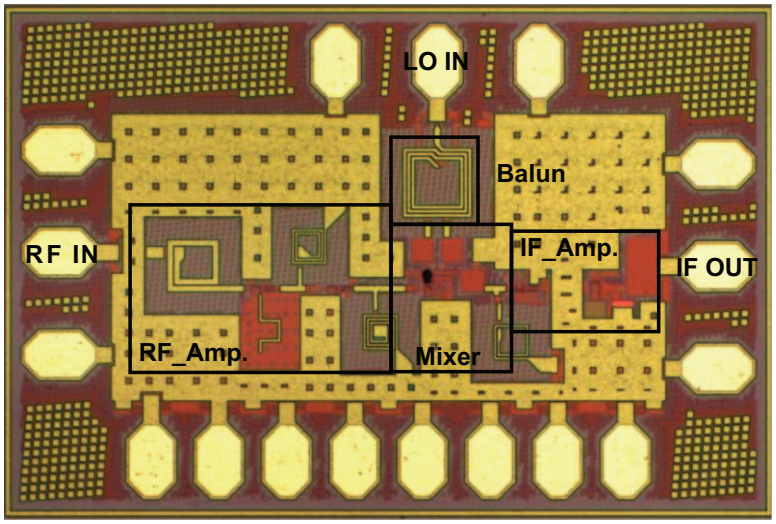


Figure A.4: Microphotograph of 18-20 GHz subharmonic down-converter (1.1×0.7 mm^2 including all pads.)

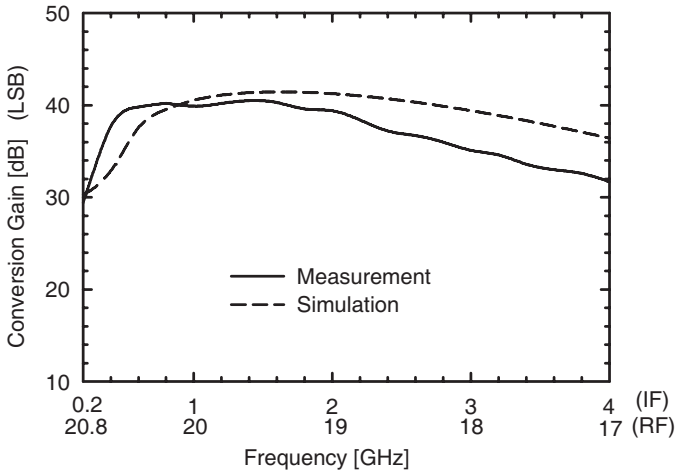


Figure A.5: Measured conversion gain of the subharmonic down-converter.

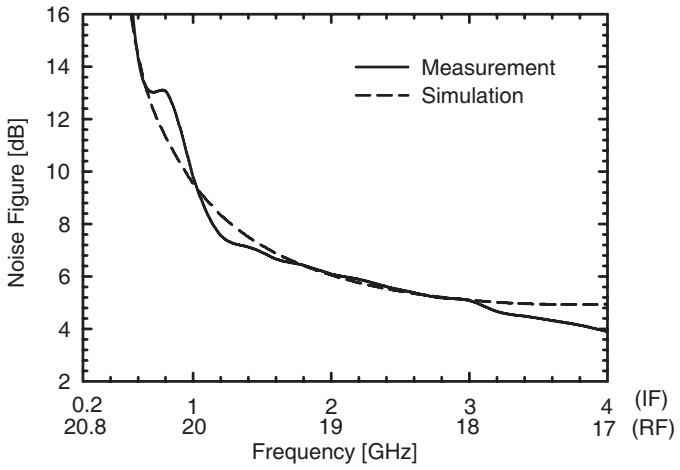


Figure A.6: Measured noise figure of the subharmonic down-converter.

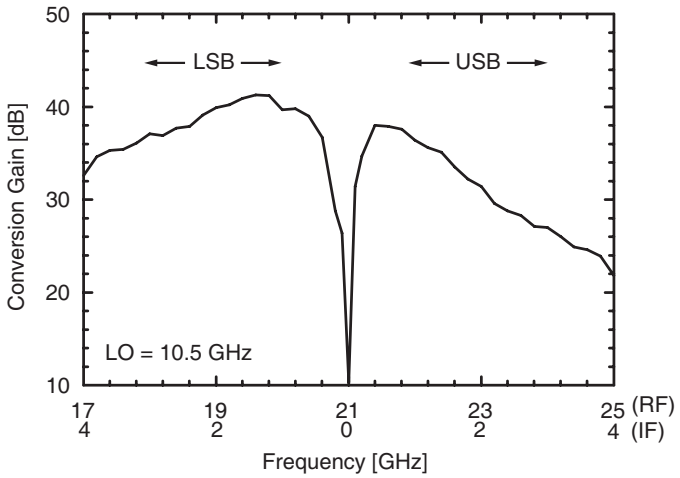


Figure A.7: Measured LSB and USB conversion gain of the subharmonic down-converter.

Table A.1: Measured LO and 2LO leakage at the RF and IF ports for an LO power of 2.5 dBm.

	LO Frequency (GHz)	Leakage (dBm)
Leakage (LO-to-RF port)	10	< -50
	10.5	
	11	
	20	< -50
	21	
	22	
Leakage (LO-to-IF port)	10	-23.2
	10.5	-23.9
	11	-23.4
	20	-17.9
	21	-14.6
	22	-15.1

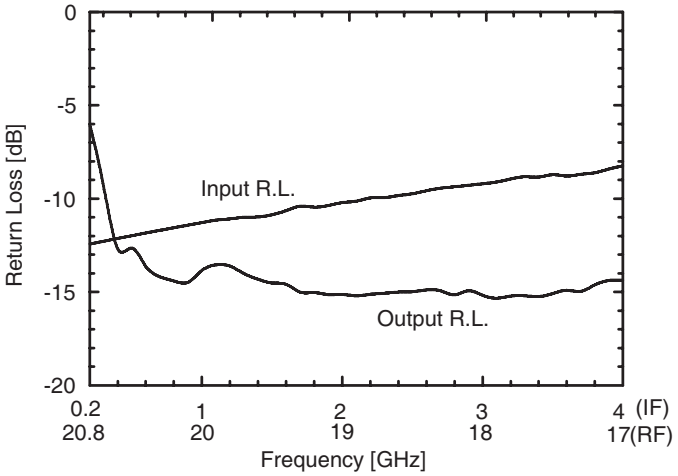


Figure A.8: Measured input and output return loss of the subharmonic down-converter.

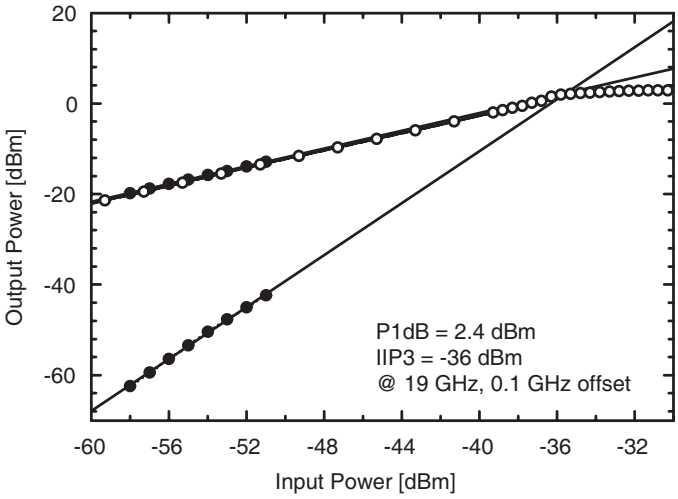


Figure A.9: Measured P_{1dB} and IIP_3 of the subharmonic down-converter.

IIP_3 is limited by the subharmonic mixer.

A.4 Conclusion

An 18-20 GHz subharmonic downconverter was developed using a low cost 0.18-μm SiGe technology. The chip achieves excellent conversion gain, acceptable noise figure and high output P_{1dB} at 18-20 GHz. In future designs and for lower NF, it is recommended that a standard Gilbert cell mixer be used with an LO doubler at 10.5 GHz. The measured performance agrees well with simulations showing the maturity of this process.

A.5 Acknowledgements

This work was supported in part by U.S. Monolithics, Gilbert, Arizona.

Appendix A is mostly a reprint of the material as it appears in IEEE Silicon Monolithic Integrated Circuits in RF Systems, 2009. Sang Young Kim; Kenneth V. Buer; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Bibliography

[1] D. Parker and D. Z. Zimmermann, "Phased Arrays - Part I: Theory and architectures," *IEEE Trans. Microw. Theory Tech.*, vol. 50, pp. 678–687, Mar. 2002.

[2] C. A. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. Wiley-Interscience, 2005.

[3] T. M. Hancock and G. M. Rebeiz, "A 12-GHz SiGe phase shifter with integrated LNA," *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 977–983, Mar. 2005.

[4] F. Ellinger, H. Jackel, and W. Bachtold, "Varactor-loaded transmission-line phase shifter at C-band using lumped elements," *IEEE Trans. Microw. Theory Tech.*, vol. 51, pp. 1135–1140, Apr. 2003.

[5] D.-W. Kang and S. Hong, "A 4-bit CMOS phase shifter using distributed active switches," *IEEE Trans. Microw. Theory Tech.*, vol. 55, pp. 1476–1483, Jul. 2007.

[6] D. W. Kang, J. G. Kim, B. W. Min, and G. M. Rebeiz, "Single and 4-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Tech.*, vol. 57, pp. 3534–3543, Dec. 2009.

[7] C. Campbell, S. Brown, T. Inc, and O. Beaverton, "A compact 5-bit phase shifter MMIC for K-band satellitecommuncaion systems," *IEEE Trans. Microw. Theory Tech.*, vol. 48, pp. 2652–2656, Dec. 2000.

[8] Y. Ayasli, S. W. Miller, R. Mozzi, and L. K. Hanes, "Wide-band monolithic phase shifter," *IEEE Trans. Microw. Theory Tech.*, vol. 32, pp. 1710–1714, Dec. 1984.

[9] C.-Y. Kim, D.-W. Kang, and G. M. Rebeiz, "A 44-46-GHz 16-Element SiGe BiCMOS High-Linearity Transmit/Receive Phased Array," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 730–742, Mar. 2012.

[10] S. Y. Kim and G. M. Rebeiz, "A Low-Power BiCMOS 4-Element Phased Array Receiver for 76-84 GHz Radars and Communication Systems," *IEEE Journal of Solid State Circuits*, vol. 47, pp. 359–367, Feb. 2012.

[11] S. Y. Kim, O. Inac, C.-Y. Kim, and G. M. Rebeiz, "A 76-84 GHz 16-Element Phased Array Receiver with a Chip-Level Built-In-Self-Test System," in *IEEE Radio Frequency Integrated Circuits Symp*, June 2012.

[12] J.-L. Kuo, Y.-F. Lu, T.-Y. Huang, Y.-L. Chang, Y.-K. Hsieh, P.-J. Peng, I.-C. Chang, T.-C. Tsai, K.-Y. Kao, W.-Y. Hsiung, J. Wang, Y. Hsu, K.-Y. Lin, H.-C. Lu, Y.-C. Lin, L.-H. Lu, T.-W. Huang, R.-B, and H. W. Wu, "60-GHz Four-Element Phased-Array Transmit/Receive System-in-Package Using Phase Compensation Techniques in 65-nm Flip-Chip CMOS Process," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 743–756, Mar. 2012.

[13] M. Chua and K. W. Martin, "1GHz programmable analog phase shifter for adaptive antennas," in *IEEE Proc. Custom Integrated Circuits Conf.*, May 1998, pp. 71–74.

[14] K. Koh and G. M. Rebeiz, "0.13-um CMOS phase shifters for X-, Ku-, and K-band phased array," *IEEE Journal of Solid State Circuits*, vol. 42, pp. 2535–2546, Nov. 2007.

[15] ——, "An X-and Ku-Band 8-Element Phased-Array Receiver in 0.18-μm SiGe BiCMOS Technology," *IEEE Journal of Solid State Circuits*, vol. 43, pp. 1360–1371, June 2008.

[16] K. Koh, J. W. May, and G. M. Rebeiz, "A millimeter-wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18-μm SiGe BiCMOS Technology," *IEEE J. Solid State Circuits*, vol. 44, pp. 1498–1509, May 2009.

[17] Y. Yu, P. Baltus, A. Graauw, E. Heijden, C. Vaucher, and A. Roermund, "A 60 GHz Phase Shifter Integrated With LNA and PA in 65 nm CMOS for Phased Array Systems," *IEEE Journal of Solid State Circuits*, vol. 45, pp. 1697–1709, Sep. 2010.

[18] I. Sarkas, M. Khanpour, A. Tomkins, P. Chevalier, P. Garcia, and S. Voinigescu, "W-band 65-nm CMOS and SiGe BiCMOS transmitter and receiver with lumped I-Q phase shifters," in *IEEE Radio Frequency Integrated Circuits Symp*, June 2009, pp. 441–444.

[19] M. Elkhouly, C.-S. Choi, S. Glisic, C. Scheytt, and F. Ellinger, "Millimeter-wave beamforming circuits in SiGe BiCMOS," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2010, pp. 129–132.

[20] M. Elkhouly, S. Glisic, F. Ellinger, and J. Schyett, "A 60 GHz four channel beamforming transmitter in 0.25 μm SiGe BiCMOS technology," in *IEEE European Microwave Integrated Circuits Conference (EuMIC)*, Oct. 2011, pp. 25–28.

[21] D.-W. Kang, K.-J. Koh, and G. Rebeiz, "A Ku-Band Two-Antenna Four-Simultaneous Beams SiGe BiCMOS Phased Array Receive," *IEEE Trans. Microw. Theory Tech.*, vol. 58, pp. 771–780, Apr. 2010.

[22] K.-J. Koh, "Integrated Microwave and Millimeter-Wave Phased-Array Designs in Silicon Technologies," *Ph.D. Dissertation, University of California, San Diego*, 2008.

[23] M. Borremans, C. D. Ranter, and M. Steyaert, "A CMOS dual-channel, 100-MHz to 1.1-GHz transmitter for cable applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1904–1913, Dec. 1999.

[24] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, pp. 873–887, Jun. 2001.

[25] K.-J. Koh, M.-Y. Park, C.-S. Kim, and H.-K. Yu, "Subharmonically pumped CMOS frequency conversion (up and down) circuits for 2-GHz WCDMA direct-conversion transceiver," *IEEE J. Solid-State Circuits*, vol. 39, pp. 871–884, Jun. 2004.

[26] *Sonnet v12*, www.sonnetsoftware.com, Sonnet Software Inc., Syracuse, NY.

[27] *Cascade Impedance Standard Substrate, P/N: 138-357*, www.cmicro.com, Cascade Microtech.

[28] A. E. Ashtiani, S. Nam, S.Lueyszyn, and I. D. Robertson, "Monolithic Ka-band 180-degree analog phase shifter employing HEMT based varactor diodes," *IEE Colloq. Microwave and Millimetre-Wave Oscillators and Mixers*, vol. 48, pp. 7/1–7/6, Dec. 1998.

[29] B. Min and G. M. Rebeiz, "Single-Ended and differential Ka-Band BiCMOS Phased Array Front-Ends," *IEEE Journal of Solid State Circuits*, vol. 43, pp. 2239–2250, Oct. 208.

[30] ——, "Ka-Band Low-Loss and High-Isolation Switch Design in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 56, pp. 1364–1371, June 2008.

[31] J. Han and H. Shin, "A scalable model for the substrate resistance in multi-finger RF MOSFETs," in *IEEE MTT-S Int. Symp. Dig.*, Jun. 2003, pp. 2105–2108.

[32] *BiCMOS-8HP Model Reference Guide*, IBM Microelectronics Division, July 2007.

[33] B. Min and G. M. Rebeiz, "Ka-band BiCMOS 4-bit phase shifter with integrated LNA for phased array T/R modules," in *IEEE MTT-S Int. Symp. Dig.*, Jun. 2007, pp. 479–482.

[34] H. P. Forstner, H. Knapp, H. Jager, E. Kolmhofer, J. Platz, F. Starzer, M. Treml, A. Schinko, G. Birschkus, J. Bock, K. Aufinger, R. Lachner, T. Meister, H. Schafer, D. Lukashevich, S. Boguth, A. Fischer, F. Reininger, L. Maurer, J. Minichshofer, and D. Steinbuch, "A 77 GHz 4-Channel Automotive Radar Transceiver in SiGe," in *IEEE Radio Frequency Integrated Circuits Symp*, June 2008, pp. 233–236.

[35] C. Wagner, H. P. Forstner, G. Haider, A. Stelzer, and H. Jager, "A 79-GHz radar transceiver with switchable TX and LO feedthrough in a Silicon-Germanium technology," in *IEEE BCTM*, Oct. 2008, pp. 105–108.

[36] S. Trotta, B. Dehlink, A. Ghazinour, D. Morgan, and J. John, "A 77 GHz 3.3V 4-channel transceiver in SiGe BiCMOS technology," in *IEEE BCTM*, Oct. 2009, pp. 186–189.

[37] S. Trotta, B. Dehlink, R. Reuter, Y. Yin, J. John, J. Kirchgessner, D. Morgan, P. Welch, J. J. Lin, B. Knappenberger, I. To, and M. Huang, "A multi-channel Rx for 76.5GHz automotive radar applications with 55 dB IF channel-to-channel isolation," in *IEEE EuMIC*, Sept. 2009, pp. 192–195.

[38] S. Trotta, H. Knapp, D. Dibra, K. Aufinger, T. F. Meister, J. Bock, W. Simburger, and A. L. Scholtz, "A 79GHz SiGe-Bipolar Spread-Spectrum TX for Automotive Radar," in *IEEE ISSCC Dig.*, Feb. 2007, pp. 430–613.

[39] T. Mitomo, N. Ono, Y. Yoshiara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE Journal of Solid State Circuits*, vol. 45, pp. 928–937, Apr. 2010.

[40] Y. Kawano, T. Suzuki, M. Sato, T. Hirose, and K. Joshin, "A 77 GHz Transceiver in 90 nm CMOS," in *IEEE ISSCC Dig.*, Feb. 2009, pp. 310–312.

[41] S. T. Nicolson, K. H. K. Yau, S. Pruvost, V. Danelon, P. Chevalier, P. Garcia, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "A Low-Voltage SiGe BiCMOS 77-GHz Automotive Radar Chipset," *IEEE Trans. Microw. Theory Tech.*, vol. 56, pp. 1092–1104, May 2008.

[42] S. T. Nicolson, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "Single-Chip W-band SiGe HBT Transceivers and Receivers for Doppler Radar and Millimeter-Wave Imaging," *IEEE Journal of Solid State Circuits*, vol. 43, pp. 2206–2217, Oct. 2008.

[43] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22-29-GHz/77-81-GHz BiCMOS transceiver for automotive radars," *IEEE Journal of Solid State Circuits*, vol. 44, pp. 3469–3485, December 2009.

[44] J. Lee, Y. Li, M. Hung, and S. Huang, "A Fully-Integrated 77-GHz FMCW Radar Transceiver in 65-nm CMOS Technology," *IEEE Journal of Solid State Circuits*, vol. 45, pp. 2746–2756, December 2010.

[45] J. Hasch, U. Wostradowski, S. Gaier, and T. Hansen, "77 GHz radar transceiver with dual integrated antenna elements," in *IEEE German Microwave Conf.*, Mar. 2010, pp. 280–283.

[46] B. Schoenlinner, X. Wu, J. P. Ebling, G. V. Eleftheriades, and G. M. Rebeiz, "Wide-scan spherical-lens antennas for automotive radars," *IEEE Trans. Microw. Theory Tech.*, vol. 50, pp. 2166–2175, Sep. 2002.

[47] I. Gresham, N. Jain, T. Budka, A. Alexanian, N. Kinayman, B. Ziegner, S. Brown, and P. Staecker, "A compact manufacturable 76-77-GHz radar module for commercial ACC applications," *IEEE Trans. Microw. Theory Tech.*, vol. 49, pp. 44–58, Jan. 2001.

[48] Y. Asano, S. Ohshima, T. Harada, M. Ogawa, and K. Nishikawa, "Proposal of millimeter-wave holographic radar with antenna switching," in *IEEE MTT-S Int. Symp. Dig.*, May 2001, pp. 1111–1114.

[49] R. Feger, C. Wagner, S. Schuster, S. Scheiblhofer, H. Jager, and A. Stelzer, "A 77-GHz FMCW MIMO Radar Based on an SiGe Single-Chip Transceiver," *IEEE Trans. Microw. Theory Tech.*, vol. 57, pp. 1020–1035, May 2009.

[50] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas," *IEEE J. Solid State Circuits*, vol. 41, pp. 2795–2806, Dec. 2006.

[51] D. Lockie and D. Peck, "High-data-rate millimeter-wave radios," *IEEE Microwave Magazine*, vol. 10, pp. 75–83, Aug. 2009.

[52] J. Wells, "Faster than fiber: The future of multi-G/s wireless," *IEEE Microwave Magazine*, vol. 10, pp. 104–112, May 2009.

[53] T. Kosugi, A. Hirata, T. Nagatsuma, and Y. Kado, "MM-wave long-range wireless systems," *IEEE Microwave Magazine*, vol. 10, pp. 68–76, Apr. 2009.

[54] I. Sarkas, S. T. Nicolson, A. Tomkins, E. Laskin, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "An 18-Gb/s, Direct QPSK Modulation SiGe BiCMOS Transceiver for Last Mile Links in the 70-80 GHz Band," *IEEE J. Solid State Circuits*, vol. 45, pp. 1968–1980, Oct. 2010.

[55] A. Valdes-Garcia, S. T. Nicolson, J. Lai, A. Natarajan, P. Chen, S. K. Reynolds, J. C. Zhan, D. Kam, D. Liu, and B. Floyd, "A Fully Integrated 16-Element Phased-Array Transmitter in SiGe BiCMOS for 60-GHz Communications," *IEEE J. Solid State Circuits*, vol. 45, pp. 2757–2773, Dec. 2010.

[56] S. K. Reynolds, A. S. Natarajan, M. Tsai, S. Nicolson, J. C. Zhan, L. Duixian, D. G. Kam, O. Huang, A. Valdes-Garcia, and B. A. Floyd, "A 16-element phased-array receiver IC for 60-GHz communications in SiGe BiCMOS," in *IEEE Radio Frequency IC Symp.*, May 2010, pp. 461–464.

[57] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A Thirty Two Element Phased-array Transceiver at 60 GHz with RF-IF Conversion Block in 90nm Flip Chip CMOS process," in *IEEE Radio Frequency IC Symp.*, May 2010, pp. 457–460.

[58] K. Kim, K. Ahn, T. Lim, H. Park, and J. Yu, "A 60 GHz Wideband Phased-Array LNA With Short-Stub Passive Vector Generator," *IEEE Microwave and Wireless Components Letters*, vol. 20, pp. 628–630, Nov. 2010.

[59] S. Kishimoto, N. Orihashi, Y. Hamada, M. Ito, and K. Maruhashi, "A 60-GHz band CMOS phased array transmitter utilizing compact baseband phase shifters," in *IEEE Radio Frequency IC Symp.*, June 2009, pp. 215–218.

[60] Y. Atesal, B. Cetinoneri, M. Chang, R. Alhalabi, and G. M. Rebeiz, "Millimeter-Wave Wafer-Scale Silicon BiCMOS Power Amplifiers Using Free-Space Power Combining," *IEEE Trans. Microw. Theory Tech.*, vol. 59, pp. 645–655, Apr. 2011.

[61] D. Shin and G. M. Rebeiz, "Low-power low-noise 0.13 μm CMOS X-band phased array receivers," in *IEEE MTT-S Int. Symp. Dig.*, May 2010, pp. 956–959.

[62] D. M. Pozar, *Microwave Engineering, New York: John Wiley & Sons*, 3rd ed. Wiley, 2003.

[63] K. Koh and G. M. Rebeiz, "A Q-Band Four-Element Phased-Array Front-End Receiver with Integrated Wilkinson Power Combiners in 0.18-μm SiGe BiCMOS Technology," *IEEE Trans. Microw. Theory Tech.*, vol. 56, pp. 2046–2053, Sep. 2008.

[64] S. Y. Kim and G. M. Rebeiz, "A 4-Bit Passive Phase Shifter for Automotive Radar Applications in 0.13 μm CMOS," in *IEEE CSICS*, Oct. 2009, pp. 1–4.

[65] T. Yu and G. M. Rebeiz, "A 22-24 GHz 4-Element CMOS Phased Array With On-Chip Coupling Characterization," *IEEE Journal of Solid State Circuits*, vol. 43, pp. 2134–2143, Sep. 2008.

[66] J.-J. Hung, T. M. Hancock, and G. M. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," *IEEE Journal of Solid State Circuits*, vol. 53, pp. 754–761, Feb. 2005.

[67] B. Cetinoneri, Y. A. Atesal, A. Fung, and G. M. Rebeiz, "W-Band Amplifiers With 6-dB Noise Figure and Milliwatt-Level 170-200-GHz Doublers in 45-nm CMOSl," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 692–701, Mar. 2012.

[68] T. Copani, S. A. Smerzi, G. Girlando, G. Ferla, and G. Palmisano, "A single-chip receiver for multi-user low-noise block down-converters," in *IEEE ISSCC Dig.*, Feb. 2005, pp. 438–440.

[69] *SBC18 Design Manual*, Jazz Semiconductor, Mar. 2006.