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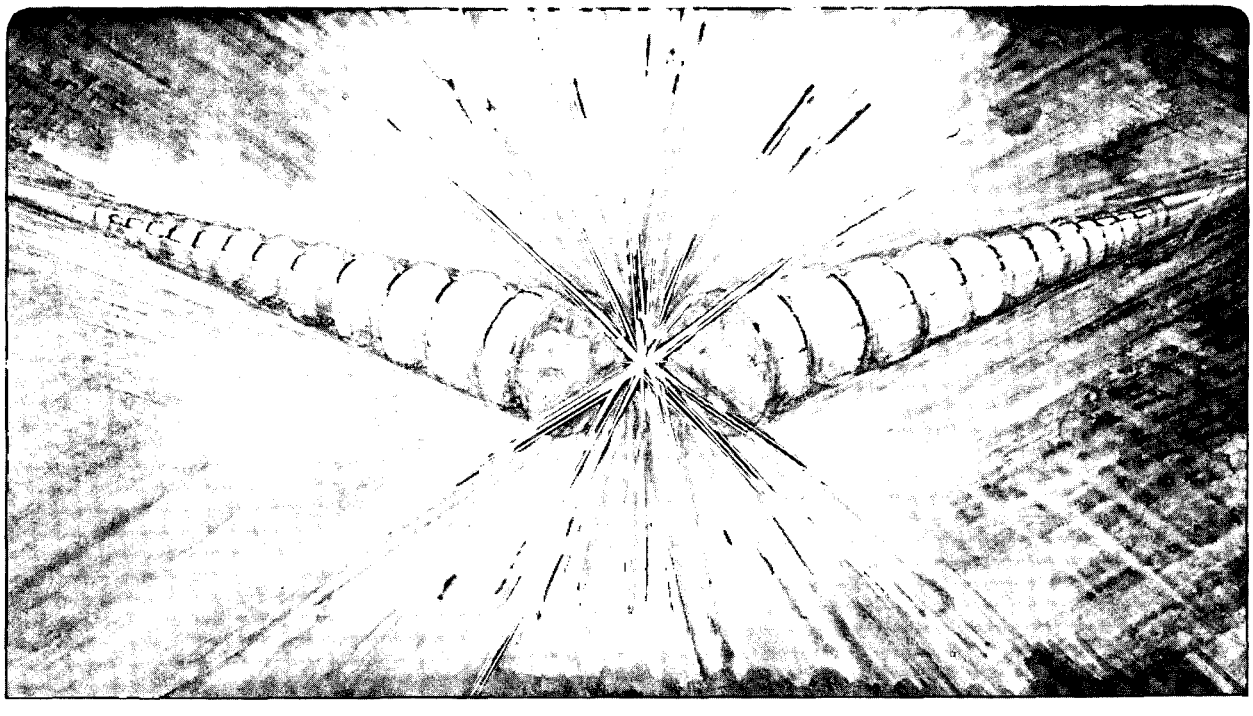

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CHARACTERIZATION AND CONTROL OF WAFER CHARGING EFFECTS DURING HIGH-CURRENT ION IMPLANTATION

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EEPROM-based sense and memory devices provide direct measures of the charge flow and potentials occurring on the surface of wafers during ion beam processing. Sensor design and applications for high current ion implantation are discussed.

INTRODUCTION

Control of charge build-up on the surface of device wafers has been recognized as a critical issue for ion implantation processing for more than a decade[1]. Detrimental effects, such as destructive breakdown of thin dielectric films and premature wearout of MOS transistors, have been linked to the buildup of excessive surface charges (either positive or negative) during exposure to the implanting ion beam. Even in the absence of the multiplier effects of large-area gate and interconnect structures, a net charge imbalance of $\approx 3\mu C/cm^2$ ($2x10^{13}$ ions/cm^2) is sufficient to exceed the 10MV/cm threshold for catastrophic rupture of SiO_2 films[2,3].

Measurements of surface potentials and currents using sensors employing EEPROM transistors as sensing and memory devices provide direct information on the process environment experienced by device wafers during ion beam processing. Data from EEPROM-based sensors is especially valuable in providing clues for the design

of advanced ion beam processing equipment since it is in the form of electrical parameters that can be directly related related to ion beam parameters such as the local charge density and plasma potential.

EEPROM SENSE-MEMORY DEVICES

The CHARM (CHARge Monitor)-2 consists of sensors employing EEPROM transistors (Fig. 1) with dual poly gates; including a thin tunnel oxide region for transfer of charges to and from the lower, "floating" gates. The upper, "control" gates are connected to large-area antenna structures which cover the EEPROM sensor sites. Voltages and currents on the wafer surface are inferred from shifts in the transistor threshold voltage after exposure to an ion beam process environment (Fig. 2).

Some of the programming gates are connected to the Si wafer substrate through poly resistors. Low-resistance shunts are used for structures which monitor the effects of uv-light from the ion beam plasma on the leakage of charge from the floating gate via carrier excitation into the oxide conduction band. High-resistance poly lines are used to monitor charge flux through the effect on the EEPROM programming state by the voltage drop across the resistor connected to the Si substrate. The range of surface currents that can be sensed by the CHARM-2 devices span from $0.1A/cm^2$ (using the full dynamic range of the threshold voltage swing (24V) and a 10^5 Ω load resistor) to $4\mu A/cm^2$ (assuming a measurement noise limit of of 0.24V on the threshold voltage)(Fig. 3). The lower net current density corresponds to a 98% space-charge neutralization of a 20mA ion beam with a $3x3cm^2$ cross-section.

The CHARM-2 device array includes a variety of structures designed to differentiate between a number of competing paths for charge flows in the device wafer. For example, lateral current paths along the wafer surface are monitored with antenna structures which are surrounded by guard-rings which are tied to the Si substrate and separated from the antenna edge by gaps ranging from 3 to 30μm. Antenna structures which are tied to the Si substrate

through p^+ or n^+ diodes record the largest signals, of positive or negative polarity, encountered during the ion beam exposure. This memory capability is particularly important in processes where transients effects are significant; such as photoresist outgassing and carbonization during the early stages of high-dose implants.

After ion implantation, the effects of antenna electrode (control gate) voltage for various antenna-to-substrate load resistances can be used to extract equivalent circuit parameters for the contributions to the current flows for the energetic ion beam, the "slow ions" [4], created by collisional ionization events between the dopant ions and background gas atoms, and the electrons in the ion beam plasma.

ION IMPLANTATION STUDIES

EEPROM-like structures have been used to study charging effects of ion beam processing during plasma etching [5] and ion implantation [7]. Early versions of CHARM devices have been used in a number of studies of ion implantation [8-11].

In the present study, 80keV As implants were investigated using an NV 10-80 high-current implanter. The CHARM devices were fabricated on 100mm wafers and were covered with patterned photoresist over the field oxide regions, leaving only the charge collection electrodes exposed to the direct ion beam. All implants were done with a dose of $5x10^{15}$ As/cm^2 at an ion beam current of 6mA.

A secondary electron-type electron shower was used to provide supplemental electrons. The emission current of the electron shower was varied so that the net current collected on the wafer holder disk varied from +6mA (with the electron shower off) to -1mA and -8mA. As the electron emission is increased, the median surface potentials measured by the unipolar sensors shifted from +20 and -10V with the electron shower off to +11 and -22V at full electron emission (Fig. 4). Electron emission corresponding to zero net current on the wafer disk resulted in nearly symmetrical values of the median unipolar potentials (+/- 15V) and optimal yield for CMOS product devices [11].

The local variation of threshold voltage shifts over the surface of the 100mm wafers often showed a strong "bulls-eye" pattern. This was particularly evident in the case of the strongly positive charging that occurred without the electron shower (Fig. 5). Strong spatial variations have also been reported in other EEPROM studies[6,7].

EQUIVALENT CIRCUIT MODEL

The correlation of electrical data from EEPROM-like sensors with SPICE-based equivalent circuit models of plasma conditions has been successfully realized for several important plasma etching configurations[5]. The complications related to the strong transient effects involved with the scanning of the ion implantation beam over the wafer surface and the many charge exchange mechanisms between the wafer surface and beam plasma [1,2] have so far precluded modeling at a similar level of detail.

A first approach[12] to modeling of the ion beam is to consider the charge flow onto the wafer surface to be a sum of current sources made up of the positive "fast" ion beam, j_{ib}, positive "slow" ions created by collisional ionization of background gases in the ion beam plasma, j_p, and electrons coupled to the beam plasma, j_e (Fig. 6). The effect of the positive ion charging by the "fast" ion beam is enhanced by the ejection of secondary electrons from the wafer surface so the net contribution is $j_{ib}(1+\gamma_s)$, where γ_s is the secondary electron emission coefficient. The flow of plasma electrons to the wafer surface is represented by $j_{ip}(\exp(eV_{device}/kT_e)$, where V_{device} is the surface-to-substrate potential and T_e is the electron temperature.

For the case of strong positive charging, a 6mA As beam with no electron shower, this equivalent source model was fitted to the observed variation of the charge collection potential with load resistance with model values of j_p = 1.26mA/cm^2, T_e = 5eV and $j_{ib}(1+\gamma_s)$ = 49.2 mA/cm^2. The beam parameters derived from the data for the small-area charge collection electrodes where checked by applying the model to the larger area electrodes (Fig. 7). The large

value of $j_{ib}(1+\gamma_s)$, nearly an order of magnitude more than the estimated value of j_{ib}, points to strong effects of secondary electron emission from the Al charge collection electrodes and the possibility of significant charge flow associated with outgassing from the photoresist layer.

The non-linear variation of the potential on charge collection electrodes with load resistance (Fig. 7) highlights the mixed behavior of the ion beam plasma as a current-voltage source. For low load impedance and small area charge collection electrodes, which collect little current, the ion beam plasma acts as a current source following an Ohmic behavior with load impedance. At higher load impedances, the beam plasma behaves like a voltage source, clamping the surface potential at a value determined by the electron temperature. For the larger area electrodes, which collect more current, the saturation of the voltage source behavior occurs at lower load impedance. Effects of charge collection area have been reported for in-situ voltage sensors (with much large geometries) imbedded in wafer disks[13].

DISCUSSION

The beam plasma model used to describe the response of the CHARM-2 devices in the high current ion beam has some interesting consequences for understanding of the buildup of potentials on wafer surfaces. Isolated conductors, such as the un-grounded charge collection electrodes or floating poly-gate lines during source/drain implant, will float to a potential such that the net current flow is zero. Under these conditions, the net positive and negative current flows balance:

$$n_p v_p/2 + j_{ib}(1+\gamma_s) \approx (n^0_e v_e/4)*\exp(e\emptyset/kT_e) \qquad [1]$$

where n_p is the plasma ion density, v_p is the plasma ion velocity, n^0_e is the electron density at a reference position where $\emptyset$, the local floating potential, is zero and v_e is the average electron velocity [12].

The potential difference across a gate dielectric, which drives the destructive effects associated with wafer charging in ion beam processes, depends on the device geometries. For example, in the case of extended lines of gate and conductor lines, one portion of the device can be biased to the level inside the ion beam plasma and the substrate can be biased to the floating potential outside the ion beam.

For the case of where only plasma electrons and ions are present, the floating potential of isolated electrodes will be negative with respect to the beam plasma potential, that is:

$$e\emptyset/kT_e \approx \mathrm{Ln}(2\{m_e/m_p\}^{1/2}) < 0 \qquad [2]$$

where m_e is the electron mass and m_p is the mass of the plasma ions. However, if the secondary electron emission is significant, the floating potential of isolated electrodes can be drive strongly positive;

$$e\emptyset/kT_e \approx [4\, j_b/e^* n^0_e {}^* v_e]^*(1+ \gamma_s) > 1 \qquad [3].$$

SUMMARY

The use of EEPROM-based sense-memory devices provide a powerful approach to the characterization of wafer charging effects. Since the data from EEPROM-based devices is not tied to oxide wearout and breakdown characteristics, it provides a direct link to the electrical characteristics of the ion beam plasma. Insights gained through the use of these devices, such as the CHARM-2 array, can be expected to play an important role in the understanding of charge mechanisms, process control of ion beam systems in production environments and design of advanced ion beam processing equipment. Successful modeling of ion beam plasma characteristics can lead to the development of reliability models where charge-damage resistant IC device designs and processes could be developed without extensive evaluation and burn-in procedures.

ACKNOWLEDGEMENTS

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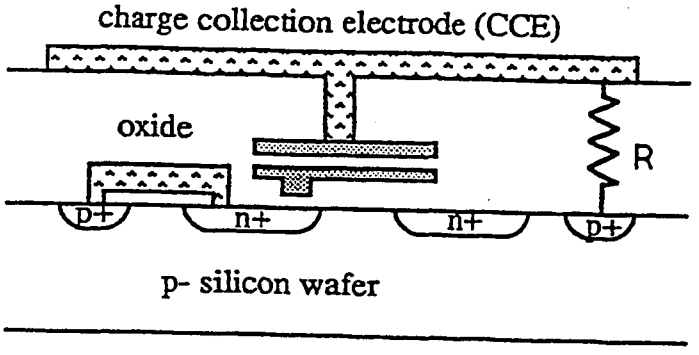


Figure 1. A resistor-loaded CHARM-2 EEPROM gate tied to the Si substrate through a p^+ diode.

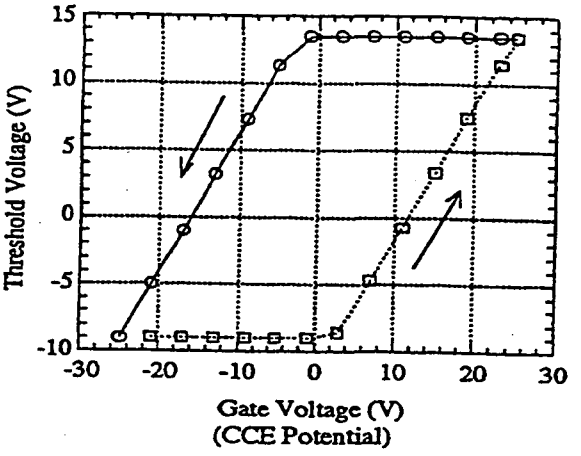


Figure 2. Calibration curves for transistor threshold voltages and control gate voltage (directly tied to charge collection electrodes).

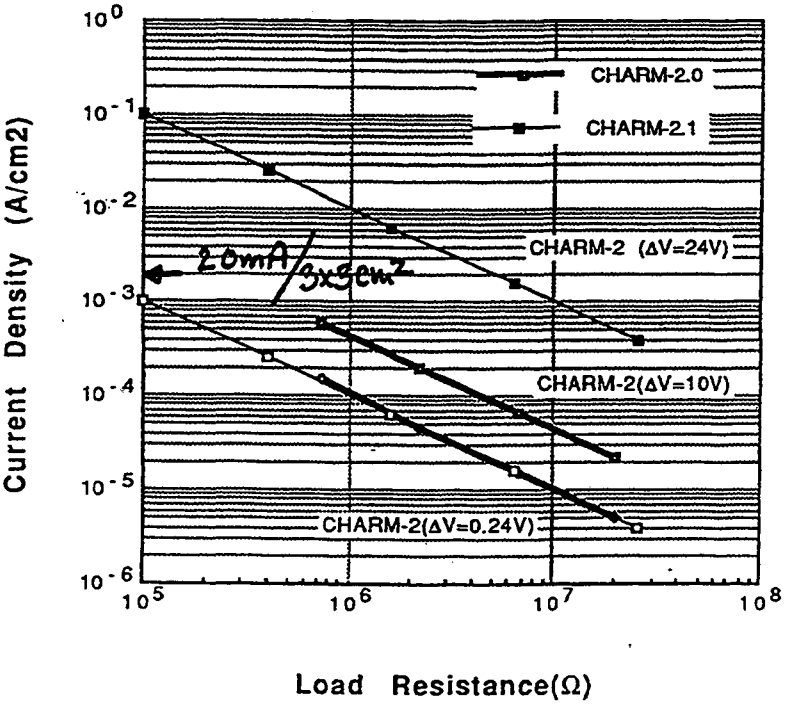


Figure 3. Range of sensitivity of CHARM-2 devices for surface charge flux measurements corresponding to potential drops of 0.24, 10 and 24V along load resistors between the charge collection electrodes and Si substrate (for 0.24mm^2 electrodes).

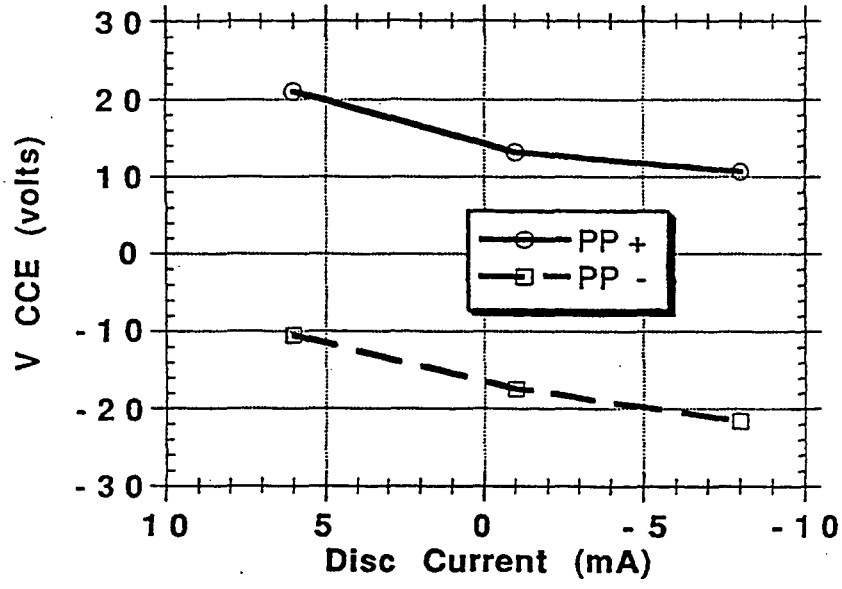


Figure 4. Median positive (PP+) and negative (PP-) voltages observed with the unipolar sensors on a CHARM-2 wafer for a 80 keV, 6 mA As^+ beam in a high current implanter with a solid-disk wafer holder. The net current to the wafer disk and the surface potentials shifted towards a negative polarity as the emission on the secondary-electron-type electron shower was increased.

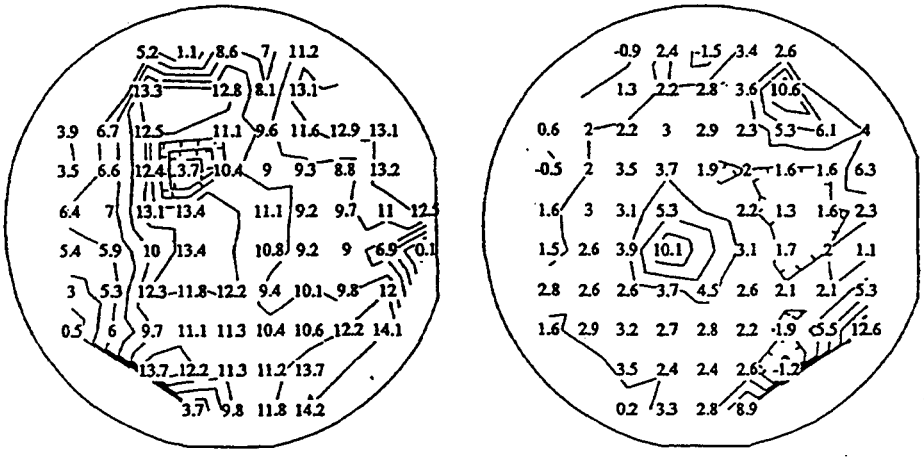
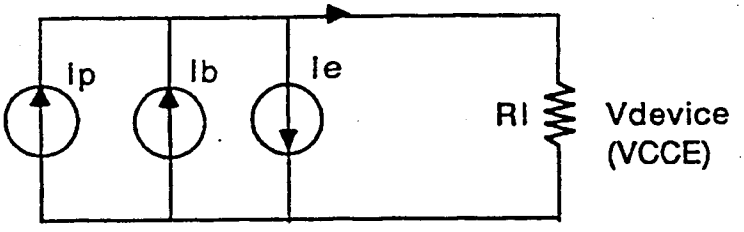


Figure 5. Wafer maps of threshold voltages after implantation by a 6mA, 80keV As beam with an NV 10-80 implanter. Note the strongly positive values near the center. The wafer maps are for net disk currents of 6mA (left) and -1mA (right).



$$V_{\text{device}} = RA\left[j_{ip}(1-\exp[\frac{eV_{\text{device}}}{kT_e}]) + j_{ib}(1+\gamma_s) \right]$$

Figure 6. Current source model of the implantation beam, including contributions from accelerated "fast" ions, Ib, "slow" ions, Ip, created by collisional ionization of background gas atoms, and electrons, Ie, from various sources.

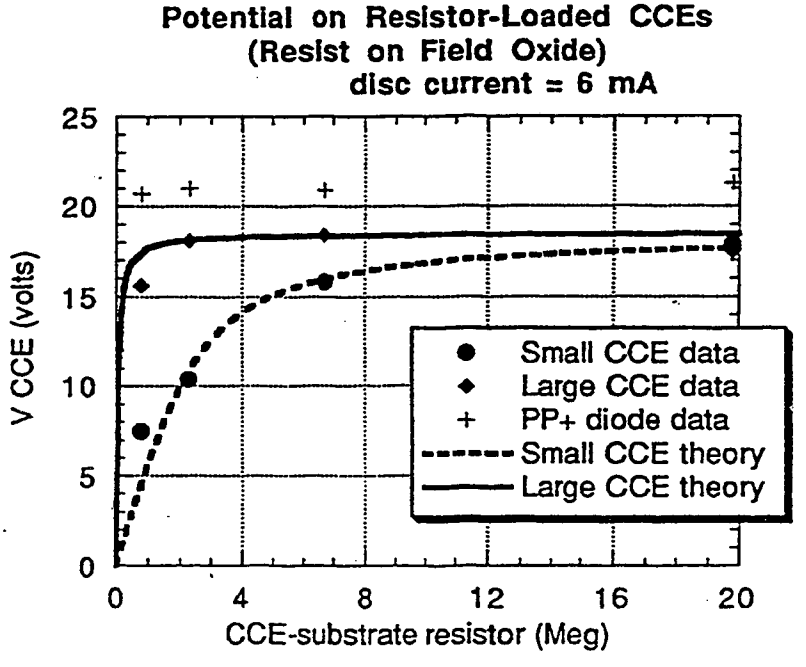
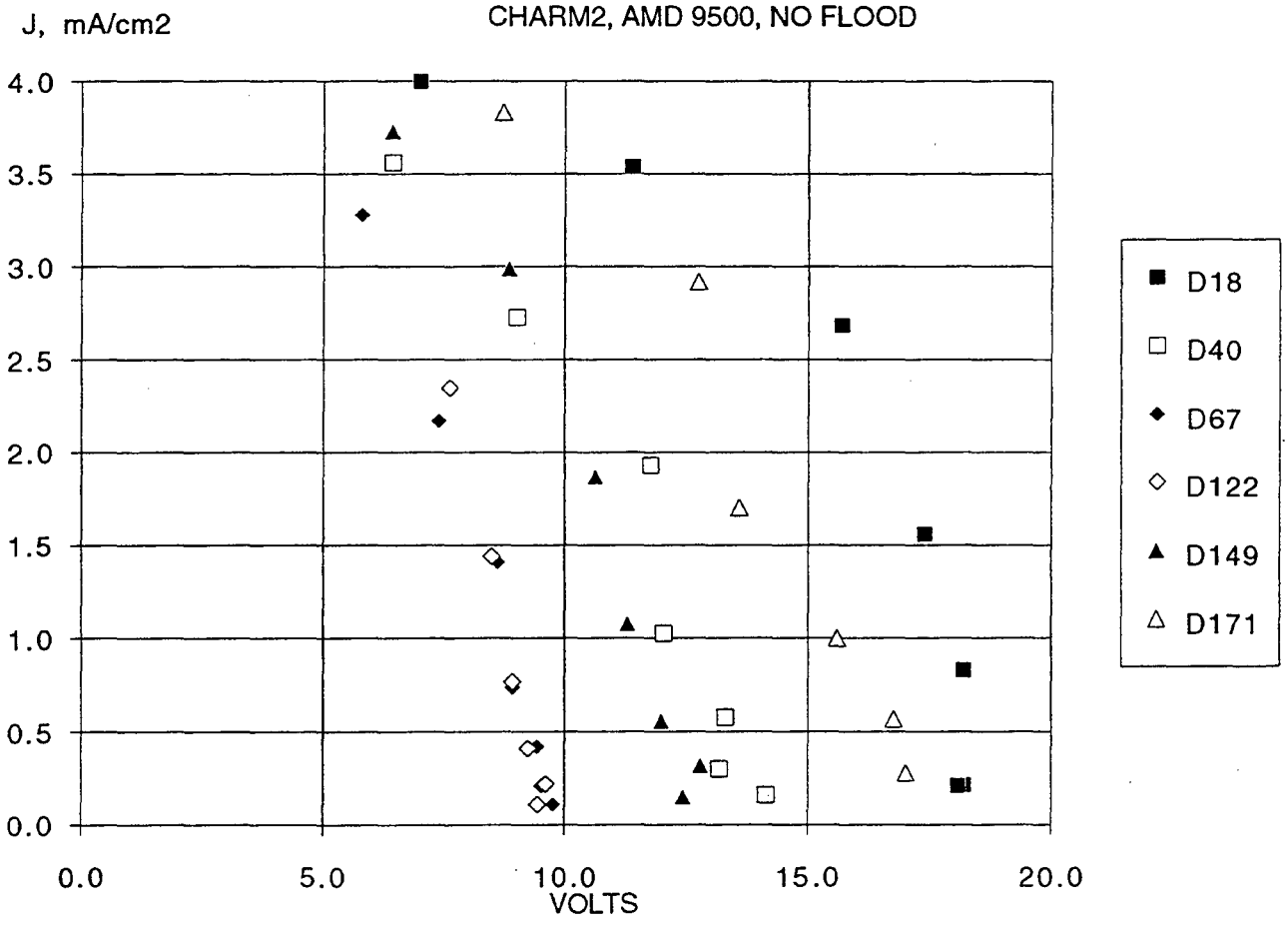


Figure 7. Non-linear voltage response of resistor-loaded charge collection electrodes under conditions of strongly positive charging for an NV 10-80 implanter.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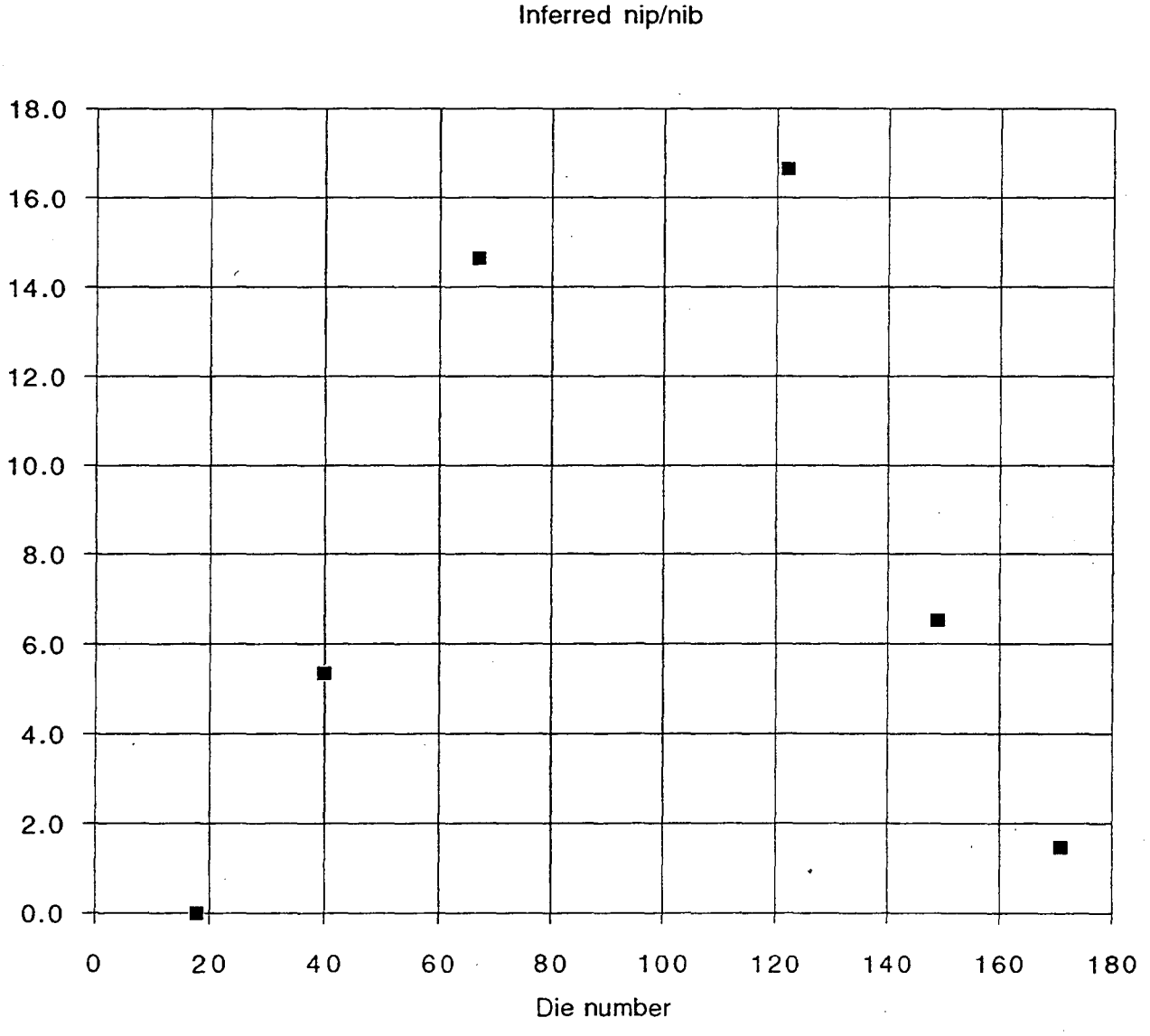
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
5.0
10.0
15.0
20.0
VOLTS
D18
D40
D67
D122
D149
D171

nip/nib vs D


Inferred nip/nib
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10.0
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0.0
0
20
40
60
80
100
120
140
160
180
Die number

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