UNIVERSITY OF CALIFORNIA, SAN DIEGO

# Single-Chip 64- and 256-Element Wafer-Scale Phased Arrays and Communication Circuits in Advanced SiGe and CMOS Technologies

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor William S. Hodgkiss

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The dissertation of Samet Zihir is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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DEDICATION

*To my parents, Ibrahim and Muzeyyen*.

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## PUBLICATIONS

S. Zihir, and G.M. Rebeiz, "A 60 GHz Single-Chip 256-Element Wafer-Scale Phased Array with EIRP of 45 dBm Using Sub-Reticle Stitching," to be submitted to *IEEE Transactions on Microwave Theory and Techniques*, February 2016.

S. Zihir and G.M. Rebeiz, "A DC-20 GHz Wideband High-Linearity IQ Modulator in 45-nm CMOS SOI," to be submitted to *IEEE Transactions on Microwave Theory and Techniques*, December 2015.

M.S. Mehrjoo, S. Zihir, G.M. Rebeiz, and J.F. Buckwalter, "A 1.1-Gbit/s, 10-GHz Outphasing Modulator with 23-dBm Output Power and 60-dB Dynamic Range in 45-nm CMOS SOI," *IEEE Transactions on Microwave Theory and Techniques*, vol.63, no.7, pp. 2289-2300, July 2015.

S. Zihir, O.D. Gurbuz, A. Karroy, S. Raman, G.M. Rebeiz, "A 60 GHz Single-Chip 256-Element Wafer-Scale Phased Array with EIRP of 45 dBm Using Sub-Reticle Stitching," in *Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2015.

S. Zihir, O.D. Gurbuz, A. Karroy, S. Raman, G.M. Rebeiz, "A 60 GHz 64-element Wafer-Scale Phased-Array with Full-Reticle Design," in *Microwave Symposium (IMS), 2015 IEEE MTT-S International*, vol., no., pp.1-3, 17-22 May 2015.

T. Kanar, S. Zihir, and G. M. Rebeiz, "A 2-15 GHz Accurate Built-in Self-Test Circuit for Wide-band Phased Arrays Using Self-Correcting 8-State I/Q Mixers," *IEEE Transactions on Microwave Theory and Techniques*, submitted for publication, November 2015.

Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin, G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2014.

ABSTRACT OF THE DISSERTATION

**Single-Chip 64- and 256-Element Wafer-Scale Phased Arrays and Communication Circuits in Advanced SiGe and CMOS Technologies**

by

Samet Zihir

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2015

Professor Gabriel M. Rebeiz, Chair

The development of millimeter-wave phased arrays has been mostly based on silicon RFIC chips containing 8-16 channels and connected to antennas on organic printed-circuit boards, or on wafer-scale phased arrays with on-chip antennas. Extending the wafer-scale array to a large number of elements results in an un-surmountable challenge, mainly that the phased-array chip may be much larger than a full reticle (approximately 22x22 $mm^2$), and this is not allowed using standard integrated circuit design and layout rules. This dissertation focuses on the implementation of wafer-scale phased array with 64- and 256-elements using sub-reticle stitching techniques. An implementation of the

largest single-chip wafer-scale phased-array ever built is demonstrated. The measured EIRP is 38 dBm and 45 dBm, with measured half-power beamwidth of 12.5° and 6° at 61 GHz for the 64- and 256-element phased arrays, respectively. This work allows the construction of large-scale (1000+ elements) phased-array systems, either on a single wafer or by assembling several of these chips together on a low cost board.

# Chapter 1

# Introduction

Silicon phased-array chips recently converged on 4, 8 or 16 elements on a single chip. Example of these chips include the recent 16-element IBM and UCSD SiGe chips at W-band using RF-beamforming [1–3], the 16-element Broadcom 60 GHz chip using RF-beamforming [4], 4-element digital beamforming chips for automotive radars at 77 GHz [5], and other 8-16 element chips at Q-band. For larger arrays, several of these chips can be placed together using a complex mm-wave printed-circuit board (PCB). This was demonstrated by IBM at 94 GHz, and four 16-element chips were used to create a 64-element array [6]. However, the PCB cost can be high due to its complexity and also, its yield can be low. In short, large size and low-cost mm-wave phased arrays are still a challenge.

Wafer-scale arrays, which include high-efficiency on-wafer antennas, phased-array front-end modules with amplitude and phase control, and a distribution network, all built on a single wafer, are another way to build large-scale arrays. This has been demonstrated at W-band using a 9-element array (6x6 $mm^2$) [7], and at 114 GHz using a 16-element array (6.5x6.5 $mm^2$) [8]. However, true-wafer scale capabilities will only occur if this concept is taken to the reticle level (22x22 $mm^2$), which will allow for a

large number of elements on a single chip, and pave the way for tiling of the reticles together to build a wafer-scale array. This work demonstrates the first full-reticle phased array at 60 GHz with 64 radiating elements and with excellent performance.

The thesis presents a 64- and 256-element 60 GHz wafer-scalable phased array transmitter design and measurements in Jazz SBC18H3 and a DC-20 GHz wideband high-linearity upconverter design and measurements in IBM 45 nm 12SOI process technology.

Chapter 2 presents sub-reticle stitching technique and the usage of this technique in 64- and 256-element 60 GHz phased-array transmitter design. The sub-reticle blocks and the sub-reticle stitching are discussed in detail to form any size of phased array system including 4x4, 8x4, 8x8, 16x8, 16x16 and 32x32. The system is scalable to any number NxN and any phased array as big as the size of wafer.

Chapter 3 presents a 60 GHz wafer-scale transmit phased-array with 256-elements spaced $\lambda/2$ apart in the x and y directions, and occupying an area of 4.14x4.2 $cm^2$ (1740 $mm^2$). The phased array is built using independent RF, transmission-line and control circuit blocks which are stitched together to form an aggregate chip which is much larger than a standard reticle (22x22 $mm^2$). This method allows for a wafer-scale design and can be extended to any size and any shape (rectangular, hexagonal, etc.) up to the edge of the wafer. The blocks include high-efficiency on-wafer antennas, phased-array channels with 3-bits amplitude and 5-bits phase control together with an amplifier having an output power of +3 dBm at 60 GHz. Also, a highly redundant RF distribution network is synthesized from several stitched blocks for improved yield, and the control blocks have redundant SPI control and power strips, also for improved yield. The 256-element array results in a half-power beamwidth of $6^o$ in the E- and H-planes, a directivity of 29 dB, and scans to +/- $55^o$ in the E- and H-planes with near-ideal patterns and a cross-polarization level of $<$-25 dB. The measured EIRP is 45 dBm at 61 GHz and with a 3-dB bandwidth

from 58 to 64 GHz. To our knowledge, this is the largest single-chip phased-array ever developed and allows the construction of large-scale (1000+ elements) phased-array systems, either on a single wafer or by assembling several of these chips together.

Chapter 4 presents 60 GHz links with different modulation schemes including QPSK, 16-QAM, 32-QAM and 64-QAM at different distances 0.4, 4, 30 and 90 m. The 64-element array transmitter is capable of achieving 2 GBps 16-QAM modulation at 4 m in the lab and 1.5 GBps QPSK link at 90 m outside the building. The measurement results presented in this chapter are the best performance shown up-to-date using a phased array transmitter at 60 GHz. Additionally, the 64-element phased array transmitter is tested with 802.11ad standards for next generation 5G systems. The transmitter successfully works with 802.11ad standards up to 90 m. Lastly, the performance of the transmitter array is presented for WirelessHD transfer at 57 GHz while maintaing the HD signal quality even at $\pm 45^{\circ}$ scanning angles.

Chapter 5 presents a 0.01-20 GHz high-linearity up-converting mixer in 45nm CMOS SOI technology. The differential up-converter is based on a combination of thin and thick oxide devices, and a stacked floating-cascode configuration with capacitive gate bias for high power handling. The up-converter consumes 80 mA from a 4 V supply, and results in measured $OIP_{1dB}$ is 15-13 dBm at 6-20 GHz with a conversion gain of $0\pm 1$ dB, and an $OIP3 > 30-25$ dBm and an $OIP2 > 40$ dBm at $10-20$ GHz. The $LO$ to $RF$ isolation and $IF$ to $RF$ isolation is $> 25$ dB at 10 GHz. To our knowledge, this work presents state-of-the-art results and shows the stacking capabilities of CMOS SOI devices.

The thesis concludes with a summary of the works proposed and suggestions for future work.

# Chapter 2

# Scalable Wafer Scale Design and Stitching

## 2.1 Introduction

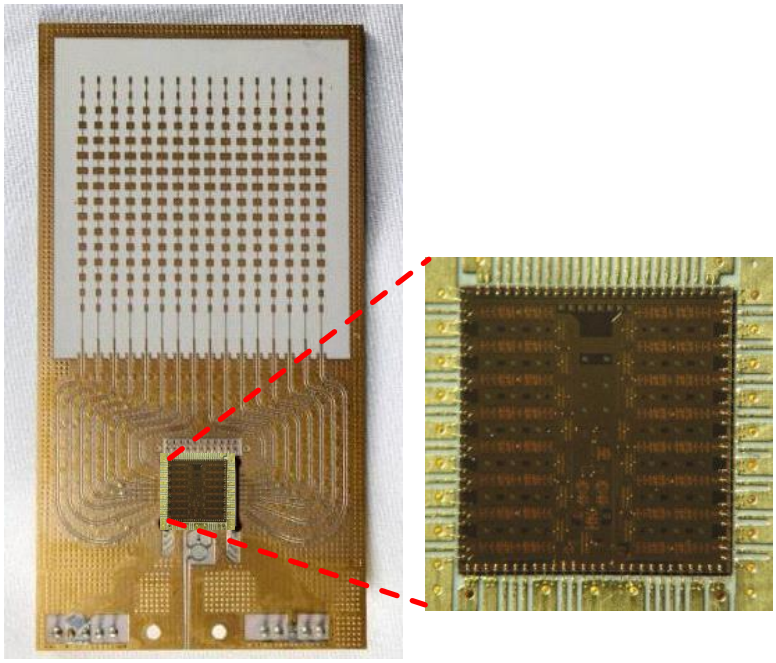
Millimeter-wave phased-arrays on silicon based RFICs have been an important research topic or many years. In recent years with the announcement of possible usage of phased-arrays in next-generation 5G systems, attention on phased-array design and development have tremendously increased. After the first demonstration of early phased-arrays of single, four and 8-elements array on a single-chip [9–17], the development of millimeter-wave phased arrays has been mostly based on silicon RFIC chips containing 8-16 channels [16, 18–21] and connected to antennas on organic printed-circuit boards, or on wafer-scale phased arrays with on-chip antennas. Example of these phased-array systems on include the 16-element IBM and UCSD SiGe chips at 77 GHz and W-band using RF-beamforming [1–3, 22, 23], the 16-element Broadcom 60 GHz chip using RF-beamforming [4], and the 4-element digital beamforming chips for automotive radars at 77 GHz [5]. As shown in Fig. 2.1, for larger arrays, several of these chips can be placed

together using a complex mm-wave printed-circuit board (PCB). This was demonstrated by IBM at 94 GHz, and four 16-element chips were used to create a 64-element array [6]. However, the PCB is complex, and the distribution network from the chip to the antennas can have a loss of 2-3 dB, which is high in a transmit/receive system.

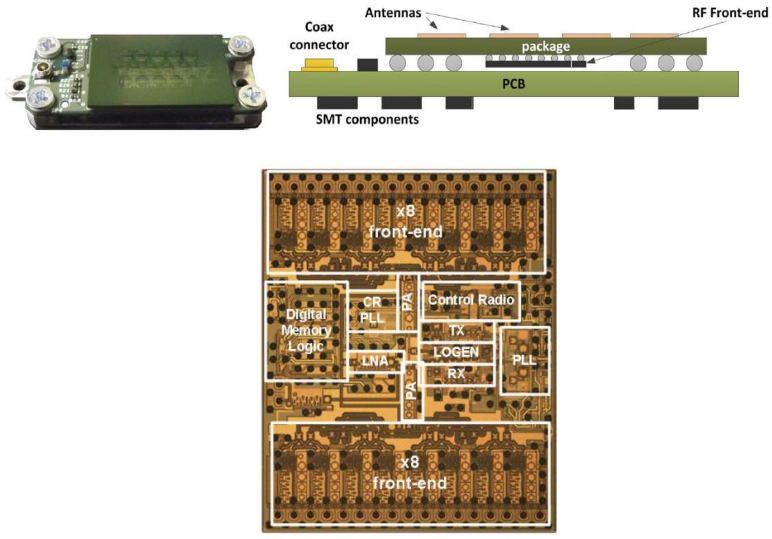
As shown in Fig. 2.2, wafer-scale arrays have been introduced by UCSD as an alternative way to build large-scale millimeter-wave arrays. In this design, high-efficiency on-wafer antennas, phased-array front-end modules with amplitude and phase control, and a distribution network, are all built on a single chip. As shown in Fig. 2.3, this has been demonstrated at W-band using a 9-element array (6x6 $mm^2$) [7], and at 114 GHz using a 16-element array (6.5x6.5 $mm^2$) [8]. Extending the wafer-scale array to a large number of elements results in an un-surmountable challenge, mainly that the phased-array chip may be much larger than a full reticle (approximately 22x22 $mm^2$), and this is not allowed using standard integrated circuit design and layout rules. One way to solve this is to break down the phased-array into fundamental building blocks and stitch them together on the wafer, resulting in a chip which exceeds the standard reticle size. This work demonstrates the first wafer-scale phased array with 256-element built using sub-reticle stitching and with excellent performance.

## 2.2 Sub-reticle stitching Technique

A reticle (22x22 $mm^2$) is the largest area that can be exposed in standard integrated circuit lithography, and a special technique called stitching is used to fabricate chips which are larger than a reticle. The stitching technique is commonly used in CMOS imaging arrays to achieve wafer-scale designs, but has never been applied to mm-wave wafer-scale designs. In this technique, the design of the entire phased-array is partitioned in small blocks called sub-fields which are repeated many times to create the wafer-scale



(a)




(b)

**Figure 2.1**: (a) 77 GHz 8-Tx/8-Rx phased array chip and (b) 16-element 60 GHz Broadcom chip.

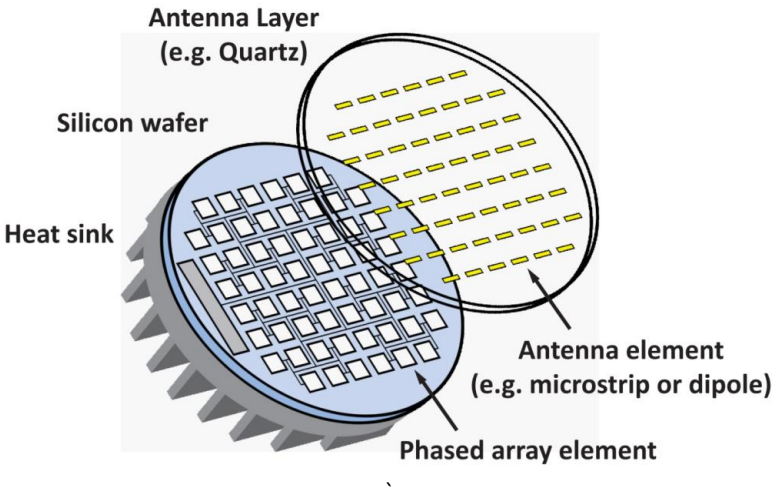



**Figure 2.2**: Wafer-scale arrays with high-efficiency on-wafer antennas as proposed by UCSD.

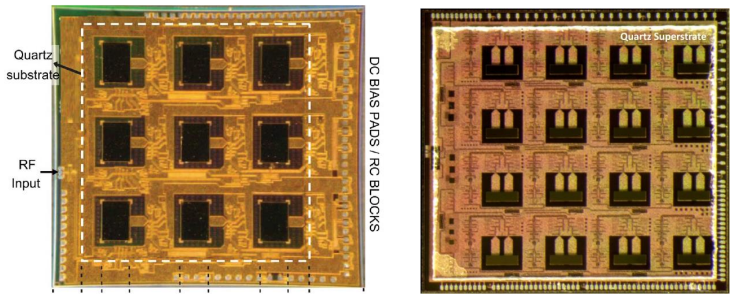



**Figure 2.3**: (a) 9-element W-Band and (b) 16-element 114 GHz phased array.

design. The stitching is done at metals M1 to M6 with an overlap of $< 0.5$ $\mu$m for M1 and $< 1$ $\mu$m for M6 using special stitching masks, but not at the polysilicon or diffusion layers. Therefore, the connections between the different blocks are stitched at all metal levels, but the transistors themselves cannot be stitched (and this is not needed anyways).

Fig. 2.4 presents the fundamental building blocks used in the wafer-scale stitched array. Block-A is the main radiating block in the design. It consists of a 4x4 array in half-wavelength (2.5 mm at 60 GHz) spacing. This block will be repeated many times to form the active radiating area of the arrays. Block-A also contains an active 1:16 distribution network with amplifiers and Wilkinson splitters, and can have two different inputs (left and right). Therefore, the center coupler is a 3-dB hybrid coupler since it allows a feed from the left or right, while keeping a high isolation between the two different feeds. Blocks B1 and B2 are RF and digital input blocks which contain a passive single-ended to differential transformer, Blocks C1 and C2 are digital control and test cells, Blocks D1/D2/D3/D4 are corner connecting blocks (mostly empty), Blocks E1 and E2 are transmission line alone and transmission-line with a hybrid coupler, Blocks F1 and F2 are amplifiers in two different directions and Block G is the center hybrid coupler. Each block contains all the mask layers (38 masks, from the p and n diffusion wells to the top metal level), and result in working circuits but without the pads to the external world (except for the edge blocks).

The wafer-scale array is built in the Jazz SiGe BiCMOS SBC18H3 process technology with $f_T$=240 GHz. The entire wafer-scale phased array (circuits transmission-lines, splitters) are differential and a transformer balun is used at the RF input port(s) to allow for single-ended inputs. Using the blocks proposed, different arrays can be designed in including 4x4, 8x8, 16x16 and 32x32 as shown in Fig. 2.5. The design can be extended any number of array NxN and the largest array will be limited by the size of the wafer used.

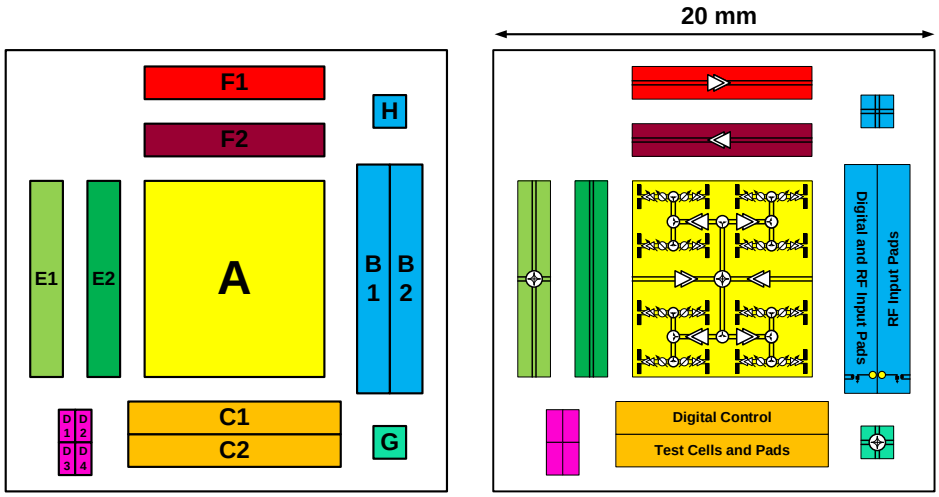



**Figure 2.4**: (a) Building blocks used in the wafer-scale sub-field stitching and (b) Details of the blocks.

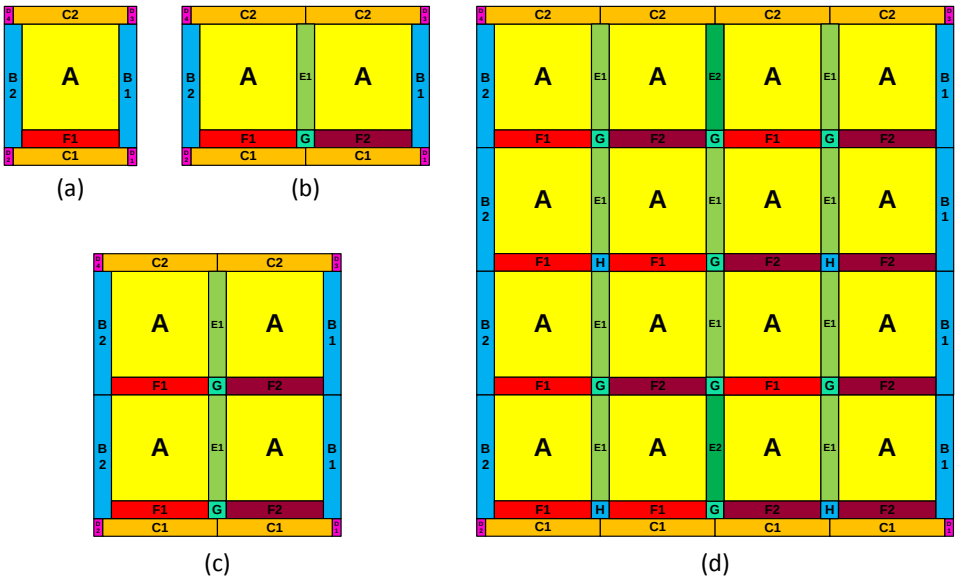



**Figure 2.5**: Possible array configurations can be designed using the proposed technique.

## 2.3 8x8 and 16x16-Element Phased Array Design

For demonstration purposes, two different designs (8x8- and 16x16-element arrays) will be shown. As a first example, a 64-element array will be designed with proposed blocks. The block-level stitching map for 64-element array is shown in Fig. 2.6. In this design 4-Block-As (radiating element with 16 channels) are used to complete 64-element design. Also in Fig. 2.6(b), a single RF-signal path is highlighted. For this design, 6-dividers and 2 line amplifiers (LA) are used to compensate the division loss and ohmic loss.

Fig. 2.7 shows how a 256-element array is constructed from these fundamental blocks (or sub-field), but arrays with other dimensions (rectangular, hexagonal, etc.) can be built using the same technique. First, Block-A is transferred to the silicon wafer at 16 different places to create the 256-element radiating channels. The RF power and digital distribution network is designed in a H-tree configuration using Blocks E, F, G and H. The distribution network utilizes Blocks E1 and 2 as vertical distribution parts, and Blocks F1 and F2 as horizontal distribution parts. The array consists of line amplifiers to compensate for the RF ohmic and division loss. Branchline couplers are used as power dividers in Blocks E1 and G for RF distribution. RF inputs, digital control and supply are provided from the edge Blocks B,C, and D. The RF input is located in the vertical Block B and the array layout results in two possible RF inputs on the left and right side of the array. The horizontal Block C also has two different serial and parallel digital inputs for redundancy. With the RF input chosen, a set of line amplifiers is turned on so as to energize every element in the array. Note that many line amplifiers in the array are not turned on, and are isolated from the array operation with the use of Wilkinson and hybrid coupler networks. Finally, the single RF-path is also provided in Fig. 2.7(b) which consists of 8-dividers and 5 LAs.

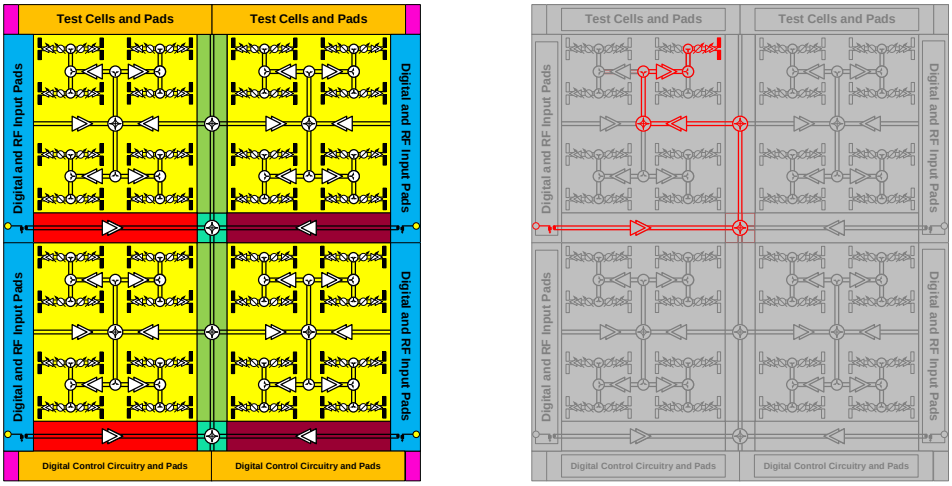



**Figure 2.6**: (a) 64-element array map, and (b) single RF-signal path in the 64-element array.

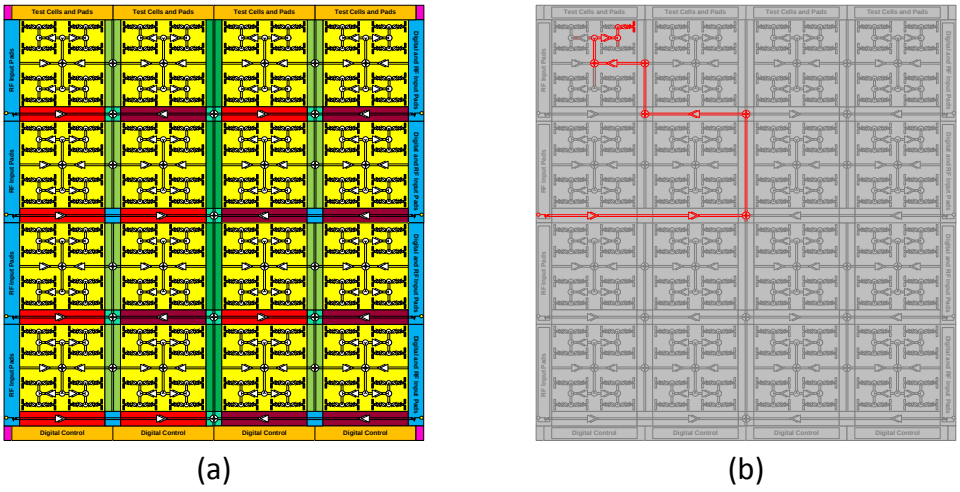



**Figure 2.7**: (a) 256-element array map, and (b) single RF-signal path in the 256-element array.

## 2.4 Conclusion

In this section, the design steps of the proposed wafer-scale array topology is shown in details. The sub-field stitching technique is explained and the steps to use this technique to form scalable array is shown. The proposed technique is shown to form 64-element and 256-element arrays.

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The dissertation author is the primary author of this material.

# Chapter 3

# 64- and 256-Element Phased Array Transmitters with High-Efficiency On-Chip Antennas

## 3.1 Introduction

Silicon phased-array chips recently converged on 4, 8 or 16 elements on a single chip. Example of these chips include the recent 16-element IBM and UCSD SiGe chips at W-band using RF-beamforming [1–3], the 16-element Broadcom 60 GHz chip using RF-beamforming [4], 4-element digital beamforming chips for automotive radars at 77 GHz [5], and other 8-16 element chips at Q-band. For larger arrays, several of these chips can be placed together using a complex mm-wave printed-circuit board (PCB). This was demonstrated by IBM at 94 GHz, and four 16-element chips were used to create a 64-element array [6]. However, the PCB cost can be high due to its complexity and also, its yield can be low. In short, large size and low-cost mm-wave phased arrays are still a challenge.

Wafer-scale arrays, which include high-efficiency on-wafer antennas, phased-array front-end modules with amplitude and phase control, and a distribution network, all built on a single wafer, are another way to build large-scale arrays. This has been demonstrated at W-band using a 9-element array (6x6 $mm^2$) [7], and at 114 GHz using a 16-element array (6.5x6.5 $mm^2$) [8]. However, true-wafer scale capabilities will only occur if this concept is taken to the reticle level (22x22 $mm^2$), which will allow for a large number of elements on a single chip, and pave the way for tiling of the reticles together to build a wafer-scale array. This work demonstrates the first full-reticle phased array at 60 GHz with 64 radiating elements and with excellent performance.

## 3.2 System Design

Fig. 3.1 presents a block-diagram of the 64-element and 256-element wafer-scale transmit array built in the Jazz SBC18H3 process technology. The entire wafer-scale phased array (circuits, transmission-lines, splitters) are differential and a transformer balun is used at the RF input port(s) to allow for single-ended inputs. The active RF signal-paths are highlighted red in Fig. 3.1.The array consists of 4 sub-arrays and 16 sub-arrays each 16 elements for 64- and 256-element arrays, respectively. Each radiating element channel consists of a Variable-Gain Amplifier (VGA), Vector Modulator (VM), Power Amplifier (PA) and a differential antenna feed. Each Block-A includes a dedicated Serial Peripheral Interface (SPI) performing read and write operation as well as with a parallel input option for redundancy. A two-way SPI input scheme, labeled as Vertical and Horizontal Inputs in Fig. 3.1, is adopted to create a redundant control I/O in case one of the inputs are not working properly. As shown in Fig. 3.1, each phased array has a redundant RF input labeled as $RF_{IN2}$ which can be activated if a problem is faced in port $RF_{IN1}$.

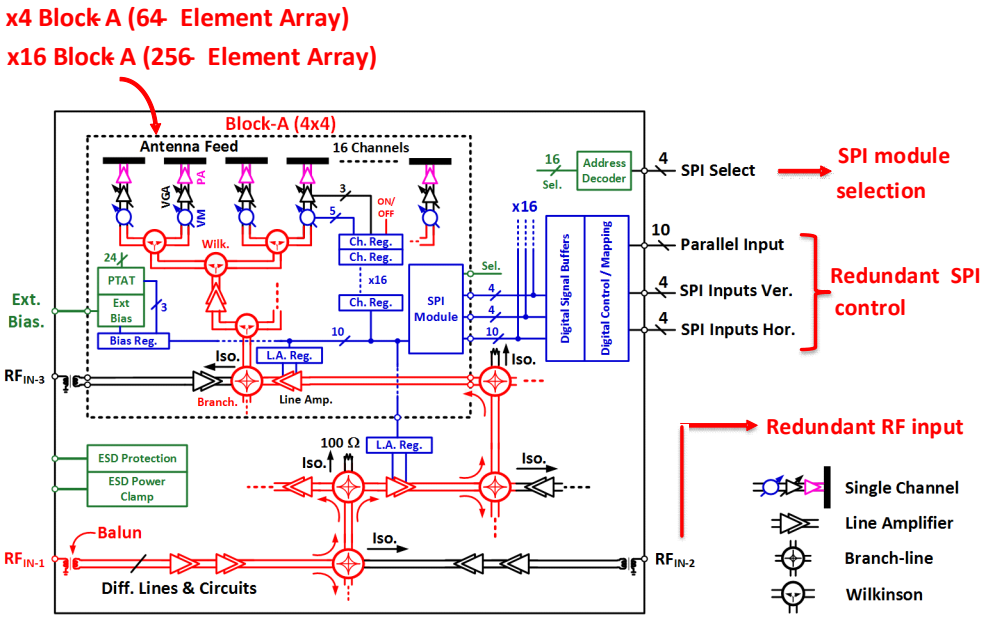
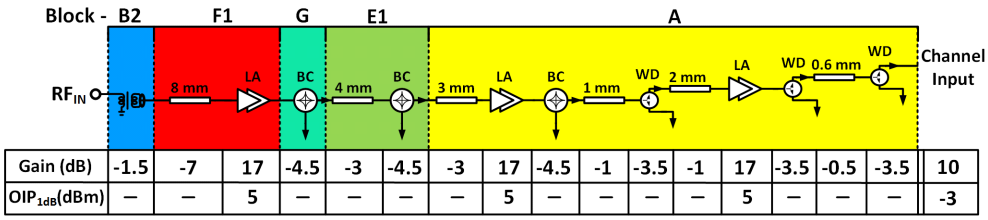
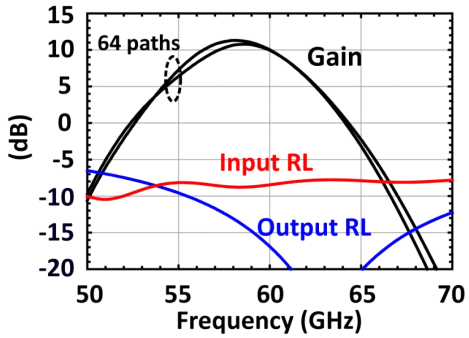



**Figure 3.1**: Block diagram of 8x8 an d16x16-element phased array chips.




| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Gain (dB) | -1.5 | -7 | 17 | -4.5 | -3 | -4.5 | -3 | 17 | -4.5 | -1 | -3.5 | -1 | 17 | -3.5 | -0.5 | -3.5 | 10 |
| $OIP_{1dB}$(dBm) | – | – | 5 | – | – | – | – | 5 | – | – | – | – | 5 | – | – | – | -3 |

(a)




(b)

**Figure 3.2**: Gain and linearity calculations for the 8x8 phased array.

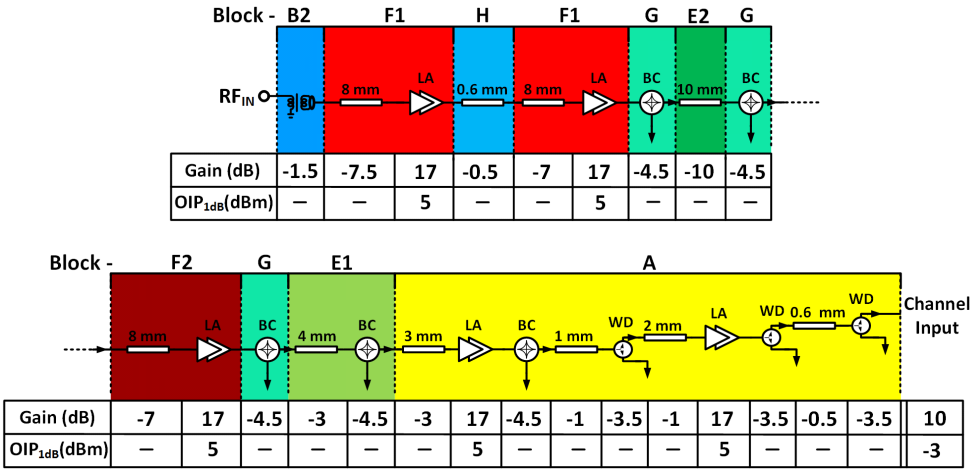
**Table 3.1**: Gain and Loss Calculations for 8x8 and 16x16-Arrays

| | **8x8 Array** | **16x16 Array** |
|---|---|---|
| Total Gain (dB) | 51 | 85 |
| Total Loss (dB) | 41 | 75 |
| Power Cons. (mW) | 850 | 3500 |

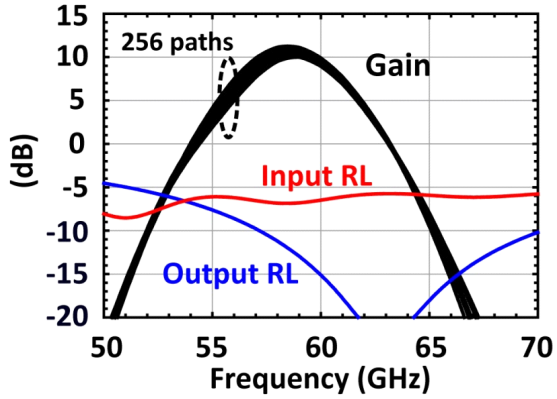
The calculated RF signal gain and linearity requirements for a single path from input to channel-input are shown in Fig. 3.2. The wafer-scale array has a power splitting loss of 41 dB with 18 dB due to the 64-elements, 23 dB due to the differential transmission-line loss (20 mm line lengths, and 0.9 dB/mm at 60 GHz) and the six differential Wilkinson and hybrid couplers used (0.9 dB loss each, 5.5 dB total). Therefore, 3 different line amplifiers, each with a gain of around 13 dB which results in 51 dB total gain as shown in Table 3.1. Similar calculations for 16x16 array are shown in Fig. 3.4. The 16x16 array has a power splitting loss of 75 dB with 24 dB due to the 256-elements, 51 dB due to the differential transmission-line loss (40 mm line lengths, and 0.9 dB/mm at 60 GHz) and the eight differential Wilkinson and hybrid couplers used (0.9 dB loss each, 7.2 dB total). The total loss and gain calculations as well as power consumption for the 8x8 and 16x16 phased arrays in the line amplifiers are tabulated in Table 3.1.

## 3.3 Redundancy Techniques

Because of its large size, the proposed 8x8 and 16x16 arrays need more attention to improve the yield. The large scale implementation may create severe problems like shortage in VDD-GND rails, RF-visa not working line amplifiers, channels and digital control issues. The multiple RF inputs from all four directions (only one of them is active at a time with the appropriate line amplifiers tuned on) also allow the reticle-based phased-array to be scalable in the X and Y directions (on a PCB) or to be stitched together on a single wafer. In short, the reticle-size phased-array is a very solid building block




(a)

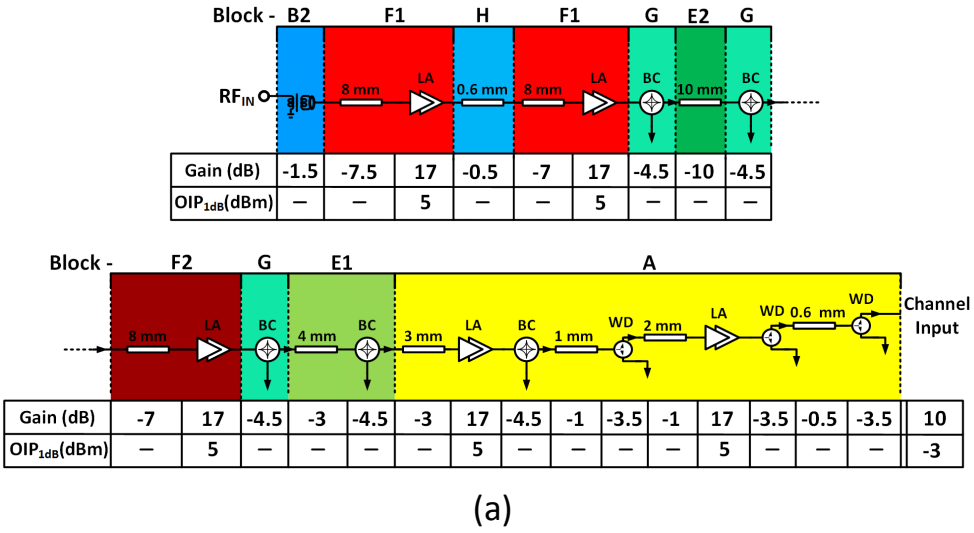



(b)

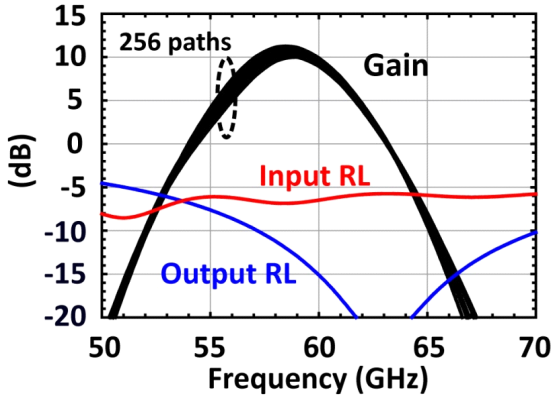
**Figure 3.3**: Gain and linearity calculations for 16x16 array.

for a wafer-scale design. We have solved this problem using a highly novel method: a) first, the entire reticle has multiple inputs and can be fed from four different ports, which is accomplished using hybrid and Wilkinson couplers at the quadrant junctions, and b) each line amplifier is built using two distinct amplifiers in parallel. In addition to RF redundancies, the array includes digital-based redundancy techniques such as parallel control as well as serial control and two side input/outpus for serial control as shown in Fig. 3.6.

We have used other features to increase the wafer-scale array yield. These include a) redundant SPI control lines, b) redundant SPI controllers for the quadrants as shown in Fig. 3.1, c) redundant power distribution from all four sides, and d) bias decoupling capacitors placed in series over the entire chip so as to not short the VDD to GND if one capacitor fails (this is at the expense of lower capacitance density) as shown in Fig. 3.5. For I/O digital control pads, two different sides of 8x8 array are used as shown in Fig. 3.7. SPI-vertical I/O pads are located in Block-C2 and SPI-horizontal I/O pads are located in Block-B which can be activated in case SPI-vertical I/O pads are not working properly to control the array. All of these innovations allow us to result in high yield wafer-scale phased-array chips.




(a)




(b)

**Figure 3.4**: Gain and linearity calculations for 16x16 array.

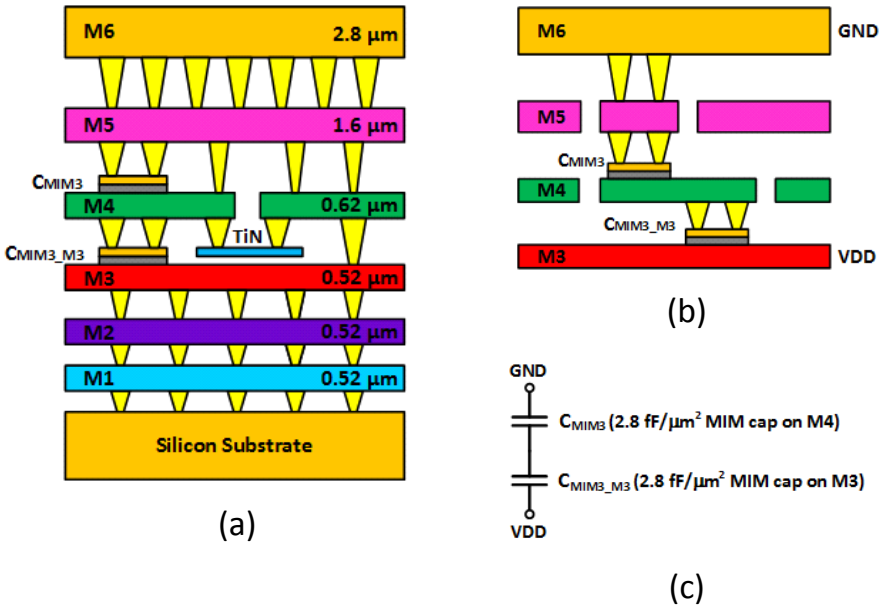



**Figure 3.5**: (a) Jazz SBC18H3 stack-up, (b) redundant stacked MIM capacitor connection in Jazz stack-up and (c) schematic of stacked MIM capacitor cell.

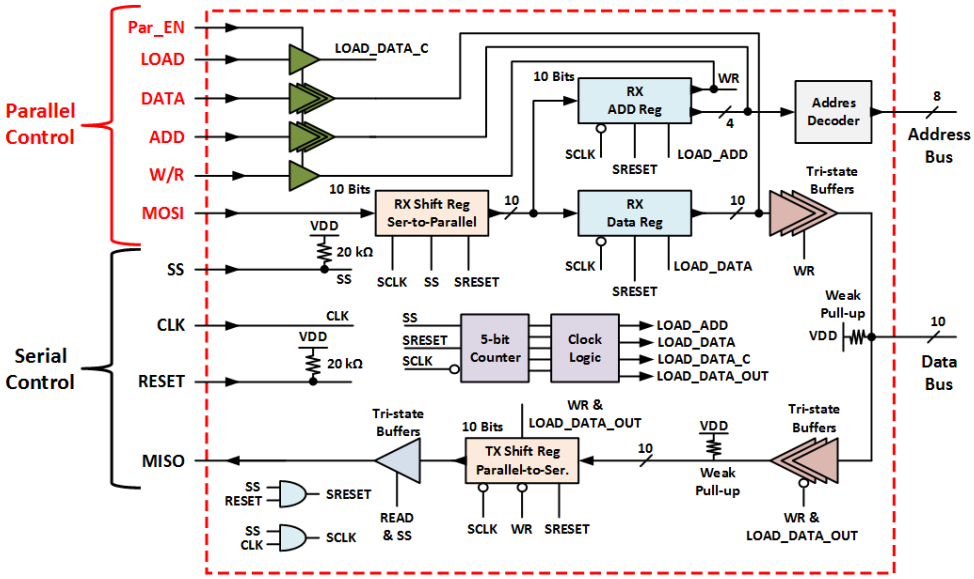



**Figure 3.6**: (a) Detailed schematic of the SPI controller in each Block-A.

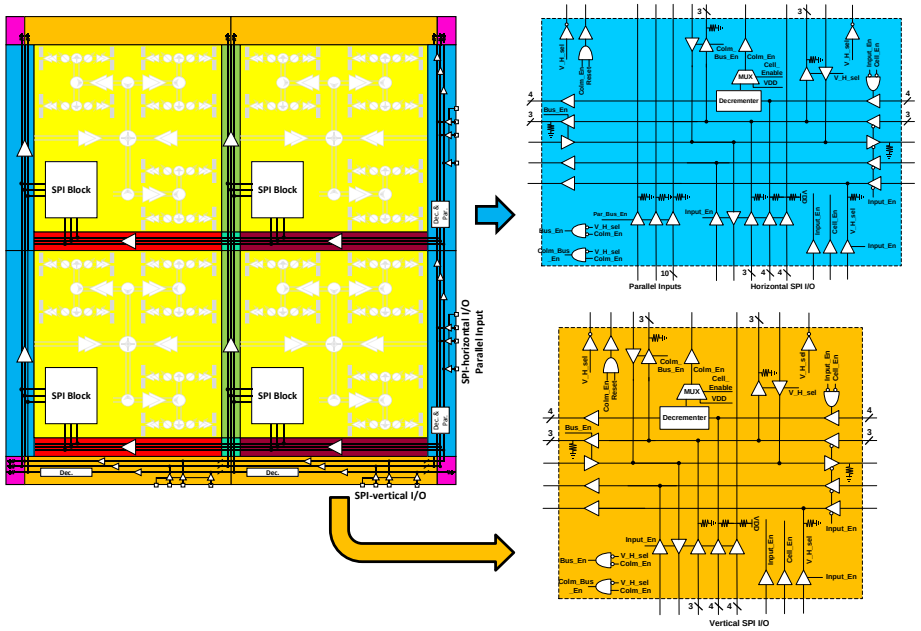



**Figure 3.7**: (a) Detailed block-diagram of the digital control circuitry in Block-B and Block-C.

## 3.4 RF Distribution Elements

The line amplifiers are critical to the operation of the wafer-scale phased array since they compensate for the distribution loss. However, if one line amplifier dies or has greatly reduced gain, then the whole array (or a quadrant of the array) will cease operation and this will result in a drastic reduction in yield. We have solved this problem using a redundant amplifier architecture. These amplifiers operate with acceptable impedance match if one amplifier is turned on (mode 01 or 10), or if both amplifiers are turned on (mode 11) as shown in Fig. 3.8. The measured gains in modes 01 and 11 are 15 and 22 dB at 60 GHz, respectively.

The other main RF distribution block is the differential hybrid coupler with a loss of 0.9-1 dB at 60 GHz as shown in Fig. 3.9. 90° Hybrid coupler is a two-way symmetric structure and this property is used to form a divider block which will divide the incoming signal in left- and right-way regardless of which port the input is applied.

## 3.5 Channel Design

Each element contains a VGA (3-bits and 10 dB gain control), phase shifter (5-bits) and two-stage differential amplifier with a $P_{sat}$ of 3-4 dBm at 60 GHz. The phase shifter is based on Vector Modulator based current-summing topology. A coupled-line coupler with $\lambda/4$ microstrip transmission lines is used in IQ generation as shown in Fig. 3.10. The generated IQ signal is summed using vector summer with 5-bits resolution. The simulated and measured gain of the phase shifter is 0-2 dB at 60 GHz with an RMS gain and phase error of 1.5 dB and $7^o$, and agrees well with simulations.

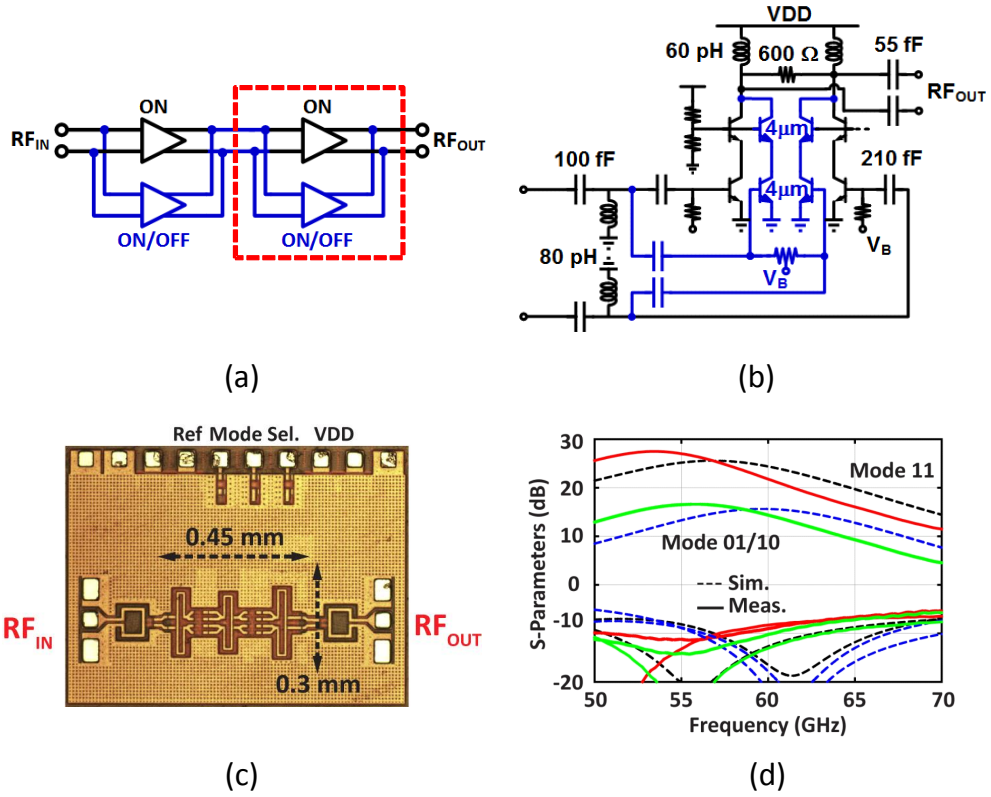



**Figure 3.8**: (a) Block diagram and (b) schematic of redundant line amplifiers.(c) Chip-photo of line amplifier and (d) simulated and measured results.

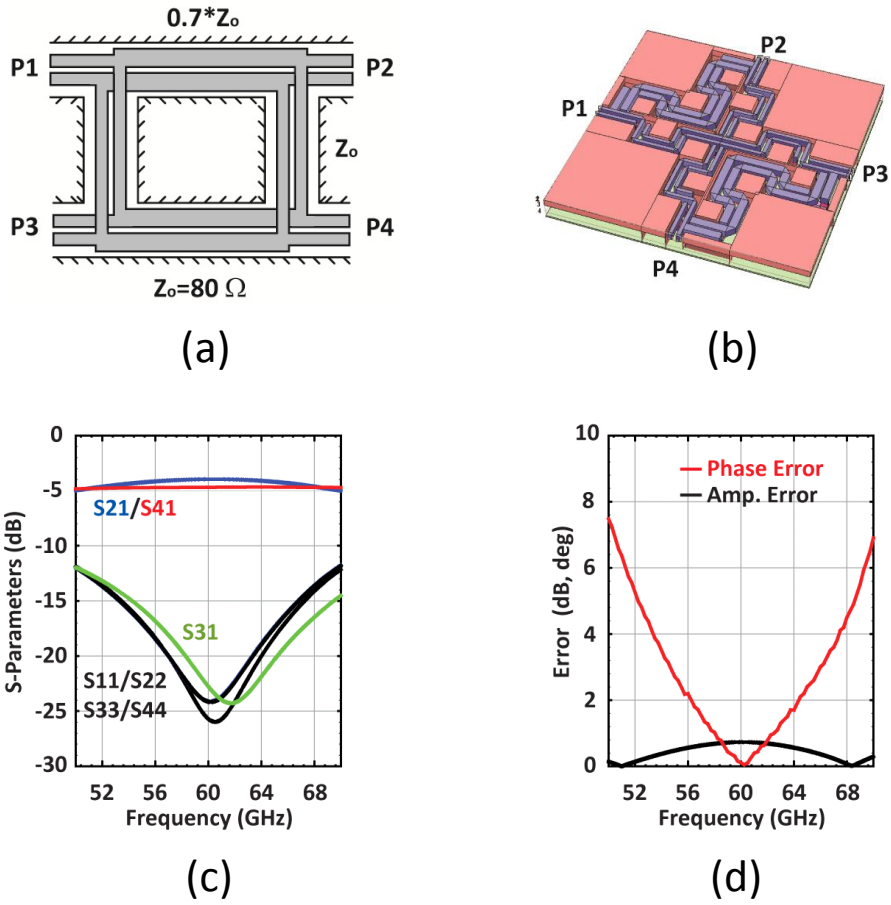



**Figure 3.9**: Hybrid coupler (a) schematic, (b) layout (c) simulation results and (d) phase and amplitude error between ports.

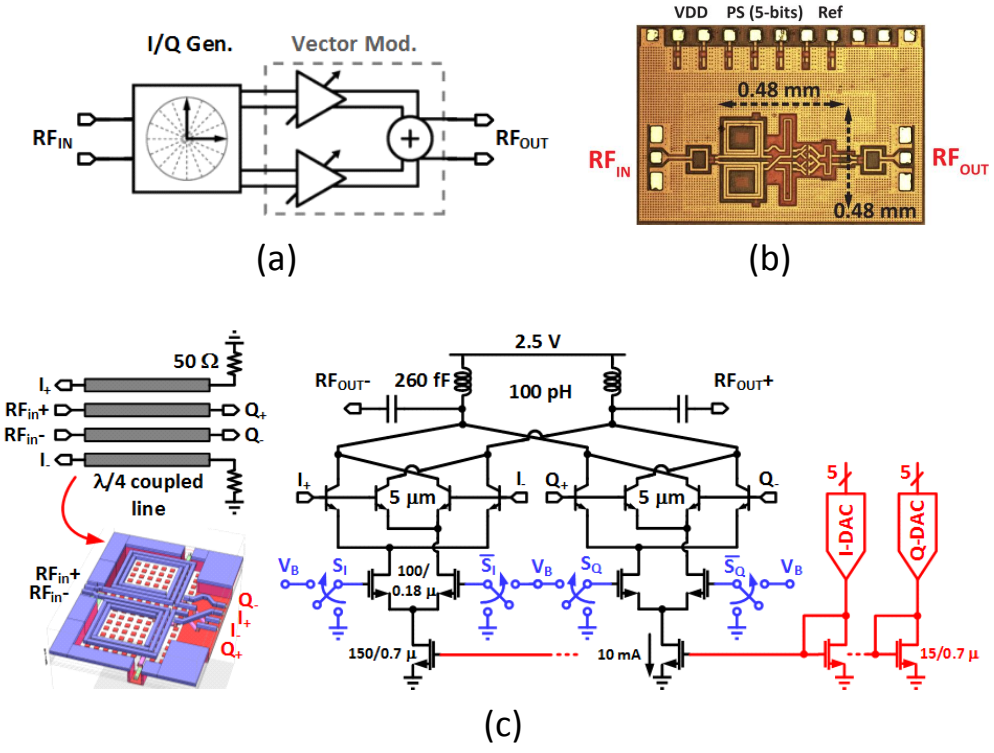



**Figure 3.10**: Phase shifter based (a) block diagram, (b) layout and (c) schematic details.

The second block in the channel is variable-gain amplifier and power amplifier (VGA and PA) blocks as shown in Fig. 3.11. The VGA and PA are based on both differential cascode topology. The VGA has a 3-bits gain control and the PA is optimized for moderate output power around 3 dBm. The measured gain of the VGA/PA phased-element is 22 dB at 60 GHz with a gain control of 9-10 dB.

The overall channel block diagram without antenna feed element is shown in Fig. 3.12. The channel has a gain of 22 dB in maximum gain state at 60 GHz and can be controlled 10 dB in gain. The overall phase control is 5-bits and has an RMS gain and phase error of 1.5 dB and $7^o$ which agree with simulations. The saturated output power of the channel is around 3 dBm. The total power consumption of the channel is 95 mW from 2.5 V power supply.

## 3.6 On-chip Antenna Design

A high efficiency antenna ($\varepsilon$ = 45% at 60 GHz) is placed on each element using a 100 $\mu$m quartz superstrate. The differential antenna feed lines are designed on top metal (Metal-6) in the process with a ground metal on Metal-4. The distance between the antenna feed lines and the ground is 5.6 $\mu$m which results in a low impedance as shown in Fig. 3.13, and therefore, the $\lambda/4$ microstrip transmission lines are used to transform the low impedance of the antenna to 100 $\Omega$ differential for the output PA matching in the channel. The simulated antenna input match has a 5 GHz bandwidth at 60.5 GHz center frequency with a -7 dB $S_11$ matching. The simulated peak gain and efficiency of the antenna is 3 dB and 50% as shown in Fig. 3.13.

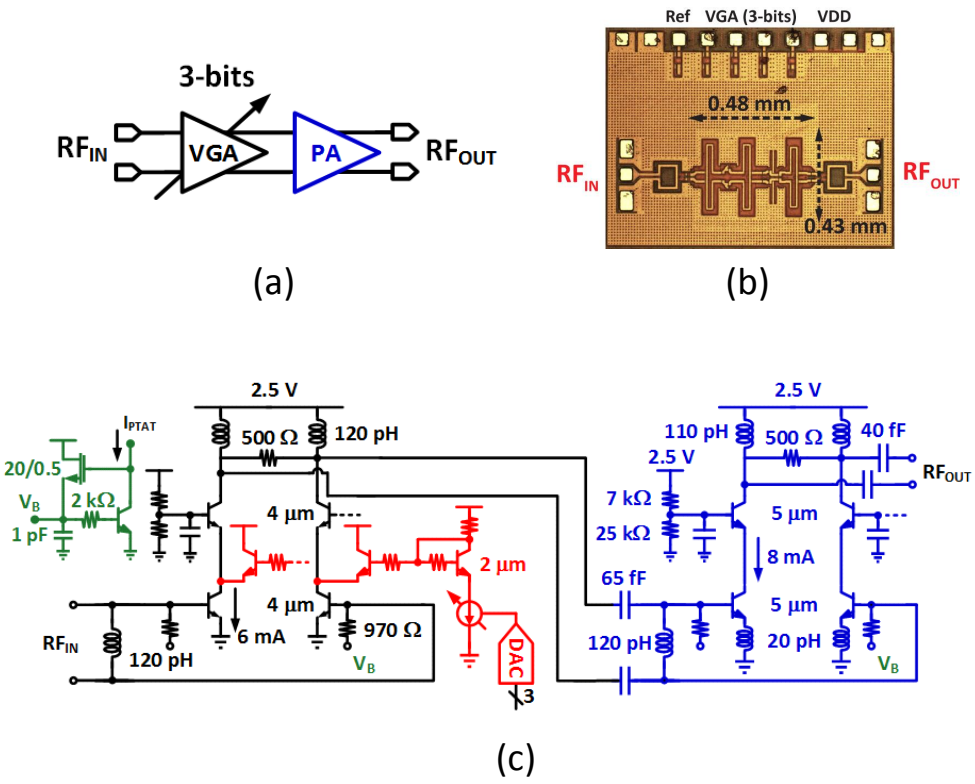



**Figure 3.11**: VGA and PA (a) block diagram, (b) layout and (c) schematic details.

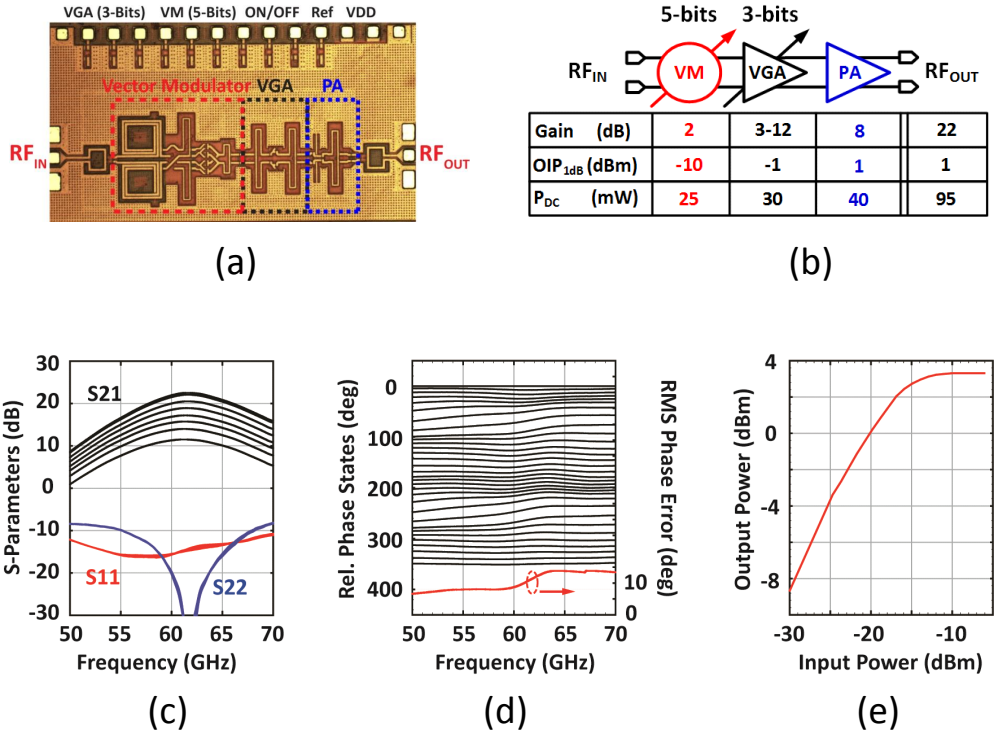



**Figure 3.12**: The Channel (a) layout, (b) block diagram, measured (c) S-parameters, (d) phase response and (e) output power.

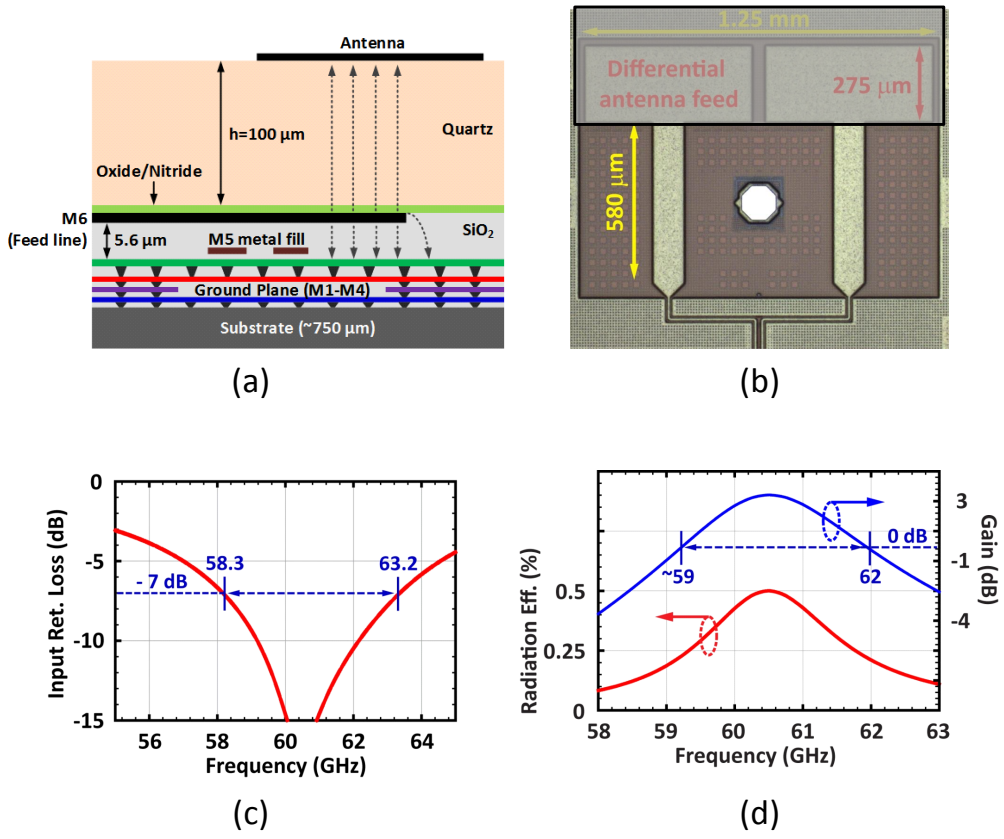



**Figure 3.13**: (a) Cross-section of the antenna, (b) layout, (c) simulated input matching and (d) simulated gain and efficiency.

## 3.7 Chip Micro-photographs

The microphotograph of the main radiating block, Block-A, is shown in Fig. 3.14. The Block-A consists of 16 channels with antenna feeds placed with $\lambda/4$ distance at 60 GHz. To monitor the process, three Process Control Modules (PCM) are located in this block. The area of the Block-A is 9.4 x 9.4 $mm^2$.

The microphoto of the 64-element array is shown in Fig. 3.15. The radiating area of the 64-element array is 20 x 20 $mm^2$ which is 8x$\lambda$ in both directions. The size of the designed array is compared with a USA Quarter. There are 45 dies in an 8" wafer and the yield of the dies is greater than 90%.

In addition to the 64-element array, the microphoto of the 256-element array is shown in Fig. 3.16. As explained before, the mapping of the sub-reticle stitching technique is highlighted in Fig. 3.16(a). 16-Block-As are used to form 256-element array in addition to many distribution sub-blocks. The total area of the phased array is 40x40 $mm^2$, and the entire chip is 41.2x42 $mm^2$ (1740 $mm^2$) which is the largest chip ever designed working at RF.

## 3.8 EIRP and Pattern Measurements

The wafer-scale phased array is placed on an FR-4 board and bonded for VDD, GND and SPI control as shown in Fig. 3.17. This is then placed on a probe station and a GSG probe is used from the West side of the chip to feed the array. The array is biased at 2.5 V and consumes 3.4 A for a total power consumption of 8.5 W. A 100 $\mu$m thick quartz wafer is attached to the top of the silicon chip and the dipole antennas are defined on the quartz wafer (the silicon chip contains the antenna feed on the top layer, see Fig. 3.13 for more details). SPI is used to control all aspects of the array, from element-level control (phase and gain) to setting the different reference currents for each quadrants for

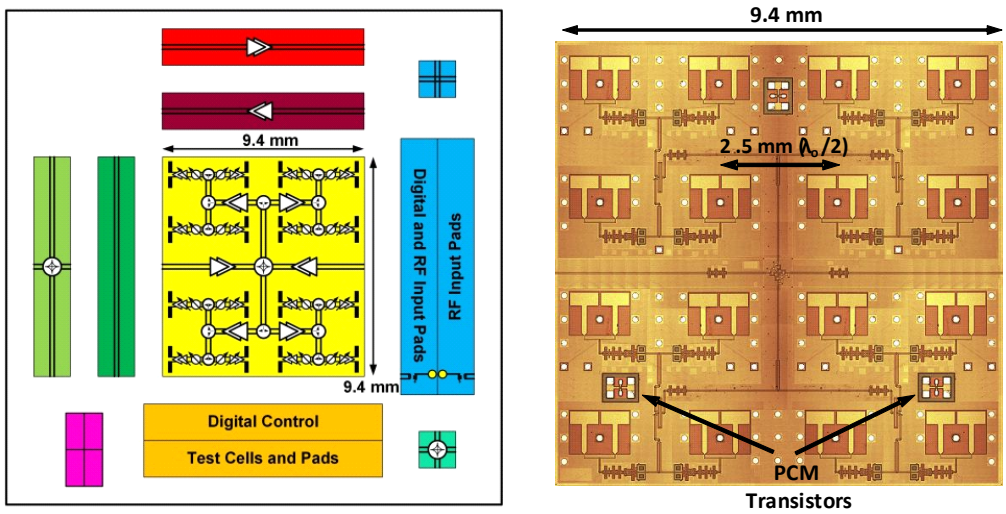



**Figure 3.14**: (a) Sub-blocks in a reticle and (b) the microphoto of the Block-A.

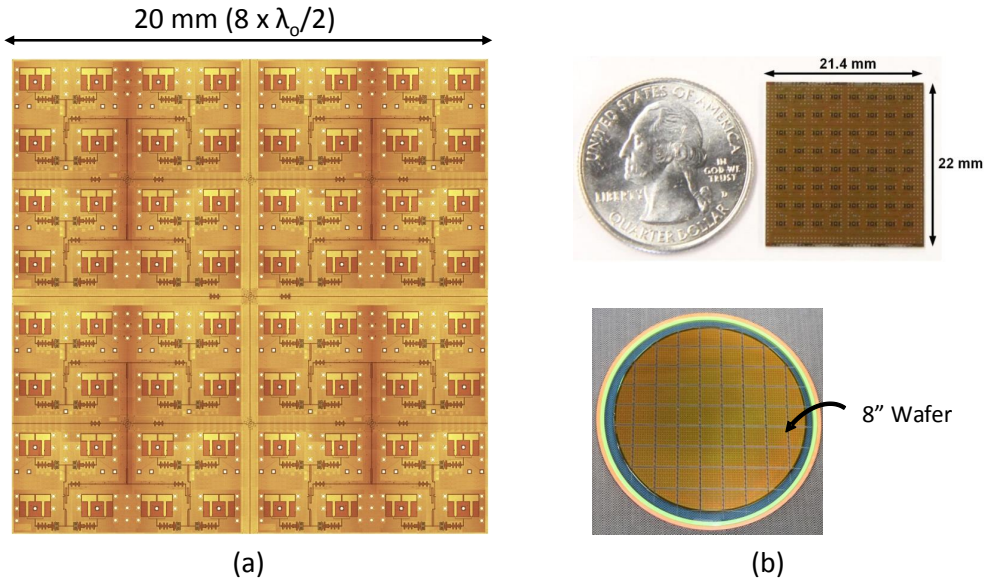



**Figure 3.15**: (a) Microphoto of the 64-element array and (b) comparison with a USA Quarter and dies in a 8" wafer.

equal gain and power per quadrant. A microcontroller is used to control the array for scanning and different gain modes.

The 8x8 and 16x16 arrays are probed with a 67 GHz GSG probe for the RF input signal and the pattern/EIRP measurement setup is detailed in Fig. 3.17. A 1 kHz square-wave modulated RF signal is pumped using Agilent 8257D Signal generator and SR830 lock-in amplifier is used to detect the modulated signal and monitored for E-/H-plane scanning and different output power levels. The measured patterns were taken using a WR-15 open-ended waveguide located at 25 and 65 cm from the wafer (far-field condition = $2D^2/\lambda$) for 64- and 256-element arrays, respectively as shown in Fig. 3.17.

First, the pattern measurements of the 64- and 256-element arrays are presented in Fig. 3.18. A 3-dB beamwidth of 12-13$^o$ is obtained in both E- and H-planes for 64-element array and the measured patterns agrees well with the simulations. Similarly, a 3-dB beamwidth of 6-6.5$^o$ is obtained in both planes for 256-element array and again measured results match with the simulations well.

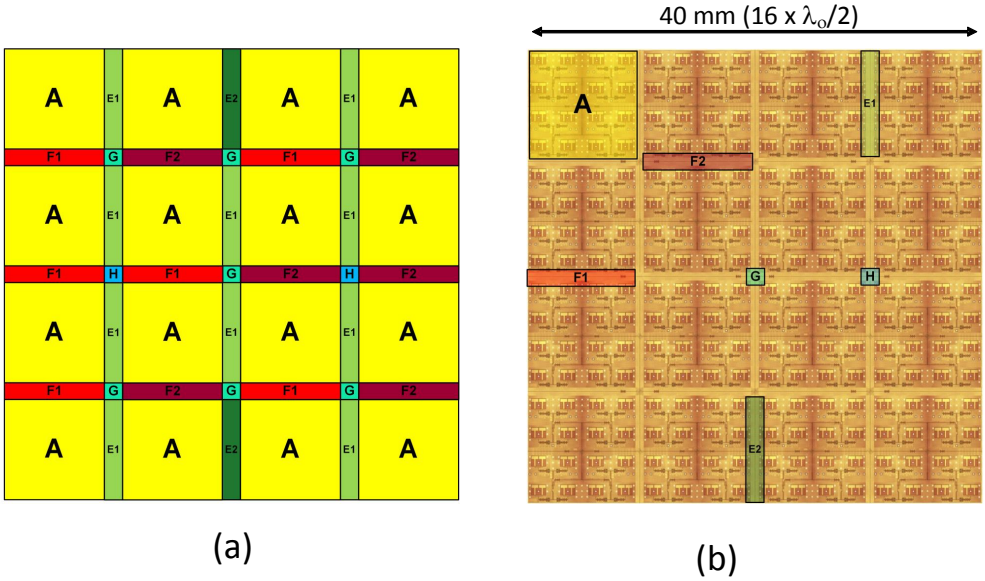
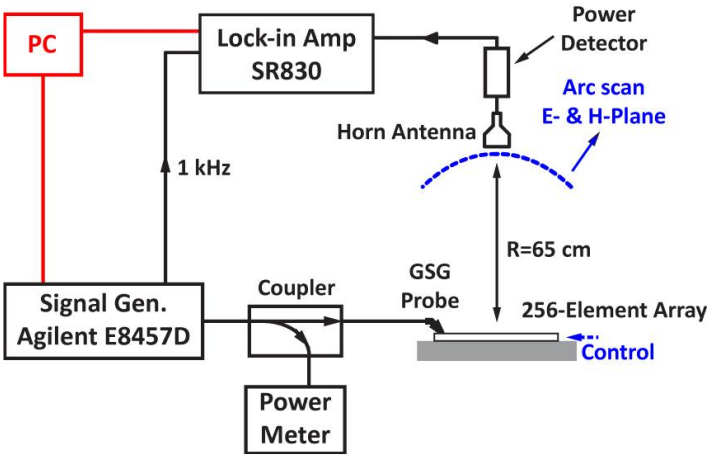
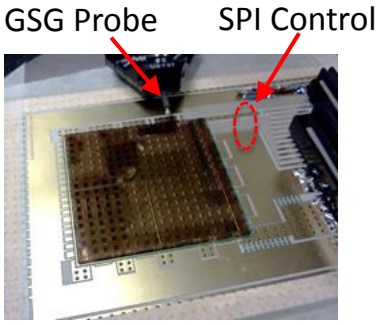



**Figure 3.16**: (a) Mapping and (b) Microphoto of the 256-element array.




(a)




(b)

**Figure 3.17**: (a) Pattern and EIRP measurement setup and (b) Photo of the 8x8 array on FR-4 board.

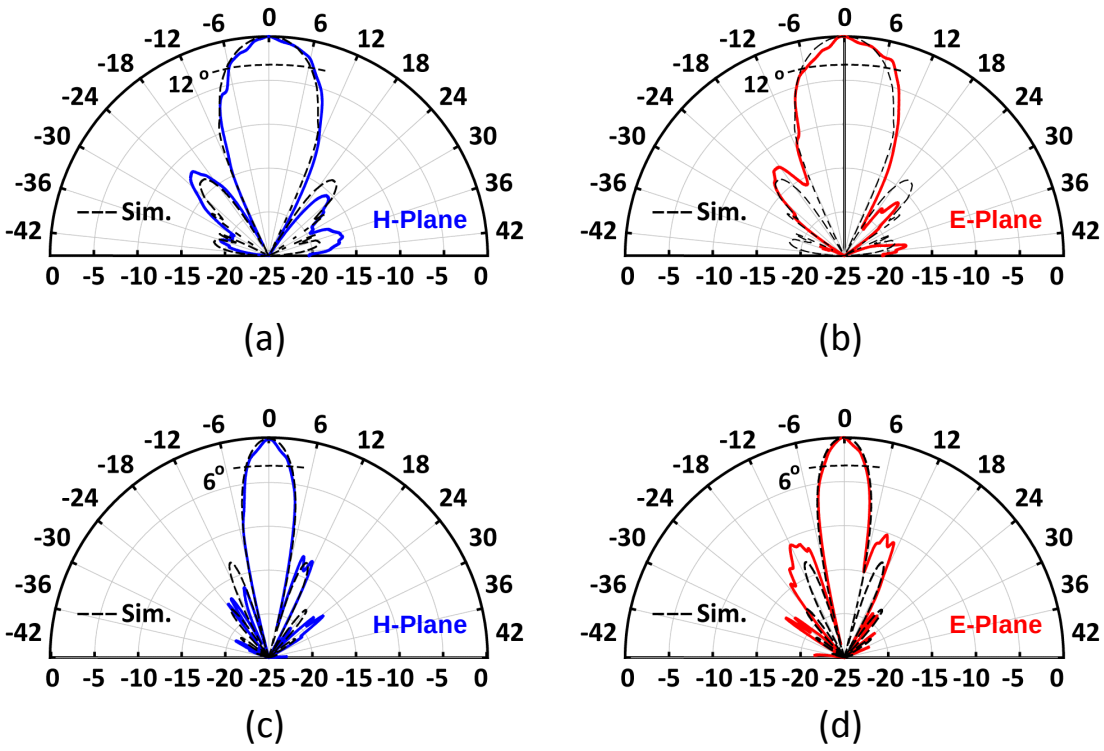



**Figure 3.18**: Measured and simulated patterns of the 64-element array for (a) H-plane, b) E-planes, 256-element array for (c) H-plane and (d) E-plane.

Both 64-element and 256-element arrays scan to +/-55$^o$ in both E and H-planes with near ideal patterns and a cross- polarization level <-25 dB (Fig. 3.19).

The measured EIRP is 38 dBm at 66 GHz which compares well with the expected EIRP of 41 dBm at 60 GHz ( Fig. 3.20). The expected EIRP is: 3.5 dBm ($P_{out}$/element) - 3.5 dB (antenna efficiency) + 23 dB (directivity) + 18 dB (elements). We believe that a small air-gap (10 $\mu$m) exists between the silicon and quartz wafers due to residues on the silicon wafer which has shifted the antenna frequency to 66 GHz and reduced the antenna efficiency and PA output power. This issue was solved by replacing the 1.25 mm Quartz antenna with a 1.34 mm long antenna to shift the frequency down to 61 GHz. Note that no amplitude and phase calibration is done on the array (using a near-field probe) except for setting the quadrant currents. This shows the exceptional repeatability in wafer-scale designs.

To study the uniformity of the 64-element array, radiating elements (channels) are activated one-by-one and the total radiated power from the array is measured. Ideally, the output power should increase with $N^2$ and the measured EIRP is very close to the ideal combination as shown in Fig. 3.21. The combining loss in the array is around 0.6 dB and mainly due to the process variation over the channels and non-uniformity in the Quartz antenna layer. As shown in Fig. 3.22, the 64-element array can be divided in four quadrants (Quad A, B, C and D) each consists of 4x4 array (Block-A). The uniformity of the 64-element array from four different quadrants are also presented in Fig. 3.21 and the radiated power from quadrants are very close to each other in +/- 0.5 dB range.

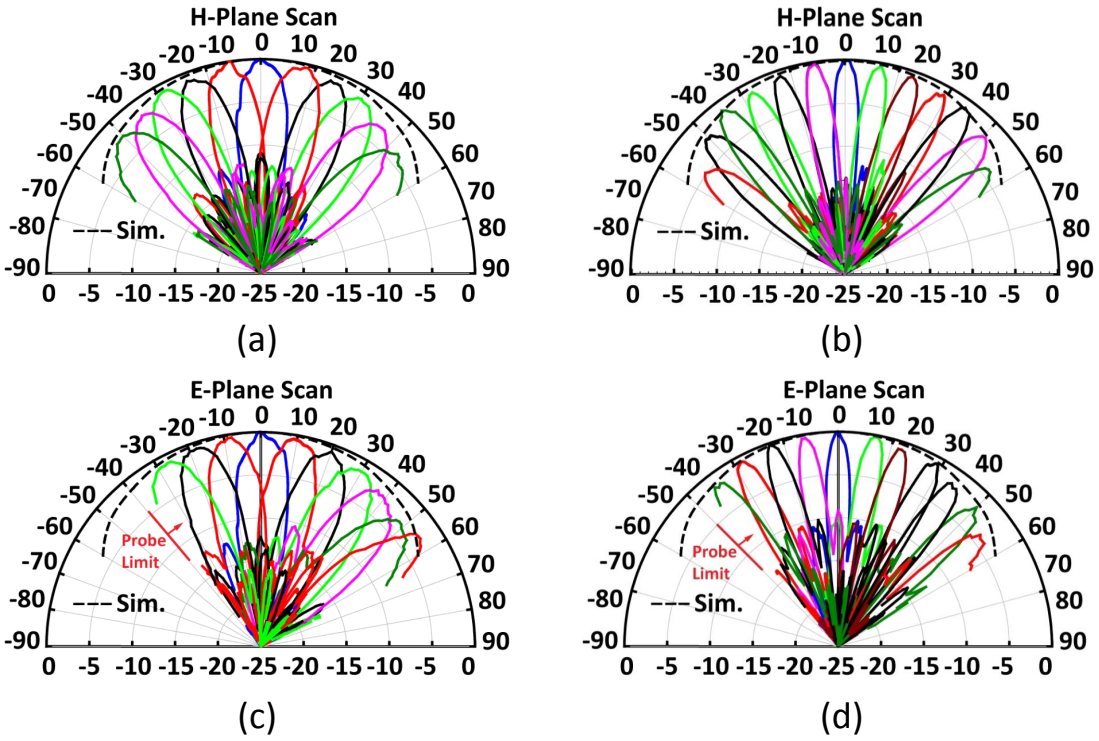



**Figure 3.19**: Measured and simulated scanned patterns of the 64-element array for (a) H-plane, b) E-planes, 256-element array for (c) H-plane and (d) E-plane.

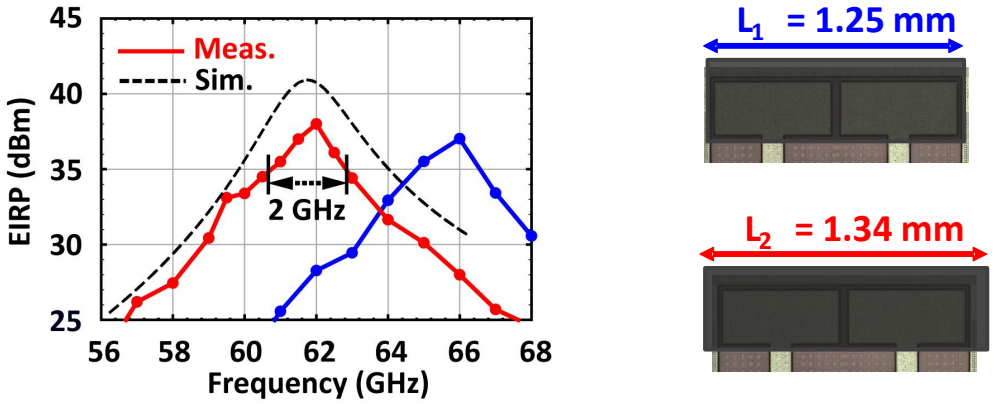



**Figure 3.20**: Measured and simulated EIRP for the 64-element array with different antenna layers.

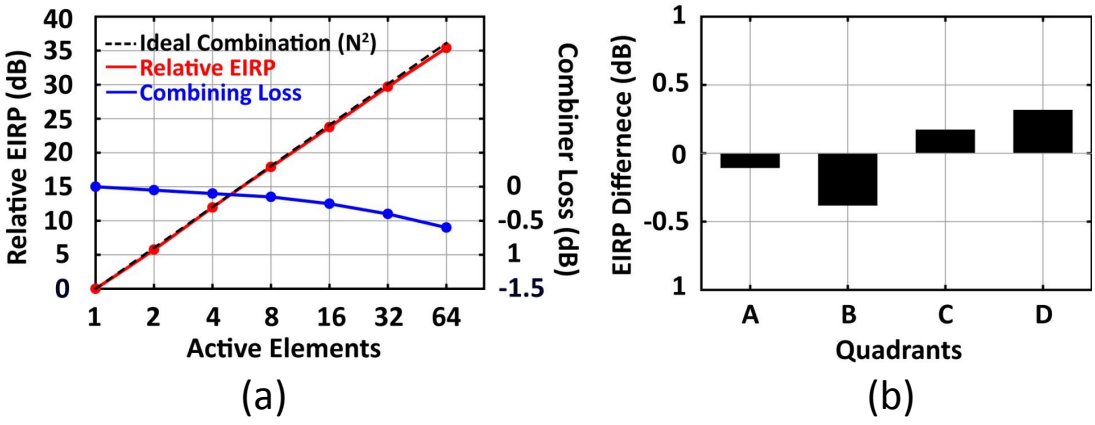



**Figure 3.21**: (a) EIRP vs active element and (b) EIRP difference for four different quadrants in the 64-element phased arary.

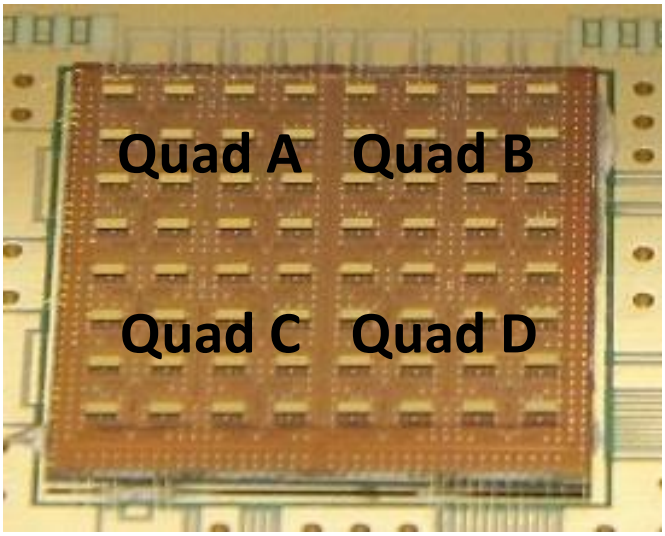



**Figure 3.22**: Quadrants in the 64-element array.

For the 256-element array, four different 100 $\mu$m-thick quartz wafers are attached to the top of the wafer-scale phased array, each on an 8x8 quarter. The differential dipole antennas are defined on the quartz wafer (the silicon chip contains the antenna feed on the top M6 layer) as shown in [7, 8]. A Serial-Parallel-Interface (SPI) is used to control all aspects of the array, from element-level control (phase and gain) to setting the different reference currents for each quadrants for equal gain and power per quadrant. Also, note that some quadrants have an inherent +/- 90$^o$ phase shift due to the use of hybrid couplers, and this is compensated by adding (or subtracting) a 90$^o$ phase shift for the entire quadrant using SPI control.

The simulated EIRP, $P_T G_T$= 52.5 dBm at 25$^o$C and is derived as $P_T$= 3 dBm ($P_{out}$/element) + 24 dB (256 elements)= 27 dBm, and $G_T$= 29 dB (directivity) - 3.5 dB (antenna efficiency)= 25.5 dB. However, it drops to 49.5 dB at 95$^o$C, which is the operational temperature of the array. The measured EIRP in the far-field range is 45 dBm with a 3-dB bandwidth of 6 GHz as shown in Fig. 3.23. The discrepancy is due

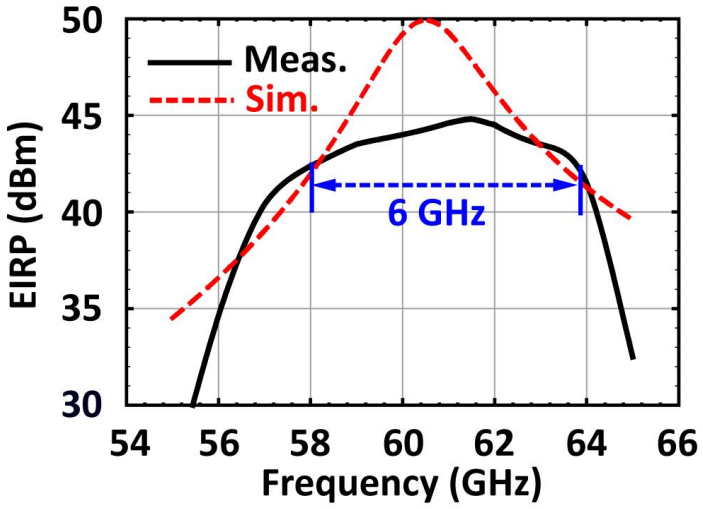



**Figure 3.23**: Measured and simulated EIRP for 256-element array.

to several factors and include a) 15-20 $\mu$m air-gap between the quartz substrate which reduces the antenna radiation efficiency to 30% (5 dB loss instead of 3.5 dB loss), b) soft compression of the line-amplifier chain in the 256-element array causing a 1.5 dB drop in $P_{sat}$ at the element level, and c) power variation between the different quadrants when measured independently causing a 0.5-1 dB drop in the overall EIRP. The soft compression is determined by measuring each 8x8 quadrant alone and finding a 1.5 dB higher EIRP per element than the 256-element array (when normalized to the number of elements). We believe that with better attachment of the quartz substrates to the silicon wafer and a better thermal heat sink for the 256-element chip, it is possible to obtain an EIRP $>$ 50 dBm from this array.

Additionally, there are four different Quartz antennas used for 256-element array due to its size of 40x40 $mm^2$. The usage of four different Quartz antennas as shown in Fig. 3.24 result shifts in the peak frequency that each quadrant operates. Therefore, the total radiated power vs frequency for 256-element widens due to different peaking of each quadrants. The pattern of each quadrant (Quad 1,2,3 and 4) is measured and similar

**Table 3.2**: Performance summary of the 64- and 256-element phased arrays

| | **8x8 Array** | **16x16 Array** |
|---|---|---|
| Antenna Array Directivity (dB) | 23 | 29 |
| Antenna Array Gain (dB) | 19 | 25 |
| Max. Measured EIRP (dBm) | 38 | 45 |
| Measured Scan Angle ($^o$) | $\pm$55 | $\pm$55 |
| 3-dB Beamwidth ($^o$) | 12 | 65 |
| Power Cons. (mW) | 3.4 A @ 2.5 V | 14 A @ 2.5 V |

results are observed from each quadrant. However, due to different air-spacing between each Quartz antenna, the peak operating frequency of each quadrant different from other as shown in Fig. 3.24.

The overall performance of the arrays are tabulated in Table. 3.2.

## 3.9 Conclusion

In this chapter, system and circuit level details of the 64- and 256-element phased arrays are discussed with simulation and measurement results. Many redundancy techniques are used to improve the yield of the chips up to 90%. The RF distribution elements including line amplifiers, 90$\circ$ Hybrid coupler and digital control circuitries are discussed in detail. The channel design (Vector Modulator, Variable Gain Amplifier and Power Amplifier) and antenna design are provided with measurement results. Finally, EIRP and electronic scanning measurements are shown that the 64-element and 256-element phased arrays can achieve an EIRP of 38 and 45 dBm, respectively.

## 3.10 Acknowledgements

This work is supported by the DARPA DAHI program under a subcontract from Jazz Semiconductor, Inc., Newport Beach, CA.

Chapter 3 is mostly a reprint of the materials from

• S. Zihir, O.D. Gurbuz, A. Karroy, S. Raman, G.M. Rebeiz, ”A 60 GHz Single-Chip 256-Element Wafer-Scale Phased Array with EIRP of 45 dBm Using Sub-Reticle Stitching,” in *Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2015.

• S. Zihir, O.D. Gurbuz, A. Karroy, S. Raman, G.M. Rebeiz, ”A 60 GHz 64-element Wafer-Scale Phased-Array with Full-Reticle Design,” in *Microwave Symposium (IMS), 2015 IEEE MTT-S International*, vol., no., pp.1-3, 17-22 May 2015.

Also mostly reprint of the materials as will be submitted to IEEE Transactions on Microwave Theory and Techniques, 2016. Samet Zihir, Ozan D. Gurbuz, Arjun Karroy, Sanjay Raman, Gabriel M. Rebeiz.

The dissertation author is the primary author of this material.

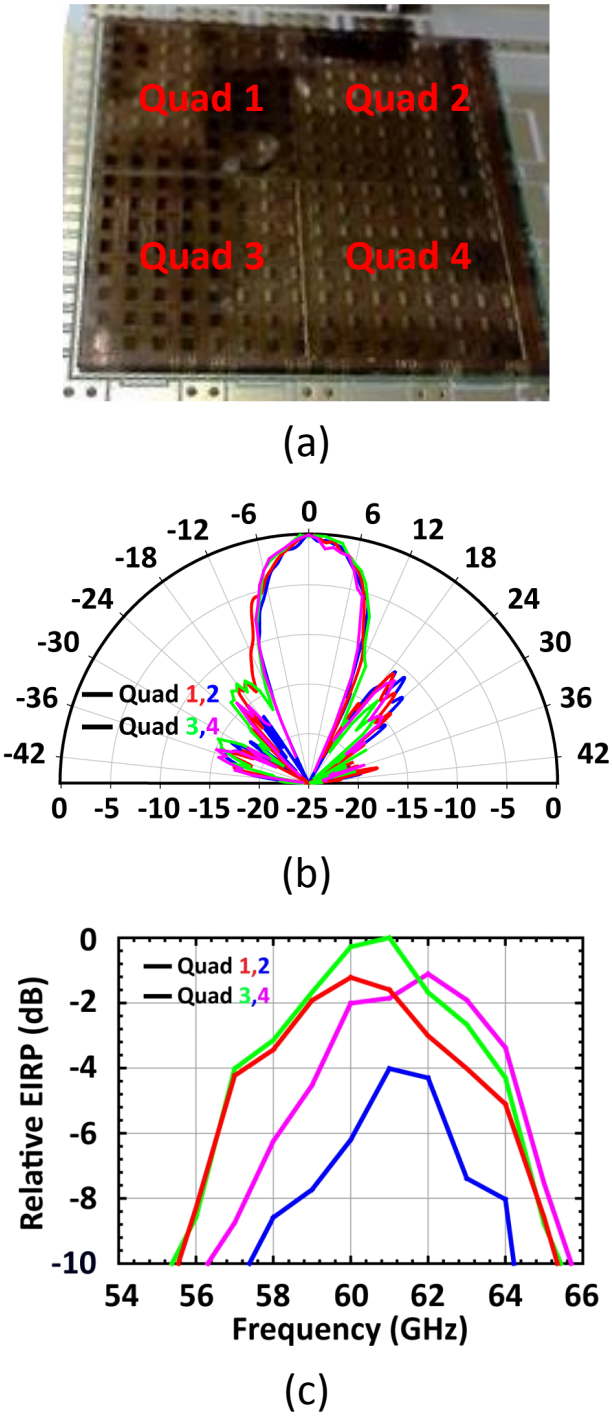



**Figure 3.24**: (a) Pattern and (b) EIRP measurements of each quadrant separately.

# Chapter 4

# 60 GHz Communications Link Measurements with 64-Element Phased Array Transmitter

## 4.1 Introduction

In this section, 60 GHz communications link measurements will be presented in detail. The measurements are done with different link distances, modulation schemes and at different locations. High order modulations such as 16-, 32-, and 64-QAM are performed in 40 cm and 4 m distances. For longer distances such as 30 m and 90 m, wideband operation with lower modulation schemes such as QPSK and 16-QAM are chosen to achieve larger than 1 GBps link budget. Additionally, real-time HD video transfer is performed at 40 cm to show that the designed 64-element phased array transmitter can be used for WirelessHD applications with $\pm 45^{\circ}$ scanning angles.

## 4.2 Measurement Setup

To demonstrate the performance of the 64-element transmitter array (8x8 array), a 60 GHz link with 0.4, 4, 30 and 90 m is shown in this chapter. The measurement setup is presented in Fig. 4.1. The baseband signals BB1 and BB2 with QPSK, 16-/64-/256-QAM modulation schemes are generated with Keysight M8190A Arbitrary Waveform Generator (AWG). The generated baseband signals are feed to Keysight E8267D Signal Generator to be modulated and up-converted to 6 GHz IF. The modulated 6 GHz IF signal is upconverted to 58 GHz using a wideband Marki Microwave Mixer (7-65 GHz). The LO for the up-conversion is selected to be 52 GHz and the up-converted image at 46 GHz is rejected using 55-65 GHz band-pass filter (BPF) before the driver PA. A 55-65 GHz Quinstar PA is used to amplify the modulated RF signal centered at 58 GHz. The amplified signal is then fed to the input of the 64-element TX array. The saturated EIRP at the output of the PA is around 36 dBm and the 64-element array will be used in the back-off mode to achieve better performance in N-QAM modulated signals.

In the receiver chain, the received signal is captured using WR-15 waveguide horn antenna with a 20 dB gain at 60 GHz and amplified using a 33 dB 55-65 GHz Quinstar Low Noise Amplifier (LNA) with 3.5-4.5 dB NF. The amplified RF signal is down-converted with a wideband Marki Microwave Mixer (7-65 GHz) to again 6 GHz with the 52 GHz LO signal generated from a Keysight E8267D Signal Generator. A MiniCircuits 3.4-0 GHz BPF is used to limit the noise bandwidth and relax the IF amplifiers before the sampling oscilloscope. The modulated IF signal is amplified using a 2-8 GHz Phase One Microwave LNA and connected to Keysight DSO804A Real-time Oscilloscope with 8 GHz BW.

The calculated SNR values for different link distances are provided in Table 4.1. The transmitted EIRP of the 64-element phased array is taken to be 32 dBm in this

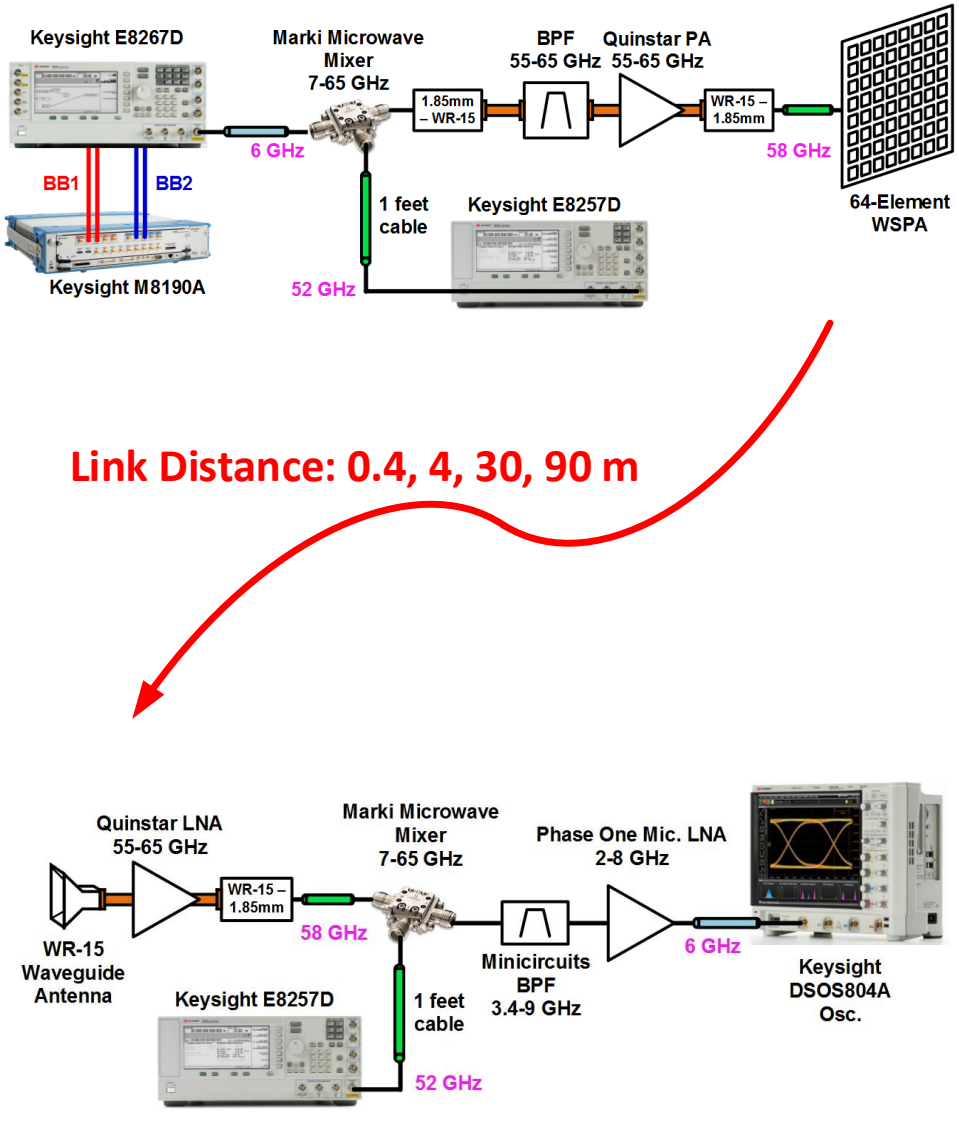



**Figure 4.1**: Measurement setup for the 60 GHz communications link.

**Table 4.1**: Calculated input-referred noise level in the RX chain

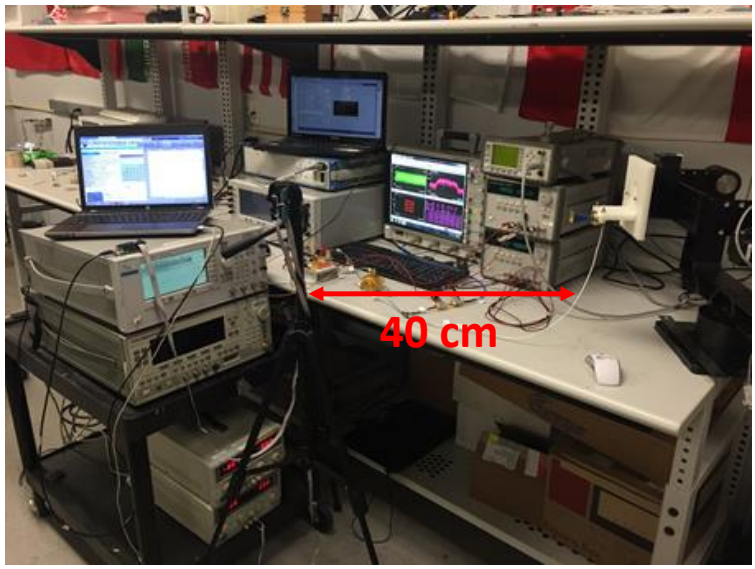
| Link Distance | Received Signal Power (dBm) | Input Ref. Noise Fig. (dB) | System BW (GHz) | SNR (dB) |
|---|---|---|---|---|
| 4 | -48 | 5 6 | 2 | 47 |
| 100 | -76 | 5 6 | 2 | 19.8 |

calculations due to 3-4 dB back-off operation for better Error Vector Magnitude (EVM) performance. The Quinstar LNA has a NF of 5-6 dB and a gain of 33 dB at 60 GHz, therefore the overall NF of the receiver chain is dominated by the LNA. According to the calculations, the TX-RX system can achieve 20 dB SNR at 100 m distance.

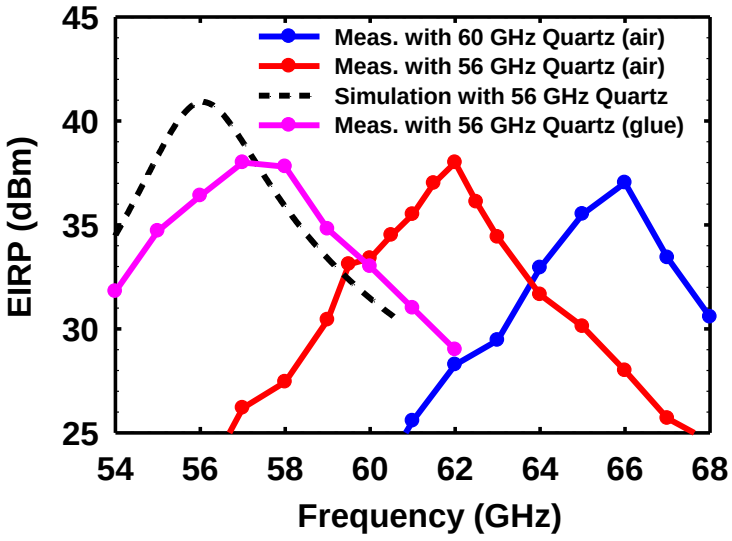
## 4.3 Link Measurements - 40 cm

The photo of the measurement setup is shown in Fig. 4.2. With a link distance of 40 cm, the associated diagram of the measurement setup is also provided in Fig. 4.1. First the radiated total EIRP is measured from the 64-element phased array and given in Fig. 4.2. The measured peak EIRP is around 36 dBm and has shifted to 57 GHz with the new quartz antennas due to the glue used for attachment. In previous measurements, the quartz antennas are not attached without glue and therefore, the frequency of operation was around 61 GHz. This shows that the 64-element phased array can work in a wide range of frequencies and the setup is mostly limited by the quartz antennas. For this reason, all the measurements in this chapter will be performed at 57 GHz center with $\pm$2 GHz frequency range. Also the modulation BW of the system will be limited by 2-3 GHz due to Quartz antenna.

First, the measurement results for the 40 cm communications link will be presented with different modulation schemes. A QPSK modulated signal is fed to the 64-element array and the de-modulated constellation is shown in Fig. 4.3. We can achieve a 1.5 GBps (0.75 GSps) successful link with an EVM of 11% and a SNR of 19




(a)




(b)

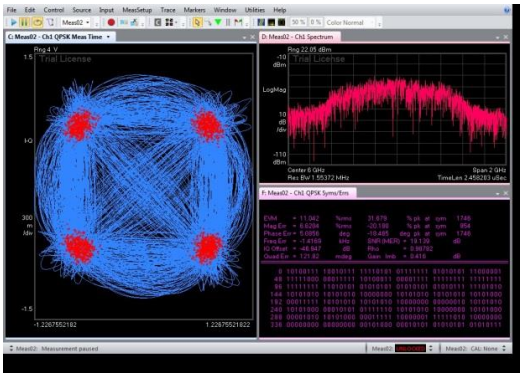
**Figure 4.2**: Photo of the 60 GHz measurement setup.

dB. In addition, 16-QAM at 2 GBps (0.5 GSps) with an EVM of 7.7% and 64-QAM at 1.5 GBps (0.25 GSps) with an EVM of 4.2% are achieved in this link. The calculations indicate that we can achieve more than 40 dB SNR (as shown in Table 4.1), however IQ phase and amplitude imbalance cause the measured SNR to be lower than 40 dB. For this reason, the THRU measurements are performed using horn antenna instead of the 64-element transmitter array. In this THRU measurements, it is observed that the minimum achieved EVM is around 7-8%. This is due to several non-linearities and non-uniformities in the measurement setup including the PA, LNA and mixers. To achieve better results, one has to perform pre-distortion techniques like Digital Pre-Distortion (DPD). For this work, the main challenge is to show a successful link rather than achieving the minimum EVM possible.

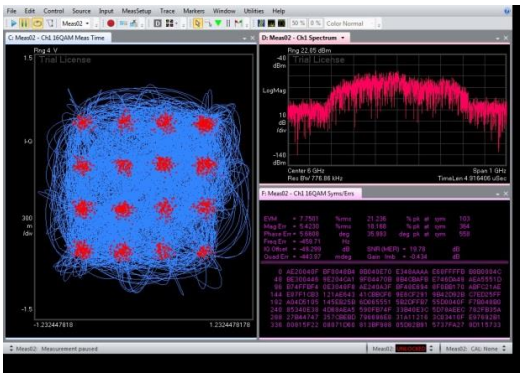
## 4.4 Link Measurements - 4 m

The same measurement is repeated at a 4 m distance. Again the same measurement block diagram is used as detailed in Fig. 4.1. The measurement is performed in the lab as shown in Fig. 4.4. In this measurement, electronic scanning is also applied to the 64-element phased array transmitter to show that the 60-GHz link can be kept successful over a wide scan angle. For this, the 64-element transmitter is scanned +30° and -45° as shown in Fig. 4.4. Higher modulation schemes are performed and the measurement results are shown in Fig. 4.8. The SNR budget is still high enough to perform high-order modulation schemes, and it is shown that successful links were achieved with 16-QAM modulation with 2 GBps (0.5 GSps) at an EVM of 9.7%, 32-QAM modulation with 1.5 GBps (0.3 GSps) at an EVM of 7.8%, and 64-QAM modulation with 0.6 GBps (0.1 GSps) at an EVM of 4.2%. As shown in these measurements, the designed 64-element transmitter can handle the 60 GHz link up to 2 GBps without degrading the link up to

QPSK (1.5 Gbps)



16QAM (2 Gbps)



64QAM (1.5 Gbps)

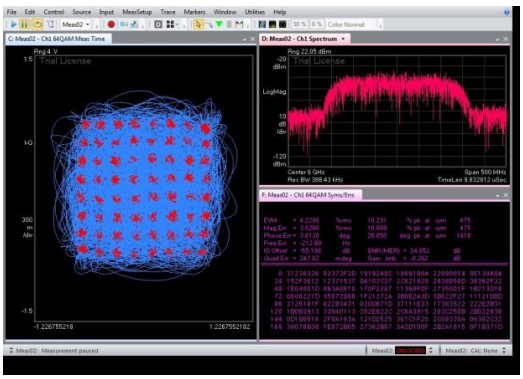


**Figure 4.3**: Measured constellation for QPSK, 16-QAM and 64-QAM at 56 GHz center frequency, with a range of 40 cm.

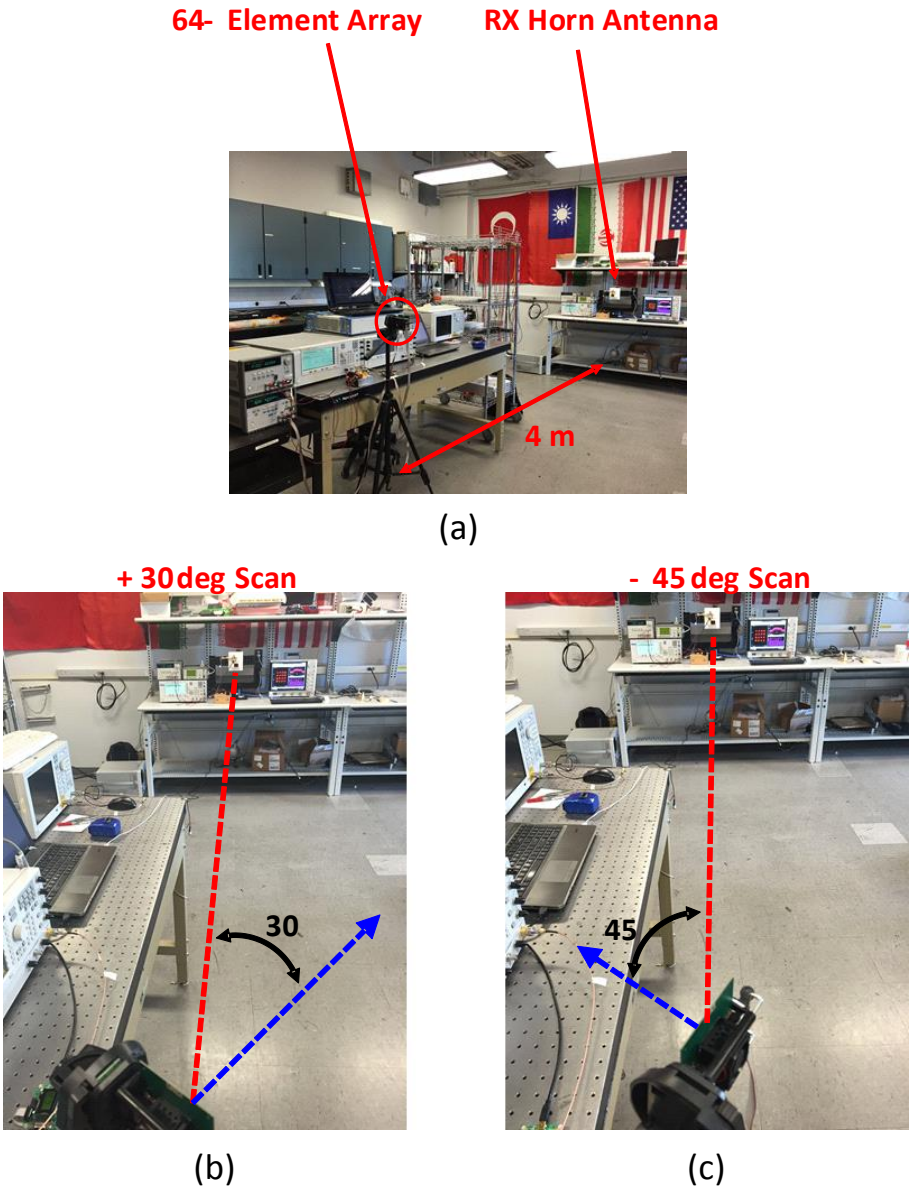
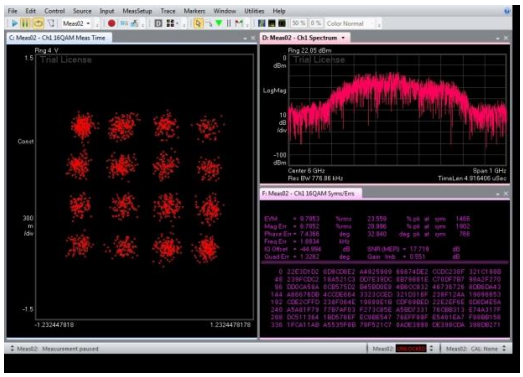



**Figure 4.4**: Photo of the 60 GHZ measurement setup for 4 m.

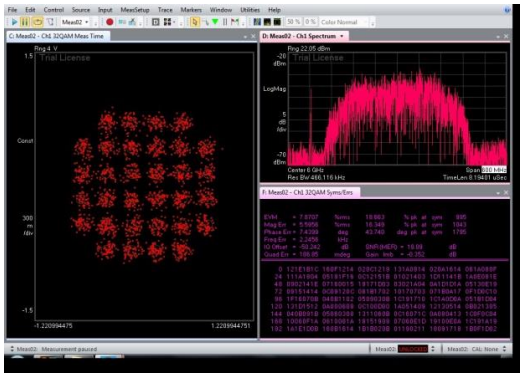
±45° scanning in both E- nd H-planes.

Finally, the modulation measurements are performed at different output powers. In this way, we can characterize the system EVM vs. output power. Because the QPSK modulation scheme has a constant envelope, the transmitter can be ideally used in the maximum saturated output power without degrading the performance. However, QAM

16QAM (2 Gbps)



32 QAM (1.5 Gbps)



64 QAM (0.6 Gbps)

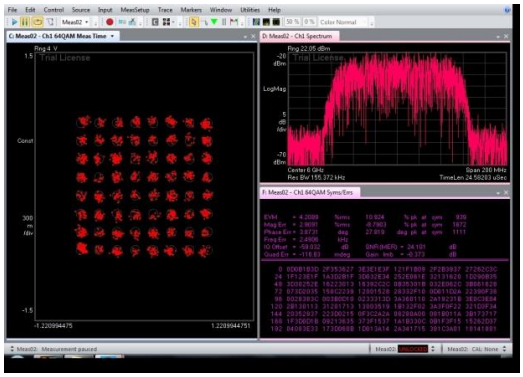


**Figure 4.5**: Measured constellation for QPSK, 16-QAM and 64-QAM at 56 GHz center frequency at 4 m.

modulation schemes require amplitude modulation and therefore, the transmitter should be operated in the back-off mode to achieve best performance. Similar analysis is performed in the 64-element transmitter, and as shown in Fig. 4.6, the 64-element phased array should be used around 4-5 dB back-off in QPSK modulation signals and in 9-10 dB back-off for 16-QAM modulations. For both cases, minimum achieved EVM is around 13% which is mainly dominated by channel imperfections rather than the SNR.

## 4.5 Link Measurements - 30 m

After successfully achieving 60 GHz link at 4 m, the next step was to analyze the channel with longer distances such as 30 m and 90 m. For this reason, first a 30 m distance link is set in the $6^{th}$ floor corridor in Jacobs Hall, UCSD, CA. The RX and TX benches are located at two far ends of the corridor and the 3 sides of the link are surrounded by walls and floor as shown in Fig. 4.7. However in the measurement setup, we were faced with many reflections from the sidewalls and the floor. Even though the 2 GBps QPSK link with an EVM of 10% could be achieved at 4 m distance while having enough SNR, the measurement results are lower than expected at 30 m. As shown in Fig. 4.8, 16-QAM modulation with 0.4 GBps (0.1 GSps) at EVM of 12.3%, QPSK modulation with 1 GBps (0.5 GSps) at EVM of 24.2% and again QPSK modulation with 2 GBps (1 GSps) at EVM of 30% were the best result achieved at 57 GHz. These are higher than the simulated results and these are attributed to mainly reflections coming from walls and floor.

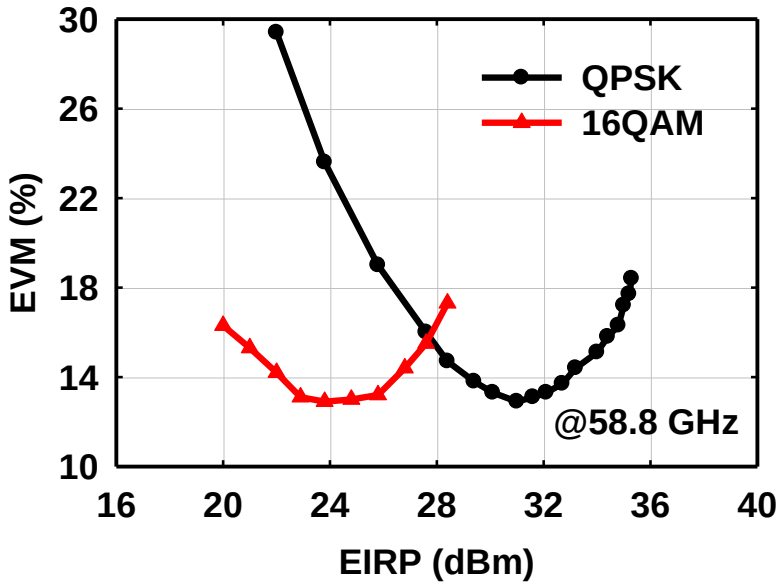



**Figure 4.6**: EVM vs output power of the 64-element transmitter for QPSK and 16-QAM modulations.

## 4.6 Link Measurements - 90-100 m

It was observed that the lick is limited with the environment therefore a new link setup is created such that the reflections will be minor and will not affect the channel as in 30 m link. For this reason, a 90-100 m link is created from $6^{th}$ floor balcony of Jacobs Hall, UCSD and to the end of the parking lot behind the building. The bird-eye distance of 80-90 m is shown in Fig. 4.9. The elevation of the $6^{th}$ floor from the parking lot is around 25-30 m and in total 90-100 m link is calculated for this measurement. The transmitter (64-element phased array transmitter) is placed on the 6th floor balcony and the RX bench is located in the parking lot as shown in Fig. 4.10. For calibration and THRU measurement purpose, a WR-15 horn antenna is used (Fig. 4.10). For this measurment, the measurement block diagram is again kept same as given in Fig. 4.1.

In this measurement environment, there are few multi-paths, and therefore, it is expected to get better results compared to the 30 m link in the corridor. A QPSK modulation with 1 GBps (0.5 GSps) at EVM of 16.6% and again QPSK modulation with 1.5 GBps (0.75 GSps) at EVM of 21.2% are achieved at 58 GHz in this setup as shown in Fig. 4.11 and in Fig. 4.12. These EVM results are below 35% in a QPSK mode therefore the link can be regarded as successful.

Similar measurements are performed with scanning to $\pm 45^{\circ}$ while keeping the output power and link distance same. The measurement photos and measurement results are shown in Fig. 4.13 and in Fig. 4.14.

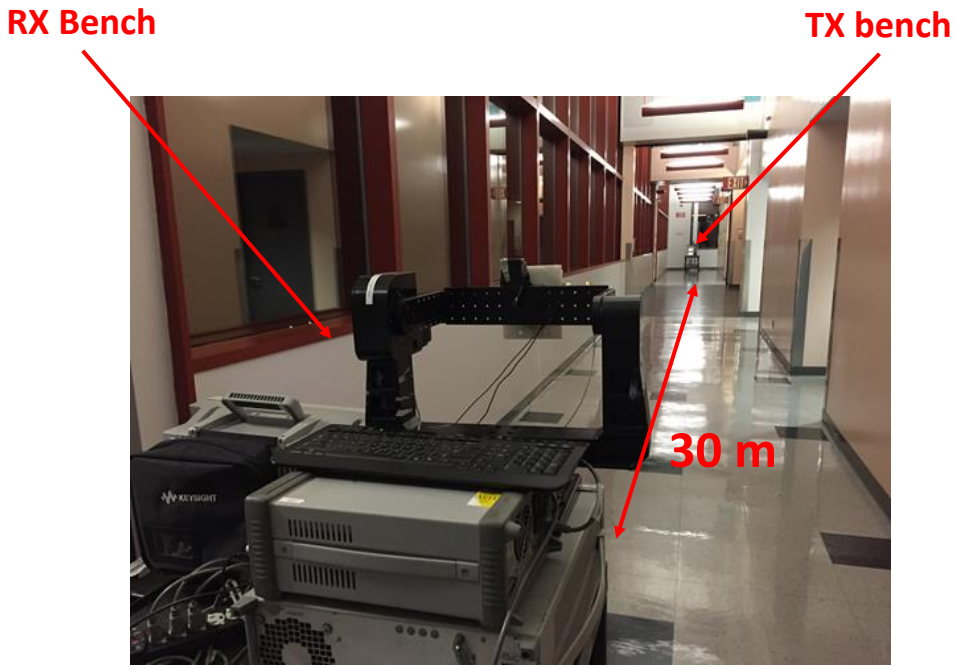
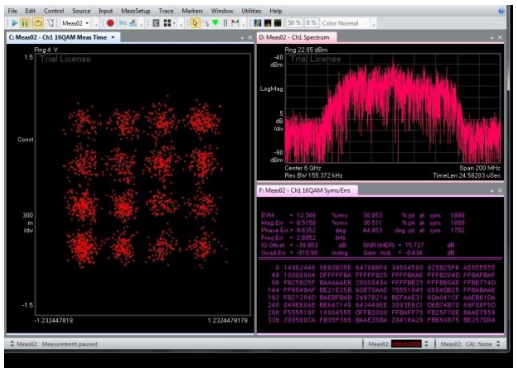
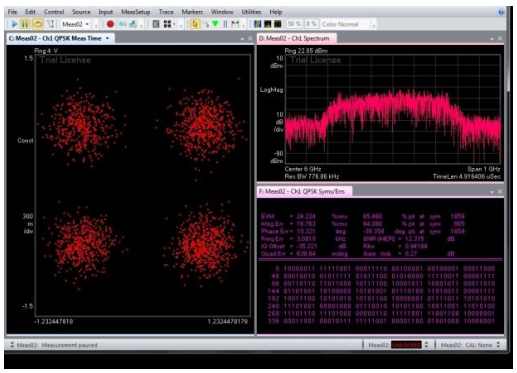



**Figure 4.7**: 60 GHz link measurement setup at 30 m.

16QAM (0.4 Gbps)



QPSK (1 Gbps)



QPSK (2 Gbps)

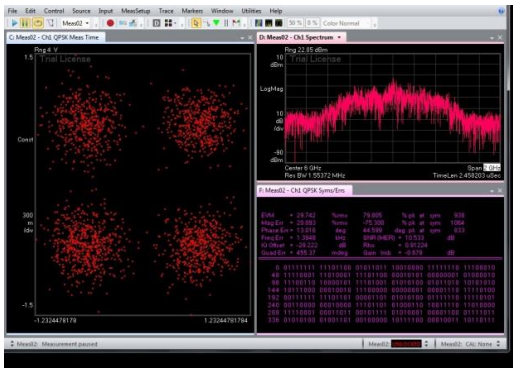


**Figure 4.8**: Measured constellation for QPSK, 16-QAM and 64-QAM at 56 GHz center frequency at 30 m.

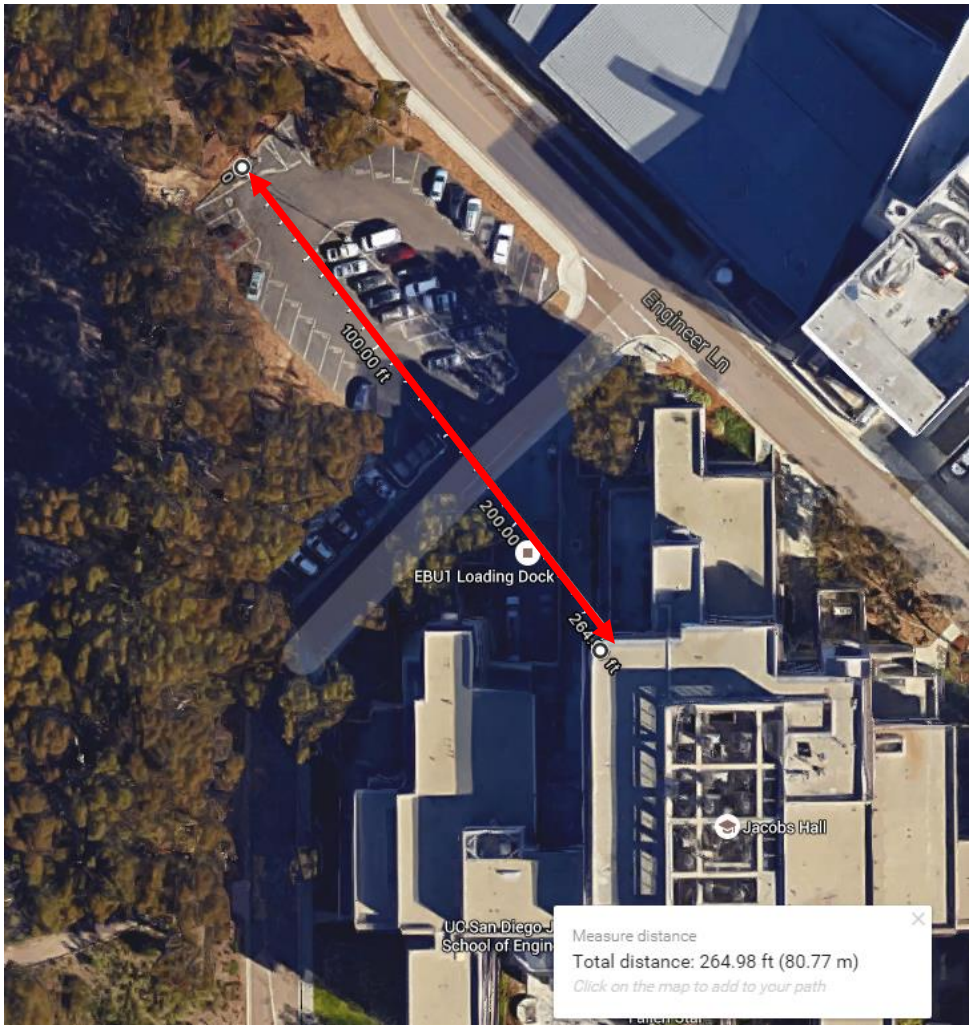



**Figure 4.9**: Bird-eye distance and map of the measurement setup for 90-100 m link.


**Figure 4.10**: Photo of the measurement setup for 90-100 m link.

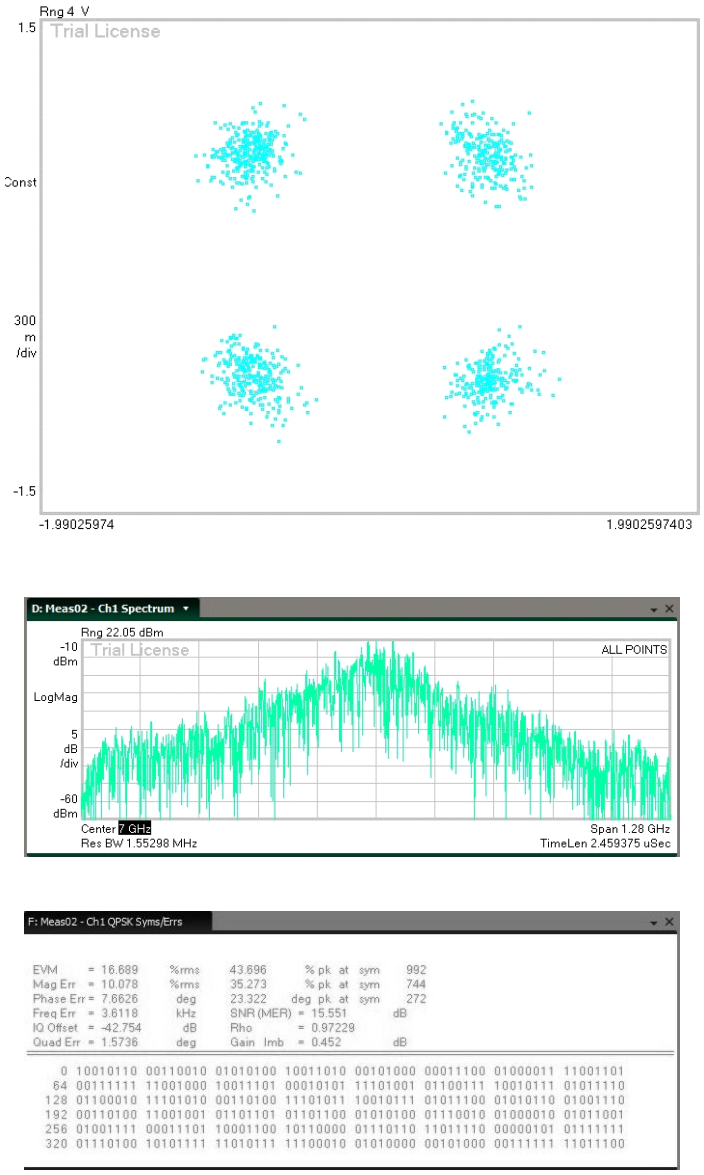



**Figure 4.11**: Measured constellations for 1 GBps QPSK modulation at 90-100 m.

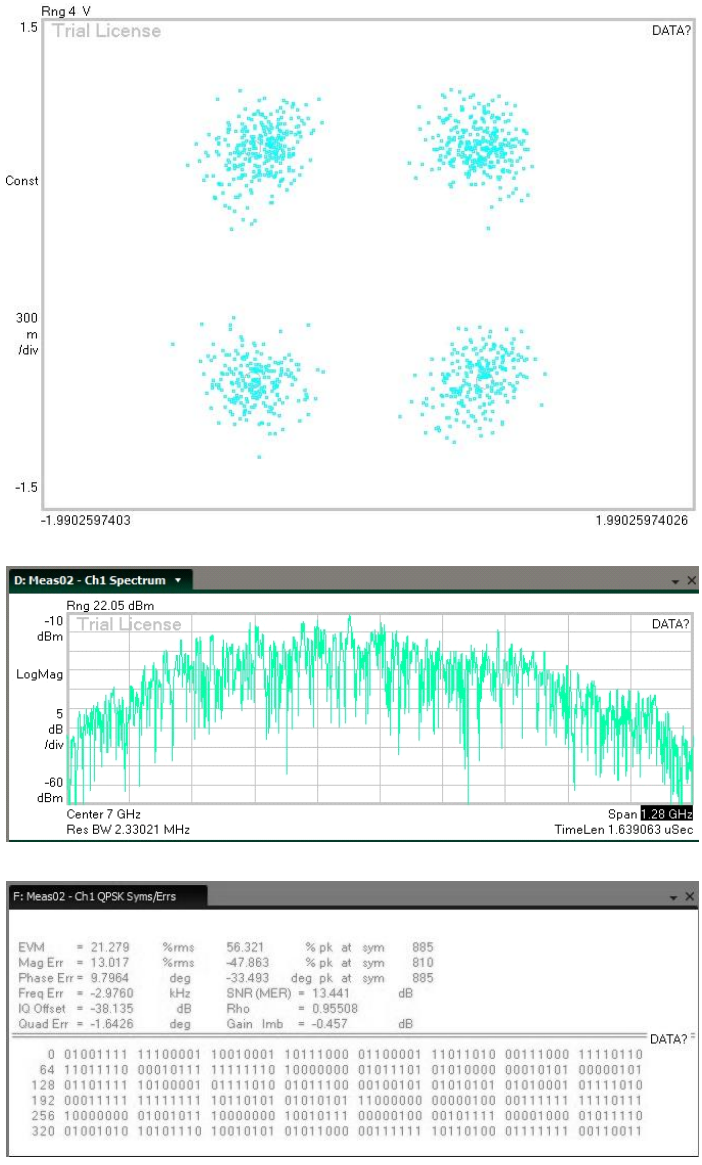



**Figure 4.12**: Measured constellations for 1.5 GBps QPSK modulation at 90-100 m.

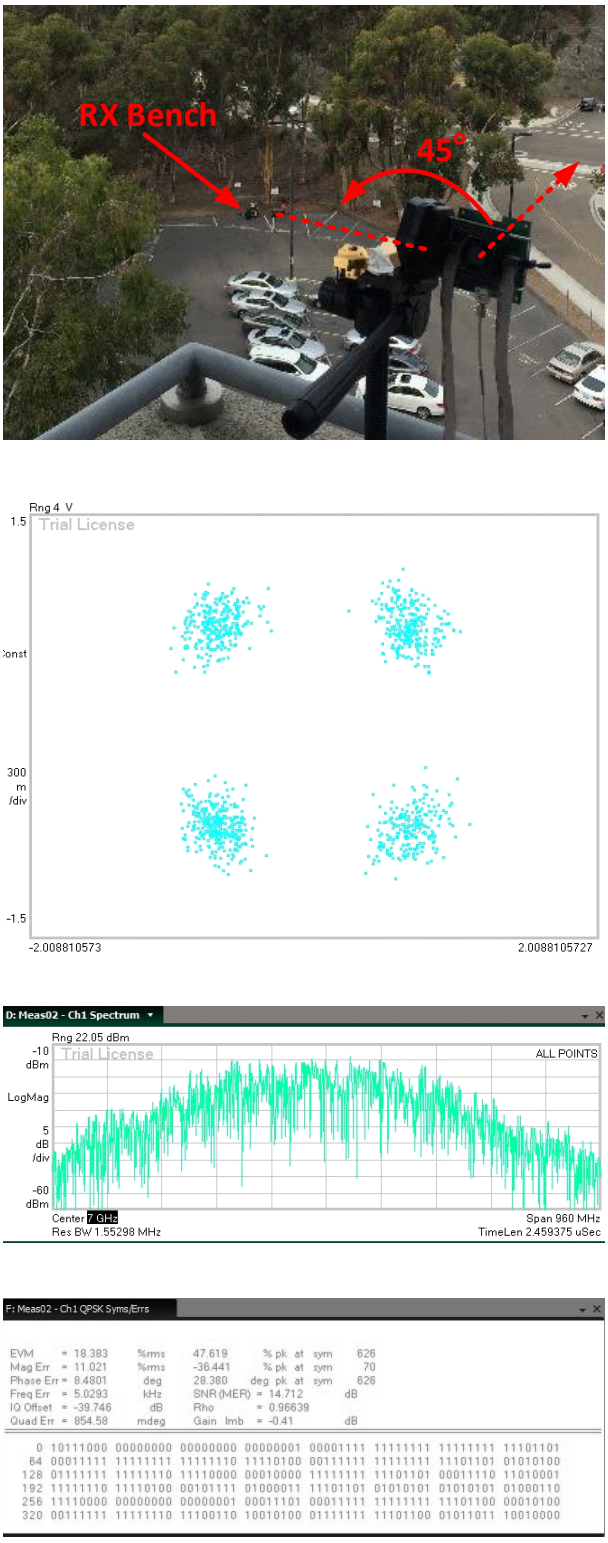



**Figure 4.13**: Measured constellations for 1.5 GBps QPSK modulation scanned to 45° at 90-100 m.

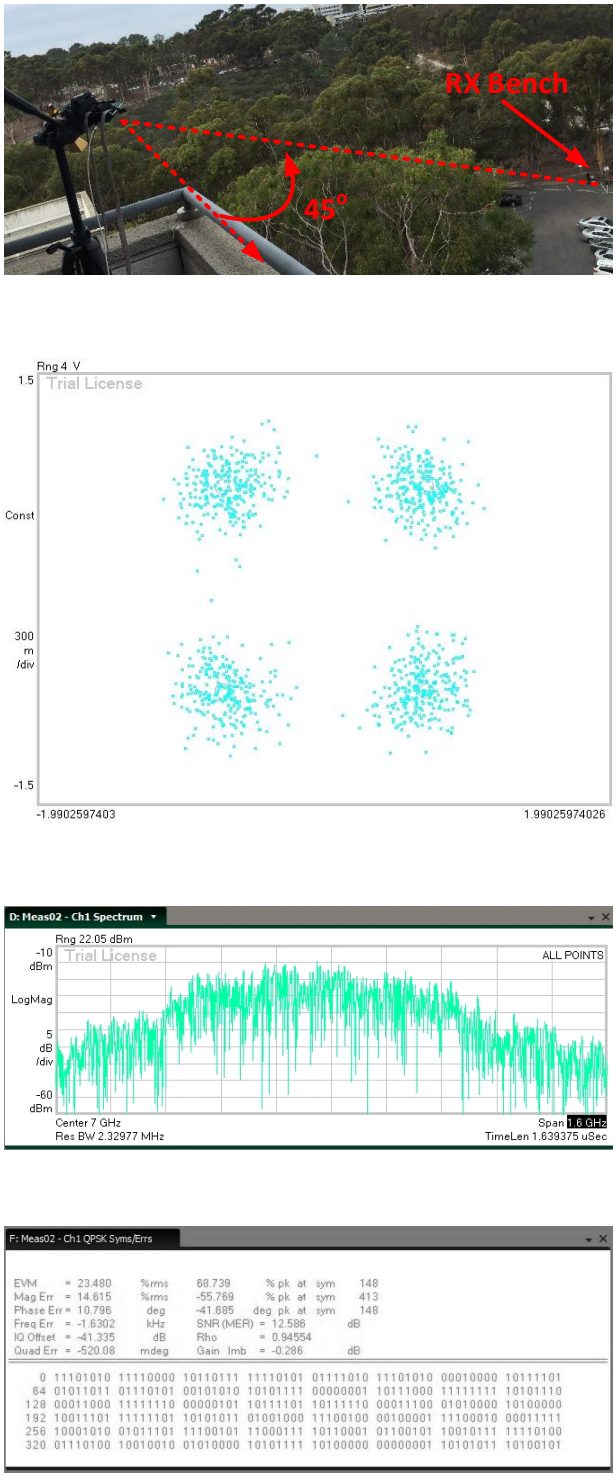



**Figure 4.14**: Measured constellations for 2 GBps QPSK modulation scanned to 45° at 90 m.

## 4.7 Link Measurements - 802.11a/d Standard

In addition to the QPSK and N-QAM measurements, wireless LAN (WLAN) specifications developed by the IEEE 802.11ad were tested. For this measurement, a very useful program, the 8199A Wideband Waveform Center (WWC) provided by Keysight (formerly Agilent) is used extensively [24]. To use this program, Keysight M8190A Arbitary Waveform Generator and Keysight DSO804A Real-time Oscilloscope are connected to a PC with WWC installed on it. The baseband signal with 802.11ad standards is modulated, upconverted and transmitted to the 64-element array. The DSO804A Oscilloscope demodulates the received signal and compares with the signal sent by AWG. The measurement setup is given in Fig. 4.15.

This program is used in the link measurements at 4 m distance. The measured results at different center frequencies are shown in Fig. 4.16. The measured EVM is around 10% from 56 to 60 GHz center frequencies. Even though the output power changes $\pm 2$ dB from 56 to 60 GHz, the channel has enough SNR to achieve the same EVM performance.

Similar measurements are performed with different scanning angles as shown in Fig. 4.17. The measured results show that EVM performance stay same for $\pm 45^{\circ}$ as provided in Fig. 4.18.

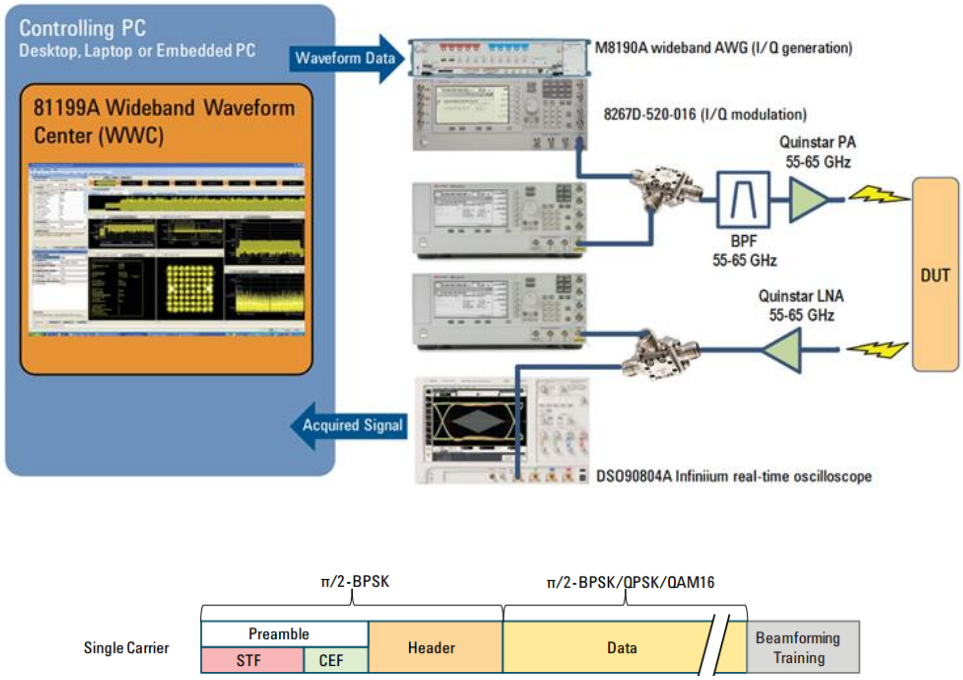
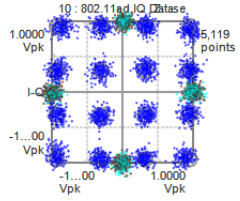



**Figure 4.15**: Measurement setup using Agilent 81199A Wideband Waveform Center (WWC)

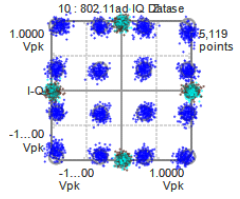
**EVM (10.5%) @ 56 GHz**




3 : 802.11ad Error Summary

| | | |
|---|---|---|
| Rho | 0.99438 | |
| Detected MCS Type | Single Carrier | |
| MCS | MCS11 | |
| Frequency Error | 323.26 Hz | |
| Symbol Clock Error | 0.6 ppm | |
| Estimated SNR | 17.978 dB | |
| EVM | -19.548 dB | 10.534 % |
| EVM (DC Compensated) | -19.552 dB | 10.529 % |
| I&Q DC Offset | -49.394 dB | |
| IQ Amplitude Imbalance | 0.036222 dB | |
| LO Quadrature Error | 1.2908 ° | |

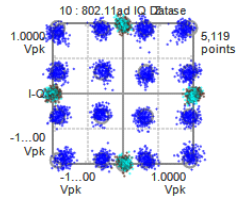
**58 GHz @ EVM (9.2%)**




3 : 802.11ad Error Summary

| | | |
|---|---|---|
| Rho | 0.99568 | |
| Detected MCS Type | Single Carrier | |
| MCS | MCS11 | |
| Frequency Error | 1.2830 kHz | |
| Symbol Clock Error | 2.2 ppm | |
| Estimated SNR | 20.260 dB | |
| EVM | -20.720 dB | 9.2041 % |
| EVM (DC Compensated) | -20.741 dB | 9.1824 % |
| I&Q DC Offset | -43.979 dB | |
| IQ Amplitude Imbalance | 0.17073 dB | |
| LO Quadrature Error | 0.82592 ° | |

**60 GHz @ EVM (9.7%)**




3 : 802.11ad Error Summary

| | | |
|---|---|---|
| Rho | 0.99114 | |
| Detected MCS Type | Single Carrier | |
| MCS | MCS11 | |
| Frequency Error | -71.058 Hz | |
| Symbol Clock Error | 1.2 ppm | |
| Estimated SNR | 22.402 dB | |
| EVM | -20.254 dB | 9.7114 % |
| EVM (DC Compensated) | -20.259 dB | 9.7060 % |
| I&Q DC Offset | -49.825 dB | |
| IQ Amplitude Imbalance | 0.080750 dB | |
| LO Quadrature Error | 1.4807 ° | |

**Figure 4.16**: 802.11ad measurement results at 56, 58 and 60 GHz.

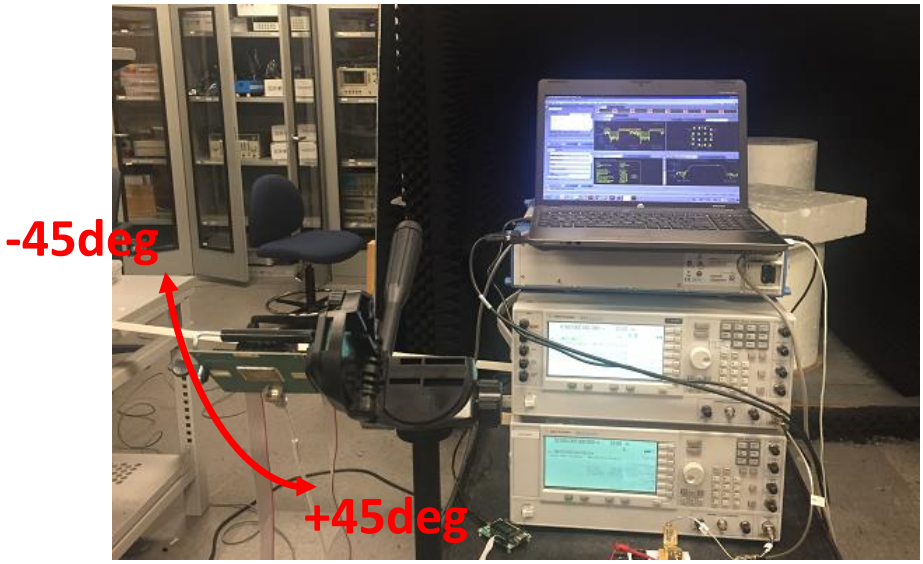



**Figure 4.17**: Measurement setup with different scanning.

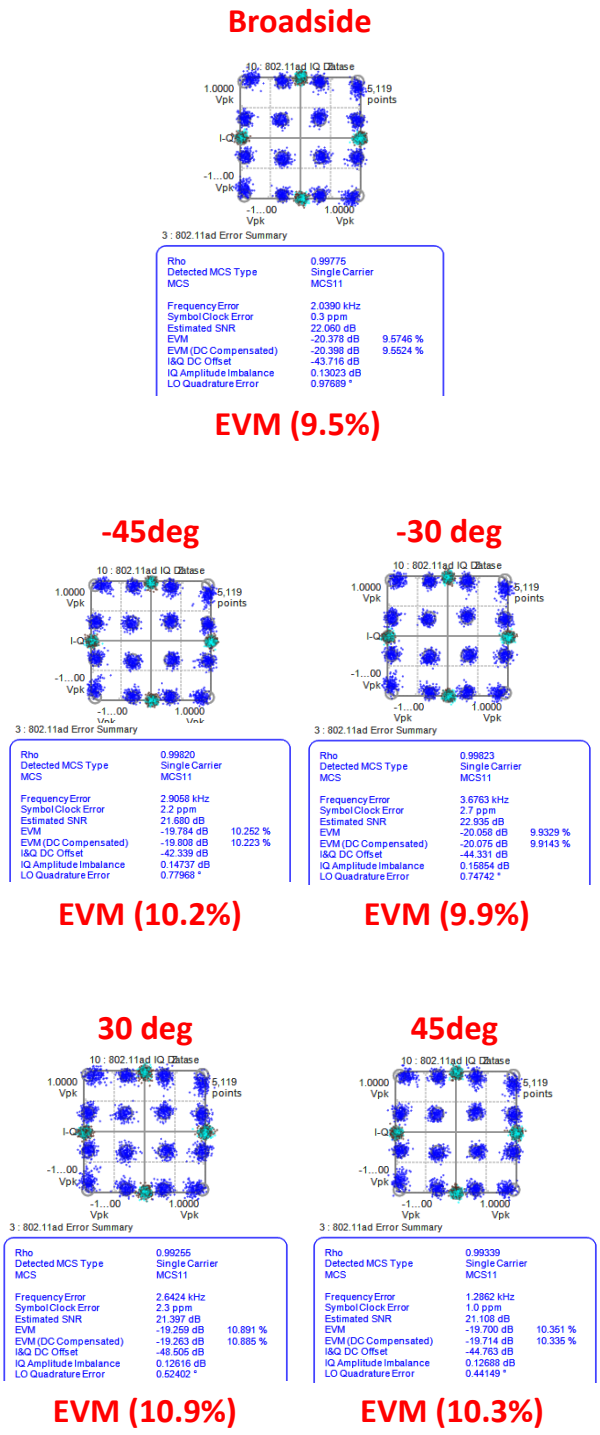



**Figure 4.18**: Measured 802.11ad channel performance at difference scan angles.

## 4.8 Link Measurements - WirelessHD

Lastly, the 64-element phased array transmitter is also tested in WirelessHD performance. For this measurement setup, HDMI-to-SDI and SDI-to-HDMI converters are used to transfer HD video into serial data (BPSK) and transmitted at 57 GHz. The received signal is again converted to HD standards and the output is connected to a LCD TV as shown in Fig. 4.19.

The measurement results are shown in Fig. 4.20 for different scanning angles in both E- and H-planes. The WirelessHD link is kept successfully.

## 4.9 Conclusion

In this chapter, 60 GHz link measurement details are provided for different frequencies, distances and standards. It is shown that the 64-element transmitter array can achieve 1.5 GBps successful link at 90-100 m and can keep the channel performance same for different scanning angles. Finally the 64-element phased array can be used for WirelessHD standard to transfer HD videos at different scan angles. For the first time, a phased array is fully characterized at 60 GHz for 802.11ad and WirelessHD standards with successful link characteristics.

## 4.10 Acknowledgements

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The dissertation author is the primary author of this material.

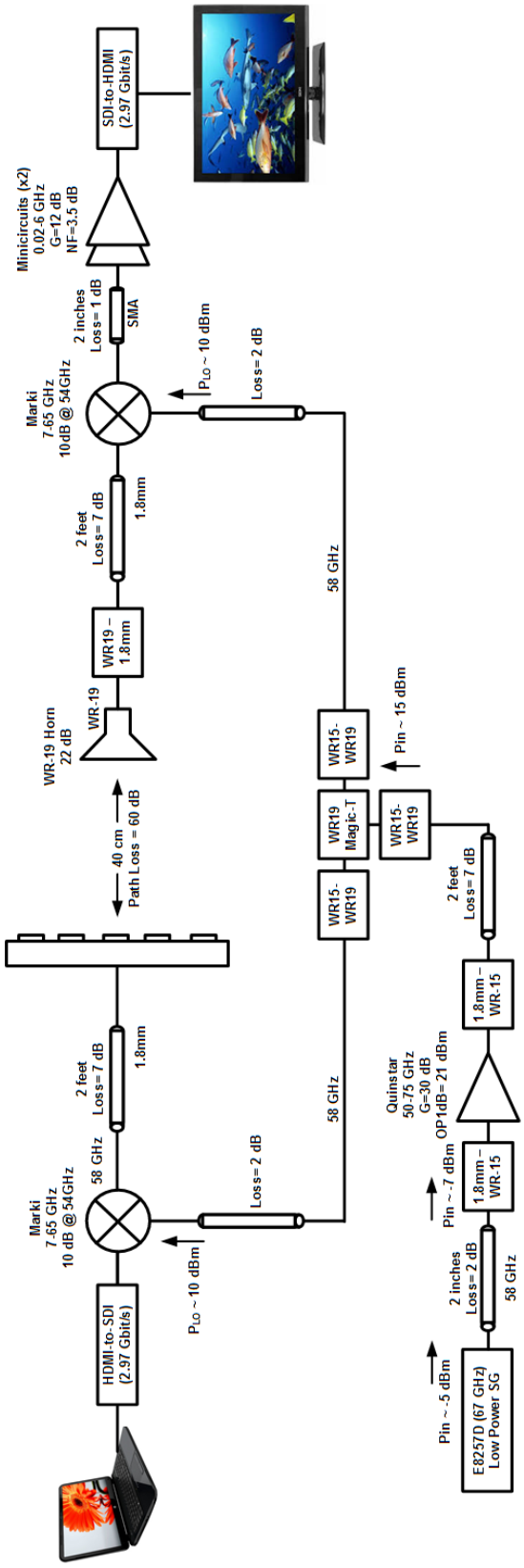



**Figure 4.19**: Measurement setup for WirelessHD.

**Figure 4.20**: Measurement results for WirelessHD at different scanning angles.

# Chapter 5

# 0.01-20 GHz High-Linearity Upconverter in 45nm CMOS SOI

## 5.1 Introduction

High linearity up-converting mixer are an essential component in base-stations, defense radios or transceivers requiring high linearity. Currently, high-linearity up-converting mixers are based on either a high-voltage, large-node BJT technology (0.5$\mu$m for example) which limits their bandwidth of operation, or on Schottky-diode mixers which require a large amount of *LO* power (15-20 dBm) and have 5-8 dB conversion loss at 10 GHz and above. This paper presents a novel high-linearity up-converting mixer with a very wide operating frequency (0.01-20 GHz), a wideband conversion gain of 0 dB, a high output power (16-13 dBm) and very high linearity ($>$ 30 dBm *OIP*3 at 10 GHz). This is achieved using a stacked transistor topology on 45nm CMOS SOI which allows high voltage, high power operation, while still using high performance devices.

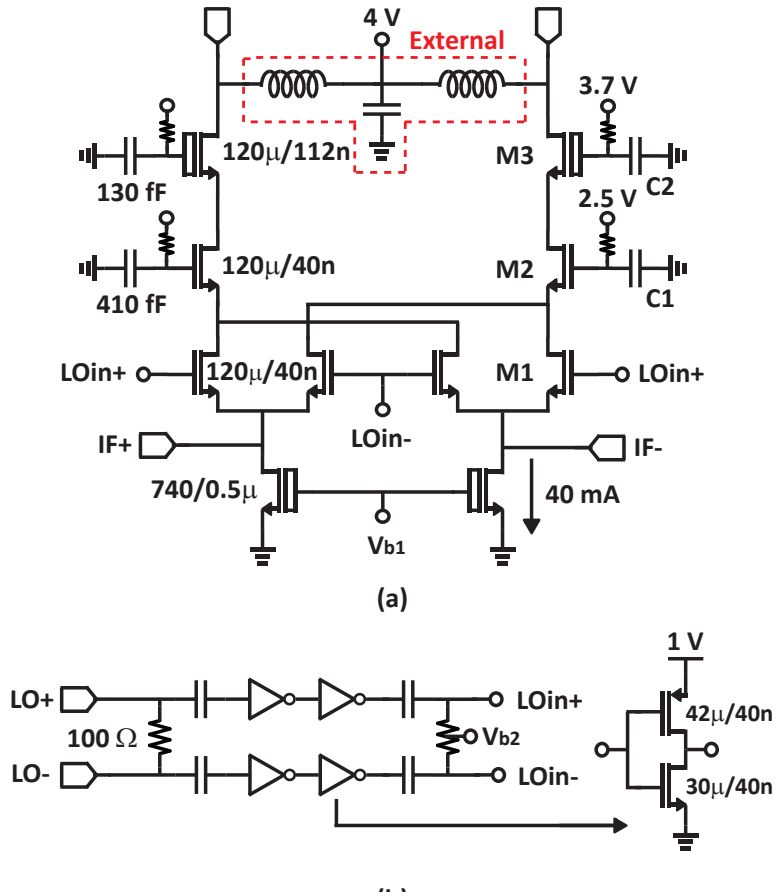



**Figure 5.1**: Simplified schematics of stacked upconverting mixer. (a) Mixer core, (b) LO buffers and CMOS inverter.

## 5.2 Design

The chip is implemented in the IBM 45-nm SOI process (IBM12SOI) with 190-240 GHz $f_t/f_{max}$ referenced to the top metal layer depending on the transistor size [25,26]. The high linearity upconverting mixer is based on a stacked-FET approach as shown in Fig. 5.1. The cross-coupled pair (*M1*) acts as a double-balanced mixer, and stacked transistors (*M2* and *M3*) operate as a power amplifying stage. The stacked transistors (*M2* and *M3*) resemble a cascode design, but unlike a cascode configuration where the gate of the common-gate transistors are RF grounded, the gate capacitances (*C1* and *C2*) allow the gate voltages to swing with the drain and source voltages. This approach ensures

that the voltage swing is shared across both the common-source (*M1*) and common-gate transistors (*M2* and *M3*) which are biased at the same D.C. current [27, 28]. The gate voltages of *M*2 and *M*3 transistors are selected such that all transistors operate below the breakdown voltage of this technology, which is approximately 1.5 V for thin-oxide and 2.5 V for thick-oxide transistors [29].

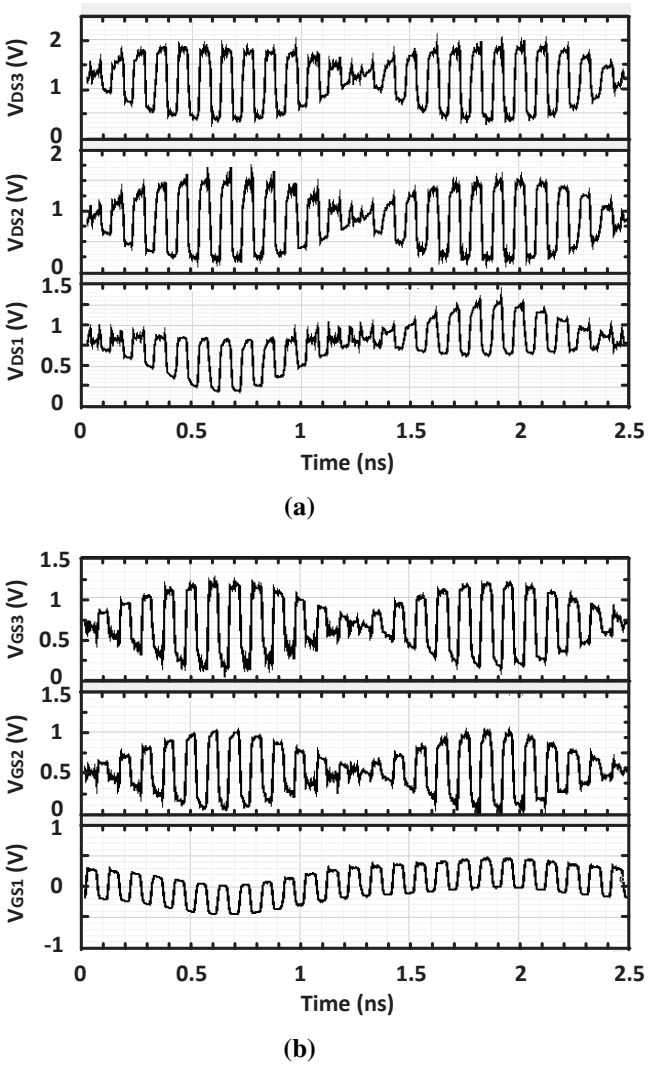



**Figure 5.2**: Simulated (a) drain-to-source and (b) gate-to-source voltage waveforms at ($P_{LO}$=-12 dBm, $P_{IF}$=14 dBm, $P_{RF}$=15 dBm, $f_{LO}$=10 GHz, and $f_{IF}$=400 MHz.

The optimum output load impedance is 100 Ω differential and the supply voltage is selected to be 4 V. The 100 Ω, together with a 80 *mA* bias current, ensures that the

output voltage swing will always be <4 V with an $OIP_{1dB}$ of 16−13 dBm at 0.01−20 GHz. The $IF$ input impedance is 15 Ω (single-ended) and is given by the 1/gm of $M1$.

Two pseudo-differential CMOS inverters are used to amplify the differential $LO$ signal and set the DC level of the $LOin$ level to 1.5 V ($V_{b2}$=1.5 V) for the optimum operation of the cross-coupled pair ($M1$). These amplifiers ensure a 0−1 V swing a the $M1$ gate for an input $LO$ power of −15 to −10 dBm up to 26 GHz.

The simulated conversion gain, defined as the output differential $RF$ power in a 100 Ω load, divided by the available power from a differential $IF$ source with a 100 Ω impedance, is 0−1 dB at $f_{LO}$= 0.01−20 GHz and $f_{IF}$= 0.01−1000 MHz including the 15 Ω $IF$ load mismatch to the 100 Ω $IF$ source impedance. A higher gain can be achieved if an external impedance transformer is used, but this will not result in a higher $OIP_{1dB}$.

Fig. 5.2 (a) and Fig. 5.2 (b) present the simulated drain-to-source and gate-to-source voltage waveforms of each FET at the highest output power, respectively, illustrating that $V_{GS}$ and $V_{DS}$ swings for all transistors are within the breakdown limit.

The chip is fabricated in the IBM 12SOI 45nm CMOS, which is built on a parrtially depleted 225nm SOI layer and a 13.5 Ω-cm substrate.

## 5.3 Measurements

The chip was assembled on an RO4003 substrate ($\varepsilon_r$=3.0, h=20 mils) using bond-wires for the $IF$ and $DC$ ports Fig. 5.3. GSSG probes were used on the RF and LO ports due to the wide bandwidth of the chip. The $IF$ inductance is ∼1.6 nH per arm which translates to j20 Ω at 2 GHz, and is not matched using capacitors on the board.

The measurement set-up is shown in Fig. 5.4. Two signal generators are used, one for the $IF$ signal and one for the LO signal, and a phase shifter is employed in the $LO$ path to compansate the phase error introduced by the 6−26 GHz hybrid coupler.

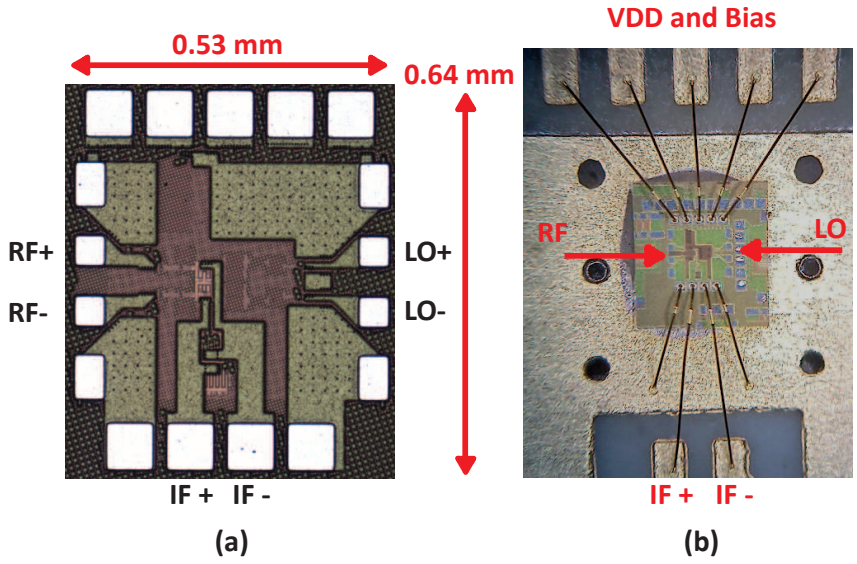



**Figure 5.3**: (a) Chip and (b) board photo.

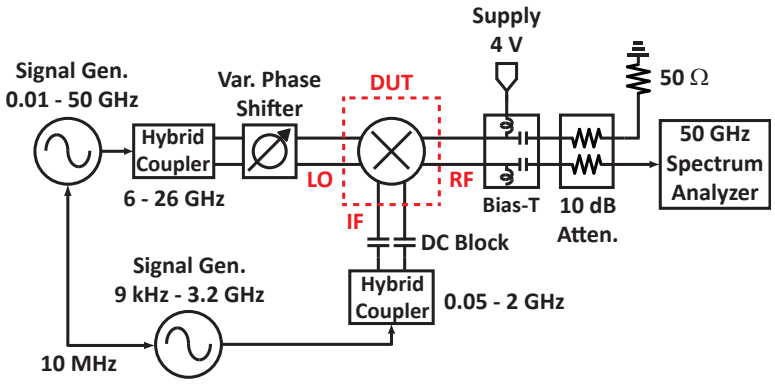
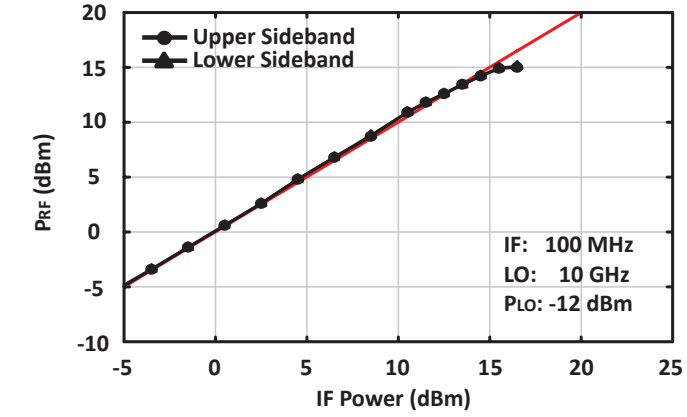
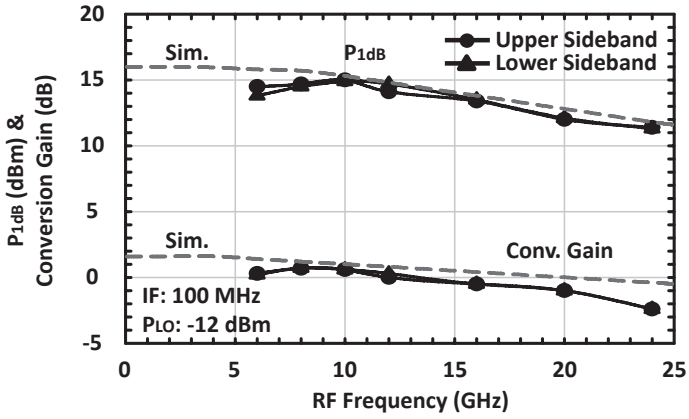



**Figure 5.4**: Measurement setup for the upconverting mixer.

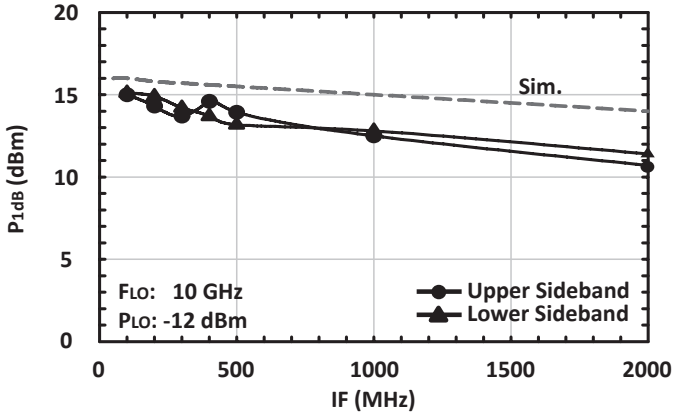
Due to the differential nature of the chip, wideband external baluns are used and this limits the lowest measurement frequency to 6 GHz (*LO*) and 50 MHz (*IF*). A bias-tee is used on the differential *RF* port and provides 4 V bias to the *M*3 drain. Due to the high output power from the upconverting mixer, a 10 dB attenuator is used before the spectrum analyzer. Note that the *RF* port does not contain an on-chip load, and the *RF* loads are the external 50 Ω loads. Therefore, it is not possible to measure the *S*22 at the *RF* port.




(a)



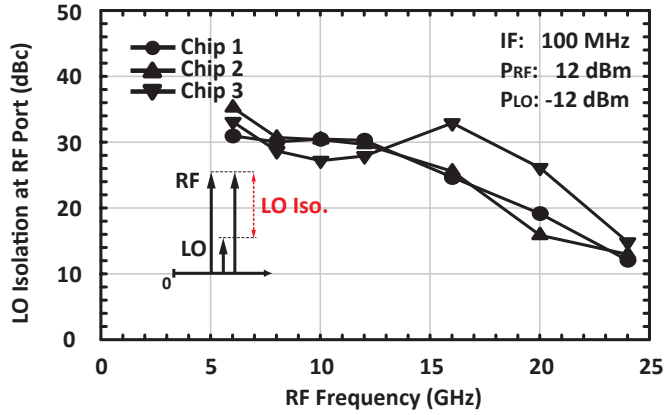

(b)



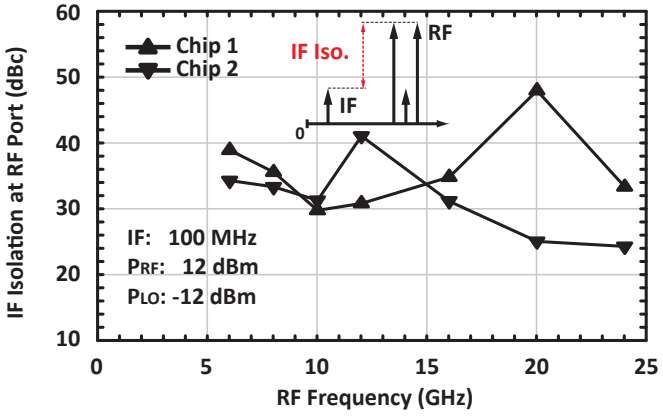

(c)

**Figure 5.5**: Measured (a) Pout vs. Pin (b) $OIP_{1dB}$, conversion gain vs. *LO* frequency, (c) $OIP_{1dB}$ vs. *IF*.

Fig. 5.5 presents the measured $P_{1dB}$ and conversion gain *vs*. frequency. An output $P_{1dB}$ of 15 dBm is achieved at 10 GHz with an $IF$ of 100 MHz for both the lower an and upper sideband response. The $OIP_{1dB}$ is $>$ 13 dBm up to 20 GHz. Note that no measurements exists below 6 GHz and also, the 1 dB difference between simulations and measurements at 6 GHz are both due to balun limitations. The measured conversion gain is $0\pm1$ dB at 6-20 GHz and agrees well with simulations. The measured $3-$dB $IF$ bandwidth is 2 GHz due to the bond-wires on the $IF$ ports. These measurements were all done at an $LO$ power of $-12$ dBm, and the $LO$ signal is amplified on-chip to 1 $V_{pp}$ at the gate of the $M1$ transistor.




**(a)**




**(b)**

**Figure 5.6**: Measured (a) $LO$ and (b) $IF$ isolation at the $RF$ port.

The $LO$ and $IF$ isolation at the $RF$ port are determined by measuring the $LO$ and $IF$ leakage in the output spectrum for an $IF$ of 100 MHz (nearly same results were achieved for an $IF$ of 500 MHz). The $LO$ and $IF$ isolation is $\sim$30 dB at 10 GHz and drops to 20 dB ($LO$) and 25 dB ($IF$) at 20 GHz (Fig. 5.6). Again, we believe that the isolation is limited by the external couplers. In fact, if a PRBS generator is used for the $LO$ path (two synchronized data streams set as sinewaves with 180° phase, one for LO+ and one for LO−), then the measured $RF$ isolation is $>$ 40 dB up to 20 GHz.

Fig. 5.7 presents the measured $IMD3$ products, and an $OIP3$ of $+$30 dBm is achieved at 10 GHz. The $OIP3$ is $\sim$25 dBm up to 20 GHz and agrees well with simulations. The measured $OIP2$ is $>$ 50 dBm at 6 GHz and $>$ 40 dBm up to 20 GHz. These represent state-of-the-art performance for an up-converting mixer.

## 5.4 Conclusion

A differential 0.01-20 GHz up-converter has been demonstrated using 45nm CMOS SOI. The design can be scaled to 50 GHz using smaller size devices. The design shows that stacking in SOI can be a powerful tool for high-power, high-linearity devices, and can result in state-of-the-art performance in advanced CMOS nodes.

## 5.5 Acknowledgements

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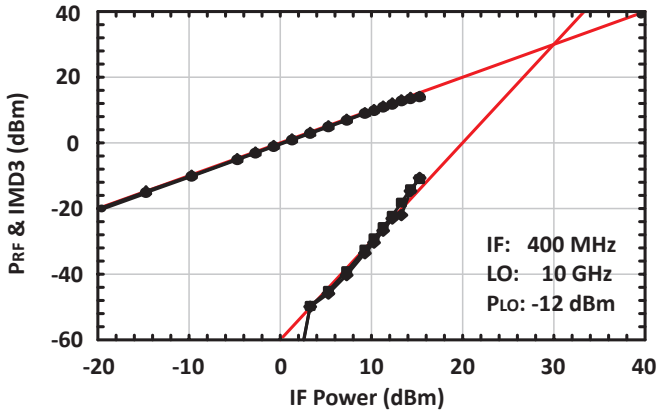
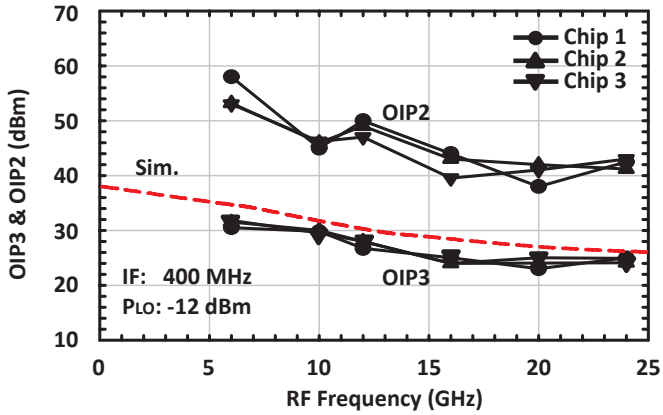
The dissertation author is the primary author of this material.




**(a)**




**(b)**

**Figure 5.7**: Measured (a) $P_{OUT}$ and *IMD*3 products and (b) *OIP*3 and *OIP*2 for single tone input signal.

# Chapter 6

# Conclusion

The thesis presented a truly wafer-scalable 60 GHz phased array transmitter for silicon RFICs and a wideband high-linearity upconverter using 45 nm in 12SOI process. First, the design challenges and as a solution sub-reticle stitching technique is presented to design a scalable phased array with 64 and 256 elements in Chapter 2. The proposed design is implemented in Jazz SBC18H3 process and the power and scanning performances are demonstrated in Chapter 3. More extensive measurements including 60 GHz link and wireless HD transfer are presented in Chapter 4. As a final work, a wideband highly linear upconverter is designed and measurement results are provided in Chapter 5.

Chapter 2 and 3 presented the design of a 60 GHz 64- and 256-element phased array transmitter with 38 and 45 dBm EIRP at 61 GHz scanning $\pm 55^{\circ}$ in both E- and H-planes. 64- and 256-element transmitters have a half-power beamwidth $12^{\circ}$ and $6^{\circ}$. To our knowledge, this is the largest single-chip phased-array ever developed and allows the construction of large-scale (1000+ elements) phased-array systems, either on a single wafer or by assembling several of these chips together.

Chapter 4 presented a 60 GHz successful link at 0.4, 4, 30 and 90 m distance

using a 64-element phased array transmitter. 2 GBps QPSK and 16-QAM modulations are presented with scanning $\pm 45^{\circ}$ without degrading the channel performance. The 64-element phased array transmitter achieved the record performance at the time of publication.

Chapter 5 presented a DC-20 GHz wideband high-linearity upconverter achieving $OIP_{1dB}$ is 15-13 dBm at 6-20 GHz with a conversion gain of $0\pm 1$ dB, and an $OIP3 > 30-25$ dBm and an $OIP2 > 40$ dBm at $10-20$ GHz. The $LO$ to $RF$ isolation and $IF$ to $RF$ isolation is $> 25$ dB at 10 GHz. To our knowledge, this work presents state-of-the-art results and shows the stacking capabilities of CMOS SOI devices.

## 6.1 Future Work

In chapter 2, a new solution using sub-reticle stitching for wafer-scale phased arrays on silicon is presented in detail. For demonstration purposes, 64- and 256-element phased array transmitters are chosen to be fabricated in Jazz SBC18H3 process. As a future work, larger phased arrays can be designed using similar techniques and 1000+ element phased arrays can be implemented in a single silicon wafers.

In chapter 3, 64- and 256- element transmitter with record-breaking EIRP and scanning were achieved. This work is promising to design better efficiency transmitter arrays with $<$50 mW transmitter channel compared to 100 mW per channel in the proposed design. Moreover, a Transmitter/Receiver (T/R) channel can be implemented for a 1000+ element T/R phased array next generation 5G applications at 60 GHz. Finally, a single-wafer phased array can be implemented achieving $>$50 dBm EIRP.

In chapter 4, the measurement results for 60 GHz link were demonstrated able to achieve 1.5 GBps link at 90 m. To achieve better performance and higher data rate at 60 GHz, digital pre-distortion (DPD) techniques can be used to demonstrate +2 GBps link

even at 100+ m.

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