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MIXED SIGNAL LETTER

Fully integrated CMOS nano-particle assembly circuit for biological detections

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Abstract Recently, along with the booming of research and production of CMOS Integrated Bio-sensing System, selective assembly of organic nano-particles on the on-chip electrodes, which serves for specific bio-sensing and detection purposes, is in high demand in areas like biological analysis and detection, DNA probing and surveying systems and etc. In this paper, a fully integrated bio-circuit targeting at electrical selective assembly of charged nano-particles is proposed and designed in SMIC 0.18 μm CMOS mixed signal process. The proposed circuit integrates the 16 pixels of 19 μm × 19 μm electrode array, counter electrode, potentiostat circuit, digital decoding circuit, as well as control logics on a single chip, and provides a rail-to-rail range of assembling voltage, a potential resolution of 8 bit, and a maximal assembling current up to 459 μA, biased at a current of 1 μA. Meanwhile, a novel electrode-reuse scheme is also proposed to further simplify the architecture and save chip area as well, without degrading the functionalities. Experimental results from on-chip selective assembly of 50 nm polystyrene nano-particles are included and discussed to verify the feasibility of the proposed circuits.

Keywords CMOS nano-particle assembly circuit (NAC) · Fully integration · Selective assembly · On-chip potentiostat · Electrode-reuse

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1 Introduction

Biomedical technology emerges since the past century and is believed to be one of the most promising industries in the twenty-first century together with micro- and nano-electronics industries. Recently, DNA molecule based biosensors are being reported by many famous literatures [1–3]. Naturally, the integrated bio-sensing system (IBS) which monolithically integrates the biomedical electrode arrays and ASICs in a single chip is avidly expected to greatly reduce the cost of common sensors used in the hospitals and markets.

Actually, some integrated DNA sensing circuits have been implemented in standard CMOS process [4–7], which firstly relies on gold–sulphur (Au–S) bond to self-assemble a DNA monolayer on the electrode surface, and detects the complementary DNA molecules in the electrolyte in terms of electric current by applying a voltage on the activated electrode. However, the non-specific Au–S bond can not selectively assemble the DNA monolayer on the target working electrode, thus limiting the specificity and diversity of the following sensing procedure. Although efforts have been made for the patterning of DNA assembly by introducing the electric releasing scheme, it becomes complicated in process and time consuming. Therefore, the selective assembling scheme is explored and realized in this paper, and the principle is shown in Fig. 1.

In this approach, nano-particles with fluorophores in side devolve in the electrolyte buffer and become negatively (or positively) charged particles, as a positive (or negative) voltage V_W is applied on the working electrode with respect to the reference voltage, these charged nano-particles are attracted by the electric field toward the activated working electrode, and eventually immobilized on the surface specifically due to electrochemical reactions.

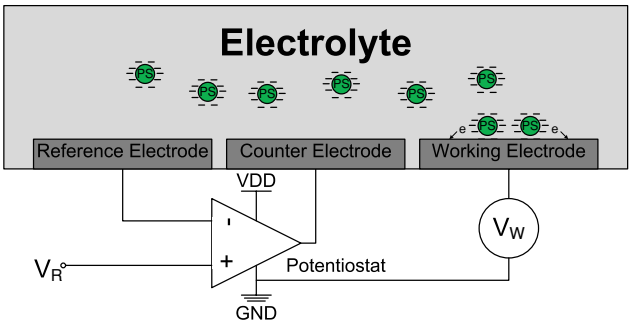

Fig. 1 Principles of nano-particles assembly

The current required for the reaction is provided by the potentiostat circuit from the counter electrode, which stabilizes the electrolyte potential at V_R from the feedback mechanism.

Furthermore, since the reference electrode serving for voltage reference and electrolyte potential control purposes in conventional architecture also introduces complexities in fabrication and extra expenses in chip area, therefore, in this paper, a fully integrated nano-particle assembly circuit (NAC) with a novel electrode-reuse architecture is designed in SMIC 0.18 μm CMOS mixed signal process. In this architecture, the electrode array combines both the functionalities of working and reference electrodes, which reduced the complexity of fabrication and substantially saved the chip area. The proposed circuit is further verified by experimentations from the selective assembly of 50 nm negatively charged polystyrene nano-particles (PS) in the mixture buffer of water and methanol onto address-activated working electrode by applying an assembling voltage, which makes it being a promising candidate of improving bio-sensing specificity and diversity of IBS in the future.

2 Circuit design and descriptions

The system topology of proposed CMOS NAC is illustrated in Fig. 2. It is designed with a 16 pixel of 19 μm × 19 μm working electrode array and a 140 μm × 19 μm counter electrode. A two-stage address decoding approach (pre-decoding and pixel decoding) is introduced to selectively activate the working electrodes of the NAC. An on-chip potentiostat circuit is implemented to control the electrolyte potential and provide electrochemical current by utilizing the negative feedback mechanism during assembly process.

2.1 Electrode-reuse architecture

As is mentioned in Sect. 2, the electrode-reuse architecture is proposed in the NAC to reduce the complexities in circuit design and fabrication and save chip area as well,

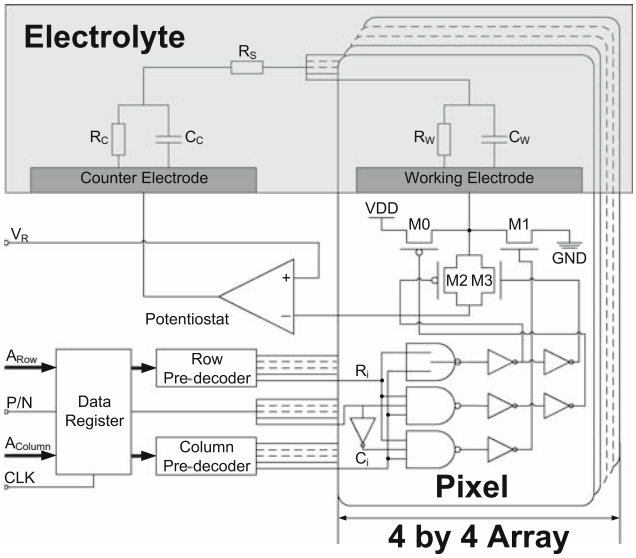

Fig. 2 System schematics of proposed CMOS NAC

which is described in Fig. 2. It can be seen that electrodes of all 16 pixels are either connected to the negative input of potentiostat circuit or shorted to the power supply VDD or ground GND by four transistors M_0, M_1, M_2, and M_3, depending on the state of that pixel. In fact, controlled by the pre-decoding logic and pixel logics, electrode of the activated pixel becomes the working electrode connected to VDD or GND, where nano-particles are assembled, while all the other inactivated electrodes are reused as the reference electrode in Fig. 1 to stabilize the electrolyte potential at V_R, which in turn saves the hardware expense of reference electrode.

Up on the rising edge of the clock *CLK*, logic states of A_{Row}, *P/N*, and A_{Column} are locked into the data register and propagating to the decoding stage. The decoding mechanism is realized by the two-stage decoding logic composed of row–column pre-decoder and pixel decoder. The standard transformation from input binary code to 1/N code is performed by the pre-decoder circuit, with the output being logic signals R_i and C_i for an arbitrary pixel i, where $i = 1, 2,\ldots,16$, as are shown in Fig. 2. If and only if both R_i and C_i are activated (logic "11"), the electrode is shorted to VDD or GND as working electrode by the pixel logic gates, depending on the logic "1" or "0" of the state signal *P/N* (in fact, the logic "1" state of *P/N* introduces a positive assembling voltage of VDD $- V_R$, while logic "0" implies a negative assembling voltage of $-V_R$ on the activated electrode); while all the other combinations of R_i and C_i (logic "00", "01", and "10") will connect it to the negative input terminal of potentiostat circuit thus functioning as the reference electrode. The true table of the proposed electrode-reuse architecture is illustrated in Table 1.

Table 1 True table of the electrode-reuse architecture

R_i	C_i	P/N	Electrode state
0	×	×	Reference
×	0	×	Reference
1	1	0	Working (GND)
1	1	1	Working (VDD)

Table 2 Specifications of CMOS NAC from the experimentations

Typical assembling voltage	1.8 ± 0.2 V
Min. assembling voltage	1 V
Electrolyte potential range	0–1.8 V
Max. potential variation	5 mV
Assembling current range	~10 nA to ~100 μA
Max. signal bandwidth	<100 kHz

2.2 Circuit design of on-chip potentiostat

The potentiostat circuit serving for stabilizations of electrolyte potential and accommodation of electrochemical current [7–9] is the major part of the proposed NAC. To satisfy specifications in Table 2, in the NAC, an OTA with rail-to-rail input common-mode range and Class-AB output stage is introduced to serve as the potentiostat circuit, which is depicted in Fig. 3.

The potentiostat OTA uses the complimentary folded-cascode input stage composed of transistor M_0 to M_{13} to achieve the rail-to-rail input common-mode range to enable the required assembling voltage, and reduce the input-referred noise to stabilize the potential as well, while incorporates the Class-AB output stage composed of transistor M_{29} to M_{32} to provide the maximized loading capability and accommodate the assembling current requirement. Transistors M_{14} to M_{21} function as the common-mode feedback circuit and provide biasing voltage for the folded-cascode input stage. M_{25} to M_{28} are two source follower to match the DC voltage between stages, while the other biases are served by M_{22} to M_{24} from a current $I_B = 1$ μA.

Post simulations are performed to verify the proposed potensiostat OTA. The results show that biasing at a current of 1 μA the circuit is capable of providing a rail-to-rail input and output dynamic range and a unit gain bandwidth up to 42.7 MHz, while the output current headroom, I_{max}, is over 450 μA, which meet the specifications in Table 2.

The potential variation is due to: (I) finite transconductance of the potentiostat OTA, (II) input referred noise, and (III) the input referred offset. If G_m^{DC} is the DC transconductance of the potentiostat OTA, the potential variation, V_{ft}, due to (I) can be expressed as

$$\frac{V_{ft} = I_{max}}{G_m^{DC}} \tag{1}$$

According to the noise theory, transistor M_0, M_1, M_5, M_6, M_7, M_8, M_{12}, and M_{13} in the first stage contribute to the overall noise. The noise power spectral density, S_I, in a MOS transistor is given by [10, 11]

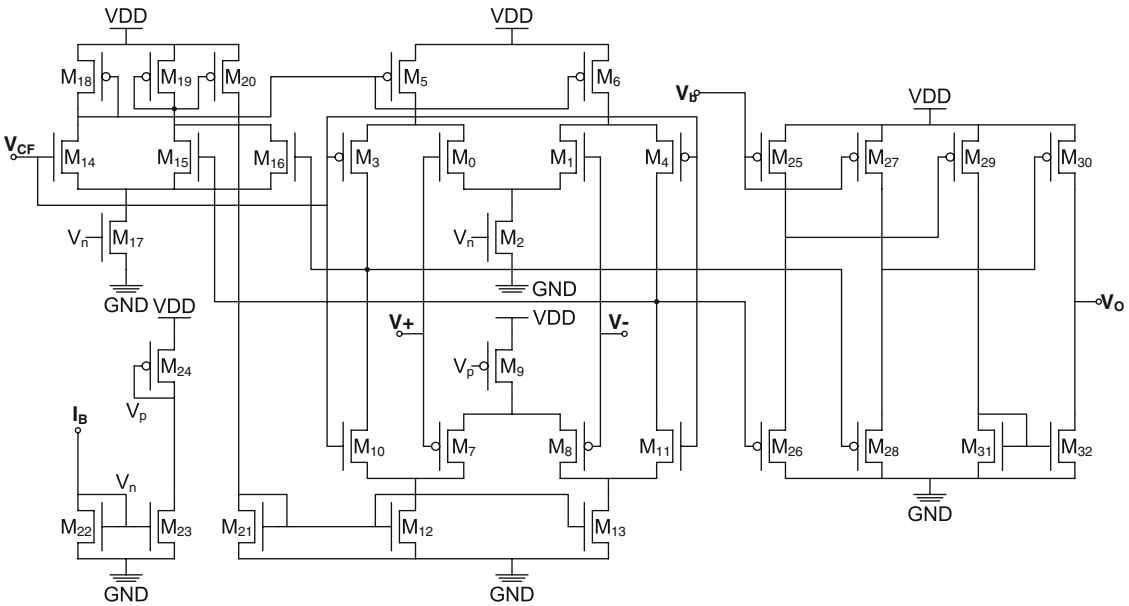

Fig. 3 Transistor level implementation of proposed potentiostat OTA with rail-to-rail input common-mode range and Class-AB output stage

Table 3 Summary of performances of proposed potentiostat OTA

Parameters	$V_{CM} = 0$ V	$V_{CM} = 0.9$ V	$V_{CM} = 1.8$ V
DC transconductance	2.22 S	5.43 S	3.90 S
3 dB bandwidth	1.97 kHz	2.07 kHz	1.94 kHz
Phase margin	>75°	>80°	>75°
Max. output pull current	451 μA	450 μA	–
Max. output push current	–	459 μA	459 μA
Input referred offset	3.51 mV	1.60 mV	2.75 mV
Input referred noise	61.8 nV/$\sqrt{\text{Hz}}$	38.2 nV/$\sqrt{\text{Hz}}$	57.7nV/$\sqrt{\text{Hz}}$
Overall potential variation	4.12 mV	1.93 mV	3.24 mV
Potential resolution	8 bit	9 bit	9 bit
DC power dissipation	40.4 μW	50.3 μW	58.0 μW
Power supply	1.8 V	1.8 V	1.8 V

$$\frac{S_I = 4\gamma kTg_m + K_F I_{ds}^{A_F}}{f^{E_F} C_{ox} WL} \tag{2}$$

where γ is the thermal noise parameter, g_m is the transconductance, I_{ds} is the drain-source current, C_{ox}, W, and L are the gate capacitance per unit area, transistor width and length, respectively, and k, T, and f are the Boltzman constant, temperature, and frequency, respectively. K_F, A_F, and E_F are flicker noise parameters with the typical values of 2×10^{-25}, 2, and 1, respectively. Since the corner frequency f_c, where thermal noise and flicker noise exhibit the same power density, is calculated as 5.4 Hz by using parameters provided by the foundry, much smaller than the unit gain bandwidth, therefore, flicker noise is negligible in the proposed OTA, and the input referred noise voltage $\overline{V_{irn}}$ can be characterized by

$$\frac{\overline{V_{irn}}^2 = 8\gamma kT(g_{m0} + g_{m5} + g_{m7} + g_{m12})}{(g_{m0} + g_{m7})^2} \tag{3}$$

where g_{mj} is the transconductance of transistor M_j, $j = 0, 1, \ldots, 32$.

$\overline{V_{irn}}$ can be diminished by increasing the biasing currents and aspect ratios of the input differential pairs, but trades off with the power consumption and the physical area. The spectral density input referred noise of proposed OTA on different common-mode input voltages are shown in Table 3.

Monte-Carlo simulation is also performed to characterize the input referred offset by utilizing the mismatch parameters provided by the foundry, and the results are also shown in Table 3. In the worst case with $V_{CM} = 0$ V, the overall potential variation due to the above three issues is 4.12 mV, which implies a 8 bit of potential resolution and satisfies the boundary condition in Table 2. The other circuit performances are summarized in Table 3.

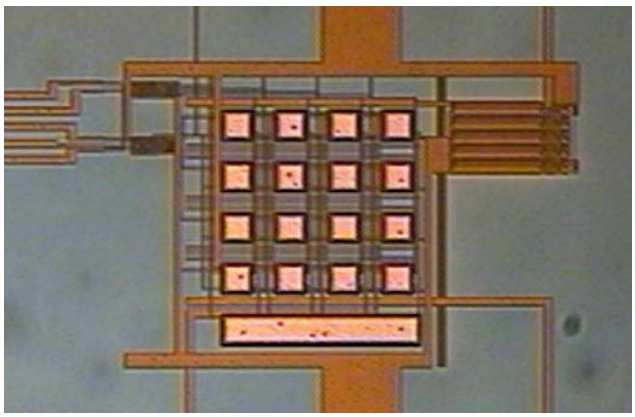

Fig. 4 Die micrograph of the CMOS NAC chip. The electrode array occupies only 170 μm × 140 μm of chip area

3 Verification and experimentation

The proposed NAC is designed in SMIC 0.18 μm CMOS mixed signal process with 1.8 V of power supply, and the electrode topology is shown in the die micrograph illustrated in Fig. 4. The selective assembly of 50 nm negatively charged PS is validated by experimentations in terms of fluorescence and atomic force microscopy (AFM), which in turn verify the feasibility of the proposed NAC.

The 50 nm PS internalized with fluorophores in the mixture buffer of water and methanol with the concentration of 0.1% are utilized as a prototype to demonstrate the selective nano-assembly in the experiment. Meanwhile, contrast experiments, fluorescence, as well as surface morphology are also investigated for further verifications.

In the experiment, a +1.8 V of assembling voltage of the activated working electrode is applied with respect to the electrolyte potential. According to the decoding scheme, the 16 electrodes in Fig. 4 are addressed as ⟨0000⟩, ⟨0001⟩, …, ⟨1111⟩ from the top-left to top-right horizontally, and from the top row to the bottom row vertically.

Firstly, the ⟨0000⟩ electrode is activated for 90 s with pure water as the electrolyte, and no fluorescence is observed as is shown in Fig. 5(a). Then electrode ⟨0001⟩ is activated for 90 s in the 1:1 mixture buffer of water and methanol with PS, and fluorescence is observed in Fig. 5(a). Thirdly, electrode ⟨0010⟩ is activated for the mixture buffer without nano-particles, as is expected, no fluorescence is observed in Fig. 5(b). Since the green emission nature of PS is foregone from the previous experiment, it can be concluded from the contrast experiment above that the PS are evidently assembled on electrode ⟨0001⟩ by the NAC. The AFM image in Fig. 6 shows the surface morphology of electrode ⟨0001⟩, which gives the direct evidence of the assembled 50 nm PS.

In order to characterize the time dependency of fluorescent intensity, electrode ⟨0011⟩, ⟨0100⟩, ⟨0101⟩, and ⟨0110⟩ are

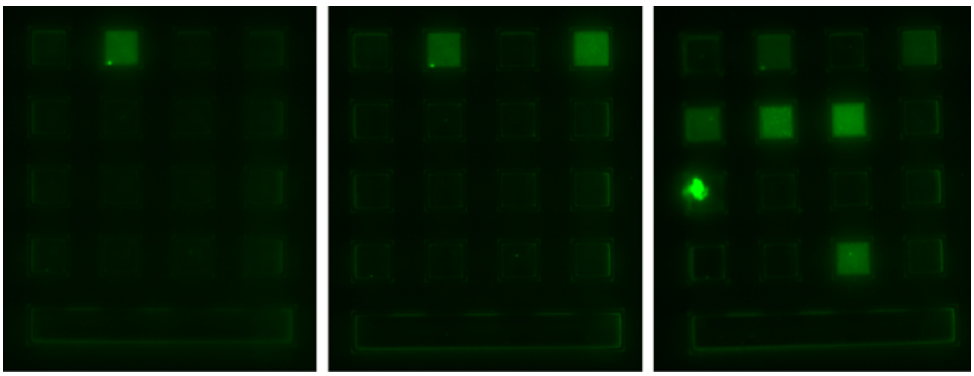

Fig. 5 Experimental results of 50 nm PS assembly on the activated working electrodes of the CMOS NAC chip

(a) Fluorescent picture of the 50 nm PS assembly on electrode ⟨0001⟩ and the contrast experiment on electrode ⟨0000⟩ by using pure water. The duration of applied voltage is 90 s.

(b) Fluorescent picture of the 50 nm PS assembly on electrode ⟨0001⟩ and the contrast experiment on electrode ⟨0010⟩ by using the mixture buffer without PS. The duration of applied voltage is 90 s.

(c) Fluorescent picture of the 50 nm PS assembly on electrodes ⟨0011⟩, ⟨0100⟩, ⟨0101⟩, and ⟨0110⟩ of different durations of applied voltages, which are 90 s, 120 s, 150 s, and 180 s, respectively. The electrode ⟨1110⟩ is also activated for 90 s to characterize the dependency of assembling rate on the distance apart from the counter electrode.

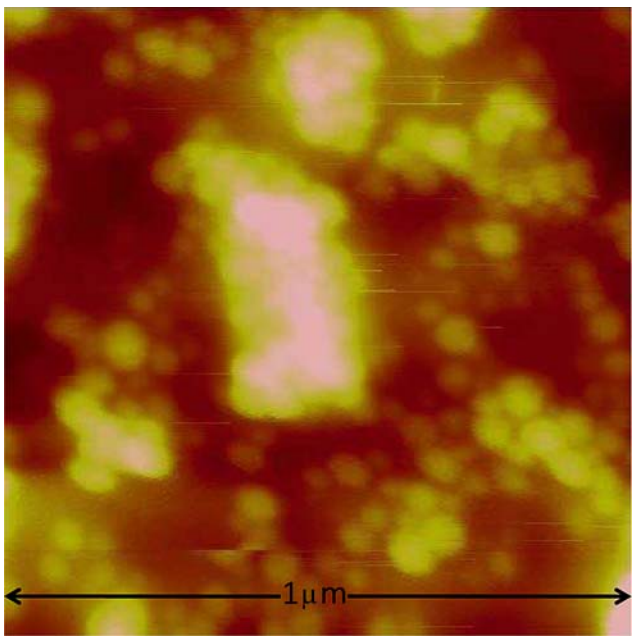

Fig. 6 The AFM picture of the electrode surface after the assembly of 50 nm PS. The area shown in this picture is 1 μm × 1 μm. It can be seen that the 50 nm PS nano-particles are evidently assembled on the electrode surface of the CMOS NAC

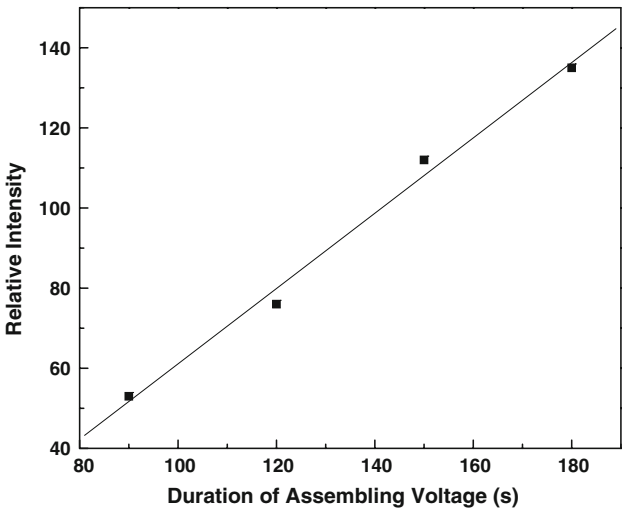

Fig. 7 The relative fluorescent intensity as a function of duration of the assembling voltage on electrodes ⟨0011⟩, ⟨0100⟩, ⟨0101⟩, and ⟨0110⟩, respectively. The *solid squares* represent the relative fluorescent intensities, while the line is the linear fit of the results

activated for 90, 120, 150, and 180 s, respectively. As is expected, Fig. 5(c) shows the gradual increment of the fluorescent intensity, while the linear time dependency of the fluorescent intensity is further illustrated Fig. 7, which implies the quantity of assembled PS on the activated electrode is proportional to the duration of the assembling voltage.

Finally, electrode ⟨1110⟩ is also activated for 90 s, however, it appears brighter than electrode ⟨0001⟩ and ⟨0011⟩, this is because it sits closer to the counter electrode, nano-particles feel stronger electric field on ⟨1110⟩ than on the other two electrodes.

4 Conclusion

In this paper, a fully integrated electrode-reuse NAC targeting at electrical selective assembly of charged nano-particles is proposed and designed in SMIC 0.18 μm CMOS mixed signal process. The circuit integrates the 16 pixels of 19 μm × 19 μm electrode array, 140 μm × 19 μm counter electrode, potentiostat OTA, digital decoding circuit, as well as control logics on a single chip, and is capable of providing

a rail-to-rail dynamic range of assembling voltage, a potential resolution of 8 bit, and a maximal assembling current up to 459 μA, biased at a current of 1 μA. Meanwhile, a novel electrode-reuse scheme is also proposed to further simplify the electrode architecture and save chip area as well, without degrading the functionalities. Experimental results show that the proposed NAC is feasible of selectively assembling the 50 nm PS prototype on the activated working electrode by the applied voltage, while the quantity of assembled PS is proportional to the duration of the assembling voltage. In fact, the 50 nm PS particle can be conjugated with multiple bio-species (biotin, streptavidin, or DNA molecule) on the surface, and selectively assembled on the activated working electrode from the proposed approach, which significantly improves the specificity and diversity of the following sensing/detection procedure and simplifies the process, comparing to the traditional self-assembly method relying on the Au–S chemical bonds.

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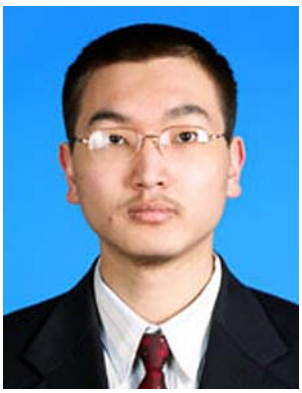

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