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High-Power CMOS SOI Switching and Applications in RF Signal Processing

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Cameron W. Hill

Committee in charge:

Professor James F. Buckwalter, Chair
Professor Forrest Brewer
Professor Umesh Mishra
Professor Mark Rodwell
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September 2020

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July 2020

High-Power CMOS SOI Switching and Applications in RF Signal Processing

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by

Cameron W. Hill

For Grampa.

Acknowledgements

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Finally thanks to my parents for supporting my education despite their continuous pleas for me to just "go get a job."

Curriculum Vitæ

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Education

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Publications

- C.1** H. AlShammary, **C. Hill**, A. Hamza and J. F. Buckwalter, “Code Selective Filters in CMOS Processes for Full Duplex Communication and Interference Mitigation,” GOMACTech, March, 2018.
- C.2** **C. Hill**, C. S. Levy, H. Al Shammary, A. Hamza and J. F. Buckwalter, “A 30.9 dBm, 300 MHz 45-nm SOI CMOS Power Modulator for Spread-Spectrum Signal Processing at the Antenna,” 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 423-426 .
- C.3** H. AlShammary, **C. Hill**, A. Hamza and J. F. Buckwalter, “A $\lambda/4$ -Inverted N-path Filter in 45-nm CMOS SOI for Transmit Rejection with Code Selective Filters,” 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 1370-1373.
- C.4** A. Hamza, H. AlShammary, **C. Hill** and J. Buckwalter, “A 52-dB Self-Interference Rejection Receiver using RF Code-Domain Signal Processing,” 2019 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, USA, 2019, pp. 1-4.
- C.5** **C. Hill**, A. Hamza, H. AlShammary and J. F. Buckwalter, “A 1.5-dB Insertion Loss, 34-dBm P1dB Power Modulator with 46% Fractional Bandwidth in 45-nm CMOS SOI,” 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2019, pp. 243-246.
- C.6** H. AlShammary, **C. Hill**, A. Hamza and J. F. Buckwalter, “A Code-Domain RF Signal Processing Front-end for Simultaneous Transmit and Receive with 49.5 dB Self-Interference Rejection, 12.1 dBm Receive Compression, and 34.3 dBm Transmit Compression,” 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2019, pp. 143-146.

- J.1** C. Hill, C. S. Levy, H. AlShammary, A. Hamza and J. F. Buckwalter, "RF Watt-Level Low-Insertion-Loss High-Bandwidth SOI CMOS Switches," in IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5724-5736. Dec. 2018.
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- J.6** H. Alshammary, C. Hill, A. Hamza and J. F. Buckwalter, "A Code-Domain RF Signal Processing Front End With High Self-Interference Rejection and Power Handling for Simultaneous Transmit and Receive," in IEEE Journal of Solid-State Circuits, vol. 55, no. 5, pp. 1199-1211, May 2020.
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Abstract

High-Power CMOS SOI Switching and Applications in RF Signal Processing

by

Cameron W. Hill

In-band full duplex (IBFD) for increased spectral efficiency but is limited by self-interference (SI) from the transmitter to the receiver. A combination of antenna-isolation, circulators, analog cancellation, and digital cancellation can achieve high levels of SI cancellation, but is still not enough to enable high-sensitivity IBFD operation. An additional layer of cancellation can be added in the code-domain. RF code-domain DSSS-CDMA approaches have been shown to add an additional 40-50 dB of SI cancellation. However, in order to make code-domain techniques compatible with other SI cancellation techniques, the interface must be RF-invisible and placed directly at the antenna interface. This requires RF-signal processing techniques in both the TX and RX paths of the transceiver. This work focuses on the development of high-power, high modulation bandwidth switches in cost-effective CMOS SOI processes which enable the transmitter side of code-domain SI without interfering with other self-interference cancellation techniques. First, theory groundwork of trade-offs between linearity, power-handling, and insertion loss in CMOS switches will be discussed. Then a variety of modulators based on this theory with fractional bandwidths (FBWs) approaching 50% and power handling of up to 40 dBm will be explained. Next, signal processing techniques to reduce unnecessary out-of-band (OOB) emissions will be given. Finally, the applications of these techniques in full-duplex systems, and further applications are discussed.

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Chapter 1

Introduction

1.1 In-Band Full Duplex and Code-Domain Approaches

With increasing demand for wireless spectrum, in-band full-duplex (IBFD) has become an active area of research with the goal of transmitting and receiving within the same bandwidth in order to increase the network capacity. [1–3]. A number of techniques have been proposed including digital cancellation [4,5], RF cancellers [6–8], CMOS circulators [9–11], electrically balanced duplexers [12, 13] and an example full duplex system diagram is shown in Fig 1.1. Each of these techniques can be combined to add another layer of cancellation. Figure 1.2 shows an outline of how much rejection can be achieved at each stage. If the sensitivity of the receiver is to approach -90 dBm with at transmit power of up to 27 dBm, then the overall rejection needs to be greater than 120 dB (assuming a moderate noise figure), and thus an additional 40-50 dB of rejection is needed when using current technology.

RF code-domain approaches are a recent development that have the potential to add additional rejection. With this additional rejection, the SI goals of Fig. 1.2 can potentially be met. Code-domain SI systems operate by adding a set of orthogonal codes

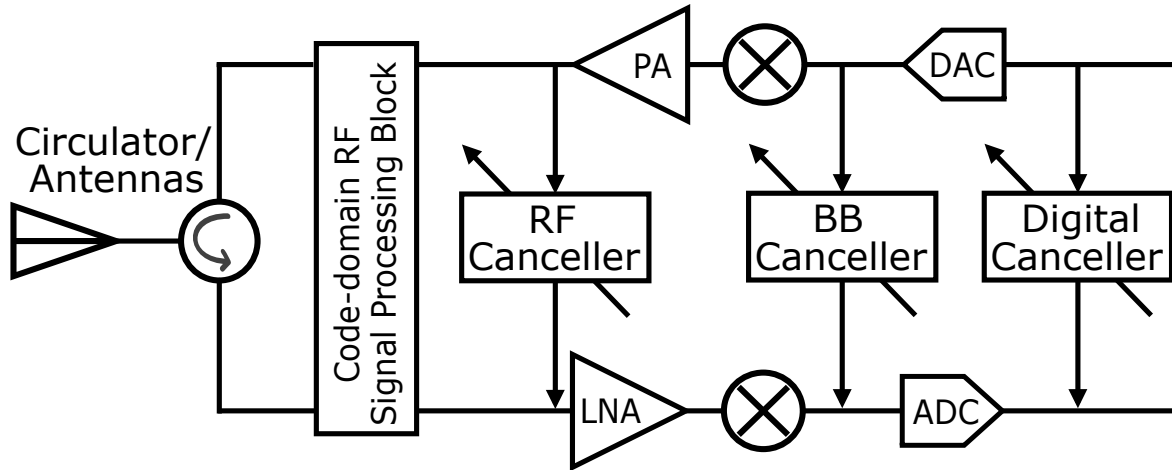


Figure 1.1: Example of serial full-duplex cancellation techniques in a transceiver.

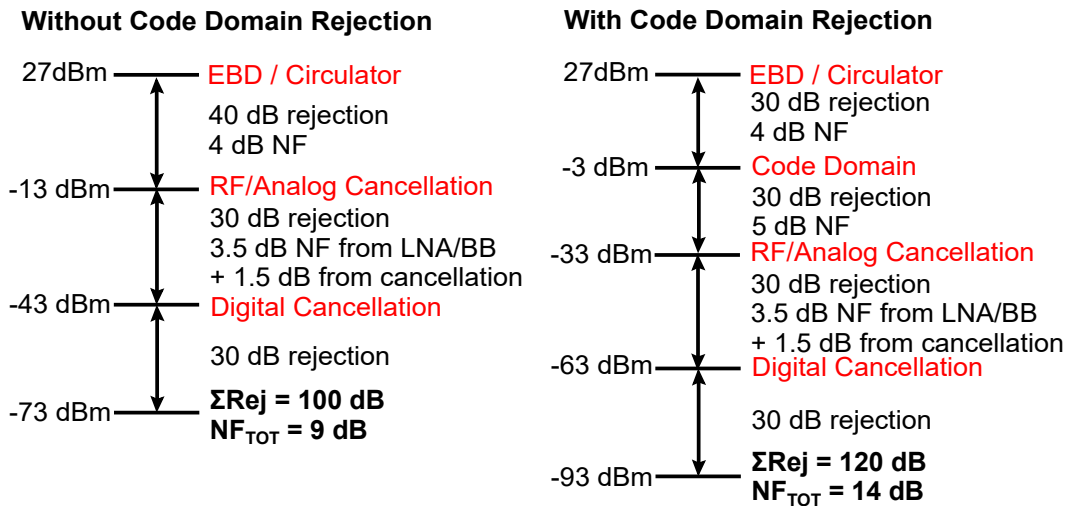


Figure 1.2: Required link budget for IBFD systems with and without code-domain techniques.

to each transmitted signal, and an integrator on each receiver to cancel undesired codes. A sketch of such a system is shown in Fig. 1.3 (a) and a diagram of the integrated waveform in Fig. 1.3 (b). The nature of adding these codes to each signal results in a much wider bandwidth than the original signal - N-times the bandwidth for an N-length code. Figure 1.4 shows that the longer the codes, the more rejection can be achieved, and thus a very wide-bandwidth is desirable. This is also shown in [14]. In order to make the code-domain systems compatible with other IBFD techniques and traditional

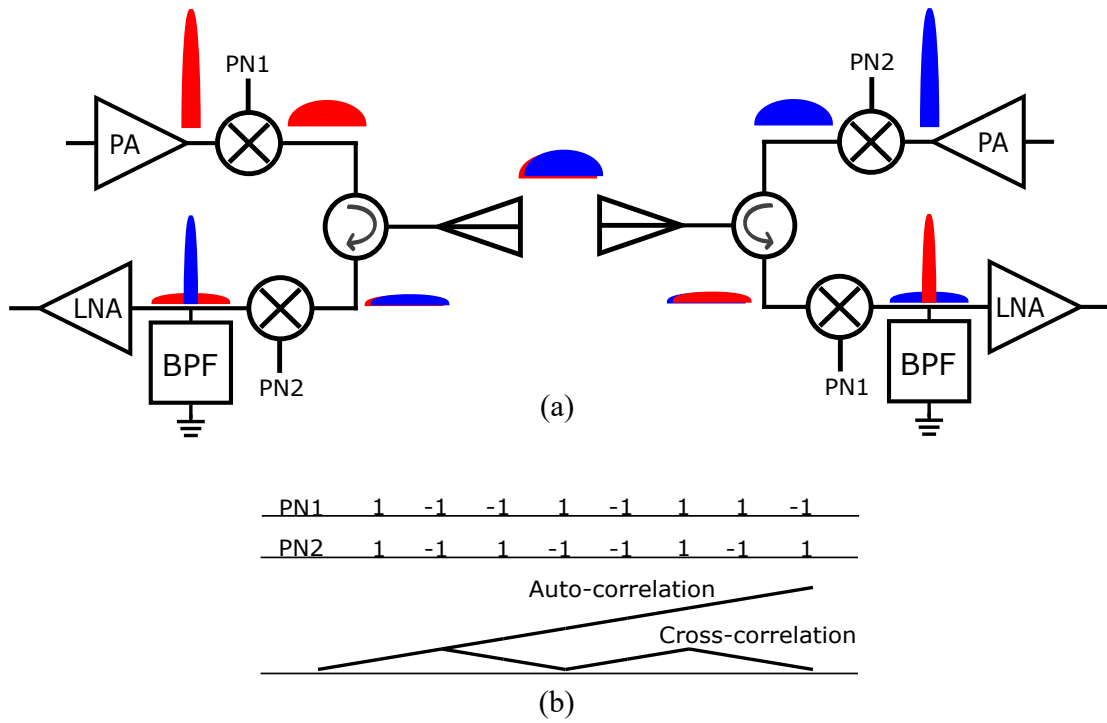


Figure 1.3: Cartoon of a code-domain channel and transceivers implemented at the RF interface.

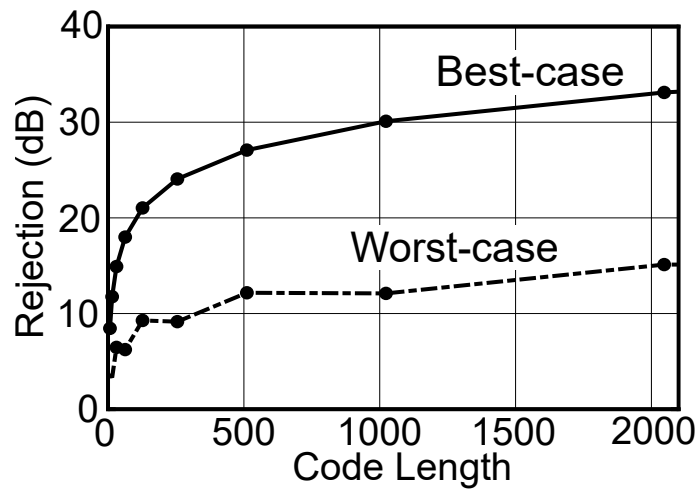


Figure 1.4: TX rejection for Gold codes with increasing code length in both best and worst-case scenarios

transceivers without adding significant bandwidth constraints, the code-domain systems must be added directly at the RF interface as shown in Fig. 1.1 and Fig. 1.3 (a).

The receive side of code-domain IBFD systems has been researched in great detail

in [14–20], however the transmit code-modulation is an area that remains to be explored. The TX PN modulators must be able to handle a high power, above 30 dBm and potentially up to 40 dBm while maintaining a high modulation bandwidth. For example, for a 1-GHz carrier, and a signal bandwidth of 1-MHz, to achieve high rejection using 128-length codes, the required fractional bandwidth (FBW) capabilities of the Tx modulating switches approaches 25%. A typical approach to building a binary modulator for BPSK modulation, or in this case PN modulation is shown in Fig. 1.5 and utilize quad configured differential RF switches and back-to-back baluns. The above specifications of high power handling, low loss, and high FBW are a challenging design space for existing RF switch technologies and serve as the motivation for the majority of this work.

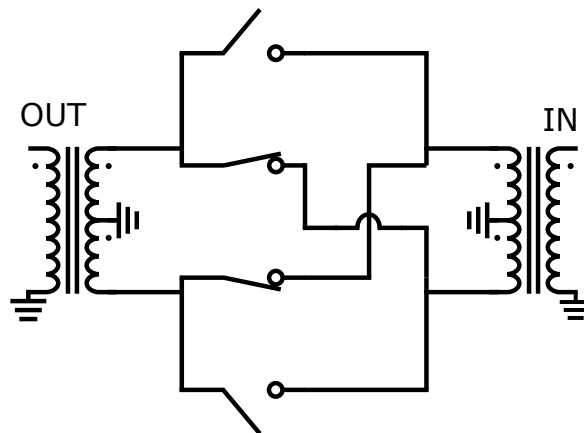


Figure 1.5: Typical BPSK modulator

1.2 Introduction to RF Switches

RF switches devices are designed to either be biased as completely non-conducting, or biased to be conducting as much as possible. Therefore traditional circuit/transistor design concepts like g_m , f_t/f_{max} and gain lose their meaning. RF switches are instead often characterized through their off-capacitance, C_{off} and their on-resistance, R_{on} . Given

a sufficiently low R_{on} and C_{off} , the switch will act like an ideal switch at low frequencies where R_{on} will look like a short circuit and C_{off} will look like an open circuit. As operation moves to higher frequencies, the impedance of C_{off} will drop and look more like a short circuit, eventually having its impedance approach that of R_{on} . The cross-over frequency where the impedance of R_{on} and C_{off} is equal and the device no longer behaves as a switch is a useful metric for switch performance that de-embeds the physical switch parameters such as width and length. This figure of merit is shown in eq. (1.1).

$$FOM = \frac{1}{2\pi R_{on} C_{off}} \quad (1.1)$$

The units of this figure of merit are in frequency, and the value is often too impractically large to measure the actual cross-over frequency - in the range of hundreds of GHz to tens of THz. In practice the factor of 2π is often ignored and the $R_{on}C_{off}$ product is used instead for simplicity. R_{on} and C_{off} are best measured by using the the setup shown in Fig. 1.6 (a). The measured S-parameters can be converted to Y-parameters, and R_{on} and C_{off} are computed from the test frequency and $-Y_{12}$ according the the Y-parameter equivalent circuit shown in Fig. 1.6 (d). [21].

The $R_{on}C_{off}$ product is useful for comparing different device technologies, but doesn't evaluate more complicated switch architectures. In most cases, several switches will be combined into single-pole double-throw (SPDT) or multi-pole multi-throw (MPMT) designs to route RF signals in different directions within the switch. An example of an SPDT switch is shown in Fig. 1.6 (e). In this case, more sophisticated figures of merit are required, such as the insertion loss to the ON state port, isolation to the OFF state port, linearity characterized by input referred 1 dB compression point (P1dB) or the input referred third order intercept point (IIP3), and switching speed.

The linearity of RF switches is highly dependent on the voltage breakdown and con-

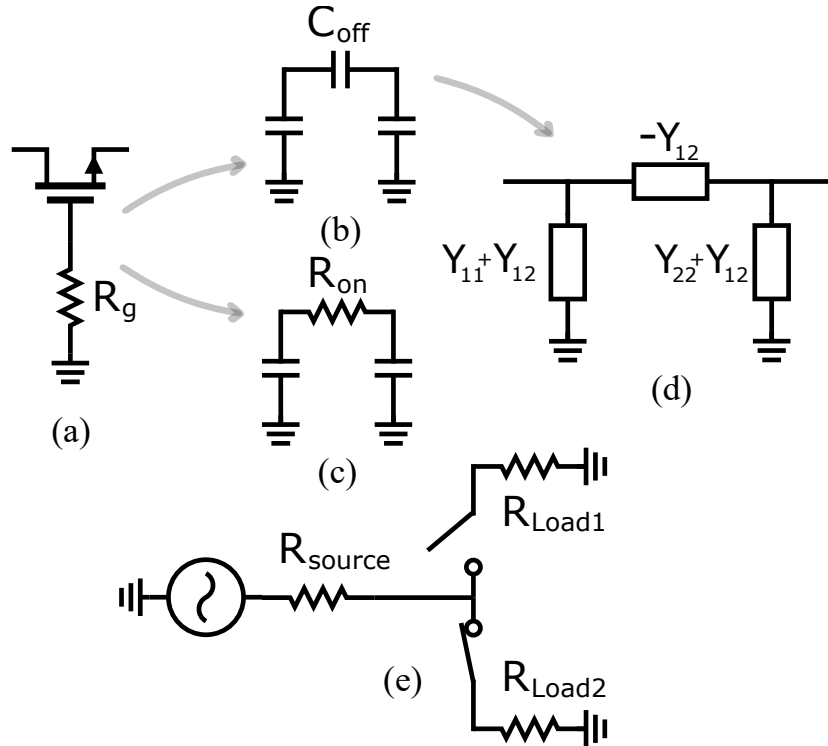


Figure 1.6: Circuit diagrams of: example switch setup (a), Off-state equivalent circuit (b), On-state equivalent circuit (c), Equivalent Y-parameters (d), and an SPDT switch (e).

trol/bias voltage of the device. Whether the switch be composed of a switching diode, III-V or silicon FET, as the RF voltage swing approaches the magnitude of the control voltage, the RF signal will become the dominant biasing signal causing unwanted turn-on or turn-off of the devices. This can be alleviated somewhat in three-terminal devices (transistors) by adding large resistors to the control line to separate the bias voltage from the RF signal. However, these large resistors in turn limit the switching speed of the devices, and thus there is a significant trade-off between switching speed and linearity of RF switches. Considering the voltage break-down and maximum biasing of the devices adds another layer to the design trade-offs and challenges. These trade-offs between technologies will be explored in the next section, and for CMOS switches in chapter 2.

To evaluate the switch designs in more detail, a different figure of merit in eq. (1.2)

can be used to capture more complicated trade-offs compared to $R_{on}C_{off}$

$$FOM = FBW \cdot P_{1dB} \cdot \left(\frac{P_{in}}{P_{lost} + P_{drive}} \right) \quad (1.2)$$

where the final component $\frac{P_{in}}{P_{lost} + P_{drive}}$ represents the system efficiency. This can be re-written in terms of the insertion loss and letting $P_{in} = P_{1dB}$ for the maximum power to give,

$$FOM = \frac{FBW \cdot P_{1dB}}{(1 - IL) + \frac{P_{drive}}{P_{1dB}}} \quad (1.3)$$

This FOM will be used to compare the switch designs in later sections.

1.3 Comparison of Switch Technologies

There are a variety of RF switch technologies that span the design trade-offs outlined previously. Here an overview of the advantages of each technology will be given with a summary in Table I.

1.3.1 PIN diodes

First PIN diodes offer excellent choices for high speed RF switches. PIN diodes rely on long carrier life-times within the intrinsic region of the diode to create a DC current controlled resistance. A unique feature of the PIN diode is that the diode is turned on and off by a DC current rather than a voltage. This means that the ON-OFF control and the RF power are completely decoupled, as it is the frequency of operation that will determine the state of the switch rather than the absolute voltage. As a result, PIN diodes offer extremely low distortion and will only compress as the devices heat up at higher RF power levels above 20 dBm [22]. However, since the operation of the switch is frequency dependent, this means that there is a minimum RF operating frequency -

as the frequency decreases, the current through the channel will cause the device to turn on and off in an undesired fashion. Even though the switching speed of the diode can be relatively low, on the order of the 10s of ns, the frequency dependent operation prevents high FBW switching. Additionally, the use of current to control the switch leads to additional complexity with any integrated drivers needing to be voltage tolerant in order to operate correctly at high power levels. The DC control current also contributes high static power dissipation.

1.3.2 MEMs

Micro-electrical mechanical (MEMs) switches offer an alternative with the best $R_{on}C_{off}$ performance possible of up to 80 THz [23] due to their operation which physically disconnects the circuit to turn off the switch. In the ON state MEMs simply act as a metal wire. This also lends itself to very high power handling on the order of hundreds of volts. While these switches can also be manufactured on a variety of substrates at low cost, they suffer from slow switching times, difficult control design, and reliability issues. Since the arm of the switch needs to physically move, the switching time is well above the micro-second threshold, and additional difficulty arises in stability and preventing the arm from resonating at faster speeds. The driver requirements are often up 70V and require specialized circuitry to activate the switch. Finally, while newer technologies are providing more mechanically robust switches, the tolerance of the switch to vibration and repeated switching is questionable with the use of moving parts. For code-domain designs, the switching time of MEMs precludes them from being an appropriate technology.

1.3.3 GaN

GaN offers advantages mainly in the high breakdown voltage offered in each device. High breakdown voltage translates directly to high linearity on the condition that the control voltage is high enough to over-ride the RF voltage and keep the switch in the correct state [24,25]. While GaN has the switching speed and power handling capabilities required for code-domain switching approaches, the linearity is simply accomplished through a high drive voltage which becomes costly to implement and prohibits easy integration. Additionally, GaN processes are not yet mature enough to offer large scale and low cost production, with the cost of a single device hundreds of times larger than previously mentioned technologies.

1.3.4 SOI CMOS

Finally, CMOS processes offer extremely fast switching on the order of 10ps, easy integration and drive characteristics, and low cost through mass production. SOI CMOS also has the additionally benefit of very low parasitics for excellent $R_{on}C_{off}$ metrics, 2-3 times better than GaN. The main drawback of SOI CMOS is the power handling since each switch can only have a gate or channel voltage of 1-2 V depending on the specific process and oxide thickness. This corresponds to approximately a 10 dBm compression point when the stated goal for code-domain techniques is above 30 dBm. Previous research has lead to designs that can alleviate this trade-off by adding large gate resistors to a series of stacked devices, enabling higher power handling [21,26–29] - these types of designs are common in commercial products. As previously mentioned these resistors improve power handling and linearity at the expense of switching speed. In the next section, the optimization of these stacking techniques will be addressed as to make a convincing argument for the use of CMOS SOI for code-domain techniques which require

both high power handling and fast switching speed in high performance RF switches.

TABLE I
SUMMARY OF COMPARISONS OF SWITCH TECHNOLOGY

Technology	Switching Speed	Power Handling	Driver Requirements	Cost
PIN Diodes	ns	High	Current Source	Low
MEMs	μ s	High	High Voltage	Low
FETs (GaN)	ns	High	High Voltage	High
FETs (SOI CMOS)	sub-ns	Low	CMOS Interface	Low

1.4 Dissertation Organization

This introduction provides a background and motivation for the rest of the thesis - why high-power, high-FBW switches are needed for code-domain IBFD systems, and why SOI CMOS is a desirable technology to explore with these types of switches.

Chapter 2 will explore the theory required to design and understand the operation of high-power CMOS switches and their trade-offs. A novel perspective on the large signal and compression modeling of the devices is presented and is used to optimize the RF switches for maximum modulation bandwidth. Additionally, different related architectures for faster series and shunt switches as well as their unique trade-offs and benefits will also be discussed.

Chapter 3 covers the design and measurements of three code-domain TX modulators designed with the techniques outlined in chapter 2. First an optimized resistive stacked switch modulator is presented, then a stacked ladder switch for higher modulation bandwidth, and finally, a reflective shunt modulator which offers the best metrics for combined

power handling and modulation speed.

Chapter 4 explores ways to curb the generation of harmonic content that is created when using signal processing at RF approaches to PN codes. This is problem similar to those faced by switching class D amplifiers and so a comparison between established techniques and a new deterministic pulse encoded transitions (PET) method is presented.

Chapter 5 outlines some experiments conducted with the integration of both TX and RX portions of the code-domain approach onto one silicon chip. System measurements and design trade-offs unique to this integration are presented and discussed.

1.5 Permissions and Attributions

The content of chapter 2.1-2.4, and chapters 3.1 and 3.2 are reprinted here, with permission, and were presented and published in the proceedings of the International Microwave Symposium (IMS) 2018 [30] ©IEEE 2018 and expanded in the IEEE transactions on Microwave Theory and Techniques (TMTT) in December, 2018 [31] ©IEEE 2018. Chapters 2.5, 3.3 are reprinted here, with permission, and were presented and published in the proceedings of the IMS 2019 [32] ©IEEE 2019 and expanded in IEEE TMTT in December, 2019 [33] ©IEEE 2019 which included the entire content of Chapter 4. The content of chapter 5 are reprinted here, with permission, and was presented and published in the proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC) 2019 ©IEEE 2019 [17] and was expanded to the IEEE Journal of Solid State Circuits (JSSC) May, 2020 [34] ©IEEE 2020.

Chapter 2

Large Signal Compression in RF Switches

In order to build high speed, high power switches and modulators, the operations of single CMOS switches must be understood first. This will be covered in detail with a focus on ensuring that the devices stay in “small signal” mode for as long as possible with increasing input power. To do this, the compression mechanisms in both the ON and OFF states must be considered along with how the two states may limit one-another. While this analysis focuses on SOI CMOS, many of the ideas and techniques apply to other types of switch design as well.

2.1 SOI Switch Modeling

The cross section of a CMOS SOI FET conventionally used as a switch is shown in Fig. 2.1(a) and the RF circuit model is simplified to Fig. 2.1(b). The 45-nm SOI process features a high resistivity substrate ($\sim 7500 \Omega\text{cm}$), which renders the substrate-parasitic capacitances negligible at RF frequencies, e.g., less than 10 GHz. Use of floating body

devices also allows for reduced parasitics which simplifies the switch model and maximizes the $R_{on} \cdot C_{off}$ product of the switch [35]. The gate resistance is significant and will be added to the analysis later as an external driving impedance.

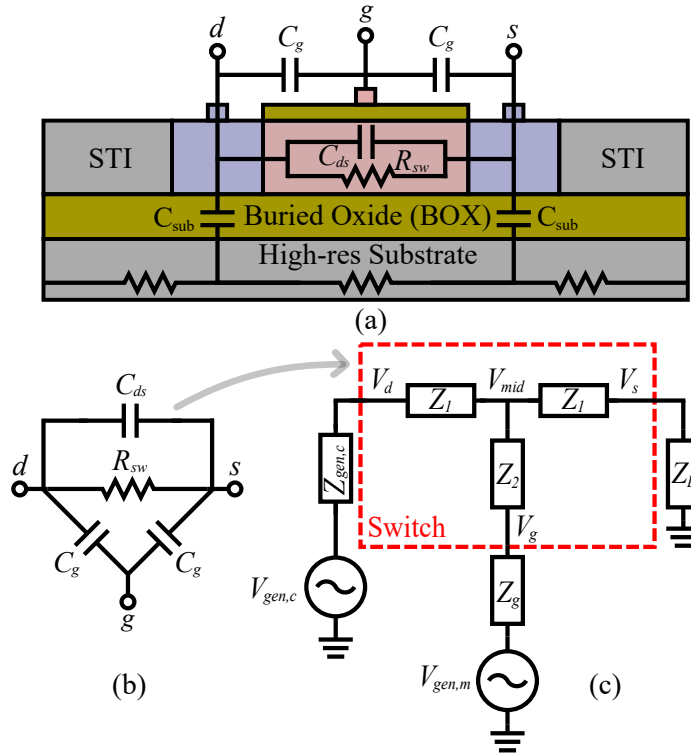


Figure 2.1: a) Diagram of intrinsic device parasitics from SOI FET structure, b) Reduced schematic for modeling, c) Switch network used for analysis after Δ -Y transformation

The model of the switch resistance could be derived based on a continuous current-voltage relationships but results in unwieldy equations that offer little intuition. Instead, the switch resistance R_{sw} can be modeled as a discrete function of the gate voltage defined by the onset of conduction relative to the characteristic impedance of the transmission line. In other words, the ideal RF switch model assumes

$$R_{sw} = \begin{cases} R_{on} \ll Z_o, & V_{gs} > V_{th} \\ R_{off} \gg Z_o, & V_{gs} < V_{th}, \end{cases} \quad (2.1)$$

where Z_o is the impedance of a generator and V_{th} is the threshold voltage of the transistor. Imperfect isolation between the source and gate implies that the on and off resistance of the switch change as a function of the RF power as a result of compression. To analyze switch under large-signal (compression) conditions, a Y-model of the switch transistor shown in Fig.2.1c) can be used. The Y model is a modification of the transistor capacitances and resistances applied to a $\Delta - Y$ transformation of the network in Fig. 2.1b) to analyze voltages that appear at the nodes of the device. The advantage of the Y model is that it incorporates intrinsic and extrinsic source, gate and drain impedances as series elements while also extending the model to more complicated stacked-FET switches in later sections.

The resulting intrinsic Y-model impedances, Z_1 and Z_2 , are

$$Z_1 = \frac{(R_{sw} || 1/j\omega C_{ds})}{2 + j\omega C_g (R_{sw} || 1/j\omega C_{ds})} \quad (2.2)$$

and

$$Z_2 = \frac{1}{j\omega C_g (2 + j\omega C_g (R_{sw} || 1/j\omega C_{ds}))}, \quad (2.3)$$

where the gate-drain and gate-source capacitances are assumed to be basically equal. If the switch is on, R_{sw} is small, e.g. R_{on} , and $Z_1 \approx R_{on}$ and $Z_2 \approx \frac{1}{2j\omega C_g R_{on}}$. The input impedance seen from the generator into the switch network is

$$Z_{in} = Z_1 + (Z_1 + Z_L) || (Z_2 + Z_g). \quad (2.4)$$

There are two signal sources of interest in this analysis, one high-frequency (or RF) generator and one low-frequency due to the modulation. Therefore, the drain, source, and gate voltages can be analyzed in superposition, using the subscript c and subscript m to represent the carrier and modulation signals, respectively. Using the Y model, the

voltages of interest at any node can be found, e.g. $V_d = V_{d,c} + V_{d,m}$.

$$V_{mid,c} = \frac{(Z_1 + Z_L) \parallel (Z_2 + Z_g)}{(Z_1 + (Z_1 + Z_L) \parallel (Z_2 + Z_g))} V_{d,c} \quad (2.5)$$

$$V_{d,c} = \frac{Z_{in}}{Z_{gen,c} + Z_{in}} V_{gen,c} \quad (2.6)$$

$$V_{s,c} = \frac{Z_L}{Z_1 + Z_L} V_{m,c} \quad (2.7)$$

$$V_{g,c} = \frac{Z_g}{Z_2 + Z_g} V_{mid,c} \quad (2.8)$$

The response due to a gate modulation, $V_{gen,m}$, reaches a similar set of equations.

$$V_{mid,m} = \frac{(Z_1 + Z_L) \parallel (Z_1 + Z_{gen,c})}{(Z_g + (Z_1 + Z_L) \parallel (Z_1 + Z_{gen,c}))} V_{gen,m} \quad (2.9)$$

$$V_{d,m} = \frac{Z_{gen,c}}{Z_1 + Z_{gen,c}} V_{mid,m} \quad (2.10)$$

$$V_{s,m} = \frac{Z_L}{Z_1 + Z_L} V_{mid,m} \quad (2.11)$$

$$V_{g,m} = \frac{Z_2 + (Z_1 + Z_L) \parallel (Z_1 + Z_{gen,c})}{Z_g + Z_2 + (Z_1 + Z_L) \parallel (Z_1 + Z_{gen,c})} V_{gen,m} \quad (2.12)$$

To compare performance, the insertion loss (IL) can be defined by $IL = -20 \log_{10}(S_{21})$ assuming the generator and load impedance are the same. Therefore, this expression is only valid when evaluating the composite switch as a whole, and as such will not be used when discussing the loss of an individual FET component of a stacked switch.

2.1.1 Conditions for On-State Conduction

The condition for the switch to remain ON in the presence of RF and modulation sources is given by

$$|V_{gd,m}| - |V_{gd,c}| > V_{th}. \quad (2.13)$$

Since (2.8) and (2.12) allow a superposition of the RF carrier voltage and the gate modulation voltage, expressions for P_{1dB} and the switch modulation rate are interdependent, and an increase in either input power, or modulation frequency can cause the switch to compress. While (2.6) through (2.12) are used to derive expressions for the IL, power compression (P_{1dB}) and modulation fractional bandwidth (FBW) of the switch, this can be in practice cumbersome and will only be used here for simulation. However, in the limit that $R_{sw} = 0$, the drain and source of the FET are effectively connected at the same node ($Z_1 = 0$), and $Z_2 = 1/(j\omega 2C_g)$ and the expressions for $V_{gd,m}$ and $V_{gd,c}$ reduce to

$$V_{gd,m} = \frac{1}{1 + j\omega_m 2C_g(Z_g + Z_{gen,c}||Z_L)} V_{gen,m} \quad (2.14)$$

and

$$V_{gd,c} = \left(\frac{-1}{1 + j\omega_c 2C_g Z_g} \right) V_{d,c}. \quad (2.15)$$

$$V_{gen,c,1dB} = \sqrt{1 + 4\omega_c^2 C_g^2 Z_g^2} \left(\frac{V_{gen,m}}{\sqrt{1 + 4(\omega_m C_g (Z_g + Z_{gen,c}||Z_L))^2}} - V_{th} \right) \left(\frac{Z_{in} + Z_{gen,c}}{Z_{in}} \right) \quad (2.16)$$

Considering (2.13) to be an equality gives a condition to calculate the 1-dB compression point in (2.16). In the simplified case of (2.14) and (2.15), this suggests a 1-dB

compression voltage of (2.16) is dependent on the input power through $V_{gen,m}$. Additionally, the switch compresses due to the dependence on both ω_m and ω_c . When the $\omega_m = 0$, (2.16) reduces to

$$V_{gen,c,1dB} = \sqrt{1 + 4\omega_c^2 C_g^2 Z_g^2} \left(\frac{Z_{in} + Z_{gen,c}}{Z_{in}} \right) (V_{gen,m} - V_{th}), \quad (2.17)$$

which indicates that the compression point is directly related to the threshold voltage of the switch compared to the bias voltage.

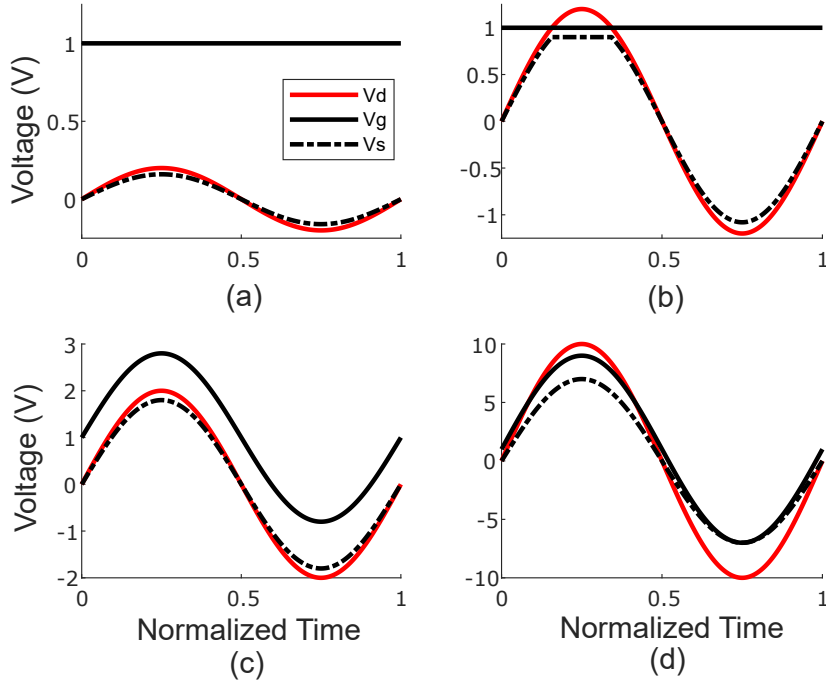


Figure 2.2: Illustration of compression with (a) $R_g = 0$, small signal, (b) $R_g = 0$ large signal, (c) $R_g \gg 0$, conduction, and (d) $R_g \gg 0$ compression

When Z_g is purely resistive, to realize the largest modulation voltage on the gate, the product of $\omega_m C_g R_g$ must be small. To ensure that the gate voltage is swinging in phase with the drain and source voltage at the carrier frequency, the product of $\omega_c C_g R_g$ must be large. Therefore, both the conditions for carrier and modulation voltages suggests that (2.13) is only satisfied if either the input power is low, or the modulation frequency

is low, but not both. Fig. 2.2 shows the compression mechanism in the cases when R_g is low, and when R_g is high, where $V_{g,m}$ is chosen to be a DC offset and time is normalized to one period for illustration purposes.

To demonstrate the trade-off between modulation bandwidth and P_{1dB} in conventional high-power RF switch design, we can define the fractional bandwidth, $FBW = 100 \cdot F_{mod}/F_c$. For the purposes of this analysis, the center frequency is taken to be 1 GHz. Fig. 2.3 uses (2.16) from (2.2)-(2.12) rather than the assumptions made in (2.14) and (2.15) to plot P_{1dB} contours for different values of R_g and FBW. Note that the power handling can reach 30 dBm only when the modulation frequency is quite limited, i.e. less than 10% FBW.

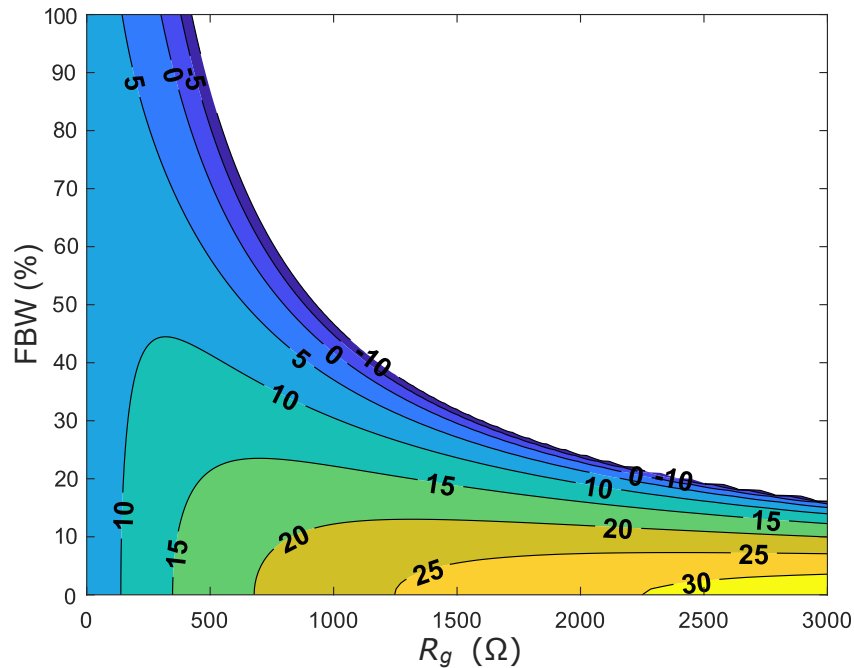


Figure 2.3: Contours of maximum power handling in dBm while sweeping modulation frequency and gate resistance for a 1 mm switch.

2.1.2 Conditions for Off-State Conduction

While adding a large resistance on the gate of the a switch allows it to remain in the on state to very high power, there are multiple conditions for the switch to remain in the OFF state with increasing input power. First, V_{gs} should remain less than the voltage threshold during the positive gate swing.

$$|V_{g,c} - V_{s,c}| - |V_{g,m} - V_{s,m}| < V_{th} \quad (2.18)$$

Second, the switch should remain off during a negative swing on the gate.

$$|V_{g,c} - V_{d,c}| - |V_{g,m} - V_{d,m}| < V_{th} \quad (2.19)$$

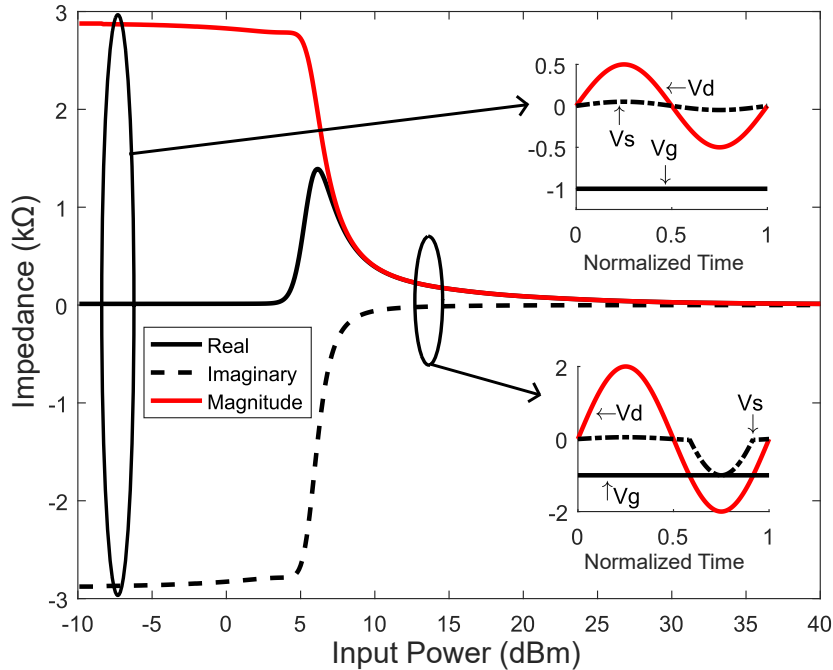


Figure 2.4: Simulated large signal input impedance of a $100 \mu\text{m}$ switch with $R_g = 0$ and illustrated waveforms for small and large signal operation

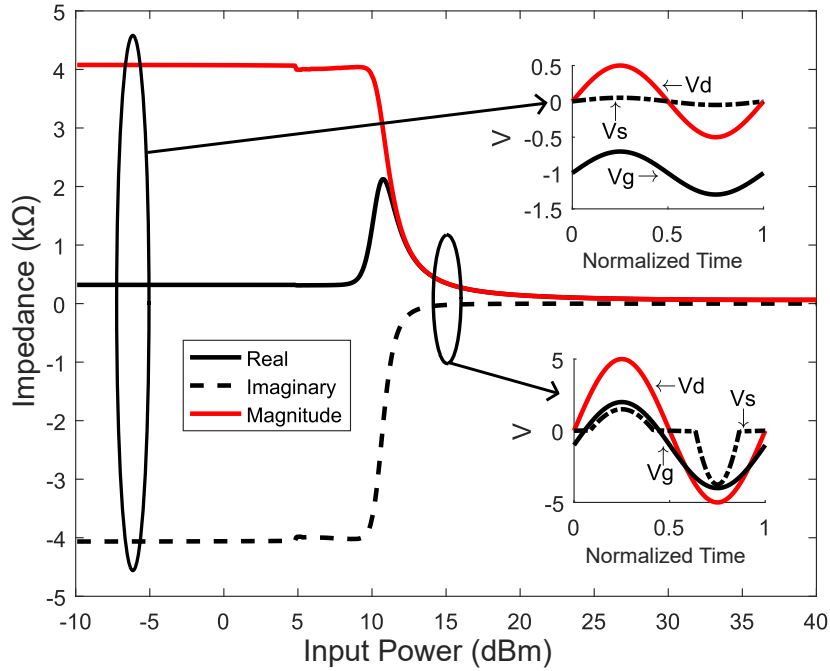


Figure 2.5: Simulated large signal input impedance of a $100 \mu\text{m}$ switch with $R_g = 15K\Omega$ and illustrated waveforms for small and large signal operation

Note that the only difference between (2.18) and (2.19) is that one is dependent on the source voltage and the other on the drain voltage. These compression mechanisms are illustrated in Fig. 2.4 for a small gate impedance and Fig. 2.5 for a large gate impedance. Therefore, the switch can be operated to around 5 dBm under this condition. With a large gate impedance, positive gate swing will always occur as the input swing approaches the gate bias voltage.

Negative swings compress the switch when the voltage division generating $V_{g,c}$ is no longer sufficient to keep $V_{g,c}$ below $V_{g,d}$. With a large gate impedance, the compression of the device in the off state serves to prevent the device from experiencing high breakdown voltages, as opposed to low gate impedance devices which will experience high gate stress beyond 10 dBm. However, in both cases, the large signal input impedance drops significantly with higher input power and the isolation drops from $>30\text{-dB}$ to $<3\text{-dB}$

rapidly.

Comparing Fig. 2.6 to Fig. 2.3 highlights the limitations of SPDT switches using only one device connected to each output, as the ON state is able to withstand very high power handling and modulation bandwidth, while the OFF state is limited severely by low compression points and low isolation. The solution to this discrepancy is to stack the FETs to distribute the voltage across many gates and increase the power handling of total switch. This technique will be discussed in detail later.

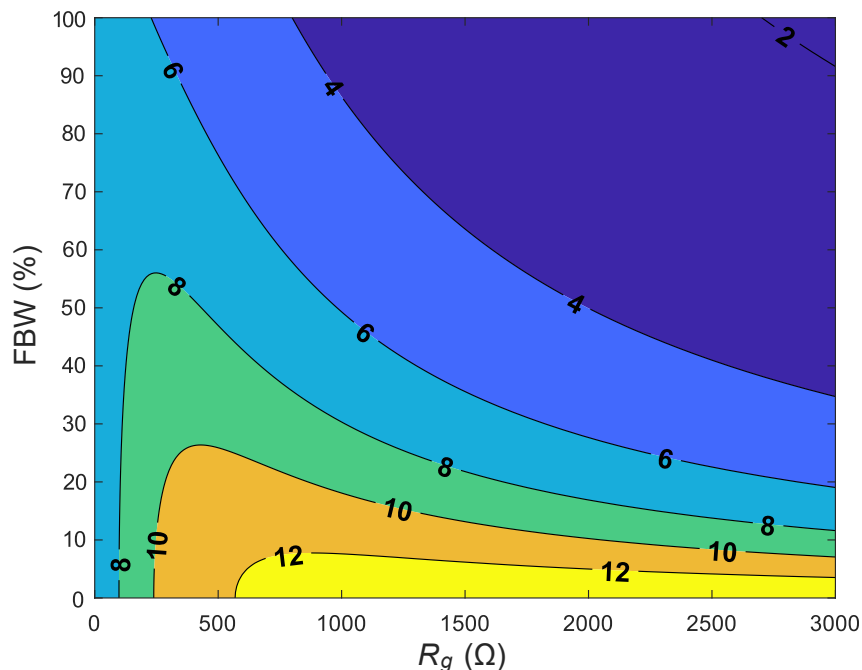


Figure 2.6: Contours of maximum power that satisfy (2.18) and (2.19) across F_{mod} and R_g for a 1 mm switch

2.2 Extension of Fractional Bandwidth

To break the trade-off between P_{1dB} and FBW, the resistive gate termination must be generalized to an arbitrary impedance. When an inductance is added to the gate, a

different impedance is presented at the carrier frequency and the modulation frequency. Looking back at the approximations when $R_{on} = 0$, it is easy to see how this might be effective as eq. 2.14 is now proportional to $1/\omega_m^2$, while (2.15) remains constant for sufficiently large $\omega C_g Z_g$ products.

In Fig. 2.7, the maximum power handling and modulation frequency possible is much higher compared to the resistive switch. Since the inductive element on the gate can store energy near the resonant frequency with the gate capacitance, the voltage across the gate can be high and cause device breakdown. The region around FBW = 20% exists due to this resonance where the peak gate voltage exceeds 2 V. This undesirable region indicates that the maximizing the P_{1dB} -FBW requires both a resistive and inductive element - the inductive element will allow high modulation bandwidth, while some resistance would prevent the gate from resonating.

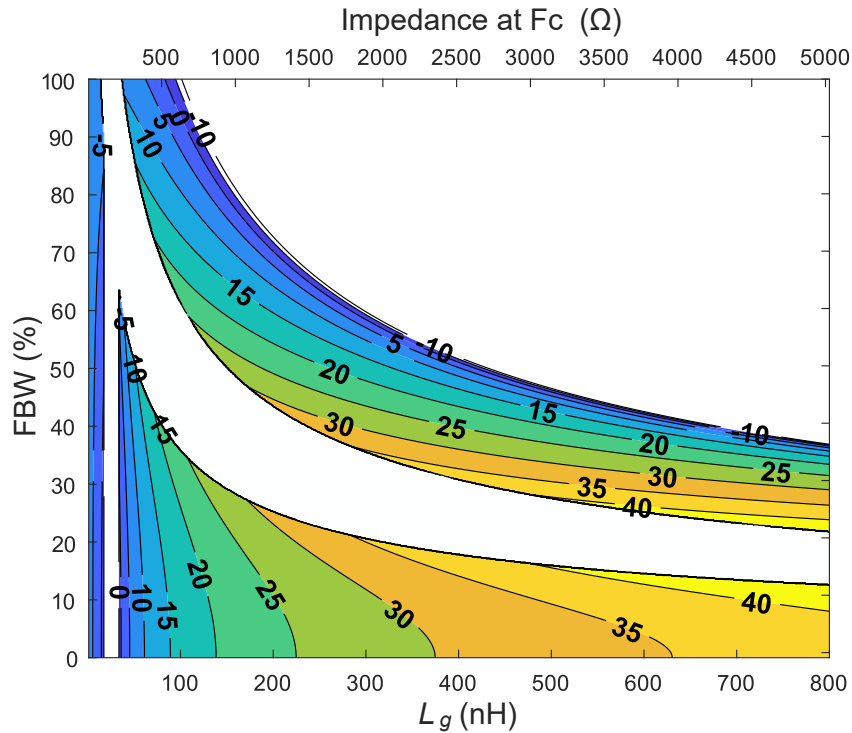


Figure 2.7: Contours of maximum power handling while sweeping modulation frequency and gate inductance for a 1 mm switch in the on state.

To simulate an arbitrary gate impedance, $Z_g = R_g + j\omega L_g$, Fig. 2.8 plots the resistive and inductive parts of Z_g for contours of FBW at 30 dBm power handling, insertion loss under 1-dB, and gate voltage less than 2 V. An interesting feature of this plot is the vertically-divided regions where the FBW jumps by nearly a factor of two between R_g values of 300 Ω to 400 Ω . This represents the required R_g necessary to suppress the resonance region such that the 30 dBm power is reached without causing device breakdown. While this shows a great improvement in FBW for high power handling in the switches, the off state will still be the limiting factor in evaluating the switches performance as the compression mechanisms are the same as outlined in the previous section.

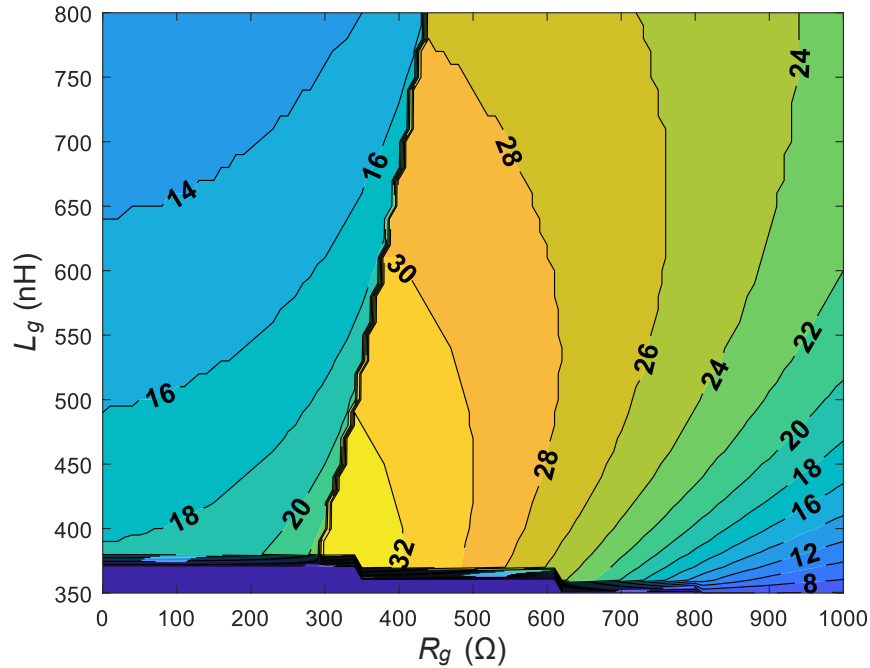


Figure 2.8: Contours of maximum modulation frequency as a fraction of the carrier frequency under the condition that (13) is satisfied up to 30 dBm with an insertion loss less than 1-dB.

2.3 SPDT design

To evaluate the performance of the switch, there are several important factors to consider. By looking at the switches in an SPDT configuration rather than as a single switch, both the on and off compression points can be evaluated simultaneously. Similarly, a low isolation value from the off switch will cause an increase in insertion loss in the on switch. As discussed in section 1.2 typical evaluation of individual devices, e.g. $\frac{1}{2\pi R_{ON}C_{OFF}}$ isn't sufficient to characterize an RF switch and all of it's parameters. To capture the effects of insertion loss, FBW, power handling, and drive power consumption, the following figure of merit can be used, as mentioned in Chapter 1,

$$FOM = FBW \cdot P_{1dB} \left(\frac{P_{in}}{P_{lost} + P_{drive}} \right) = \frac{FBW \cdot P_{1dB}}{(1 - IL) + \frac{P_{drive}}{P_{1dB}}}$$

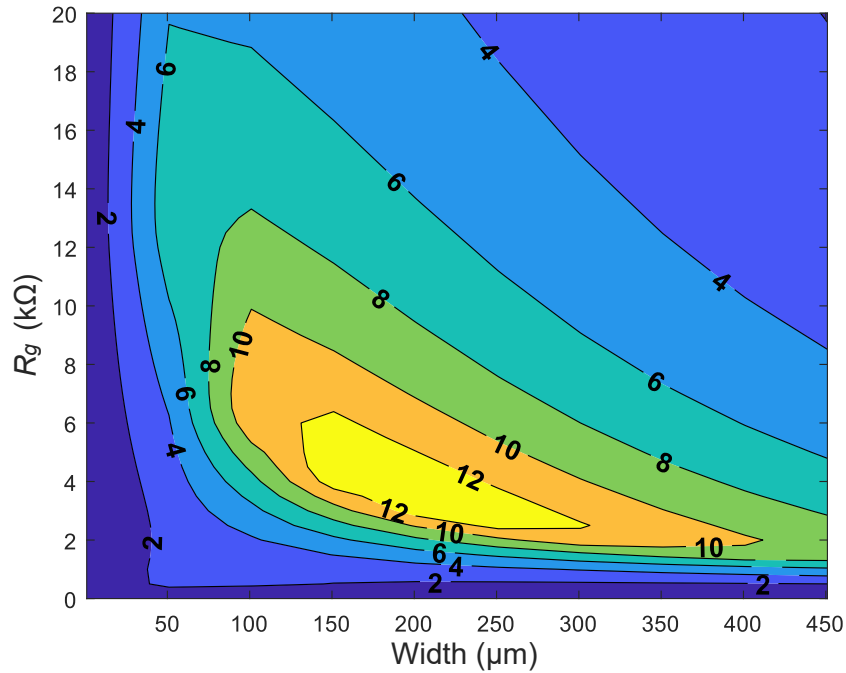


Figure 2.9: Calculated FOM across a sweep of switch width and R_g for a simple SPDT

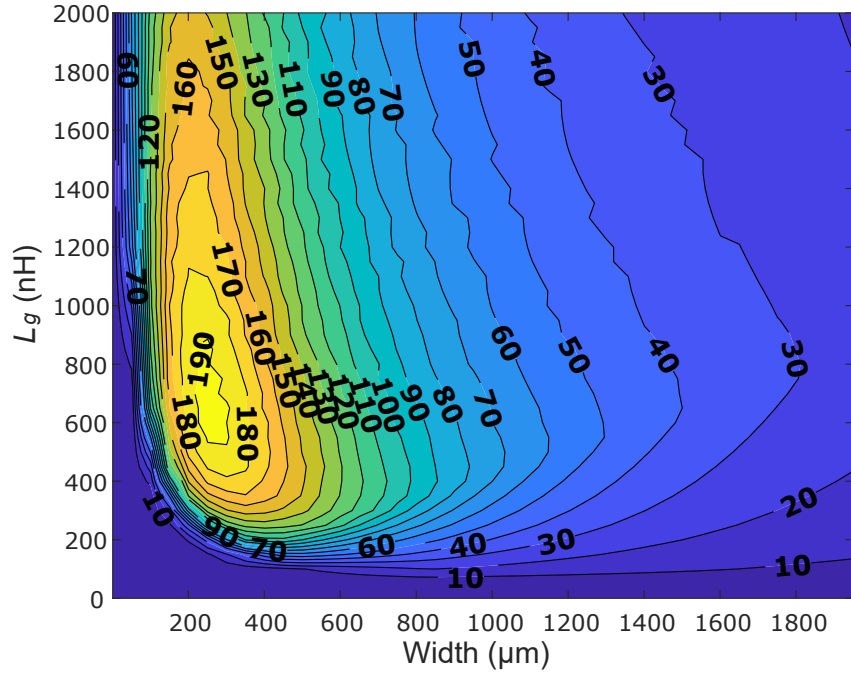


Figure 2.10: Calculated FOM across a sweep of switch width and R_g for a simple SPDT

The FBW and IL are linear, unitless values while all power values are in units of Watts. The FOM is specified such that an increase in FBW or P_{1dB} cannot be accompanied by a corresponding increase of insertion loss to create the illusion of an improved system. By considering the fractional value, $P_{in}/(P_{lost} + P_{drive})$, the net system efficiency is also evaluated. In CMOS processes, the drive power is typically small and does not strongly impact FOM. However, other processes might handle higher power with higher gate dissipation. Figure 2.9 calculates the FOM across a sweep of switch width and gate resistance to find the optimal parameters of the device that balance modulation speed and power handling.

Similarly, the same set of equations and FOM can be used to evaluate an SPDT with an inductive gate element and a 300Ω damping resistance on the gate. This optimization is shown in Fig. 2.10 and the benefit of using the inductive termination is immediately

apparent. Due to the relaxation of the FBW limitations from the inductive gate, the total gate impedance can be increased without degrading FBW and in turn improves both power handling and insertion loss for a significantly higher FOM.

2.4 Stacked FET Design and Optimization

The previous analysis demonstrates that raising the load impedance on the off switch might help prevent voltage compression. With a larger load, the input impedance seen into the open switch is higher, leading to more isolation, and the output voltage swing will be able to track the gate voltage more closely leading to a higher compression point. Adding series 'stacks' of switches increases the cascaded Z_{in} at each transistor towards the source.

2.4.1 Resistive Stack Optimization

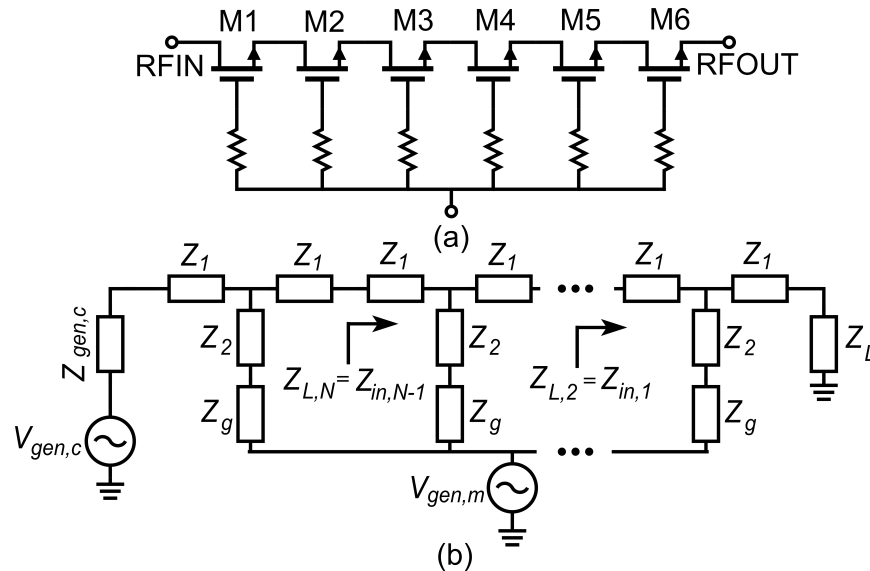


Figure 2.11: a) Schematic of a stacked FET switch with resistive gates and b) stacked FET switch circuit model to calculating impedance and isolation

A circuit schematic of this approach is illustrated in Fig. 2.11(a) and the equivalent

model as previously discussed in section II is shown in Fig. 2.11(b). The compression point of the switches is predicted from eqs. 2.18 and 2.19 by checking each switch in the stack to determine if compression has occurred. Beyond the compression point, the large signal behavior is approximately modeled by assuming $V_s = V_d - V_{th}$ given that R_g is sufficiently large. Since V_s and V_d are determined by the combination of circuit parameters including R_{sw} , if V_s and V_d are known a priori, the equivalent large signal R_{sw} can be determined. This process is used to generate Figs. 2.12 and 2.13.

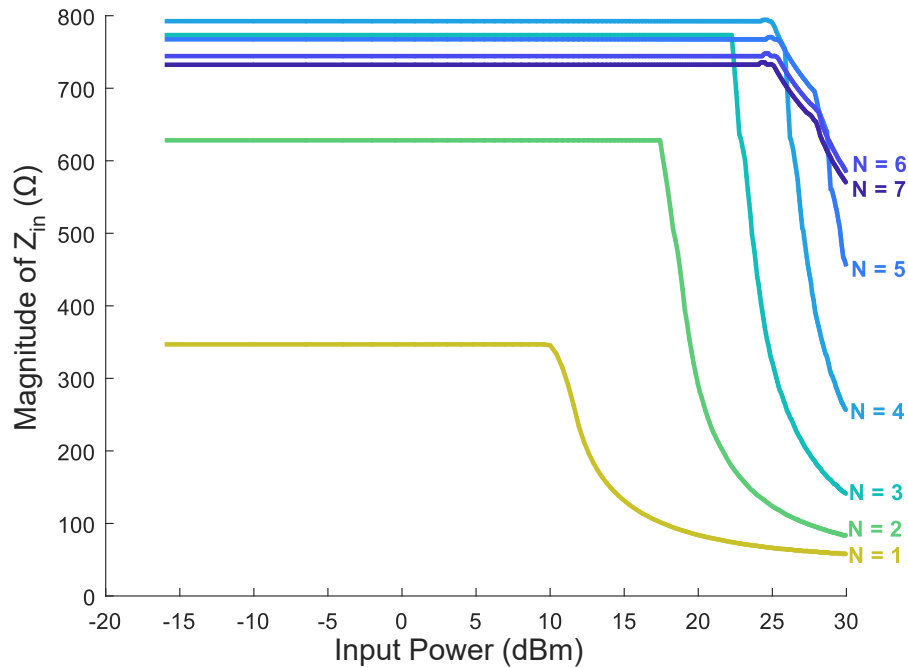


Figure 2.12: Z_{in} with increasing input power for N stacked FETs for 1 mm FETs with $R_g = 1500 \Omega$.

In the case of Fig. 2.12, a relatively small value for R_g was chosen to maintain high modulation bandwidth. The Z_{in} of each additional transistor increases to $N = 4$ before the benefits of stacking begin to diminish largely due to the accumulating parallel gate resistances. Increasing the value of R_g to $20 \text{ k}\Omega$ rather than $1.5 \text{ k}\Omega$ leads to Fig. 2.13, which shows that by sacrificing some modulation speed with a larger R_g , the use of FET

stacking remains viable for larger values of N and input power.

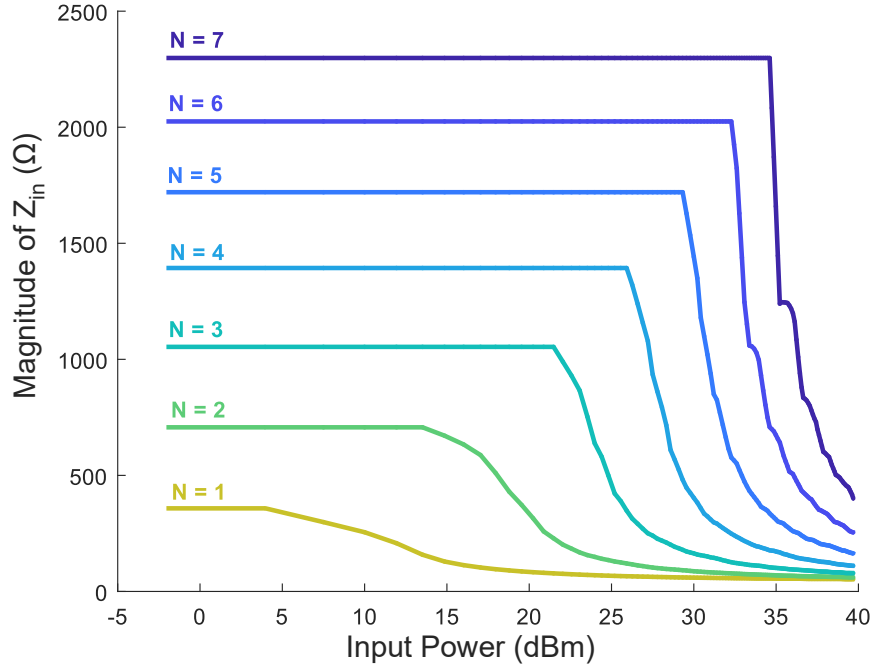


Figure 2.13: Z_{in} with increasing input power for N stacked FETs for 1 mm FETs with $R_g = 20 \text{ k}\Omega$.

This result suggests an optimization in the number of stacked devices for higher power handling and maintaining modulation bandwidth. Revisiting the FOM in (1.3), P_{drive} increases by a factor of N to take into account the total power consumption of the stacked FETs. Again, using the SPDT model to ensure that both on and off compression, as well as IL and isolation are captured, any standard maximization algorithm can be used to determine the optimum values for N , switch width, and each individual gate resistance.

The FOM comparison is plotted in Fig 2.14 as a function of N . The corresponding P_{1dB} , IL, and maximum FBW are also plotted. The simulation indicates that the FOM is maximized between $N = 5$ and 7 FETs while $N = 7$ has the highest (>1 Watt) power handling. For $N = 6$, a 30 dBm switch is realized with width = $935 \mu\text{m}$, $R_{g1} = 4300 \Omega$, $R_{g2} = 6200 \Omega$, $R_{g3} = 5500 \Omega$, $R_{g4} = 5600 \Omega$, $R_{g5} = 5800 \Omega$, $R_{g6} = 4800 \Omega$. The tapering

of the gate resistance is performed to balance the load voltage on the switch.

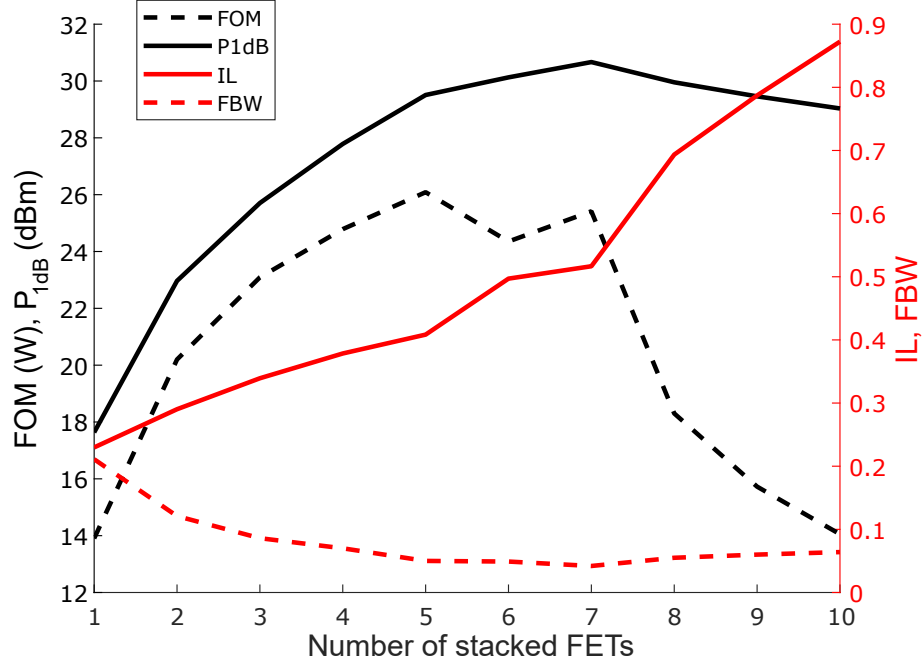


Figure 2.14: Optimization of the number of stacked FETs and their parameters.

2.4.2 Inductive Stack Implementation

While a resistive stack can easily be integrated, developing a stacked switch with an inductive termination relies on prohibitively large numbers of inductors. Even if these inductors are moved off chip, the number required for any number of stacked FETs would be layout intensive as each transistor would need a separate inductor.

A solution is to modulate the gate impedance of the stacked FETs using a secondary stack of switches, first proposed in [36], and displayed here in Fig. 2.15. While this switch was originally proposed as a shunt switch, it is also converted to a series switch by using a large inductor on the control line in the spirit of section II-C. When the control voltage is high, the gate of the first NMOS device and the source of the first PMOS device are

biased high, turning both of the switches on. This allows the control voltage to propagate to the next stack in the ladder and so on, cascading up the switch. When the switch is on, all the gates of the primary devices, A_1 through A_N , are tied together to make one large device with a composite gate length. This also makes the gate capacitance N times larger than each individual device which allows the size of the control inductor to be greatly reduced.

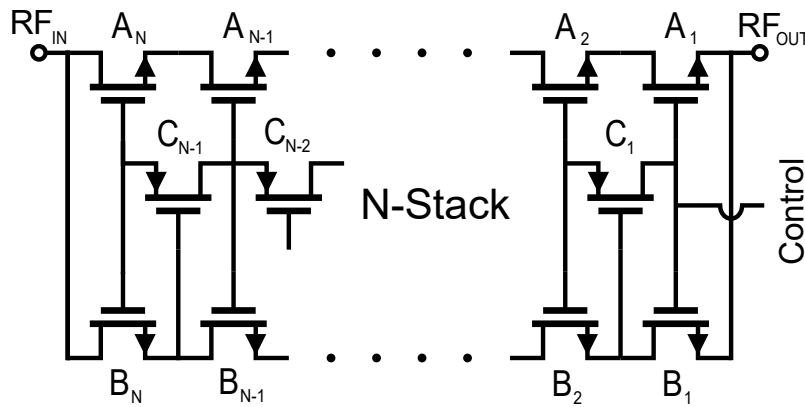


Figure 2.15: Modified stacked switch to enable fast switching through an inductive gate impedance in series with the control node. This architecture can also be used in a shunt configuration

When the switch is turned off, each secondary switch presents a large capacitive impedance to the gate of each primary switch. Typically, a purely capacitive gate impedance prevents any modulation from occurring, particularly if the data has a DC offset. In this case, the switches are turning on and off, presenting alternately small resistances and large capacitances.

Assuming a static capacitive load on each gate of the device, the same process used to generate Figs. 2.12 and 2.13 can be used to generate Fig. 2.16. In this case, since each capacitor is cascaded on top of the next capacitor on the stack, the effective impedance seen on each gate NC_{ds} at the N th FET, with A_1 seeing the largest impedance and A_N the smallest. Conveniently, this trend breaks the trade-off that was evident in Figs. 2.12 and 2.13 in that progressive stacks continue to add power handling capabilities without

compromising the maximum FBW.

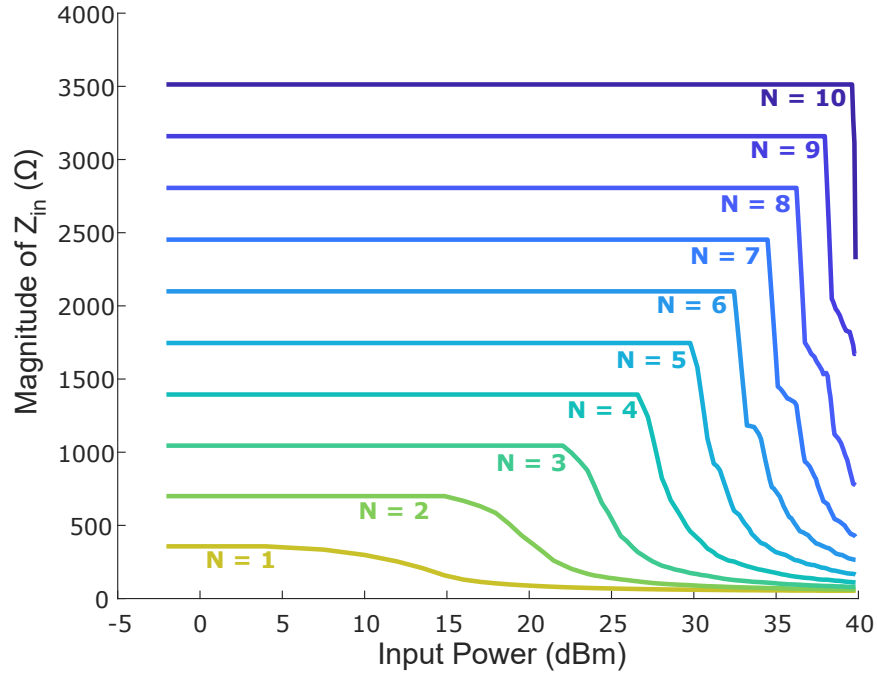


Figure 2.16: Input impedance with increasing input power in the off state for different numbers of stacked switches for the design in Fig. 2.15 approximating the gate impedance as the capacitance from the total cascade of the secondary transistors below each switch

2.5 Shunt Switches

The ladder switch design shown in Fig. 2.15 can also be used in a shunt configuration for various applications. In this case, the control node does not need any termination and can be driven directly from digital logic. Digital logic can be used in the ON state because the RFIN node will be shunted to ground and have zero voltage swing, while in the OFF state, the RFIN voltage is distributed between each of the switches.

To significantly improve the voltage handling of these types of switches, a tapering approach to the secondary switches (B and C) is proposed here. Typically, power han-

dling is limited by self conduction when the switch is OFF. This is caused by the drain of A_1 swinging while the gate of the device is connected to the DC-grounded control line. In order to prevent the bottom most devices from conducting in the OFF state, the voltage swing at the drain of A_1 must be less than the threshold of the device. In addition, if the voltage drop across each transistor is to be approximately the same, the voltage division from the drain to the gate of each consecutive device must be a smaller fraction of the total remaining incident voltage. This means that the bottom secondary devices (B_1, C_1) must be the largest and the top secondary devices (B_N, C_{N-1}) must be the smallest while the size of the primary devices ($A_1 \rightarrow A_N$) remain the same to ensure the highest voltage handling. Conversely, adding stacks with increasingly aggressive tapers has a significant impact on the achievable FBW. To describe this trade-off, a tapering function can be defined as

$$B_N = C_N = \frac{A_N}{N^x} \quad (2.20)$$

with A_N , B_N , and C_N representing the size of the N^{th} device in the respective stacks as labeled in Fig. 2.15 and x representing the tapering factor.

Fig. 2.17 shows the simulated P_{1dB} of tapered stacked shunt switches with different numbers of stacked devices and increasingly aggressive device tapering factors. To maintain a constant switch resistance, the size of the primary devices, A is scaled linearly with the number of stacked devices. Adding a taper to the switch, $x = 1$, the power handling of the shunt switch is improved by 15-20 dB over a switch with uniform sizing, $x = 0$ at high numbers of stacked devices. Using more aggressive tapering, e.g. $x = 2$, further increases the P_{1dB} but additional tapering provides limited benefits.

Conversely, increasing the number of stacks adds both additional gate capacitance, due to more devices in the stack and larger devices to keep the switch resistance low, and series resistance in the control line which also increases with the tapering factor. As

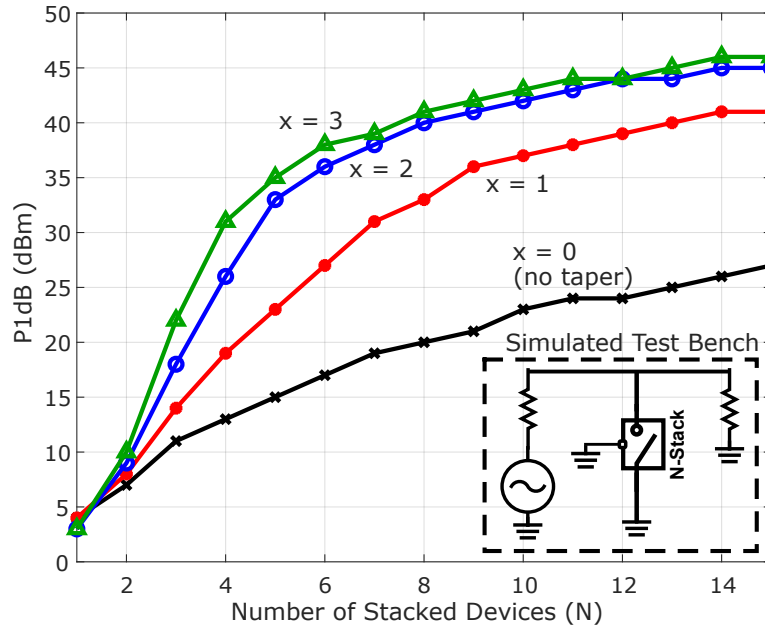


Figure 2.17: Effect of device stacking and tapered switch sizing for different tapering factors, x , on switch power handling.

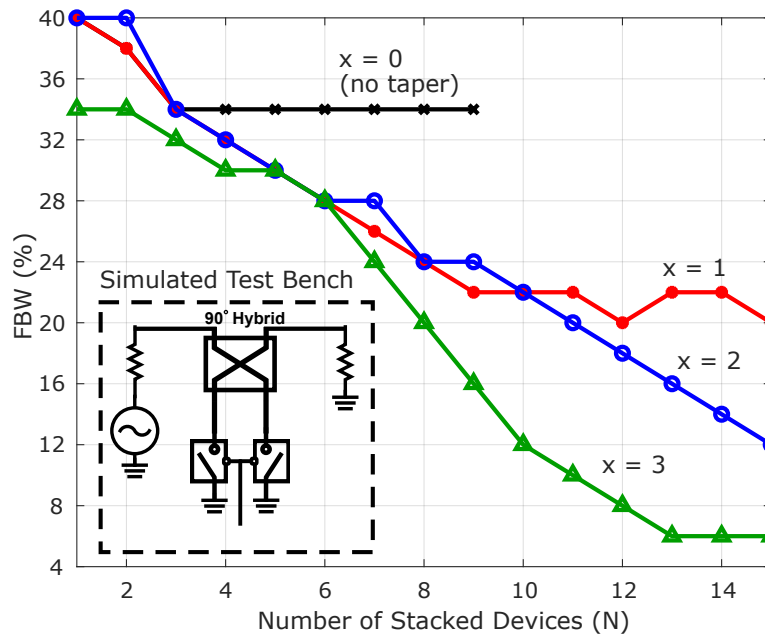


Figure 2.18: Effect of device stacking and tapered switch sizing for different tapering factors, x , on maximum achievable FBW.

a result, the switching speed is reduced. To quantify the trade-off in the additional gate capacitance, the FBW is plotted in Fig. 2.18 for increasing stacks and tapering factors.

The test-bench uses a reflection phase shifter (RPS) so that both the on and off state have similar losses to the output and switching speed is isolated from other variables. The implementation of this RPS will be discussed later in Chapter 3. In this case, the maximum FBW is defined as the switching frequency at which the losses increase by 1 dB. Without a taper in device sizing ($x = 0$), increasing the number of stacked devices beyond 9 requires very large devices to maintain low switch resistance, which results in a low input impedance in the off state due to C_{SW} and modulation becomes impossible in the RPS test bench shown in Fig. 2.18. Adding the tapering function allows modulation at high values of N and thus higher power handling concurrent with modulation. From Figs. 2.17 and 2.18, the design trade-offs between power handling and FBW are clear - larger N leads to more power handling but lower maximum FBW. Ultimately, using the same tapering factor in both the B and C devices is not ideal as it is better to have larger C devices to keep the series resistance down for higher FBW.

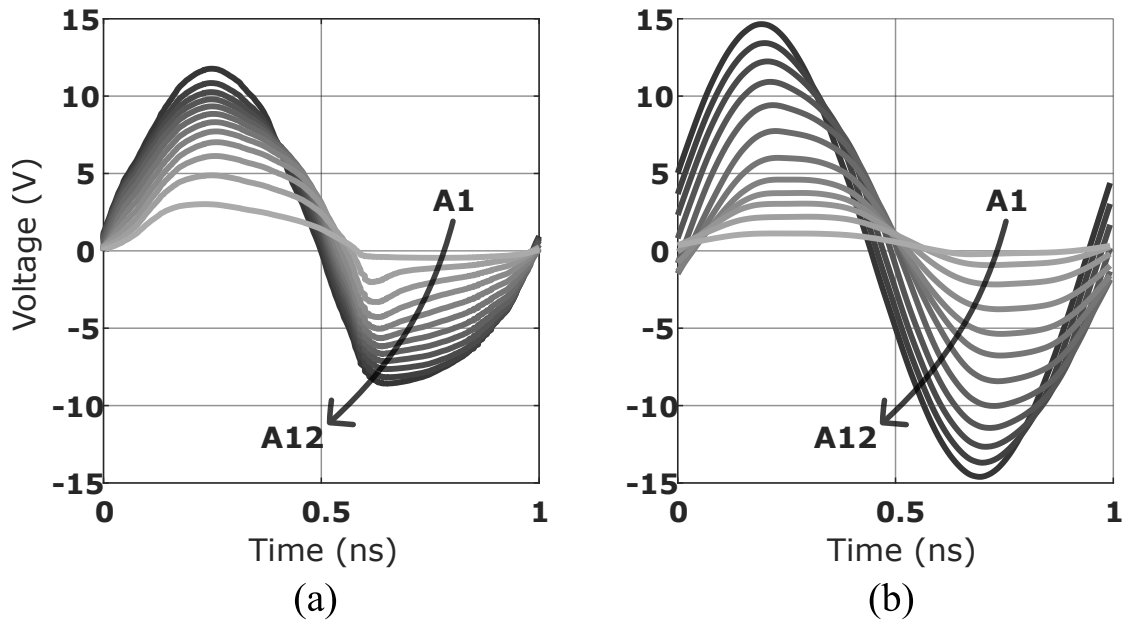


Figure 2.19: Drain voltages for a RPS in the OFF state with a 30 dBm input when the switches are sized with (a) static sizing, and (b) a tapering technique.

To observe the effect of tapering at the internal nodes of the switch on the OFF state,

the simulated drain voltages for each primary (A) device are shown in Fig. 2.19 (a) for a 12-stack switch used in an RPS modulator where each of the B and C devices is $1/12$ the size of the A devices [36] - in this case, $150 \mu\text{m}$, and Fig. 2.19 (b) for a tapered 12-stack switch. The voltages across the FETs are more evenly distributed, allowing lower stress on each device and a significantly higher maximum voltage swing on the stacked switch. This leads to lower insertion loss and higher power handling.

Chapter 3

Stacked Switch Implementation in Power Modulators

Using the theory presented in the last chapter on RF switches, a variety of different styles of modulators for code-domain applications have been built and are presented in the following chapter. The first objective is to demonstrate the utility of the resistive switch optimization for building a modulator (modulator A) with the highest FOM possible. Next, a modulator (modulator B) utilizing the new type of inductively terminated RF switch will be presented to show how the switching speed can be greatly improved over any type of resistive termination. Finally, a type of modulator (modulator C) which does not use any baluns will be discussed as a way to maintain high power handling and fractional bandwidth while significantly lowering the insertion loss for better system efficiency. The target center frequency for each of these modulators is 1-GHz.

3.1 Modulator A: Optimized Resistive Modulator

3.1.1 Design

Because CMOS is fundamentally limited by the voltage swing of the RF signal, one method to improve the linearity of the system is to lower the reference impedance of the system - lowering the voltage and increasing the current for the same total power. This approach has been presented previously in [37] and [38], however without considering the implications on the modulation speed of the switches. The downside to this approach is that the switch resistance becomes relatively large compared to the load resistance, offsetting the benefits in power handling through higher insertion loss. The switch resistance might subsequently be lowered by scaling the size of the switches with a proportional cost in the gate capacitance and power consumption. Examining eqs. (2.14) and (2.15), we find that both equations rely on a $\omega C_g Z_g$ product. If C_g increases, both the voltage handling and the maximum modulation frequency can be maintained by decreasing Z_g by the same factor. Due to the nature of (2.15) the gate voltage due to the carrier stays constant as long as the $\omega C_g R_g$ product stays constant. This leads to an optimum switch size determined by the point when R_g becomes small enough that the constant voltage across it burns enough power to offset any benefits from lowered R_{sw} .

While the power handling of the switch could in theory be extended well beyond 40 dBm by lowering the reference impedance, there is a practical limit on the impedance conversion ratio that is possible without adding insertion loss. For this design, the Anaren 3A425S is an appropriate down conversion balun with an output impedance of 12.5Ω referenced to ground on each of the differential ports. Re-optimizing with the methodology in chapter 2 gives the results in Fig. 3.1. The predicted P_{1dB} is now above 36 dBm with a peak FOM between 5 and 6 stacks. As the maximum power handling has increased by a factor of four, so has the FOM - indicating that by lowering the source

and load impedance to increase the power handling of the switch, none of the other important metrics have been negatively effected. This analysis assumes that the switch turns off completely once compression occurs. This technique predicts which switches will perform best, but, in reality, a softer compression occurs, so the actual measured compression point will be somewhat higher by a constant offset.

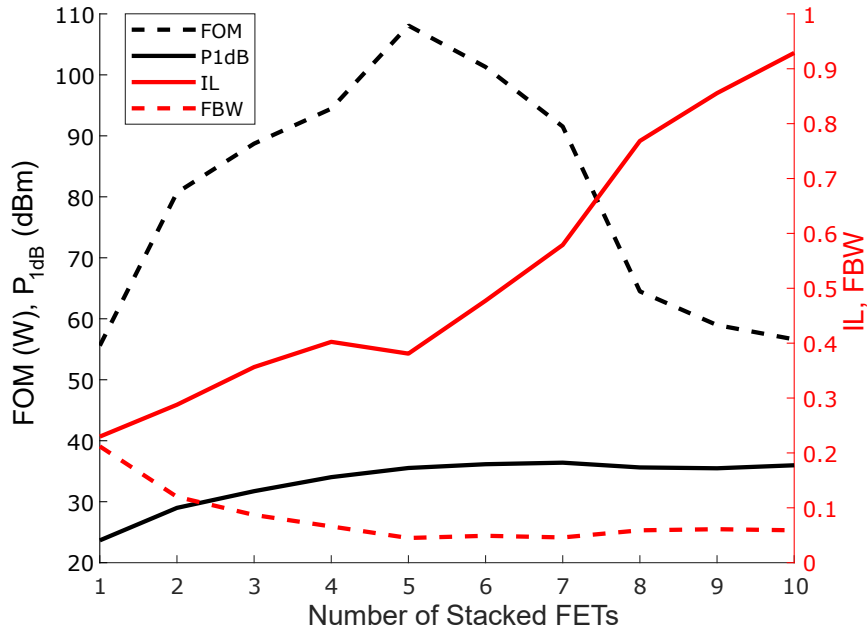


Figure 3.1: Optimization of the number of stacked FETs and their parameters.

Through this optimization for an $N = 6$ stack switch, the width of each switch in the stack is $3400 \mu\text{m}$ and the gate resistances range from $R_g = 1100 \Omega$ to $R_g = 1600 \Omega$. Transitioning to a device model requires some adjustments to reach a P_{1dB} of 40 dBm and a FBW of 0.05 at a small sacrifice in IL. Each transistor was sized to $3800 \mu\text{m}$, and $R_{g1} = 1600 \Omega$, $R_{g2} = 1200 \Omega$ and, $R_{g(3-6)} = 800 \Omega$. The simulated drain-source voltages are shown in Fig. 3.2 and demonstrate the reduction in the voltage stress on the devices.

Since much of the analysis up to this point relies on a gate voltage swing from -1 V to 1 V, a level shifter based on the the design outlined in [39] is used to translate basic 1 V

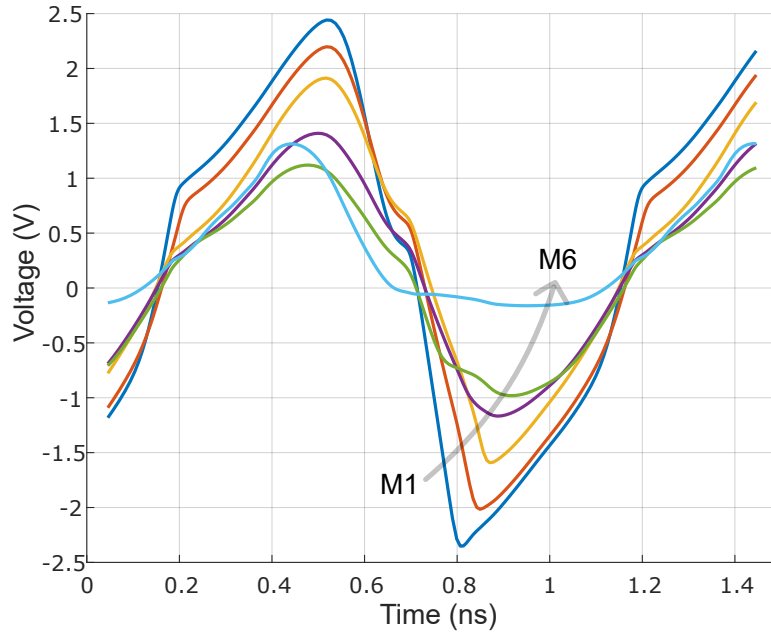


Figure 3.2: Simulated drain-source voltages of the resistive design operating at 40 dBm when the switch is off

CMOS logic up to a 0-2 V swing while the RF path is biased at 1 V. A shift register was included to enable data encoding if necessary, and the schematic of the constructed chip and PCB is shown in Fig. 3.3. Additionally, in anticipation of high power dissipation within the switch, tie-throughs from metal one connecting to the handle wafer through the BOX layer were interwoven within the device cells with the intention of aiding in thermal dissipation.

Within the differential section of the PCB, the inductive and capacitive elements are symmetrical both vertically and horizontally. $L1$ represents the wirebond inductance in the RF path. Because the characteristic impedance is low, any small additional wirebond inductance can cause large mismatches making evaluation of the switches difficult. To offset this wirebond inductance, the matching network consisting of $C1 = 10$ pF and $L2 = 1$ nH is used to minimize the losses. $L3 = 100$ nH and is used to bias the switches to 1 V. A close up of the wirebonded chip and the full test board are shown in Fig. 3.4.

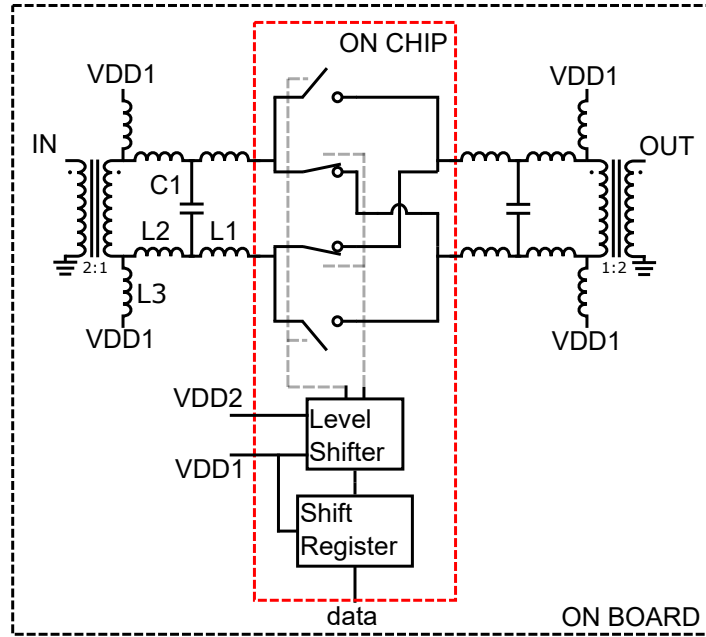


Figure 3.3: Schematic of chip and testing PCB for the Resistive gate, 40 dBm modulator

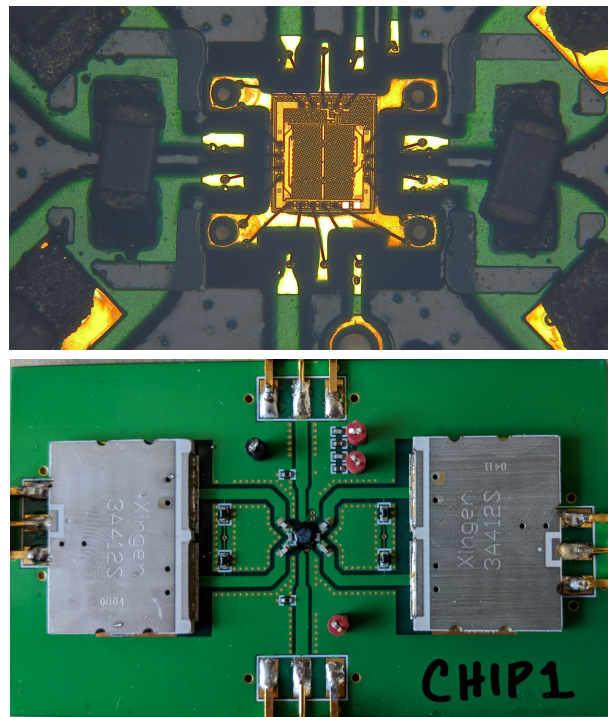


Figure 3.4: Die photo and test board for modulator A. The size of the modulator is 840 μm by 950 μm

Again, in order to de-embed the losses of the board, a version without the chip, but wirebonded directly across the chip landing area was also constructed.

Because the RF voltage is high, standard ESD cells cannot be used on the drain and source of the switches, and thus no ESD was implemented in this design. However, previous work [40] shows that ESD on the drain and source of stacked CMOS switches is possible without significantly degrading the performance of the switch.

3.1.2 Measurements

Measured and simulated S -Parameters for modulator A including the test board are shown in Fig. 3.5. The wire bond inductance was estimated at 500 pH when designing the test board and comparing the simulated and measured S -parameters indicates that the wire bond inductance is in this range though there are some additional losses.

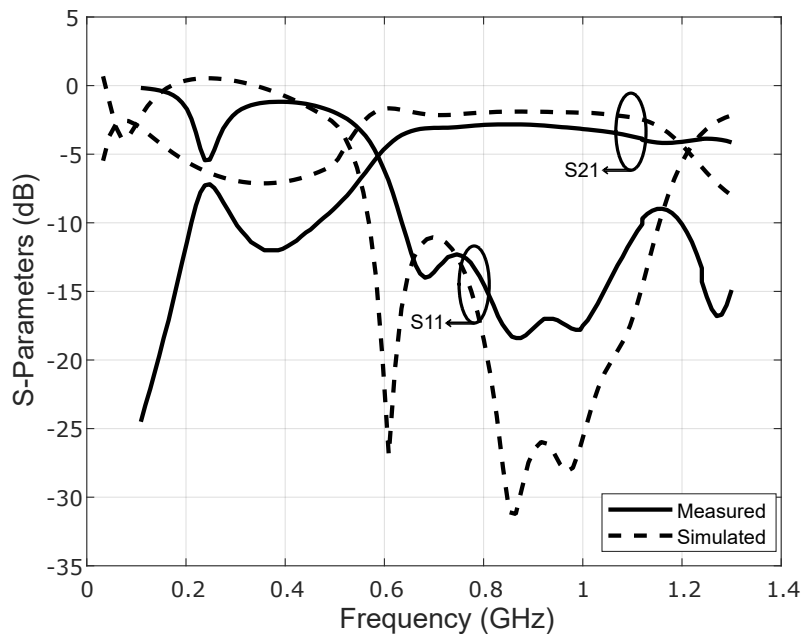


Figure 3.5: S -Parameters for modulator A including the test-board and baluns

The measured and simulated P_{1dB} of modulator A are plotted in Fig. 3.6. While

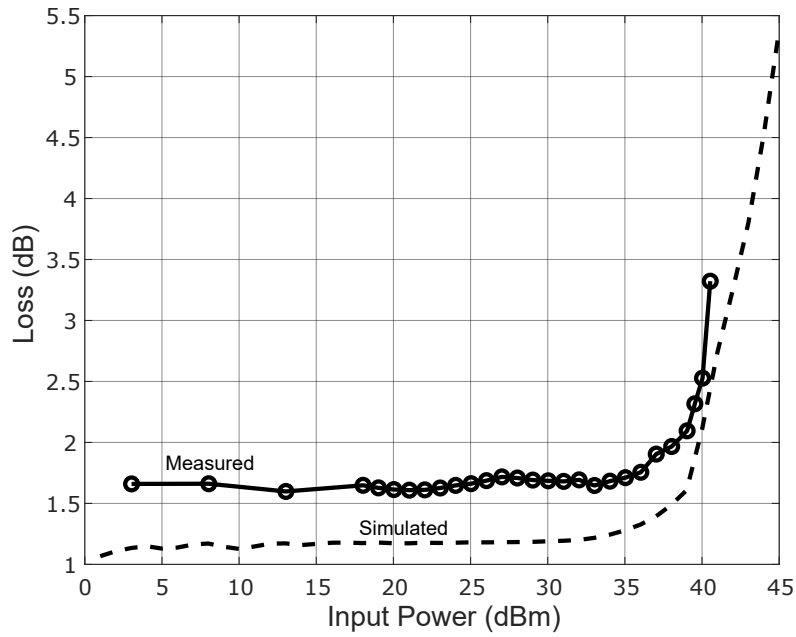


Figure 3.6: Compression of modulator A with increasing input power

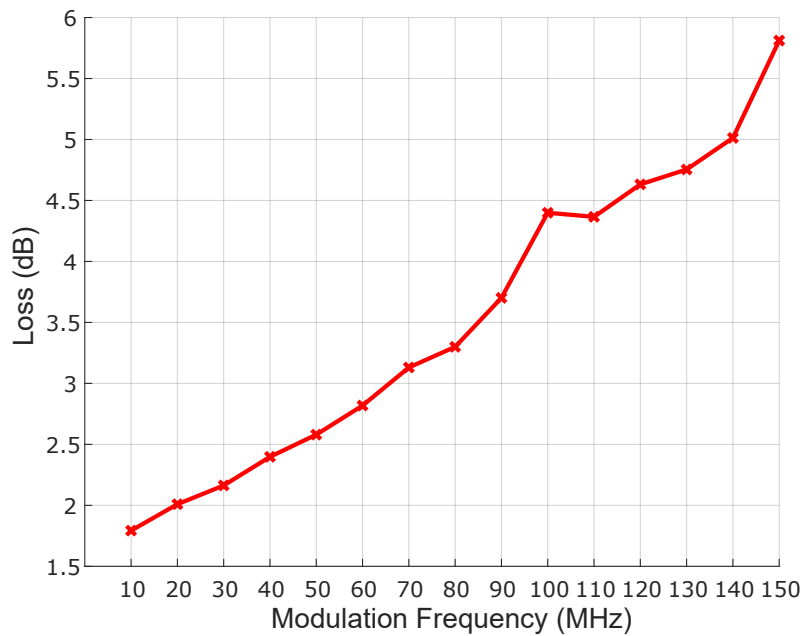


Figure 3.7: Measured loss with increasing modulation frequency for modulator A

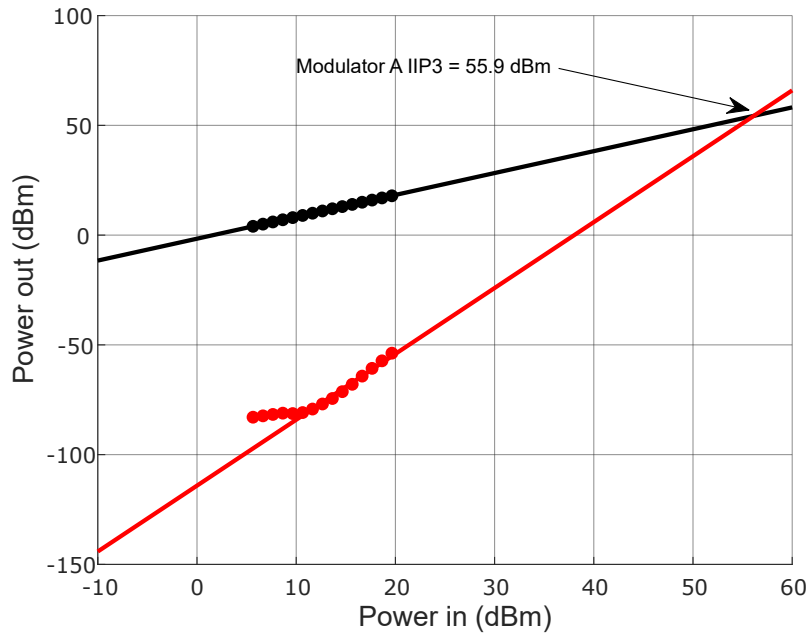


Figure 3.8: P_{in} vs. P_{out} and IM3 products to extrapolate IIP3 for modulator A at a 1 MHz offset

the insertion loss is slightly higher when measured compared to simulated, there is good agreement between the compression point which is 40.1 dBm. The measurement was conducted up to a maximum input power of 40.5 dBm. Beyond this point, the insertion loss will begin to degrade over time - gradually at first, then rapidly towards complete device failure. So long as the degradation continues to be gradual, if the input power is reduced slightly the device performance will recover to previous levels. This slow, non-catastrophic failure suggests that the switches are entering thermal run-away and that the temperature limits of the process have been reached. Simulating loss vs. temperature for modulator A indicates that the the loss gradually increases by 1dB of loss at 360°C before quickly rising to almost 20 dB at 400°C supporting the theory that thermal run-away is occurring in the switches. Because voltage compression and thermal compression occur around the same input power, it is difficult to evaluate the effect of modulation frequency on P_{1dB} . As the modulation frequency increases from 0 to 60 MHz, the compression

TABLE II
IIP3 MEASURED VS. TWO-TONE OFFSET

Offset (MHz)	1	5	20	40	60	80	100
IIP3 (dBm) Modulator A	55.9	55.9	56.2	56.5	56.7	57.2	55.7

point decreases from 40.1 dBm to 38.7 dBm. Additionally from Fig. 3.7 it's clear that the insertion loss increases relatively rapidly with modulation frequency. Therefore it's unclear if the reduced compression point at higher modulation frequency is due to higher insertion loss and thus higher temperature, or because of the effect of modulation frequency in eq. 2.16. Finally, IIP3 was measured for modulator A and is plotted in Fig. 3.8 which shows an IIP3 of 55.9 dBm in a two-tone test at a 1 MHz offset. A sweep of Two-tone offset and corresponding IIP3 is shown in Table II.

3.2 Modulator B: Ladder Inductive Modulator

3.2.1 Design

Modulator B uses the ladder switches with an inductive termination as described previously in section 2.4.2. Each RF switch is composed of a back to back set of ladder switches with their control lines connected together. This allows each switch to look like a shunt switch when in the off state as the differential configuration will cause a virtual ground at the center of the back to back switch. This is illustrated in fig. 3.9 (b). The inductive termination is then shared between the two back to back switches allowing for only 4 off-chip inductors used with the modulator.

The sizing of modulator B for each of the primary and secondary switches in this design were based on previous results in [36] with the primary switches 600 μm in width and the secondary switches 50 μm wide. This sizing is sufficient to demonstrate the inductive concept, however, subsequent simulations suggest that much larger switches

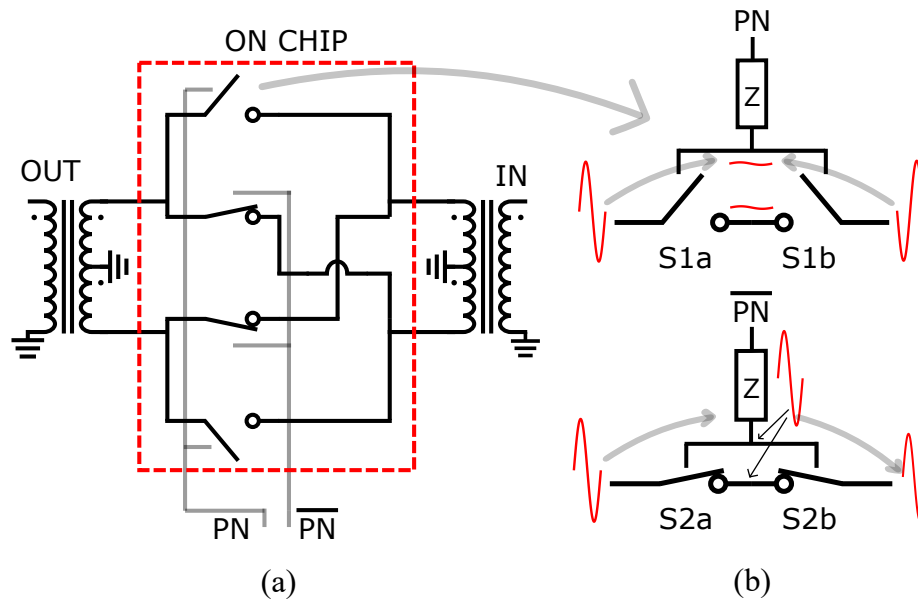


Figure 3.9: Modulator design with the chip edge shown (a) and the use of back to back switches to create a virtual ground (b) in modulator B.

in a lower impedance environment would allow for better performance as well as full integration with smaller inductors.

When this modified stacked switch is on, the secondary switches tie the gates of all the primary switches together leading to an equivalent gate capacitance of $12C_g$ for back to back switches consisting of 6 stacks each. For a switch this size, a gate resistance in the range of $50 - 100\Omega$ is necessary in addition to a gate inductance of $50 - 100$ nH. To provide the necessary resistance for each of the gate elements, long, low-level metals were used to route the gate connections to the I/O pads such that the resistance is $\sim 70\Omega$. The simulated drain-source voltages of the switches in the off state are shown in Fig. 3.10.

The chips were wirebonded to a PCB with two surface mount ATB 2012E-50011M baluns and four high impedance components - one for the control input of each series-series switch. Two versions of this modulator were constructed to provide a direct com-

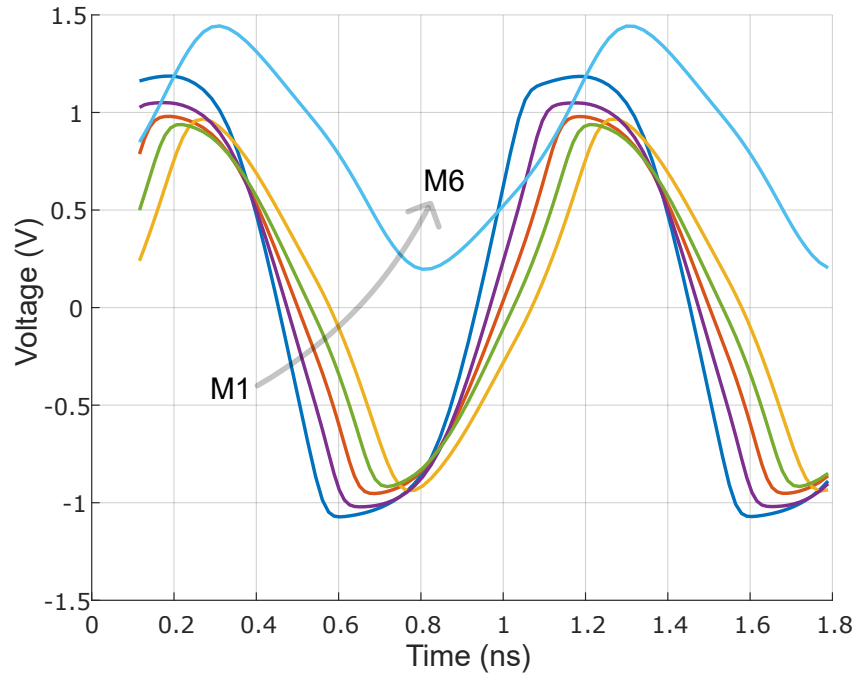


Figure 3.10: Simulated drain-source voltages of the inductive design operating at 30dBm when the switches are off

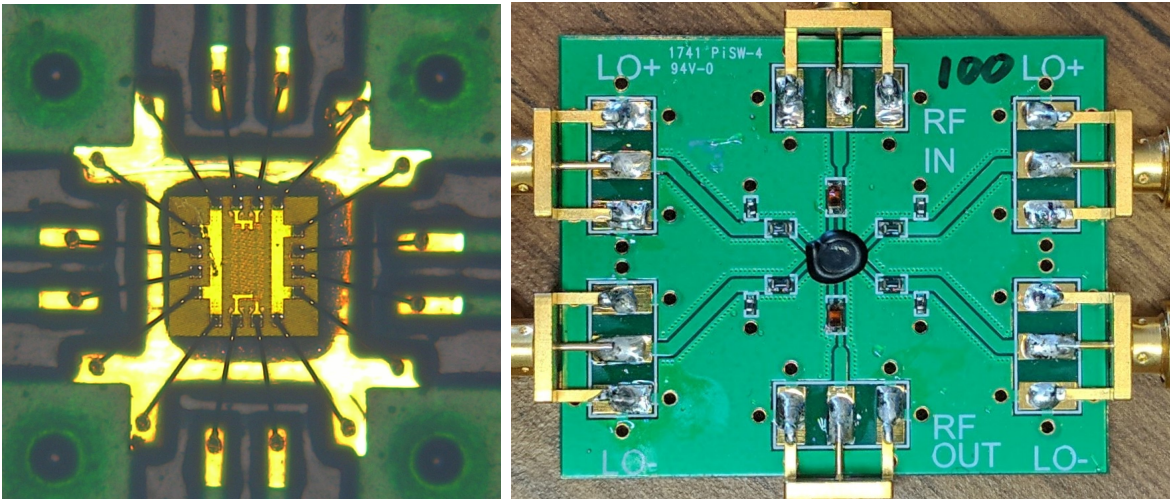


Figure 3.11: Die photograph and constructed PCB for modulator B. The total size of the die is $570 \mu\text{m}$ by $640 \mu\text{m}$. Four 100 nH inductors are placed horizontally with the baluns on the top and bottom

parison for FBW: one with resistive elements and one with inductive elements. The resistive version was mounted with 800Ω terminations while the inductive version was

mounted with 100 nH TDK-B82496C inductors. The mounted chips are shown in Fig. 3.11. A back-to-back balun version of the PCB was also constructed in order for the baluns to be de-embedded so that the insertion loss of the switches themselves could be determined.

3.2.2 Measurements

S -parameters of both the resistive and inductive version of modulator B are plotted in Fig. 3.12. The small signal insertion loss is 2.6 dB for the inductive version and 2.9 dB for the resistive version. Of this loss, 1.8 dB is contributed by the back-to-back balun and test board and the total switch loss is less than 1.1 dB. Above 1.3 GHz, the loss of the switch cannot be evaluated due to the balun cutoff frequency.

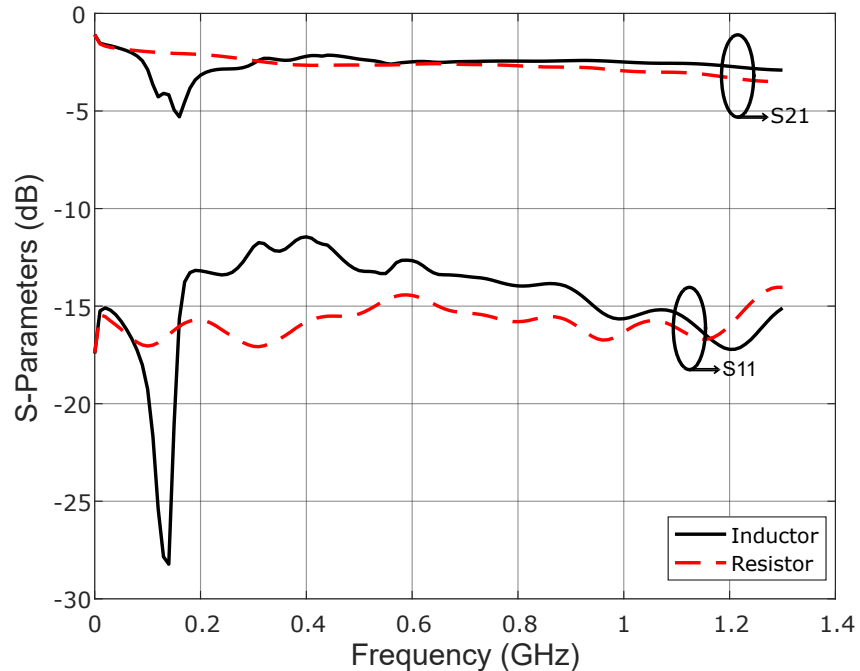


Figure 3.12: Measured S -parameters for resistive (dashed) and inductive (solid) switch versions of modulator B without de-embedding balun losses.

To test the power handling of the switches, a Mini-Circuits ZHL-10W-2G+ 10-Watt

amplifier was used to generate the required output power with a carrier frequency of 1 GHz. The P1dB of this amplifier is greater than 41 dBm with an IIP3 of 53 dBm. Since modulator A was not designed with on-chip gate drivers, the switch control inputs were driven using an M8195 arbitrary waveform generator in combination with splitters and amplifiers to create the required 2 V_{pp} swing on all clock ports. The output was attenuated and measured using a N9030B spectrum analyzer, and all output harmonics were summed to determine the final output power. A 30 dB coupler was inserted between the amplifier and the DUT, and the input power verified using an HP437B power meter. The insertion loss and compression points are measured with increasing power for both resistive and inductive versions and are shown in Fig. 3.13. Due to the attenuation required in the high power test setup, higher order modulation harmonics became hidden below the noise floor at lower input power levels. This leads to an apparent improvement in IL as the input power is increased in the inductive design, however in simulation, or when only dominant harmonics are taken into account, this effect does not occur. The 1 dB compression point of the inductive version was measured to be 30.9 dBm compared to 25.8 dBm for the resistive version. To test reliability, the inductive design was tested for 100 hours at 30 dBm input power while being modulated at 10 MHz to ensure that both carrier and modulation signals would not cause device breakdown. No performance degradation was observed over the duration of this test. Sudden, catastrophic failure was observed when the input power approached 35 dBm.

Beyond a higher compression point, the major distinction between the resistive and inductive version of modulator A is the maximum possible FBW. This is shown in Fig. 3.14 in which the inductive version is capable of handling modulation speeds of up to 300 MHz before the loss compresses by 1 dB while the resistive version compresses at 40 MHz.

From the theory in section II, eq. 2.16 predicts that the compression point of the

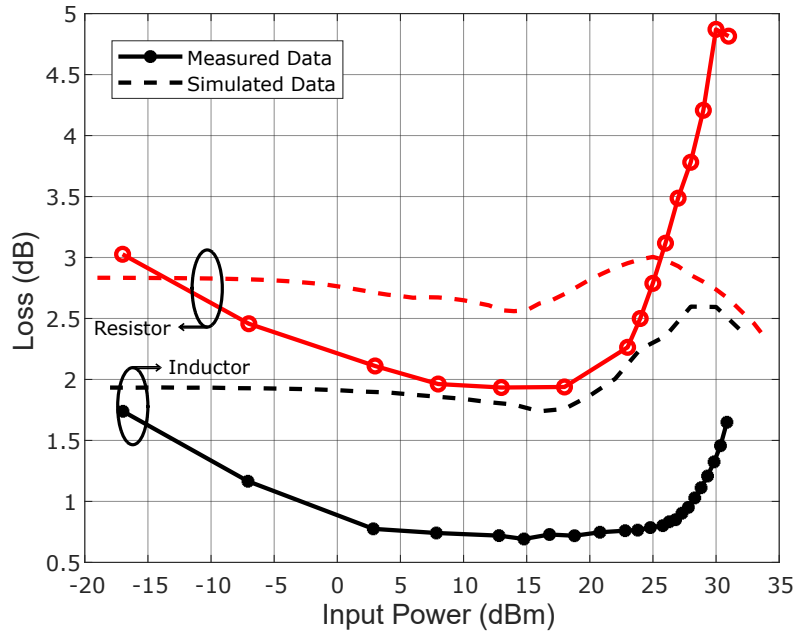


Figure 3.13: Loss vs. P_{in} at 20 MHz modulation including all power from harmonics for both resistive and inductive versions of modulator B

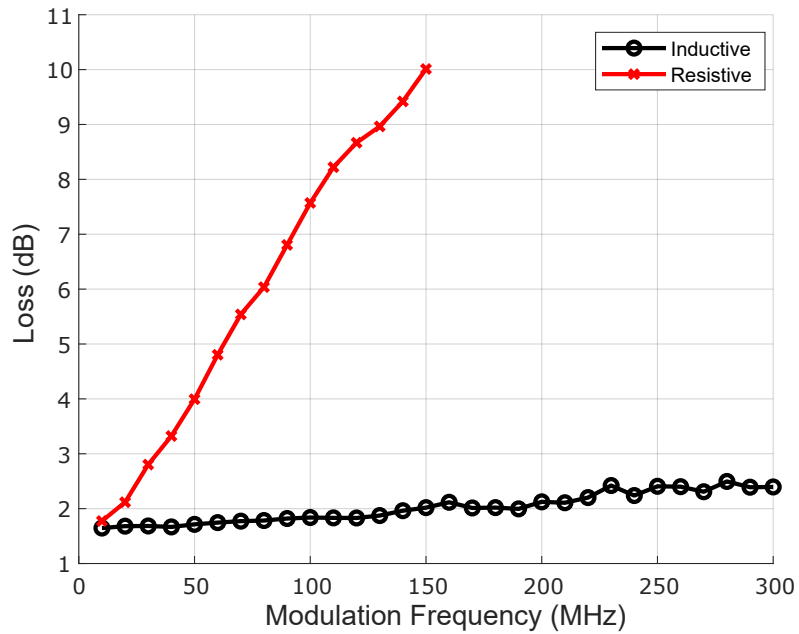


Figure 3.14: Loss versus modulation bandwidth with 20 dBm input power considering dominant spectral lobes for both the resistive and inductive versions of modulator B

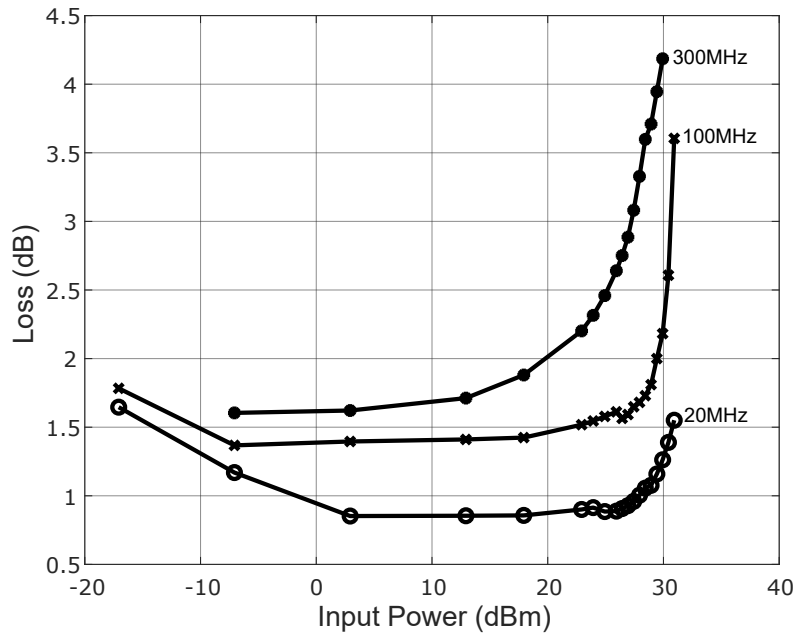


Figure 3.15: Power compression of the inductive version of modulator B with increasing modulation bandwidth

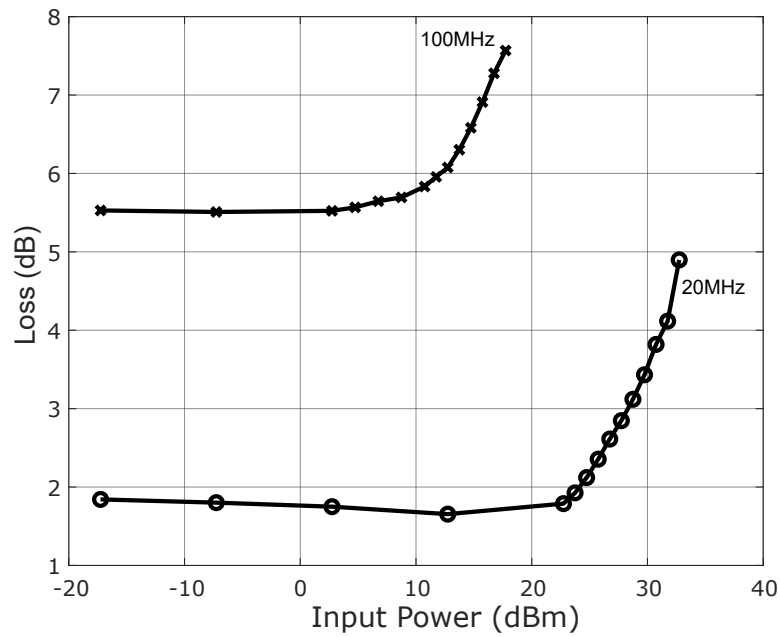


Figure 3.16: Power compression of the resistive version of modulator B at 20 MHz and 100 MHz modulation bandwidth

TABLE III
IIP3 MEASURED VS. TWO-TONE OFFSET

Offset (MHz)	1	5	20	40	60	80	100
IIP3 (dBm) Modulator B	42	42.9	42.8	42.8	42.9	42.2	42

switches is inversely proportional to modulation frequency. To demonstrate this, the P_{1dB} of the inductive version was measured at 20, 100, and 300 MHz and is plotted in Fig. 3.15. At 100 MHz the P_{1dB} drops slightly to 30.2 dBm while at 300 MHz, the P_{1dB} drops to 25.9 dBm. Similarly, the P_{1dB} of the resistive version is plotted in Fig. 3.16. Even though the IL is very high from the slow rise times of the switch, the power compression point has also dropped more than 10 dB compared to when modulating at a lower frequency.

A two-tone test is performed with CF1020 circulators at the output of each signal generator to prevent crosstalk before signals were combined. Terminating the third port with a 50Ω load allows the circulators to act as isolators and improve the linearity of the test-bench. Additionally, the attenuation of the N9030B spectrum analyzer used to measure the output was set to 40 dB in order to maximize the linearity of the spectrum analyzer itself. This test setup allowed for a maximum input power of the two tones to be 21 dBm and the IIP3 of the test-bench was measured at 62 dBm. This measurement using a 1 MHz offset is shown in Fig. 3.17 and demonstrates that the IIP3 of modulator B when using an inductive gate termination is 42 dBm. The measurement was repeated at various offsets and is given in table I. Like with modulator A, the IIP3 of modulator B was measured over several offsets and the data is given in table III.

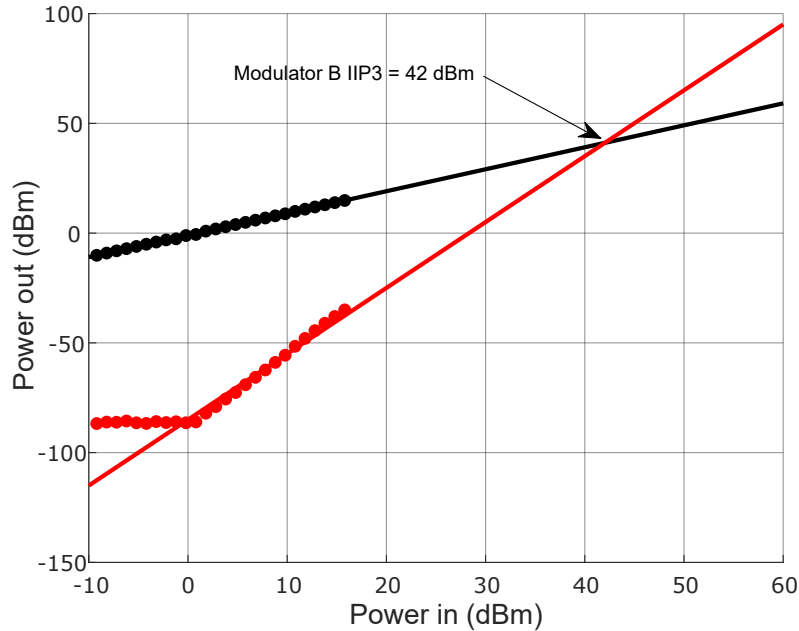


Figure 3.17: P_{in} vs. P_{out} and IM3 products to extrapolate IIP3 for the inductive version of modulator B at a 1MHz offset

3.3 Modulator C: Reflective Shunt Modulator

3.3.1 Design

The previous designs use back-to-back differential baluns to perform modulation. While these designs are good for low phase and amplitude imbalance, and the switches allow for low loss, the baluns add an additional loss of up to 1.6 dB making them the limiting factor of the design.

Alternatively, a reflection phase shifter (RPS) can be used to perform BPSK modulation. The proposed circuit makes use of a hybrid coupler rather than back-to-back baluns. Hybrid couplers with a loss of < 0.2 dB are readily available and, therefore, the RPS design offers significant advantages in overall loss compared to those using back-to-back baluns. The principle of operation for the RPS is to modulate the load seen by the through and coupled ports of a hybrid coupler. The reflections at these ports cancel at

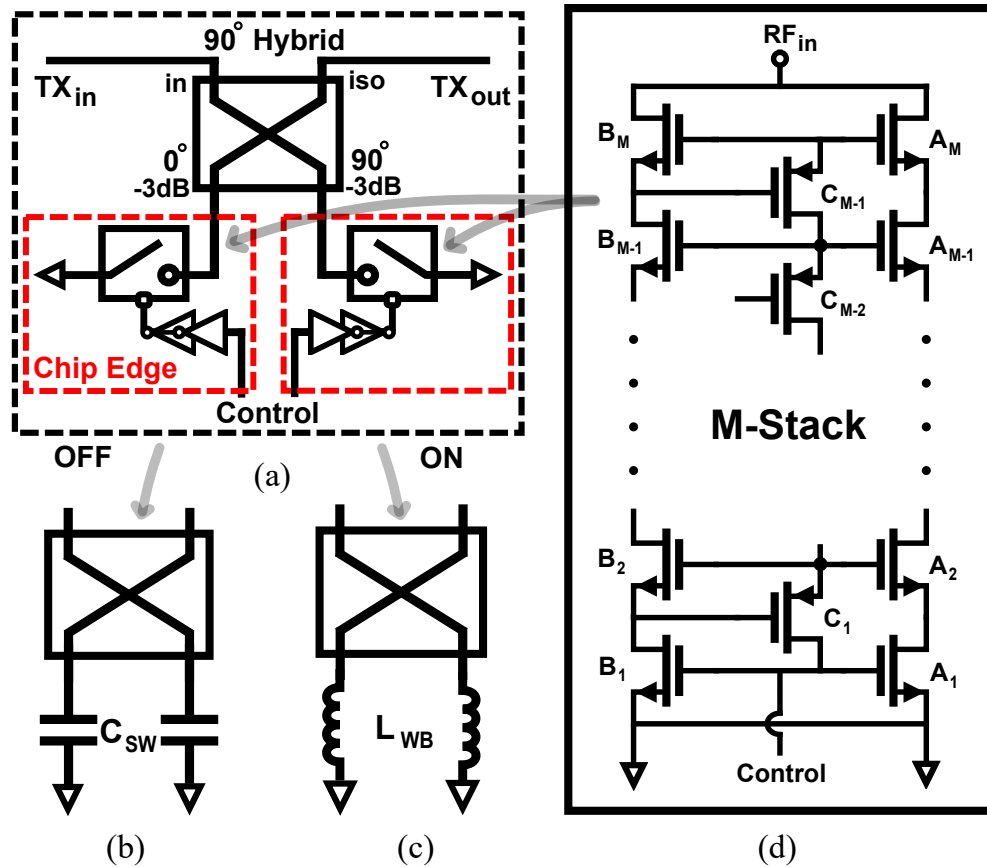


Figure 3.18: (a) Schematic of the RPS modulators, (b) Equivalent circuit when switches are open, (c) Equivalent circuit when switches are closed, and (d) Schematic of stacked-FET switches for high power, high bandwidth modulation.

the input port and add constructively at the isolated port of the coupler, respectively. By changing the phase of the reflection coefficient, the relative change in phase is imparted on the summed signal at the isolated port, creating a phase shift. For 2-state phase modulation, i.e. BPSK, only two reflection coefficients are needed, $\Gamma = 1$ and $\Gamma = -1$. An RF switch can be opened and closed at each output of the coupler to create either a 0 or 180 degree phase shift as shown in Fig. 3.18 (a).

When the switches are OFF, the reflection is ideally open, e.g. $\Gamma = 1$. However, the switch contributes some parasitic capacitance, labeled C_{SW} , to ground. The equivalent

schematic is shown in Fig. 3.18 (b). Consequently, the reflection coefficient is

$$\Gamma_{OFF} = \frac{1 - j\omega C_{SW} Z_o}{1 + j\omega C_{SW} Z_o}. \quad (3.1)$$

When the switches are ON, the reflection is ideally shorted, e.g. $\Gamma = -1$. Due to the inductance contributed by the wirebonds, L_{WB} , between the signal path and the switch and between the PCB and chip grounds as in Fig.3.18 (c), and the reflection coefficient is

$$\Gamma_{ON} = \frac{j\omega L_{WB}/Z_o - 1}{j\omega L_{WB}/Z_o + 1}. \quad (3.2)$$

While the effect of C_{SW} and L_{WB} would be detrimental to generating the precise reflection coefficient, the phase shift remains 180 degrees when C_{SW} and L_{WB} present equal impedance. Adding additional switches and passives could generate any desired phase shift which could have other implications for phased array design, load-pull networks or analog self interference cancellers.

Using an RPS approach does add some additional challenges in switch design. Because the incident wave is reflected off of $\Gamma = 1$ when the switch is open, the peak voltage seen at the input of the switch is doubled. Since the hybrid coupler divides the power equally between the two ports, the incident voltage on the switches is equal to $2/\sqrt{2} \cdot V_{TXin}$. To handling the high voltage, the shunt switches from section 2.5 can be used.

Two versions of the RPS modulator were designed. First a 12-stack switch was used to test what the highest voltage the CMOS switches could tolerate while still having relatively fast switching speeds. Second, an impedance transformation network at the input of each switch can be used to lower the voltage requirements for the same power handling. This allows the fewer stacks to be used with larger individual devices. The total load capacitance of the switch driver remains about the same, but since the stack

has fewer series components, the gate resistance is reduced and therefore switching speed can be increased. The trade-off for this design is that the RPS will only produce the desired phase shift at the design frequency as opposed to wide-band operation in the case of the non-transformed design. After optimizing for power handling, and phase and amplitude imbalance, an impedance transformation Z_0 in the range of 12.5-25 Ω requires 8 stacked FETs with FETs A_1 - A_8 each 5 mm wide. For a design without impedance transformation, the maximum useful number of stacks is 12 with each A device having a width of 1.8 mm. The secondary device sizing of the tapered ladder switches is given in Table IV - the tapering factor for the B devices is $x \sim 2.5$ while for the C devices $x \sim 2$.

TABLE IV
STACKED FET SWITCH SIZING

FET Index (M)	8 Stack		12 Stack	
	B Sizing	C Sizing	B Sizing	C Sizing
1	5mm	5mm	1.8mm	1.8mm
2	1.25mm	1.25mm	450 μ m	450 μ m
3	312 μ m	312 μ m	112 μ m	112 μ m
4	104 μ m	200 μ m	38 μ m	72 μ m
5	52 μ m	138 μ m	19 μ m	50 μ m
6	39 μ m	113 μ m	14 μ m	40 μ m
7	36 μ m	96 μ m	13 μ m	35 μ m
8	35 μ m	N/A	12 μ m	30 μ m
9-12	N/A	N/A	12 μ m	28 μ m

3.3.2 Measurements

The RF switches were designed and fabricated in the GlobalFoundries 45-nm SOI CMOS process. A micrograph of the 12-stack switch is shown in Fig. 3.19 (a), the 8

stack switch shown in Fig. 3.19 (b), and the PCB used to demonstrate the RPS shown in Fig. 3.19 (c). The hybrid coupler used for both designs is the Anaren XC0900A-03S chosen for operation at 1 GHz and an extremely low insertion loss of 0.2 dB. An impedance transformation network from 50Ω to 25Ω was used at the input of the 8-stack switch and was designed to incorporate the wire-bond inductance. The switches within each RPS were placed at a distance from each other on the PCB to prevent interference between the two at large input power levels.

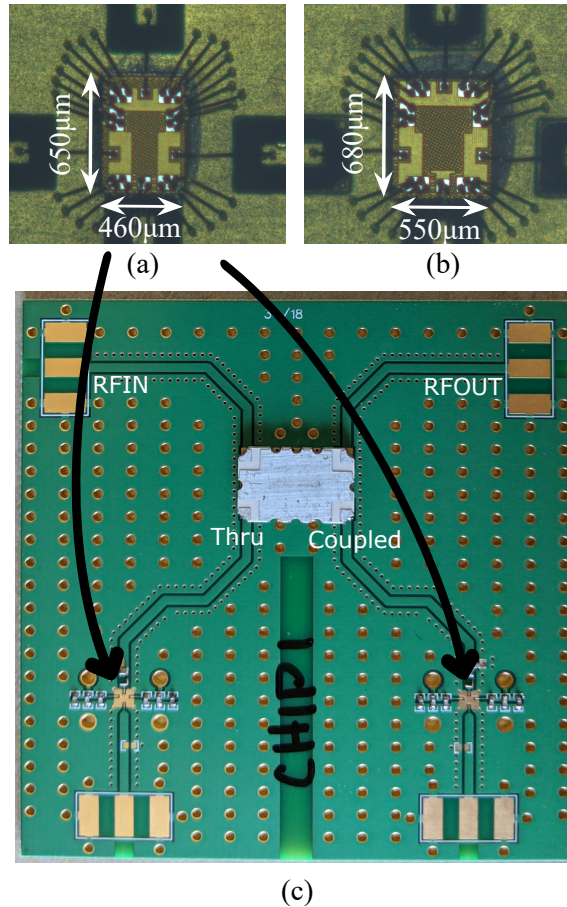


Figure 3.19: Photographs of (a) 12-stack switch, (b) 8-stack switch, and (c) reflection-based phase shifter board with surface mount hybrid coupler.

The measured small-signal S-parameters of the 12-stack RPS and 8-stack RPS are in Figs. 3.20 (a) and (b) respectively. Both versions exhibit wideband matching and low

loss from 600 MHz to 1.3 GHz. At 1 GHz, the losses of the 12-stack RPS are 0.88 dB and 1.5 dB in the OFF and ON state respectively. For the 8-stack RPS, the losses are 0.78 dB and 1.9 dB in the two states, respectively. Fig. 3.21 (a) shows the measured phase difference between the ON and OFF state of each RPS. The 12-stack RPS shows very low phase error from 400 MHz to 1200 MHz while the 8-stack RPS shows a narrower response, due to the impedance transformation, with minimum phase error at 1.09 GHz. Both modulators display amplitude error of less than 2 dB across the entire measured frequency range as shown in Fig. 3.21 (b).

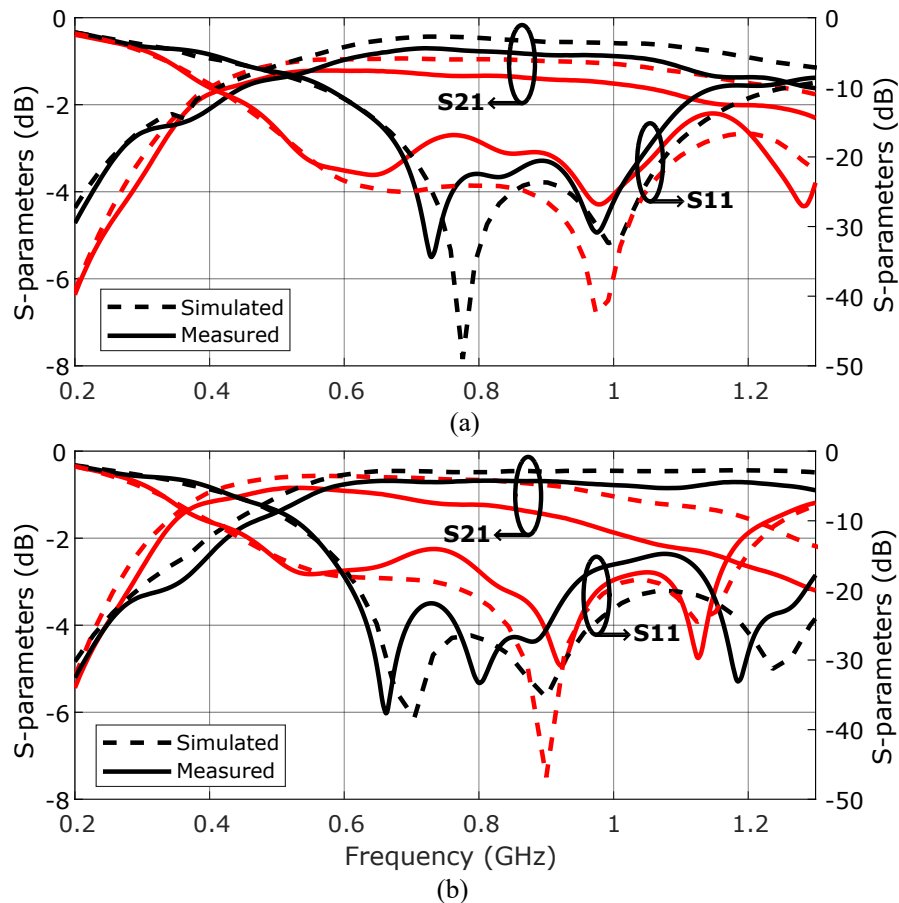


Figure 3.20: Measured and simulated (a) S-parameters of the 12-stack RPS in the ON (red) and OFF (black) states, (b) S-parameters of the 8-stack RPS in the ON (red) and OFF (black) states,

Measured compression characteristics are plotted in Fig. 3.22 (a) and (b) for the

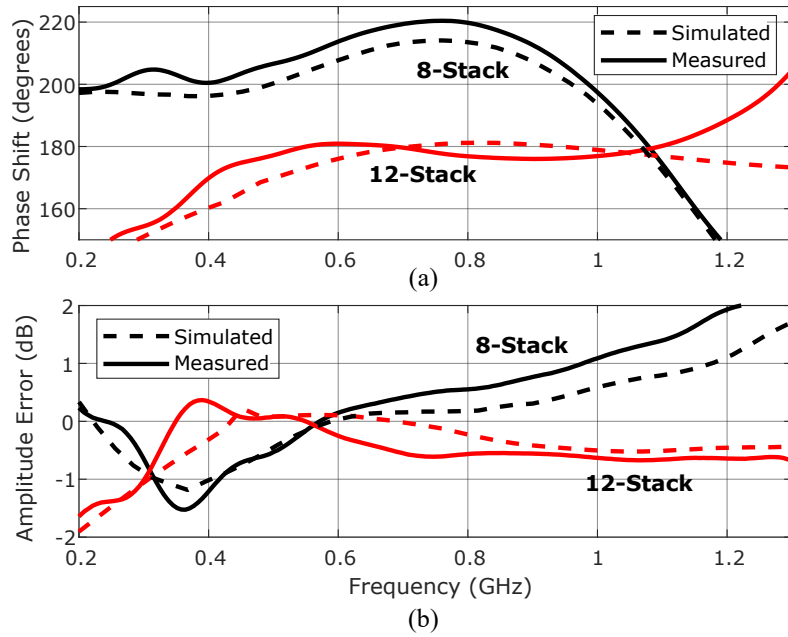


Figure 3.21: Measured and simulated (a) phase shift created between the two states of each RPS, and (b) amplitude error between the ON and OFF states of the 8-stack RPS and the ON and OFF states of the 12-stack RPS.

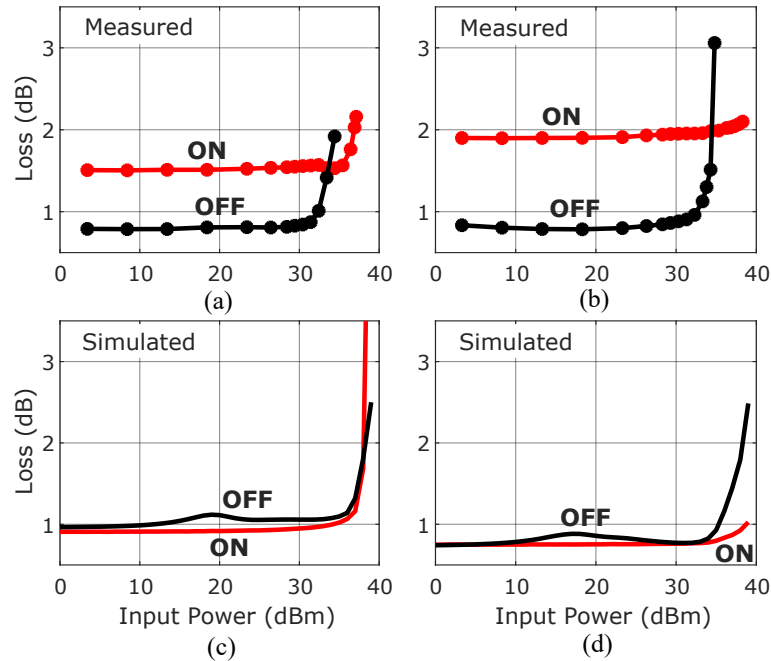


Figure 3.22: Measured compression characteristics of (a) 12-stack RPS, and (b) 8-stack RPS in both ON and OFF states. Simulated power compression of the (c) 12-stack RPS and (d) 8-stack RPS is also plotted.

12-stack and 8-stack RPS, respectively. In both modulators, the ON state has a higher compression point because it is limited by the ground wirebond inductance rather than any device characteristics. From Figs. 3.19 (a) and (b), the grounds of the chips have been provided through several wirebonds, and therefore compression of the ON state does not occur until nearly 40 dBm. In the OFF state, the devices are voltage-limited by the switch and therefore compress at lower power levels. The P_{1dB} for the 12-stack RPS is 34.2 dBm which corresponds to a simulated peak incident voltage of 23.2 V. For the 8-stack modulator, the P_{1dB} is 34.4 dBm in the limiting OFF state case, though at a lower voltage due to the impedance transformation. Simulated modulator compression is shown in Fig. 3.22 (c) and (d). Discrepancy between measured and simulated loss, particularly in the ON state can be attributed to non-ideal modelling of the wirebonds, PCB, and lumped element impedance transformation network. The measured IIP3 is plotted in Fig. 3.23 using a test-bench with a maximum IIP3 of 62 dBm. The 12-stack RPS has an IIP3 of 46.3 dBm and 57.4 dBm in the OFF and ON states, respectively, while the 8-stack RPS has an IIP3 of 46.2 dBm and 61 dBm in the OFF and ON states, respectively.

Fig. 3.24 highlights a key difference between the two modulators. When modulated at low frequency, the total loss including the hybrid coupler of the 12-stack RPS is 1.4 dB and the loss of the 8-stack RPS is 1.6 dB. While the 12-stack modulator offers lower IL, faster switching favors the 8-stack RPS to maintain a lower IL over a wider bandwidth beyond 100 MHz. Fig. 3.24 plots the loss integrated over the two dominant lobes of modulated spectrum and normalizes to the minimum loss of the 12-stack modulator to show how performance degrades at faster switching speeds. The FBW is determined at the frequency when the losses increase by 1-dB compared to the minimum modulation losses.

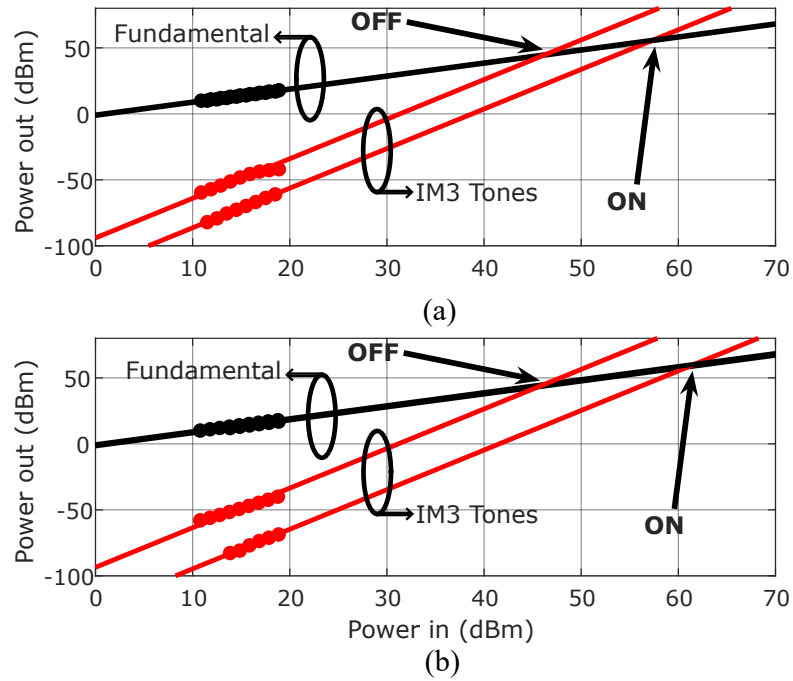


Figure 3.23: IIP3 measurements of (a) 12-stack RPS, and (b) 8-stack RPS in both ON and OFF states.

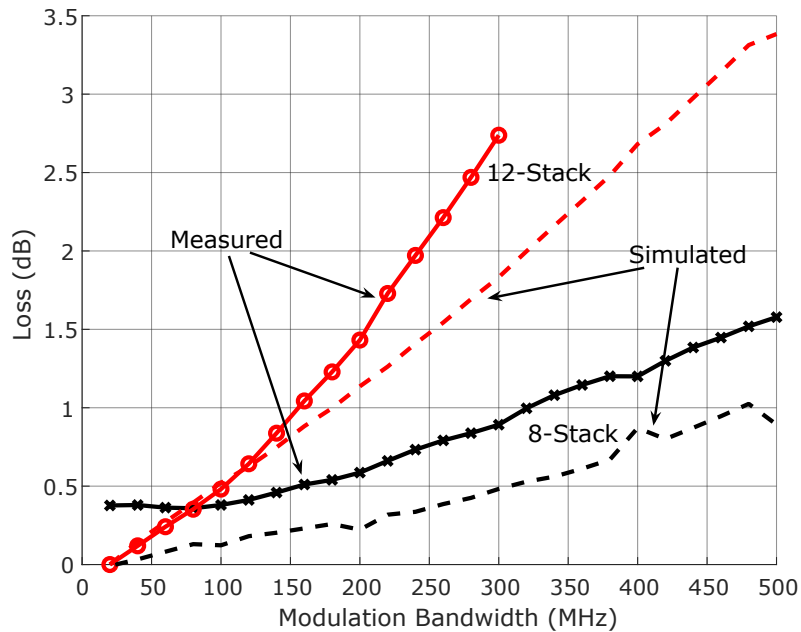


Figure 3.24: Loss of the 12-stack and 8-stack designs with 30 dBm input power with increasing modulation frequency. Loss is normalized to the minimum losses of the 12-stack modulator.

3.4 Analysis and Comparisons

Below in Table V is a summary and comparison of the previously reported results along with some prior work. Modulator C achieves the highest figure of merit due to its low loss, and fast switching speed, and moderate (>2 W) power handling. However, in terms of pure power handling, the balun designs are able to achieve >40 dBm due to the impedance transformation and the voltage reduction in the baluns. Additionally, the differential nature of the balun designs means that there are fewer issues with proper grounding and ground inductance on the chip which can cause problems in the control signals in the single ended RPS designs.

The cited prior work consists of only RF switches since these types of high-speed, high-power RF modulators are a new application. As such, the numbers may be somewhat over-represented because the complexity of a modulator is somewhat higher than just an SPDT or SPST switch stand-alone. Regardless, the presented designs offer higher figures of merit than every other prior work other than the commercial GaN device. However, these GaN devices need drive voltages in excess of 50 V to achieve such high linearity and FOMs and are therefore unsuitable for the RF modulator applications.

TABLE V
COMPARISON OF RF SWITCHES

Design	Technology	Freq.	IL	FBW	P1dB	IIP3	FOM
[27]	130 TW	0.9 GHz	0.5 dB	4% ⁺	31.3 dBm	43 dBm	5.41 ⁺
[28]	45 SOI	14 GHz	0.6 dB	0.2% ⁺	31.5 dBm	65 dBm*	1.26 ⁺
[41]	SiGe	23.8 GHz	-1.9 dB	42% ⁺	0.5 dBm	9 dBm*	$5e^{-5}$ ⁺
[38]	130 CMOS	1.9 GHz	1.5 dB	N/A	33.7 dBm	N/A	N/A
Qorvo QPC1005	0.25 μ m GaN	1.4 GHz	0.7 dB	1.7% ⁺	50 dBm	N/A	557 ⁺
[36]	45 SOI	5 GHz	N/A	48 %	29.6 dBm	N/A	N/A
Mod. A	45 SOI	1 GHz	3.2 dB	12 %	40.1 dBm	56 dBm	113
Mod. B (res)	45 SOI	1 GHz	3.6 dB	6 %	25.8 dBm	N/A	2.7
Mod. B (ind)	45 SOI	1 GHz	2.4 dB	60 %	30.9 dBm	43 dBm	69
Mod. C (12-Stack)	45 SOI	0.6-1.1 GHz	1.4 dB	16 %	34.1 dBm	46 dBm	72
Mod. C (8-Stack)	45 SOI	1.09 GHz	1.6 dB	46 %	34.4 dBm	46 dBm	201

⁺estimated from circuit parameters, *only single tone test reported

Chapter 4

Out of Band Spurs in RF signal Processors: PET

4.1 Introduction

One issue that arises when modulating at the antenna in these types of code-domain systems is that the “hard switching” results in significant harmonic content in the transmitted spectrum. While there are clear benefits to modulating at the antenna in terms of reducing bandwidth requirements of other system elements as well as in terms of overall system efficiency, the spectral noise of generated by the square edges must be considered fully. This concept of out-of-band processing noise extends beyond just the use of code-domain systems, and also applies to transmitters that wish to generate their data at the output, direct RF modulation (DRFM) schemes. These types of systems aim to improve system efficiency by using non-linear, high efficiency amplifiers in conjunction with RF modulators at the output to circumvent bandwidth-efficiency trade-offs. To generalize the analysis, most of this section will be presented with DRFM systems in mind.

An example spectrum that results from the hard switching is shown in Fig. 4.1At-

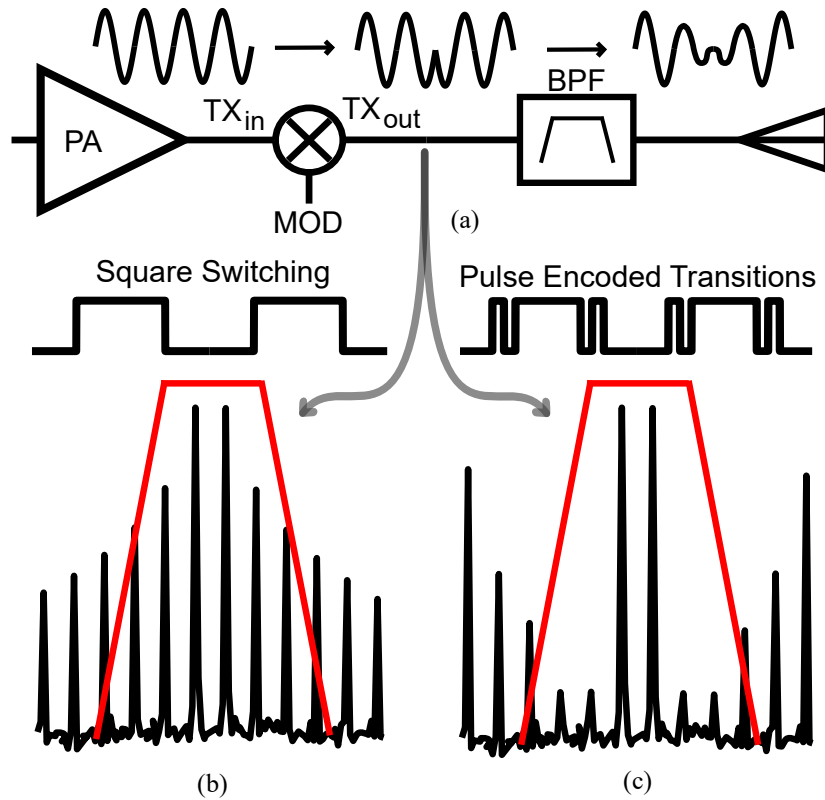


Figure 4.1: (a) TX chain used in direct RF modulators, (b) Example spectrum using square pulses with significant in-band content that cannot be removed by the filter profile highlighted in red, and (c) illustrated spectrum when using pulse-encoded transitions to eliminate in-band spectral components.

tempting to use a bandpass filter before the antenna to reduce the ACLR is impractical and demands narrow-band filter banks that introduce a large insertion loss (IL). Typically, raised cosine filtering and pre-distortion are used to control the ACLR but doing so in DRFM systems would reduce the efficiency benefits of DRFM already outlined while also requiring higher precision and high sampling rate power DACs. An established alternative is to use $\Sigma - \Delta$ modulation ($\Sigma\Delta M$) in conjunction with a BPF to approximate a raised cosine signal and shift the harmonic content to higher frequencies while easing filter requirements [42–53]. However, this requires significant digital processing power in addition to increasing the sampling rate of the available DACs by more than 100-fold to get sufficient ACLR reduction. In this section, ACLR reduction in DRFM is imple-

mented through a pulse-encoded transition (PET) technique that can be applied directly at the power modulator. The PET waveforms introduce switching intervals during each transition between symbols to approximate a band-limited signal and shift the harmonic content away from the band of interest to higher frequencies where it is easier to filter, as outlined in Fig. 4.1(c). While this chapter demonstrates the PET approach for DRFM, where the RF signal is randomly modulated, the outlined approach has important implications in other applications such as low-power harmonic reject mixers or harmonic cancellation in switching power amplifiers.

4.2 Periodic Analysis

The PET approach considers adding signal transitions and adjusting the pulsewidths of these transitions to reject aliased signal power. Previous work has provided a framework for cancelling harmonic content through careful calculation of pulse widths to emulate smooth transitions [54], [55]. Similarly, [56] constructs smooth clock transitions by adding phase shifted square waves with different weights to eliminate harmonic content of a mixer drive signal. Ultimately, both of these techniques construct signals that make use of both pulse-width and amplitude modulation to approximate arbitrary waveform generation which adds complexity.

The proposed technique seeks to maintain a purely digital approach to RF spectral shaping. At each transition of the original modulated waveform, $x(t)$, additional pulse transitions, $p_n(t)$, are added to synthesize an ideal band-limited signal, such as raised cosine. The modulated waveform, $y(t)$, is digital in nature but is represented as the product of $x(t)$ and a set of pulses of width Δt_n , centered at the original edges of $x(t)$.

Thus,

$$y(t) = x(t) \cdot \prod_{n=1}^N p_n(t) \quad (4.1)$$

The choice of the number of additional transitions, N , is limited by the available switching bandwidth and will be explored in the following sections.

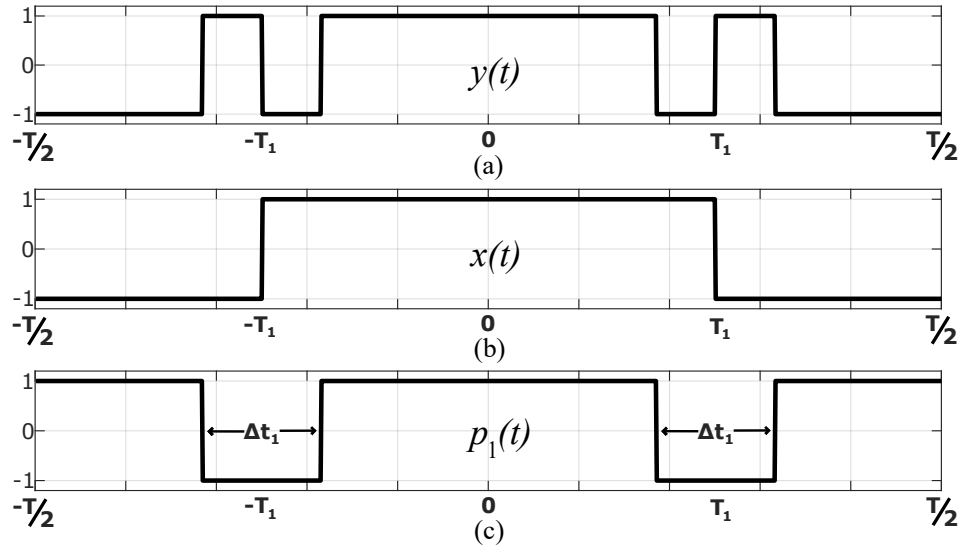


Figure 4.2: Decomposition of (a) the approximated band-limited square wave into more easily defined parts, (b) the original square wave, and (c) a pair of pulses of width Δt_1 centered at the transitions of (b).

To understand the construction of $p_n(t)$, initial considerations are limited to periodic forms for $x(t)$ and in the base case, a square wave, such as for a local oscillator driving a mixer. For $N = 1$, (4.1) reduces to,

$$y(t) = x(t) \cdot p_1(t), \quad (4.2)$$

where $y(t)$, $x(t)$, and $p_1(t)$ are plotted in Fig. 4.2 (a), (b), and (c), respectively. Since $x(t)$ is periodic, the composite signal, $y(t)$, can also be written as a Fourier series,

$$y(t) = \sum_{k=-K}^K a_k \cdot e^{j\frac{2\pi kt}{T}} \quad (4.3)$$

Solving for the Fourier coefficients, a_k , gives

$$a_k = \frac{2}{\pi k} \sin\left(\frac{2\pi k T_1}{T}\right) \left[-1 + 2 \cos\left(\frac{\pi k \Delta t_1}{T}\right) \right] \quad (4.4)$$

where T is period, and T_1 is half the pulsewidth of $x(t)$. Inspection shows that this solution can be decomposed into important components, $a_k = b_k \cdot c_k$, where b_k is the Fourier coefficients of $x(t)$, i.e. a square wave, and c_k is the coefficients of $p_1(t)$ convolved with $x(t)$. Since c_k depends on Δt_1 , it becomes clear that for a given k , a specific value for Δt_1 can be found such that c_k , and, therefore a_k , are zero. For example, the solution for $k = 3$ can easily be found analytically as $\Delta t_1 = T/9$ and the third harmonic is eliminated. It is also interesting to note that this solution does not depend on $x(t)$, i.e. T_1 , and, therefore, this analysis can be extended to any random modulation as will be subsequently discussed.

Analyzing values of $N > 1$ gives

$$a_k = \frac{2}{\pi k} \sin\left(\frac{2\pi k T_1}{T}\right) \left[(-1)^N + 2 \sum_{n=1}^N (-1)^{N-n} \cos\left(\frac{\pi k \Delta t_n}{T}\right) \right] \quad (4.6)$$

for a_k . This result yields N values of Δt_n that are solved with N equations. Consequently, for every pulse added to each transition, another harmonic can be cancelled. In the case of (4.6), there does not appear to be analytic solutions for values of $N > 1$, however solving them numerically is not difficult given the constraints;

$$\Delta t_n < \Delta t_{n+1} < 2T_1 \quad (4.7)$$

These constraints ensure that the solutions do not result in any wrapping errors that might occur when performing the integration used to find (4.6).

Fig. 4.3 (a) compares the spectrum for a square-wave $x(t)$ and corresponding PET

spectrum of $y(t)$ when $N = 10$ for which the odd harmonics, 3 through 21 are cancelled. While the harmonics are eliminated, some of the aliased energy has been moved to higher frequencies where it can be more easily filtered. When the PET signal is passed through a first-order filter, as in the case of the RC -limited switch, the resulting filtered version of $y(t)$ is illustrated in Fig. 4.3 (b). As the high frequency content is filtered, the PET waveform converges to a sinusoidal signal.

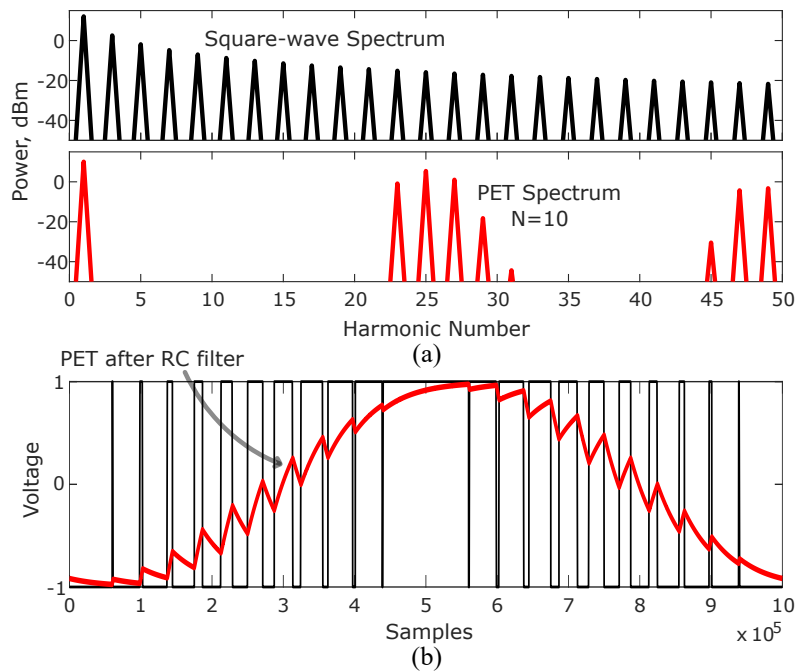


Figure 4.3: (a) Spectrum using PET compared to the original square-wave spectrum, (b) time domain of unfiltered and RC filtered PET signal when $N = 10$ and the RC time constant is 5% of the period, T .

Fig. 4.3 (b) also highlights one limitation of any PWM approximation of band-limited signals in that the maximum amplitude of the fundamental frequency is limited to the amplitude of the digital signal. When removing the high-order harmonic content through ideal raised cosine filtering, the fundamental amplitude is $4/\pi$ times the amplitude of the square wave. Therefore, the PET technique introduces an insertion loss (IL) as a function of the number of cancelled harmonics in Fig. 4.4. For a large N , the IL converges to

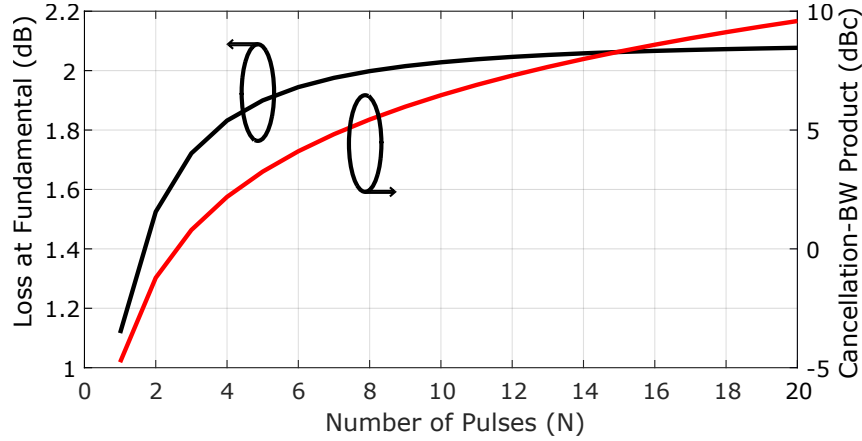


Figure 4.4: Fundamental insertion loss and cancellation-bandwidth product as a function of increasing number of pulses.

2.1 dB, however this loss also comes with an increased total cancellation as N increases.

Fig. 4.4 also plots the cancellation-BW product (CBW) defined by

$$CBW = (2N + 1) \sum_{n=1}^N (HD_{2n+1,o} - HD_{2n+1,c}) \quad (4.8)$$

where HD_{2n+1} is the harmonic distortion defined by the ratio of the power in the $2n + 1$ harmonic relative to the fundamental and the subscript, o , denotes the original HD while c denotes the cancelled HD . The bandwidth is normalized to the fundamental frequency. For example, when $N = 1$ the $HD_{3,o}$ is $1/9$ and is eliminated, i.e. $HD_{3,c} = 0$. Then $CBW = 10 \log_{10}(3 \cdot (1/9 - 0)) = -4.77dB$ which is the result shown when $N = 1$ in Fig. 4.4. Alternatively, multiple harmonics can be cancelled partially for $N = 1$ or N can be increased to cancel more harmonics completely. The effectiveness of the PET scheme for real DRFM switches will be evaluated by measuring this cancellation bandwidth and comparing to the ideal curve in Section 4.5.

4.3 Random Analysis

The previous analysis considered the case where $x(t)$ is periodic, i.e. a square-wave. More generally, it is important to consider random modulation and the impact of PET filtering on the resulting power spectrum. Previously, the observation was made that solutions for Δt_n do not depend on the duty cycle, or pulse width of $x(t)$. Therefore, arbitrary modulation can be decomposed into individual pulses and hence we can reconsider the earlier analysis where T_1 does not equal $T/4$. Additionally, since the Fourier transform is a linear operation, the addition of the pulses in the time domain also leads to the addition of the pulses in frequency domain (with the exception of the DC component which in this case is not important). The power spectral density (PSD) of the modulated signal then becomes

$$S_{yy}(f) = S_{xx}(f) \left| (-1)^N + 2 \sum_{n=1}^N (-1)^{N-n} \cos\left(\frac{\pi f \Delta t_n}{T}\right) \right|^2 \quad (4.9)$$

The PSD of $x(t)$ is S_{xx} and follows a $\text{sinc}^2(f)$ function, as highlighted in Fig. 4.5 (a) with nulls occurring at multiples of $1/(2T_1)$, the symbol rate. However, when the same solutions for Δt_n in $p_n(t)$ are scaled to the pulsewidth they still cancel energy at the k^{th} harmonic as if the integration period were scaled to the pulse width, i.e. $T = 4T_1$ which is equivalent to enforcing (4.7) for a narrower pulse. This is demonstrated for $N = 1$ and $k = 3$ in Fig. 4.5 (b) where the x-axis is normalized to $1/T_1$, so that the indices of the k^{th} harmonic align correctly (solving for $k = 3$ results in a notch at 3 on the x-axis). What remains are two smaller lobes on either side of the k^{th} harmonic that are significantly reduced in magnitude, but still present.

To eliminate these remaining lobes, (4.6) can be solved for non-integer values of k . This yields cancellation at any desired location in the spectrum which is shown in Fig.

4.5 (c) where $N = 2$, $k_1 = 8/3$, and $k_2 = 10/3$. As such, an increasing number of pulses N can be added to an arbitrary signal that will reduce harmonic content over a specified bandwidth.

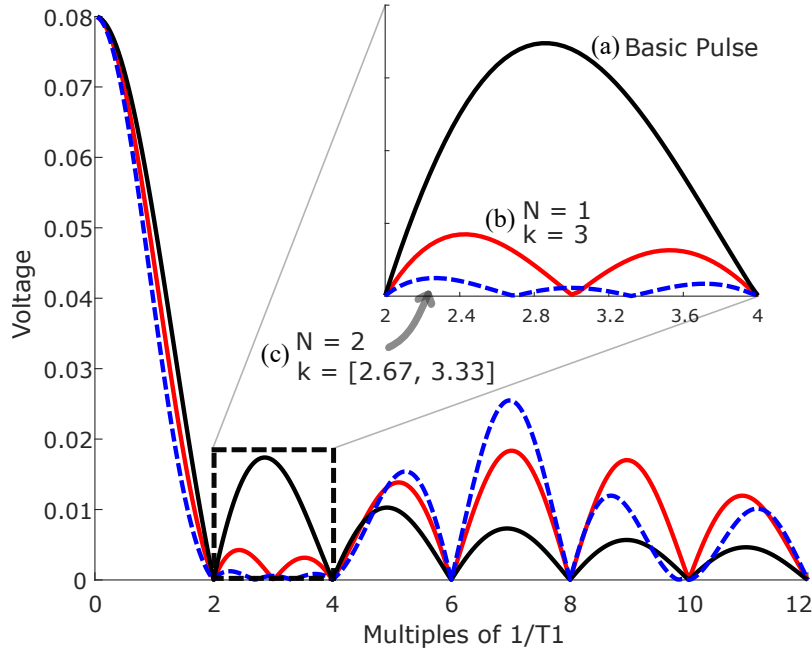


Figure 4.5: (a) Spectrum of a single pulse, (b) Spectrum when $N = 1$ and $k = 3$, i.e. $\Delta t_1 = 1/9 \cdot 4T_1$, and (c) when $N = 2$, $k_1 = 8/3$, and $k_2 = 10/3$.

Fig. 4.6 compares the resulting PSD for a random PET signal, $y(t)$, when using different solutions for different values of N and an averaging filter with a resolution bandwidth equal to $1/10$ of the sample rate to smooth the spectrum. For $N = 3$, the PSD is filtered for one adjacent channel, i.e. between 1 and 2 times the symbol rate, while for $N = 4$, the filtering extends over two adjacent channels, i.e. between 1 and 3 times the bit rate. Different locations for k enable a variety of notch depths and cancellation bandwidths in the modulated signal.

Since the analysis of PET does not rely on the width or amplitude of each data point/pulse, applying PET to amplitude modulated I/Q streams is effective at reducing the adjacent channel emissions. If the I and Q channels are independently modulated

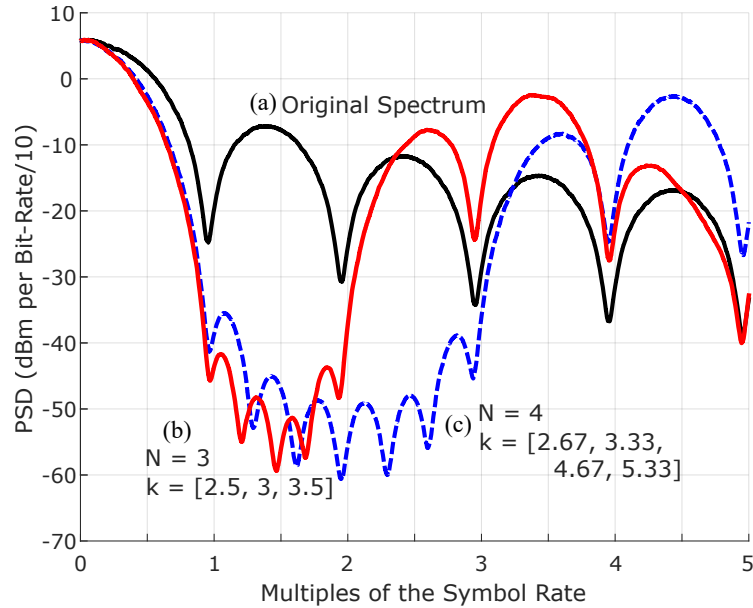


Figure 4.6: Spectrum for (a) random BPSK data, (b), cancellation of the first lobe with $N = 3$, and (c) cancellation of the first two lobes with $N = 4$.

using PET, the composite QAM waveform will alternate between subsequent symbols rather than simply between -1 and 1 to generate the band-limited symbol. In such a case, the solutions found through (4.6) are still valid. Therefore, if a DRFM system is capable of generating a constellation, it will also be capable of utilizing PET waveforms to reduce OOB emissions. Fig. 4.7 plots PET on a 16-QAM signal, highlighting the spectrum showing close to -50 dB ACLR, as well as the resulting time domain waveforms and the corresponding received constellations. While the circuits demonstrated in this work are limited to BPSK implementations of PET, various forms of DRFM transmitters have the potential to use PET waveforms for higher order modulation such as [57, 58] and [59]. In these cases, the PET waveforms could enable the use of lower resolution DACs through increased sampling rates.

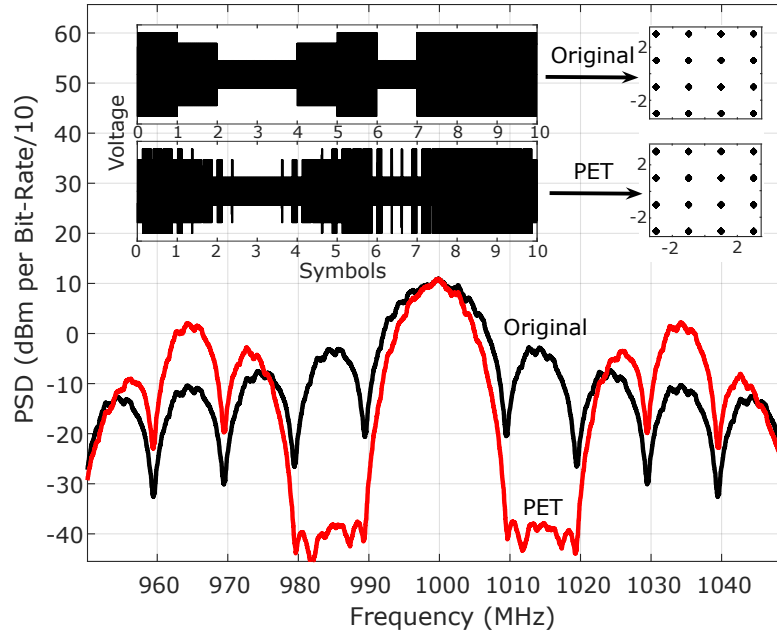


Figure 4.7: Simulated spectrum for a 16-QAM signal comparing the original spectrum to the PET spectrum and corresponding time domain waveforms and their received constellations. Relevant architectures that could accomplish this include [57, 58] and [59]

4.4 Comparison to $\Sigma - \Delta$ Modulators

With this motivation for using the PET technique, it is important to compare it with conventional approaches to filtering aliases produced by DRFM using pulse-width modulation (PWM) to emulate a band-limited signal originally suggested in [60]. As illustrated in Fig. 4.8 (a), the input signal is passed through a raised cosine filter, then converted to a PWM signal with constant envelope to generate a pulse stream that reconstructs the desired transmitter signal [61] [62]. However, [61] and [62] use a simple PWM encoding schemes which leads to high OOB quantization noise and spurious harmonics due to the required comparison waveforms.

Subsequent work demonstrated $\Sigma\Delta M$ techniques to generate PWM signals as shown in Fig. 4.8 (b) to shape the noise near the TX band. First, [42] uses $\Sigma\Delta M$ to emulate the entire RF carrier and envelope at the cost of an excessively high sample rate. Next, [43]

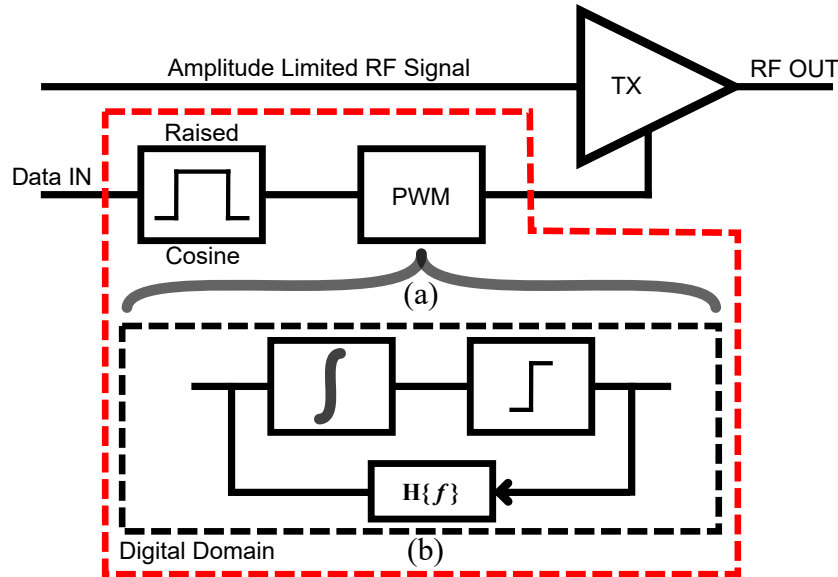


Figure 4.8: (a) PWM direct modulation transmitter chain, and (b) block diagram of a $\Sigma\Delta M$.

and [44] improve on this architecture by applying the $\Sigma\Delta M$ to the envelope of the RF signal to significantly lower the required sample rate. However, the OOB quantization noise level achieved is still only -18 dBc at an over-sample rate (OSR) of 200. Other approaches such as [46] and [47] present up to -50 dBc noise cancellation techniques for RF $\Sigma\Delta$ transmitters at low OSRs, but in doing so, re-introduce minor amplitude modulation and additional computational complexity, making these techniques unsuitable for DRFM. More recently, a variety of techniques to combat the noise, quantization, and bandwidth trade-offs have been proposed [48–53], and will be summarized in Table III at the conclusion.

It is important to distinguish between SNR and ACLR of the proposed designs - while they are related, SNR specifically deals with in-band noise while ACLR is the noise in the adjacent channel. For example, [50] provides excellent SNR over a very wide bandwidth, however, the ACLR at that bandwidth would be significantly higher than the in-band SNR after integrating the $\Sigma\Delta$ noise power over an additional 500 MHz. This is a general characteristic of $\Sigma\Delta M$ approaches for which the noise increases with out-of-band

frequency. In the case of higher-order $\Sigma\Delta M$ s, the slope at which the noise increases is also higher. While second order $\Sigma\Delta M$ can provide better ACLR as shown in Fig. 4.9, the input power of the signal must be backed off ~ 3 dB in order to increase the chance of stability [63]. This results in an additional 3 dB of loss when using a DRFM system which will highly impact the overall efficiency of the system. Because this work focuses on ACLR rather than SNR as well as minimizing losses, a comparison to a first-order $\Sigma\Delta M$ is sufficient due to the OOB noise shaping and stability issues in second order modulators. Finally, the ACLR is defined as the integrated power within the bandwidth of the first side-lobe of the spectrum (from one to two times the symbol rate) compared to the signal integrated power up to the desired bit-rate. This is shown by the spectrum plot in fig. 4.9.

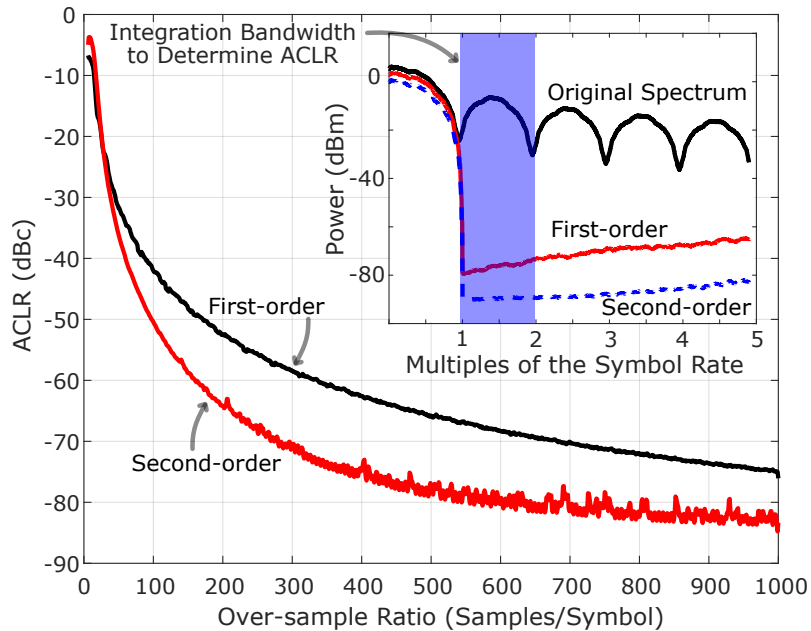


Figure 4.9: ACLR rejection using first and second order $\Sigma\Delta M$ for increasing OSR. A sample spectrum is provided to show the spectrum of the $\Sigma\Delta M$ at an OSR of 1000.

Regardless of any stability or noise shaping issues, to provide direct comparison with PET waveforms, Fig. 4.9 uses both a first and second-order $\Sigma\Delta M$ algorithm to simulate the digital domain of Fig. 4.8 with random BPSK data as the input. To provide an

ACLR of at least 50 dB demands an OSR of 200 for the first order modulator and 100 for the second order modulator. The high OSR places a significant burden on not only the digital power consumption, but also the tolerated switching speed of the RF modulator when using wideband signals.

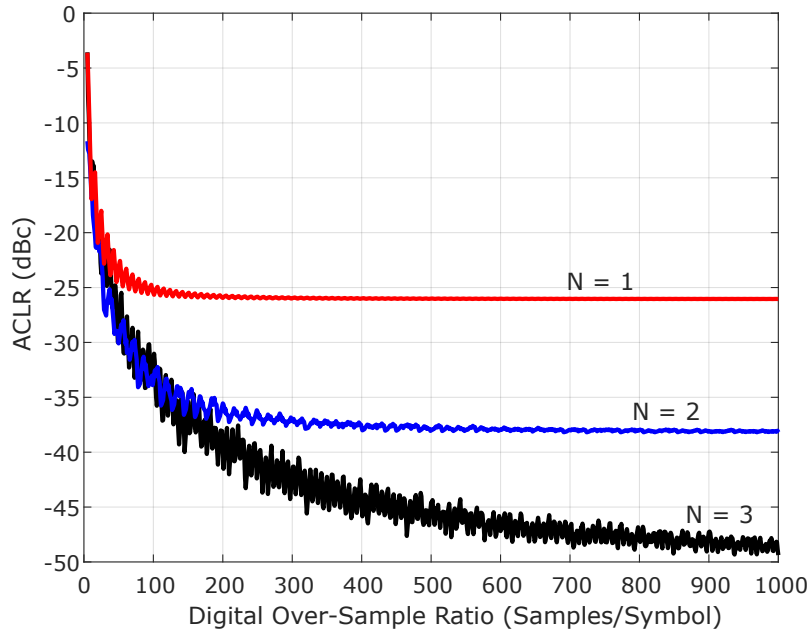


Figure 4.10: Adjacent channel leakage reduction for increasing number of pulses as a function of the digital OSR for the PET waveforms.

Ultimately, the proposed PET waveform is limited by two factors in any DRFM transmitter. First, the minimum pulsewidth will determine the required switching speed (RF OSR), of any power modulator at the antenna. Second, the decimal precision of the generated pulsewidths required to provide rejection will determine the required clock rate (digital OSR), of the digital processor. These represent the RF and digital switching speed bottlenecks, respectively. Both bottlenecks can be compared to the OSR of the $\Sigma\Delta M$ for which the minimum switching interval will always be related to the digital clock speed. Fig. 4.10 shows how the digital OSR of the generated pulses effects the rejection for different values of N for PET waveforms. The trends at higher values of N are similar to OSR values required by $\Sigma\Delta M$ s, and therefore indicate that the required

digital clock speed is similar. The benefit of the PET technique is clear in Table VI which compares the ACLR of PET and $\Sigma\Delta M$ using the minimum PET RF OSR as a reference sampling rate which can be determined from (4.10). For each case the simulated ACLR is in the range of 10-15 dB lower when using PET than when using $\Sigma\Delta M$ at the same RF OSR.

$$RF\ OSR = \frac{4T_1}{\min(\Delta t_{n+1} - \Delta t_n)} \quad (4.10)$$

TABLE VI

COMPARISON OF ACLR USING PET AND $\Sigma\Delta M$
AT SPECIFIED RF OSR VALUES

PET N	RF OSR	Simulated ACLR (dBc)				
		PET N			$\Sigma\Delta M$ order	
		1	2	3	1	2
1	18	25.8			16.1	10.7
2	32		38.0		25.5	25.9
3	58			49.1	34.4	39.2

4.5 Measurements

The 3-W RPS modulators are used to produce BPSK modulation at high power levels. To test the potential adjacent channel leakage reduction using PET, the 8-stack modulator is used because of its higher switching bandwidth to take advantage of the PET techniques. These ACLR measurements are at a center frequency of 1.09 GHz to minimize the phase imbalance and carrier leakage. It is important to look at the harmonic suppression and ACLR reduction with increasing data rates and over a range of cancellation bandwidths. MATLAB was used to calculate the required PET waveforms

which were sent to an M8195 AWG with a sample rate of 32 GS/s. The output of the AWG was used to drive the control lines for the two switches in the RPS modulators, while the RF input was a 30 dBm CW signal generated by a 10 W linear amplifier.

First, Fig. 4.11 shows the 3rd-harmonic rejection (PET $N = 1$) in the 8-stack RPS modulator as the modulation frequency increases. The RPS modulator is able to maintain > 35 dBc 3rd-harmonic rejection up to a 50 MHz modulation bandwidth. Additionally, the loss at the fundamental frequency stays around 1 dB over the range of modulation frequency.

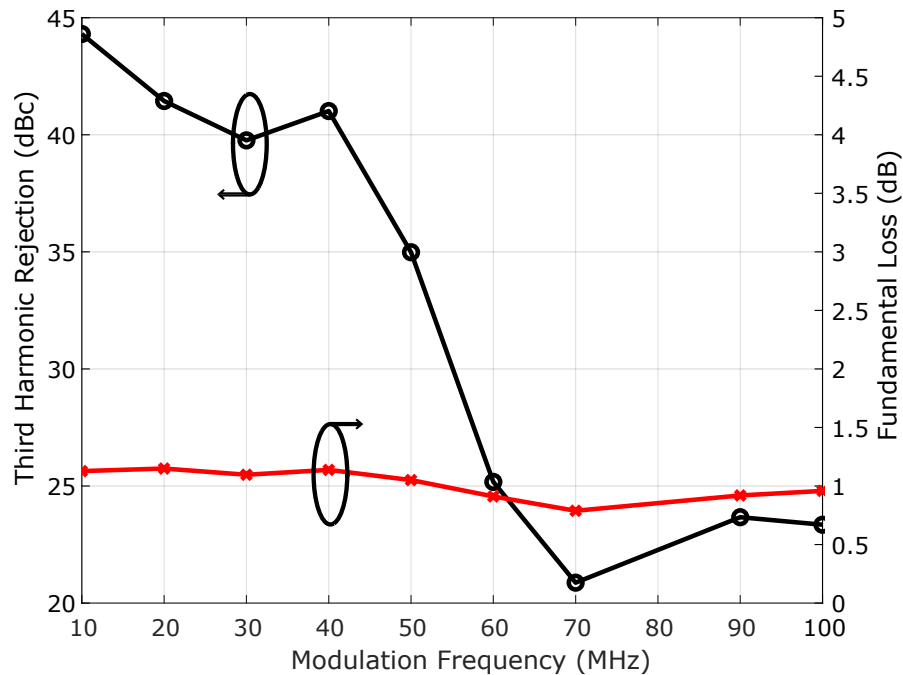


Figure 4.11: 3rd-harmonic rejection as a function of modulation rate and the loss at the fundamental.

Similarly, Fig. 4.12 gives the total rejected power for increasing numbers of pulses, N , with $x(t)$ as a 10 MHz square wave. With additional pulses, the total energy removed from the spectrum remains relatively constant as the majority of the power is located within the first few harmonics. However, this power is cancelled over a wider bandwidth and the measured data compares well to the simulated cancellation-bandwidth presented

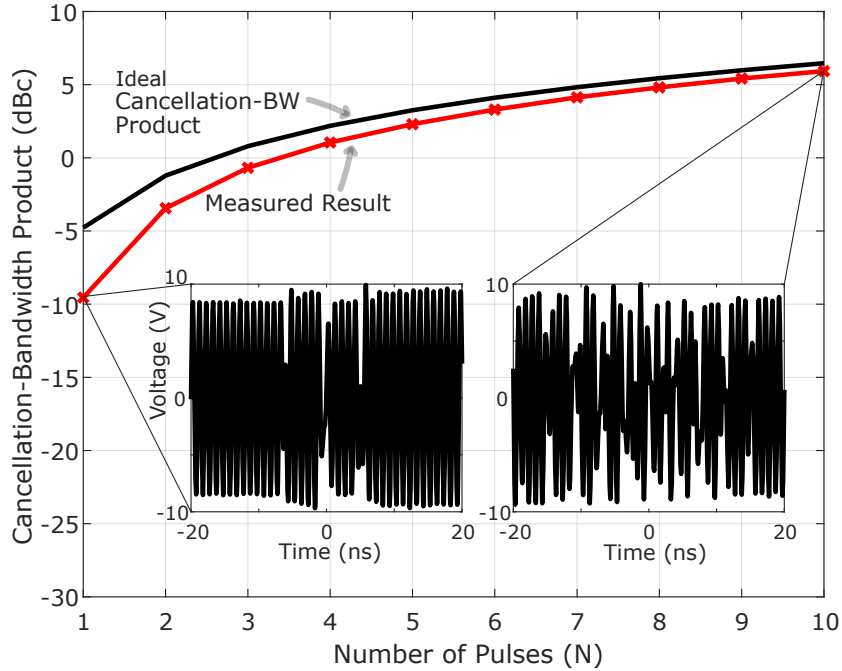


Figure 4.12: Rejection-bandwidth product for increasing values of N with the spectrum of the $N = 1$ PET waveform highlighted.

and defined as (4.8) in Section II-A. As N is increased, the measured result approaches the ideal simulation since the BW becomes the dominant term in the cancellation-BW product and the rejection remains relatively good. Time domain waveforms of the switching intervals are also shown in Fig. 4.12 for both $N = 1$ and $N = 10$. When $N = 10$, the switching intervals shorten to < 1 ns and the RPS modulator is unable to completely switch, though many of the lower harmonics are still cancelled.

Fig. 4.13 (a) shows the output spectrum when $N = 10$. The first 10 odd harmonics are cancelled, which results in a harmonic floor of -32 dBc across the first 21 harmonics. The higher odd harmonics, 23 through 27 are increased above what they would normally be since the PET algorithm shifts the energy from the low harmonics to higher ones. Using a first order band-pass filter with a bandwidth of 100 MHz causes the highest harmonic power to be suppressed to -26.5 dBc, shown in Fig. 4.13 (b), and demonstrates the ability of PET to relax the OOB filtering requirements. The OOB harmonic power

may be reflected off the filter and mixed again by the RPS modulator, or by the PA non-linearity, back in-band and cause interference. In the example of Fig. 4.13 (b), it was observed that the second harmonic increased by 5 dB due to the impedance reflection but remains at a power less than that of other harmonics that are cancelled by the PET technique. All other harmonics were only attenuated by the addition of the filter.

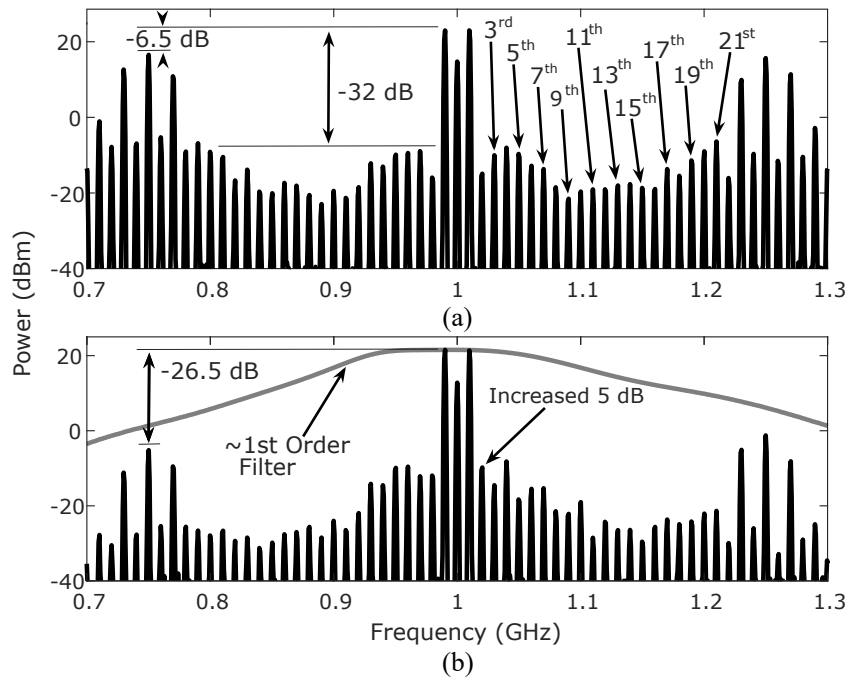


Figure 4.13: Measured PET spectrum for a 10 MHz square wave when $N = 10$, (a), and the same spectrum after being passed through a 1 GHz, low Q filter, (b). Wide-band harmonics are significantly attenuated, while near band mixing from the non-linearity is only marginally present.

Fig. 4.14 demonstrates examples of using PET waveforms for ACLR reduction. At a symbol rate of 20 Msps, significant side-lobe reduction is achieved as shown in Fig. 4.14 (b) for one adjacent channel and (c) for two adjacent channels. Similar to square wave modulation, the rejection is limited by the maximum switching bandwidth of the modulator.

Fig. 4.15 plots the ACLR reduction over the bandwidth of the first sidelobe with increasing symbol rate. The $N = 1$ case indicates a relative constant ACLR of -28 dBc

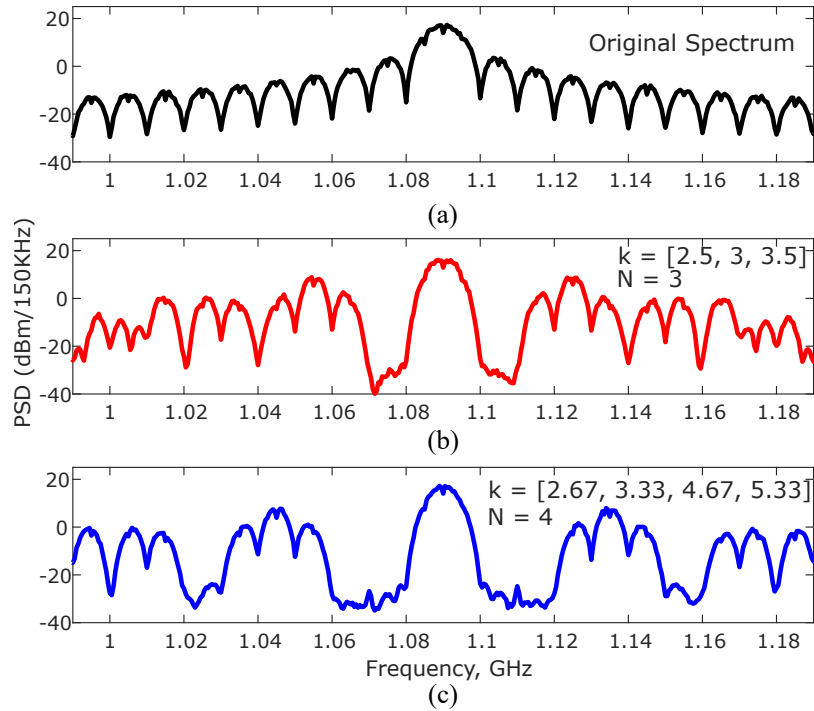


Figure 4.14: Measured DRFM spectra created using the 8-stack modulator with (a) the original spectrum, (b) cancelling the first lobe with $N = 3$, and (c) cancelling the first two lobes with $N = 4$ all with a data rate of 20 Msps.

over the data rate. For $N = 2$ and 3, an ACLR of better than -40 dBc is realized. In the case of $N = 3$, the required switching rate is roughly 11 GHz for a bit rate of 200 Msps based on Table I. Since the 8-stack modulator is not capable of this switching speed, the ACLR is significantly reduced from the predicted level. However, the RC -limited waveform still provides some ACLR reduction. For $N = 3$, the ACLR is not improved over $N = 2$ beyond 60 Msps when using this RPS modulator.

While Fig. 4.15 demonstrates the RF bottleneck for the PET algorithm, Fig. 4.16 shows the digital bottleneck. This can be measured by lowering the data rate significantly below the switching bandwidth of the modulator and then reducing the sample rate of the driving AWG. For a 2 Msps signal, the PET pulses were generated by limiting the sample rate of the 32 Gs/s arbitrary waveform to measure the ACLR at different digital OSRs. For each of $N = 1, 2$ and 3, excellent performance is still achieved at relatively low

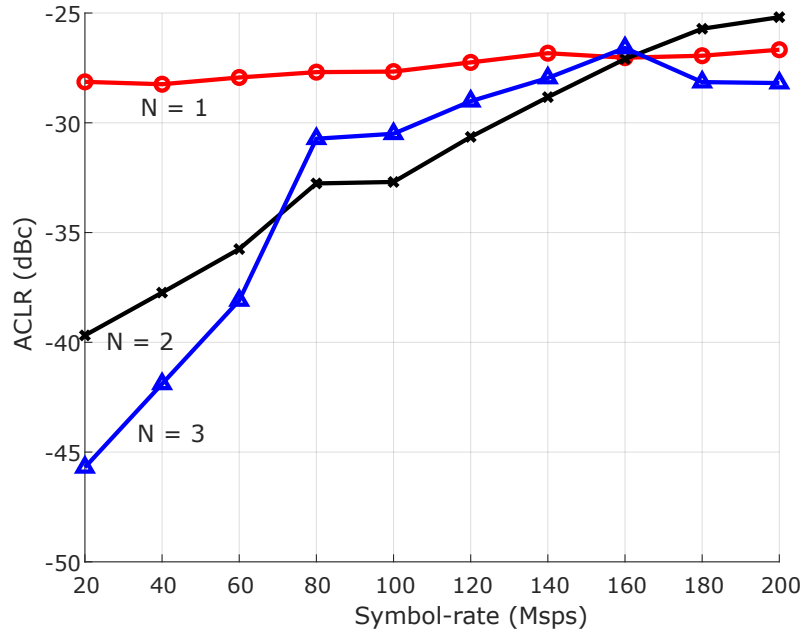


Figure 4.15: Measured ACLR for one cancelled lobe for increasing symbol rates and different values for N.

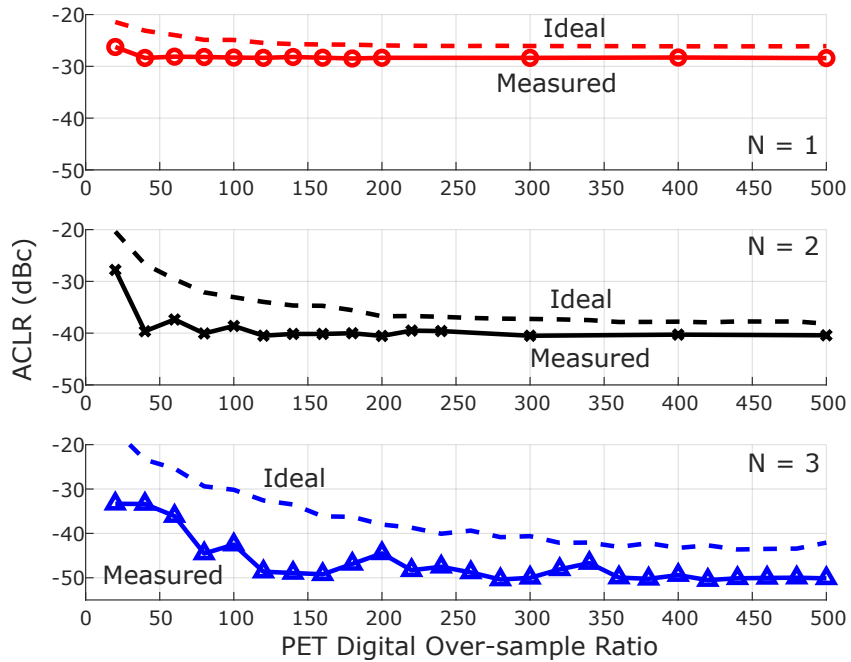


Figure 4.16: Measured ACLR with 2 MSPs base-band signal for increasing over-sample rates. The signals were generated by artificially lowering the sample rate on the 32 Gs/s arbitrary waveform generator.

OSRs. The measured results match well with the ideal ALCR simulated in MATLAB, and are in fact slightly better due to carrier leakage increasing the in-band power while not effecting the power measured in the adjacent sidelobes. To verify this assumption, measurements were performed at both 1 GHz and 1.09 GHz, and it was observed that the discrepancy between the ideal and measured values decreased at 1.09 GHz compared to 1 GHz as the carrier leakage was reduced.

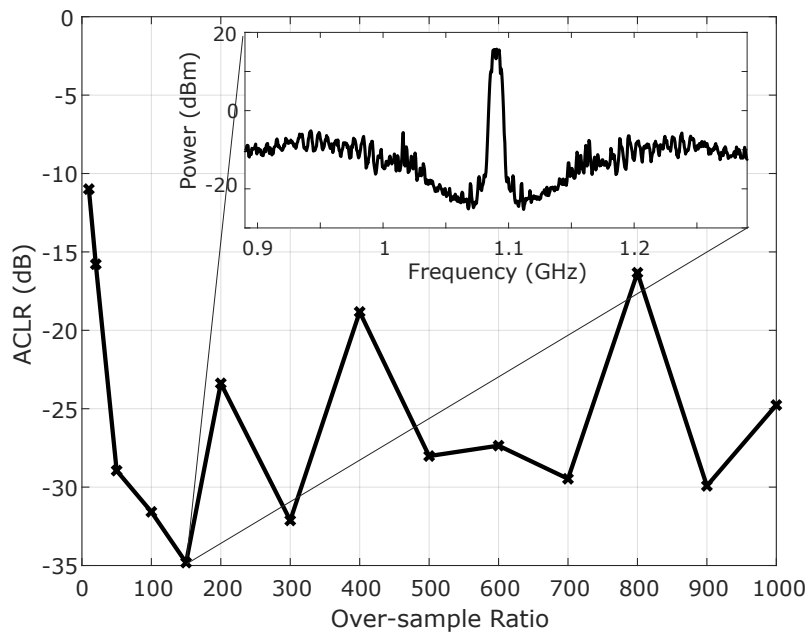


Figure 4.17: Measured ACLR for increasing over-sample ratios using the $\Sigma\Delta M$ technique in conjunction with the 8-stack RPS power modulator and 20 Msps BPSK data.

Finally, the 8-stack modulator was measured with a $\Sigma\Delta M$ approximation of a 20 Msps raised-cosine signal, shown in Fig. 4.17. For oversampling rates greater than 100 times the symbol rate, the power modulator is limited by switching speed, and the theoretical benefits of increased OSR are not realized. Comparing Figs. 4.15 and 4.17 shows that when using the PET approach with the same power modulators, the PET technique is capable of achieving >10 dB more ACLR than $\Sigma\Delta M$ at the same bandwidth. Referring back to section 4.4, Table VI predicts this result for when the RF switching bandwidth is the limiting factor in the system.

Table VII, below, compares the metrics for a variety of DRFM transmitters.

TABLE VII
COMPARISON WITH OTHER DRFM INTERFACES

Reference	Technology	Freq.	Min. ACLR	Signal BW	RF OSR
[44]	0.3 μ m GaAs	2.46 GHz	-18 dBc	4 MHz	200
[46]	NXP LDMOS	1 GHz	-50 dBc	1 MHz	20
[49]	0.25 μ m GaN	0.9 GHz	56.2 dBc	20 MHz	150
[50]	FPGA	4.8 GHz	34.8 dB (SNR)	500 MHz	20
[51]	FPGA	2.5 GHz	40.3 dB (SNR)	37.5 MHz	267
[52]	90nm CMOS	1 GHz	-53.6 dBc	50 MHz	80
[53]	90nm CMOS	2.7 GHz	-50 dBc	17 MHz	> 300
This work: 8-Stack	45 SOI	1.09 GHz	-50.5 dBc	200 MHz	58

Chapter 5

Applications in Code-Domain Self-Interference Cancellation

5.1 Introduction

The next step in the design of high-power, high modulation bandwidth RF switches and modulators is to implement them in the previously highlighted application - namely code-domain IBFD systems. The following sections will discuss some of the design challenges that come with this integration and the corresponding RX design challenges that need to be considered.

As previously outlined in chapter 1, simultaneous transmit and receive (STAR) within the same signal band offers the potential to estimate the channel response and support full-duplex communication. Defense systems use spread-spectrum communication but cannot support FD operation since the co-located Tx typically has peak power levels exceeding 33 dBm and produces significant Rx band interference. Even with 23 dB isolation between the Tx and Rx, self-interference power levels exceed 10 dBm in the Rx path, demanding high in-band linearity (>20 dBm) and high-rejection (>40 dB) at the

LNA.

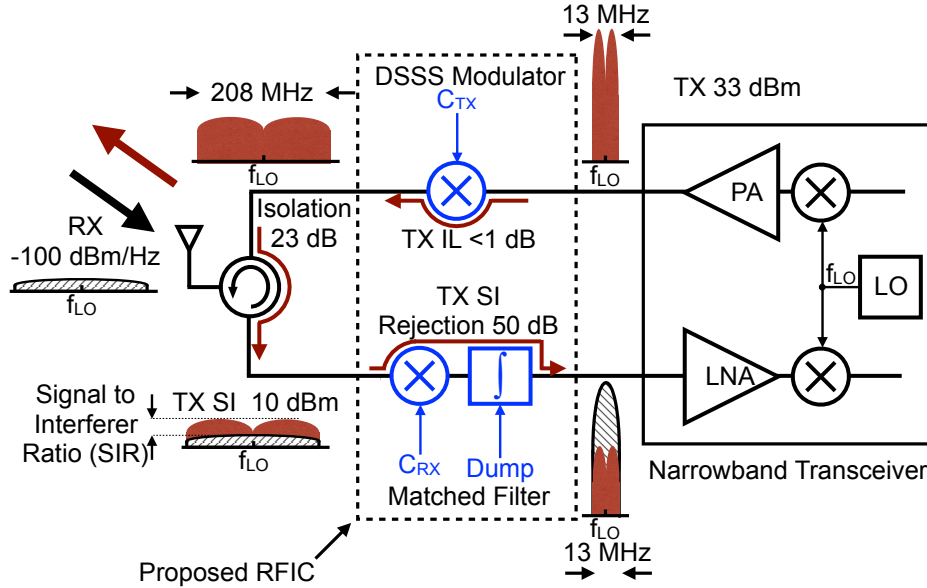


Figure 5.1: Proposed DSSS modulator and matched filter with RF code correlator and integrate and dump.

Prior work on STAR has been demonstrated [10,11,14–16,64,65]. In [8], a combination of electrical balanced duplexer with a 3-dB TX power penalty, and analog cancellation before and after the LNA offers 70 dB of rejection, but is limited to low TX SI power levels. Furthermore, analog cancellation does not reject other multiple access interference. An alternative approach based on code-domain receiver has been demonstrated at LNA/mixer with 38.5 dB of rejection [14], however, without the capability of handling strong TX SI (in-band P1dB = -11.8 dBm). Code-domain approaches [14] [64] also assume TX coding prior to the power amplifier (PA) which increases the required PA bandwidth to several hundred MHz which limits the overall system efficiency.

To solve these issues a fully-integrated code-domain transceiver capable of signal processing at the antenna is proposed. This interface is able to overlay a code-domain STAR system onto narrowband components leading to savings in ADC/DAC resolution and baseband power while maintaining efficiency by modulating the TX after the PA.

Additionally, filtering before the LNA mitigates the linearity requirements of the active circuits.

The proposed approach is shown in Fig. 5.1. In the TX path the direct-sequence spread-spectrum (DSSS) modulator is a fast high-power BPSK modulator and modulates the original TX signal by a code sequence C_{TX} and spreads the signal bandwidth by a factor of L . The TX signal is then isolated from the RX by more than 20 dB using a circulator or duplexer technique. In the RX path, the RF signal is correlated with code C_{RX} . For matching codes, the RX signal is increased by the processing gain and concentrated within the signal bandwidth. For orthogonal codes, the RF signal is spread out of band (OOB). Consequently, the remaining OOB spectral components are rejected by the receive correlator as shown in Fig. 5.1.

This chapter demonstrates the first fully integrated code modulator and demodulator operating in the RF domain. TX modulation after the PA is accomplished using a reflection phase shifter and high power stacked switches which can achieve modulation speeds of up to 300 Mc/s while handling an input power of 34.3 dBm. The receive correlator is implemented using an N -path filter, chosen for its high level of integration and tunability. Compared to previous N -path implementations, which have insufficient linearity to handle strong interferers present in a STAR system [66] [67], this work uses a hybrid transmission gate switch with optimum biasing to achieve a record setting in-band P1dB of 12.1 dBm. Additionally, the N -path filter has reset circuitry to implement an integrate and dump (IAD) feature which can be used to reduce inter-symbol interference (ISI) and lower the system noise. The integration of the TX and RX components of the system onto one chip is advantageous for reducing the lag time for synchronization of the TX and RX codes and achieving the highest SI cancellation.

The following section reviews the circuit techniques for the high-power DSSS modulator, the linear code correlator, and IAD filter. The measurements demonstrate the

rejection of the receiver as well as the insertion loss and power handling of both the TX and RX circuitry. Finally EVM measurements indicate that the proposed solution can handle TX power of 30 dBm with nearly 50 dB of SI rejection while the RX still achieves an EVM under 20% for a QPSK signal.

5.2 Integrated Code-Domain Tranceiver Module Design

Fig. 5.2 shows a block diagram of the proposed code-domain front-end chip with off-chip passive components for code-domain signal processing. The transmitter consists of a pair of high-power RF switches designed to add a PN code as a BPSK signal. The RX implements RF-domain code correlation with high input power compression. Both the transmitter and receiver were integrated on a single die to share the code generation circuitry and simplify synchronization between the TX and RX. The front-end is built upon the high-power and high-linearity RF switches available in the 45-RF CMOS SOI process. These switches have an $R_{ON}C_{OFF}$ product on the order of 130 fs and support the low-loss RF signal processing functions.

5.2.1 High-power TX Modulator

The TX DSSS modulator includes two 35-dBm RF CMOS SOI switches connected to the isolated and coupled port of an off-chip 90° hybrid coupler. The principle of the BPSK modulator is presented in [32] and in section 3.3, and uses a reflection phase shifter to alternate between 0 and 180 degree phases. When turned off (open), the switches create an in-phase reflection and produce no phase shift on the RF signal. When turned on (short), the switches produce a 180° reflection. The use of open and short reflections adds

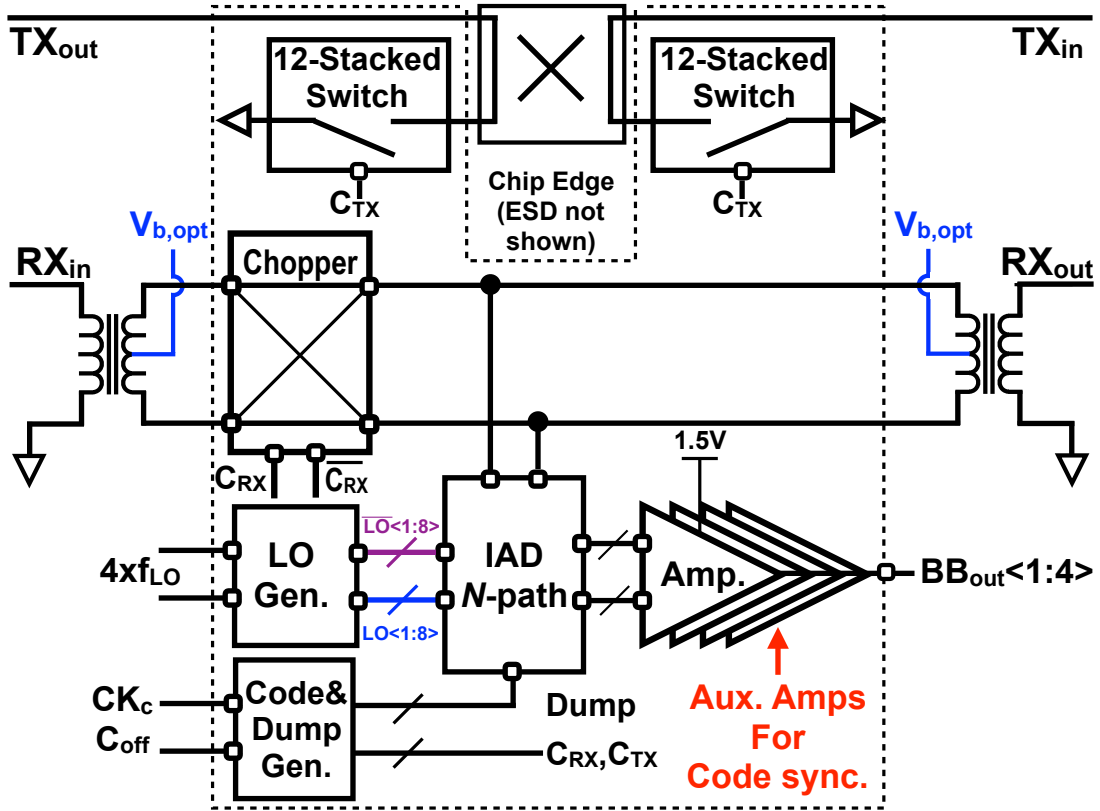


Figure 5.2: Block diagram of the code-domain front-end for STAR applications.

additional design challenges in the RF switch design since the open reflection doubles the incident voltage while the short reflection results in a high current through the switch.

To handle the high voltage under the open condition, the RF switch is based on a 12-stack CMOS SOI FET with 1.8mm NFET and auxiliary PFET/NFET switches shown in Fig. 5.3 (a) and sized according to the 12-stack switch in [32]. The device stacking distributes the voltage swing between the transistors and prevents breakdown without inhibiting switching speed [30]. The progression of drain voltages across the switch devices is shown in Fig. 5.3 where it is clear that the voltage drop across each device is approximately 1 V. Most notably, tapering the size of the *B* and *C* devices in the auxiliary switches supports high power handling along with high switching speeds on the order of 3ns for high fractional bandwidth. To differentiate this design from [32] and

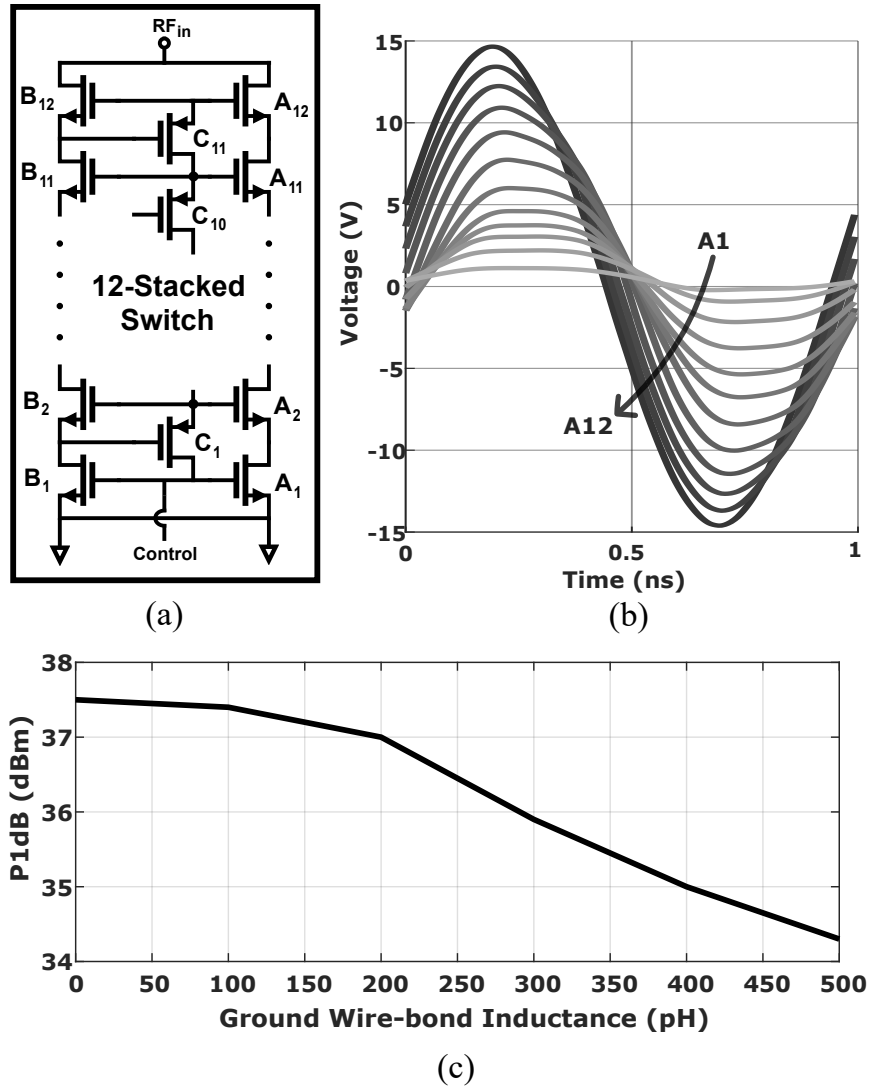


Figure 5.3: Diagrams of (a) the circuit used to build the high-power switches, (b) the drain voltage on each subsequent primary A device at an input power of 30 dBm, and (c) the simulated compression point of the modulator for different wire-bond inductance.

that of section 3.3, the high-power switches are integrated onto the same silicon die as the receiver circuits posing additional design challenges since the reduced overall usable space for wide ground planes and multiple wire-bonds that are required to maintain a low ground impedance when the switch is on and high currents are passed through the chip. Even relatively small wire-bond inductance becomes an issue at high RF power

levels at 1 GHz since the switches are driven with standard CMOS logic levels, e.g. 0 to 1 V, and voltage ripple in the ground plane can lead to premature device turn-off and therefore power compression.

The effect of wire-bond inductance on power handling is simulated in Fig. 5.3 (c) which shows that power handling is limited to below 35 dBm even with ground inductance as small as 400 pH at 1 GHz. To mitigate this problem, large area of decoupling NCAPs were used to connect the digital ground/power and RF ground planes. Additionally, multiple ground pads were placed on perpendicular edges of the chip to minimize inductive coupling and overall ground inductance between them. This can be seen later in Section 5.3, Fig. 5.6. To prevent additional interference in the RX path from the TX signal, the TX modulator and RX correlator are constructed with separate on-chip grounds which are connected together off-chip.

5.2.2 Rx Design

In the RX path, the incoming RF signal is modulated with a chopper to correlate the RF signal against a desired code sequence. The signal is then passed through a shunt N -path filter that incorporates an IAD to reset the N -path filter after every code correlation completes. The processed signal is available at the RF output port or for the baseband amplifiers to sample the voltage across the N -path capacitors and directly receive the desired signal or aid in the synchronization process. The chip also includes circuitry to generate non-overlapping clocks to drive the switches of the N -path. The code and dump signal generation produces signals to drive the RX chopper, dump switches and DSSS modulator. On-chip logic generates Walsh (for a better rejection) and Barker codes (for synchronization phase) as well as a bypass for an off chip code.

Schematics of the RX chopper and IAD N -path filter are shown in Fig.5.4. The

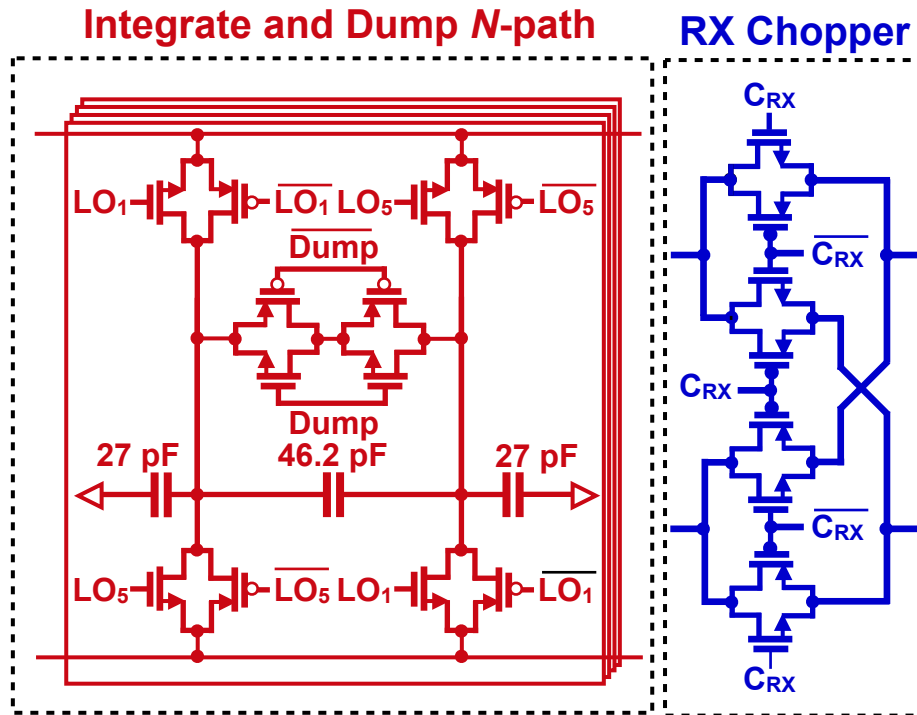


Figure 5.4: Circuit schematics for RF receiver blocks including the 10-dBm RX chopper and a single path of the integrate and dump N -path filter.

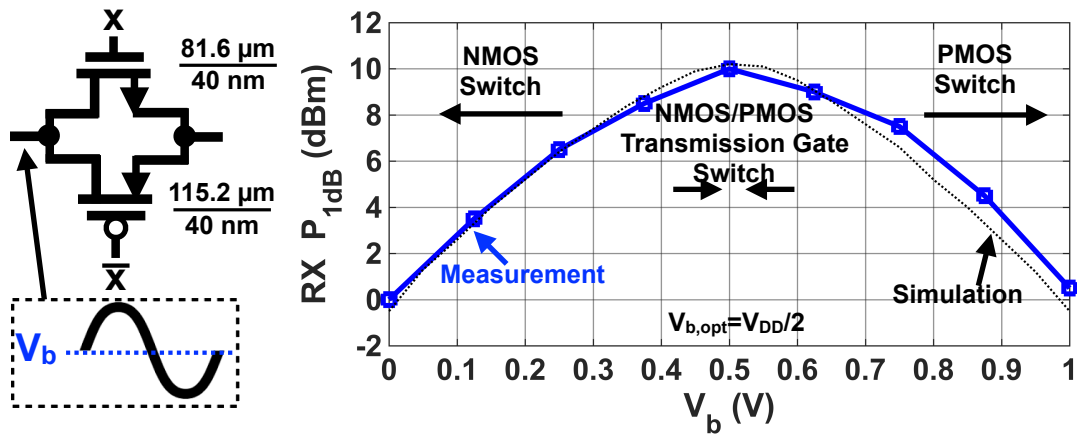


Figure 5.5: Implementation of the RF transmission gate switch with comparison of the simulated and measured 1-dB power compression.

chopper resembles a FET ring mixer but the gates are driven with relatively low speed code signals. The IAD feature is built into a standard N -path filter as a switch which equalizes the differential voltage on the N -path when the dump signal is active to reset

accumulated charge to avoid ISI in the correlation. As shown in Fig. 5.4, the IAD N -path filter has a hybrid capacitor bank with high-density capacitors and shunt capacitors to improve OOB rejection and common-mode noise generated on chip (e.g. LO leakage, dump leakage, etc.).

To improve the linearity of these receive circuits, a transmission gate (TG) is used rather than a single n-FET for the RF switches. Recent work also proposed using TG switches and measured an in-band 1-dB power compression (P1dB) of -17 dBm ($\Delta f/BW = 0$) [68]. Our measurements and simulations of the TG RF switch based on a 45-nm CMOS SOI design in Fig. 5.5 demonstrate that the TG extends the in-band P1dB to 10.1 dBm with an optimum bias ($V_b = V_{b,opt}$) that maintains the proper state of the switches (i.e. on/off) under high RF swing. Additionally, the on-resistance of the switch remains constant over a larger signal swing which improves the switch linearity. All TGs are of the same size as shown in Fig. 5.5.

5.3 Measurements

The proposed system was fabricated with GlobalFoundries 45-nm RF SOI process. The die is shown in Fig. 5.6 and occupies an area of 2.59 mm² including the pads and ESD circuitry while the active area is 1.12 mm². The RX power consumption was less than 18 mW including digital circuitry at $f_{LO} = 4f_{RF} = 4$ GHz and code rate of 200 Mcps from 1-V supply and four baseband amplifiers from 1.5-V supply.

Fig. 5.7 compares the RX performance in the presence of an in-band blocker at the same frequency as the desired RX signal at $f_{RF} = 0.5$ GHz. The spectrum is plotted for matching and orthogonal codes and illustrates a rejection of 47 dB for a QPSK signal with a spreading BW while the signal data rate is 3.125 Mbps (code lengths of $M = 64$). The measured rejection is plotted on Fig. 5.7 (bottom) for varying data rates but fixed

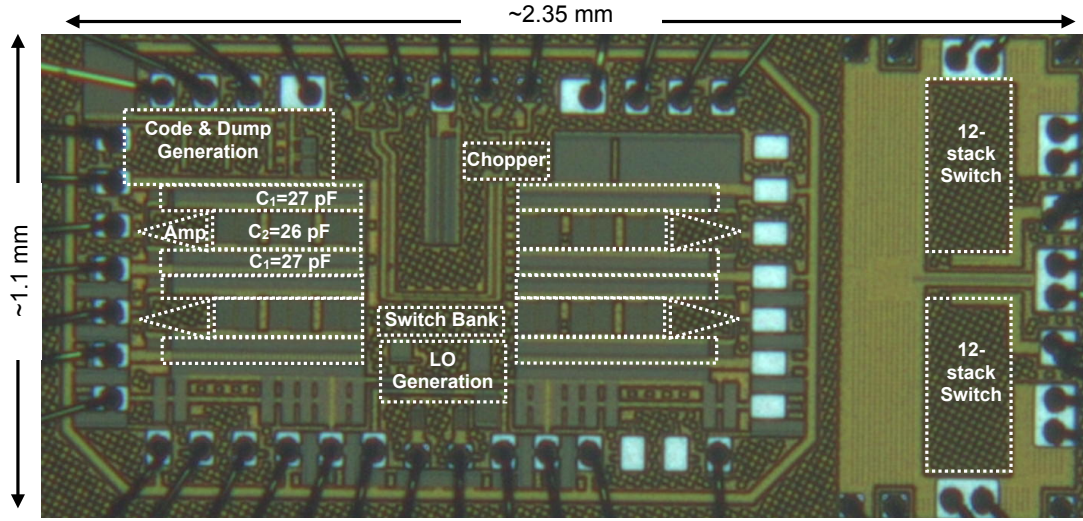


Figure 5.6: Chip micro photograph of the code-domain transceiver.

spreading bandwidth of 100 MHz. The rejection is 49.5 dB for a 0.5 GHz CW signal and reduces to 42 dB at 1 GHz with the on-chip DSSS modulator operating at 30 dBm.

The TX modulator 1-dB bandwidth extends from 400 MHz to 1 GHz and insertion loss (IL) is less than 1.6dB up to a 1-dB power compression of 34 dBm at 600 MHz as shown in Fig. 5.8 (top). The switching time is under 3ns which enables 300 MHz spread bandwidth. The TX IIP3 is measured to be 50 dBm using a two-tone measurement setup.

The IL of the RX correlator is 0.8-3.55 dB across a tuning range from 0.4 to 1.1 GHz with P1dB of 10.1 dBm and 12.6 dBm depending on the balun ratio as shown in Fig. 5.8 (bottom). The in-band IIP3 is better than 23.1 dBm across the tuning range. The NF for RX is measured at RX_{out} between 2.6 and 5.6 dB depending on f_{LO} . The gain of the auxiliary amplifiers is measured to be 30 dB. The measured RF BW of the RX correlator is 13 MHz.

The EVM is plotted as a function of TX SI power as well as signal-to-interference ratio (SIR) in Fig. 5.9 for a RX signal power of -18 dBm when the TX and RX are both

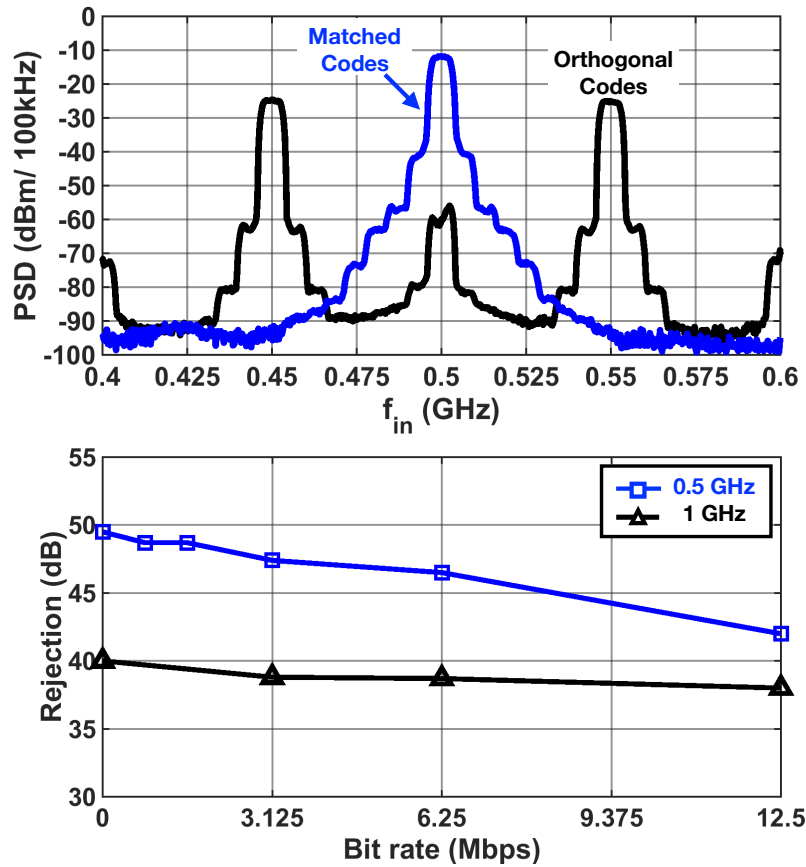


Figure 5.7: Measured spectrum for matched and orthogonal codes (top) and orthogonal rejection as a function of data rate.

at 0.5 GHz. For SIR greater than 30 dB, the noise floor limits the EVM (i.e. SNR 30 dB) to around 1%. In the absence of any TX rejection, the EVM degrades to 10% as the SIR reduces to 18 dB. When RF correlation is applied, the EVM curve is shifted by 38 dB such that the same EVM is tolerated for an SIR of -20 dB. The QPSK (bit rate of 12.5 Mbps for RX and 12.4 Mbps for TX) constellation is shown for TX SI of +10 dBm.

Finally, STAR operation is demonstrated over a short-range link with two prototype RFIC circuits mounted on PCB. This is to investigate code synchronization for the receiver which was not fully addressed in earlier work [14]. Fig. 5.10 demonstrates an over-the-air (OTA) measurement of the proposed STAR system when the transmit and receive signal are at 900 MHz. Transmitter TX_A transmits a CW tone at 900MHz

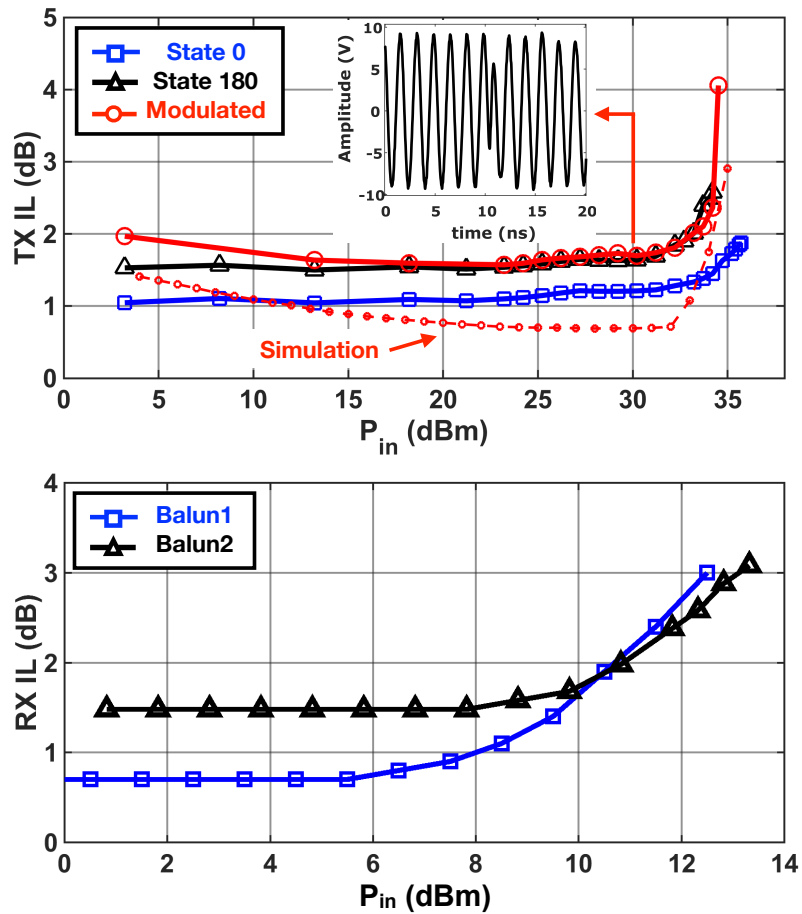


Figure 5.8: Measured in-band IL compression point of the transceiver RFIC: TX (top) and RX (bottom).

modulated with a 100 Mcps Barker code of length 11. An off-the-shelf circulator isolates the TX and RX. After propagating over a 1-m channel, the signal is received at receiver RX_B and correlated against the 11 possible timing lags for the Barker code through the observation receiver. The delay mismatch between the two transceivers (T_1) can be estimated by interpolation between the highest two peaks in the autocorrelation function. The variation in the receive power indicates a processing gain of the RX signal of at least 12 dB. The asymmetry across the peak in Fig. 5.10 is attributed to the non-ideal RC shape of the filter compared to an ideal integrator. Nevertheless, this filter shape is accurate to identify the highest peak.

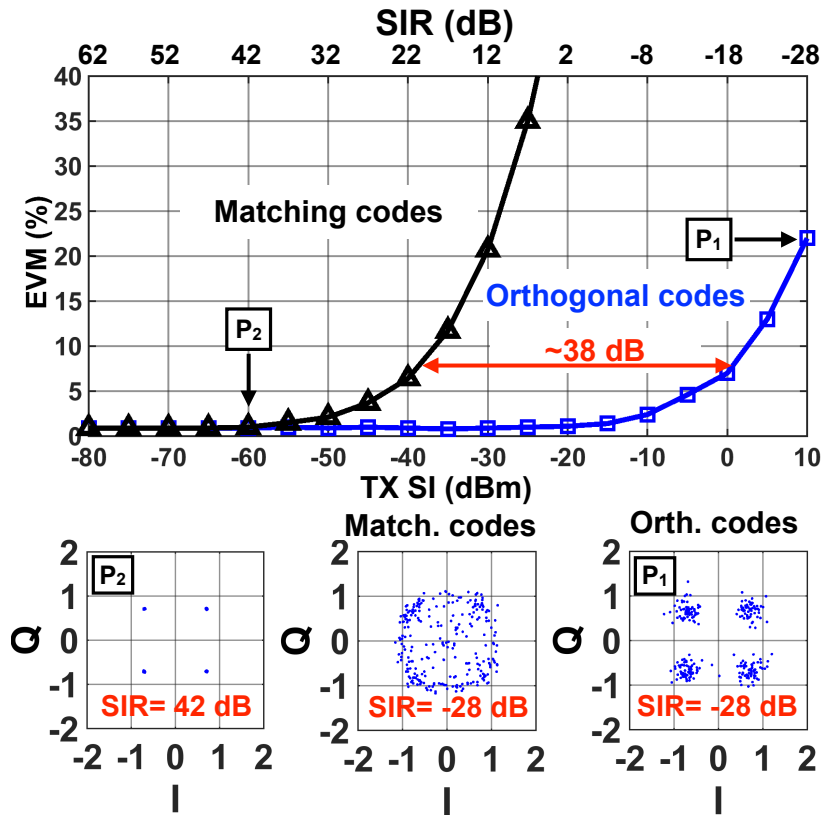


Figure 5.9: EVM as a function of transmit power and normalized to signal-to-interference ratio (SIR) and QPSK constellations at selected points.

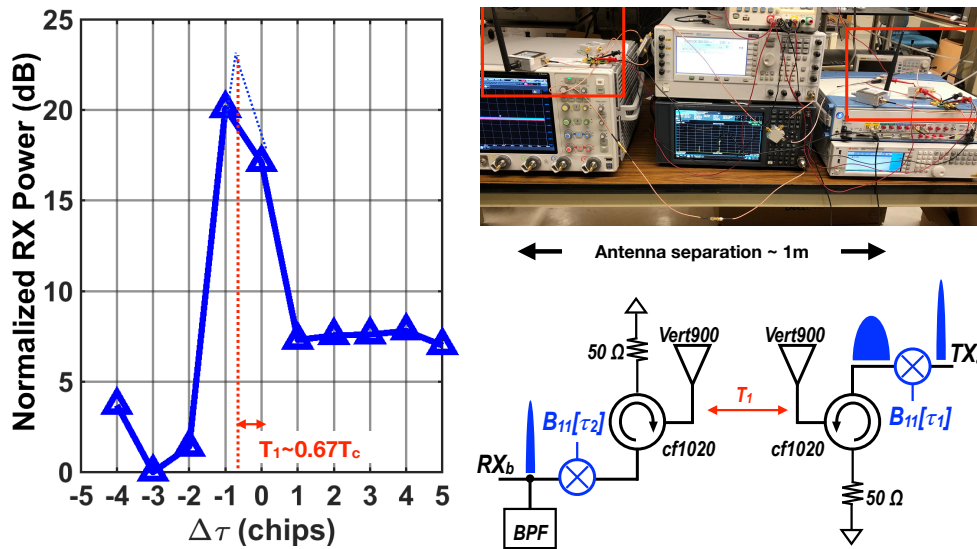


Figure 5.10: Over-the-air measurement for code synchronization and its set-up.

Table VIII shows a comparison with state of the art work on full-duplex. The proposed code-domain transceiver provide higher rejection at the antenna while also handling higher power levels and higher levels of integration. Furthermore, this work demonstrates the highest N -path linearity in terms of 1-dB compression for in-band blockers.

TABLE VIII
COMPARISON AGAINST STATE-OF-THE-ART

Spec.	[14]	[10]	[11]	[16]	[64]	[15]	[65]	This work
CMOS Process	65 nm	65 nm	180 nm	45 nm	45 nm	45 nm	65 nm	GF 45 nm SOI
Frequency (GHz)	0.30-1.40	0.61-0.97	0.86-1.08	0.30-0.675	1.10-2.50	0.90-1.10	0.40-1.00	0.40-1.10
BW (MHz)	1	20	6.8-37.4	10	1	300	NA	13
TX-RX isolation (dB)	0	20	25-40	0	31	0	NA	0
Pre-LNA SI Rejection (dB)	0	0	0	23.2	20	21.9	33	49.5
Post-LNA SI Rejection (dB)	38.5	0	0	0	0	0	0	0
BB SI Rejection (dB)	0	0	0	0	0	0	0	0
TX SI (dBm)	NA	-26	-5 to +10	NA	NA	NA	NA	+10
IB RX P1dB (dBm)	-11.8	NA	21	2	NA	NA	NA	+12.1
IB RX IIP3 (dBm)	>17	-26	36.9	6.3	NA	21.6	NA	>+23.1
RX Power Consumption (mW)	37	36	NA	28.2	50	9.37	24	18
TX Power Consumption (mW)	NA	59	170	NA	NA	NA	24	<40
TX Power Handling (dBm)	NA	8	+30.7	NA	15	NA	NA	+34.3
TX IL (dB)	NA	1.8-3.2	2.1	NA	NA	NA	NA	1.6
Active Area (mm ²)	0.31	0.94	16.5	0.9	1.4	1.77	3.1	1.12

Conclusion

This work has introduced code-domain signal processing techniques for self-interference cancellation. The design of these systems relies on the use of high-power, high modulation bandwidth modulators comprising of RF switches, preferably in CMOS processes. These switches have been previously limited in their ability to switch quickly, and thus a majority of this work is focused on how to build modulators which increase this switching speed while maintaining the same high power handling. Resistive and inductive balun modulators have been discussed and it was shown that while power handling and switching speed can be greatly improved, the limiting factor was the balun losses. As a result an alternative reflection phase shifter modulator was designed to lower the overall insertion loss and decreases the losses of the system with equally high power handling and modulation bandwidth. Additionally a method for reducing the harmonic output of these fast switching modulators was proposed, the pulse encoded transitions (PET) technique. Finally a demonstration of the code-domain approach using the designed modulators along with a receiver side integrator was presented.

There are many directions that this work can move in the future. Obvious areas of research include combining the proposed code-domain modulators with wide-band RF cancellors or integrated circulators and would be useful in proving the feasibility of the overall code-domain system. The PET algorithms have applications in many types of RF modulators, whether they be direct RF modulation techniques to improve system

efficiency, or load modulation circuits that can change the load seen by the power amplifier and boost the efficiency at back-off. Finally, the switching theory could be extended to look for solutions which allow FBWs greater than 1 and enable the construction of high linearity mixers in SOI CMOS.

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