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### Author

Dayeh, Shadi A.

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**Semiconductor Nanowires for Future Electronics: Growth, Characterization,  
Device Fabrication, and Integration**

A dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

Shadi A. Dayeh

Committee in charge:

Professor Deli Wang, Chair  
Professor Edward T. Yu, Co-Chair  
Professor Peter M. Asbeck  
Professor Prabhakar Bandaru  
Professor M. Brian Maple

2008

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Chair

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Co-Chair

University of California, San Diego

2008



To my parents

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## VITA

- 2001 Maitrise-en-Sciences, Physics and Electronics, Lebanese University, Beirut, Lebanon
- 2003 M. S., Electrical Engineering, Southern Methodist University, Dallas, TX
- 2007 C. Phil., Electrical Engineering, University of California, San Diego, CA
- 2008 Ph. D., Electrical Engineering, University of California, San Diego, CA

## PUBLICATIONS

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## **ABSTRACT OF THE DISSERTATION**

### **Semiconductor Nanowires for Future Electronics: Growth, Characterization, Device Fabrication, and Integration**

by

Shadi A. Dayeh

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Professor Deli Wang, Chair

Professor Edward T. Yu, Co-Chair

This dissertation concerns with fundamental aspects of organo-metallic vapor phase epitaxy (OMVPE) of III-V semiconductor nanowires (NWs), and their structural and electrical properties inferred from a variety of device schemes. An historical perspective on the NW growth techniques and mechanisms, and an overview of demonstrated NW devices and their performance is summarized in chapter 1.

In part I of the dissertation, OMVPE synthesis of InAs NWs on SiO<sub>2</sub>/Si and InAs (111)B surfaces is discussed and their growth mechanism is resolved. Nucleation, evolution, and the role of Au nanoparticles in the growth of InAs NWs on SiO<sub>2</sub>/Si surfaces are presented in chapter 2. Our results indicate that In droplets can lead to InAs NW growth and that Au nanoparticles are necessary for efficient AsH<sub>3</sub> pyrolysis. Chapter

3 discusses the key thermodynamic and kinetic processes that contribute to the InAs NW growth on InAs (111)B surfaces. Controversy in the interpretation of III-V NW growth is overviewed. Experimental evidence on the nucleation of InAs NWs from In droplets as well as the catalytic effect of Au nanoparticles on the InAs (111)B surfaces are described. NW cessation at high growth temperatures or at increased input molar V/III ratios is explained via a switch-over from vapor-liquid-solid (VLS) NW growth to vapor-solid thin film growth, in contrast to previous interpretation of vapor-solid-solid growth of III-V NWs. The substrate-NW adatom exchange is also treated, and experimental distinction of two NW growth regimes depending on this exchange is demonstrated for the first time. Our results indicate that when growing extremely uniform InAs NWs, solid-phase diffusion of In adatoms on the NW sidewalls is the dominant material incorporation process with surface diffusion lengths of  $\sim 1 \mu\text{m}$ . This understanding was further utilized for the growth of axial and radial InAs-InP heterostructure NWs. Polymorphism in III-V NW crystal structure is also discussed and growth conditions that lead to its observation are summarized.

In part II of the dissertation, transport coefficient extraction, field-, diameter-, and surface state-dependent transport properties, and their correlation with crystal structure in InAs NWs is presented. Chapter 4 overviews the fabrication of top-gate InAs NW field-effect transistors (NWFETs), presents a model for accurate extraction of carrier mobility and carrier concentration from NWFETs, and demonstration of high electron mobility values in InAs NWs is illustrated. Chapter 5 describes the effects of surface states on transport properties and parameter extraction from InAs NWFETs. Mobility values in excess of  $10000 \text{ cm}^2/\text{V}\cdot\text{s}$  are obtained from measurements at slow gate voltage sweep

rates at which charge balance in carrier capture and emission from interface states is achieved. Chapter 6 discusses scaling effects on the NW transport properties and provides experimental evidence of ballistic electron transport over length scales of  $\sim 200$  nm in InAs NWs at room temperature. Diameter-dependent mobility and free carrier concentration is observed and is attributed to Fermi energy pinning in the conduction band that leads to surface electron accumulation and enhanced surface scattering. Chapter 7 discusses direct correlation of InAs NW microstructures with their transport properties. Our results show that the distinct difference observed in the subthreshold characteristics between wurtzite and zinc blende InAs NWFETs is due to the presence of spontaneous polarization charges at the WZ  $\{0001\}$  plane interfaces with ZB segments. Numerical simulations point out that a polarization charge density of  $\sim 10^{13}$  cm $^{-2}$  is required to surpass surface state induced electron accumulation and result in high  $I_{on}/I_{off}$  ratios for the WZ NWFETs. Chapter 8 presents detailed experimental studies on the gate and source-drain field-dependent transport properties in InAs NWFETs. Mobility degradation at high injection fields is observed and is attributed to enhanced phonon scattering, which was verified through electro-thermal simulations and *ex-situ* transmission electron microscopy (TEM) and scanning TEM compositional studies on NWs exposed to high injection fields. Chapter 9 presents a novel scheme for III-V NW integration to the standard Si mainstream utilizing ion-cut induced transferred III-V layers to SiO $_2$ /Si. Vertically integrated and electrically isolated III-V NWs on Si are achieved for the first time. Key challenges related to growth and implementation of vertical devices in future technology nodes are also summarized.



# 1. INTRODUCTION

## 1.1 Introduction to Semiconductor Nanowires

Semiconductor device miniaturization has enabled high integration density, versatile functionality, and enhanced performance. With the current combination of materials and device architectures, further device scaling with improved performance is restricted by several technological and fundamental limits. For example, technology node feature size of 65 nm in 2007 is projected to be 13 nm by 2021,<sup>1</sup> a goal which may not be achieved with the current high-k/Si technology. New materials with controlled morphologies and desired properties are being actively researched and assessed for meeting future technological needs.<sup>2</sup>

The bottom-up assembly of nanostructured materials is an appealing strategy that may provide alternative and unconventional methods to accomplish future technological and miniaturization needs. In bottom-up assembly, the active portions of a three-dimensional (3D) device are formed by synthetic means without further structural processing. This is in contrast to the top-down processing technique in which lithography is typically used to define the active portions of a 3D device. Among different materials synthesized through the bottom up technique such as carbon nanotubes<sup>3</sup> and graphene,<sup>4</sup> semiconductor nanowires (NWs) are currently the most controlled bottom-up assembled nanostructures in several aspects including morphology over large areas, conductivity (semiconducting vs. a mixture of both semiconducting and metallic), and doping. We define semiconductor NWs as engineered one-dimensional nanostructures with diameters

in the range of  $\sim 1$  nm to  $\sim 100$ - $200$  nm. Such NWs have unusual electronic and optoelectronic properties – owed to quantum confinement effects in two dimensions – and hold great promise for next generation nanoelectronic devices.<sup>5</sup> In addition, and due to their dimensionality, semiconductor NWs enable novel axial<sup>6,7,8</sup> and radial<sup>9</sup> heterostructure growth, surround-gate field-effect transistor (FET) architectures,<sup>10,11</sup> and efficient size<sup>12</sup> and alloy<sup>13</sup> bandgap engineering. NWs of virtually any semiconductor material can be grown using the Chemical Vapor Deposition (CVD) or Molecular Beam Epitaxy (MBE) techniques or their variations. Thus, it is not surprising that research efforts have heavily concentrated on semiconductor NWs in electronics,<sup>14</sup> photonics,<sup>15</sup> thermoelectrics,<sup>16</sup> chemical sensing,<sup>17</sup> biosensors,<sup>18</sup> biostimulants,<sup>19</sup> etc. In this chapter, we provide a historical perspective on NW research, their synthesis techniques and mechanisms, demonstrated performance at the time of writing this thesis, as well as an outline of the forthcoming thesis chapters.

## 1.2 Historical Perspective

Experimental observation of anisotropic 1D semiconductor crystals, or so-called whiskers with diameters  $\geq 100 - 200$  nm, dates back to 1961 when Holonyak *et al.* observed Si whisker crystallization in the presence of large amounts of arsenic<sup>20</sup> and whose formation was greatly enhanced when nickel iodide was added.<sup>21</sup> Wagner *et al.* have performed studies of Si whisker growth from arsenic-doped Si and assisted by iodine, nickel iodide, iodides of copper, silver, manganese and cadmium, the addition of

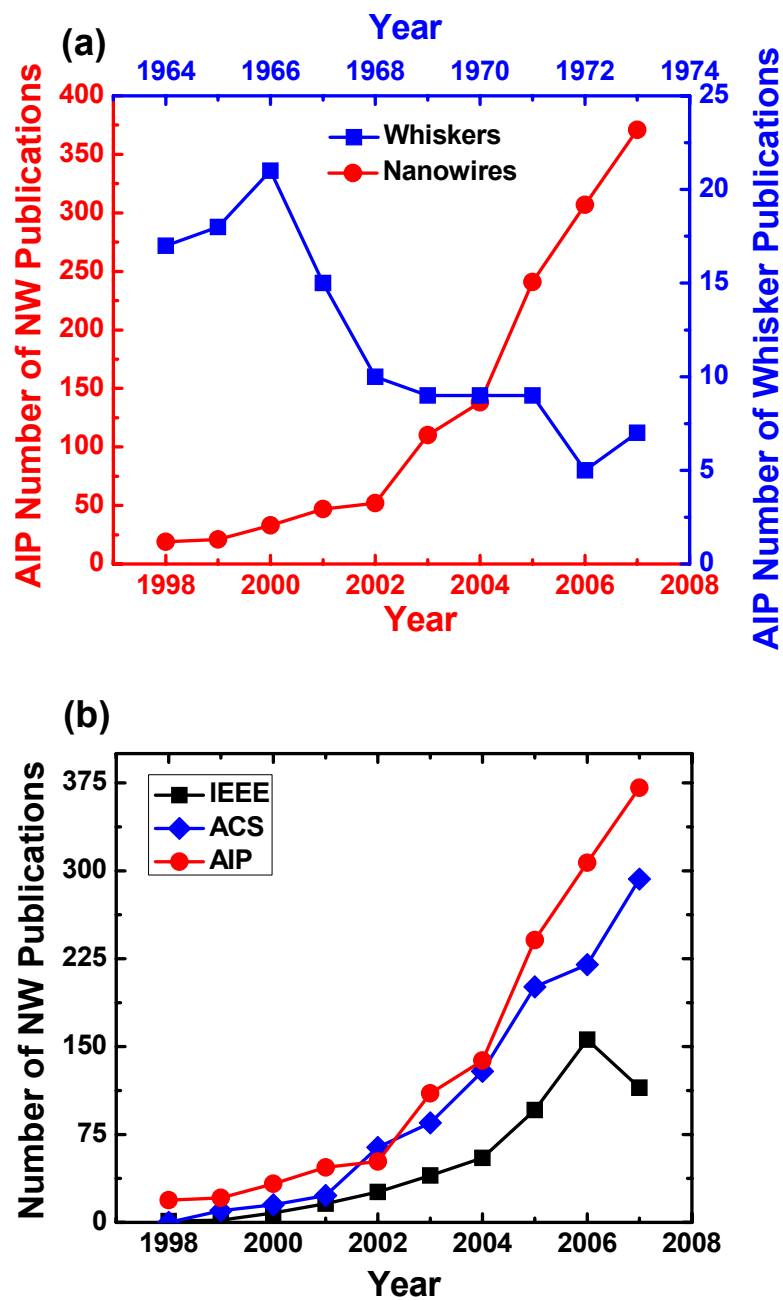


Figure 1.1. (a) Plot of the number of NW and whisker research articles from AIP over the time period of 1998 – 2007, and 1964 – 1973, respectively. (b) Plot of the number of NW research articles from IEEE, ACS, and AIP over the time period of 1998 – 2007.

which have also promoted whisker growth.<sup>22</sup> Similarly, addition of Au to high purity Si sources have resulted in abundant Si whisker growth which seemed to be dislocation free with hemispherical globules at their tips suggesting that liquid phase material existed at the whisker tip during growth. This led Wagner and Ellis to propose the Vapor-Liquid-Solid (VLS) growth mechanism.<sup>23</sup> Since then, systematic experiments to understand and control whisker growth evolved in the 1960s – 1970s involving elemental semiconductors such as Si,<sup>24</sup> Ge,<sup>25</sup> and their axial heterostructures,<sup>26</sup> as well as compound semiconductors such as GaAs,<sup>27</sup> GaP,<sup>28</sup> InAs,<sup>29</sup> and their alloys of InGaAs,<sup>29</sup> GaAsP,<sup>30</sup> etc. Despite these efforts on whisker growth, it wasn't until 1991 that Haraguchi *et al.* fabricated p-n junctions from GaAs whiskers grown using selective area metal-organic chemical vapor deposition.<sup>31</sup> A few years later, the work of A. M. Morales and C. M. Lieber who utilized VLS to prepare Si and Ge NWs with diameters of 3 – 20 nm and lengths of 1 – 30  $\mu\text{m}$ <sup>32</sup> triggered an intense world-wide research interest in the field of NWs in the context of nanoelectronics and nanophotonics. *Some* of the ground-breaking work in the decade that followed is summarized in section 1.4. Evolution of the NW research as function of time is depicted in Figure 1.1 (a) which plots the number of NW publications from the American Institute of Physics (AIP) per year over the time range of 1998 – 2007 as well as the number of whisker publications from AIP over the time range of 1964 – 1973. It can be seen from Figure 1.1 (a) that directly after the discovery of the VLS mechanism, whisker research has witnessed a slight increase which then decayed to a few number of publications in the early 1970s. For NWs however, the number of publications per year from AIP shows a super-linear and continual increase as function of time in the time period of 1998 – 2007. Physicists, chemists and engineers have had

extensive interest in NWs in the past decade. This is illustrated in Figure 1.1 (b) in the number of NW publications per year from AIP, American Chemical Society (ACS), and International Institute of Electrical and Electronic Engineers (IEEE) in the time range 1998 – 2007.

### 1.3 Nanowire Growth Techniques and Mechanisms

Semiconductor NWs can be synthesized using a variety of growth techniques including organo-metallic vapor phase epitaxy (OMVPE),<sup>33,34,35</sup> selective area OMVPE (SA-OMVPE),<sup>36</sup> molecular<sup>37</sup> and chemical<sup>38</sup> beam epitaxy, wafer annealing,<sup>39</sup> chemical vapor deposition,<sup>40</sup> laser ablation,<sup>41,42</sup> and low temperature solution methods.<sup>43</sup> In most of these NW synthesis techniques, a metal seed is utilized to initiate the 1D growth. In OMVPE, epitaxial growth of compound semiconductors via chemical reactions is achieved by final decomposition of the input reactants/precursors at the surface. This technique utilizes metal organics such as tri-methyl-indium ( $\text{In}(\text{CH}_3)_3$ ) and hydrides such as Arsine ( $\text{AsH}_3$ ) as input precursors. SA-OMVPE enables the selective epitaxy of compound semiconductors over masked regions typically with thin layers of  $\text{SiO}_2$ . MBE growth utilizes ultra-high vacuum chambers and solid as well as gas sources, where a beam of the reactants is directed toward the growth substrate, at which they condense and react at very slow growth rates when compared to OMVPE. CBE is a hybrid of OMVPE (source-wise) and MBE (species transport-wise) and sometimes is referred to MOMBE, which employs non-reactive atomic and molecular beams with long diffusion lengths at low chamber pressures. Wafer annealing is a process in which a solid source or a wafer is

heated to high temperatures to produce an excess of group III or group V in the vapor that is thermally transported to a low-temperature zone at which layer epitaxy occurs. In CVD, high quality epitaxy can be performed when the substrate is exposed to one or more volatile precursors that decompose or react at its surface. Laser ablation is a process in which a laser beam is used to heat and subsequently remove material from a solid source, which may then be used for layer epitaxy in a similar manner to CVD. Finally, solution growth techniques enable layer epitaxy in solution at much lower temperatures than those employed for vapor phase epitaxy, however, with lower control over crystallinity and purity.

The detailed mechanisms for NW growth that apply for different growth techniques and conditions remain an active subject of investigation. In the presence of catalytic metal particles, NW growth evolution is interpreted to occur via the Vapor-Liquid-Solid (VLS)<sup>33,36-41</sup> and Vapor-Solid-Solid (VSS)<sup>34,44</sup> growth mechanisms. In the absence of metal particles, their growth is interpreted via group-III catalyzed VLS growth,<sup>35,45,46</sup> oxide-assisted growth,<sup>42</sup> ligand-aided solution-solid (LSS) growth,<sup>43</sup> reactive Si-assisted growth,<sup>47</sup> and dislocation-driven growth.<sup>48</sup> Since this thesis concerns with OMVPE growth of III-V NWs using the VLS mechanism, we provide below a brief overview of this growth mechanism.

In the original work of Wagner and Ellis,<sup>23</sup> a Au particle is deposited on a Si (111) surface and heated up to 950 °C to form a Au-Si liquid droplet. H<sub>2</sub> and SiCl<sub>4</sub> are introduced and the liquid droplet acts as a preferential sink for arriving Si atoms as well as a catalyst involved in the reduction of SiCl<sub>4</sub>. Si then diffuses through the droplet and

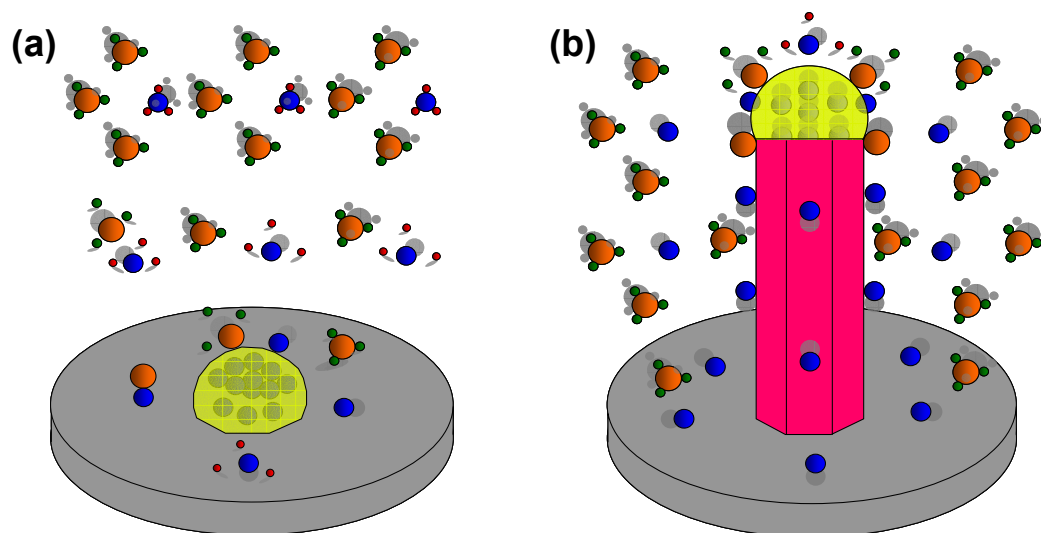


Figure 1.2. (a) Cartoon illustrating the precursor decomposition, ((•••) is TMIn, and (•••) is AsH<sub>3</sub>), and NP alloying with In forming a liquid Au-In alloy at the growth temperature. (b) Cartoon illustrating the Vapor-Liquid-Solid NW growth including continual precursor decomposition and solid-phase diffusion on the growth substrate and NW sidewalls.

freezes at the liquid-solid interface. Upon continuation of this process, the liquid droplet is displaced from the Si substrate and rides atop a solid whisker.

For III-V NWs, the VLS growth proceeds in a similar manner to that for Si, however with more complexity since it involves material reactants from group-III and group-V. Figure 1.2 shows a cartoon illustrating III-V NW VLS growth. In general, group-III from a precursor such as TMIn which is typically fully decomposed<sup>49</sup> at the NW growth temperatures forms a liquid alloy with the Au NP seed. Group-V precursor such as AsH<sub>3</sub> which is not typically fully decomposed at the NW growth temperatures either undergoes a 1:1 pyrolysis with TMIn,<sup>50</sup> or decomposes at the surface of the Au NP.<sup>51</sup> Since As solubility is low in Au-In,<sup>52</sup> As would have to diffuse at the surfaces toward the liquid-solid interface to react with ejected In from the supersaturated Au-In

alloy. This reaction at the liquid solid interface leads to NW crystallization and rise-up of the Au-In seed atop the NW.

For NW growth to proceed as described above, a number of system and growth conditions need to be satisfied, the most important of which are briefly summarized below. According to Wagner & Ellis<sup>53</sup> and Givargizov,<sup>54</sup> the NP must form a liquid solution with the material to be grown and must have a large contact angle ( $95^\circ - 120^\circ$ ) with the growth substrate to enable its rise above the surface. The chemical reactions should be thermodynamically possible but not favored kinetically so that the catalytic and adsorption properties of the liquid NP become effective in precursor decomposition and incorporation and consequently in the one-dimensional NW growth.<sup>55</sup> In addition, high supersaturations in the NP are required especially in the initial stages of growth to enable NP rise above the substrate surface.<sup>54</sup> For vertical NW growth with respect to the substrate surface, the surface must be oxide free. Thus, (111)B or As-terminated substrates are preferred over (111)A or In-terminated substrates attributed to enhanced capability to be oxidized for (111)A surfaces as well as the too large contact angles with these surfaces that cause instabilities in nucleation and growth at angles with respect to the substrate normal.<sup>56</sup> These requirements determine the temperature ranges over which NW growth is preferred, which are typically  $100 - 200^\circ\text{C}$  lower than those used in thin film growth. Within the NW growth temperature window, low temperatures may not allow the formation of the liquid NP alloy and oxide desorption, whereas high temperatures increase the material solubility in the liquid NP and reduce its supersaturation and consequently the NW nucleation and growth rates. Once the above



conditions are satisfied, NW growth is enabled and control over the NW morphology is possible, a topic that is discussed in details chapter 3 of this thesis.

#### **1.4 Demonstrated Devices and Device Performance using Nanowires**

Due to the large number of publications in the field of NWs, we provide a brief summary of some of the most significant NW device results. Because of the small electron effective mass in InAs ( $m_e=0.023 m_0$ ) that leads to pronounced quantum confinement effects, InAs NWs were utilized to in a number of interesting low-dimensional transport studies. Björk et al. have reported in 2002 on 1D resonant tunneling diodes in InAs/InP NW heterostructures that utilize 5 nm InP barriers inserted in an InAs NW creating a quantum-confined InAs island.<sup>57</sup> With bias applied across the InAs NW terminals, quantum mechanical tunneling of electrons through the barriers controlled by the available quantized energies in the InAs island, and negative differential conductance was observed with peak-to-valley current ratios of 50:1 at 4.2 K. Doh et al. have measured in 2005 tunable supercurrent through InAs NWs contacted with Al superconductor electrodes at 40 mK.<sup>58</sup> Since electrically transparent electrodes can be formed to InAs, the InAs NWs exhibited superconducting properties due to proximity effect in which electron Cooper pairs form a superconductor in a normal type conductor. Similarly, Ge, a high hole-mobility material, has been utilized in fundamental transport measurements in the core-shell Ge-Si heterostructure configuration. Xiang et al. reported in 2006 such Ge-Si core-shell NW Josephson junctions<sup>59</sup> with superconducting properties when contacted with Al contact leads similar to the case of InAs NWs.<sup>58</sup> Hu et al. have

consequently used the same material system (Ge-Si core-shell NWs) with controlling top gates to form a double quantum dot (DQD) in Ge-Si NW coupled capacitively by another gate to a single quantum dot in another Ge-Si NW, thus enabling single electron charge transfer in the DQD.<sup>60</sup>

In addition to these fundamental studies in quantum confined NWs, the NW field-effect transistor (NWFET) has been researched as a potential candidate for beyond-the-roadmap logic applications. Here, we discuss a number of the most significant results in VLS synthesized NWFETs and compare them to top-down processed NWFETs and planar CMOS FETs. To do so, we utilize a number of the benchmarking metrics introduced by Chau et al. in 2005,<sup>2</sup> and by Cohen et al. in 2008.<sup>61</sup> In particular, we use the method of Chau et al. for calculating the  $I_{on}/I_{off}$  ratio (when not stated in the original paper) by considering the  $I_{on}$  current at  $V_G + 2/3 V_{DD}$  and  $I_{off}$  at  $V_G - 1/3 V_{DD}$ . When comparing NW to planar CMOS, several researcher have normalized the on-state currents and transconductances to either the NW diameter or NW perimeter. In addition to the error introduced to the gate width by doing so, this method does not account for oxide-equivalent-thickness differences between devices under comparison and their channel lengths. Cohen et al. have used a new metric for this comparison, namely  $I_{on-norm} = I_{on} L_g / C$  ( $A \cdot cm^2 / F$ ) which takes into account geometrical and material differences in device comparison, where  $C$  is the NW capacitance per unit length. Table 1 shows a summary for devices and materials under consideration. This includes NWFETs fabricated from bottom up synthesized Si NWs,<sup>61</sup> Ge-Si core-shell NWs,<sup>62</sup> Ge-Si core-shell NWs with silicided nano contacts,<sup>63</sup> InAs NWs,<sup>64</sup> top-down processed Si NWs,<sup>65</sup> and planar CMOS FET.<sup>61</sup> The device materials and physical dimensions are also included

in Table 1. For p-type FETs, Ge cores with  $\sim 25$  nm diameter and  $\sim 2$  nm Si shells have shown hole mobility values of  $\sim 640$   $\text{cm}^2/\text{V}\cdot\text{s}$ . This high hole mobility value was attributed to the formation of a hole-gas at the Ge-Si interface.<sup>66</sup> This, however, is still lower than CVD grown strained Ge on  $\text{Si}_{0.5}\text{Ge}_{0.5}$  which have shown hole mobility values of  $\sim 1700$   $\text{cm}^2/\text{V}\cdot\text{s}$  for 12 nm Ge epitaxial layers.<sup>67</sup> For n-type FETs, InAs NWs have

Table 1.1. Comparison of FET device performance for a sample of bottom-up NWs (a – d), a Si top-down NW (e), and a planar CMOS n-FET (a).

	Si <sup>a</sup> bottom-up	Ge-Si <sup>b</sup> bottom-up	Ge-Si <sup>c</sup> bottom-up	InAs <sup>d</sup> bottom-up	Si <sup>e</sup> top-down	Si <sup>a</sup> Planar
Orientation	<112>	<110>	<110>	<0001>	-	-
polarity	n	p	p	n	n	n
$D$ (nm)	17	27	16	50 $\pm$ 10	10	-
$L_G$ (nm)	515	190	40	50	130	515
Oxide $t_{ox}$ (nm)	SiO <sub>2</sub> 7.4	HfO <sub>2</sub> 4	HfO <sub>2</sub> 4	HfO <sub>2</sub> 10	SiO <sub>2</sub> 5	SiO <sub>2</sub> 7.4
$V_{DS}$ (V)	1	1	0.5	0.5	1.5	-
$\mu_{FE}$ ( $\text{cm}^2/\text{V}\cdot\text{s}$ )	> 300	640	-	>10000	600	-
$I_{on-norm}$ ( $\text{A}\cdot\text{cm}^{-2}/\text{F}$ )	> 200	88	75.5	6.45	43	$\sim 90$
$g_{m-norm}$ ( $\text{S}\cdot\text{cm}^{-2}/\text{F}$ )	-	143	45.5	8.34	-	-
$S.S.$ mV/decade	63 – 75	100	140	100 $\pm$ 8	72 – 74	-
$DIBL$ (mV/V)	<10	1450	1000	60	4-12	-
$I_{on}/I_{off}$	$\sim 10^5$	$\sim 10$	$<10^2$	$10^3$	$>10^8$	-

[a] G. M. Cohen, S. Bangsaruntip, S. Laux, M. J. Rooks, J. Cai, and L. Gignac, *DRC Tech. Dig.*, 187 (2008).

[b] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, *Nature* **441**, 489 (2006).

[c] H. Yongjie, J. Xiang, G. Liang, Y. Han, C. M. Lieber, *Nano Lett.* **8**, 925 (2008).

[d] C. Thelander, L. E. Fröberg, C. Rehnstedt, L. Samuelson, and L.-E. Wernersson, *Elect. Dev. Lett.* **29**, 206 (2008).

[e] Y. Tian, R. Huang, Y. Wang, J. Zhuge, R. Wang, J. Liu, X. Zhang, and Y. Wang, *IEEE IEDM'07 Proceedings*, 895 (2007).

shown room-temperature mobility values in excess of  $10000 \text{ cm}^2/\text{V}\cdot\text{s}$ , extracted through simulation,<sup>11</sup> lower than that of bulk InAs ( $33000 \text{ cm}^2/\text{V}\cdot\text{s}$ ). Mobility values in InAs NWs in excess of  $10000 \text{ cm}^2/\text{V}\cdot\text{s}$  have been measured by us.<sup>68</sup> The bottom-up synthesized Si NWs have shown, remarkably, the highest  $I_{on-norm}$  when compared to other devices and in particular to that of InAs, as well as when compared to bulk n-FET fabricated at IBM with similar gate length and dielectric thickness.<sup>61</sup>

For InAs surround gate NWFETs,  $I_{on-norm}$  does not account for the underlap regions of the channel length, i.e. the un-gated NW regions between the source and drain, which are several times larger than  $L_G$  and contribute to a significant series resistance. It worth to note that p-type Si NWFETs have also shown decent and comparable performance when compared to planar p-FET counterpart with the same channel length and oxide thickness. Cohen et al. attributed this high performance to the low ohmic contact resistance obtained in these NWs by ion-implanting the source and drain regions. P-type Ge-Si core-shell NWs show the highest  $I_{on-norm}$  and  $g_m-norm$  among the devices listed in Table 1. Near ideal inverse subthreshold slope ( $60 \text{ mV/decade}$ ) was obtained from VLS and top-down Si NWFETs (for both p-type and n-type) and decent ones were obtained from Ge-Si and InAs NWFETs. Tunnel or impact ionization FETs, which exploit band-to-band tunneling for carriers below the  $k_bT$  spread of  $f(E)$ , allow these devices to achieve subthreshold slopes  $< 60 \text{ mV/decade}$ .  $k_b$  is Boltzmann's constant,  $T$  is the temperature,  $E_F$  is the Fermi energy, and  $f(E)$  is the Boltzmann distribution function. Recently, Björk et al. have demonstrated a  $6 \text{ mV/decade}$  inverse subthreshold slope in vertical Si NWFETs at room temperature.<sup>69</sup> However, the presence of tunnel barriers in such devices leads to reduction of on-state currents when compared to

conventional FETs. The drain-induced barrier lowering (DIBL) that accounts for short channel effects for Si NWFETs are superior to all other devices, particularly for the omega-gate Si VLS NWFET when compared to the top-gate Ge-Si ones. The surround gate InAs NWFET with extension regions have shown decent DIBL effect but at the expense of transconductance and on-currents as indicated above. Finally, Si NWFETs have also shown the highest  $I_{on}/I_{off}$  ratios when compared to other devices in Table 1 due to the larger band-gap of Si (1.12 eV) when compared to Ge (0.64 eV) and InAs (0.34 eV).

Rapid progress has also occurred in NW optoelectronics, thermoelectrics, and bio-applications. Huang et al. reported in 2001 ZnO ultraviolet NW lasers operating at 385 nm emission wavelength.<sup>70</sup> Blue laser emission from individual GaN NWs has been observed by Johnson et al. in 2002.<sup>71</sup> In 2005, Qian et. al. reported GaN core  $\text{In}_x\text{Ga}_{1-x}\text{N}$ -GaN-p-AlGaIn-p-GaN multishell NW light emitting diodes with tunable wavelength emission from 365 – 600 nm by changing the In mole fraction.<sup>72</sup> Very recently, roughened VLS<sup>16</sup> and top-down processed<sup>73</sup> Si NWs, with poor thermal conductivity and good electrical one, have yielded a high ZT of 0.6 at room temperature, a value that cannot be achieved with bulk Si. In bio applications, Patolsky et al. in 2006 have used Si NWFET arrays to detect, stimulate, and/or inhibit neuronal signals when interfaced with individual axons and dendrites of live mammalian cells.<sup>19</sup> Kim et al. have cultured human embryonic kidney cells and mouse stem cells on vertically aligned Si NWs, the latter of which maintained cardiac myocytes for several days.<sup>74</sup> These examples are clear indication of the potential impact of NWs in a wide range of science and technology disciplines.

## 1.5 Thesis Overview

This thesis encompasses two inter-related categories of materials and device research focusing on organo-metallic vapor phase epitaxy (OMVPE) of InAs NWs and analysis of their electronic transport properties in a variety of device schemes. Thus, the thesis is organized into two parts. Part I concerns the OMVPE synthesis of InAs NWs on SiO<sub>2</sub>/Si and InAs (111) B surfaces, whereas part II concerns 2- and 3-terminal device fabrication, measurement, and transport analysis, as well as heterogeneous integration of InAs NWs on Si.

Despite the numerous amounts of reports on III-V NW synthesis in the literature, the detailed mechanisms of NW growth remains an active subject of debate. In chapter 2 of this thesis, SiO<sub>2</sub>/Si (001) substrates are utilized to study the nucleation, evolution, and role of Au NPs in the InAs NW growth. Due to the chemical inertness of the SiO<sub>2</sub> surface with respect to InAs, and through systematic characterization of InAs NW morphology as a function of input V/III precursor ratio, precursor flow rates, growth temperature and time, and the presence or absence of Au nanoparticles, a number of significant insights into the InAs NW growth have been developed. Specifically, we found that (i) the growth of InAs NWs can be initiated from a single Indium (In) droplet, (ii) Au nanoparticles enhance group V precursor (AsH<sub>3</sub>) pyrolysis but are not necessary to nucleate NW growth, (iii) growth of InAs NWs on SiO<sub>2</sub> substrates occurs in the kinetically limited VLS growth regime, (iv) InAs NWs on SiO<sub>2</sub> films decompose at elevated temperatures even under significant AsH<sub>3</sub> overpressure, and (v) the V/III ratio is the growth-rate limiting factor in the VLS growth of the InAs NWs. These results elucidate the role of Au

nanoparticles in the growth of InAs NWs as well as the nucleation and evolution of the nanowire growth via the VLS growth mechanism.

In chapter 3, we discuss several aspects of the InAs NW growth on InAs (111)B substrates, and the key thermodynamic and kinetic processes that contribute to achieving optimal control over the InAs NW morphology. When applicable, a comparison with GaAs NW growth and other III-V NWs is provided. In particular, we examine first the nucleation of InAs NWs on InAs (111)B substrates in the presence or absence of Au nanoparticles, at high TMIn flow rates, and in the absence of any input precursor in a sealed tube system. We show that excess liquid In nucleates InAs NWs on InAs (111)B substrates during their OMVPE growth through the VLS mechanism. The excess liquid In can be supplied either from the input precursor or from the substrate decomposition that is enhanced in the presence of Au nanoparticles. In a closed system, the InAs NW growth confirms the catalytic decomposition of the InAs (111)B substrate by Au nanoparticles and shows that both group-III and group-V constituents decomposed from the growth substrate can be incorporated into the NWs. InAs NWs were also observed to grow from pre-deposited In droplets on the InAs (111)B substrate surface. Faceted tips with periodic instability in the diameter of long NWs were observed due to fluctuations in the curvature of the In droplet. These insights reveal the catalytic effect of Au nanoparticles and the growth of InAs NWs from In droplets on InAs (111)B substrates.

Secondly, the effect of substrate temperature and input V/III ratio on the growth of InAs NWs on InAs (111)B substrates is investigated. Temperature-dependent growth was observed within certain temperature windows that are highly dependent on the input

V/III ratios. This dependence was found to be a direct consequence of the drop in NW nucleation with increasing the V/III ratio at a constant growth temperature due to depletion of indium at the NW growth sites, and thus reduction of nanoparticle supersaturation. The growth rate was found to be determined by the local V/III ratio, which is dependent on the input precursor flow rates, growth temperature, and substrate decomposition. These studies support the validity of the VLS mechanism for growth of III-V NWs and improving the control over their growth morphology.

Thirdly, new fundamental insights into the NW nucleation and evolution of InAs NWs were obtained from time-dependent growth studies performed at two input group-III flow rates and the first experimental distinction between two growth regimes defined by the substrate-NW adatom exchange is achieved. At low group-III flow, no substrate-to-NW diffusion occurs – in contrast to what is commonly believed – and the NW growth proceeds at an exponential rate for NW lengths ( $L_{NW}$ ) less than the group-III diffusion length on the NW surface ( $\lambda_{NW}$ ) followed by an asymptotic-linear growth rate when  $L_{NW} > \lambda_{NW}$ . Both the Au-In alloy at the NW tip and the growth substrate act as material sinks in this case. On the other hand, large group-III flow allows longer surface diffusion lengths on the substrate and substrate-to-NW diffusion prevails allowing earlier NW nucleation and an increased growth rate that proceeds sub-linear for  $L_{NW} > \lambda_{NW}$  and asymptotic for  $L_{NW} < \lambda_{NW}$ . By extracting  $\lambda_{NW}$  and controlling the growth regime, axial and radial heterostructure NW growth is feasible. These results not only improve our understanding of the fundamental aspects of NW growth but also set a limit for the lengths of NWs over which optimum control over NW morphology is possible.



In Part II of this thesis, we present electron transport studies performed on 2- and 3-terminal InAs NW devices, extraction of their transport coefficients and analysis of their transport behavior, as well as a demonstration of a feasible method for integration of III-V NWs to Si. In chapter 4, fabrication of InAs NWFETs on  $\text{SiO}_2/\text{n}^+\text{-Si}$  with a global  $\text{n}^+\text{-Si}$  back-gate and sputtered  $\text{SiO}_x/\text{Au}$  underlap top-gate is presented. For top-gate NWFETs, a model that allows accurate estimation of characteristic NW parameters including carrier field-effect mobility and carrier concentration by taking into account series and leakage resistances, interface state capacitance, and top-gate geometry, is developed. Both the back-gate and the top-gate NWFETs exhibited room-temperature field-effect mobility as high as  $6,580 \text{ cm}^2/\text{V}\cdot\text{s}$ , which is the lower bound value without interface capacitance correction. The model developed and the high electron mobility obtained from these NWs have stimulated extensive experiments discussed in the subsequent chapters in this thesis.

In chapter 5, we show that interface trap states have pronounced effects on carrier transport and parameter extraction from top-gate InAs nanowire field effect transistors (NWFETs). Due to slow surface state charging and discharging, the NWFET characteristics are time dependent with time constants as long as  $\sim 45 \text{ s}$ . This was also manifested in a time-dependent extrinsic transconductance that severely affects carrier mobility and carrier density determination from conventional three-terminal current-voltage characteristics. Slow gate voltage sweep rates result in charge balance between carrier capture and emission from interface states and lead to reduced hysteresis in the transfer curves. The gate transconductance is thus increased and intrinsic NW transport parameters can be isolated. In the InAs NWFETs, a carrier mobility value of  $\sim 16000$

$\text{cm}^2/\text{V}\cdot\text{s}$  was obtained from the transfer curves at slow sweep rates, which is significantly higher than  $\sim 1000 \text{ cm}^2/\text{V}\cdot\text{s}$  obtained at fast sweep rates. A circuit model that takes into account the reduction in the extrinsic transconductance is used to estimate an interface state capacitance to be  $\sim 2 \mu\text{F}/\text{cm}^2$ , a significant value that can lead to underestimation of carrier mobility.

In chapter 6, we first study the effects of channel length and diameter scaling on the transport properties of InAs NWs. Conductive atomic force microscopy is used to characterize distance-dependent electron transport behavior in InAs NWs. For this, a conducting diamond-coated tip as a local electrical probe in an atomic force microscope was used, and the resistance of the InAs NW has been measured as a function of electron transport distance within the NW. Two regimes of transport behavior were observed: for distances of  $\sim 200 \text{ nm}$  or less, resistance independent of electron transport distance, indicative of ballistic electron transport, is observed; for greater distances, the resistance is observed to increase linearly with distance, as expected for conventional drift transport. These observations are in very good qualitative accord with the Landauer formalism for mesoscopic carrier transport, and the resistance values derived from these measurements are in good quantitative agreement with carrier concentrations and mobilities determined in prior experiments presented in chapters 4 and 5. These results provide direct information concerning distances over which ballistic transport occurs in InAs NWs. Secondly, the room-temperature transport properties of InAs NWFETs as function of their diameters are discussed. Due to their field dependence, device analysis that enables extraction of the transport coefficients at constant vertical and lateral fields is developed and utilized for a set of 26 top-gate InAs NWFET devices with diameters in the range of

62 – 115 nm. Room temperature field-effect mobility values of 625 – 3600 cm<sup>2</sup>/V·s with correspondent free carrier concentrations of  $1.6 \times 10^{18} - 4 \times 10^{17}$  cm<sup>-3</sup> at zero gate bias were computed. Diameter dependences of mobility and carrier concentration are attributed to surface Fermi energy pinning in the conduction band that leads to a surface electron accumulation layer with enhanced surface scattering. Assuming the presence of a fixed positive charge of  $Q_f/q = 2.7 \times 10^{12}$  cm<sup>-3</sup>, one dimensional Schrödinger-Poisson solutions for different InAs slab thicknesses show that the average integrated carrier concentration increases as the InAs slab thickness is reduced, in agreement with the experimentally extracted values in the InAs NWs.

In chapter 7, we directly correlate the microstructure of InAs NWs and their individual electronic transport behavior at room temperature. Pure zincblende (ZB) InAs NWs grown on SiO<sub>2</sub>/Si substrates were found to be characterized by a rotational twin along their growth-direction axis while wurtzite (WZ) InAs NWs grown on InAs (111)B substrates have numerous stacking faults perpendicular to their growth-direction axis with small ZB segments. From transport measurements on back-gate NWFETs fabricated from both types of NWs, we observe significantly distinct subthreshold characteristics ( $I_{on}/I_{off} \sim 2$  for ZB NWs and  $\sim 10^4$  for WZ NWs) despite only a slight difference in their transport coefficients. We attribute this difference to the presence of spontaneous polarization charges at the WZ/ZB interfaces that suppress carrier accumulation caused by interface charges at the NW surface, thus enabling to full depletion of the WZ NW FET channel. We have used two-dimensional Silvaco-Atlas simulations for ZB and WZ channels to analyze subthreshold current flow and found that a polarization charge density  $\sim 10^{13}$  cm<sup>-2</sup> leads to good agreement with experimentally observed subthreshold

characteristics for a WZ InAs NW in the presence of surface state densities in the  $5 \times 10^{11}$  –  $5 \times 10^{12}$   $\text{cm}^{-2}$  range.

In chapter 8, we present detailed studies of the field dependent transport properties of InAs NWFETs. Transconductance dependence on both vertical and lateral fields is discussed. Velocity-field plots are constructed from a large set of output and transfer curves which show negative differential conductance behavior and marked mobility degradation at high injection fields. Two dimensional electro-thermal simulations at current densities similar to those measured in the InAs NWFET devices indicate that a significant temperature rise occurs in the channel due to enhanced phonon scattering that leads to the observed mobility degradation. Scanning transmission electron microscopy measurements on devices operated at high current densities reveal Arsenic vaporization and crystal deformation in the subject nanowires.

In chapter 9, we develop and implement a novel scheme for III-V NW integration to Si substrates that allows vertical integration, electrical isolation, and individually addressable III-V NWs on Si for 3D circuit applications. This integration scheme utilizes the smart-cut® technique – typically used for producing Silicon-on-Insulator (SOI) wafers – to transfer InAs (111)B layers onto  $\text{SiO}_2/\text{Si}$ . After wet etching, planarization and activation of the transferred InAs layers for growth, InAs NW arrays were grown at specified locations followed by etching InAs islands at the base of the grown NWs, suitable for electrical contacts. This results in vertical and electrically isolated InAs NWs on  $\text{SiO}_2/\text{Si}$  suitable for high performance 3D III-V circuits on Si with simple device architecture and physics of operation. The last section of chapter 9 discusses key remaining challenges for the growth and integration of III-V NWs as well as related

device issues for future electronics applications. Appendix I contains Matlab scripts for energy-subband calculation in InAs NWs used in chapter 6. Appendix II encloses Silvaco-Atlas script for self-consistent Schrödinger-Poisson solutions used in chapter 6, script for simulating the effects of polarization and surface charges in WZ and ZB InAs NWs presented in chapter 7, script for electro-thermal simulations presented in chapter 8, and script for simulating the output and transfer curves of 3D surround gate InAs-GaAs core-shell NWs presented in chapter 10.

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## 2. INDIUM ARSENIDE NANOWIRE GROWTH ON $\text{SiO}_2$ SUBSTRATES: NUCLEATION, EVOLUTION, AND ROLE OF GOLD NANOPARTICLES

### 2.1 Introduction

The growing interest in semiconductor nanowires (NWs) for electronic and photonic applications<sup>1,2,3,4</sup> necessitates rational control over their structure and key properties, and therefore a thorough understanding of the growth mechanisms specific to the growth technique and material system. Metal-assisted NW growth for Group IV, II-VI and III-V semiconductor material systems was envisioned to occur via the vapor-liquid-solid (VLS) mechanism<sup>5</sup> for growth of Si whiskers, in which a liquid metal alloy (Au-Si) initiates the growth of a solid whisker (Si) from vapor reactants. However, there are some recent reports on different possibilities than VLS growth, such as Ti-catalyzed growth of Si NWs in which the Ti seed particle is believed to remain in the solid phase during Si NW growth<sup>6</sup> in a process analogous to the VLS mechanism, and the growth of GaAs NWs from Au nanoparticles where the Au nano-catalysts could possibly remain in solid phase during NW growth, as indicated by TEM analysis, at temperatures above those used for NW growth.<sup>7</sup> This growth mechanism was proposed to be the vapor-solid-solid (VSS) growth mechanism, which relies on the solid-phase diffusion of a single component (Group III) through a solid seed particle. The observation of cessation of InAs NW growth at temperatures higher than the “melting temperature” of Au-In alloy was taken to be further evidence for the VSS growth mechanism.<sup>8</sup>

While NW growth is often initiated by Au nanoparticle catalysts, NW growth in the absence of a “foreign” metal catalyst has been reported using various growth techniques such as (1) the growth of GaAs and AlGaAs on GaAs (111)B substrates using selective-area metal organic vapor phase epitaxy (SA-MOVPE),<sup>9</sup> (2) epitaxial growth of In-catalyzed InP NWs on InP (111)B substrates,<sup>10</sup> (3) oxide-assisted growth of GaAs NWs on Si substrates through laser ablation of a mixture of GaAs and GaO<sub>3</sub>,<sup>11</sup> and (4) Au-free epitaxial growth of InAs NWs on InP (111)B and InAs (001) substrates.<sup>12</sup> These examples of the growth of NWs in the absence of the metal particle raise the question of the particle’s role in metal-assisted NW growth.

## 2.2 Summary of Results

In this chapter, we present studies of nucleation and growth of InAs NWs on SiO<sub>2</sub>/Si substrates in an OMVPE reactor, and systematic characterization of InAs NW morphology as a function of V/III precursor ratio, precursor flow rates, substrate growth temperature, growth time, and the presence or absence of Au nanoparticles. The SiO<sub>2</sub> surface provides a unique platform for studying InAs NW growth, particularly as a function of input V/III ratio, because there is no local alteration of input V/III ratio from the SiO<sub>2</sub> substrate surface, in contrast to the influence of substrate decomposition for growth on InAs substrates.<sup>13</sup> Our results indicate that (i) the growth of InAs NWs can be initiated from In droplets, (ii) Au nanoparticles (NPs) enhance AsH<sub>3</sub> pyrolysis but are not necessary to nucleate NW growth, (iii) growth of InAs NWs on SiO<sub>2</sub> surfaces occurs in the kinetically limited Vapor-Liquid-Solid (VLS) growth regime, (iv) InAs NWs on SiO<sub>2</sub>

films decompose at elevated temperatures even under significant  $\text{AsH}_3$  over pressure, and (v) the V/III ratio is a growth rate limiting factor in the VLS growth of the InAs nanowires. Transmission electron microscope (TEM) analysis on these NWs reveal zinc blende crystal structure and  $\langle 110 \rangle$  growth orientation.

### 2.3 Experimental

InAs NW growth was performed in a horizontal OMVPE reactor at a pressure of 100 Torr with Trimethylindium (TMIn) and Arsine ( $\text{AsH}_3$ ) precursors in 1.2 slm (Standard Liters per Minute)  $\text{H}_2$  carrier gas. Growth was conducted over a substrate temperature range of 300-390 °C on Si substrates with 600 nm thermally grown oxide. 40 nm diameter Au nanoparticles from colloidal solution were dispersed on the substrate surface prior to growth at an average particle density of 0.21 particles/ $\mu\text{m}^2$ . For all growth experiments, the temperature was ramped up at a rate of  $\sim 2$  °C/s, and allowed to stabilize at the growth temperature in  $\text{H}_2$  ambient. The reaction precursors were introduced for the duration of the growth run, after which  $\text{AsH}_3$  flow was maintained during the cool down for 2 minutes followed by a 2 min  $\text{H}_2$  purge; the reactor was then left in  $\text{N}_2$  ambient till sample removal. The input V/III precursor ratio was varied between  $\sim 30 - 90$  by adjusting the  $\text{AsH}_3$  flow rate (44 – 134  $\mu\text{mol}/\text{min}$ ) and maintaining a constant TMIn flow rate of 1.5  $\mu\text{mol}/\text{min}$ . The growth times were varied in the range of 30-600 s. The morphology of nanoparticles and NWs was characterized using an FEI XL 30 Environmental Scanning Electron Microscope (ESEM) operating at 10 KV acceleration voltage. Dimensions and statistical distributions of nanoparticles, islands,

and InAs NWs were determined in each case by measuring the sizes of 50 particles or wires at  $\sim 600,000$  X magnification.

## 2.4 The Role of Au Nanoparticles

The catalytic effect of Au nanoparticles in NW nucleation and growth is of critical importance to the understanding of their growth mechanism, and has been the subject of extensive recent studies.<sup>5-12</sup> However, the significant catalytic effect of Au nanoparticles to precursor pyrolysis in NW growth received less attention. Specifically, it is known that Au has the ability to form the weakest bonds and hence has the highest surface reactivity among all metals.<sup>14</sup> Therefore, the pyrolysis temperatures of the precursors are expected to be lower when Au is present in the chamber. In order to study the catalytic effect of Au nanoparticles on precursor pyrolysis, we have investigated the nucleation of InAs NWs on SiO<sub>2</sub>/Si substrates (i.e. a non-reactive substrate) in the presence or absence of Au nanoparticles at different growth temperatures. Figure 2.1 (a) shows a schematic of the experiment design with varying growth temperature, precursor input sequence, and the presence or absence of the Au nanoparticles indicated for each experiment (I-VIII).

In experiment I, 40 nm diameter Au nanoparticles were dispersed on the SiO<sub>2</sub>/Si substrate at a particle density of  $\sim 10$  particles/ $\mu\text{m}^2$  and TMIn flow (6  $\mu\text{mol}/\text{min}$ ) was introduced for 6 minutes at 350 °C. The diameter of the nanoparticles increased to  $\sim 50 - 200$  nm and a spherical shape is maintained due to Au-In alloying, as shown in Figure 2.1 (b). This occurs because at 350 °C and in H<sub>2</sub> ambient, TMIn pyrolysis is complete on

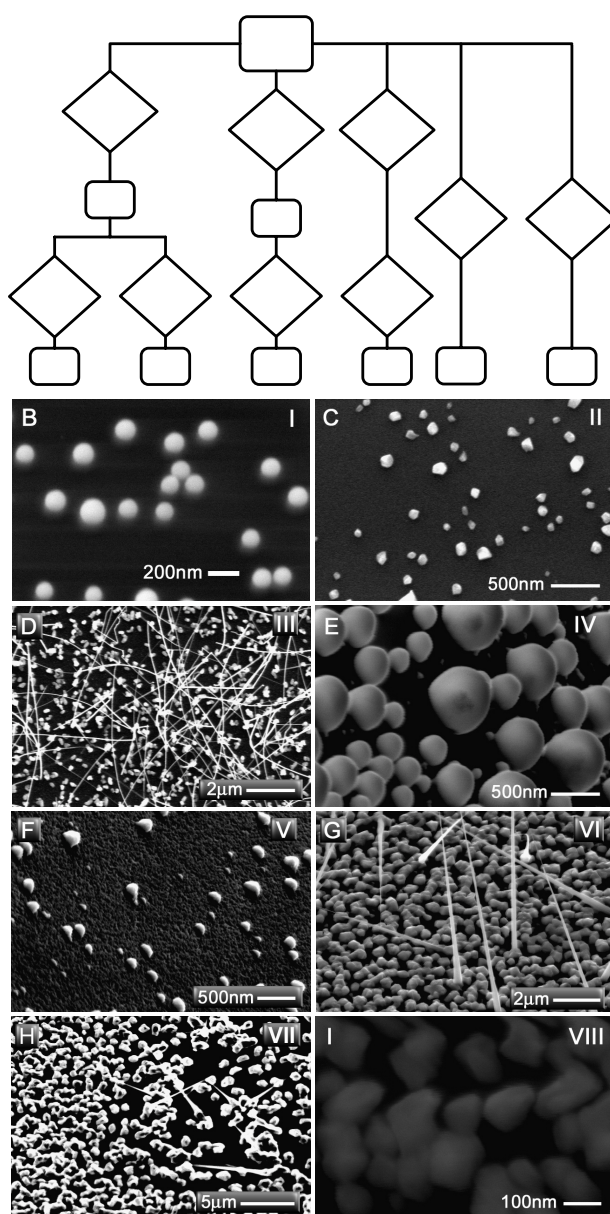


Figure 2.1. (A) Schematic diagram showing MOCVD growth experiment details on  $\text{SiO}_2$  substrate. SEM images of (B) In-Au nanoparticles after TMIn exposure, (C) half of sample in (B) after  $\text{AsH}_3$  exposure, (D) half of sample in (B) after  $\text{AsH}_3$  and TMIn exposure. In the absence of Au nanoparticles, SEM images of (E) In droplets formed after TMIn exposure, (F) sample in (E) after TMIn and  $\text{AsH}_3$  exposure, (G) same as in (E) at a growth temperature of  $500^\circ\text{C}$ , (H) InAs NWs grown on  $\text{SiO}_2$  surface after TMIn and  $\text{AsH}_3$  flow at  $500^\circ\text{C}$ , (I) InAs islands formed on  $\text{SiO}_2$  surface after TMIn and  $\text{AsH}_3$  flow at  $350^\circ\text{C}$  with no NW growth.

SiO<sub>2</sub> surfaces.<sup>15</sup> This substrate with Au-In alloy nanoparticles from experiment I was then cleaved outside the growth tube into two pieces for experiments II and III. In experiment II, the sample was subjected to an AsH<sub>3</sub> flow of 74 μmol/min for 6 min at 350 °C. The spherical Au-In nanoparticles crystallize and form InAs islands as shown in the SEM micrograph in Figure 2.1 (c) and confirmed by Energy Dispersive X-ray (EDX) analysis (Figure 2.2); but with no NW growth. Because AsH<sub>3</sub> is only 50 % pyrolyzed even at 600 °C on SiO<sub>2</sub> surfaces in H<sub>2</sub> ambient and in the absence of TMIn and Au nanoparticles,<sup>16</sup> the partly pyrolyzed AsH<sub>3</sub> and the already deposited In were insufficient to create the concentration gradient required to initiate InAs NW growth.<sup>17</sup> To further investigate this point, we performed experiment III, where the sample was subjected to TMIn and AsH<sub>3</sub> flows of 6 and 74 μmol/min respectively at 350 °C for the same growth time (6 minutes) resulting in significant NW growth on the substrate as shown in Figure 2.1 (d). Similar results to those of experiments II and III were obtained without interrupting the growth run for sample cleavage. From experiments II and III, we conclude that NW growth was only possible when TMIn and AsH<sub>3</sub> are present in the chamber simultaneously even in the presence of Au-In alloy on the SiO<sub>2</sub> substrate; from this, we deduce that the presence of TMIn plays an important role in AsH<sub>3</sub> pyrolysis and thus NW growth. When both TMIn and AsH<sub>3</sub> are present in the reaction chamber, the pyrolysis temperatures are expected to be reduced significantly with heterogeneous reactions dominating the precursor pyrolysis at low temperatures.<sup>18</sup> Studies on AsH<sub>3</sub> pyrolysis in the presence of TMGa have shown that the AsH<sub>3</sub> pyrolysis temperatures are reduced by ~ 200 °C.<sup>19</sup>

As a comparison study, a second set of experiments was carried out on SiO<sub>2</sub> substrates without Au nanoparticles on top. In experiment IV, a bare SiO<sub>2</sub> substrate is



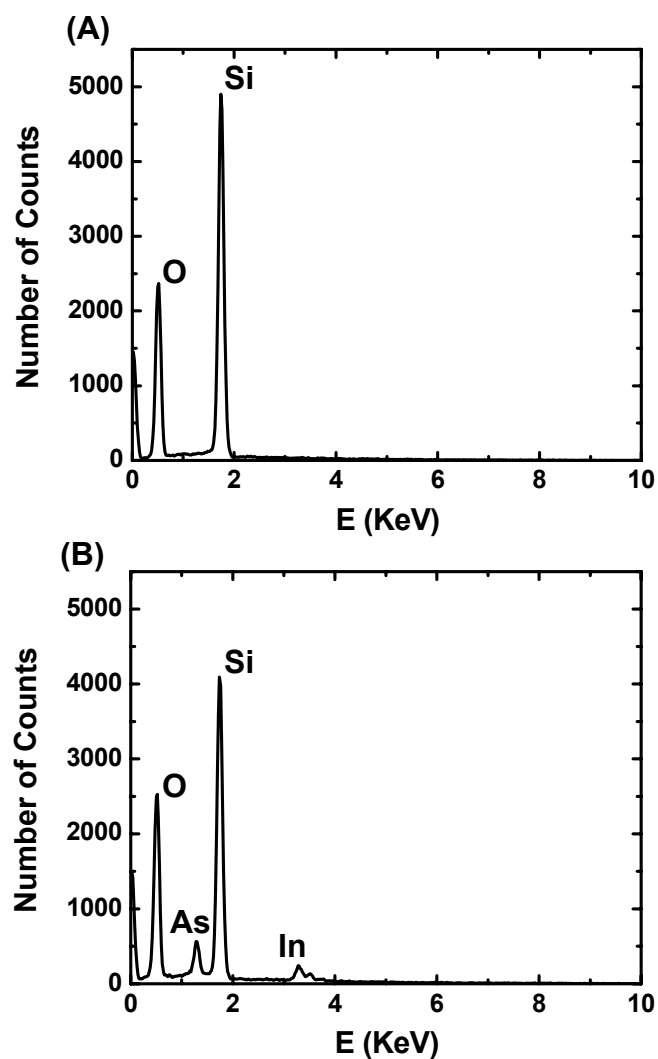


Figure 2.2. (A) EDX spectrum obtained near a bright dot of Figure 1(C) of experiment II showing only Si and O peaks. (B) EDX spectrum obtained from a bright dot of Figure 1(C) of experiment II showing In and As peaks in addition to the Si and O peaks.

exposed to 6  $\mu\text{mol}/\text{min}$  of TMIIn at 350  $^{\circ}\text{C}$  for 6 min resulting in sufficient TMIIn pyrolysis for formation of In droplets, as shown in Figure 2.1 (e). This sample was then used in experiment V for comparison to experiment III, where the substrate was subjected to identical growth conditions, i.e. flow of 6 and 74  $\mu\text{mol}/\text{min}$  of TMIIn and  $\text{AsH}_3$ , respectively, at 350  $^{\circ}\text{C}$  for 6 min. No NW growth was observed from experiment V, as

shown in Figure 2.1 (f), indicating that the presence of the Au nanoparticles on the substrate is essential for efficient  $\text{AsH}_3$  pyrolysis at 350 °C. However, in experiment VI with the same growth time and flow rates as in experiment V but a substrate temperature of 500 °C, NW growth was observed on the bare  $\text{SiO}_2$  substrate due to improved  $\text{AsH}_3$  pyrolysis at 500 °C as shown in Figure 2.1 (g). Furthermore, the pre-deposition step of In droplets at 350 °C is not necessary because the TMIIn pyrolysis is efficient at 500 °C. Indeed, experiment VII demonstrates NW growth on the bare  $\text{SiO}_2$  surface at 500 °C, as shown in Figure 2.1 (h). Finally, no NW growth at 350 °C was observed on the bare  $\text{SiO}_2/\text{Si}$  substrate from experiment VIII with identical TMIIn and  $\text{AsH}_3$  flows as in experiments I-VII, as shown in Figure 2.1 (i). Thus, we conclude that  $\text{AsH}_3$  pyrolysis is a limiting factor in the InAs NW growth and our results suggest that Au nanoparticles help in the  $\text{AsH}_3$  pyrolysis process.

To further assess the role of the Au nanoparticles, we loaded a bare  $\text{SiO}_2/\text{Si}$  sample with no Au nanoparticles on top downstream from another  $\text{SiO}_2$  substrate onto which Au nanoparticles had been dispersed, as shown schematically in Figure 2.3 (a). NW growth at 350 °C was observed not only on the  $\text{SiO}_2$  substrate with Au nanoparticles on top, as shown in Figure 2.3 (b), but also on the bare  $\text{SiO}_2$  substrate that was not dispersed with Au catalysts, as shown in Figure 2.3 (c); the growth on the bare  $\text{SiO}_2$  substrate is different from the growth of experiment VIII shown in Figure 2.1 (i), where only InAs islands form on a bare  $\text{SiO}_2$  substrate under the same growth conditions. The NWs grown on the  $\text{SiO}_2$  substrate with Au nanoparticles are long, bent, and tapered.

There is a very large diameter variation and the diameter does not appear to be defined by the initial Au nanoparticle size as normally seen in Au nanoparticle-mediated

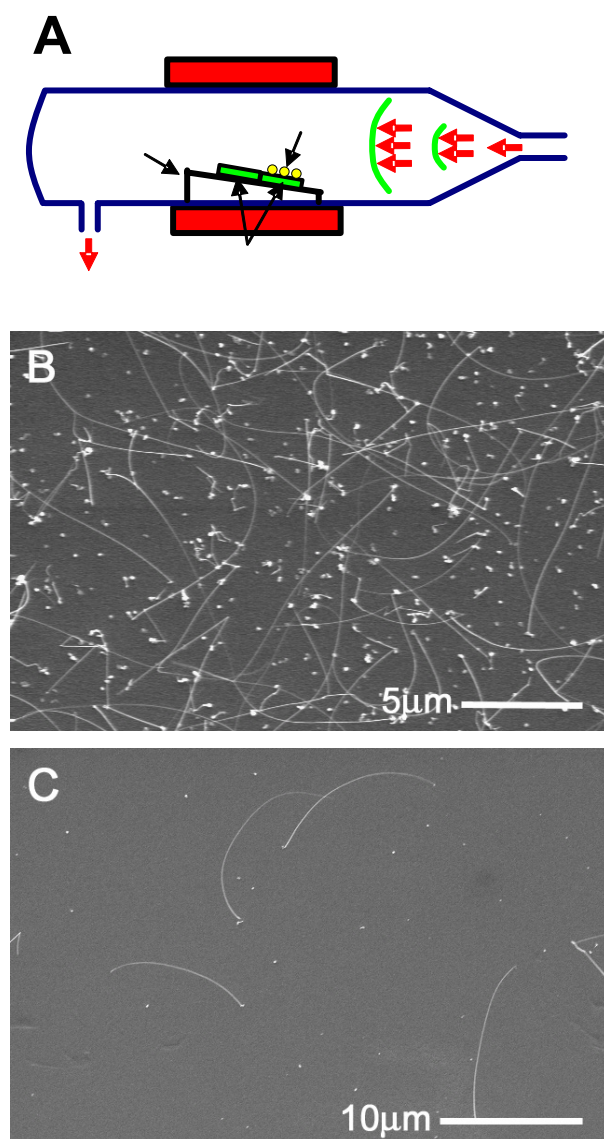


Figure 2.3. (A) Schematic diagram showing the growth setup for the remote effect of the Au nanoparticles in the  $\text{AsH}_3$  pyrolysis on  $\text{SiO}_2$  substrate, (B) SEM image of NWs grown on the upstream  $\text{SiO}_2$  sample with Au nanoparticles on top, (C) SEM image of NWs grown on the downstream  $\text{SiO}_2$  sample with no Au nanoparticles on top.

VLS NW growth. There are InAs islands (solidified from Au-In alloy particles) that are much larger in size (50 – 300 nm) after NW growth, some of which grow multiple NWs.

Typically, no “catalyst” was found at the tip of the NWs under SEM. The InAs NWs grown on the bare SiO<sub>2</sub> substrate have very similar morphologies but the InAs islands on the substrate are smaller. NW growth on the bare SiO<sub>2</sub> substrate was also reproduced at a 0.4 mm separation from the SiO<sub>2</sub> substrate with Au nanoparticles on top. Similar experiments were also carried out on patterned substrates, with growth conducted under identical conditions on SiO<sub>2</sub> substrates with a 10 nm Au thin film deposited at the center of the substrate using a shadow mask. No InAs NW growth was observed upstream from the Au film, but there is NW growth downstream from the Au film area at a separation distance of  $\geq 1.5$  mm. There is no NW growth for distances  $< 1.5$  mm, presumably due to the depletion of In necessary for the NW growth sites at the peripheries of the Au film. Moreover, there is no NW growth gradient observed downstream from the Au film. These experiments exclude the possibility in our studies of transport of the metal catalyst via droplet breakup during the growth, as reported recently for Si NW growth.<sup>20</sup> Moreover, InAs NW growth was observed only at the peripheries of the Au film and not at its center due to the higher local V/III ratio at the center of the sample that inhibits NW growth, which we will discuss later in 2.6.

These experiments demonstrate that at temperatures around 350 °C, the Au nanoparticles play an important role in catalyzing the AsH<sub>3</sub> pyrolysis. Specifically, the observations that Au-In forms much larger particle sizes from which multiple NWs grow from single island, and the NW growth on bare SiO<sub>2</sub> substrate without Au nanoparticles indicate that the presence of Au nanoparticles is important for reactant pyrolysis at moderate growth temperatures but the nanoparticles do not necessarily directly nucleate NW growth. This catalytic effect has also been observed in other III-V NW growth; for

example, study of the growth of GaP NWs has shown that the dissociation reaction of  $\text{PH}_x$  on the catalytic Au surface is the rate limiting step for the growth of GaP NWs.<sup>21</sup> The possible origin for the one dimensional NW growth we observe at this temperature is a liquid group III (In) droplet (or In rich Au-In alloy) that serves as a catalyst for VLS NW growth. Indeed, it had been suggested by Wagner that the metal “impurity” in VLS growth could be an excess of one of the material constituents for growth of compound semiconductor NWs.<sup>5</sup> An atomic probe microscopy experiment could help to analyze the incorporation of Au elements in InAs NWs and further illustrate involvement of Au in the InAs NW growth.<sup>22</sup> The post-growth absence of an alloy droplet on the NW tips for longer growth runs and within the resolution limits of the SEM imaging, can be attributed to In consumption during temperature cooling down in  $\text{AsH}_3$  flow after NW growth. Although very unlikely, In evaporation during growth, as seen in Ga evaporation from Ga droplets in the GaAs whisker growths, cannot be ruled out.<sup>23</sup>

To further investigate the nucleation and evolution of InAs NWs during growth, we monitored the morphological changes of the Au nanoparticles by SEM imaging for different growth times but otherwise identical growth conditions (with input V/III ratio of 25 and growth temperature of 350 °C). Figure 2.4 shows FE-SEM images of the InAs NW growth evolution as a function of time. After short growth intervals (30 – 90 s), the apparent Au colloid diameter increased from 40 nm to ~ 55 nm due to InAs deposition on the Au colloid but spherical shape is maintained. For longer growth runs up to 3 min, InAs islands with irregular shapes were observed to form on the substrate with density comparable to that of the deposited Au nanoparticles, suggesting that one island form around each Au nanoparticle, but there is no NW formation. NWs were observed to

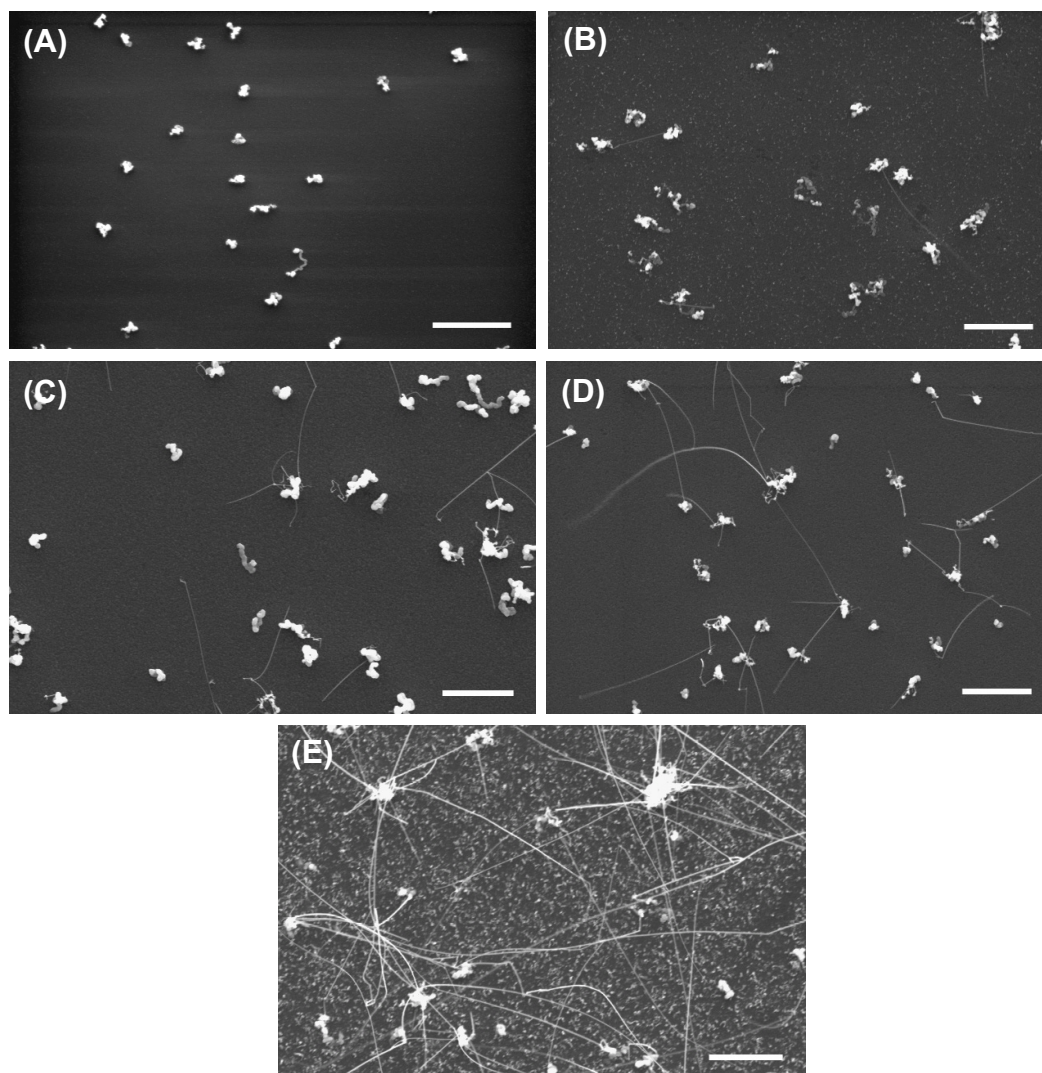


Figure 2.4. FE-SEM images of InAs island and nanowire growth at 350°C and V/III=25 for (A) 2min, (B) 3min, (C) 4min, (D) 6min, and (E) 10min. Scale bars are 2 $\mu$ m.

nucleate and grow for growth times longer than 3 min. For long growth runs, multiple NWs were observed to grow from single InAs islands. Figure 2.5 (a) – (d) shows histograms of NW diameter distribution for different growth times. It is evident that the NWs start to grow with very thin diameters, mostly smaller than that of the 40 nm Au nanoparticles. A very large variation in NW diameter is observed with the average NW

diameter and dispersity increasing with growth time: The NWs have diameters ranging from 12 – 26 nm, 18 – 47 nm, and 20 – 57 nm for growth times of 3, 4, and 10 min, respectively. NW length increases with growth time as well, ranging from 0.3  $\mu\text{m}$  to 17  $\mu\text{m}$  for growth times from 3 min to 10 min. The increases in NWs diameter and length indicate VLS growth in the axial direction and VS growth in the radial direction. These results suggest a growth mechanism different from the Au mediated VLS or VSS growth, and provide further evidence that Au nanoparticles are not necessarily initiating NW growth, and that NW growth is nucleated by In droplets in our study.

Due to the NW diameter variation for different growth times, growth rate is calculated in terms of the average NW volume instead of length. Furthermore, because there is more than one NW per single InAs island, we can further normalize the growth rate with respect to the number of islands and calculate the NW growth as function of time using

$$\rho = \frac{\sum_{i=1}^N \frac{\pi}{4} d_i^2 L_i}{N} \frac{M}{t}, \quad (1)$$

where  $\rho$  is the NW growth rate,  $d$  and  $L$  are the NW diameter and length respectively,  $N=50$  is the number of characterized NWs,  $M$  is the number of NWs per single InAs island, and  $t$  is the growth time. The resulting growth rate is plotted in Figure 2.5 (f). The island volume change is negligible compared to the NW volume change with time, and thus was not included in calculating the growth rate. Note that the NW length increases steadily with increasing growth time, with no restriction imposed by the diffusion length of any of the reactants on the  $\text{SiO}_2$  substrate or the InAs NW. This is highly plausible due to the high mobility of In on the  $\text{SiO}_2$ , as observed for NW growth using SA-OMVPE.<sup>9</sup>

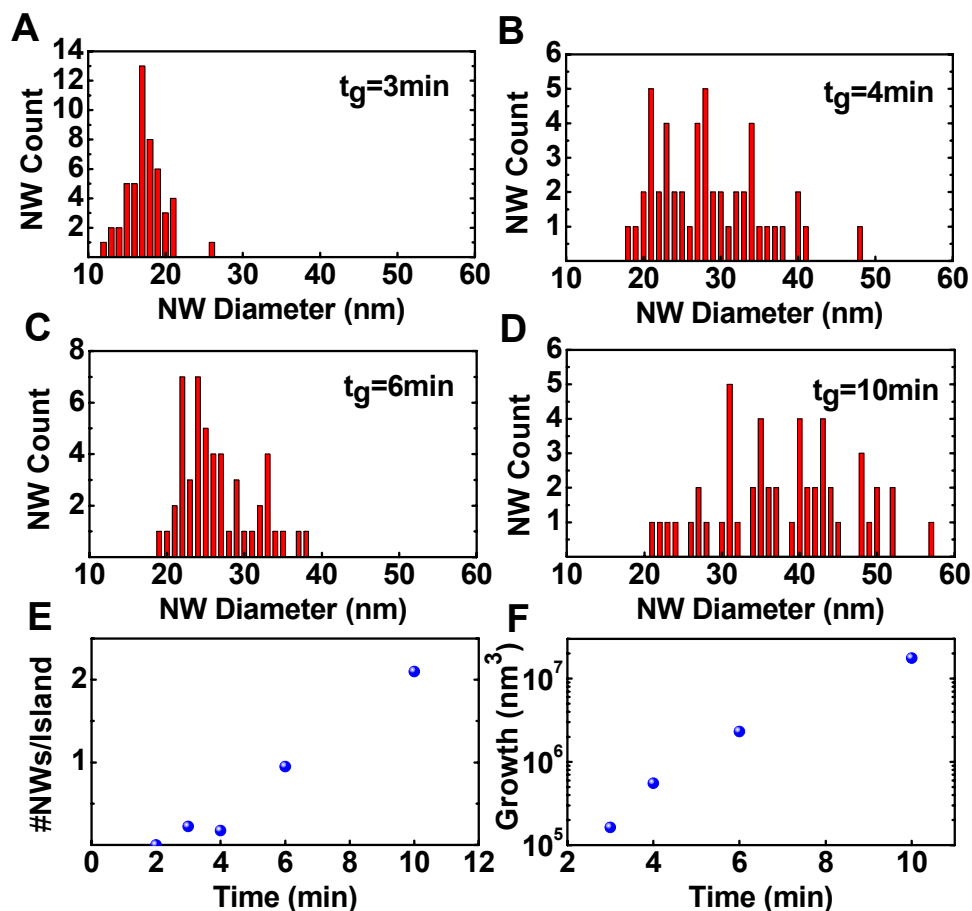


Figure 2.5. (A)-(D) Histograms of NW diameter variation for different growth times. (E) Number of InAs NWs per single island for different growth times, (F) Total NW growth as function of growth time.

## 2.5 Temperature Effects

To assess the influence of substrate temperature, InAs NW growth was studied at temperatures ranging from 310 to 390 °C for 6 minutes with fixed TMI and AsH<sub>3</sub> flows. At 310 °C, there is no NW growth due to inefficient pyrolysis of the input precursors. NWs start to grow at temperatures higher than 330 °C and the growth rate (volume/time) increases exponentially with substrate temperature as shown in Figure 2.6, indicating



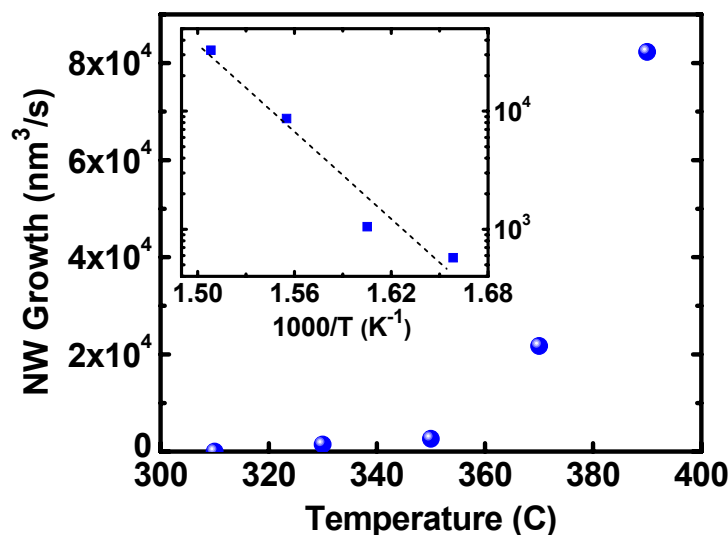


Figure 2.6. NW growth rate as function of growth temperature on the SiO<sub>2</sub> surface. Inset is Arrhenius plot of the NW growth rate.

kinetically limited NW growth with activation energy of ~56 Kcal/mol. The NWs are tapered, but SEM imaging indicates the tapering is minimal for NW growth at temperatures up to 350 °C (approximately 1.37 nm/μm measured from tip to root). The tapering becomes more severe at higher temperatures, due to the enhanced sidewall coating because of the excess material supplied and increased VS growth.

The InAs NWs grown on SiO<sub>2</sub> substrates suffer severe morphological changes at higher temperatures even under AsH<sub>3</sub> flow. Significant morphological change of NWs grown at 350 °C and a sharp decrease in the NW density were observed when the substrate was heated up to 450 °C in 444 μmol/min AsH<sub>3</sub> flow. Figure 2.7 shows FE-SEM images of InAs NWs grown at 350 °C (Figure 2.7 (a)) and heated InAs NWs at 450 °C (Figure 2.7 (b)). This indicates severe As out-gassing and decomposition of the InAs NWs at 450 °C due to insufficient AsH<sub>3</sub> pyrolysis. At 500 °C, but with both TMIn and

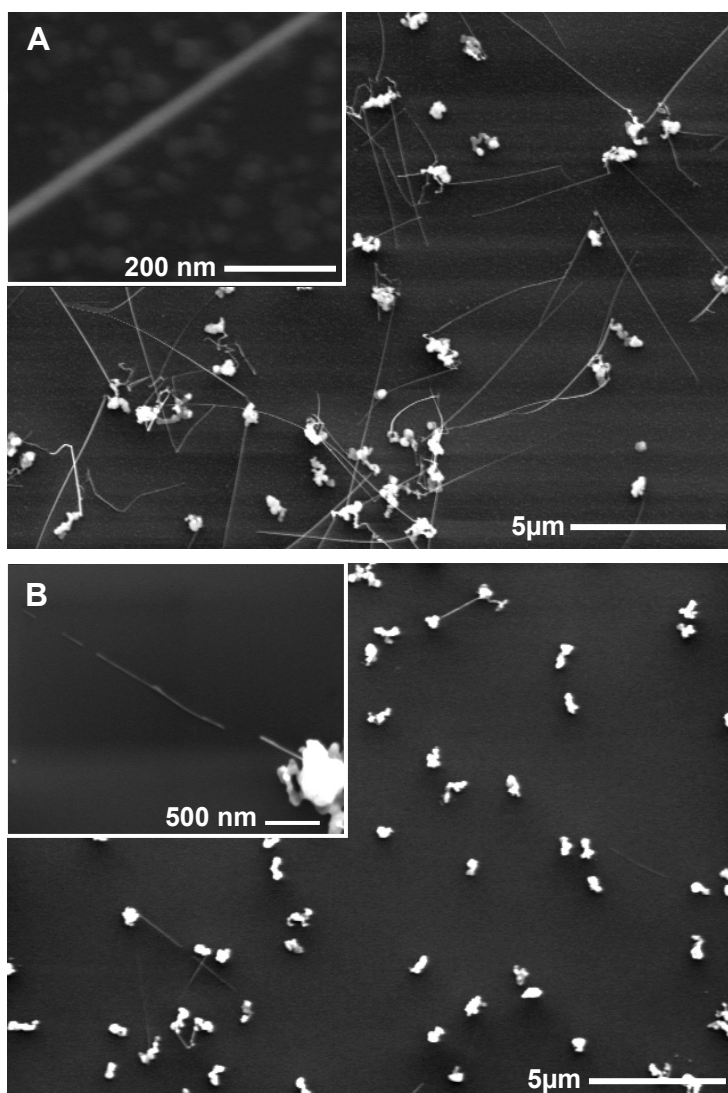


Figure 2.7. (A) SEM image of InAs NWs grown on SiO<sub>2</sub> at 350 °C with Au nanoparticles on substrate, inset is a high magnification SEM image of a single InAs nanowire, (B) same sample in (A) after being heated to 450 °C in 444 μmol/min AsH<sub>3</sub> flow. The density of the nanowires have decreased; inset in (B) shows a high magnification SEM image of an InAs nanowire at the stage of decomposition.

AsH<sub>3</sub> flows into the reactor, only morphological imperfections with no drop in the NW density were observed, which can be attributed to the enhanced As pyrolysis due to the simultaneous presence of TMI<sub>n</sub> and AsH<sub>3</sub>. These experiments confirm the importance of

maintaining  $\text{AsH}_3$  flow during cool down after NW synthesis, similar to the growth of 2D epilayers.

## 2.6 Input V/III Ratio Effects

The input V/III ratio emerges in our studies as an important limiting factor for compound semiconductor NW growth. This particular study on  $\text{SiO}_2$  surfaces is instructive due to its chemical inertness to the grown materials (InAs NWs) at the given growth temperatures. Thus, a set of growth experiments were conducted at 350 °C for 6 min at different input V/III ratios; a growth temperature of 350 °C was chosen because minimal tapering was observed in our earlier studies at this temperature. By varying the  $\text{AsH}_3$  flow rate over a range of 44 – 134  $\mu\text{mol}/\text{min}$  and maintaining a constant TMIn flow rate at  $\sim 1.5 \mu\text{mol}/\text{min}$ , the input V/III ratio was varied between 30 and 90. The InAs NW diameters, lengths, and density decrease as the input V/III ratio increases, as shown in the FE-SEM images of Figure 2.8 (a) – (c). At constant TMIn flow, growth pressure, and temperature on a  $\text{SiO}_2/\text{Si}$  substrate, the input V/III ratio determines the growth rate and the partial pressures at the growth interface (and consequently, the interface V/III ratio) determine the solid stoichiometry.<sup>18</sup> The activation energies for heterogeneous reactions tend to decrease with increasing V/III ratio in thin film deposition,<sup>24</sup> and as a result the thin film growth rate increases with increasing V/III ratio. On the other hand, InAs crystallization may consume the available In required for NW nucleation and hinder its supply to the seed particle,<sup>25</sup> leading to a decrease in the NW growth rate with increasing V/III ratio. We also observed in these experiments that InAs island deposition on the

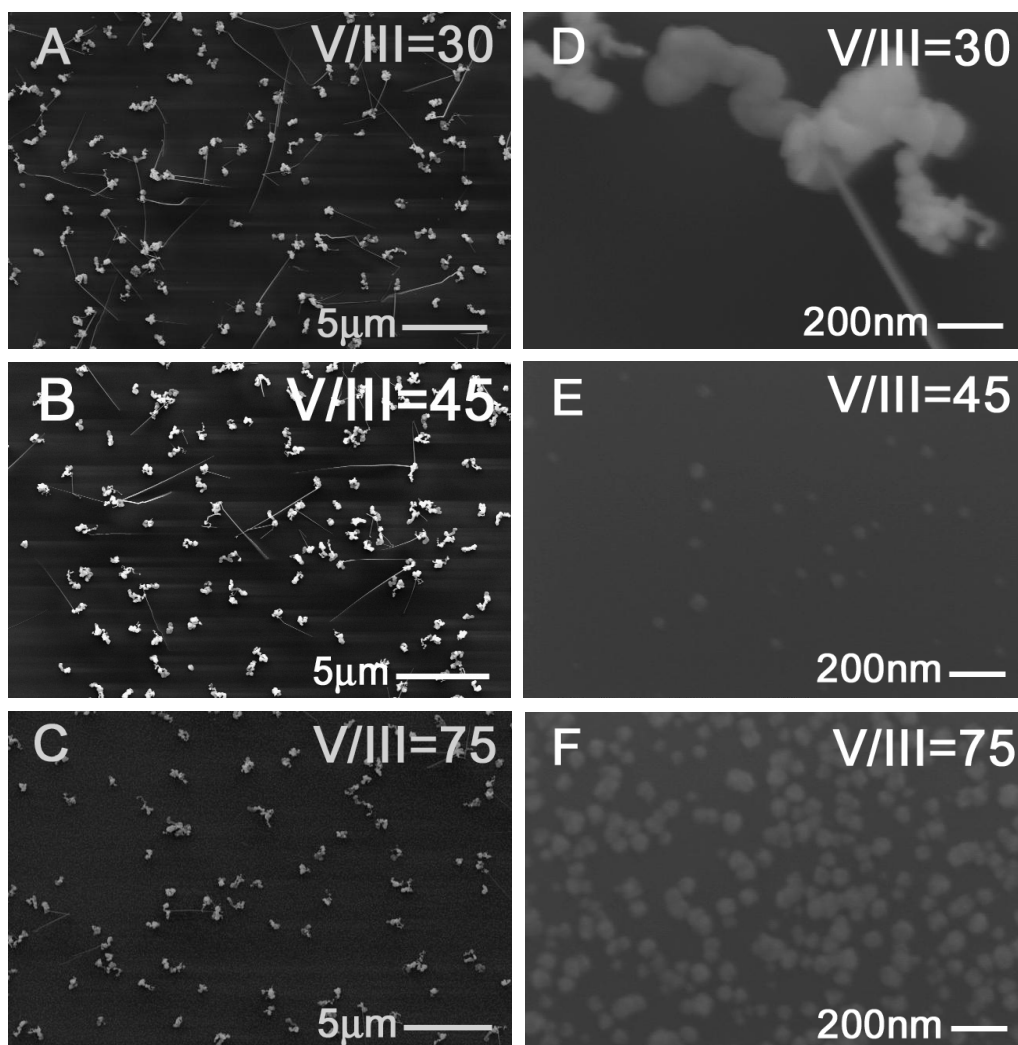


Figure 2.8. FE-SEM images of (A) – (C) InAs NW growth on a  $\text{SiO}_2/\text{Si}$  substrate at different input V/III ratios and (D) – (F) surface growth corresponding to those growths of (A) – (C).

$\text{SiO}_2$  surface increases as the input V/III ratio increases (Figure 2.8 (d) – (f)). This also explains our observation of InAs NW growth only at the peripheries of the Au film but not at its center: There exists a very high local V/III ratio at the center of the Au film due to enhanced  $\text{AsH}_3$  pyrolysis leading to suppression of NW growth in this area. Figure 2.9 (a) shows a plot of the NW growth rate as function of time for different input V/III ratios

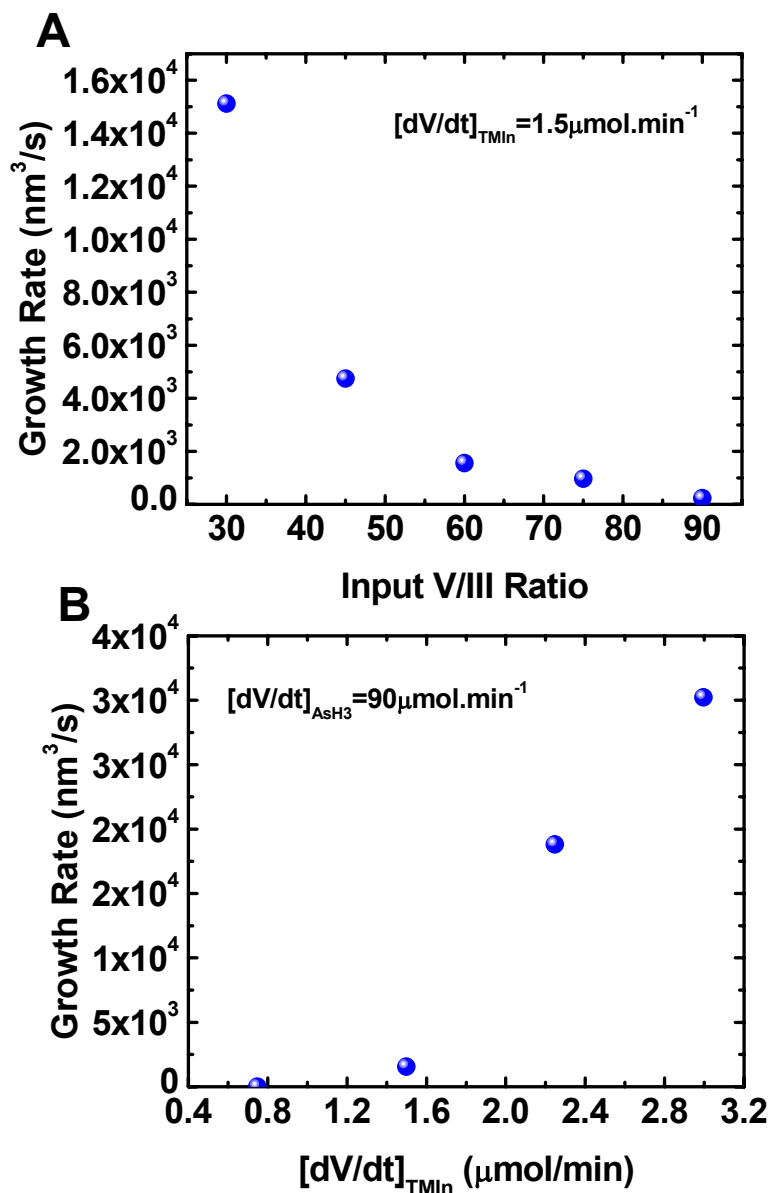


Figure 2.9. (A) NW growth rate as function of the input V/III ratio with constant TMI flow rate. (B) NW growth rate as function of TMI flow rate with constant AsH<sub>3</sub> flow rate.

showing reduced NW growth rates as the input V/III ratio increases. We have also performed InAs NW growth at different V/III ratios with fixed AsH<sub>3</sub> flow ( $\sim 90 \mu\text{mol}/\text{min}$ ) and varying TMI flow rate ( $\sim 0.75 - 3 \mu\text{mol}/\text{min}$ ). Figure 2.9 (b) shows a

plot of the NW growth rate as function of the TMIn flow rate, revealing that the growth rate increases with increasing TMIn flow. This trend is similar to thin film epitaxy whose growth rate is known to be determined by the group III flow rate. For the InAs NW growth rate in Figure 2.9 (b), the V/III ratio decreases with increasing TMIn flow leading to an enhancement in the NW growth rate.

## 2.7 Crystal Structure

Although InAs NWs are known to often crystallize in the wurtzite (WZ) crystal structure,<sup>26,27,28,29</sup> as we shall discuss in next chapter, InAs NWs grown on SiO<sub>2</sub> surfaces at 350 °C crystallize in the cubic zinc blende (ZB) crystal structure similar to bulk InAs. In general, growth temperatures of 350 °C or less have resulted in ZB crystal structure.<sup>27,30,31</sup> Figure 2.10 (a) shows a transmission electron microscope (TEM) image of an InAs NWs grown on SiO<sub>2</sub> surfaces. Figure 2.10 (b) shows selective area diffraction pattern of the InAs NW shown in Figure 2.10 (a) indicating ZB crystal structure and  $\langle 110 \rangle$  growth orientation. In general, NWs with diameters  $\geq 40$  nm have a twin boundary along their growth-direction axis highlighted by the white line in Figure 2.10 (a). Figures 2.10 (c) and (d) show high resolution TEM (HR-TEM) images of the ZB InAs NW taken at two different sections at the twin boundary, highlighted by the white dashed line. Fast Fourier patterns of the TEM data taken at the top (Figure 2.10 (c)) or bottom (Figure 2.10 (d)) confirm a common  $\langle 110 \rangle$  growth direction.

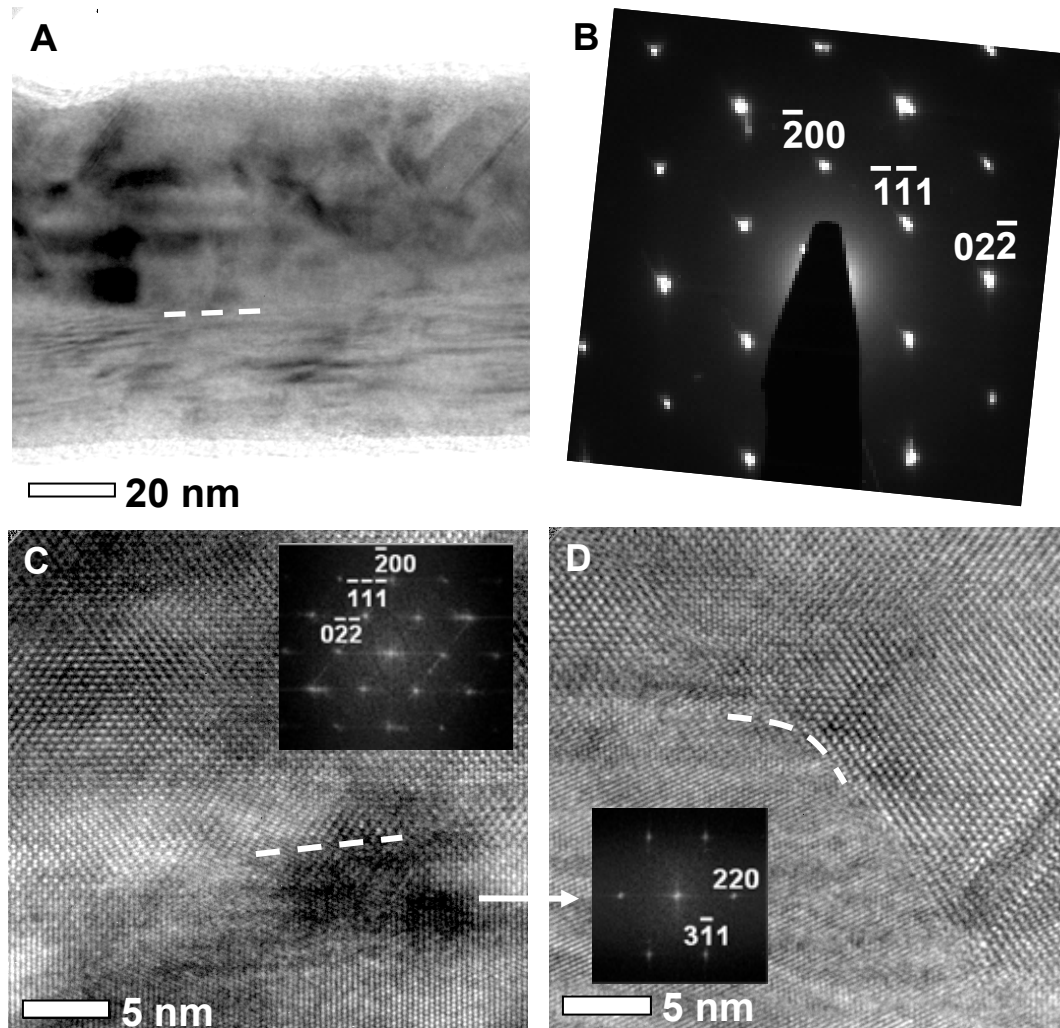


Figure 2.10. TEM characterization of InAs NWs grown on  $\text{SiO}_2$  substrates: (A) Bright field TEM image and (B) the corresponding diffraction pattern of the same NW showing a  $\langle 220 \rangle$  growth orientation. (C) and (D) lattice fringes of the same ZB InAs NW with inset FFT patterns of the top and bottom portions showing  $[011]$  and  $[\bar{1}14]$  pole orientations, respectively. The dashed line in (B) – (D) highlights the interface between the twinned NW segments.

## 2.8 Conclusions

In this chapter, we presented studies on the nucleation and growth evolution of InAs NWs on SiO<sub>2</sub>/Si substrates. By varying key growth parameters such as presence or absence of Au nanoparticles, sequential input and flow rates of TMI<sub>n</sub> and AsH<sub>3</sub> precursors, growth time, substrate temperature, and input V/III ratio, significant insights into the InAs NW growth have been developed. The Au nanoparticles were found to facilitate efficient pyrolysis of AsH<sub>3</sub> but are not necessary to nucleate InAs NW growth. InAs NWs are most likely nucleated through In seed particles created from excess In supply on the substrate, and grow via the VLS growth mechanism. The input V/III ratio was shown to play a critical role in NW growth. High V/III ratios causes switch over from VLS NW growth to thin film growth on SiO<sub>2</sub> substrates. TEM analysis on these NWs have shown that they exhibit the zinc blende crystal structure with <110> growth orientation. These findings are very useful for understanding and rational synthesis of InAs and other III-V compound semiconductor NWs.

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### 3. INDIUM ARSENIDE NANOWIRE GROWTH ON INDIUM ARSENIDE (111)B SUBSTRATES

#### 3.1 Introduction

Growth of InAs whiskers dates back to 1959 when Antell and Effer observed during the vapor growth of InAs, InP, GaAs, and GaP crystals the formation of InAs whiskers (from  $\text{InI}_3$  and solid arsenic at a growth temperature of 840 °C).<sup>1</sup> Antell and Effer state that “The whiskers always seemed to grow from what appeared to have been a molten globule.” Takahashi and Muriizumi have synthesized InAs whiskers on Au- and Ag-coated glass substrates using a chemical vapor deposition (CVD) technique; the details of the growth mechanism were not discussed in their report.<sup>2</sup> Koguchi et al.<sup>3</sup> (1992) and Yazawa et al.<sup>4</sup> (1993) have synthesized InAs and GaAs whiskers on their respective substrates using OMVPE and attributed their growth to the vapor-liquid-solid (VLS) mechanism put together by Wagner and Ellis in 1964 for Si whisker growth.<sup>5</sup> The VLS growth mechanism discussed in chapter 1 remained the general accepted model for III-V NW growth until Persson et al. did *in-situ* TEM annealing studies of GaAs NWs with Au nanoparticles at their tips at temperatures higher than those used during growth in a chemical beam epitaxy (CBE) reactor.<sup>6</sup> They suggested that the Au-Ga droplet remained in solid-phase during the GaAs NW growth, and consequently attributed the growth to a vapor-solid-solid (VSS) growth mechanism analogous to VLS. Harmand et al. followed up on this study in 2005 by growing InAs NWs using MBE with different growth terminations, i.e. stopping the GaAs NW growth by ceasing either group III flow,

or both groups III and group V.<sup>7</sup> They concluded that the final composition of the metal particles depends on the growth history, and from scanning transmission electron microscope (STEM) analysis of the Au-Ga atomic constituents, they asserted that the Au-Ga particle was in liquid phase during NW growth, thus validating the VLS growth mechanism for III-V NWs. Based on Persson's experiment, Dick et al. suggested that growth cessation of InAs NWs using OMVPE, at growth temperatures thought to be Au-In melting temperatures, occurs when the Au-In becomes liquid, and that the only possible condition for InAs NWs to grow is when the Au-In nanoparticle is in solid phase.<sup>8</sup> These studies were supported by *ex-situ* STEM analysis of the Au-In nanoparticle constituents that also suggested their solid phase character. These cessation observations and suggestions of growth from solid nanoparticles were extended to GaP, GaAs, and InP NWs.<sup>9</sup> Park et al. have shown using STEM analysis on InAs NWs grown in CVD and cooled down rapidly to room temperature in a water bath immediately after growth that the Au-In nanoparticle remains in liquid phase during the InAs NW growth.<sup>10</sup> They verified the VLS nature of the InAs NW growth with nanoparticle sizes down to 25 nm.<sup>11</sup> Although growth from a solid particle, i.e. the VSS mechanism, was first proposed in 1979 for Ag-catalyzed Si whiskers<sup>12</sup> and more recently for Ti-catalyzed<sup>13</sup> and Al-catalyzed<sup>14</sup> Si NWs that were grown at temperatures much lower than the eutectic melting temperatures of Ag-Si, Ti-Si or Al-Si alloys and have been recently further confirmed by *in-situ* TEM observation of Ge NW growth from solid seeds (at 10 – 100 times slower growth rates than VLS),<sup>15</sup> the studies of Harmand<sup>7</sup> and Park<sup>10,11</sup> have confirmed through STEM the liquid nature of the growth seed for III-V NWs. The key

factors that led to InAs NW growth cessation observed by Dick et al.<sup>8,9</sup> will be discussed in this chapter.

On the other hand, NW nucleation in the absence of Au or metal nanoparticles has been demonstrated. Mandl et al. have reported the epitaxial growth of Au-free InAs NWs on InP (111)B, InAs (001) and Si (001) substrates.<sup>16</sup> The NW growth was attributed to nucleation from cluster related sites that lead to anisotropic growth. This proposition was supported by patterned growth of InAs NWs on InP (111)B from SiO<sub>x</sub> islands, which was suggested to occur in a manner similar to the oxide-assisted growth (OAG) established for Si NWs,<sup>17</sup> and is in contrast to selective area growth of InAs NWs and the like in SiO<sub>2</sub> masks on III-V substrates.<sup>18</sup> Park et al. have performed similar growth experiments on InAs (111)B substrates coated with SiO<sub>x</sub> in different O<sub>2</sub> ambient and suggested that the InAs NW growth occurs from nano-meter sized highly reactive Si clusters in a mechanism different from the VLS, VSS, or OAG.<sup>19</sup> Novotny and Yu have clearly demonstrated the OMVPE growth of In-catalyzed InP NWs on InP (111)B substrates in the absence of any “foreign” metal particle,<sup>20</sup> similar to the growth of GaAs whiskers from excess Ga droplets<sup>21</sup> and was suggested by Wagner and Ellis in their VLS paper in 1964.<sup>5</sup> The growth of InAs NWs from excess In in the presence or absence of Au nanoparticles on InAs (111)B substrates will be treated in this chapter.

The growth of III-V NWs using OMVPE is considered to be diffusion-limited, i.e. the growth rate increases for thinner diameter NWs<sup>22</sup> due to solid-phase diffusion over the substrate surface and NW sidewalls. During their investigation of the competitive or synergetic growth of GaP NWs, Borgstöm *et al.* have observed  $r$  dependent NW growth rates and proposed gas-phase diffusion of Ga species,<sup>23</sup> where  $r$  is the NW radius. In

addition, the Gibbs-Thomson effect (reduction of supersaturation for smaller  $r$  and therefore a drop in the NW growth rate) has been observed for GaAs NWs with small NP diameters and low V/III ratios.<sup>24</sup> Several models that take into account diffusion and Gibbs-Thomson effects have thus emerged.<sup>25,26,27</sup> In this chapter, we will show that solid phase diffusion of group In species through substrate-NW interaction lead to non-linear elongation of the InAs NWs with time and that the Gibbs-Thomson effect is not effective for InAs NWs.

### 3.2 Summary of Results

This chapter is divided into three major sections. In section 3.4, we discuss the nucleation and growth of InAs NWs from In droplets on an InAs (111)B substrate with and without Au nanoparticles. In the presence of Au nanoparticles on the substrate surface, we show that the nucleation density increases as excess In is (i) supplied from the tri-methyl-indium precursor source, or (ii) available on the substrate surface due to substrate decomposition. In the absence of Au nanoparticles on the substrate surface, we demonstrate large area epitaxial growth of InAs NWs is observed when the growth conditions are adjusted to maintain excess liquid In that forms globules leading to VLS growth of InAs NWs. We show that Au nanoparticles facilitate the decomposition of the InAs (111)B substrate and further confirmed this catalytic effect by NW growth in a closed chemical vapor deposition tube mediated by Au nanoparticles without the use of external sources other than the growth substrate itself. The results discussed in part 1 aid in the understanding of III-V nanowire nucleation and growth from excess group III via

the VLS growth mechanism and elucidate the importance of substrate decomposition and the consequent material incorporation into the grown NWs.

In section 3.5, we show that temperature dependent growths observed within certain temperature windows are highly dependent on input V/III ratios. We find that this dependence is a direct consequence of the drop in NW nucleation and growth rate with increasing V/III ratio at a constant growth temperature due to depletion of Indium at the NW growth sites. The growth rate is found to be determined by the local V/III ratio, which is dependent on the input precursor flow rates, growth temperature, and substrate decomposition. These studies advance understanding of the key processes involved in III-V NW growth, support the general validity of the VLS growth mechanism for III-V NWs, and improve rational control over their growth morphology.

In section 3.6, we present new fundamental insights into the NW nucleation and evolution of InAs NWs from time-dependent growth studies performed at two input trimethyl-indium (TMIn) flow rates and the first experimental distinction between two growth regimes defined by the substrate-NW adatom exchange. At low group-III flow, no substrate-to-NW diffusion occurs – in contrast to what is commonly believed – and the NW growth proceeds at an exponential rate for NW lengths ( $L_{NW}$ ) less than the group-III diffusion length on the NW surface ( $\lambda_{NW}$ ) followed by an asymptotic-linear growth rate when  $L_{NW} > \lambda_{NW}$ . Both the Au-In alloy at the NW tip and the growth substrate act as material sinks in this case. On the other hand, large group-III flow allows longer surface diffusion lengths on the substrate and substrate-to-NW diffusion prevails allowing earlier NW nucleation and an increased growth rate that proceeds sub-linear for  $L_{NW} > \lambda_{NW}$  and asymptotic for  $L_{NW} < \lambda_{NW}$ . By extracting  $\lambda_{NW}$  and controlling the growth regime, axial

and radial heterostructure NW growth is feasible. These results not only improve our understanding of the fundamental aspects of NW growth but also set limit lengths only over which optimum control over NW morphology is possible. We finally discuss through TEM analysis polymorphism and formation of WZ crystal structure in these NWs in section 3.7.

### 3.3 Experimental

The growth experiments reported in this chapter were performed in a horizontal OMVPE growth tube using Trimethylindium and Arsine precursors in 1.2 L/min  $H_2$  carrier gas and at a chamber pressure of 100 Torr. 40 nm diameter Au nanoparticles were dispersed at a density of  $\sim 0.3 \mu\text{m}^{-2}$  on InAs (111)B substrates pre-coated with poly-L-lysine, followed by UV Ozone cleaning at 100 °C for 5 min.  $AsH_3$  flow was maintained in the chamber throughout the entire growth process including temperature ramp up and cool down, while TMIIn was introduced for 6 min after reaching the desired growth temperature. The V/III ratio was changed both by altering the  $AsH_3$  flow rate at a fixed TMIIn flow and vice versa. For patterned and ordered growths, e-beam lithography (Joel 6400 at 35 KeV acceleration voltage with 10 pA current and  $1000 \mu\text{C}/\text{cm}^{-2}$  dose) was employed in a double layer MMA/PMMA with variable dot sizes. 25 nm Au was evaporated after resist development in MIBK/IPA for 30 s followed by IPA rinse for 15 s and lift off afterwards for  $\sim 2 - 3$  hours in acetone at room temperature. During the growth experiment, the Au discs ball up and act as nucleating sites for NW growth. The NW morphology was characterized using an FEI XL 30 Environmental Scanning



Electron Microscope (ESEM) operating at 30 KV acceleration voltage. Dimensions and statistical distributions were determined in each case by measuring the sizes of 15 NWs at the highest achieved magnifications. The structural properties of these NWs were characterized by a 200 KeV FEI Tecnai scanning transmission electron microscope. For the growths in a closed system, Au NPs were dispersed atop an InAs (111)B substrate which was then loaded into a small quartz tube with a  $\sim 1/4$  inch diameter which was pumped down to  $\sim 10$  mTorr. The sealed tube was then inserted to the center of a Lindberg-Blue furnace which was then heated to the desired growth temperature.

### **3.4 Excess Indium and Substrate Effects on the InAs Nanowire growth**

In this section, we examine nucleation and growth of InAs NWs from excess In with and without Au nanoparticles. Au nanoparticles on  $\text{SiO}_2/\text{Si}$  substrates were found to facilitate  $\text{AsH}_3$  pyrolysis but not to be necessary to nucleate NWs as has been demonstrated in chapter 2, while excess In, supplied from either the input group III precursor source or the III-V substrate, was found to nucleate InAs NWs. We show that due to the catalytic effect of Au nanoparticles on substrate decomposition, NW growth in a closed CVD tube is possible without any additional source other than the growth substrate itself.

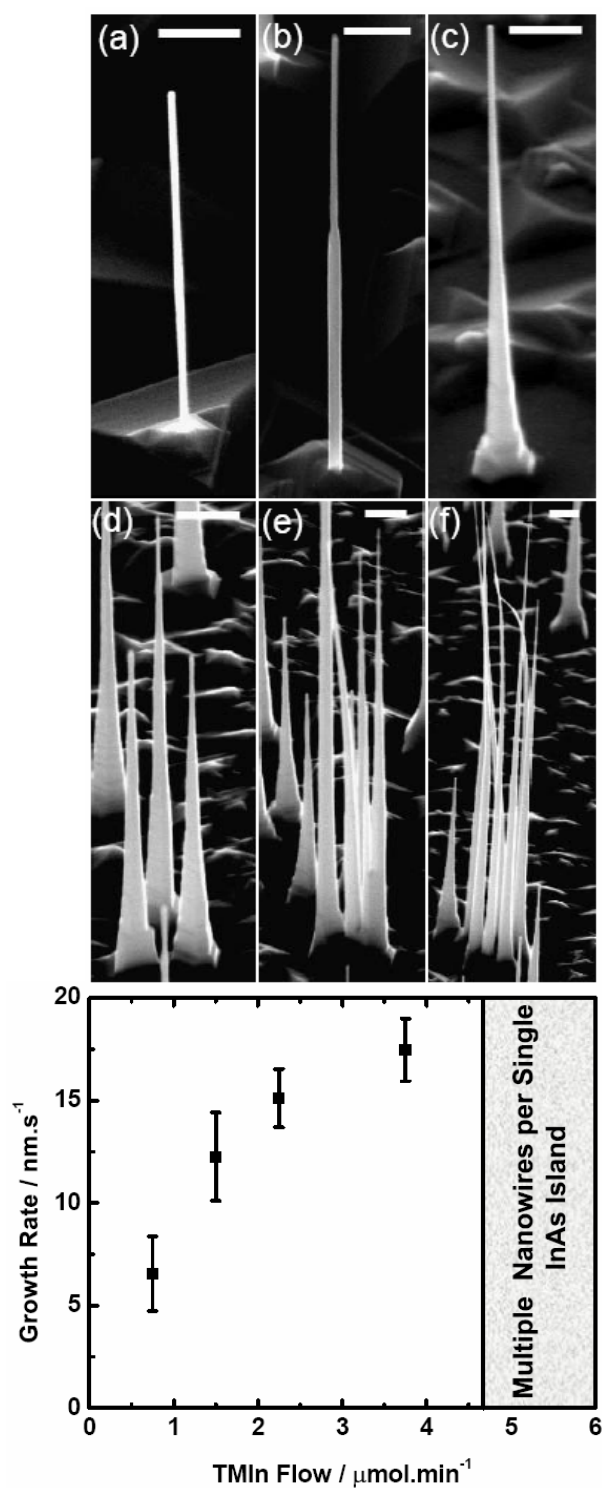


Figure 3.1. 45° FE-SEM images of InAs NWs grown on InAs (111)B at 500 °C with  $\text{AsH}_3$  flow rate of 45  $\mu\text{mol}/\text{min}$  and TMIIn flow rates of (a) 0.75, (b) 1.5, (c) 2.25, (d) 4.7, (e) 6, (f) 7.5  $\mu\text{mol}/\text{min}$ . Scale bars are 500 nm. g) Growth rate of InAs NWs vs. TMIIn flow rates. At TMIIn flow rates  $\geq 4.7$   $\mu\text{mol}/\text{min}$ , multiple InAs NWs grow per single Au nanoparticle.

### 3.4.1 Excess Indium from Input TMIn Precursor

We examine the effects of TMIn flow on the nucleation density and growth rate of InAs NWs grown on InAs (111)B substrates on which 40 nm Au nanoparticles had been dispersed. The growth time, substrate temperature and input AsH<sub>3</sub> flow rate were 6 min, 500 °C, and 45 μmol/min, respectively, while the input TMIn flow rate was varied between 0.75 – 7.5 μmol/min. Figure 3.1 (a) – (f) shows 45° field-emission scanning electron microscope (FE-SEM) images of the grown NWs, and the corresponding growth rate is plotted in Figure 3.5 (g). First, we observe that the lengths of the NWs increase as the TMIn flow rate is increased, although with different morphologies. Second, InAs NWs grow with uniform diameter determined by that of the Au nanoparticle (~ 40 nm) when the TMIn flow rate is low (0.75 μmol/min). With increased TMIn flow rate, the NWs are tapered with the diameter at the base of the NWs being larger than that at their tips. Third, for TMIn flow rates  $\geq 4.7$  μmol/min, multiple InAs NWs grow in the vicinity of a single Au nanoparticle.

We explain these observations as follows. The growth rate follows the universal dependence on group III input precursor flow rate (TMIn), which is normally consumed at the growth interface for a V/III ratio greater than 1.<sup>28</sup> As the TMIn flow rate increases, the axial NW growth rate increases as shown in Figure 3.1 (g) at a rate of 0.34 μm/μmol for TMIn flows of 0.75 – 2.25 μmol/min. Also, the concentration of In adatoms at the surface of the substrate will increase as the TMIn flow rate increases. Due to the In concentration gradient between the substrate surface and NW, diffusion of In adatoms from the substrate surface to the NW becomes prominent at TMIn flow rates greater than 1.5 μmol/min. Excess In available at the base of the InAs NW, where the mobility of In

diffusing on the substrate surface to the NW tip is most impeded, allows radial growth and tapering at their bases. The base diameter thus increases steadily with increasing TMIn flow until the In concentration near the base is sufficiently high to form liquid In droplets and nucleate multiple NWs in the vicinity of the Au-catalyzed InAs NWs. Figure 3.1 (d) – (f) also shows evidence of surface growth due to excess available In on the substrate surface. The growth of multiple InAs NWs from a single nucleation site cannot be explained through the common VLS or VSS mechanism from a Au-In alloy particle, but rather suggests additional nucleation from In droplets made available from the input precursor.

#### 3.4.2 Excess Indium from Substrate Decomposition

The effect of excess In was also observed during NW growth under identical growth conditions both with and without AsH<sub>3</sub> flow during temperature ramp up. AsH<sub>3</sub> is typically introduced in the reactor during temperature ramp-up to counteract As sublimation and maintain the surface stoichiometry of the InAs substrate. Thus, one would expect that As sublimation would lead to the formation of an In rich surface and the excess In responsible for NW growth could be supplied from the substrate itself. We have therefore performed growth experiments on an InAs (111)B substrate with Au nanoparticles 40 nm in diameter on its surface, where the growth temperature was kept constant at 520 °C, and the AsH<sub>3</sub> and TMIn flow rates were fixed at 150 μmol/min and 6 μmol/min, respectively, for a growth time of 6 min. When AsH<sub>3</sub> flow was maintained during temperature ramp up, a single InAs NW is grown per single Au nanoparticle as

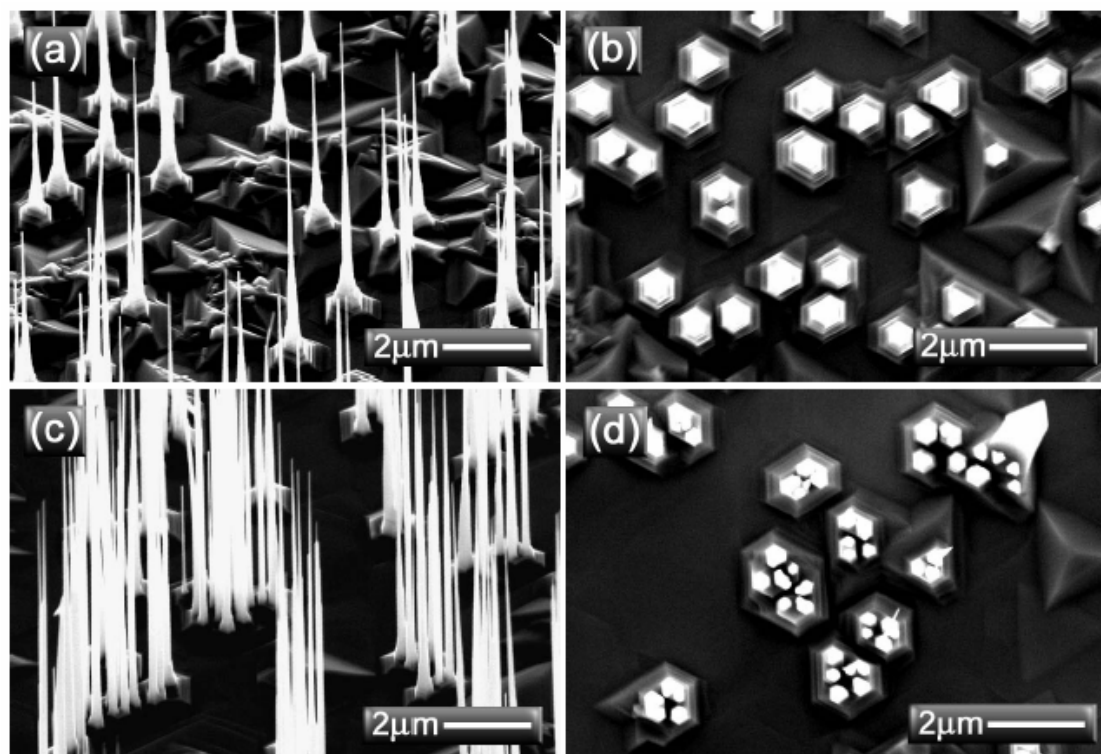


Figure 3.2. Representative FE-SEM images of a) 45° angle view and b) top view of InAs NWs grown on InAs (111)B substrate at 520 °C, while AsH<sub>3</sub> flow was maintained during temperature ramp up. FE-SEM micrographs of c) 45° angle view and d) top view of multiple InAs NWs per single Au nanoparticle grown at same conditions in (a) and (b) with no AsH<sub>3</sub> flow during temperature ramp up.

shown in the side view FE-SEM image in Figure 3.2 (a) and the top view FE-SEM image in Figure 3.2 (b). A few islands show two InAs NWs due to the presence of two Au nanoparticles in a close proximity. In the absence of AsH<sub>3</sub> during temperature ramp up, multiple NWs grow from a single InAs island formed around a single Au nanoparticle as shown in the side view FE-SEM image in Figure 3.2 (c) and top view FE-SEM image in Figure 3.2 (d). It is known that the decomposition temperature of InAs to produce As<sub>x</sub> in the form of As<sub>2</sub> and As<sub>4</sub> is lowered by ~ 300 °C in the presence of Au.<sup>29</sup> The presence of AsH<sub>3</sub> in the growth chamber during the temperature ramp compensates the decomposed

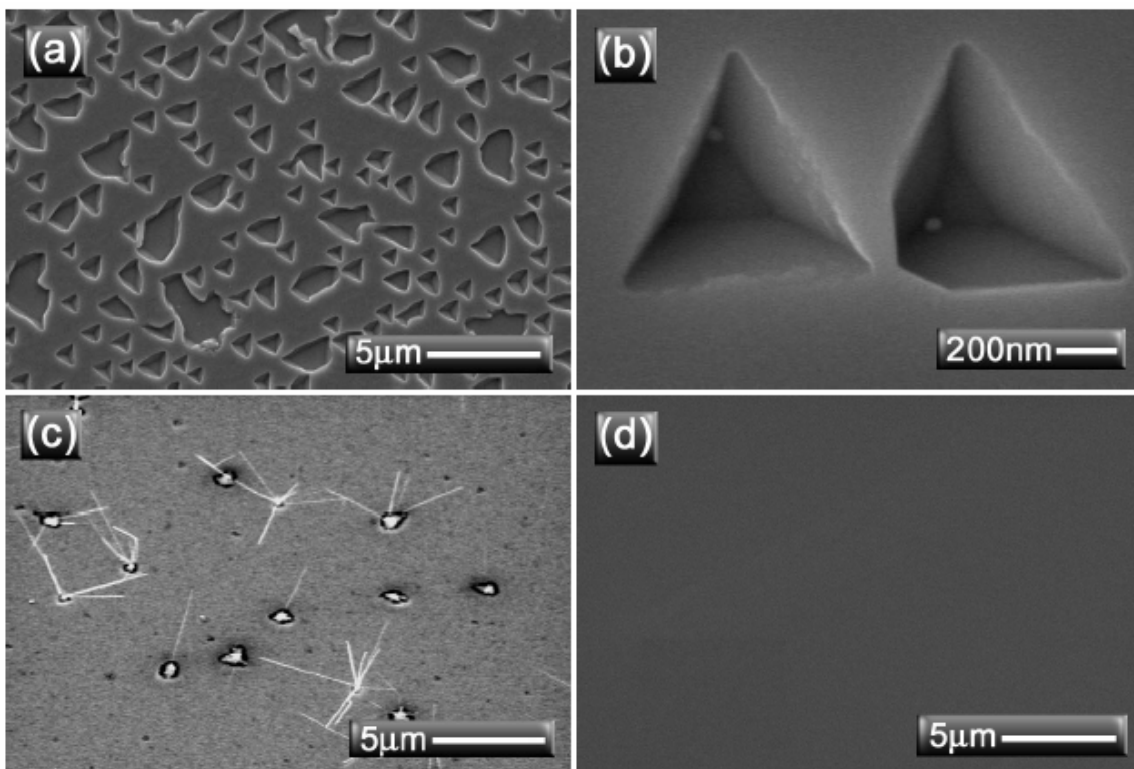


Figure 3.3. FE-SEM images of a) InAs (111)B surface with Au nanoparticles atop heated to 500 °C under  $\text{AsH}_3$  flow. b) Zoom in view of etch pits formed on the InAs (111)B surface around Au nanoparticles. c) InAs NWs grown on InAs (111)B surfaces in a closed tube in the presence of Au nanoparticles. d) InAs (111)B substrate without Au nanoparticles atop subjected to same growth conditions as in (c). No NWs were observed.

$\text{As}_x$  and prevents the formation of In droplets that can initiate NW growth. In the absence of  $\text{AsH}_3$  during temperature ramp up, As sublimation leaves an In rich surface, especially around the Au nanoparticle where the decomposition is most effective, allowing formation of In droplets that can initiate multiple InAs NW growth.

The catalytic decomposition of the InAs substrate by Au nanoparticles is further illustrated in Figures 3.3 (a) and 3.3 (b), which clearly show that deep etch pits form only around Au nanoparticles on the InAs (111)B substrate when the substrate temperature was ramped up to 500 °C and cooled down in  $\text{AsH}_3$  flow. It can be clearly seen in Figure

3.3 (b) that Au nanoparticles are present at the bottom of the etch pits. No such severe decomposition was found on a substrate without Au nanoparticles when subjected to identical conditions.

To further illustrate the catalytic decomposition of the InAs substrate, we performed growth in a simple closed CVD tube containing an InAs (111)B substrate with Au nanoparticles at 550 °C for 5 min and a pressure less than 0.1 Torr. From Figure 3.3 (c), it is evident that substrate decomposition is enhanced in the vicinity of the Au nanoparticles where single or multiple NWs grow. This result, in the absence of any additional source other than the growth substrate itself, is different from previously reported InAs NW growth using a two temperature zone closed CVD tube.<sup>10</sup> Under identical growth conditions but without Au nanoparticles on the InAs (111)B substrate, no severe surface decomposition was found, as shown in Figure 3.3 (d). These results further demonstrate the catalytic effect of Au nanoparticles on decomposition of the InAs substrate and suggest that material incorporation of both group III and group V constituents from the substrate can occur in the grown NWs – an observation with important consequences for purity and doping control in III-V NW growth on a III-V substrate. However, during MOCVD NW growth, the abundant material constituents from the input precursors dominate material incorporation into the NW and minimize substrate decomposition. These results also highlight the importance of maintaining AsH<sub>3</sub> flow during temperature cool down to prevent NW decomposition after growth.

As the growth temperature is increased in a closed system, the growth density and the length of the NWs decrease. Growth using this technique was observed up to temperatures greater than 600 °C with a nanoparticle density of  $\sim 0.04 \mu\text{m}^{-2}$ , above which

no NWs were observed on top of the substrate. If the density of the Au nanoparticles increases, the upper limit of the growth temperature decreases (eg. 550 °C for a nanoparticle density of  $\sim 0.5 \mu\text{m}^{-2}$ ). Higher growth temperature and larger Au nanoparticle density both enhance the substrate decomposition and As sublimation, and thus increase the local V/III ratio during growth. As a result, the NW growth rate is reduced, as discussed in chapter 2.

### 3.4.3 Growth of InAs Nanowires in the Absence of Metal Particles

To further illustrate InAs NW growth from In droplets in the absence of a foreign metal catalyst, we performed growth experiments on a bare InAs (111)B substrate. The substrate was heated to a growth temperature of 400 °C in AsH<sub>3</sub> flow of 44.6  $\mu\text{mol}/\text{min}$ . After the temperature stabilized, the AsH<sub>3</sub> flow was switched off and TMIIn (6  $\mu\text{mol}/\text{min}$ ) was introduced for 90 s. Figure 3.4 (a) shows a typical SEM image of In droplets with diameters ranging from 50 nm to 200 nm formed atop the InAs (111)B substrate from TMIIn decomposition. Without interrupting the growth after pre-depositing In droplets, the AsH<sub>3</sub> and TMIIn input precursors were introduced for NW growth at 400 °C, followed by temperature cool down in AsH<sub>3</sub> flow. Figure 3.4 (b) shows InAs NWs grown for 15 min, with diameters in the range of 200 – 300 nm. The growth density of these NWs does not correspond to the In droplet density obtained in Figure 3.4 (a) due to the continual supply of In throughout the growth experiment. Note that all NWs grown for 15 min have flat tips, smooth surfaces, and hexagonal facets as shown in the top view inset of Figure 3.4 (b), similar to prior reported growth of InAs NWs on SiO<sub>x</sub> surfaces.<sup>16,19</sup> The absence of a globule on the NW tips can be attributed either to In consumption when the TMIIn



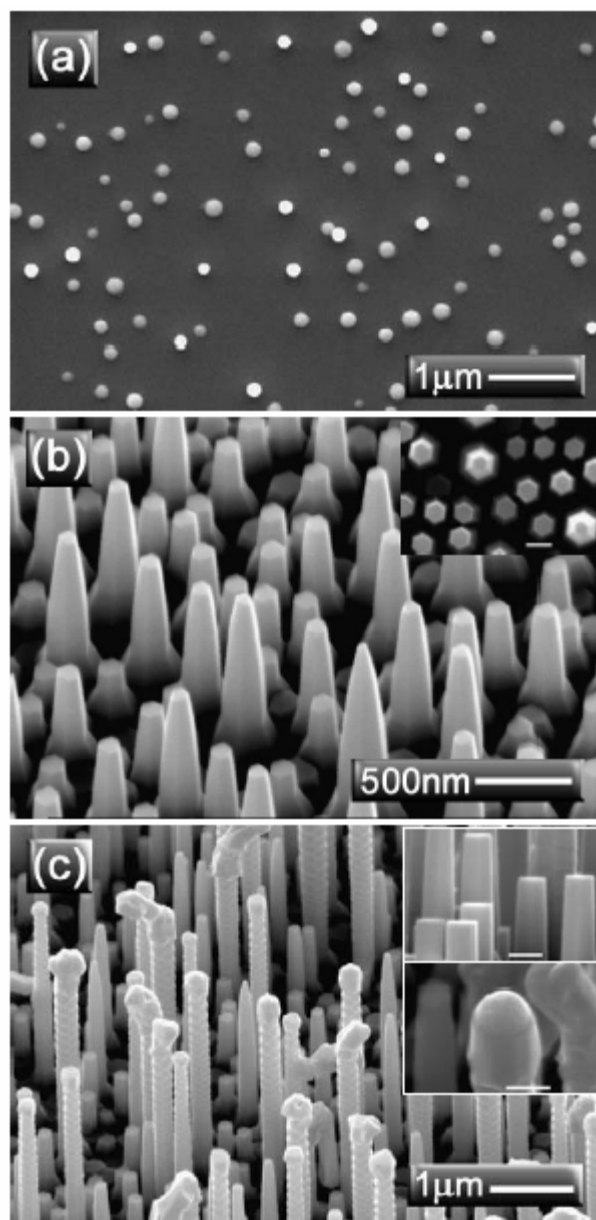


Figure 3.4. InAs NW growth from In droplets: a) Top view FE-SEM image of In droplets formed on InAs (111)B substrate after 90 s TMI exposure. 45° angle view of b) InAs NWs grown for 15 min. Inset is a top view image showing hexagonal facets of InAs NW sidewalls. c) InAs NWs grown for 30 min, top inset shows flat tips for shorter NWs and bottom inset shows a globule at the longer NW tip.

precursor is shut off and AsH<sub>3</sub> flow is maintained during temperature cool down, or to In evaporation from the globule during growth.<sup>30</sup>

Figure 3.4 (c) shows InAs NWs grown for 30 min using identical growth conditions as in the 15 min growth (Figure 3.4 (b)). Two kinds of NW morphologies were observed: (1) short NWs with flat tips and smooth surfaces as shown in the top inset of Figure 3.4 (c), and (2) long NWs with faceted tips, where the bases of the NWs have smooth surfaces and the upper sections show periodic variation in diameter as seen in Figure 3.4 (c). The globular tips are typically larger than the NW diameter and have irregular shapes, except for a few where a spherical globule is maintained as shown in the bottom inset of Figure 3.4 (c). The faceted tips could be formed during temperature cool down where AsH<sub>3</sub> flow is maintained and excess In at the NW globule is consumed after the TMIIn supply was stopped. This was also suggested for Ge whiskers that showed faceted tips when grown from Au seeds.<sup>30</sup> Periodic instability in NW/whisker growth is typically observed due to variation in the supersaturation of the growth droplet at the tip of the NW.<sup>30</sup> Givargizov proposed a self-oscillation model to explain the periodic instability in Si whiskers with a positive feedback due to fluctuation in the curvature of the growth droplet which alters its supersaturation, its surface roughness at the liquid solid interface, and its contact angle.<sup>31</sup> Such periodic oscillations were also observed in InAs whiskers grown at 800 °C on GaAs (111)B, and disappeared as the growth temperature was decreased.<sup>32</sup> In the case of the InAs NWs shown in Figure 3.4 (c), it is highly plausible that higher In concentrations, available from TMIIn source, in globules of some NWs lead to longer growth after the cessation of the shorter wires. The periodic instability in their diameters can thus be explained by Givargizov's model. In general,

there is no diameter dependence for cessation of the NW growth. Therefore, instability<sup>33</sup> in NW growth or Ostwald ripening behavior,<sup>34</sup> where the smaller diameter NWs lose their caps either to the bottom of the NW<sup>33</sup> or to the larger diameter NWs,<sup>34</sup> could be excluded as possible reasons for the cessation in the NW growth and formation of flat tips. Toward the edge of the substrates, a few thin NWs show globules at their tips, and the globule size decreases as the NW length increases and finally vanishes resulting in needle like NWs.

Without the in-situ In pre-deposition step through exposing the InAs (111)B surface to TMI<sub>n</sub> flow, no InAs NW growth was observed. InAs NWs can grow at certain sites where excess liquid In is formed. A low temperature of 400 °C is required to maintain the liquid In on the substrate. At higher temperatures, excess In is subject to crystallization resulting in surface growth rather than NW growth. For example, at a growth temperature of 460 °C, fewer NWs, which are generally needle-shaped, are grown. We have noted earlier that growth from excess In droplets can occur at 520 °C when Au nanoparticles are present on the substrate surface (Figure 3.2 (c) and 3.2 (d)). In the latter case, the Au nanoparticle not only catalyzes the decomposition of AsH<sub>3</sub> but also acts as a material sink for both In and As. When high TMI<sub>n</sub> flow is maintained during growth, NWs can grow from In droplets in the presence of Au at even higher growth temperatures of ~ 500 °C.

### 3.4.4 Summary

In this section, we have shown that excess liquid In nucleates InAs NWs on an InAs (111)B substrate through the VLS growth mechanism during MOCVD growth. The liquid In can be supplied either from the input precursor or from substrate decomposition that is enhanced in the presence of Au nanoparticles. InAs NW growth in a closed system confirms the catalytic decomposition of the InAs substrate by Au nanoparticles and also shows that both group III and group V constituents decomposed from the growth substrate can be incorporated into the NWs. InAs NWs were also observed to grow from pre-deposited In droplets. Faceted tips and periodic instability in the diameter of long NWs were observed due to fluctuations in the curvature of the In droplet. Since In is one of the growth constituents, short NWs with flat tips or needle like NWs were formed due to In consumption during growth. These insights reveal new key processes during the growth of III-V semiconductor nanowires and aid in understanding their growth mechanism.

### 3.5 Temperature and Input V/III Ratio Effects

In this section, we discuss the dependence of Au assisted InAs NW growth on InAs (111)B substrates on substrate temperature and input V/III precursor ratio using OMVPE. Temperature dependent growth was observed within certain temperature windows that are highly dependent on input V/III ratio ( $\sim 425 - 560$  °C with a peak growth rate at  $\sim 530$  °C for V/III=7.5 and  $\sim 425 - 510$  °C with a peak growth rate at  $\sim 475$  °C for V/III=60). This dependence was found to be a direct consequence of the

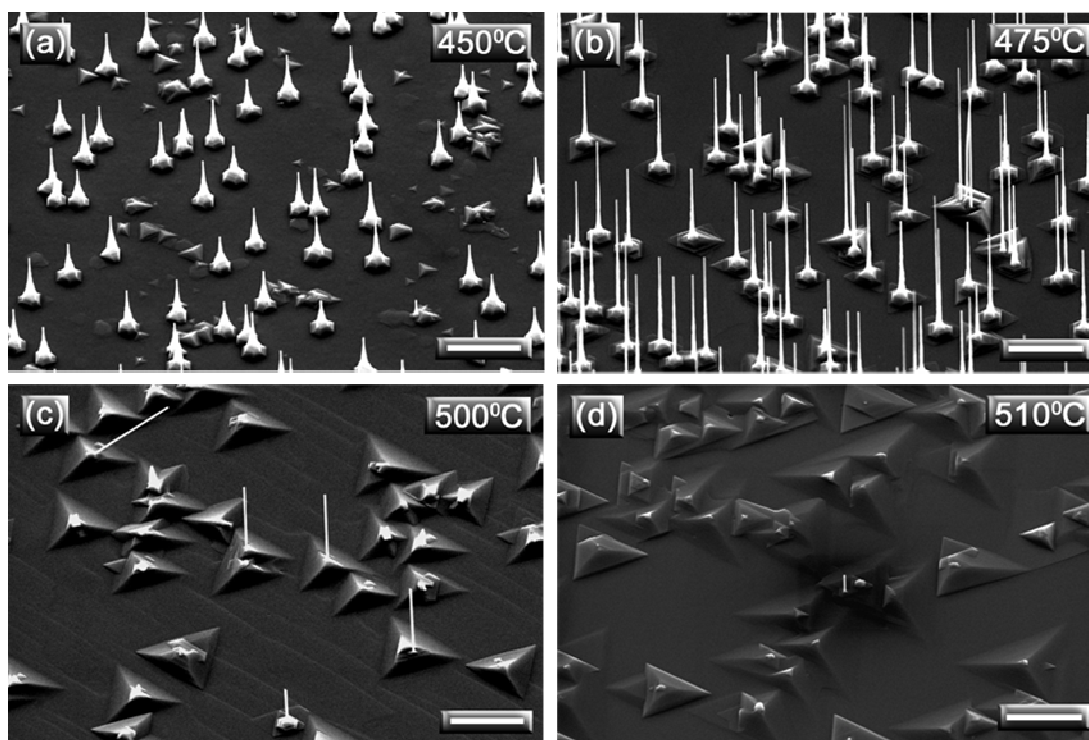


Figure 3.5. Growth of InAs NWs on InAs (111)B at a constant V/III=60 and different growth temperatures. Scale bars are 2  $\mu\text{m}$ .

drop in the NW growth rate with increasing V/III ratio at a constant growth temperature due to depletion of Indium at the NW growth sites. Our results demonstrate that surface kinetics, which control Indium diffusion to the growth globule, are influenced by both growth temperature and input V/III ratio, and support the general validity of the VLS growth mechanism for III-V NWs.

### 3.5.1 Temperature Dependent Growth Rates

The temperature dependent InAs NW growth rate on InAs (111)B substrates was studied by fixing the input V/III ratio at 60 with a TMIIn flow rate of 0.75  $\mu\text{mol}/\text{min}$ , and

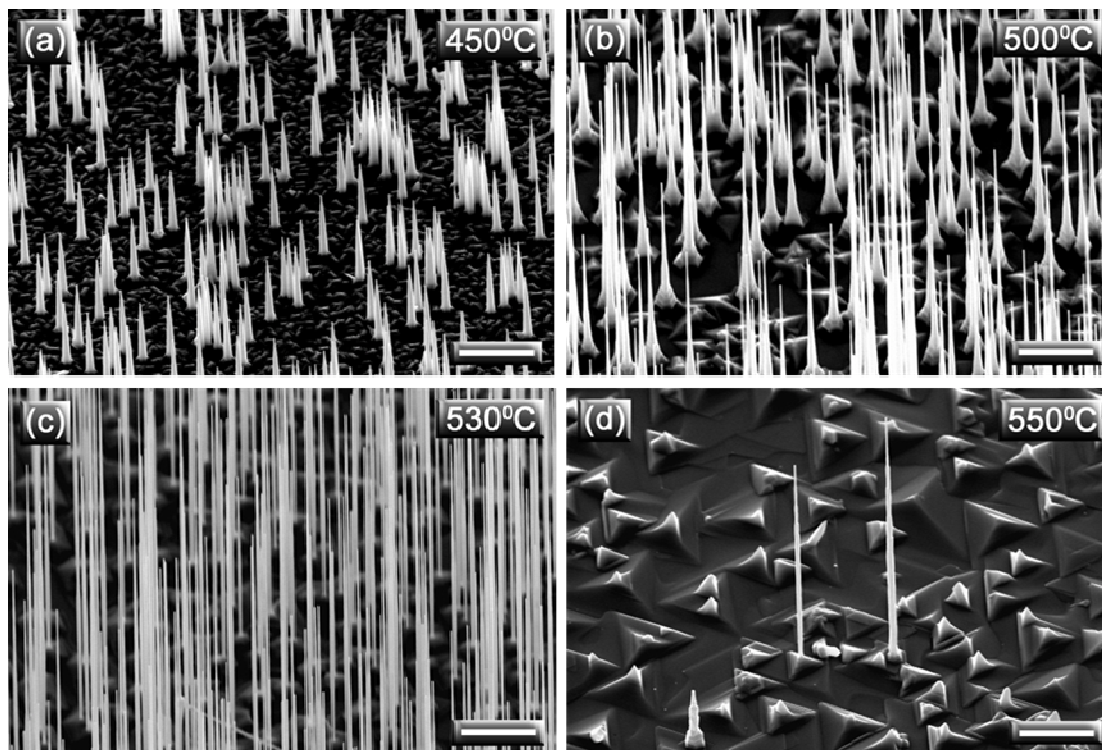


Figure 3.6. Growth of InAs NWs on InAs (111)B at a constant  $V/III=7.5$  and different growth temperatures. Scale bars are  $2\mu\text{m}$ .

varying the substrate temperature in the range of  $425 - 525\text{ }^{\circ}\text{C}$ . Figure 3.5 (a) – (d) shows  $45^{\circ}$  angle Field Emission Scanning Microscope (FE-SEM) images of the resulting InAs NWs at different temperatures, taken from the center of InAs (111)B samples of similar area for consistency in comparison. The NW growth rate increases as the temperature increases up to  $\sim 475\text{ }^{\circ}\text{C}$ , after which the NW growth rate drops. No NW growth was observed at a temperature of  $525\text{ }^{\circ}\text{C}$ . This is consistent with earlier growth reports on the temperature dependence of InAs NW growth.<sup>8,9</sup> However, as the input  $V/III$  ratio is altered, the nanowire growth exhibits different cessation temperature. Figure 3.6 (a) – (d) shows  $45^{\circ}$  FE-SEM images of InAs NWs grown in the temperature range of  $425 - 560\text{ }^{\circ}\text{C}$  with a TMIIn flow rate of  $6\text{ }\mu\text{mol}/\text{min}$  (input  $V/III=7.5$ ). Growth at the same

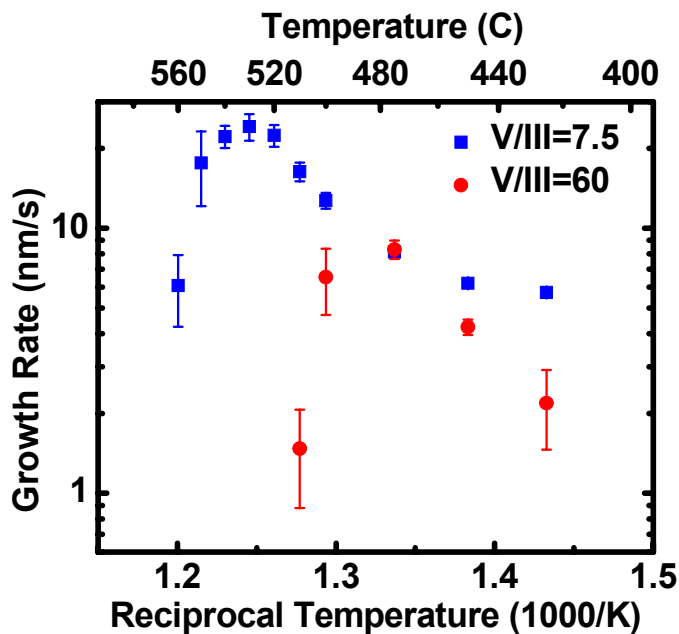


Figure 3.7. Temperature dependent growth rate of InAs NWs on InAs (111)B substrates for two different V/III ratios. Red dots are obtained at a TMIIn flow rate of  $0.75\mu\text{mol}/\text{min}$  ( $V/\text{III}=60$ ) and blue squares were obtained at an input flow rate of  $6\mu\text{mol}/\text{min}$  ( $V/\text{III}=7.5$ ).

temperature and lower V/III ratio leads to longer NWs with higher density. NW growth persists up to at least  $560\text{ }^\circ\text{C}$ , which is higher than the temperature at which NW growth rate drops sharply at an input V/III ratio of 60.

Figure 3.7 shows the temperature dependent growth rate calculated for the two sets of growth experiments described above. Although the NW growth rate should take into account the NW growth density and volume,<sup>35</sup> here only the NW lengths are considered for consistent comparison with other growth reports by Dick et al.<sup>8,9</sup> For the two studied input V/III ratios, the NW length increases with temperature due to the lowered energy barriers and increased surface In adatom mobility. At a V/III ratio of 60, the InAs NW growth rates and the temperature ( $\sim 510\text{ }^\circ\text{C}$ ), at which the NW growth ceases, are very similar to those reported in a similar growth experiment performed at a

V/III ratio of 67.<sup>8</sup> However, we observe that the NW growth rate drops sharply at about 560 °C at an input V/III ratio of 7.5, which is ~ 50 °C higher than that for V/III ratio of 60. These results demonstrate that the input V/III ratios strongly influence the temperature dependence of NW growth and cessation, in contrast to what has been postulated previously.<sup>8</sup> Similar activation energy of ~ 116 KJ/mol for both V/III ratios were extracted. This implies that the activation energy for NW elongation does not vary significantly with input V/III ratio once the InAs NW nucleates. Thin film growth rates, however, are dependent on the V/III ratio, which is attributed to differences in the probability of adsorption/desorption of adatoms on the substrate surface,<sup>36</sup> and to the reduction of the pyrolysis activation energies as the input V/III ratio is increased.<sup>37</sup>

### 3.5.2 V/III Ratio Dependent Growth Rates

To elaborate on the dependence of growth rate on the input V/III ratio, we have performed a set of experiments at 500 °C and varied input V/III ratio. Figure 3.8 shows FE-SEM images of InAs NWs grown on InAs (111)B at T=500 °C, and with a constant TMIIn flow rate of 0.97  $\mu\text{mol}/\text{min}$  and different AsH<sub>3</sub> flow rates. For V/III ratios of 92 (Figure 3.8 (a)) and 150 (not shown), no NW growth was observed at the center of the sample. It is known that the activation energy for the heterogeneous reactions at the growth interface (which are dependent on precursor pyrolysis) decreases as the input V/III ratio is increased.<sup>38</sup> Thus, the mobility of available In on the substrate surface is reduced due to crystallization on the substrate surface rather than at the NW growth site at its tip. Due to the resulting depletion of In from the NW growth sites, the NW



nucleation rate drops as the effective V/III ratio is increased. Thus, VS or thin film growth is expected to be favored over VLS growth as the V/III ratio is increased. The inset of Figure 3.8 (a) shows a cross-sectional FE-SEM image with InAs islands formed under Au nanoparticles but with no NW growth. The enhanced surface growth under the Au nanoparticle is due to more efficient AsH<sub>3</sub> pyrolysis in the nanoparticle vicinity and consequently the more favored surface growth. As the V/III ratio is reduced to 68 (Figure 3.8 (b)), InAs NWs grow, but at a relatively small density of NW/Au nanoparticle (~ 3 %). At a V/III ratio of 45 (Figure 3.8 (c)), more efficient NW growth is obtained (~ 50 % NW/Au nanoparticle), and the average NW length is slightly increased. Further reduction in the V/III ratio is limited by the accuracy of the AsH<sub>3</sub> mass flow controllers in our OMVPE system. Note that at high V/III ratios, some NWs grow at an angle with respect to the substrate normal (Figure 3.8 (b)).

On the other hand, for a fixed AsH<sub>3</sub> flow rate of 44.6  $\mu\text{mol}/\text{min}$ , the NW growth rate and density are reduced as the input V/III ratio is increased due to the direct dependence of the growth rate on group III flow for V/III ratio greater than 1. Specifically, at a V/III ratio of 60 corresponding to a TMIn flow rate of 0.75  $\mu\text{mol}/\text{min}$ , the growth density was ~ 15 % NW/Au nanoparticle whereas for very low V/III ratios (< 10) corresponding to a TMIn flow rates (> 4.7  $\mu\text{mol}/\text{min}$ ), multiple NWs per single InAs island can grow as seen in Figure 3.1. Figure 3.9 shows a plot of the NW growth rate as function of the input V/III ratio obtained by changing either AsH<sub>3</sub> or TMIn precursor flow rates demonstrating reduction in the effective NW growth rate as the input V/III ratio increases. The NW growth rate  $\rho$  was calculated using  $\rho = \frac{L}{t} \frac{N}{M}$ , where  $L$  is the

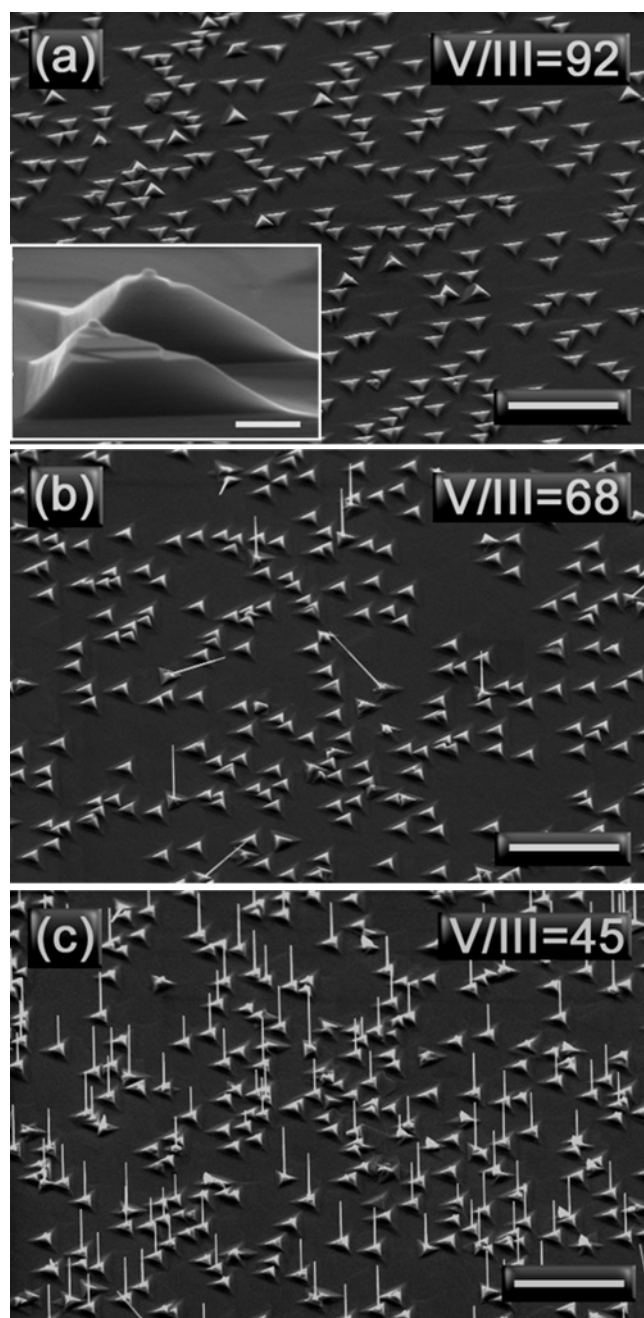


Figure 3.8. 45° FE-SEM images of InAs NWs grown at 500 °C and different input V/III ratios. Scale bars are 5  $\mu\text{m}$ . Inset of (a) is a cross-sectional view of two islands showing surface growth with Au nanoparticles atop the islands. Inset scale bar is 200 nm.

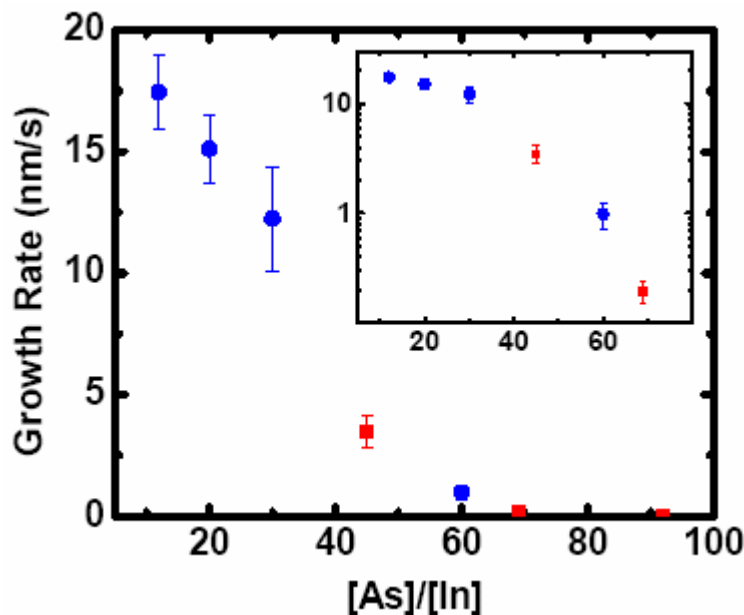


Figure 3.9. Input V/III ratio dependent growth rate of InAs NWs on InAs (111) B at a growth temperature 500 °C. Inset is the same growth rate plotted in log scale. Blue circles were obtained at a fixed AsH<sub>3</sub> flow rate of 44.6 μmol/min and the red squares were obtained at a fixed TMIn flow rate of 0.97 μmol/min.

average NW length,  $t$  is the growth time, and  $N/M$  is the growth density of NW/Au nanoparticle where  $N$  is the number of NWs and  $M$  is the number of InAs islands formed around the Au nanoparticles, both calculated in constant area. Note from Figure 3.9 that the NW growth rates are dependent on the V/III ratio when either TMIn or AsH<sub>3</sub> are varied. However, the NW growth rate shows a stronger dependence on changing TMIn flow not only because the V/III ratio is changed, but also due to the direct dependence of the growth rate on group III flow for  $V/III \geq 1$ . From the inset of Figure 3.9, we can observe that at high V/III ratios, the NW growth rate drops similarly as both TMIn or AsH<sub>3</sub> flow rates are changed, whereas at low V/III ratios (high TMIn flow), the NW growth rate follows a different and larger slope dictated by the change in TMIn flow.

The growth rate dependence on V/III ratio can be clearly seen on an inert surface of different atomic constituents than the grown material. For example, on SiO<sub>2</sub>/Si surfaces, NW growth is favored at low input V/III ratio with little island growth on the substrate surface. As the input V/III ratio is increased, the NW length, diameter, and growth density decreases until NW growth ceases and the InAs 2D growth density on the SiO<sub>2</sub> surface increases (See chapter 2, section 2.6).

We also observe that the NW growth rate is relatively constant across the growth substrate for a low input V/III ratio, i.e. when the growth rate is high. However, variations in the growth rate from the center toward the edges of the substrate become apparent as the input V/III ratio or temperature increases. Figure 3.10 shows variation in the NW lengths as function of distance from the substrate edge at an input V/III ratio of 150 and growth temperature of 500 °C. The growth density decreases as the distance from the sample edge increases until no NW growth was observed at a distance of 2.4 mm. This is similar to what we have observed for the growths at 510 °C with V/III ratio of 60 and at 550 °C with V/III ratio of 7.5, where little to no NW growth was observed at the center of the substrates (~ 1x1 cm<sup>2</sup>) as seen in Figures 3.5 (d) & 3.6 (d), respectively. NW growth prevails toward the substrate edges with higher growth density, growth rate and different morphology. Such behaviors are commonly referred to as “edge” effects where precursor pyrolysis and barrier layers may differ at the edge from the center of the substrate. Because Au nanoparticles enhance AsH<sub>3</sub> pyrolysis<sup>35</sup> and decomposition of the InAs substrate at high temperatures as demonstrated in section 3.4.2, the local V/III ratio is thus expected to vary over the substrate surface. This effect is thus maximal at the substrate center as compared to its edges. We believe that substrate decomposition and

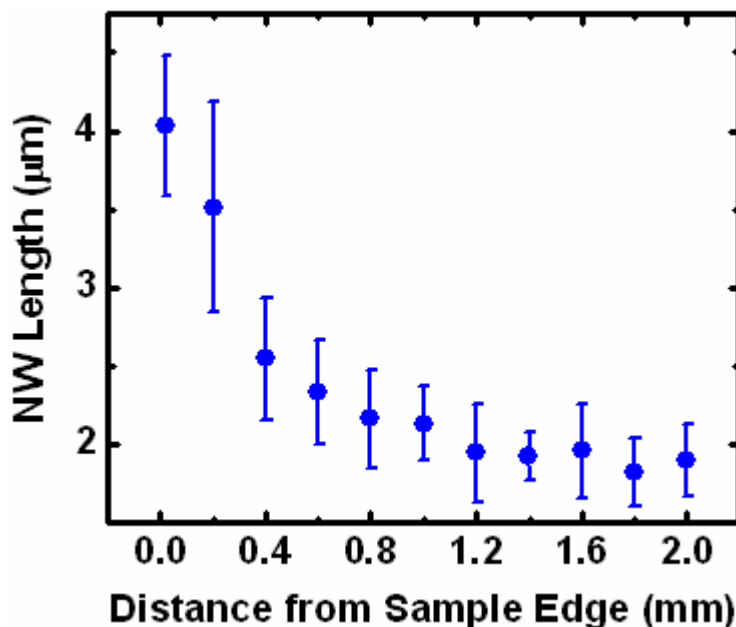


Figure 3.10. Variation of the NW length as function of distance from the sample edge grown at 500°C and input V/III=149 (TMIn=0.9 $\mu$ mol/min and AsH<sub>3</sub>=134 $\mu$ mol/min).

the subsequent alteration of the V/III ratio leads to such variation in the NW growth rate across the sample.

The effective V/III ratio during growth depends not only on the input precursor molar fraction but also the growth temperature. As the temperature is increased, AsH<sub>3</sub> pyrolysis is also increased resulting in a higher effective local V/III ratio, which favors VS growth over VLS growth. Consequently, the NW growth rate drops and eventually the NW growth ceases. More specifically, at a lower input V/III ratio (V/III=7.5) with less group V in the vapor, higher temperatures are required to pyrolyze AsH<sub>3</sub> and create a high enough local V/III ratio to cease the NW growth, when compared to a higher input V/III ratio (V/III=60). This precisely describes the NW growth rate behavior in Figure 3.9. Indeed, the slight difference reported previously in the cessation temperature (490 °C vs. 460 °C) for NW growth on InAs (111)B surfaces subjected to different pre-growth

annealing treatments was attributed to differences in In content in the Au-In alloy particle at the NW tip,<sup>8</sup> as a higher In content would imply a lower melting temperature from the Au-In phase diagram. A close examination of the same growth report, however, shows that input V/III ratios of 67 and 83 resulted in NW growth cessation at 490 °C and 460 °C, respectively, in good agreement with our postulate on the NW growth rate dependence on the input V/III ratio. Therefore, we attribute the difference in the growth rate and cessation temperature to the variation in the input V/III ratio, and not to difference in the melting temperatures of the Au-In particle alloy at the tip of the NW. In a related study of NWs that were grown on InAs (111)B substrates covered with SiO<sub>x</sub>, the contribution of the substrate in altering the effective V/III ratio is likely to be reduced by the capping SiO<sub>x</sub>, which also may allow longer surface diffusion lengths of In adatoms than on the InAs (111)B surface. As a result, In may not be easily depleted from the NW growth sites due to crystallization on the SiO<sub>x</sub> surface and the NW growth would consequently prevail to temperatures higher than those on InAs (111)B surfaces. Thus, we conclude from our studies and analysis of related results that experimental observations of NW growth cessation at different growth temperatures do not necessarily constitute evidence for the VSS growth mechanism for III-V NWs.<sup>8,9</sup> Moreover, as we noted earlier, it has been shown by Park et al. that when the growth substrate is cooled rapidly in a water bath immediately after growth, and thus minimizing In diffusion from the growth globule,<sup>10</sup> the presence of substantial In in the Au nanoparticle suggested growth via the VLS mechanism.<sup>10,11</sup> Furthermore, recent in-situ transmission electron microscope studies on Au catalyzed Ge NW growth have shown hysteresis in the solid-liquid phase transformation with temperature.<sup>15</sup> These studies suggest that post-growth

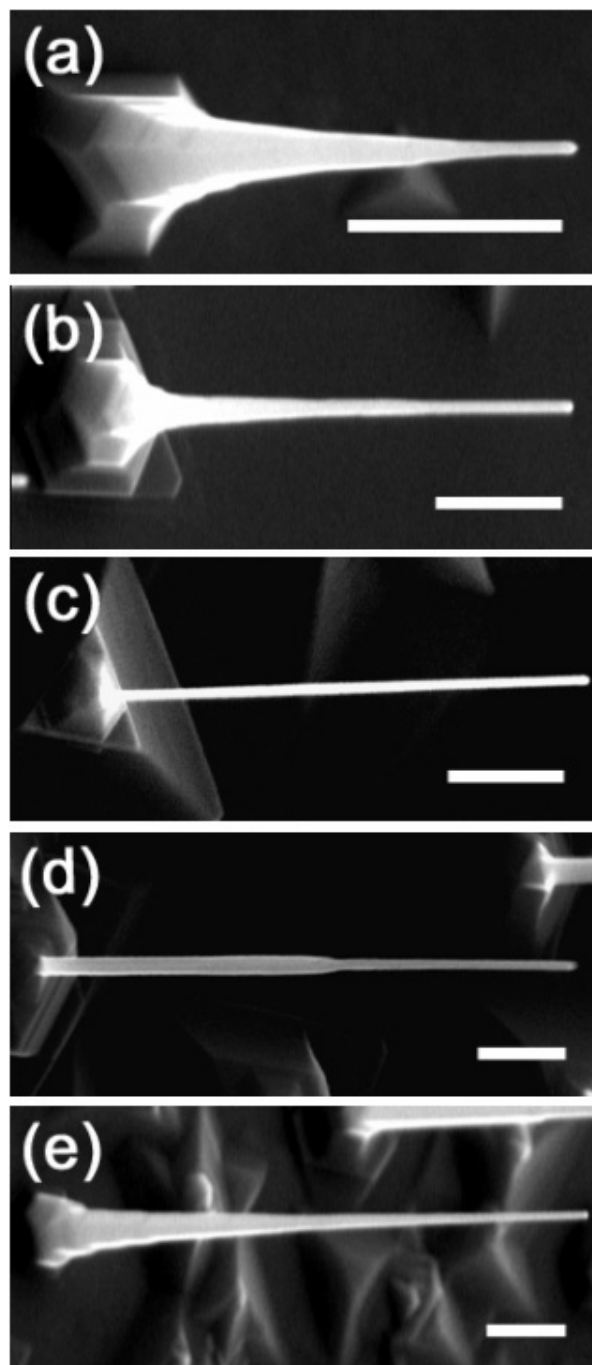


Figure 3.11. 45° FE-SEM images of InAs NWs grown at (a) 450°C, (b) 475°C, (c) 500°C with constant TMIIn and AsH<sub>3</sub> molar flow rate of 0.75 μmol/min and 44.6 μmol/min respectively (V/III=60). InAs NWs grown at 500°C and different TMIIn molar flow rates of (d) 1.5 μmol/min, and (e) 2.25 μmol/min. Scale bars are 500nm.

compositional<sup>8</sup> and phase analyses<sup>6</sup> at the tip of the NW are not necessarily definitive in determining the possibility of growth from a solid seed.

These studies not only enable understanding of the III-V NW growth mechanism, but also allow control over their morphology. Figure 3.11 (a) – (c) shows FE-SEM images of InAs NWs grown at a constant input V/III ratio of 60 and different growth temperatures. As the growth temperature is increased, mobility of In adatoms on the surface of the NW is increased which enables them to reach the growth tip. Thus, tapering which is observed at 450 °C (Figure 3.11 (a)) and 475 °C (Figure 3.11 (b)) is diminished at 500 °C (Figure 3.11 (c)). At a constant growth temperature of 500 °C, if the input TMIn flow rate is increased, more In is available at the surface of the NW, and tapering increases as shown in Figure 3.11(d) and 3.11 (e).

### 3.5.3 Summary

We have shown in this section that OMVPE growth of InAs NWs occurs within certain temperature windows, where NW nucleation and growth increase with increase of temperature, reach maxima, then decrease, and stop. The temperature window within which NWs grow depends on the input V/III ratio, and both the growth temperature and the V/III input ratio determine the NW growth rate and morphology. At a constant temperature, higher V/III input ratio results in higher surface growth rates and reduced NW growth rates. For a constant V/III ratio, III-V NWs grow in the kinetically limited growth regime up to temperatures at which the local V/III ratio is enhanced due to efficient hydride pyrolysis and thus the NW growth rate starts to drop. These results help



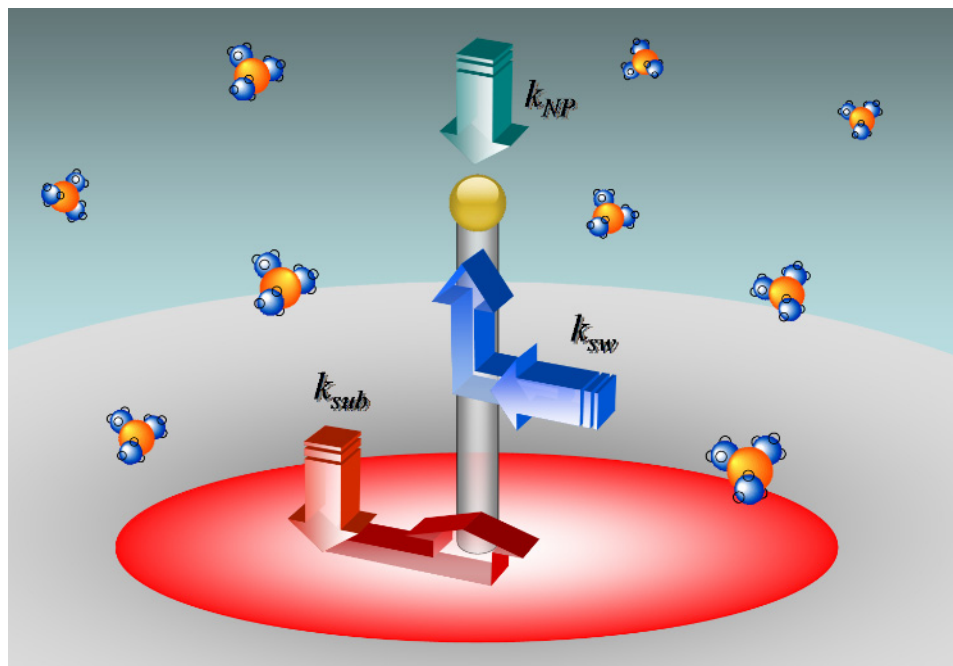


Figure 3.11. Illustration of NW VLS growth including group III flux impingement on the NP, NW sidewalls, and growth substrate, each contributing to the NW growth rate by  $k_{NP}$ ,  $k_{sw}$ , and  $k_{sub}$ , respectively.

in explaining different III-V NW growth behavior obtained from different growth techniques, support the general validity of the VLS growth mechanism for III-V NWs and facilitate control over their growth morphology.

### 3.6 Surface Diffusion in InAs Nanowire Growth

After their observation of whisker growth during vapor condensation of potassium crystals, Dittmar and Neumann were the first to solve the diffusion equation for whisker growth.<sup>39</sup> Blakely and Jackson,<sup>40</sup> Ruth and Hirth,<sup>41</sup> and Simmons et al.<sup>42</sup> have solved similar equations with different boundary conditions and approximations. Ruth and Hirth however have considered the substrate-whisker adatom exchange and identified regimes

in which the whisker elongation varies non-linearly with time for short growth times. Here, we consider a simple model<sup>43,44</sup> to gain insight into the time-dependent NW elongation, which in turn leads to isolation of the most dominant thermodynamic processes occurring during the NW growth.

### 3.6.1 Background

As illustrated in Figure 3.12, material fluxes contributing to the growth may arise from direct impingement on the NP, NW sidewalls, or growth substrate leading to individual contribution to the NW growth rate  $dl/dt$  of  $k_{NP}$ ,  $k_{sw}$ , and  $k_{sub}$ , respectively such that

$$\frac{dl}{dt} = k_{NP} + k_{sw} + k_{sub}. \quad (3.1)$$

Each of these contributions is proportional to the flux of metal-organic precursor impinging on the respective collection area, namely  $S_{NP} = 2\pi r^2$  for material impinging on the NW top,  $S_{sw} = 2\pi r l$  for material impinging on the NW sidewalls, and  $S_{sub} = \pi r_s^2$  for material impinging on the growth substrate, thus leading to a different growth rate behavior as we discuss below. Here,  $r$  is the NW radius,  $l$  is the NW length, and  $r_s$  is the radius of the collection area on the substrate for those adatoms that reach the NW tip and contribute to the VLS growth. By considering that materials that adsorb within  $r_s$  need to diffuse a distance of  $r_s + l$  in order to contribute to the NW growth at the tip, and assigning  $\lambda_{NW}$ , and  $\lambda_{sub}$  for the surface diffusion length on the NW sidewalls and growth substrate, respectively, one can write:

$$r_s = \frac{\lambda_{sub}}{\lambda_{NW}}(\lambda_{NW} - l). \quad (3.2)$$

From above, and with an impingement flux  $J$ , we can write the individual growth rate equations as follows. For the material impinging on the NW tip,

$$k_{NP} \propto \frac{1}{\pi r^2} 2\pi r^2 \cdot J, \quad (3.3)$$

which individually, would lead to a linear NW elongation as function of time.

For material impinging on the NW sidewalls,

$$k_{sw} \propto \frac{1}{\pi r^2} \begin{cases} S_{sw} \cdot \alpha \cdot 2\pi r l \cdot J & (l < \lambda_{NW}) \\ S_{sw} \cdot \alpha \cdot 2\pi r \lambda_{NW} \cdot J & (l > \lambda_{NW}) \end{cases}, \quad (3.4)$$

where  $S_{sw}$  is the sticking coefficient to the NW sidewalls, and  $\alpha$  is the fraction of those which can make it to the NW tip. If one considers only the growth rate due to material impingement on the NW sidewalls, it can be seen directly from equation 3.4 that the NW elongation will proceed exponentially for  $l < \lambda_{NW}$ , and linearly for larger  $l > \lambda_{NW}$ .

For material contribution from the substrate,

$$k_{sub} \propto \frac{1}{\pi r^2} \begin{cases} S_{sub} \cdot \beta \cdot \pi \cdot \left(\frac{\lambda_{sub}}{\lambda_{NW}}\right)^2 (\lambda_{NW} - l)^2 \cdot J & (l < \lambda_{NW}) \\ 0 & (l > \lambda_{NW}) \end{cases}, \quad (3.5)$$

where  $S_{sub}$  is the sticking coefficient to the substrate surface, and  $\beta$  is the fraction of those which can make it to the NW tip. In the case of only substrate contribution to the NW growth rate, one can deduce from equation (3.5) a sub-linear time-dependent NW elongation of  $\lambda_{NW}^2 Kt / 1 + \lambda_{NW} Kt$ , where  $K$  is a constant. Note also that the strength of the substrate contribution to the total NW growth rate is dependent on the  $\lambda_{sub} / \lambda_{NW}$  ratio, which is key to determination of substrate-NW adatom exchange.

By combining equations (3.1) – (3.5) for all contributions, we can write:

$$\frac{dl}{dt} = \begin{cases} A + \frac{B}{r}l + \frac{C}{r^2} \left( \frac{\lambda_{sub}}{\lambda_{NW}} \right)^2 (\lambda_{NW} - l)^2 & \text{for } l < \lambda_{NW} \\ A + \frac{B}{r} \lambda_{NW} & \text{for } l > \lambda_{NW} \end{cases}, \quad (3.6)$$

where  $A$ ,  $B$ , and  $C$  are constants from equations (3.3) – (3.5).

The solution of equation (3.6) can be written as:

$$l = \begin{cases} \Lambda - \eta \tan \left( -\frac{\eta Ct}{r^2} + \arctan \left( \frac{\Lambda}{\eta} \right) \right) & \text{for } l < \lambda_{NW} \\ \lambda_{NW} - \left( \frac{\lambda_{NW} B}{r} + A \right) (t - t_\lambda) & \text{for } l > \lambda_{NW} \end{cases}, \quad (3.7)$$

$$t_\lambda = \frac{1}{C} \left[ \arctan \left( \frac{\lambda_{NW} - \Lambda}{\eta} \right) + \arctan \left( \frac{\Lambda}{\eta} \right) \right]$$

where

$$\Lambda = \lambda_{NW} - B/2C$$

$$\eta = \sqrt{4AC + 4\lambda_{NW}BC - B^2/2C}$$

We shall show next that InAs NW elongation as function of time and diameter can indeed be well described by equation (3.7).

### 3.6.2 Experimental Results and Discussion

The InAs NW growth from 40 nm diameter Au nanoparticles on InAs (111)B substrates at 500 °C was performed for different growth times. Figure 3.12 (a) – (h) show FE-SEM images of InAs NWs grown with a TMIn flow rate of 1  $\mu\text{mol}/\text{min}$  as function of time. For short growth times (Figure 3.12 (a) – (e)), uniform NWs with 40 nm diameter dictating that of the Au nanoparticle are observed with a non-linear elongation with time.

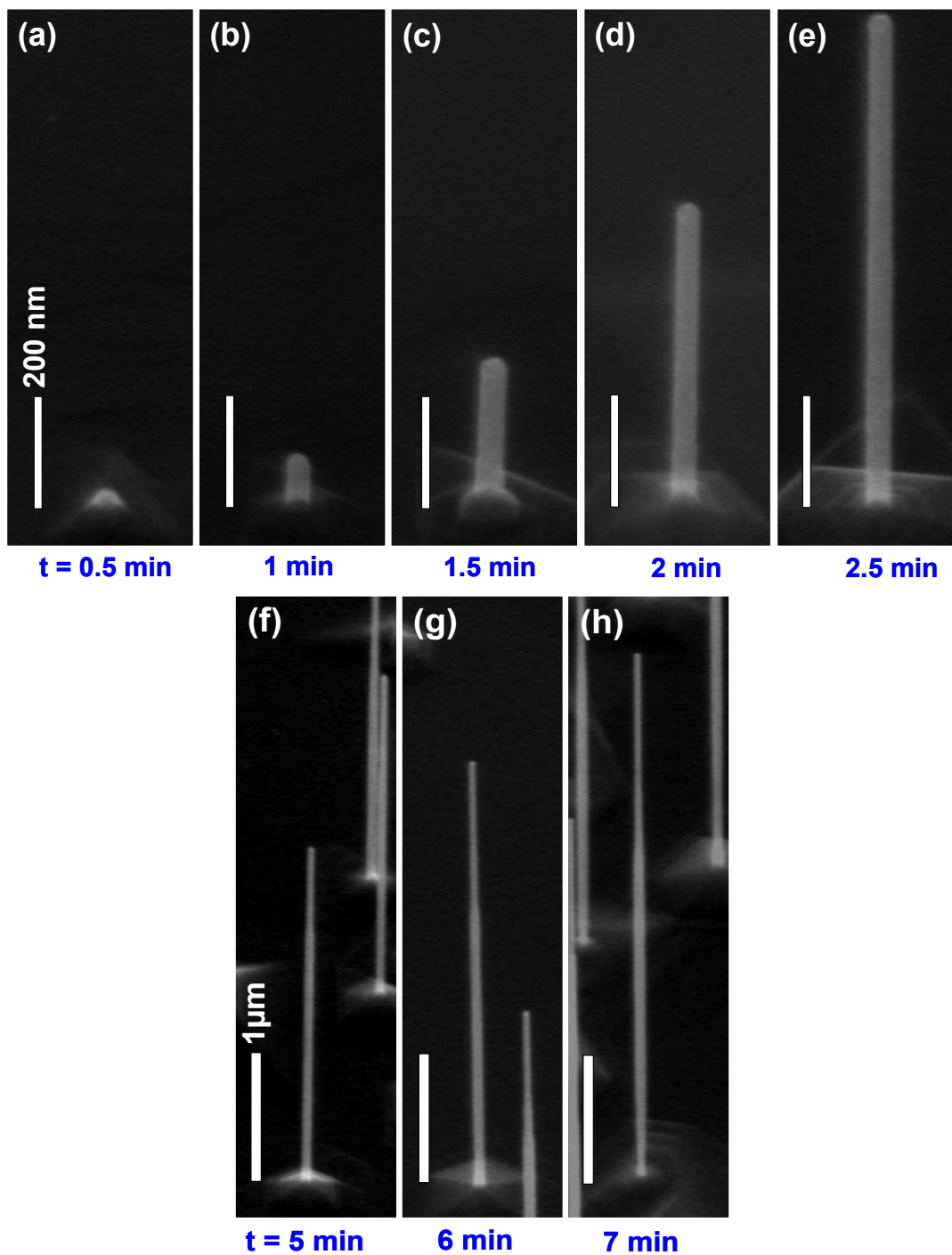
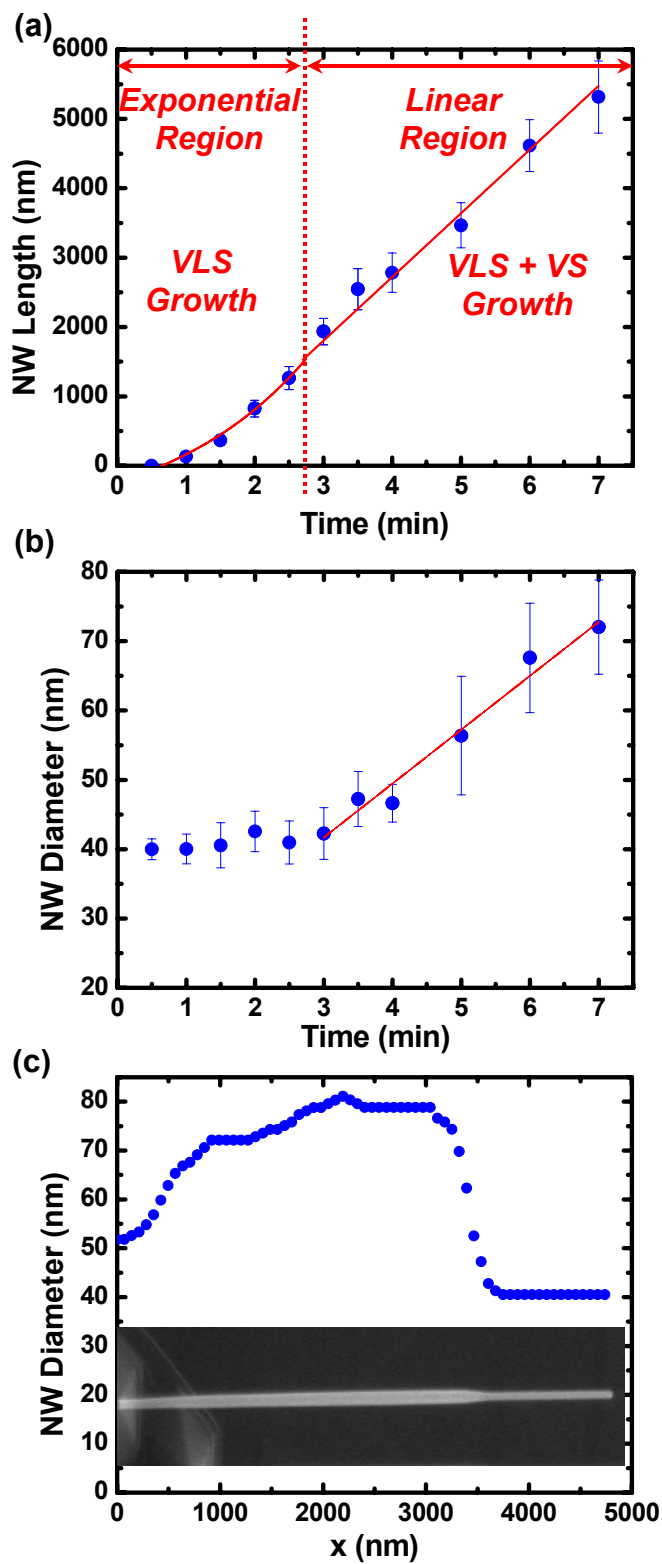


Figure 3.12.  $45^\circ$  angle view FE-SEM images of InAs NWs grown with  $1 \mu\text{mol}/\text{min}$  TMIn flow rate at  $500 \text{ }^\circ\text{C}$  for different growth times.

Figure 3.13. (a) Plot of the NW length as function of time at a TMIn flow of 1  $\mu\text{mol}/\text{min}$ . NW elongation with time switches from exponential (VLS growth) to linear (VLS + VS growth) for  $l > 1 \mu\text{m}$ . (b) Plot of the NW diameter as function of time for the same set of NWs whose lengths are plotted in (a). (c) Plot of the NW diameter variation as function of length for an InAs NW grown for 7 min, whose FE-SEM is shown as inset, showing a uniform section near its tip whose length is  $\sim 1 \mu\text{m}$ .



For long growth times (Figure 3.12 (f) – (h)), the NW diameter is larger than 40 nm across the major portions of the NW, and becomes  $\sim 40$  nm close to the NW tip and close to the substrate. The NW length seems to increase linearly with time in Figure 3.23 (f) – (h). Note that in Figure 3.12 (a) – (e), planar growth at the bottom of the InAs NW increases with time while the NW maintains a uniform diameter as time progresses. This, in addition to the fact the diameter of the NW base is always close to  $\sim 40$  nm for all  $t$ , indicates that the substrate acts as a material sink for adatoms that adsorb on the NW sidewall within  $\lambda_{NW}$  from the substrate and that  $\lambda_{sub} \ll \lambda_{NW}$ .

Figure 3.13 (a) shows a plot of the InAs NW lengths as function of time at the TMI flow rate of  $1 \mu\text{mol}/\text{min}$ . It can be seen clearly from Figure 3.13 (a) that the NW length increases exponentially for short growth time and becomes linear after about 3 min. This dependence can be attributed to the  $k_{sw}$  contribution to the growth rate depicted as can be deduced from equation (3.4). This is expected as the collection area for In adatoms increases as the NW elongates for short growth times where  $l < \lambda_{NW}$ ,<sup>45</sup> which would lead to a super-linear increase of NW length with time, namely an exponential increase. For longer growth times where  $l > \lambda_{NW}$ , the collection area for In adatoms remains constant ( $2\pi r \lambda_{NW}$ ) leading to a linear increase of NW length with time. The transition from the exponential to the linear elongation with time allows extraction of  $\lambda_{NW}$ . As can be seen from Figure 3.13 (a), this transition occurs for  $l > 1 \mu\text{m}$  indicating a  $\lambda_{NW} \sim 1 \mu\text{m}$ . Figure 3.13 (b) shows the NW diameter increase as function of time. It can be seen that in the exponential region of Figure 3.13 (a), the diameter of the NW remains constant  $\sim 40$  nm, whereas in the linear regime of Figure 3.13 (a), where  $l > \lambda_{NW}$ , the NW diameter increases linearly with time due vapor-solid or thin film deposition at the NW



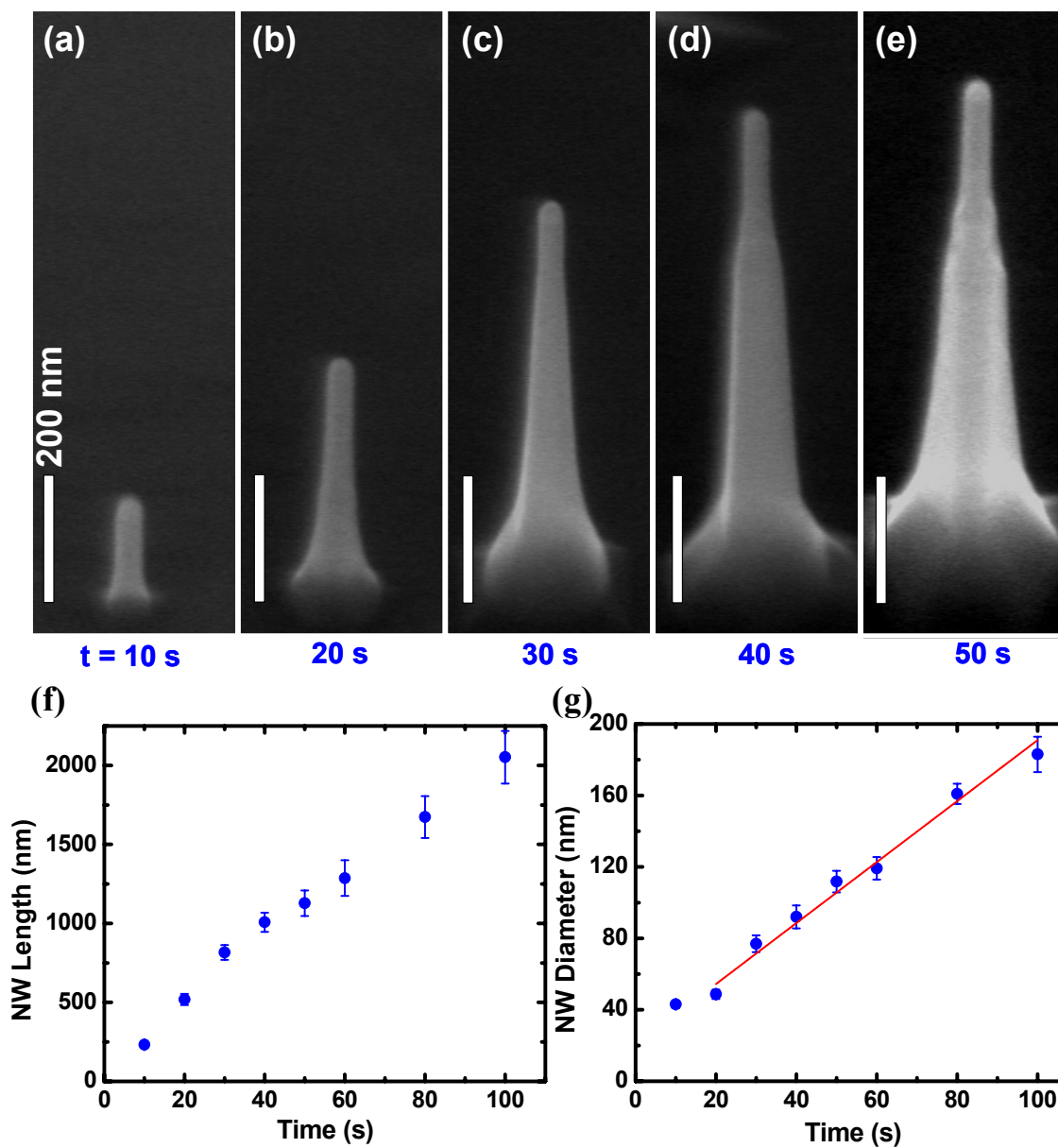


Figure 3.14. (a) – (e) 45° angle view FE-SEM images of InAs NWs grown with 6  $\mu\text{mol}/\text{min}$  TMIIn flow rate at 500 °C for different growth times. (f) Plot of the NW length as function of time at a TMIIn flow of 6  $\mu\text{mol}/\text{min}$ . (g) Plot of the NW diameter as function of time for the same set of NWs.

sidewalls (adatoms cannot make it to the tip anymore and stick to the NW sidewalls or desorb). Figure 3.13 (b) shows a plot of the NW diameter as function of length for a NW grown for 7 min (Inset of Figure 3.13 (c)). The length of the uniform section of the NW near the tip is  $\sim 1 \mu\text{m}$ , within which material can make it to the NW tip, which is in agreement with the transition length of Figure 3.13 (a).

At a higher TMIn flow rate of  $6 \mu\text{mol}/\text{min}$  but otherwise the same growth conditions of Figures 3.12 and 3.13, the NWs grow tapered with large diameters at their bases as shown in Figure 3.14 (a) – (e). Figure 3.14 (f) shows a plot of the NW lengths grown at a TMIn flow of  $6 \mu\text{mol}/\text{min}$  as function of time. It can be seen from Figure 3.14 (a) and (f) that the InAs NWs nucleate earlier at the higher TMIn flow rate (10 s vs 1 min) and elongates at a faster growth rate. The NW length increases sublinearly with time for short growth times and then becomes linear for  $t > 1 \text{ min}$ . At high TMIn flow rates,  $\lambda_{sub}$  of In adatoms on the InAs (111)B increases such that  $\lambda_{sub}/\lambda_{NW}$  becomes appreciable leading to substantial contribution of the substrate to the growth rate as can be seen from equation (3.5). This results in a sublinear NW elongation with time for  $l < 1 \mu\text{m}$  and linear increase afterwards as shown in Figure 3.14 (f) and can be deduced from equation (3.6). Figure 3.14 (g) shows a plot of the NW diameter as function of time showing continual increase of the NW diameter beyond 40 nm for all  $t$ . The NW diameter here is taken at the center of the NW. The radial growth rate (increase in NW diameter) in this case is  $1.64 \text{ nm}/\text{s}$  which is  $\sim 16$  times greater than that at a TMIn flow rate of  $1 \mu\text{mol}/\text{min}$  ( $0.1 \text{ nm}/\text{s}$  for  $t \geq 3 \text{ min}$ ).

Figure 3.15 plots together NW lengths as function of time at the used TMIn flow rates. As discussed earlier, at the low TMIn flow rate, exponential followed by linear NW

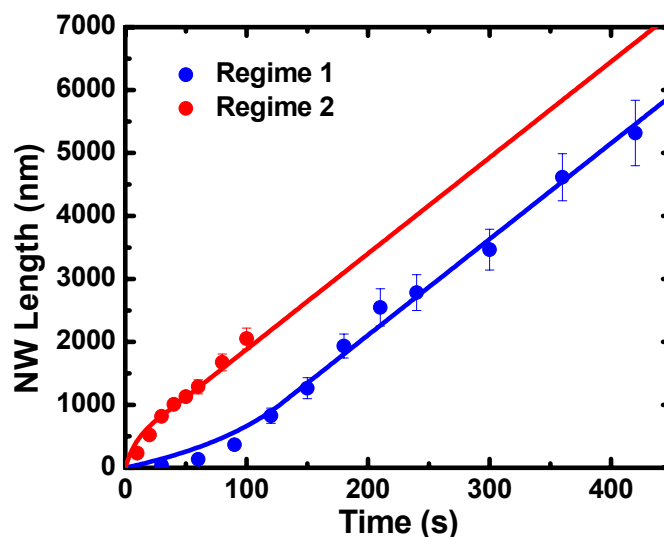


Figure 3.15. Plot of the NW length as function of time for TMIn flow rates of  $1 \mu\text{mol}/\text{min}$  (Regime 1) and  $6 \mu\text{mol}/\text{min}$  (Regime 2). The solid lines are for both regimes using equation (3.7) resulting in  $\lambda_{NW} \sim 1 \mu\text{m}$ .

elongation with time was obtained, whereas a sublinear followed by linear elongation with time was obtained for the higher TMIn flow rate. This allows us to distinguish between two NW growth regimes. In *Regime 1*, where substrate to NW diffusion is minimal, uniform NWs can be obtained for short growth times where the NW elongation proceeds exponentially with time. In *Regime 2*, where substrate-to-NW diffusion is dominant, the NW length increases sub-linearly with time and the NWs are tapered. These experimental results are in excellent agreement with theoretical predictions for NW growth rates as function of time when substrate-NW adatom exchange is taken into account as postulated by Ruth and Hirth,<sup>41</sup> and indicated by equation (3.7). These results provides the first experimental evidence for reciprocal adatom exchange from the substrate to the NW and identifies growth conditions and lengths over which uniform InAs NW morphology can be attained.

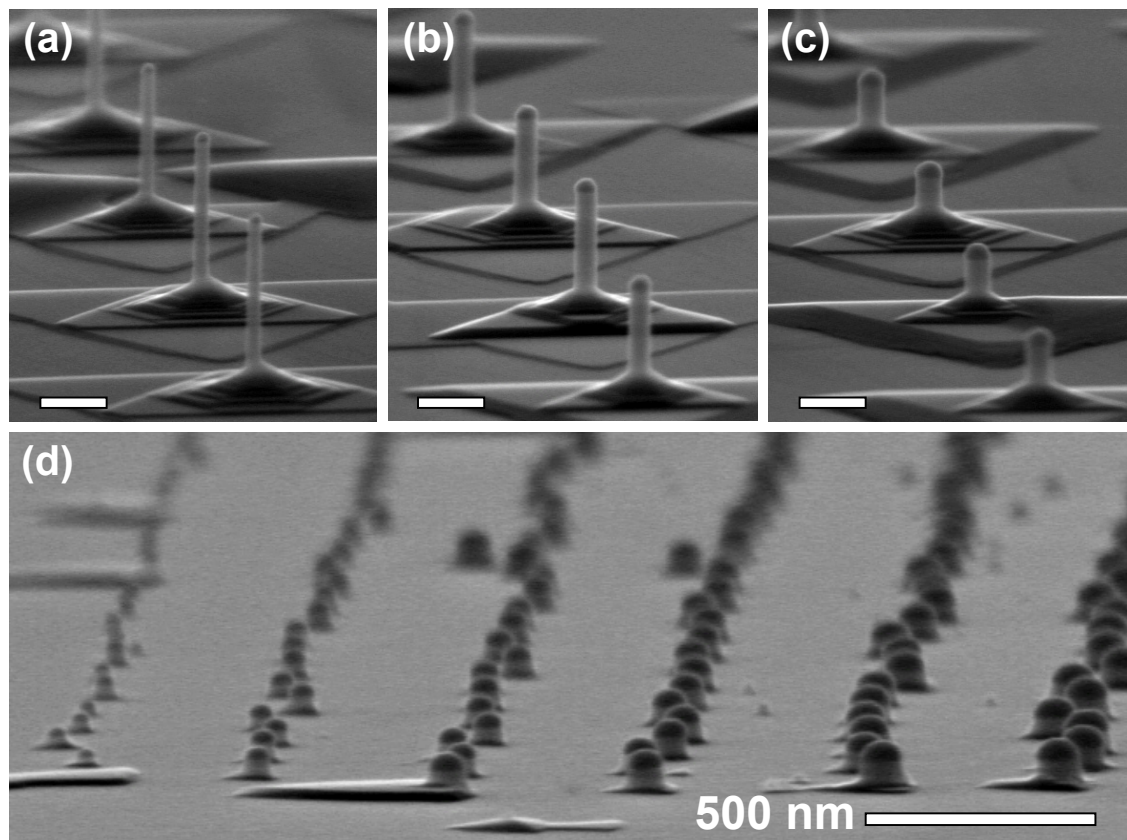


Figure 3.16. 83° angle view FE-SEM images of InAs NWs grown at predefined locations on the same substrate for 120 s with different diameters (a) 45 nm, (b) 70 nm, and (c) 90 nm. Scale bars are 200 nm. (d) 83° angle view FE-SEM images of InAs NWs grown at predefined locations on the same substrate for 30 s with variable diameters of 45 nm (most left) to 115 nm (most right).

This situation is in contrast to GaAs NW growth which independent of the growth substrate and tri-methyl-gallium flow rates, their time dependent elongation display linear dependence as function of time.<sup>44,46</sup> This indicates that the sidewall and the substrate contributions to the total NW growth rate for GaAs NWs are minimal and contribution from the NP is the dominant process. Soci et al. have extracted a diffusion length of  $\sim 10$  nm for Ga species on the GaAs NW sidewalls.<sup>47</sup> This is significantly lower than the Ga “migration length” of 3  $\mu\text{m}$  suggested by Harmand et al. for MBE grown GaAs NWs, and

is in agreement with Borgstöröm et al. postulate of the dominant gas phase diffusion of Ga species in OMVPE growth of GaP NWs.<sup>23</sup>

The solid phase diffusion of In adatoms on the NW sidewalls that leads to the non-linear growth rates for short growth times is further supported by the diameter-dependent growth rates for InAs NWs. Figure 3.16 (a) – (c) shows FE-SEM images of uniform InAs NWs grown for 120 s from 45, 70, and 90 nm Au NP diameters, respectively, patterned by e-beam lithography on the same growth substrate with 2  $\mu\text{m}$  spacing. The growth conditions were similar to those of *Regime 1* in Figure 3.15 (exponential NW elongation with time), where uniform NW morphology is attained while minimizing the substrate contribution to the growth rate. Note that for short growth times, larger diameter NWs nucleate earlier than those of smaller diameters as demonstrated in Figure 3.16 (d). This has been also observed for randomly dispersed Au nanoparticles on InAs (111)B substrates where NW nucleation for 80 nm diameter particles is efficient when compared to NW nucleation from 40 nm diameter particles. This indicates the effectiveness of the Gibbs-Thomson effect when the NW is at the nucleation stage. For GaAs NWs, the diameter dependent growth rates vary with the growth conditions and are dominated by the Gibbs-Thomson effect for small V/III ratios and deviate toward those of diffusion limited growth for high V/III ratios.<sup>43,47</sup>

### 3.6.3 Axial and Radial Heterostructure Nanowire Growth

The studies performed above are of significant importance for achieving control over radial and axial NW heterostructures, since optimal control over the NW

morphology has been demonstrated in section 3.6.3 (necessary for axial heterostructure), and switching from NW to thin film growth is realized through higher growth temperatures and V/III ratios as accomplished in section 2 (necessary for radial heterostructures). We consider here the growth of InAs-InP NW axial and radial heterostructures. Such heterostructures are important in their axial configuration for performing low-dimensional transport studies (eg. single electron transistors as demonstrated in 2002 by Björk et al.)<sup>48</sup> or reducing/eliminating the detrimental effects of surface states in their radial configuration for carrier confinement and high electron mobility applications as demonstrated in 2007 by Jiang et al.<sup>49</sup> We have shown in section 2.5 that InAs NWs decompose at  $T \sim 450$  °C on SiO<sub>2</sub> surfaces, even under AsH<sub>3</sub> overpressure. On InAs (111)B surfaces, it was observed that these NWs decompose at  $T \sim 500$  °C in AsH<sub>3</sub> overpressure, which is the same temperature they were grown at in OMVPE. Perhaps, a similar reason has led Zanolli et al. to perform CBE growth of InAs NWs at 425 °C followed by InP shell growth at a lower temperature of 370 °C.<sup>50</sup> From SEM images of the 20 nm thick InP shell on 20 nm InAs core in Zanolli's et al. report, the morphology of the shell appears to be very rough, with a small angled section at the tip of the NW. Similar experiments performed by us have resulted in amorphous InP shell coating at 400 °C as indicated by TEM studies.<sup>51</sup> Jiang et al. have synthesized InAs-InP core-shell NWs (20 nm – 2 nm) on SiO<sub>2</sub> substrates in a tube furnace using CVD.<sup>49</sup> They were able to grow the single crystal shell at 500 °C which is quite higher than the decomposition temperature of InAs NWs we have observed on SiO<sub>2</sub>. This is attributed to differences in sources where a hydride compound (AsH<sub>3</sub>) is used in our OMVPE case and a solid source of InAs powder maintained at 710 °C enabling efficient sublimation of In

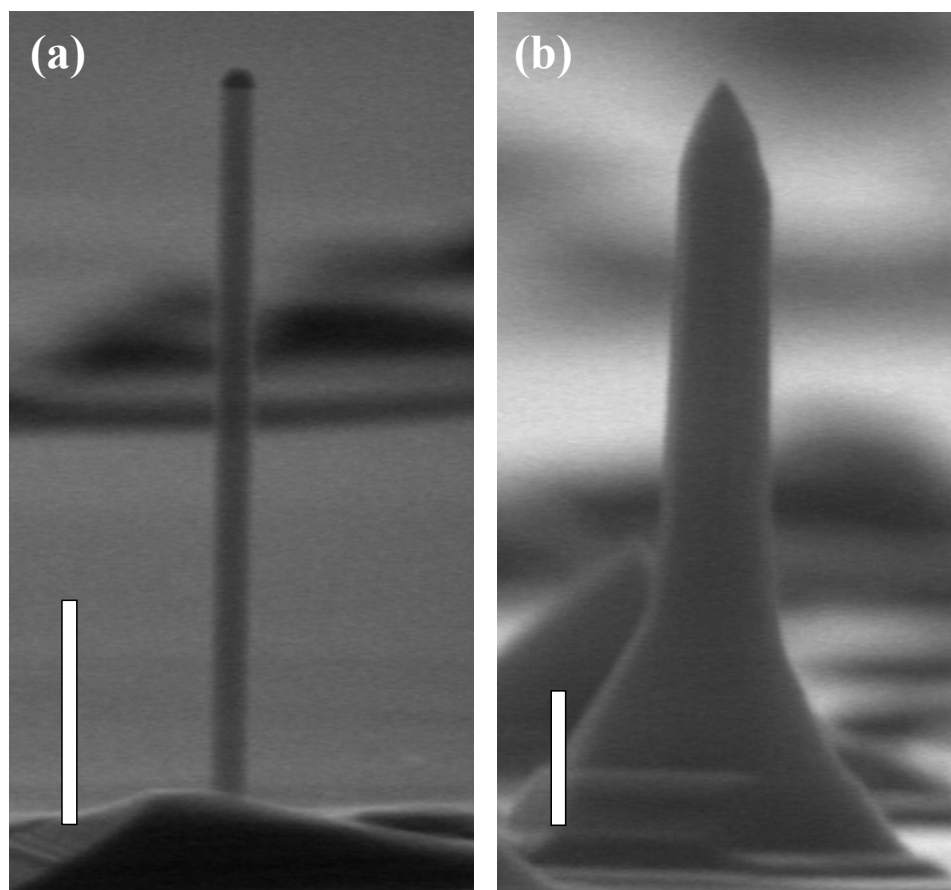


Figure 3.17. 88° angle view FE-SEM images of (a) InAs NW grown for 3 min at 500 °C and (b) InAs-InP core-shell NW grown for 3 – 10 min at 500 °C – 550 °C, respectively. Scale bars are 200 nm.

and  $As_x$  was used in their case. Jiang et al. have not discussed yield across the sample and shell morphology throughout a whole NW.<sup>49</sup> Li et al. have synthesized InAs-InP core-shell NWs on InP (111)B substrates using OMVPE to “remotely p-dope InAs NWs” with a p-type InP shell.<sup>52</sup> Their InAs core was grown at 420 °C whereas their InP shell was grown at 500 °C; temperature ramp-up was performed in  $AsH_3$  flow. Li et al. did not discuss the reason for using the InP (111)B substrates; At 500 °C, and in  $AsH_3$  overpressure, InAs NWs grown on InAs (111)B substrate would decompose as pointed

out earlier. Since adatom diffusion lengths and precursor pyrolysis are surface and orientation dependent,<sup>53</sup> this may lead to enhanced elemental As on the InP (111)B surface when compared to the InAs (111)B surface; more detailed investigation needs to be done in order to explain this behavior.

Since OMVPE growth of InP shells is feasible only at lower temperatures than those of InAs NW cores, single crystalline shells may not be achieved, as discussed above. Following Li et al., we have used InP (111)B substrates with 40 nm Au nanoparticles dispersed atop for our InAs-InP heterostructure studies. For the radial heterostructures, the growth of the InAs NW core is performed at 500 °C for 3 min (TMIn flow  $\sim 0.75$   $\mu\text{mol}/\text{min}$  and AsH<sub>3</sub> flow  $\sim 44.6$   $\mu\text{mol}/\text{min}$ ), after which the temperature is ramped up to 550 °C in AsH<sub>3</sub> flow. Figure 3.17 (a) shows an 88° angle view FE-SEM image of the InAs NW cores. InP shell deposition was performed for 10 min (TMIn flow  $\sim 0.75$   $\mu\text{mol}/\text{min}$  and PH<sub>3</sub> flow  $\sim 7143$   $\mu\text{mol}/\text{min}$ ) in an attempt to verify cessation of the axial NW growth and clear thickening of their diameters under SEM. Figure 3.17 (b) shows an 88° angle view FE-SEM image of the InAs-InP core-shell NWs. Energy dispersive x-ray analysis (EDX) using SEM with the NWs standing 90° with respect to the incident x-ray confirmed the presence of the InP shell around the InAs NW. The NWs did not seem to increase in length when the InP shell was deposited. Further high resolution and local EDX analysis using transmission electron microscopy is required to confirm axial growth cessation and only radial growth at the conditions specified above.

Material requirements and growth conditions for axial heterostructure NW growth are different from those of radial heterostructure NW growth. Dick et al. have performed



in 2007 extensive and detailed studies on the growth of several group IV and III-V NW axial heterostructures.<sup>54</sup> They experimentally verified that in axial heterostructure NW growth of material B on A, the sum of the interfacial energies of Au-B and A-B must be lower than that of Au-A in order for layer-by-layer growth and straight axial heterostructure NWs to be realized. About the same time, Paladugu et al. have reported similar studies and analysis on InAs-GaAs axial NW heterostructures.<sup>55</sup> For the InAs-InP axial NW heterostructures, InP on InAs NW growth results in straight NWs whereas InP on InAs NW growth results in kinked or straight NWs depending on the growth conditions.<sup>54</sup> We were able to grow InAs-InP axial NW heterostructures on InAs (111)B and InP (111)B substrates, both at 500 °C. For this, InAs NWs were first grown for 120 s on an InP (111)B substrate at conditions specified above (Figure 3.18 (a)), followed by 15 s purge in AsH<sub>3</sub> and 15 s purge in PH<sub>3</sub>. The InP section was grown after the InAs section, also for 120 s. Figure 3.18 (b) shows a 45° angle view FE-SEM image of the InAs-InP axial NW heterostructure where the total NW length is more than four times longer than that in Figure 3.18 (a). We found that InP in general has higher nucleation efficiency (could be nucleated from In droplets as demonstrated by Novotny and Yu)<sup>20</sup> and higher growth rate (at the same TMIn flow rates) when compared to InAs NWs. Slight tapering is observed at the base of the NW and the InP section is generally uniform. For shorter growth times and with growth conditions of Regime 1 in Figure 3.13, the whole axial NW heterostructure is uniform. However, EDX analysis in TEM is required to verify the axial heterostructure. We presented here the case of longer NWs in order to show that InP segment growth indeed occurs as can be inferred from the increase in the length of the NW in Figure 3.18 (b). STEM analysis on both radial and axial

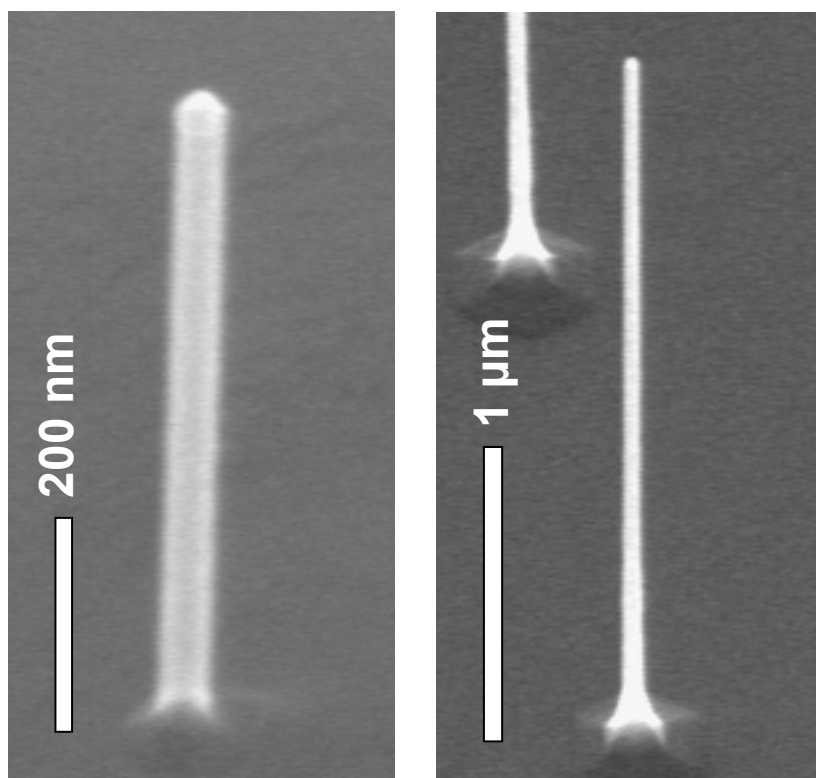


Figure 3.18. 45° angle view FE-SEM images of (a) InAs NW grown for 120 s at 500 °C and (b) InAs-InP axial NW heterostructure grown for 120 s – 120 s at 500 °C.

heterostructures are in progress at the time of writing this thesis.

#### 3.6.4 Summary

In this section, we considered material impingement and contribution to the NW growth from its tip, sidewalls, and growth substrate. Each of these contributions leads to a different time-dependent growth rate, namely linear for tip contribution, exponential followed by linear for NW sidewall contribution, and sub-linear followed by linear for substrate contribution. From time-dependent growth studies of InAs NWs grown on InAs

(111)B substrates at 2 different TMIn flow rates, we have experimentally distinguished, for the first time, between two NW growth regimes that are dependent on the NW-substrate adatom exchange. Uniform NW morphology is obtained only in regime 1 at low TMIn flow rates where no substrate to NW diffusion occurs and  $\lambda_{NW} > \lambda_{sub}$  such that the NW elongation is exponential for short growth times and becomes linear for  $t > \lambda_{NW}$ . This also allowed us to extract the surface diffusion length on the NW facets which we found to be  $\sim 1 \mu\text{m}$  at  $T = 500 \text{ }^\circ\text{C}$ . In regime 2 at high TMIn flow rates where substrate to NW adatom diffusion prevails, the InAs NWs become tapered and NW elongation proceeds sub-linear for short growth times followed by a linear increase for longer growth times. The diffusion model considered above was further validated by the diameter-dependent growth rates for InAs NWs where within regime 1, the NW length increases as the NW diameter decreases. Only for very short growth times, where NW nucleation is comparable to the experiment growth time, large diameter NWs are longer than those of small diameters. This understanding and control over the NW length have allowed us to grow axial and radial InAs-InP NW heterostructures and set the length limit over which these NWs and their heterostructures can be obtained with uniform morphology.

### **3.7 Crystal Structure of InAs Nanowires grown on InAs (111)B Substrates**

Most III-V materials crystallize in the zinc blende crystal structure. However, III-V NWs often show zinc blende (ZB) / wurtzite (WZ) polymorphism under different growth conditions and techniques, which has direct consequences on their electronic and

optical properties. Such polymorphism was observed in our InAs NWs grown on InAs (111)B substrates, whose structural properties will be discussed in this section.

Takahashi's and Muriizumi's XRD analysis on CVD grown InAs whiskers (at 400 °C) have shown that these whiskers exhibit the WZ crystal structure, which converts fully to ZB when annealed at 800 °C.<sup>2</sup> Koguchi et al.<sup>3</sup> and Yazawa et al.<sup>4</sup> have shown through cross-sectional TEM, XRD, and high resolution TEM studies that InAs NWs grown at temperatures greater than 400 °C assume the WZ crystal structure with numerous planar defects perpendicular to their growth direction. Their results were summarized and reviewed by Hiruma et al. in 1995.<sup>56</sup> Similar trends were also observed for other III-V NWs such as GaAs<sup>2,4,56,57</sup>, GaP and their heterostructures.<sup>58</sup> These NWs generally grow in the <0001> direction, equivalent to <111> ZB (independent of the growth substrate orientation in most cases). This is the case because the surface free energy of the (111) plane is the lowest among all other planes in the lattice.<sup>59</sup> ZB and WZ crystals are based on face-centered cubic and hexagonal close-packed, respectively, and both are most densely packed with very similar bond lengths and system energies.<sup>60</sup> Twinning in their bulk or nanostructure forms is thus possible. A simple rotation of the third nearest neighbors in the (111) planes by a quarter of the body diagonal of ZB crystal with ABCA layer stacking (Figure 3.19 (a)) leads to ABAB layer stacking and to the formation of WZ InAs (Figure 3.19 (b)).

Hurle have successfully modeled in 1995 the formation of twinned bulk III-V compound semiconductor crystals grown through the Czochralski technique.<sup>59</sup> According to Hurle, the formation of a twin necessitates the presence of a triple phase boundary at an edge facet, a specific contact angle, and supercooling at an edge facet exceeding a

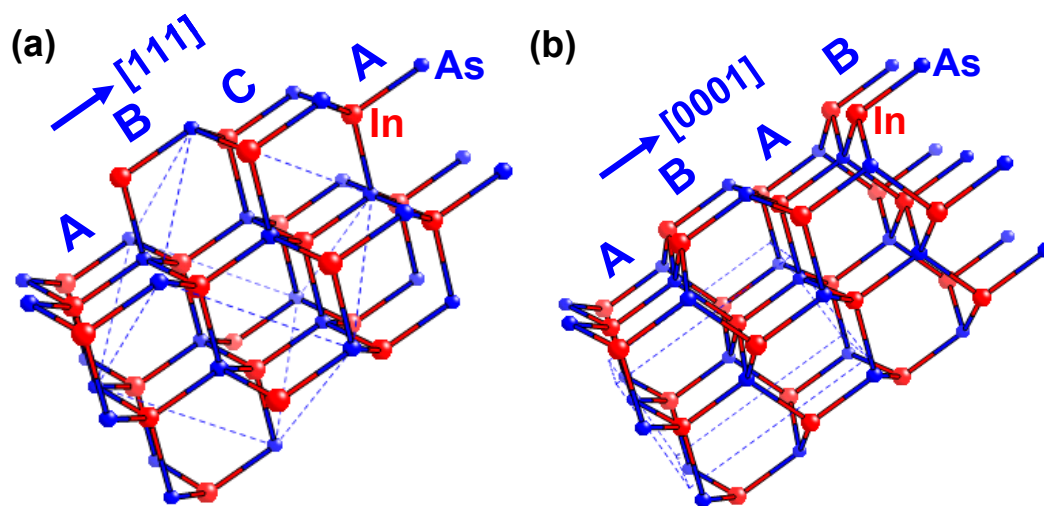
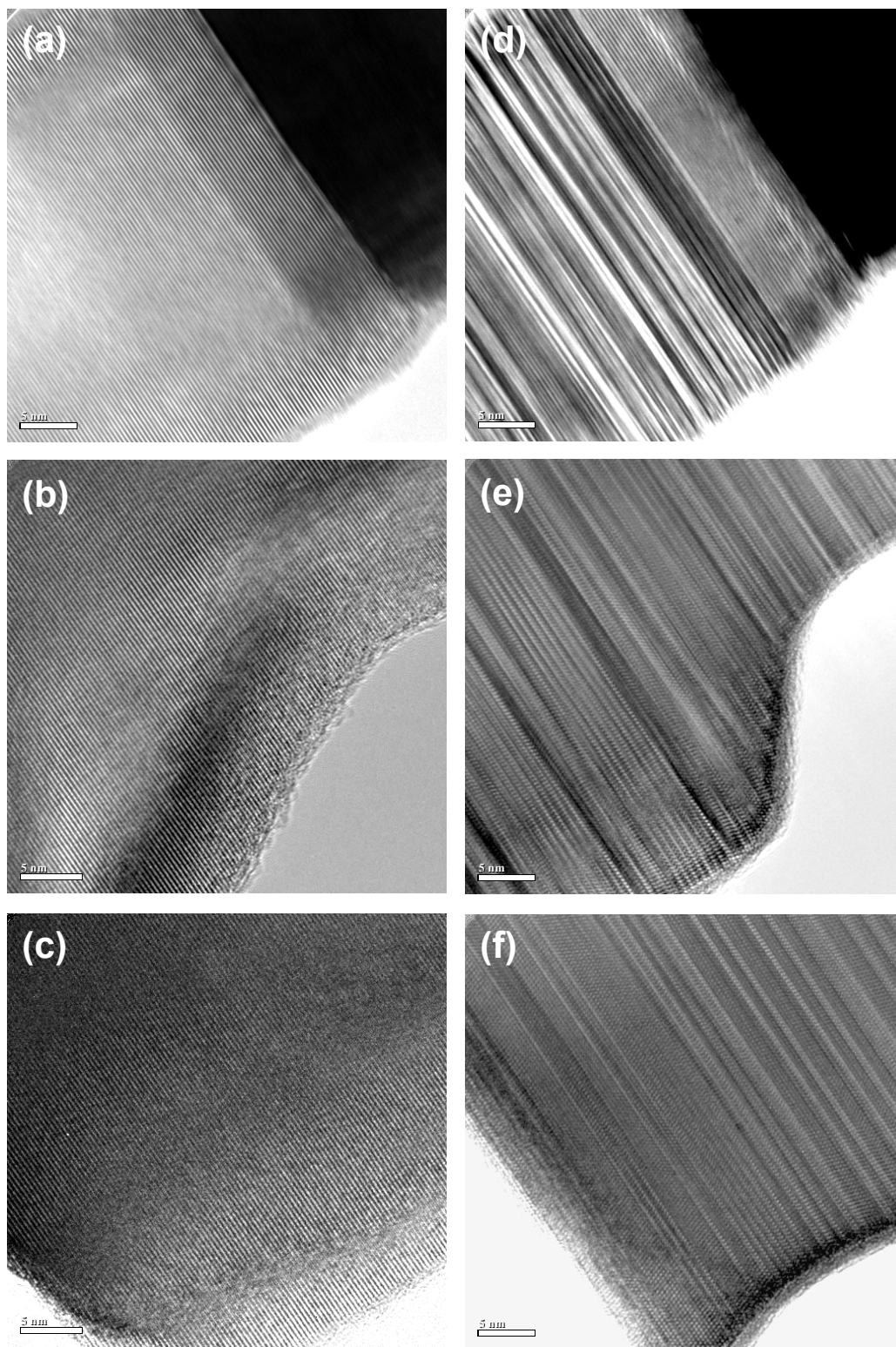


Figure 3.19. (a) Schematic of the WZ crystal structure with ABAB layer stacking along the  $[0001]$  direction and (b) Schematic of the ZB crystal structure with ABCA layer stacking along the  $[111]$  direction.

certain value.<sup>59</sup> Very interestingly, he also pointed out that fluctuations in the contact angle (due to growth condition variations such as temperature changes) may lead to twinning. Glas et al. in 2007 have suggested that the surface energies of the NW facets may lead to preferential nucleation at triple phase interfaces rather than at the liquid-solid interface.<sup>61</sup> Lower WZ facet energies and high nanoparticle supersaturations would then favor the formation of WZ NWs for III-V semiconductors. In general, it was found experimentally that for a growth temperature of 350 °C or less, ZB InAs NWs are crystallized,<sup>3,35,62</sup> whereas growth temperatures of 390 °C or above, WZ InAs NWs with stacking faults and small ZB segments.<sup>2-4,63,64</sup>

Twinning may be clearly identified under TEM, however, at only certain pole axes. Figure 3.20 shows HR-TEM images of an InAs NW taken at its tip, center, and bottom. In Figure 3.20 (a) – (c), where the NW is imaged from the  $[0\bar{1}10]$  pole

Figure 3.20. HR-TEM images of an InAs NW at (a) its tip, (b) middle, and (c) base, all taken at a pole orientation of  $[0\bar{1}10]$ . (d) – (f) HR-TEM images of the same NW sections in (a) – (c), respectively, taken at a pole axis of  $[2\bar{1}\bar{1}0]$  where stacking faults are visible.



orientation, the atomic planes across the whole NW are aligned such that the NW appears to be defect free. In Figure 3.20 (d) – (f), where the NW is imaged from the  $[2\bar{1}\bar{1}0]$  pole axis, difference in layer stacking between WZ and ZB can be identified such that twin planes are visible. The density of these twin planes did not seem to vary from the tip of the NW toward its base. Moreover, their density also seems to be independent of the growth temperature (450 °C - 500 °C) or V/III ratio (20 - 60), and consequently with NW diameter and morphology.

Figure 3.21 (a) shows a HRTEM image of another InAs NW whose diffraction pattern (Figure 3.21 (b)) indicates a WZ crystal structure with  $[0002]$  growth orientation. This mostly WZ NW have small ZB segments (one larger section is labeled) in addition to the presence of stacking faults perpendicular to the growth-direction axis as well as twin boundaries separating small ZB sections. Typical density of ZB structure in the WZ InAs NW is  $\sim 10 - 15\%$ . We will show in chapter 8 that these alterations of WZ/ZB segments have significant consequences on the performance of field-effect transistor devices fabricated from this type of NWs.

To summarize this section, InAs NWs grown on InAs (111)B substrates exhibit WZ crystal structure with  $[0001]$  growth orientation. This type of NWs contains a large density of planar defects that are only visible when the NW is aligned at a certain pole axis under the electron beam in TEM. These defects are identified to be twinning defects due to alterations from WZ InAs to ZB InAs, where small segments of the latter can be clearly visible under TEM. Obtaining a single crystal InAs NW on an InAs (111)B substrate remains a challenge at the time of writing this thesis.



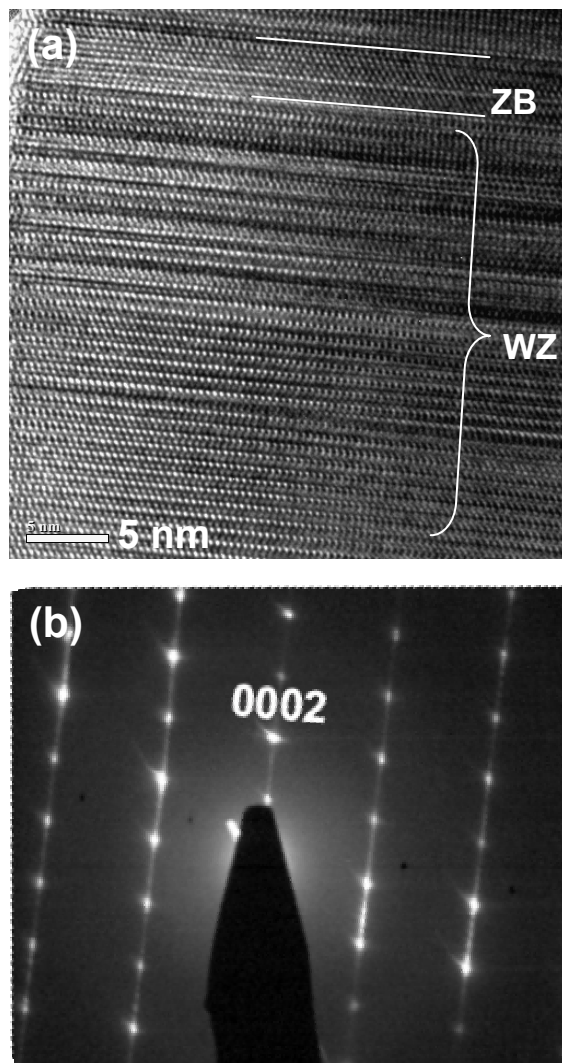


Figure 3.21. (a) HR-TEM image showing lattice fringes of an InAs NW grown on InAs (111) B substrate where stacking faults are clearly visible and a small ZB segment is highlighted by 2 white lines. (b) Diffraction pattern for NW in (a) indicating WZ crystal structure with [0002] growth orientation.

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## 4. TOP GATE INDIUM ARSENIDE NANOWIRE FIELD EFFECT TRANSISTORS: FABRICATION, CHARACTERIZATION AND MODEL FOR PARAMETER EXTRACTION

### 4.1 Introduction

Semiconductor nanowires (NWs) are very attractive and versatile building blocks for future electronic systems because of the unique possibilities they offer for rational control of fundamental properties such as dimension, composition, and doping during growth.<sup>1,2</sup> A wide range of NW based devices and systems, including transistors and circuits,<sup>3,4,5</sup> light emitters,<sup>6,7,8,9</sup> and sensors<sup>10</sup> have been explored. NW field-effect transistors (NWFETs) have been of particular interest recently both as vehicles for investigation of basic carrier transport behavior and as potential future high-performance electronic devices. NWFETs fabricated from group IV,<sup>11,12,13</sup> III-V,<sup>3,14,15,16</sup> and II-VI<sup>17,18</sup> semiconductors and conductive oxide<sup>19</sup> have demonstrated promising FET characteristics in top-gate,<sup>11,12,15</sup> back-gate,<sup>3,14,15</sup> and surround-gate<sup>16,18</sup> FET geometries. InAs in particular is an attractive candidate for NW-based electronic devices because of its very high electron mobility at room temperature<sup>20</sup> and its surface Fermi level pinning in the conduction band<sup>21</sup> that lead to the formation of an electron surface accumulation layer<sup>22</sup> and allowing straightforward formation of low resistance ohmic contacts.<sup>23</sup> Indeed, resonant tunneling diodes,<sup>24</sup> single electron transistors,<sup>25</sup> and Josephson junctions<sup>26</sup> have been implemented using InAs NWs and InAs/InP NW heterostructures with carrier mobilities in the range of 200 – 3000 cm<sup>2</sup>/V·s.<sup>16,26</sup> In all these studies, NW transport coefficients are extracted directly from the extrinsic measured output and transfer curves

without taking into account the parasitic resistances and capacitances of the NWFET device. In this chapter, we discuss the fabrication and characterization of back- and top-gate InAs NWFETs and develop a model that allows accurate parameter extraction from such devices.

## 4.2 Summary of Results

We have studied the room temperature characteristics of depletion mode InAs-based NWFETs with both global back-gate and underlap (i.e. non-zero spacing to source/drain electrodes) top-gate geometries. To assure accurate parameter extraction for such structures from device measurements, we have developed a circuit model for top-gate FETs that takes into account the contact, series, and leakage resistances, interface state capacitance, and top-gate geometry-defined capacitance. We have analyzed the InAs NWFET's using this new device model and the conventional back-gate NWFET model. Both the back-gate and the top-gate NWFETs exhibit room-temperature field-effect mobility as high as  $6580 \text{ cm}^2/\text{V}\cdot\text{s}$ , which is the lower bound value without interface state capacitance correction, and exceeds mobility values reported to date in any homogenous semiconductor NW.

## 4.3 Experiment

The InAs NWs were grown in a horizontal growth tube on  $600 \text{ nm SiO}_2/\text{n}^+\text{-Si}$  substrates by organo-metallic vapor phase epitaxy.  $40 \text{ nm}$  – diameter Au colloids (Ted



Pella) were dispersed from solution on cleaned substrates pre-treated with Poly-L-Lysine. The substrates were then loaded into the growth chamber and the temperature was ramped to the final growth temperature (350 °C) in H<sub>2</sub> ambient. 148 μmol/min Arsine (10 % AsH<sub>3</sub> in H<sub>2</sub>) and 6 μmol/min Tri-methyl-Indium (TMIn) precursors were then introduced in 1.2 slm H<sub>2</sub> carrier gas with an input V/III ratio of 25 and a chamber pressure maintained at 100 Torr. The samples were then cooled down to room temperature in AsH<sub>3</sub> ambient. The InAs NWs are 30 – 75 nm in diameter and 20 – 30 μm long for 15 minutes of growth time, making them suitable for FET fabrication.

The grown NWs were then sonicated in ethanol solution for 7 seconds to suspend the NWs in the solution and were then transferred to a 600 nm SiO<sub>2</sub>/n<sup>+</sup>Si substrate with a pre-patterned indexed grid with alignment marks. Optical microscopy was used to determine the locations of the randomly dispersed NWs on this grid structure. Patterning of contacts by electron beam lithography followed by 15 nm/85 nm Ti/Al metallization and a standard liftoff process were used to create ohmic contacts to the NWs. Gate pattern definition by e-beam lithography, sputtering of 100 nm/100nm SiO<sub>2</sub>/Au, and subsequent liftoff were used to form top-gate structures. Current – voltage characteristics were then obtained with an HP 4155 semiconductor parameter analyzer in air at room temperature. The device dimensions were measured after electrical measurements under the highest attainable magnification using a FEI XL 30 Environmental Scanning Electron Microscope (ESEM) operating at 10 KV acceleration voltage.

#### 4.4 Model for Parameter Extraction

Figure 4.1 (a) shows the schematic of an underlap top-gate NWFET device. Careful consideration of the device geometry of this structure suggests the need for an analysis that extends beyond those employed previously<sup>3,12-14,16,18</sup> in order to extract key characteristic NW parameters such as mobility and carrier concentration. Specifically, we have taken into account the contact resistance, the resistance of the ungated NW regions between source/drain and gate electrodes, and the unmodulated NW volume underneath the gate, which are important factors that had not been accounted for in any prior reported studies. Because the Fermi level is pinned in the conduction band at the InAs surface, the ungated portions of the NW remain conducting with no band-bending under top-gate bias, as illustrated in Figure 4.1 (b); the resistance of each NW section should therefore be calculated separately to analyze device current-voltage characteristics. Thus, we define two series resistances  $R_{s1}$  and  $R_{s2}$ , each of which includes the contact resistance and the resistance of the corresponding ungated NW segments. The unmodulated portion of the NW underneath the gate gives rise to a current leakage path that is constant for a wide range of negative gate voltages, and can be described by a leakage resistance,  $R_{leak}$ , which can be obtained from the lowest measured current in the device,  $I_{leak}$ . The gate leakage current through the thick oxide is negligible so that the gate leakage resistance is not included in this model. Figure 4.1 (c) shows the resulting equivalent circuit model employed in our analysis.  $V_{DS}^0$  and  $V_{GS}^0$  are the applied source-drain and gate-source voltages, respectively, and  $I_{DS}^0$  is the measured source-drain current.  $V_{DS}$ ,  $V_{GS}$ , and  $I_{DS}$  are related to the active transistor portion of the device.

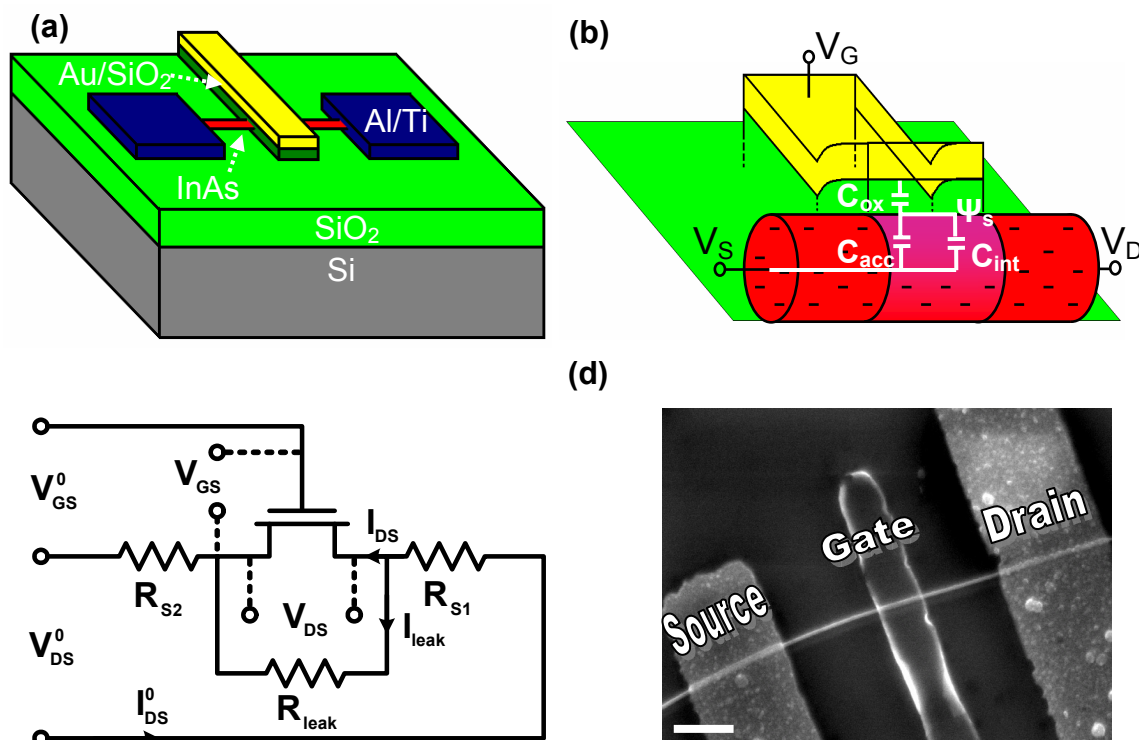


Figure 4.1. (a) Schematic of the underlap NWFET fabricated on oxidized Si substrate, with 85 nm/15 nm Al/Ti as source and drain contacts and 100 nm/100 nm Au/SiO<sub>x</sub> as the top-gate electrode and dielectric. (b) Schematic of the underlap top-gate NWFET and its equivalent capacitance circuit. (c) DC circuit model for the underlap top-gate NWFETs. (d) An SEM image showing the “ungated” regions between the source and the drain, that contribute to series resistances. Scale bar is 1  $\mu\text{m}$ .

The contact resistance for the Al/Ti contact to the InAs NWs has been measured through the transmission line measurement (TLM) technique. The separation of the Al/Ti electrodes patterned on the InAs NWs was varied between 0.5 – 4  $\mu\text{m}$ . The electrode patterning and Ti/Al deposition by e-beam evaporation were performed together for the devices used in the TLM-type measurements and for the source-drain fabrication for the NWFETs to assure the same processing conditions. For each channel length, resistance measurements for 2-5 devices were performed to yield the data shown in Figure 4.2.

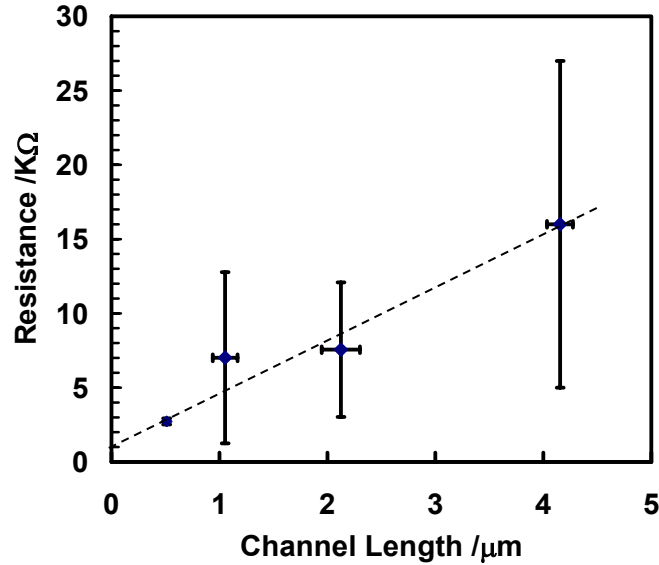


Figure 4.2. Transmission Line Measurement (TLM) for calculation of the contact resistance of  $\sim 1 \text{ K}\Omega$ .

Extrapolation of the measured resistance versus electrode separation to zero electrode separation results in a contact resistance of  $1 \text{ K}\Omega$  as shown in Figure 4.2.

As a conservative estimate for mobility computation, a contact resistance of  $1 \text{ K}\Omega$  has been used; this assumes the highest possible NW resistance values. Numerical calculation to determine the number of confined modes in the InAs NWs by solving Schrödinger's equation in cylindrical coordinates<sup>27</sup> yields occupation of  $\sim 10$  modes for the carrier densities calculated in these wires, as discussed later, which in turn results in a contact resistance of  $1.3 \text{ K}\Omega$  due to the mismatch in the 1D (NW) and 3D (metal contact) densities of states.<sup>28</sup> This result suggests, as expected, the absence of a significant Schottky barrier at the Al-Ti/InAs interface.

In the linear operating region,<sup>20</sup> the accumulation charge is given by  $Q_{acc} = C(V_{GS} - V_t)$ , where  $C$  is the gate capacitance and  $V_t$  is the threshold voltage. The source-drain current,  $I_{DS}$ , can then be derived as

$$I_{DS} = \int qnvdA = \mu_{FE} Q_{acc} V_{DS} / L_G^2 = \mu_{FE} C (V_{GS} - V_t) V_{DS} / L_G^2, \quad (4.1)$$

where  $q$  is the electron charge,  $n$  is the electron concentration,  $v$  is the drift velocity,  $\mu_{FE}$  is the field-effect mobility and  $L_G$  is the gate length. Ballistic effects are expected to be negligible for the NW lengths we report in this paper: numerical computations indicate a mean free path of  $\sim 50$  nm and Scanning Probe Microscopy (SPM) measurements on NWs grown and fabricated together with the devices we discuss here have demonstrated ballistic or nearly ballistic transport only over distances of up to 200 nm, much shorter than the gate lengths employed here.<sup>27,29</sup>

The gate capacitance,  $C$ , is critical in obtaining the field-effect mobility. The dielectric capacitance for a top-gate NWFET is difficult to determine precisely because of the curved gate geometry and the dependence of the curvature on the oxide thickness, and the wire-to-plate capacitance model used for back-gate NWFETs is not applicable. For back-gated NWFETs and nanotube FETs, the general form of capacitance is

$$C = 2\pi\epsilon L_G / \ln\left(\left(t_{ox} + a + \sqrt{(t_{ox} + a)^2 - a^2}\right) / a\right), \quad (4.2)$$

where  $L_G$  is the gate length,  $\epsilon$  is the insulator dielectric constant,  $t_{ox}$  is the gate insulator thickness, and  $a$  is the NW radius; this can be reduced to  $C = 2\pi\epsilon L_G / \ln\left(\frac{2t_{ox}}{a}\right)$ , when  $t_{ox} \gg a$ . These equations are applicable for degenerately doped NWs and have been used extensively elsewhere. For top-gated NWFETs employed in our work, we have used a 2D device simulator<sup>30</sup> to compute the capacitance between the metal gate and the InAs NW, and we find that the capacitance calculated using equation is underestimated by  $\sim 10 - 14$  % when compared to the numerically computed capacitance; for 100 nm oxide thickness

used in our devices, the error in using equation (2) or its approximation is  $\sim 13\%$ . Note that the  $\text{SiO}_x$  dielectric layer was sputtered on a rotating stage at 60 rpm and uniform coverage along the circumference of the NW was used in the simulation. Use of the wire-to-plate capacitance model would therefore lead to an overestimate by  $\sim 10 - 14\%$  compared to the values we have calculated using the numerically simulated capacitance of  $\mu_{FE}$ .

An additional contribution to  $C$  can arise due to the unavoidable presence of surface states in InAs.<sup>31</sup> To take surface and interface states into account, we introduce – in analogy to a conventional MOSFET<sup>32</sup> – an interface capacitance,  $C_{int}$ , in parallel with the accumulation capacitance,  $C_{acc}$ , for the depletion mode InAs NWFET, as shown in Figure 4.1 (b). The modulated electron charge density will then be:

$$\Delta Q_{acc}/A = \Delta \Psi_s C_{acc} = \Delta V_{GS} C_{ox} / (1 + C_{int}/C_{acc} + C_{ox}/C_{acc}) \quad (4.3)$$

where  $\Psi_s$  is the surface potential at the InAs/ $\text{SiO}_2$  interface with area  $A$  and all capacitances are in  $\text{F}/\text{cm}^2$ .  $C_{ox}/C_{acc} = (\epsilon_{ox}/\epsilon_{InAs})(t_{acc}/t_{ox})$  is negligible in the planar approximation due to the dielectric constant difference and the large oxide thickness:  $\epsilon_{ox}=3.31$  was determined experimentally for a sputtered  $\text{SiO}_2$  layer from the same target,  $\epsilon_{InAs}=15.1$ ;  $t_{acc}$  and  $t_{ox}=100$  nm are the accumulation layer and oxide thicknesses, respectively, with  $t_{acc} \ll t_{ox}$ . The accumulation capacitance can be expressed as  $C_{acc} = Q_{acc}/bV_T$  where  $b=2$  for planar enhancement-mode MOSFETs,<sup>32</sup> and can be approximated as  $C_{acc} = \epsilon_{InAs}/t_{acc}$  where  $t_{acc}$  is the separation of the accumulation charges from the surface of the NW due to quantum-mechanical confinement. The interface state capacitance can be expressed as  $C_{int} = qD_{it}$  where  $D_{it}$  is the interface state density in units

of  $\text{cm}^{-2}\cdot\text{eV}^{-1}$ , distributed over an energy range within the energy bandgap and in the conduction band of InAs.<sup>33</sup> The interface state density and its energy distribution have not been studied yet for NWs in general, and for InAs NWs in particular. If a surface state density of  $5 \times 10^{12} \text{ cm}^{-2}\cdot\text{eV}^{-1}$  (eg.  $10^{12} \text{ cm}^{-2}$  for an energy range of 0.2 eV), and even a very small  $t_{acc}$  of 3 nm are assumed, then  $C_{int}/C_{acc} = 0.2$ . Thus, the term  $C_{int}/C_{acc}$  may not be negligible and has to be taken into account for accurate NW field-effect mobility calculations. However, the mobility values reported in this paper do not take into account the interface charge capacitance correction and are thus the lower bound mobility values.

Straightforward circuit analysis is employed in Figure 4.1 (c) to relate the quantities appearing in equation (4.1) to the quantities applied at the physical electrodes of the NW device. Using the accumulation capacitance from equation (4.3), a field effect mobility equation can then be derived from equation (4.1) as

$$\mu_{FE} = \frac{L_G^2 V_{DS}^0 (1 + C_{int}/C_{acc})/C}{\left[ (V_{DS}^0 - I_{DS}^0 R_s)^2 / g_m^0 - (I_{DS}^0)^2 R_s^2 R_{s2} - V_{DS}^0 R_{s2} (V_{DS}^0 - 2I_{DS}^0 R_s) \right]} \quad (4.4)$$

where  $g_m^0 = \partial I_{DS}^0 / \partial V_{GS}^0$  is the extrinsic transconductance. If the series resistances and effects of interface states are neglected, equation (4.4) simplifies to

$$\mu_{FE} = g_m^0 L_G^2 / C V_{DS} \quad (4.5)$$

which is the usual expression employed to determine carrier mobility in NWs.

#### 4.5 Results and Discussion

Representative  $I_{DS}^0$  vs.  $V_{DS}^0$  plots are shown in Figure 4.3 (a) for gate voltages  $V_{GS}^0 = -2, 0, +2\text{V}$ , revealing that the InAs nanowires are highly conductive with low ohmic contact resistance. The extrinsic transconductance  $g_m^0$  obtained from the slope of  $I_{DS}^0$  vs.  $V_{GS}^0$  in the linear region (Figure 4.3(b)) is  $3\mu\text{S}$ , from which the field-effect mobility can be calculated using equation (4.4) to be  $6580\text{ cm}^2/\text{V}\cdot\text{s}$  - the highest room temperature field-effect mobility reported to date in any elemental or compound semiconductor NWFET. It should be noted that these NWFET devices exhibit hysteresis in their  $I_{ds}$ - $V_{gs}$  characteristics (Figure 4.3 (b)) that could alter the obtained extrinsic transconductance by a considerable amount (6 to 50 %). We have used the lowest obtained transconductance in the mobility values reported in this paper. A detailed analysis of the hysteresis and measurement time delay effects will be discussed in detail in chapter 5.

One can also extract the current voltage characteristics  $I_{DS} - V_{GS}$  intrinsic to the InAs NWFET device using circuit analysis in Figure 4.1 (c). This is shown in Figures 4.3 (c) and 4.3 (d) with the applied voltages corresponding to those in Figures 4.3 (a) and 4.3 (b). The potential drop across the series resistances lowers  $V_{DS}$  across the active portion of the NWFET device. As the source-drain current  $I_{DS}$  increases with applied  $V_{GS}^0$ , the measured current  $I_{DS}^0$  increases, causing more potential drop across the series resistances. Hence,  $V_{DS}$  decreases with increasing  $V_{GS}^0$ , unlike the fixed  $V_{DS}^0$  applied to the physical electrodes of the device, causing a decrease in  $I_{leak}$ . The intrinsic transconductance can be calculated to be  $g_m = \partial I_{DS} / \partial V_{GS} = 7.7\mu\text{S}$ . The differential transconductance can be



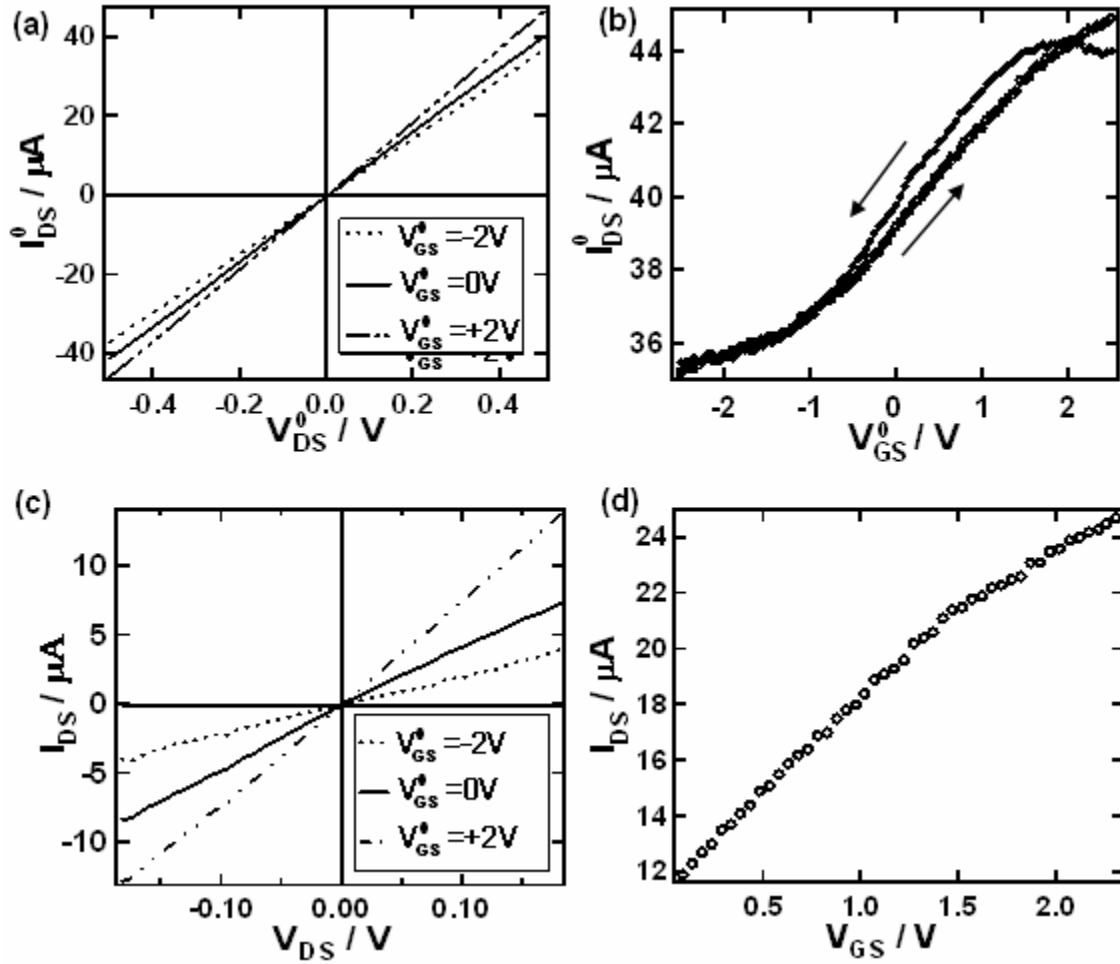


Figure 4.3. (a)  $I_{DS}^0$  vs.  $V_{DS}^0$  for  $V_{GS}^0 = -2\text{V}$ ,  $0\text{V}$ ,  $+2\text{V}$  of a representative top-gate InAs NWFET. (b)  $I_{DS}^0$  vs.  $V_{GS}^0$  at  $V_{DS}^0 = 0.5\text{V}$  of the same InAs NWFET. The arrows indicate the direction of the gate sweep with sweeping rate of  $2.7\text{V/s}$ . (c)  $I_{DS}$  vs.  $V_{DS}$  for the active portion of the NWFET device extracted from (a). (d)  $I_{DS}$  vs.  $V_{GS}$  for top-gate NWFET, extracted at  $V_{DS}^0 = 0.5\text{V}$  for the same device. Device dimensions correspond to device F in Table 4.1.

incorporated along with  $V_{DS}$  into  $\mu_{FE} = g_m L_G^2 / CV_{DS}$  to yield mobility values of 4320-8160  $\text{cm}^2/\text{V}\cdot\text{s}$  for the same device discussed above. These mobility values extracted using this conventional technique are quite consistent with those extracted using equation (4.4).

Table 4.1. Summary of some representative InAs NWFET parameters and calculated field effect mobility.

<b>NWFET</b>	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>E</b>	<b>F</b>	<b>G</b>
<b>D (nm)</b>	73	49	74	63	65	68	47
<b>L<sub>SD</sub> (μm)</b>	3.87	3.72	3.72	3.66	3.41	3.48	3.64
<b>L<sub>G</sub> (μm)</b>	1.62	1.69	1.42	1.52	1.45	1.3	1.61
<b>L<sub>SG</sub> (μm)</b>	1.75	0.986	1.07	1.15	1.21	1.04	1.25
<b>R<sub>T</sub> (KΩ)</b>	21.9	20.9	12.6	11.9	16	13.2	25.5
<b>R<sub>s</sub> (KΩ)</b>	13.14	11.9	8.15	7.36	9.64	8.63	14.6
<b>R<sub>s2</sub> (KΩ)</b>	9.93	5.78	3.81	3.9	5.85	4.31	8.87
<b>g<sub>m</sub> (μS)</b>	1.18	9.06	1.93	1.67	0.88	3.04	1.88
<b>I<sub>meas</sub> (μA)</b>	22.8	23.9	39.7	42.4	31.2	38	19.6
<b>C<sup>‡</sup> (fF)</b>	0.149	0.134	0.132	0.132	0.128	0.116	0.127
<b>C* (fF)</b>	0.174	0.154	0.153	0.154	0.147	0.133	0.145
<b>μ<sup>‡</sup> (cm<sup>2</sup>/V·s)</b>	2630	2070	4800	4070	1830	7500	4320
<b>μ* (cm<sup>2</sup>/V·s)</b>	2260	1800	4160	3500	1590	6580	3770

Table 4.1 summarizes the extracted field-effect mobilities of seven representative devices, where the NW diameters ( $D$ ), source-drain lengths ( $L_{SD}$ ), gate lengths ( $L_G$ ), and gate-source lengths ( $L_{SG}$ ) were measured using SEM.  $R_T$  is the total device resistance and is equal to the sum of the NW resistance ( $R_{NW}$ ) and the contact resistance ( $R_c$ ).  $R_s$  is the total series resistance and be calculated using  $R_s = (R_T - R_c)(L_{SD} - L_G) / L + R_c$ ,  $R_{s2}$  is the source series resistance and can be calculated using  $R_{s2} = (R_s - R_c)L_{SG} / (L - L_G) + R_c/2$ ,  $I_{meas}$  is the measured current at  $V_{DS}^0 = 0.5$  V,  $C^{\ddagger}$  is the capacitance calculated using equation (4.2),  $\mu^{\ddagger}$  is the mobility calculated using  $C^{\ddagger}$  and equation (4.4),  $C^*$  is the numerically computed capacitance using Silvaco and  $\mu^*$  is the mobility calculated using  $C^*$  and equation (4). The field-effect mobility in these InAs nanowires is much lower than the bulk InAs mobility (33000 cm<sup>2</sup>/V·s) due to surface scattering, but higher than that typically measured for the accumulated free electron gas on the InAs surface (2000 – 3000 cm<sup>2</sup>/V·s).<sup>34,35</sup> Such an intermediate value is expected, given the combination of surface and bulk electron transport likely to be present in these NWs. We anticipate that

Table 4.2. Comparison of different semiconductor NWFETs (non-passivated nanowires).

NW	Carrier	$\mu(\text{cm}^2/\text{V}\cdot\text{s})$	$n(\text{cm}^{-3})$	$J_{DS}^* (\text{A}/\text{cm}^2)$	$I_{on}/I_{off}$	Ref.
Ge	h	600	$3 \times 10^{18}$	$\sim 10^4$	$10^3$	11
Si	h	560		$1.41 \times 10^5$	$10^4$	13
GaN	e	650	$10^{18} - 10^{19}$	$2.88 \times 10^5$		14
ZnO	e	$13 \pm 5$	$5 \times 10^{17}$	$3.74 \times 10^3$	$10^5 - 10^7$	16
InAs	e	6580	$10^{17} - 10^{18}$	$10^6 - 10^7$	2 – 100	This work

[\*At  $V_{DS}=0.5\text{V}$  and  $V_{GS}=0\text{V}$  or the maximum available values.]

carrier mobility can be increased by surface passivation<sup>36</sup> or in heterostructure core-shell NWs. Table 4.1 also lists the mobilities calculated using the capacitance given by the wire-to-plate model, which quantifies the discrepancy compared to those obtained using the numerical simulated capacitance.

The modulated carrier concentration in the NWFET channel underneath the gate can be calculated from equation (1), and is given by

$$\Delta n_{channel} = \frac{I_{DS} L_G}{q \mu_{FE} V_{DS} A} \quad (3.6)$$

The typical calculated  $\Delta n_{channel}$  values are  $\sim 10^{17} - 10^{18} \text{ cm}^{-3}$  with a leakage carrier concentration  $n_{leak} \sim 10^{16} - 10^{17} \text{ cm}^{-3}$ . The entire carrier concentration  $n$  is expected to be the sum of these two quantities.

Finally, we also fabricated back-gate InAs NWFETs and performed back-gate measurements (Figure 4.4) to compare our top-gate model with the back-gate model and to enable a fair comparison of our results with carrier mobilities reported in other NW studies. A field-effect mobility  $\mu_{FE} = 2740 \text{ cm}^2/\text{V}\cdot\text{s}$  was obtained using equation (4.5) and the wire-to-plate capacitance model, corresponding to a transconductance of  $2 \mu\text{S}$ . This value is significantly higher than the mobility values reported for other NWs listed in

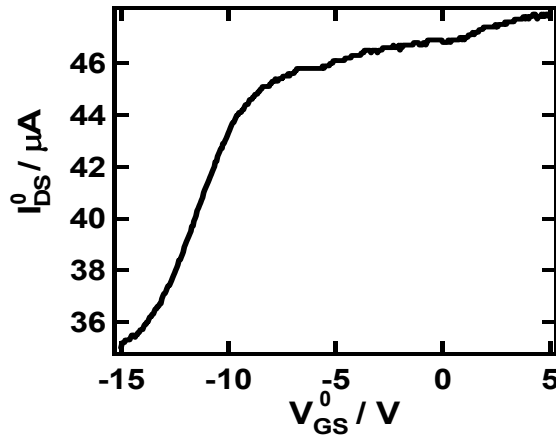


Figure 4.4. Back gate  $I_{DS}-V_{GS}$  at  $V_{DS}=0.5$  V for same device of Figure 4.3.

table 4.2 and is comparable to that of the free electron gas on the InAs surface, suggesting an increased influence of surface states due to poor physical contact between the nanowire and the  $\text{SiO}_2$  substrate compared to the top-gate NWFETs, and substantial gate coupling to the source and drain electrodes.

#### 4.6 Conclusion

In summary, we have fabricated and characterized underlap top-gate and global back-gate InAs NWFETs, and demonstrated the highest semiconductor NW electron mobility reported to date. For top-gate NWFET's, we have developed a model that allows more accurate estimation of field-effect mobility and carrier concentration in semiconductor NWs by taking into account series and leakage resistances, interface state capacitance, and top-gate geometry for oxide capacitance calculation. In particular, we have derived a new mobility equation for the analysis of the underlap gate NWFET

device structure. A peak mobility value of  $6580 \text{ cm}^2/\text{V}\cdot\text{s}$  at low drift fields of  $\sim 1.5 \text{ KV/cm}$  was measured in a top-gate InAs NWFET, and measurements on several devices yield a representative average mobility value of  $\sim 3400 \text{ cm}^2/\text{V}\cdot\text{s}$ . Both values represent lower bounds on the calculated mobility, which are conservative estimates because (1) we have used the lowest possible ohmic contact resistance, (2) the lower extracted transconductance from the hysteretic NWFET measurements was employed for mobility calculation and (3) the effect of surface states has not been taken into account. These results demonstrate the promising potential of using InAs nanowires for high-speed nanoelectronics.

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## 5. IMPACT OF SURFACE STATES ON TRANSPORT PROPERTIES AND PARAMETER EXTRACTION FORM INDIUM ARSENIDE NANOWIRE FIELD EFFECT TRANSISTORS

### 5.1 Introduction

Because of the high surface area to volume ratio in nanoscale devices, surface effects become important, and even dominant, in their influence on electronic transport<sup>1</sup> and optical behavior.<sup>2</sup> While these effects can be desirable in some applications such as highly sensitive photodetectors<sup>3</sup> or chemical and biological sensors,<sup>4</sup> they may be detrimental to carrier transport properties in nanowire field-effect transistors (NWFETs).<sup>5</sup> In order to obtain accurate and representative measures of transport properties in NWFETs, the capacitive effects of interface states must be considered. While traditional capacitance-voltage ( $C$ - $V$ ) measurements can offer detailed information concerning the presence, nature and density of interface trap states,<sup>6</sup> these techniques are not readily applicable to NWFETs due to their small gate capacitance. Our efforts focus on InAs NWFETs, which are promising for high speed nanoelectronics due to their high electron mobility and ability to form low resistance ohmic contacts<sup>1</sup> ( $\sim 1 - 10 \text{ K}\Omega$ ) due to surface Fermi energy pinning in the conduction band.<sup>7</sup> Surface Fermi level pinning in InAs is caused by surface reconstruction<sup>8</sup> and by the abundance of donor-type surface states.<sup>9</sup> Therefore, it is expected that the effects of surface states will be highly pronounced in this material system. Indeed, as discussed in this chapter, the InAs NWFETs show marked transient characteristics and sweep-rate-dependent transconductance. By performing a systematic characterization of the transport properties of InAs NWFETs as



well as an equivalent circuit analysis, we are able to model and quantify their transport properties and extract transport parameters reflective of the inherent properties of the NWs.

## 5.2. Summary of Results

In this chapter, we present an investigation of the capacitive effects of surface states on the analysis of transport properties of InAs NWFETs. We observe that the transfer characteristics of the NWFETs are strongly dependent on gate voltage sweep rate. Detailed analysis indicates that surface state charge modulation creates additional capacitance and alters the modulated mobile charge density in the NWFET channel, resulting in a time-dependent extrinsic transconductance which will limit the device operating speed and severely affects carrier mobility and carrier density determination from conventional three-terminal current-voltage characteristics. Slow gate voltage sweep rates result in charge balance between carrier capture and emission from interface states and lead to reduced hysteresis in the transfer curves. The gate transconductance is thus increased and intrinsic NW transport parameters can be isolated. In the InAs NWFETs, a carrier mobility value of  $\sim 16000 \text{ cm}^2/\text{V}\cdot\text{s}$  was obtained from the transfer curves at slow sweep rates, which is significantly higher than  $\sim 1000 \text{ cm}^2/\text{V}\cdot\text{s}$  obtained at fast sweep rates. A circuit model that takes into account the reduction in the extrinsic transconductance is used to estimate an interface state capacitance to be  $\sim 2 \text{ }\mu\text{F}/\text{cm}^2$ , a significant value that can lead to underestimation of carrier mobility.

### 5.3 Experiment

InAs NWs were grown by metal-organic chemical vapor deposition (MOCVD). 40 nm diameter Au colloids were dispersed on thermally grown SiO<sub>2</sub> on Si (001) and the growth was performed at a substrate temperature of 350 °C under 100 Torr chamber pressure using Tri-methyl-indium and Arsine in H<sub>2</sub> carrier gas at an input V/III ratio of 50 for 13 – 30 min. The resulting NWs are n-type and have diameters of 60 – 120 nm and lengths of ~ 10 μm. The NWs were then suspended in ethanol solution and transferred onto a pre-patterned grid on a 600nm SiO<sub>2</sub>/n<sup>+</sup>-Si(001) substrates for device fabrication and characterization.

Source-drain contact leads with variable separation of ~ 0.5 – 4 μm were patterned by e-beam lithography and e-beam evaporation of Ti/Al (15/90 nm) followed by lift-off. A 73 nm ZrO<sub>2</sub>/Y<sub>2</sub>O<sub>3</sub> gate dielectric ( $\epsilon_r=12$ ) layer was then RF sputtered, and e-beam lithography and bi-layer liftoff were then performed to pattern the 100 nm thick Al top-gate, which was also deposited by RF sputtering. Figure 1 shows a field-emission scanning electron microscope (FE-SEM) image of the final top-gate InAs NWFET device. The transfer curves were measured using an HP4155 parameter analyzer and the transient characteristics were measured using a computerized data acquisition board (National Instruments PCI-6030E, 100 KS/s), a current pre-amplifier (Ithaco 1211), and a voltage source (Keithley 6487).

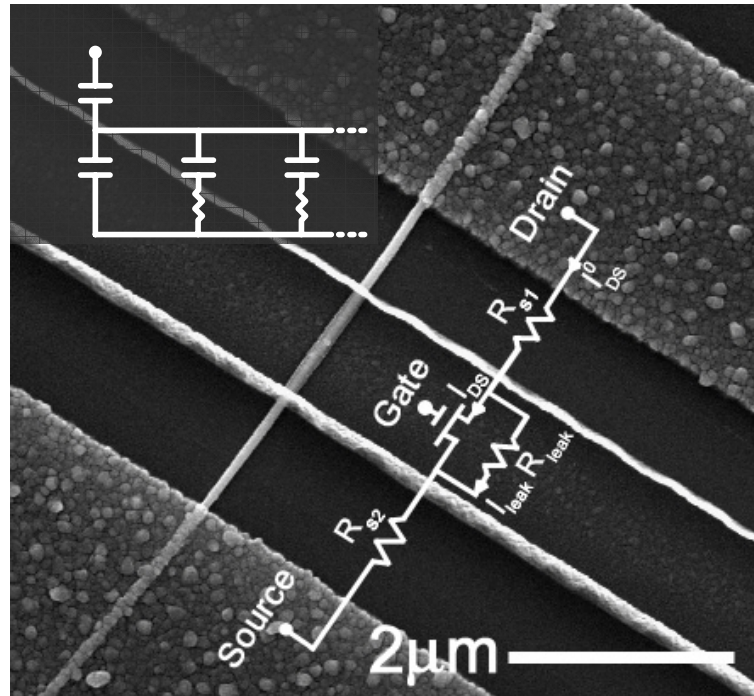


Figure 5.1. FE-SEM image of a top-gate InAs NWFET. Top inset is the equivalent capacitance circuit where  $C_{int}$  and  $R_{int}$  are associated with the interface trap density. Bottom inset is equivalent DC circuit model for the underlap top-gate NWFET.

## 5.4 Results and Discussion

In order to extract transport parameters such as carrier mobility and carrier density from the top-gate InAs NWFET device shown in Figure 1, one has to take into account parasitic circuit components characteristic of the device geometry as shown in the bottom inset to Figure 1.<sup>1</sup> The DC equivalent circuit model consists of drain ( $R_{s1}$ ) and source ( $R_{s2}$ ) extension and contact resistances, and a leakage resistance  $R_{leak}$  which accounts for the unmodulated portion of the NWFET device. The equivalent capacitance model shown in the top inset of Figure 1 includes the oxide capacitance  $C_{ox}$ , an accumulation

capacitance per unit area  $C_{acc}(\Psi_s)$ , an interface state capacitance per unit area  $C_{int}(\Psi_s)$ , and resistance  $R_{int}$  which in combination account for interface trap states with characteristic time constant  $\tau_{int}=AR_{int}C_{int}$ ,  $A$  is the gate area.<sup>10</sup>  $\Psi_s$  is the oxide-InAs surface potential. A detailed circuit analysis taking into account these parasitic components yields an expression for the field-effect mobility ( $\mu_{FE}$ ) as a function of the applied and measured quantities across the three physical device electrodes:<sup>1</sup>

$$\mu_{FE} = \frac{L_G^2 V_{DS}^0 (1 + C_{int}/C_{acc}) / C_{ox}}{\left[ \frac{(V_{DS}^0 - V_s)^2}{g_m^0} - V_s^2 R_{s2} - V_{DS}^0 R_{s2} (V_{DS}^0 - 2V_s) \right]}, \quad (5.1)$$

where  $L_G$  is the gate length,  $V_{DS}^0$  is the applied source-drain voltage,  $g_m^0 \equiv dI_{DS}^0 / dV_{GS}^0$  is the extrinsic transconductance, and  $V_s$  is the voltage drop across  $R_{s1}$  and  $R_{s2}$ . An increased interface state density results in an increase in the interface state capacitance and a corresponding reduction of the equivalent gate capacitance,  $C_G = C_{ox} / (1 + C_{int}/C_{acc})$ . As a result, extraction of the field effect mobility without considering the interface state capacitance results in underestimated mobility values as evident from equation (5.1).

The interface state capacitance can be expressed as<sup>10</sup>

$$C_{int} = \frac{dQ_{int}}{d\Psi_s} = q \frac{dn_{int}}{dE_s} \quad (\text{F/cm}^2) \quad (5.2)$$

where  $\Psi_s$  and  $E_s$  are the surface potential and energy at the gate oxide-semiconductor interface, respectively,  $Q_{int}$  is the modulated interface charge density in the gate area  $A$ , and  $n_{int}$  is the surface state density.  $\Psi_s$  is a function of both the axial and the radial potential drops across the device. Thus,  $C_{int}$  is a differential capacitance which is function of  $\Psi_s$ , and is subject to change while measuring the device output and transfer curves.

Substantial errors might arise in calculation of  $\mu_{FE}$  from equation (5.1) if one assumes a single numerical value for  $C_{int}$ . Measurements of the transfer curves where the interface charge density is modulated or reduced (by varying the gate voltage sweep rate) are therefore utilized to reveal the effects of  $C_{int}$  on electrical characteristics and parameter extraction.

Figure 5.2 shows transient transfer curves measured at constant  $V_{DS}=0.5$  V and various  $V_{GS}$  values held for 150 s each with  $V_{GS}$  switched in the following sequence: 0 V, -4 V, 0 V, +4 V, 0 V, ... -1 V, 0 V, +1 V, 0 V. The transient decays were fitted using a stretched exponential rise and decay of the form

$$I = I_{\infty} + (I_0 - I_{\infty}) \exp(-t/\tau)^{\alpha}, \quad (5.3)$$

where  $I_0$  and  $I_{\infty}$  are the initial and final values of the source-drain current when the interface states are populated (charge neutral) and empty (positively charged), respectively,  $\tau$  is the surface state trapping and de-trapping time constant, and  $\alpha$  ( $0 < \alpha < 1$ ) is the stretching parameter.<sup>11</sup>  $1-\alpha$  indicates the strength of the driving force which determines the change in current rise or decay rates with time. This force changes with time due to surface state trapping and de-trapping that affects the current rise and decay rates  $k$ , where  $dI/dt = -k(t)I(t)$ ,  $k(t) \propto t^{\alpha-1}$ . From the curves fitted to the data in Figure 5.2 using equation (5.3),  $\alpha$  decreases from 0.64 to 0.15 as  $V_{GS}$  is reduced from -1 V to -4 V. At -4 V, the larger electrostatic fields at the oxide-InAs interface produce faster change of the decay rates as time progresses when compared to the smaller fields at  $V_{GS} = -1$  V.

Interface trap states for InAs are known to have donor-type characteristics,<sup>12</sup> i.e.

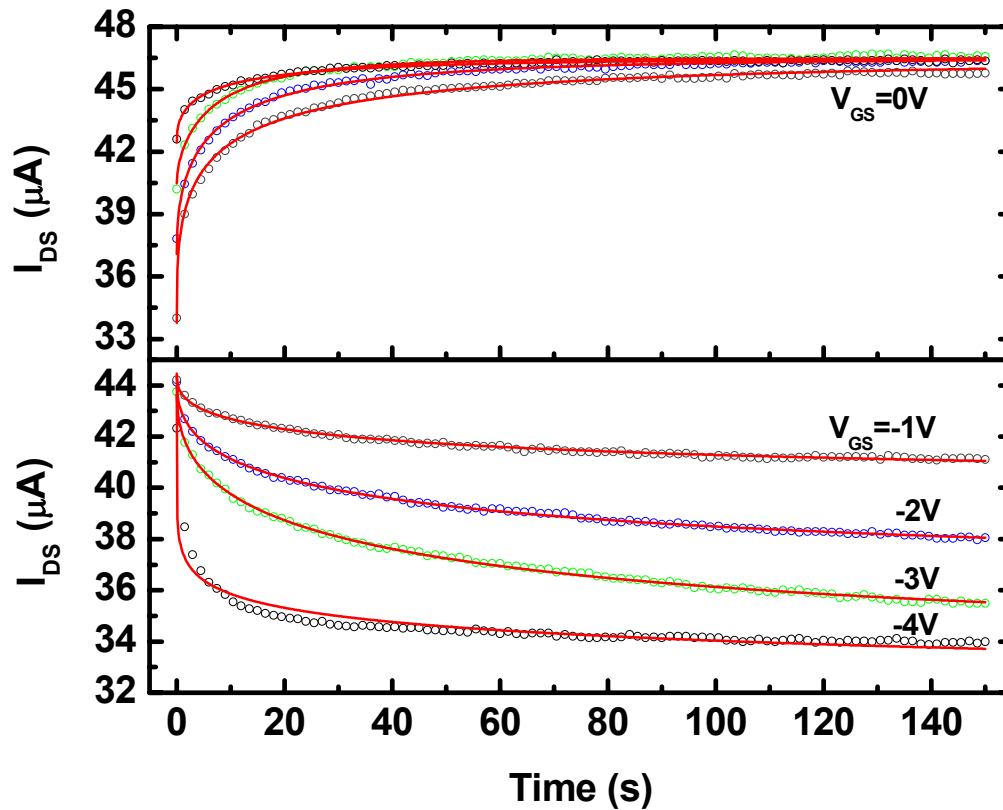


Figure 5.2. Time resolved transfer characteristics of an InAs NWFET with  $L_{SD}=3.35 \mu\text{m}$ ,  $L_G=1.02 \mu\text{m}$ ,  $D=72 \text{ nm}$ , showing long characteristic time constants up to 45 s (open circles) and stretched exponential fits to these curves (solid lines).

are charge neutral when occupied by an electron and positively charged otherwise.<sup>13</sup> As the surface state density increases, the localized states can begin to overlap, forming a “surface band” through which conduction may occur.<sup>14</sup> Thus, turning off the channel of the NWFET can require depleting the “surface band” and overcoming the resulting positively charged states without inverting the surface. When negative  $V_{GS}$  is applied, positively charged surface states at the InAs surface ( $Q_{int}$ ) reduce the gate field by  $Q_{int}/\epsilon_{ox}$  and the gate voltage by  $Q_{int} \cdot t_{ox}/\epsilon_{ox}$ , where  $t_{ox}$  and  $\epsilon_{ox}$  are the oxide thickness and dielectric constant, respectively. This will reduce full depletion of the NWFET channel. To confirm

the latter behavior, we have performed 2D Silvaco Atlas simulations for a device structure similar to the fabricated one. Contour maps of the carrier concentration for  $V_{GS}=-2$  V and  $V_{DS}=0.5$  V are shown in Figure 5.3. In the presence of a fixed positive charge ( $Q_f/q=10^{12}$  cm<sup>-2</sup>)<sup>15</sup> at the NW surface, an accumulation layer of electrons is formed at the surface and the depletion region extends only a small distance under the gate, as shown in Figure 5.3 (a). For the same device structure and same applied voltages, but without the fixed positive charge, the depletion width extends further into the channel as shown in Figure 5.3 (b). From Figure 5.3 (a), we see that even if the surface conduction channel associated with the “surface band” is turned off, the presence of positive charges prevents full NW channel depletion leading to high off-state currents.

Figure 5.4 (a) shows a set of sweep rate dependent transfer curves with negative to positive sweep direction obtained with  $V_{DS}=0.5$  V. Slow  $V_{GS}$  sweep rates allow interface state charging and discharging to follow the sweep rate and minimize the interface state capacitance resulting in higher transconductance. The extrinsic transconductance varies by more than one order of magnitude (1 to 12  $\mu$ S) when the sweep rate is varied from  $10^3$  V/s to 1.7 mV/s. Moreover, for slower sweep rates (i.e. when  $qd\psi_s / dt \leq E_{trap} / \tau$ ),  $I_{DS}$  exhibits evident decay in the off-state biasing region. This is a consequence of a long de-trapping time constant which causes the apparent “tail” in the  $I_{DS}$ - $V_{GS}$  characteristics seen in Figure 4(a). The highest measured gate leakage current was six orders of magnitude less than that of the source-drain current and thus, gate leakage current has no effect on the observed  $I_{DS}$  tails. For such devices with high turn off currents, the onset gate voltage for current modulation in the NW segment under the gate can be defined as the threshold voltage,  $V_T$ . Once  $V_{GS} \geq V_T$ , the gate transconductance

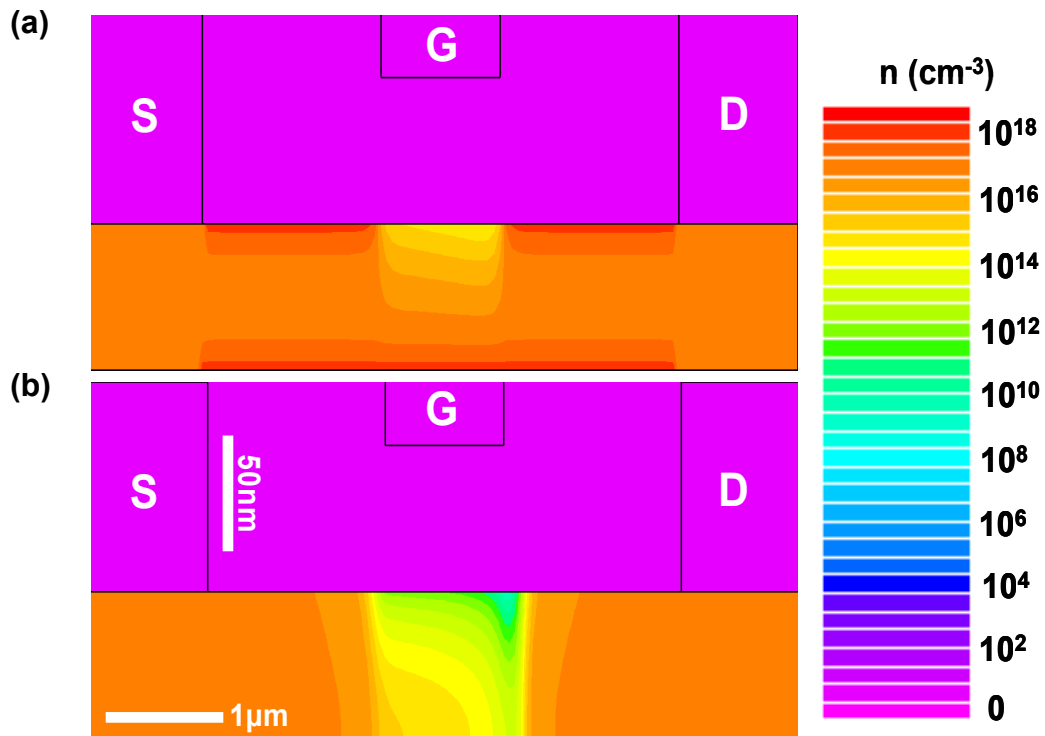


Figure 5.3. 2D Silvaco Atlas simulation of the carrier concentration for a 70 nm diameter InAs NWFET ( $N_D = 5 \times 10^{16}$  cm<sup>-3</sup>) with (a) fixed positive charged traps ( $Q_f/q = 10^{12}$  cm<sup>-2</sup>) under the gate and (b) charge neutral surface under the gate.  $V_{DS} = 0.5$  V and  $V_{GS} = -2$  V.

overcomes the current decay and  $I_{DS}$  increases with increasing  $V_{GS}$ . An increase in the transconductance implies a higher measured carrier mobility as seen from equation (1). Figure 5.4 (b) shows the computed apparent mobility values from the transfer curves using equation (5.1) where  $C_{int}/C_{acc}$  was set to zero. Mobility values of  $\sim 1000$  cm<sup>2</sup>/V·s extracted using this technique from these InAs NWFETs with fast  $V_{GS}$  sweep rates are in good agreement with those reported for similar InAs NW devices.<sup>16,17</sup> For slow  $V_{GS}$  sweep rates, much higher field-effect mobility value (16000 cm<sup>2</sup>/V·s) is obtained and is



suggestive of the potential of InAs NWs for high speed nanoelectronics provided that the necessary surface passivation is achieved.

Similarly, the effects of interface states on the charge carrier density in the channel are non-negligible. One can compute the channel charge from the extracted  $I_{DS}$ - $V_{GS}$  characteristics for the NW portion under the gate using  $n_{channel} = I_{DS}L_G / q\mu_{FE}V_{DS}A$ , where  $\mu_{FE}$  as obtained from equation (1) accounts for the effect of interface states. Figure 5.4 (b) shows the extracted carrier densities for this NWFET with different  $V_{GS}$  sweep rates. Slow  $V_{GS}$  sweep rate results in greater depletion width and consequently reduction in the carrier concentration under the gate as discussed earlier, and is consistent with the extracted carrier concentration values. This is opposite to what is observed in, for example, GaN/AlGaIn-based HFETs, where the negative interface state charge in the gate-drain extension region acts as a surface virtual gate and causes further depletion of the channel.<sup>18</sup> Interface state charging in the extension regions for this InAs NWFET has not been considered in this analysis due to its minimal effects when  $V_{DS}$  is held constant. The potential drop differences in these extension regions would be insignificant between successive measurements. Interface state charge modulation is expected to be higher directly beneath the top-gate due the rapid decay of the gate field in the extension regions as can be seen in Figure 5.3 (a).

Figures 5.5 (a), (b) and (c) show the transfer curves obtained with a  $V_{GS}$  sweep rate  $> 10$  V/s in both directions at  $V_{DS}=50$  mV, 250 mV and 500 mV, respectively, revealing clear hysteresis. With a slow sweep rate of 6.7 mV/s, hysteresis in the transfer curves is diminished for all  $V_{DS}$  values as shown in Figures 5 (d), (e) and (f). This indicates that surface state modulation occurs mostly under the gate in these InAs

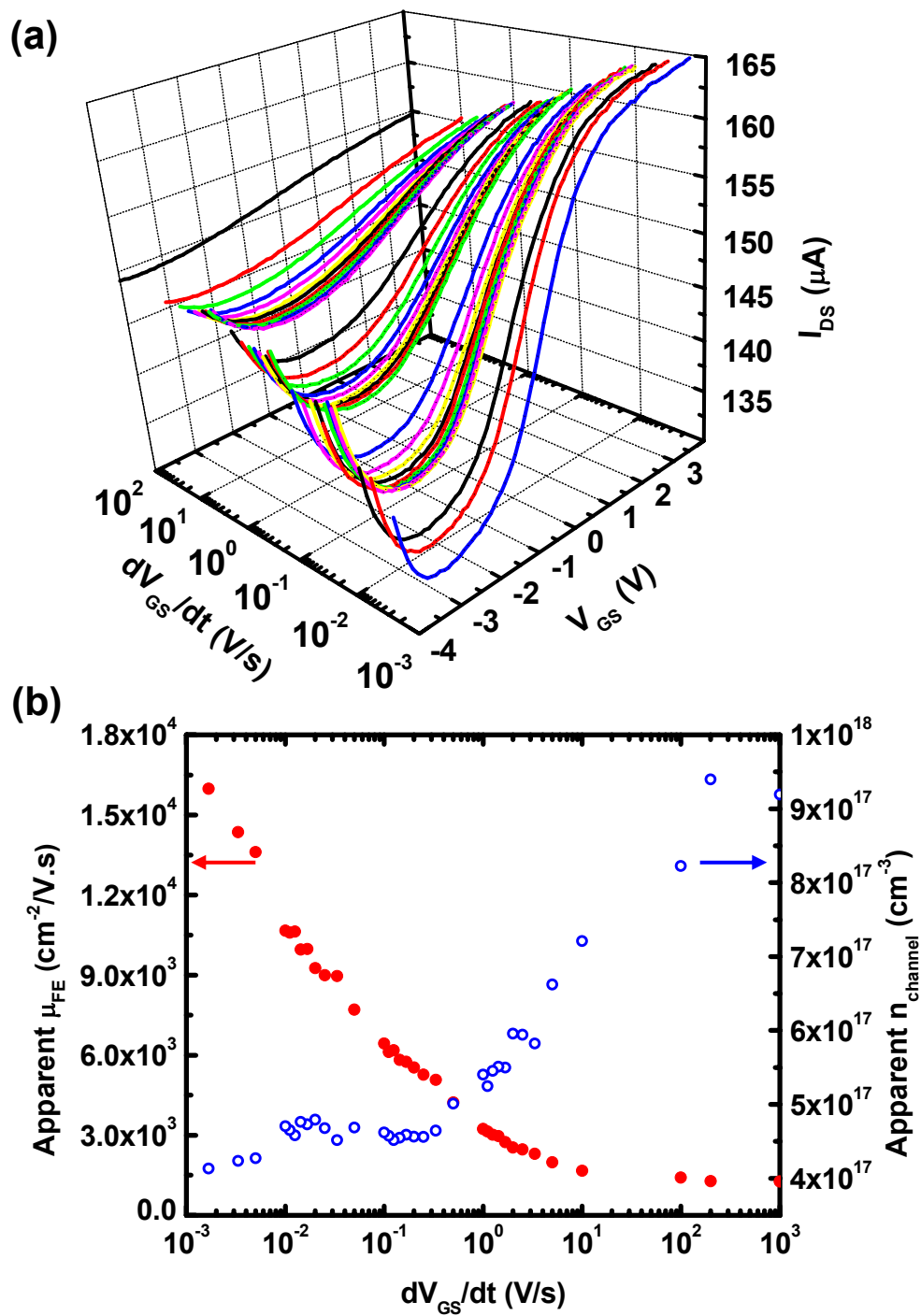


Figure 5.4. (a) Transfer curves of an InAs NWFET with  $L_{SD}=3.5\mu\text{m}$ ,  $L_G=0.78\mu\text{m}$ ,  $D=110\text{nm}$ , plotted for different gate voltage sweep rates. (b) Computed  $\mu_{FE}$  and  $n_{channel}$  from the transfer curves in (a).

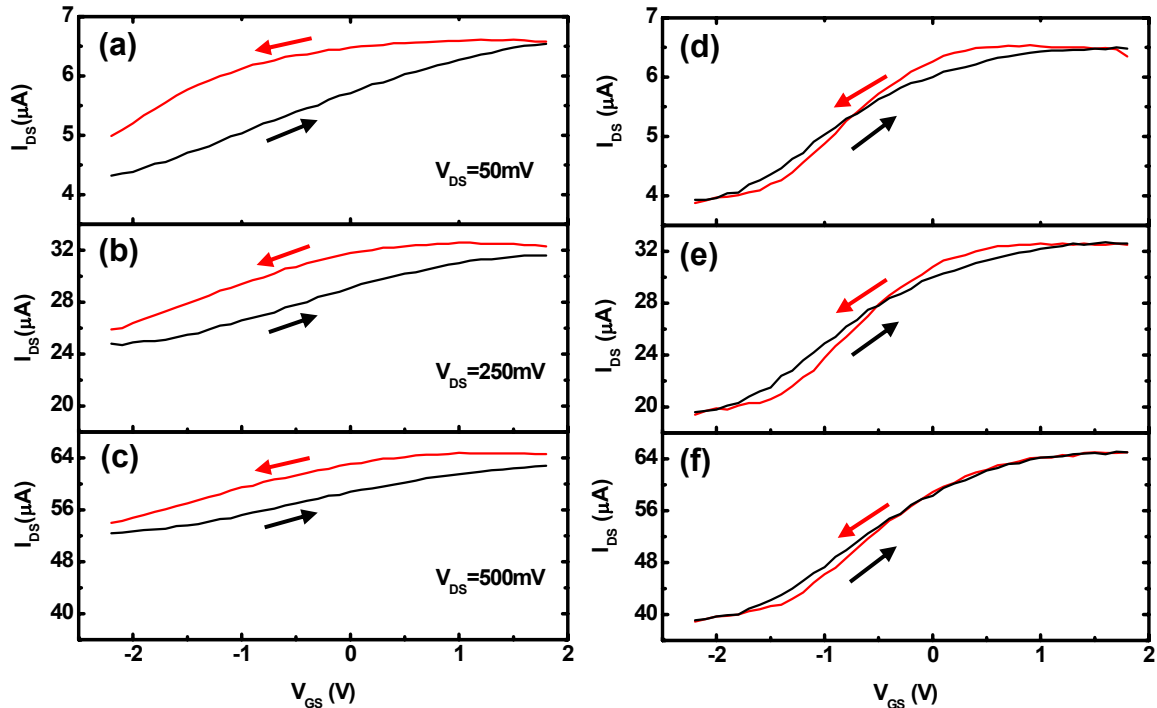


Figure 5.5.  $I_{DS}$ - $V_{GS}$  for an InAs NWFET device with  $L_{SD}=1.85 \mu\text{m}$ ,  $L_G=585 \text{ nm}$ ,  $D=63 \text{ nm}$ . (a), (b), (c): Hysteresis plots for fast gate voltage sweep rate  $> 10 \text{ V/s}$ ; (d), (e), (f): Hysteresis plots with slower gate voltage sweep rate of  $6.7 \text{ mV/s}$ .

NWFETs because reduction in hysteresis prevails for all  $V_{DS}$  values. Also, the “off” current levels at negative  $V_{GS}$  for slower sweep rates are lower than those obtained with fast sweep rates. Hysteresis that arises from surface-related mechanisms, due to time lags between capture and emission from interface states, can be reduced by surface passivation.<sup>19,20</sup> However, the possibility of mobile ion drift in the oxide can not be excluded when explaining the observed hysteresis. Ion-drift type hysteresis is typically observed and quantified from oxide  $C$ - $V$  measurements not readily available for NWs.<sup>21</sup> Since the gate leakage current in these devices is negligible, oxide and mobile charges were not included in our analysis. The reduction in the hysteresis plots through the

measurement technique we present here indicates a charge balance between surface state trapping and de-trapping, and implies that our measurements with reduced sweep rates yield transport parameters for the InAs NWFETs channel that reflect more accurately the inherent transport behavior in the NW.

Using an equivalent circuit model for the NWFET as shown in Figure 1,<sup>1,22</sup> one can also estimate the interface state capacitance contributing to the hysteresis shown in Figure 5, by quantifying its effects on the intrinsic transconductance. In the presence of interface state modulation, the current in the NW portion under the gate can be expressed as<sup>1</sup>

$$I_{DS} = \mu_{FE} \left[ C_{ox} / (1 + C_{int} / C_{acc}) \right] (V_{GS} - V_T) V_{DS} / L_G^2. \quad (5.4)$$

The intrinsic transconductance can then be calculated from equation (4) to be

$$g_{m1} = \mu_{FE} \frac{C_{ox}}{1 + C_{int} / C_{acc}} \frac{V_{DS}}{L_G^2}. \quad (5.5)$$

When interface state capture and emission processes are balanced,  $I_{DS}$  can be expressed in the form

$$I_{DS} = \mu_{FE} C_{ox} (V_{GS} - V_T) V_{DS} / L_G^2, \quad (5.6)$$

due to the elimination of  $C_{int}$ . The expression for intrinsic transconductance in this case reverts to its more usual form,

$$g_{m2} = \mu_{FE} C_{ox} \frac{V_{DS}}{L_G^2}. \quad (5.7)$$

Note that for each measurement at a fixed sweep rate, there is a shift in the threshold voltage. However, this does not alter equation (5.7) which represents the slope of  $I_{DS}$ - $V_{GS}$  that is independent of  $V_T$  shift.

The ratio of the transconductances in equations (5.5) and (5.7) can then be written as

$$g_{m2} / g_{m1} = 1 + \frac{C_{int}}{C_{acc}}. \quad (5.8)$$

Equation (5.8) quantifies the contribution of  $C_{int}$  to the extrinsic transconductance, and relates its variation with  $V_{GS}$  sweep rates as shown in Figure 5.4 (a) due to the variation of  $C_{int}$ .

With a slow sweep rate of 6.7 mV/s, hysteresis in the transfer curves was greatly diminished due to the charge balance between trapping and de-trapping of interface states. In this case, equation (5.7) provides an adequate description of the intrinsic transconductance. For faster sweep rates, the intrinsic transconductance is described by equation (5.5). The interface state capacitance can then be obtained from equation (5.8). The ratio of the intrinsic transconductance extracted from the transfer curves of Figure 5.5 (c) and (f) is  $g_{m1}/g_{m2}=35.4 \mu\text{S}/15.3 \mu\text{S}=2.3$ . From a 1D Schrödinger-Poisson solution using Silvaco Atlas<sup>23</sup> for a planar structure similar to that of the InAs NWFET used in this study,  $\sim 10$  nm spatial separation of the accumulation charges from the interface was computed. Equation (8) can then be used to estimate the interface state capacitance to be  $\sim 2 \mu\text{F}/\text{cm}^2$  which is a non-negligible quantity compared to  $C_{acc}$  and leads to mobility under estimation if not considered, as can be seen from equation (5.1).

## 5.5 Conclusion

In this chapter, we discussed the fabrication of top-gated InAs NWFETs and analyzed the capacitive effects of surface states on their transport properties. The InAs

NWFETs exhibited transient behavior that severely affects characteristic NW parameter extraction. From circuit and device analysis, we obtain apparent field-effect mobility values in the range of 1000 – 16000 cm<sup>2</sup>/V·s, and interface state capacitance of 2 μF/cm<sup>2</sup>. The upper end of the mobility range is believed to best reflect the values intrinsic to transport within the NW. This analysis may help explain the wide range of NW parameters reported in the literature, indicates that measurements with a charge neutralized (or passivated) surface allow the extraction of the intrinsic nanowire transport parameters, and highlights the potential of InAs NWs for high speed electronics with effective surface passivation.

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## 6. EXPERIMENTAL OBSERVATION OF BALLISTIC TRANSPORT IN INDIUM ARSENIDE NANOWIRES AND THEIR DIAMETER DEPENDENT TRANSPORT PROPERTIES

### 6.1 Introduction

The rapid progress in vapor-liquid-solid nanowire (NW) synthesis and device processing have allowed the realization of NWs with diameters down to  $\sim 3$  nm<sup>1</sup> (less than 10 atoms across the NW diameter) and field-effect transistor channel lengths down to 40 nm.<sup>2</sup> As these NWs shrink in dimensions, distinct behavior from that of bulk is expected, even when quantum confinement conditions are not met yet. First, the growth direction of these extremely small NWs differs from those of larger ones. Wu et al. have observed  $\langle 110 \rangle$  growth orientation for  $\sim 3$  nm diameter Si NWs compared to the  $\langle 111 \rangle$  growth orientation for larger diameter NWs. For indirect bandgap semiconductors such as Si, this will have pronounced effect on the transport properties. Second, the surface-to-volume ratio increases with reduced NW diameters leading to enhanced surface states effects. Seo et al. have measured reduced conductivities in Si NWs as their diameter decreases, and attributed this effect to surface depletion.<sup>3</sup> Chang et al. have observed increased conductivity in ZnO NWs as the NW diameter reduces, due to “enrichment of surface states;”<sup>4</sup> a three order of magnitude increase in the free carrier concentration of 18 nm diameter ZnO NWs when compared to 190 nm diameter ZnO NWs was calculated. Motayed et al. on the other hand reported mobility reduction in GaN NWs from 310 cm<sup>2</sup>/V·s for 200 nm diameter NWs to 40 cm<sup>2</sup>/V·s for 95 nm diameter NWs.<sup>5</sup> For InAs NWs, Bryllert et al. have reported 3000 cm<sup>2</sup>/V·s for 80 nm diameter NWs,<sup>6</sup> and

Lind et al. have reported  $1500 \text{ cm}^2/\text{V}\cdot\text{s}$  for 40 nm diameter NWs.<sup>7</sup> Hang et al. have shown that 20 nm diameter InAs NWs exhibit enhanced inverse subthreshold slope and mobility when surface states are passivated with 1-octadecanethiol (ODT).<sup>8</sup> These studies clearly indicate the diameter and surface state effects on transport properties of NWs. Third, devices with reduced channel lengths may exhibit ballistic transport and suffer from short channel effects; the latter was discussed in chapter 1. Ballistic transport in semiconducting single wall carbon nanotubes (CNTs) was observed for length scales  $\sim 0.5 \mu\text{m}$  at room temperature using the transmission line measurement technique.<sup>9</sup> Another procedure to obtain detailed information on the channel resistance in nanostructures is the use of conductive atomic force microscopy (cAFM) as demonstrated by Yaish et al. who were able to isolate CNT-contact, CNT intrinsic, and CNT-tip resistances.<sup>10</sup> Jo et al. have used such technique in 2007 to measure channel length dependent resistance for  $\text{In}_2\text{O}_3$  NWs for which the resistance kept on decreasing linearly with channel length down to 20 nm.<sup>11</sup> Using cAFM, we have observed in 2005 ballistic transport in InAs NWs over length scales of  $\sim 200 \text{ nm}$  at room temperature.<sup>12</sup> Details of this study and detailed device analysis for extraction of transport coefficients as function of NW diameter will be discussed in this chapter.

## 6.2 Summary of Results

We have studied the scaling effects of channel length and channel diameter in InAs NWs on their transport properties. First, using a conducting diamond-coated tip as a local electrical probe in an atomic force microscope, the resistance of the InAs NW has

been measured as a function of electron transport distance within the NW. We observe two regimes of transport behavior: for distances of  $\sim 200$  nm or less, resistance independent of electron transport distance, indicative of ballistic electron transport, is observed; for greater distances, the resistance is observed to increase linearly with distance, as expected for conventional drift transport. These observations are in very good qualitative accord with the Landauer formalism for mesoscopic carrier transport, and the resistance values derived from these measurements are in good quantitative agreement with carrier concentrations and mobilities determined for the same type of NWs. These results provide direct information concerning distances over which ballistic transport occurs in InAs NWs.

Second, room temperature transport properties of InAs NWFETs as function of their diameters are discussed. Due to their field dependence, device analysis that enables extraction of the transport coefficients at constant vertical and lateral fields is developed and utilized for a set of 26 top-gate InAs NWFET devices with diameters in the range of 62 – 115 nm. Room temperature field-effect mobility values of 625 – 3600  $\text{cm}^2/\text{V}\cdot\text{s}$  with correspondent free carrier concentrations of  $1.6 \times 10^{18} - 4 \times 10^{17} \text{ cm}^{-3}$  at zero gate bias were computed. Diameter dependences of mobility and carrier concentration are attributed to surface Fermi energy pinning in the conduction band that leads to a surface electron accumulation layer with enhanced surface scattering. Assuming the presence of a fixed positive charge of  $Q_f/q = 2.7 \times 10^{12} \text{ cm}^{-3}$ , one dimensional Schrödinger-Poisson solutions for different InAs slab thicknesses show that the average integrated carrier concentration increases as the InAs slab thickness is reduced, in agreement with the experimentally extracted values in the InAs NWs.

### 6.3 Experiment

InAs NWs used in these studies were grown on SiO<sub>2</sub> substrates using organo-metallic vapor phase epitaxy as discussed in chapter 2. In brief, 40 nm diameter Au nanoparticles atop SiO<sub>2</sub>/Si substrates were utilized for the growth of InAs NWs at 350 °C substrate temperature and 100 Torr chamber pressure, using tri-methyl-indium and arsine precursors in H<sub>2</sub> carrier gas at an input V/III ratio of 50 and for growth times of 13, 20 and 30 min. This results in n-type NWs with lengths of ~ 10 μm and diameters of ~ 60 – 120 nm. Following growth, the InAs NWs were suspended in an ethanol solution and transferred to a thermally grown 600 nm SiO<sub>2</sub>/n<sup>+</sup>-Si substrate with a pre-patterned grid for lithography alignment. E-beam lithography was then used to pattern source-drain electrodes with variable spacing followed by 15 nm/85 nm Ti/Al deposited by e-beam evaporation and lift off. This results in ohmic contacts with contact resistance of ~ 1 KΩ. Scanned probe measurements were performed using a Digital Instruments/Veeco Nanoscope III Multimode atomic force microscope to which a current preamplifier was attached to enable cAFM measurements.<sup>13</sup> The experimental geometry is shown schematically in Figure 6.1. A diamond-coated scanning probe tip served as a positionable electrical contact to the InAs nanowire, with the macroscopic Ohmic contact fabricated lithographically serving as the second contact to the nanowire for a two-terminal measurement of electrical current flow through the nanowire. A dc bias voltage  $V_{DS}$  was applied between the macroscopic contact and the conducting probe tip and the resulting current was measured as a function of distance  $L$  between the probe tip and the edge of the contact. For top-gate InAs NWFETs, a 73 nm ZrO<sub>2</sub>-Y<sub>2</sub>O<sub>3</sub> dielectric layer was then deposited, followed by e-beam lithography to define a ~ 1 μm wide gate. 100 nm

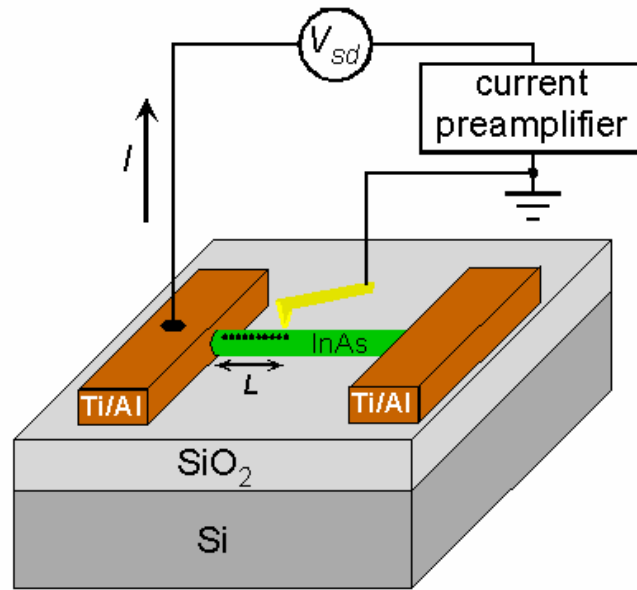


Figure 6.1. Schematic diagram of experimental probe tip and sample geometry and electrical measurement configuration. Current  $I$  is measured for fixed bias voltage  $V_{DS}$  as a function of tip-contact distance  $L$ , with the probe tip forming a positionable contact to the nanowire in a two-terminal device measurement.

thick Al top-gate metal was sputtered, leaving extension regions with the source and drain electrodes. The output and transfer curves for these NWFETs were measured using an HP4155 parameter analyzer

#### 6.4 Ballistic Transport in InAs Nanowires

Current images acquired at fixed  $V_{DS}$  simultaneously with the topograph reveal a trend of constant to decreasing current  $I$  with increasing tip-contact distance  $L$ , suggesting that the nanowire resistance contributes significantly to the total device resistance, and as expected generally increases with transport distance within the nanowire. A total device

resistance  $R=V_{DS}/I$  can then be determined as a function of electron transport distance  $L$ , as shown in Figure 6.2. The data in Figure 6.2 were derived from cAFM images by averaging current measured at several points over a distance of  $\sim 20$  nm normal to the nanowire axis, and clearly reveal two distinct regimes of behavior. For electron transport distances below approximately 200 nm,  $R$  is observed to be independent of  $L$ , while for larger distances  $R$  increases approximately linearly with  $L$ . Linear fits to these two regions are also shown in Figure 6.2, and yield a constant contribution to the device resistance of  $\sim 40$  k $\Omega$  and, for carrier transport distances over 200 nm, an additional length-dependent contribution of  $\sim 23$  k $\Omega/\mu\text{m}$ .

To interpret these results, we decompose the total measured resistance into several components of distinct physical origin. The total resistance of the tip-nanowire-Ohmic contact structure can be written, adapting the well-known Landauer formalism, as<sup>14</sup>

$$R = R_{drift} + R_{tip-NW} + R_s + \frac{h}{2e^2M} \quad (6.1)$$

where  $R_{drift}$  is the contribution due to scattering during drift transport in the nanowire,  $h/2e^2M$  is the contact resistance to the nanowire with  $M$  being the number of propagating electron modes in the nanowire,  $R_{tip-NW}$  is the additional resistance between the probe tip and the nanowire, and  $R_s$  is the parasitic series resistance arising from, e.g., external wiring and wire bonds and the patterned metal electrodes. Of these contributions, only  $R_{drift}$  depends directly on  $L$ ; therefore, any dependence observed of  $R$  on  $L$  should constitute primarily a dependence of the nanowire resistance on  $L$ .

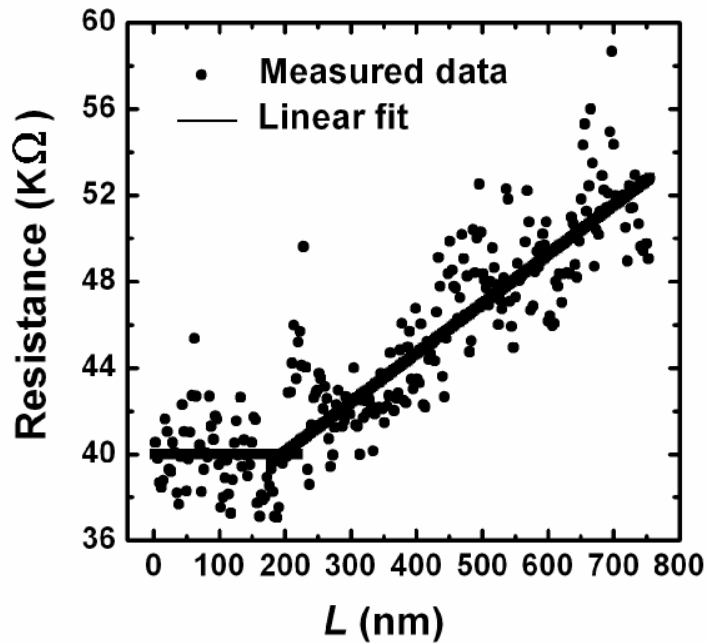


Figure 6.2. Resistance measured by cAFM as a function of tip-contact distance  $L$  (dots), with linear fits for  $L$  below  $\sim 200$  nm, for which resistance is independent of  $L$ , and for  $L$  above  $\sim 200$  nm, for which resistance increases linearly with  $L$ .

The observation of a range of tip-contact distances for which  $R$  is nearly independent of  $L$  suggests that electron transport over these distances within the nanowire is primarily ballistic. However, the  $\sim 200$ nm distance over which this behavior is observed should not be necessarily taken to be a direct measure of the electron mean free path in the nanowire. Specifically, assuming an electron mean free path  $\lambda$ , interpreted as the average distance an electron travels in the nanowire before experiencing a scattering event, a nonzero probability  $t$  that a single scattering event will result in transmission of the electron (and, consequently, a probability  $1 - t$  that the electron will be reflected), and a Poisson distribution for the number of scattering events experienced by an electron

while traversing a distance  $L$ , relatively straightforward calculations show that the resistance of the nanowire increases much more slowly with  $L$ , for values up to a few mean free paths, than would be predicted by the conventional scattering-induced resistance,<sup>14</sup>

$$R = \frac{h}{2e^2 M} \left( \frac{L}{L_m} \right). \quad (6.2)$$

Thus, the experimental observation shown in Figure 6.2 suggests a mean free path approximately in the range of 40-80 nm. The electron mean free path in the InAs nanowire can also be estimated using independently measured values for electron mobility and calculations of electronic structure within the wire to determine the Fermi velocity. Specifically, the mean free path is given by

$$L_m = v_f \tau, \quad (6.3)$$

where  $v_f$  is the Fermi velocity and  $\tau$  is the scattering relaxation time.  $\tau$  can be estimated from the electron drift mobility  $\mu$  using the relation  $\mu = q\tau/m^*$ , where  $q$  is the fundamental electronic charge and  $m^*$  is the electron effective mass in InAs. Separate measurements on very similar InAs nanowires have yielded mobility values in the range of 1600 – 6600  $\text{cm}^2/\text{V}\cdot\text{s}$  as discussed in chapter 4. For our purposes we assume an electron mobility for the InAs nanowire of 3000  $\text{cm}^2/\text{V}\cdot\text{s}$ , which combined with the InAs electron effective mass  $m^* = 0.023m_e$  yields a scattering relaxation time  $\tau \sim 0.04$  ps. While the measured values of electron mobility in InAs nanowires are much lower than those for bulk InAs, the large contribution of electrons in the InAs surface accumulation layer to carrier



transport in the nanowire geometry should lead to effective mobility values closer to the measured mobilities<sup>15,16</sup> of surface electrons in InAs, approximately 1000 – 3000 cm<sup>2</sup>/V·s – as is indeed observed.

To estimate the Fermi velocity, we perform an analytical calculation of the conduction subband structure assuming a model InAs nanowire of radius  $r$  with a constant potential within the nanowire and infinite potential barriers at the nanowire surface. For this model nanowire structure, Schrödinger's equation in cylindrical coordinates  $(\rho, \phi, z)$  can be written as,

$$-\frac{\hbar^2}{2m} \left[ \frac{1}{\rho} \frac{\partial}{\partial \rho} \left( \frac{\rho \partial \Psi}{\partial \rho} \right) + \frac{1}{\rho^2} \frac{\partial^2 \Psi}{\partial \phi^2} + \frac{\partial^2 \Psi}{\partial z^2} \right] = E \Psi . \quad (6.4)$$

Using a simple separation of variables with  $\Psi(\rho, \phi, z) = R(\rho)F(\phi)Z(z)$  such that

$\frac{1}{Z} \frac{\partial^2 Z}{\partial z^2} = -k^2$  is a constant and  $\frac{1}{F} \frac{\partial^2 F}{\partial \phi^2} = -m^2$  is a periodic function of  $\phi$ , (6.4) can be

written as,

$$\rho^2 \frac{\partial^2 R}{\partial \rho^2} + \rho \frac{\partial R}{\partial \rho} + \left[ \rho^2 \left( \frac{2m}{\hbar^2} E - k^2 \right) - m^2 \right] R = 0 , \quad (6.5)$$

whose solution is  $R(\rho) = AJ_m(x\rho) + BN_m(x\rho)$ , where  $J_m$  and  $N_m$  are the Bessel

functions of the first and second order, and  $x = \sqrt{\frac{2mE}{\hbar^2} - k^2}$ . Since  $R(\rho)$  is bounded at

$\rho=0$ ,  $B=0$ . The Eigen values  $x$  are found by finding the solutions satisfying  $J_m(xr) = 0$

where  $r$  is the NW radius. These eigen values are the discrete subband energies of the

NW, and can be calculated using

$$E_{m,n} = \frac{\hbar^2}{2m^* r^2} \rho_{m,n}^2, \quad (6.6)$$

where  $\rho_{m,n}$  is the  $n^{\text{th}}$  root of the  $m^{\text{th}}$  order Bessel function  $J_m$ . Figure 6.3 (a) and (b) shows the subband energies for a 75 nm diameter InAs NW and the correspondent radial wavefunctions. To compute the number of confined modes or subband energies, one have to solve for a one-dimensional free carrier concentration  $n_{1D}$  equal to that measured from experiment. This is done using

$$n_{1D} = \left( \frac{2m^*}{\hbar^2} \right)^{1/2} \int_{E_c}^{\infty} \frac{\sum_{m,n} H(E - E_{m,n})}{\sqrt{E - E_{m,n}}} \cdot \frac{1}{1 + e^{(E - E_F)/k_b T}} dE, \quad (6.7)$$

where  $H(E - E_{m,n})$  is the Heaviside function that is equal to unity when  $E > E_{m,n}$  and is zero otherwise,  $\hbar$  is Plank's constant,  $k_b$  is Boltzmann's constant, and  $E_F$  is the Fermi energy.  $E_F$  is varied such that the  $n_{1D}$  obtained from equation (6.7) is equal to that measured from experiment ( $n_{1D} \sim 9 \times 10^6 \text{ cm}^{-1}$ ). Figure 6.5 shows a plot of the 1D density of states and  $n_{1D}$  for the 75 nm diameter InAs NW used for  $E_F$  computation. This results in  $E_F - E_c \sim 100$  meV and  $\sim 10$  confined modes whose energies are shown in Figure 6.3 (a). Using an average mobility of  $3000 \text{ cm}^2/\text{V}\cdot\text{s}$  and invoking  $E_f - E_{gr} = \hbar^2 k_f^2 / 2m^*$  with  $v_f = \hbar k_f / m^*$  into equation (6.3), we estimate a mean free path  $L_m \sim 55$  nm, well within the range of values that are consistent with the observations shown in Figure 6.2. The mean free path can also be calculated from equation (6.2), obtaining the number of occupied transverse modes  $M$  from the numerical calculation of  $E_F - E_c$  and of the conduction subband energies  $E_{m,n}$ . This approach yields  $M=10$  and, using the measured value for  $\rho/L$  of  $23 \text{ k}\Omega/\mu\text{m}$ , a mean free path  $L_m=56$  nm – very consistent with the first

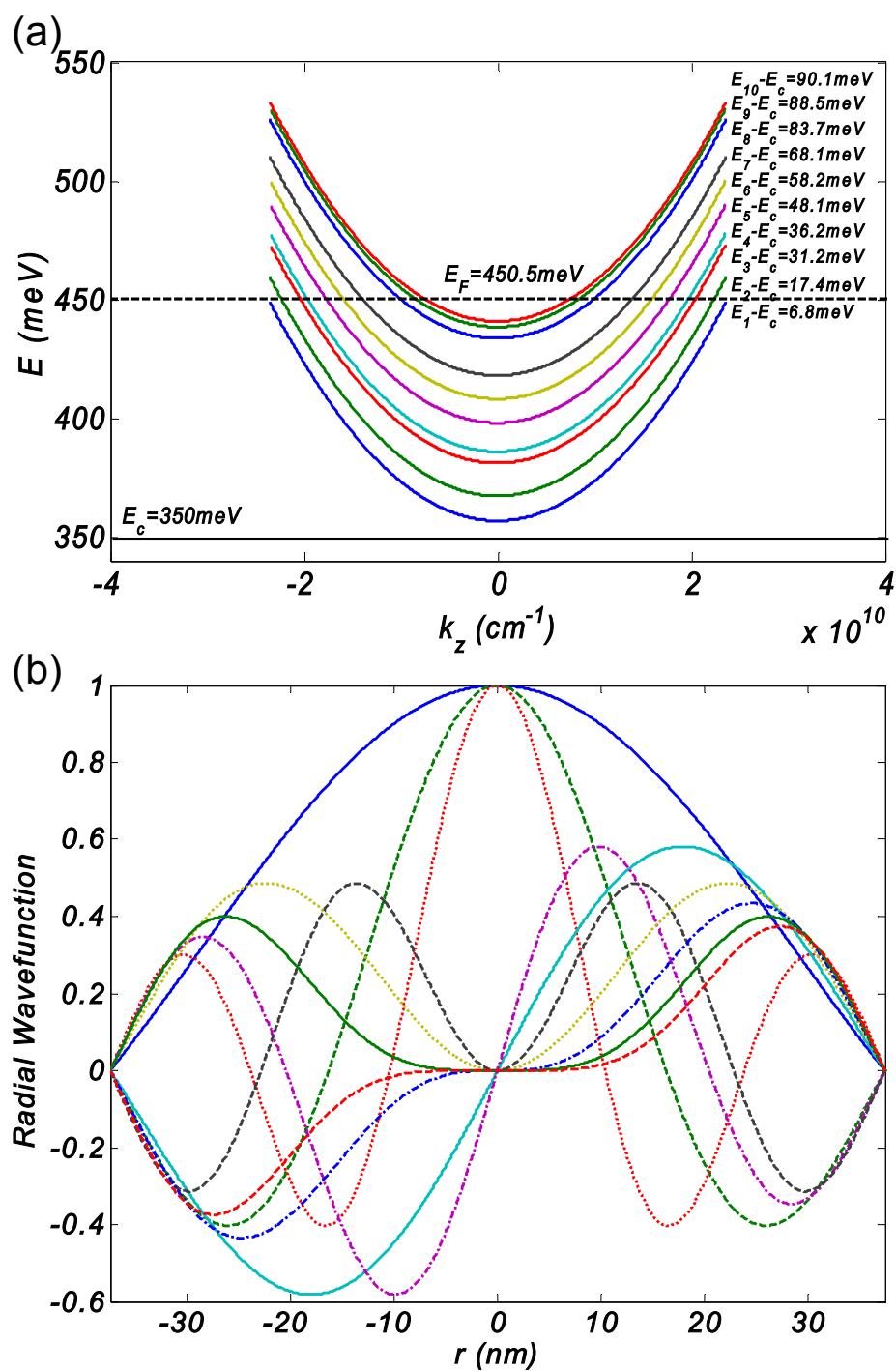


Figure 6.3. (a)  $E(k)$  energy subband diagram showing the 10 confined modes for a 75 nm diameter InAs NW. (b) Radial wavefunction distribution for the subband energies in (a).

approach and with our experimental observations.

### 6.5 Transport Properties of InAs Nanowires as function of their Diameter

Another important aspect of NW scaling is their diameter dependent transport properties. We have studied this effect by extracting the transport coefficients for the InAs NWs from NWFET measurements. In these electrical measurements, we observe that, as expected, the current capacity of the NW decreases as the NW diameter decreases, as illustrated in Figure 6.5 (a), which shows current voltage ( $I$ - $V$ ) characteristics of a selected set of InAs NWs with different diameters taken at an applied gate voltage of  $V_{GS}^0 = 0$  V. The observed trends in the  $I$ - $V$  characteristics as a function of diameter are valid for all  $V_{GS}$  values, and  $V_{GS}^0 = 0$  V is chosen for convenience. However, the measured current at a given value of applied source-drain bias  $V_{DS}^0$  depends on both the NW length  $L_{SD}$  and the NW cross-sectional area  $A$ . Variation of the transport coefficients as function of NW diameter can be better evaluated through conductance,  $\sigma = qn_{av}\mu_{FE} = L_{SD} / \left[ A dV_{DS}^0 / dI_{DS}^0 \Big|_{V_{GS}^0 = 0V} \right]$ , calculated near  $V_{DS}^0 = 0$  V, where  $q$  is the fundamental charge constant. Figure 6.5 (b) shows a plot of conductance vs. NW diameter calculated from the  $I$ - $V$  curves of Figure 6.5 (a). It is evident from Figure 6.5 (b) that the conductance decreases as the NW diameter decreases. For a proper interpretation of the decrease in NW conductance with diameter, however the effects of diameter reduction on  $n_{av}$  and  $\mu_{FE}$  have to be isolated.

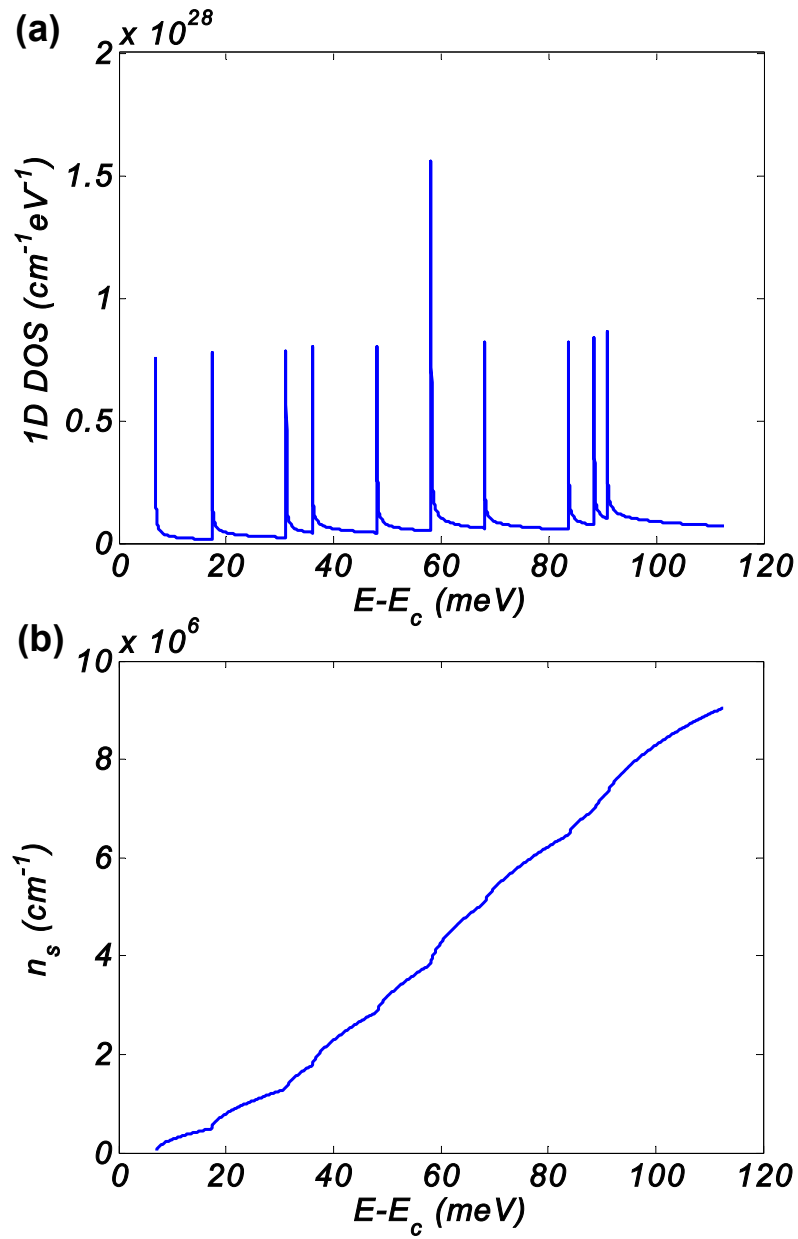


Figure 6.4. (a) Plot of the 1D density of states for a 75 nm diameter InAs NW. (b) Plot of the 1D free carrier concentration  $n_{1D}$  calculated using equation (6.7) to estimate  $E_F$ .

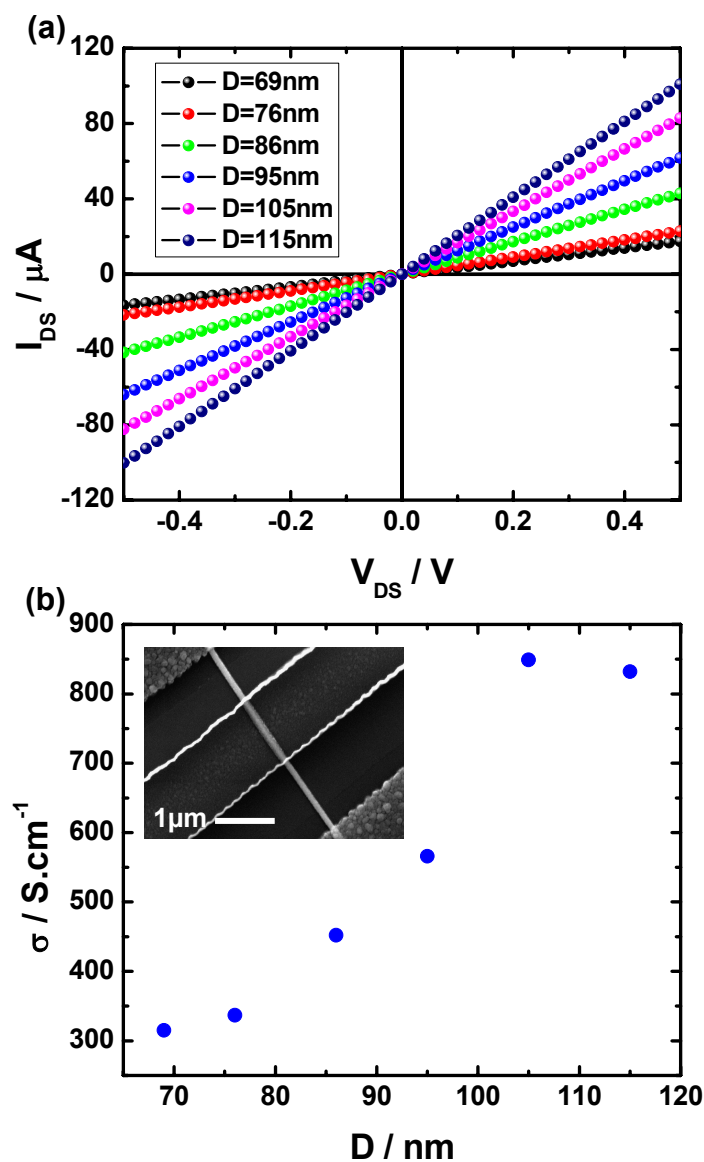


Figure 6.5. (a) Current voltage characteristics of several InAs NWFETs with different diameters at  $V_{GS}^0 = 0$  V. (b) Corresponding conductance calculated near  $V_{DS}^0 = 0$  V. Inset is a representative FE-SEM image of a top-gate InAs NWFET used in this study.

For the underlap top-gate geometry, one can assign a drain series resistance,  $R_{s1}$ , that accounts for the contact and gate-to-drain extension region resistances, and a source series resistance,  $R_{s2}$ , that accounts for the contact and gate-to-source extension region resistances. The presence of positively charged surface states<sup>17</sup> at the oxide-InAs

interface decreases the gate field by  $Q_{int}/\epsilon_{ox}$ , where  $Q_{int}$  is the interface charge density and  $\epsilon_{ox}$  is the oxide dielectric constant, and prevents full depletion of the InAs NW channel. Thus, a leakage resistance,  $R_{leak}$ , associated with the lowest source-drain current  $I_{DS}^0$  through the channel at negative  $V_{GS}^0$ , is introduced. Simple circuit analysis can then be used to account for potential and current drops across these parasitic resistances in order to extract the intrinsic  $I$ - $V$  characteristics of the active portion of the InAs NWFET according to

$$V_{DS} = V_{DS}^0 - I_{DS}^0 (R_{s1} + R_{s2}), \quad (6.8)$$

$$I_{DS} = I_{DS}^0 \left( 1 + \frac{(R_{s1} + R_{s2})}{R_{leak}} \right) - \frac{V_{DS}^0}{R_{leak}}, \quad (6.9)$$

$$V_{GS} = V_{GS}^0 - I_{DS}^0 R_{s2}, \quad (6.10)$$

where  $V_{DS}^0, V_{GS}^0$ , and  $I_{DS}^0$  are the applied drain-source and gate-source voltages and the measured drain-source current, respectively,  $V_{DS}, V_{GS}, I_{DS}$  are the potential and current values at the terminals of the NWFET segment directly under the gate.

The field-effect mobility and the average carrier concentration are typically calculated from the transfer characteristics in the linear operating regime. Figure 6.6 (a) shows a set of intrinsic transfer curves extracted using equations (6.8) – (6.10) which is then used to calculate the intrinsic transconductance  $g_m = \partial I_{DS} / \partial V_{GS} |_{V_{DS}=const}$  plotted in Figure 6.6 (b). The intrinsic transconductance, which is linearly dependent on  $\mu_{FE}$ , decreases as the NW diameter decreases. Moreover, the transconductance plot develops a plateau as the NW diameter is reduced. It is known that the surface Fermi energy in InAs is pinned in the conduction band<sup>18</sup> which causes the formation of a surface accumulation layer.<sup>19</sup> The transconductance thus is expected to peak at flat band voltages,  $V_{fb}$ , which

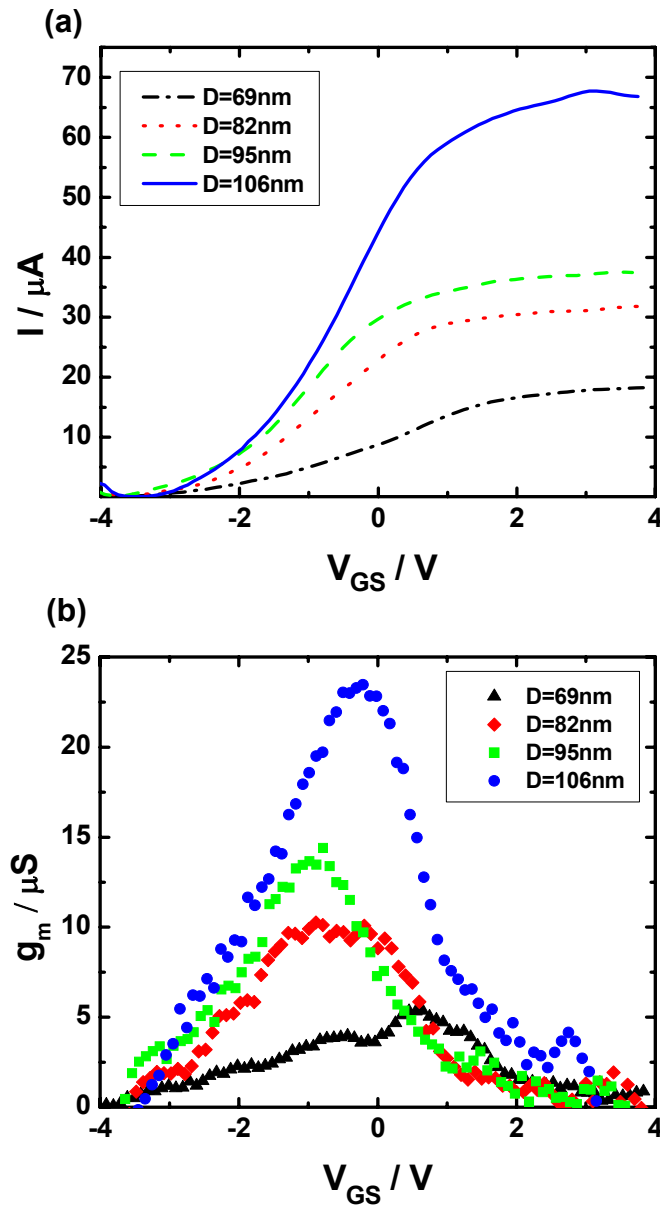


Figure 6.6. (a) Extracted transfer curves for a set of InAs NWs with different diameters at  $V_{DS}^0 = 0.5\text{ V}$  and (b) their corresponding transconductance as function of gate voltage.

are negative due to the presence of positively charged interface states, at which surface accumulation is eliminated.<sup>20</sup> In the depletion regime, at negative gate voltages relative to  $V_{fb}$ , coulomb scattering due to fixed oxide charges, interface state charges, and ionized impurity charges reduces  $\mu_{FE}$ .<sup>21</sup> Coulomb scattering is reduced in the accumulation



regime, at positive gate voltages relative to  $V_{fb}$ , due to screening from accumulated electrons; However, surface scattering becomes dominant leading to reduced  $\mu_{FE}$ .<sup>22,23</sup> As the NW diameter is reduced, surface-like transport coefficients dominate the transport properties of the InAs NW due to carrier transport predominantly in a surface-like region, and strong peaking in the transconductance is less likely to occur, which is clearly evident in Figure 6.6 (b). This is consistent with variation of transport properties for InAs epitaxial layers with different thicknesses where the bulk contribution to the mobility decreases as the thickness of the InAs layer decreases.<sup>24</sup>

For the NW lengths used in this study ( $L_{SD}=3 - 4 \mu\text{m}$ ,  $L_G \approx 1 \mu\text{m}$ ) ballistic effects can be neglected as the mean free path determined from scanned probe measurements above or estimated from the Fermi wave vector is consistently smaller than  $L_G$ . From the  $I$ - $V$  curves extracted using equations (6.8) – (6.10), one can therefore compute  $\mu_{FE}$  using

$$\mu_{FE} = g_m I_G^2 / C V_{DS} , \quad (6.11)$$

where  $C$  is the gate-to-channel capacitance and is equal to the oxide capacitance in the linear operating regime.<sup>25</sup> Note that equation (6.11) does not account for the effects of interface states and the associated interface state capacitance correction for  $C$  leading to an underestimation of  $\mu_{FE}$ . Also, prior measurements presented in chapter 5 have shown that apparent mobility values are highly dependent on the  $V_{GS}$  sweep rate and direction that allow different interface state dynamic charging and discharging, which leads to different  $C$ .<sup>26</sup> In order to minimize measurement artifacts, a fixed sweep rate of  $\sim 20$  mV/s was used in measuring all 26 devices in this study.

Figure 6.7 (a) shows a plot of the average values of calculated  $\mu_{FE}$  vs. NW diameter computed from extracted  $I$ - $V$  characteristics and accounting for parasitic

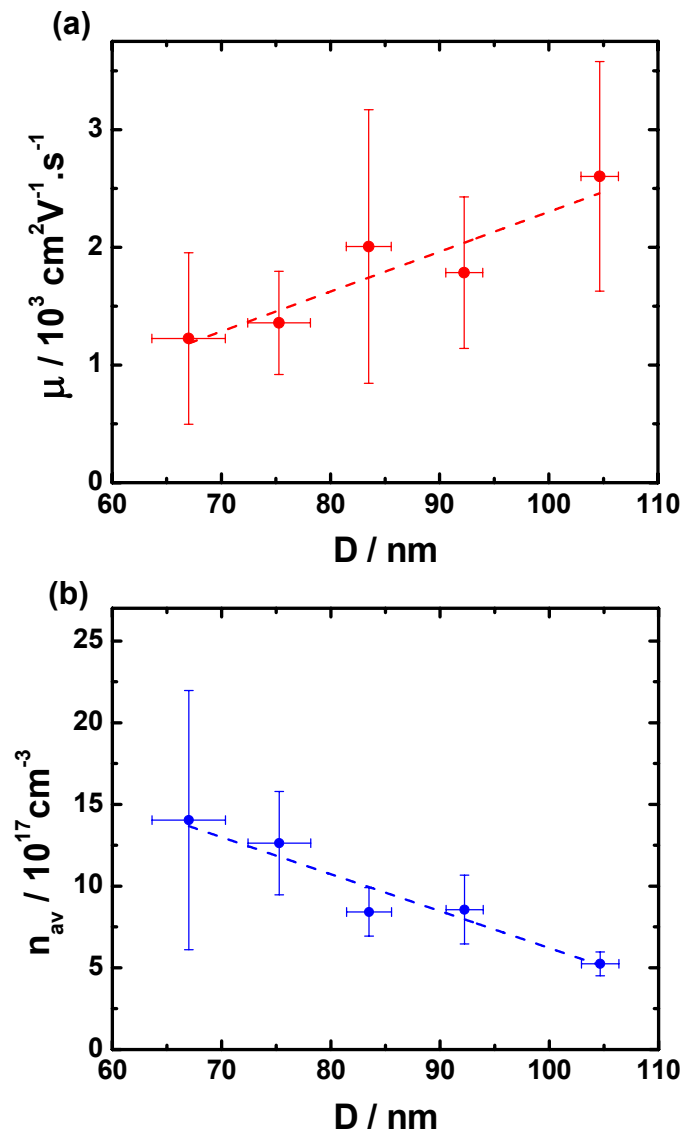


Figure 6.7. (a) Measured field effect mobility and (b) measured average carrier density as function of InAs NW diameter. Dashed lines are linear fits with statistical weighting for both sets of data.

resistances of each device depending on its particular geometry for all 26 devices. From the extracted  $I$ - $V$  characteristics, and for fair comparison between different NW diameters,  $\mu_{FE}$  was calculated according to equation (6.11) at constant  $V_{GS}=0$  V and constant  $V_{DS}=0.15$  V. These values of  $V_{GS}$  and  $V_{DS}$  are used for consistency in comparison

and do not reflect the highest value of  $\mu_{FE}$  that can be obtained in each NW. Specifically, it can be seen from Figure 6.5 (b) that  $V_{GS}=0$  V does not necessarily result in the highest obtained transconductance, and consequently the highest  $\mu_{FE}$ , in each device. The low  $V_{DS}$  value chosen here lies within the linear biasing regime where the  $\mu_{FE}$  is constant and is the low-field mobility. It is evident from Figure 6.7 (a) that  $\mu_{FE}$  decreases as the NW diameter decreases, consistent with enhanced surface scattering in smaller diameter NWs. This is also in agreement with recent mobility-diameter dependence studies in GaN NWs obtained from back-gate geometry by Motayed et al.<sup>6</sup>

Another important transport coefficient is the carrier concentration dependence on NW diameter which can be computed, again at the same fields for fair comparison, according to

$$n_{av} = I_{DS} L_G / q \mu_{FE} V_{DS} A. \quad (6.12)$$

Figure 6.7 (b) shows a plot of computed  $n_{av}$  for different NW diameters showing an increase in  $n_{av}$  as the NW diameter decreases. This is due to the presence of an accumulation layer at the InAs surface whose relative contribution to  $n_{av}$  increases as the NW diameter decreases. If the Fermi energy were pinned in the band-gap at the NW surface, reduction of  $n_{av}$  or  $p_{av}$  as the NW diameter decreases is expected (eg. in Si NWs),<sup>3</sup> where  $p_{av}$  is the average hole concentration in a p-type NW. In InAs NWs, reduction of the interface states through proper surface passivation or forming core-shell heterostructures may lead to unpinning of the Fermi energy in the conduction band and reduction of its detrimental effects on electron mobility.<sup>27</sup>

To validate the observed  $\mu_{FE}$  and  $n_{av}$  dependence on NW diameter, numerical simulation using Silvaco, Atlas in 1D is used. For the NW diameters used in this study

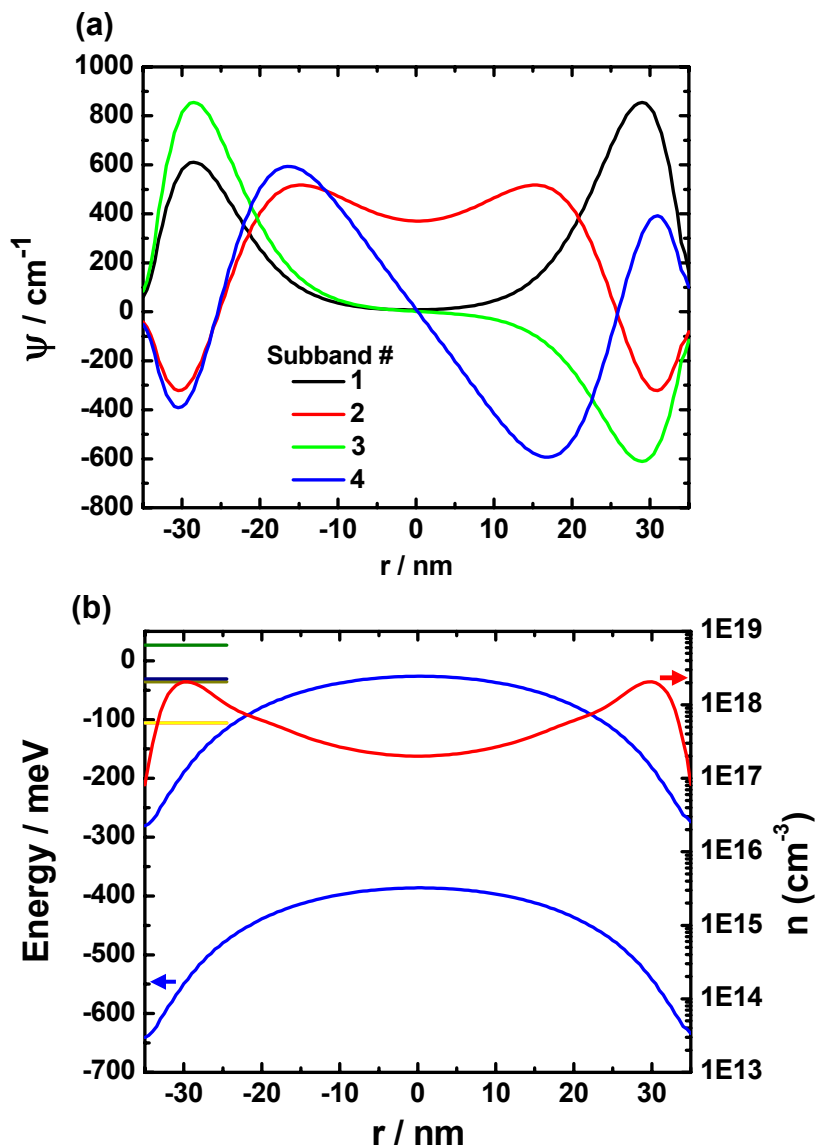


Figure 6.8. 1D Schrödinger-Poisson solution for a 70nm-thick InAs slab in the presence of  $Q_f/q=2.7 \times 10^{12} \text{ cm}^{-2}$  surface fixed charge density. (a) Distribution of first four subband wavefunctions across the slab thickness, (b) energy-band diagram across the slab thickness showing strong surface Fermi Energy pinning in conduction band together with electron accumulation. The first few subband energies are shown to the top left.

and due to their cylindrical symmetry, 1D Schrödinger-Poisson solutions for electron wavefunctions, energy bands, and electron distribution in InAs slabs are close to the exact solutions in cylindrical coordinates.<sup>28</sup> A material stack similar to that used in the

actual NWFET device was employed to perform the simulations. In order to account for the presence of surface states at the oxide-InAs interface, a fixed positive interface charge density of  $2.7 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$  and a bulk carrier concentration of  $5 \times 10^{16} \text{ cm}^{-3}$  were used in order to match the simulated and the experimental extracted values. Figure 6.8 (a) shows the radial distribution of the first four electron wavefunctions in a 70 nm thick InAs slab at  $V_{GS}=0 \text{ V}$ . Note that this distribution is different from that in Figure 6.3 (a) which assumed infinite potential well case. The positive surface potential due to the fixed interface charges pulls the electron wavefunction peaks toward the surface of the InAs slab. The first four subband energies and the energy band-edge profiles across the slab thickness are plotted in Figure 6.8 (b) showing  $\sim 270 \text{ meV}$  band bending at the slab surface due to the presence of interface charges. Figure 6.8 (b) also shows a plot of the electron distribution across the slab thickness illustrating peaking in the electron distribution near the surface of the NW.

Figure 6.9 (a) shows calculated electron concentration distribution for different InAs slab thicknesses with the same background doping and fixed charge density of  $5 \times 10^{16} \text{ cm}^{-3}$  and  $2.7 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ , respectively. The electron concentration peaks for thinner slabs are higher than those for thicker slabs, due to the dominance of accumulation electrons in thinner slabs. The average carrier concentration for a single NW diameter can be obtained using

$$n_{av} = \frac{2\pi \int_0^R nrdr}{\pi R^2}. \quad (6.13)$$

Figure 6.9 (b) shows a plot of the average carrier concentration for different NW

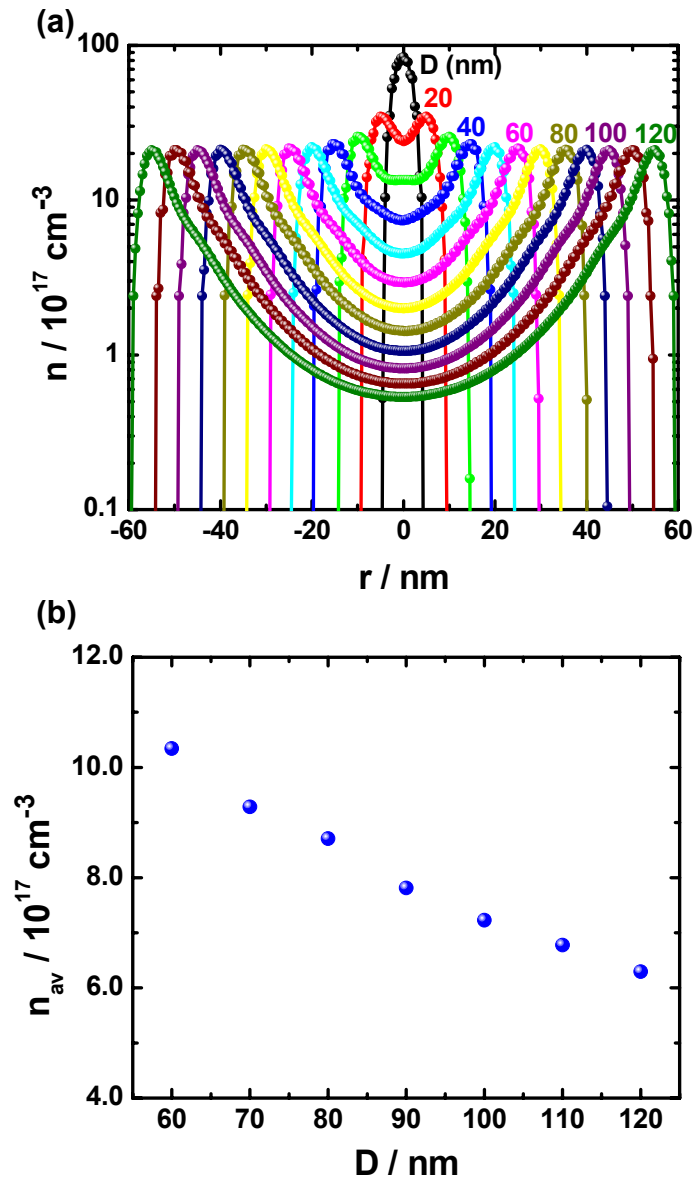


Figure 6.9. (a) Plot of the free carrier distribution along the channel for different NW diameter obtained by Schrödinger-Poisson solver in 1D. (b) Average NW carrier density obtained from (a) by integrating across the radial direction and dividing by the NW area.

diameters showing an increase in the computed  $n_{av}$  as the NW diameter decreases. This trend is consistent with the experimental extracted  $n_{av}$  from the InAs NWFETs. Smaller diameter NWs are thus dominated by accumulation electrons that encounter enhanced

surface scattering. The numerical simulations thus support the experimental observation in  $\mu_{FE}$  reduction and  $n_{av}$  increase with decreasing NW diameter.

## 6.6 Conclusions

In this chapter, we have presented direct experimental measure of distances over which ballistic or quasi-ballistic electron transport in InAs NWs prevail using conductive atomic force microscopy. For electron transport distances  $L$  within the nanowire of  $\sim 200$ nm or less, the nanowire resistance is observed to be nearly independent of  $L$ , while for larger transport distances the resistance increases approximately linearly with  $L$ . These observations suggest that for transport distances of  $\sim 200$  nm or less, transport is ballistic or nearly ballistic, while for larger distances scattering-induced resistivity eventually dominates and the resistance increases linearly with distance. Model calculations of carrier transmission and total resistance in the nearly ballistic regime, for which the number of scattering events is small and assumed to obey a Poisson distribution, confirm that for distances up to a few mean free paths the resistance should increase much more slowly with  $L$  than in the drift transport regime. Calculations of electronic subband structure within the InAs nanowire combined with experimentally determined mobilities, resistance, and carrier concentrations yield, for a variety of approaches, a mean free path of  $\sim 55$  nm, which is very consistent with our experimental observations of resistance as a function of transport distance and analysis of transport in the quasi-ballistic regime. Also, we have extracted the diameter dependent transport coefficients in InAs NWs at equal vertical and lateral fields and at equal  $V_{GS}$  sweep rate

for consistent comparison. Smaller diameter NWs were found to have lower  $\mu_{FE}$  and higher  $n_{av}$  due to the presence of an electron surface accumulation layer that increases the effect of surface scattering. For larger diameter wires, bulk-like transport properties lead to higher  $\mu_{FE}$  values and lower  $n_{av}$ . Numerical simulations with a 1D Schrödinger-Poisson solver support the presence of the electron accumulation layer near the positive interface state charges that lead to the observed trends in the transport coefficients of the InAs NWs. We believe that the latter comprehensive extraction technique of the NW transport properties as function of diameter enables fair and more accurate assessment of the transport properties of NWFETs.

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## 7. ROOM TEMPERATURE TRANSPORT PROPERTIES OF ZINCBLLENDE AND WURTZITE INDIUM ARSENIDE NANOWIRES

### 7.1 Introduction

The Vapor-Liquid-Solid growth of semiconductor nanowires (NWs) has enabled realization of engineered electronic and optoelectronic one-dimensional nanostructures with outstanding promise for device applications.<sup>1,2,3,4</sup> Realization of this promise requires understanding of their growth mechanism,<sup>5,6,7,8,9,10</sup> crystal structure,<sup>11,12</sup> and carrier transport behavior.<sup>13,14,15,16,17,18</sup> Understanding the relationships between these NW properties is vital to exploiting their full potential for reliable and reproducible device characteristics. This is particularly important for III-V compound semiconductor NWs for which wurtzite (WZ) /zincblende (ZB) polymorph crystal structures are observed with various growth techniques.<sup>19,20,21,22,23,24,25</sup>

Although Takahashi and Muriizumi have shown through x-ray diffraction (XRD) analysis in 1966 that InAs NWs grown using chemical vapor deposition at 400 °C have WZ crystal structure, Koguchi et al.<sup>20</sup> and Yazawa et al.<sup>21</sup> were the first to study the details of the InAs and GaAs NW crystal structure through cross-sectional transmission electron microscope (TEM), XRD, and high resolution TEM. Their studies indicated that InAs NWs grown at temperatures greater than 400 °C exhibit the WZ crystal structure with large density of twinning or stacking faults perpendicular to their growth direction. Since the (111) planes have the lowest surface energies among all planes, NWs typically grow in the <111> direction. In addition, both WZ and ZB InAs have similar bond

lengths and system energies.<sup>26</sup> Thus, a simple rotation of the third nearest neighbors in the (111) plane changes the crystal structure from ZB with ABCA layer stacking to WZ with ABAB layer stacking. (See Figure 3.19).

In similar arguments to Hurlé, who modeled the formation of twinned bulk III-V semiconductors in 1995,<sup>27</sup> Glas et al. suggested in 2007 that the surface energies of the NW facets may lead to preferential nucleation at triple phase interfaces which may favor the formation of WZ NWs for III-V semiconductors at high super-saturations.<sup>28</sup> However, there is no unique model that explains the polymorphism in III-V NWs grown using different growth systems and conditions. For instance, GaAs NWs grown using molecular beam epitaxy at 590 °C by Harmand et al.<sup>6</sup>, which formed the basis for Glas et al.'s model,<sup>28</sup> have shown WZ crystal structure, while GaAs NWs grown using OMVPE in our lab have shown ZB crystal structure over a temperature range of ~ 400 – 500 °C exhibited ZB crystal structure.<sup>29</sup> For InAs NWs, ZB crystal structure has been observed for a growth temperature of 350 °C or less,<sup>17,22,30</sup> whereas growth temperatures of 390 °C or above resulted in mainly WZ InAs NWs with stacking faults and ZB segments.<sup>19,22,31,32</sup>

Despite the clear differences in crystal structure, the effect of polymorphism and correlation of crystal structure with electronic and optoelectronic properties of NWs have received little attention. Jacobs et al. have correlated cathodoluminescence spectra of bi-phase crystalline WZ and ZB GaN NWs and deduced energy bandgaps of 3.64 eV and 3.88 eV for ZB and WZ segments, respectively.<sup>33</sup> In a related study of the transport properties and *in-situ* SEM breakdown characteristics of these bi-phase GaN NWs, Jacobs et al. suggested that the WZ phase is the current carrying portion of these NWs.<sup>34</sup> Bao et al. have recently correlated optical properties of rotationally twinned InP NWs

with their twinned crystal structure<sup>35</sup> based on the energy band-edge offsets of the WZ/ZB heterostructure interface.<sup>36</sup> The blue shift in the photoluminescence peaks as function of excitation energy for rotationally twinned InP NWs was related to the staggered heterostructure of the WZ/ZB heterointerface; no such shift was observed for pure ZB InP NWs.<sup>35</sup> In parallel with these investigations, we have observed distinct subthreshold characteristics of twinned WZ and pure ZB InAs NWs. We attribute these effects to the presence of spontaneous polarization charges at the WZ/ZB heterointerface as discussed below.

## 7.2 Summary of Results

We report in this chapter direct correlation between the microstructure of InAs NWs and their individual electronic transport behavior at room temperature. Pure ZB InAs NWs grown on SiO<sub>2</sub>/Si substrates are characterized by a rotational twin along their growth-direction axis while WZ InAs NWs grown on InAs (111)B substrates have numerous stacking faults perpendicular to their growth-direction axis with small ZB segments. From transport measurements on back-gate field-effect transistors (FETs) fabricated from both types of NWs, we observe significantly distinct subthreshold characteristics ( $I_{on}/I_{off} \sim 2$  for ZB NWs and  $\sim 10^4$  for WZ NWs) despite only a slight difference in their transport coefficients. We attribute this difference to the presence of spontaneous polarization charges at the WZ/ZB interfaces that suppress carrier accumulation caused by interface charges at the NW surface, thus enabling to full depletion of the WZ NW FET channel. We have used two-dimensional Silvaco-Atlas

simulations for ZB and WZ channels to analyze subthreshold current flow and found that a polarization charge density  $\geq 10^{13} \text{ cm}^{-2}$  leads to good agreement with experimentally observed subthreshold characteristics for a WZ InAs NW in the presence of surface state densities in the  $5 \times 10^{11} - 5 \times 10^{12} \text{ cm}^{-2}$  range.

### 7.3 Experiment

The InAs NWs used for this study were grown in a home-built organo-metallic vapor phase epitaxy system utilizing Au colloids, tri-methyl-indium and arsine precursors in  $\text{H}_2$  carrier gas and 100 Torr chamber pressure. To obtain uniform NW morphology, the optimal growth conditions on  $\text{SiO}_2/\text{Si}$  substrate were found to be a substrate temperature of  $350^\circ\text{C}$  with a molar V/III ratio of 25 as demonstrated in chapter 2.<sup>37</sup> For a growth time of 15 min, the InAs NW diameters are in the range of 35 – 80 nm and their lengths exceed 10  $\mu\text{m}$ , making them suitable for fabricating long channel NWFETs for transport characterization. The structural properties of these NWs were characterized by a 200 KeV FEI Tecnai scanning transmission electron microscope (TEM). We found InAs NWs with diameters  $\geq 40$  nm have a grain boundary along their growth-direction axis and exhibit the ZB crystal structure and the [110] growth orientation. (See section 2.7).

The growth conditions and crystal structure of InAs NWs grown on InAs (111)B substrates are quite different from those on  $\text{SiO}_2/\text{Si}$  substrates. The optimal growth conditions to obtain uniform NWs on InAs (111)B substrates are a growth temperature of  $500^\circ\text{C}$  with  $\text{V/III} = 60$  as demonstrated in chapter 3.<sup>10</sup> These NWs are mostly WZ and have small ZB segments in addition to the presence of stacking faults perpendicular to the

growth-direction axis as well as twin boundaries separating small ZB sections. (See section 3.7).

The InAs NWs were suspended –separately– in ethanol solution by sonication, and consequently transferred onto a 100 nm SiO<sub>2</sub>/n<sup>+</sup>-Si(001) substrate for device fabrication. ZB or WZ InAs NWs were drop-cast on pre-defined grids – for NW positioning – that were patterned ~ 1 cm apart in order to maintain identical processing conditions for both types of devices and to minimize process induced artifacts. Electron-beam lithography was then used to define source-drain electrodes with variable spacing (0.7 - 5 μm) followed by e-beam evaporation and lift-off for 15 nm/85 nm Ti/Al contact electrodes. After transport measurements, device dimensions were measured using an FEI XL 30 Environmental Scanning Electron Microscope (ESEM) operating at 30 KV acceleration voltage for transport analysis.

#### 7.4 Experimental Results and Analysis

Figures 7.1 and 7.2 show the output and transfer curves, respectively, for back-gate ZB and WZ InAs NWFETs with equal source-drain separation  $L_{SD} = 3.4 \mu\text{m}$ . Inset of Figure 7.1 (a) shows a FE-SEM image of a representative back-gate InAs NWFET. Since the transport properties, and the extracted transport coefficients thereafter, can be influenced by surface states as demonstrated in chapter 5,<sup>38,39</sup> a constant  $V_{GS}$  sweep rate (50 mV/s) and direction (from -20 V to + 20 V) are used to measure all 17 devices discussed in this paper. From Figure 7.1 and 7.2, we can note the following: (i) The ZB NWs exhibit poor subthreshold characteristics with  $I_{on}/I_{off} < 2$  (Figure 7.2 (a)), whereas

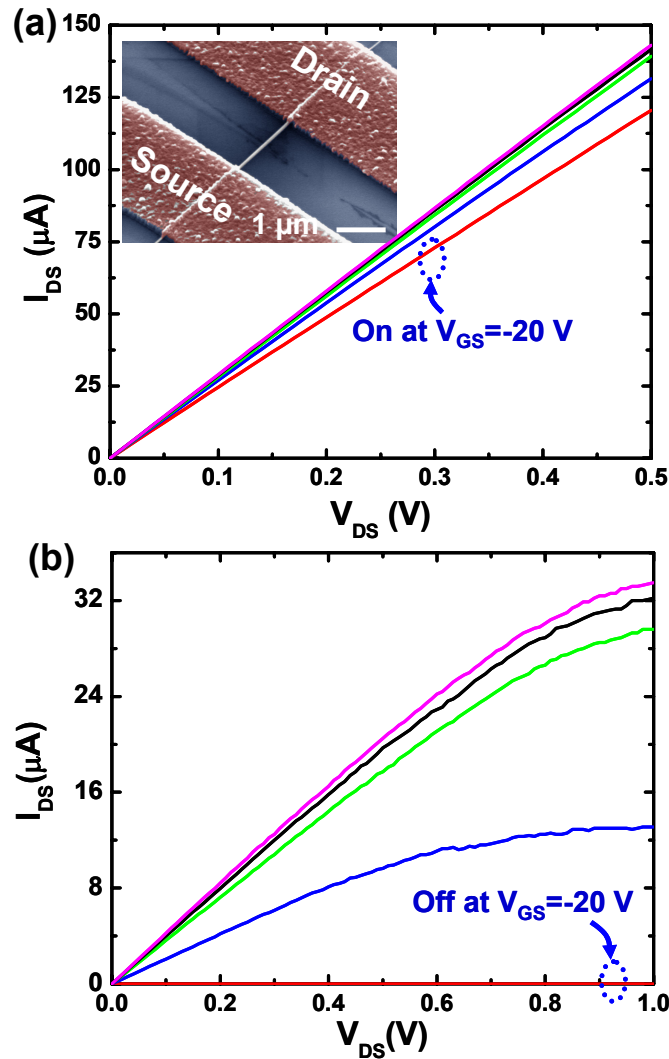


Figure 7.1. Output characteristics of long channel ( $L_{SD} = 3.4 \mu\text{m}$ ) back-gate InAs NW FETs ( $V_{GS} = -20$  V to +20 V in 10 V step) made from (a) ZB ( $D \sim 81$  nm) and (b) WZ ( $D \sim 60$  nm) InAs NWs. Inset to (a) is a false color SEM image of a representative back-gate NW FET device.

The WZ far better subthreshold characteristics with  $I_{on}/I_{off} \sim 10^4$  (Figure 7.2 (b)). (ii) The measured currents (and current densities) at the same  $V_{DS}$  and  $V_{GS}$  are larger by about one order of magnitude for the ZB NWFET when compared to that of the WZ NWFET (Figures 7.1 (a) and 7.1 (b)). This is due to differences in contact resistances ( $R_c$ ) extracted from the transmission line method as shown in Figure 7.4:  $R_c$  (ZB) = 1480  $\Omega$



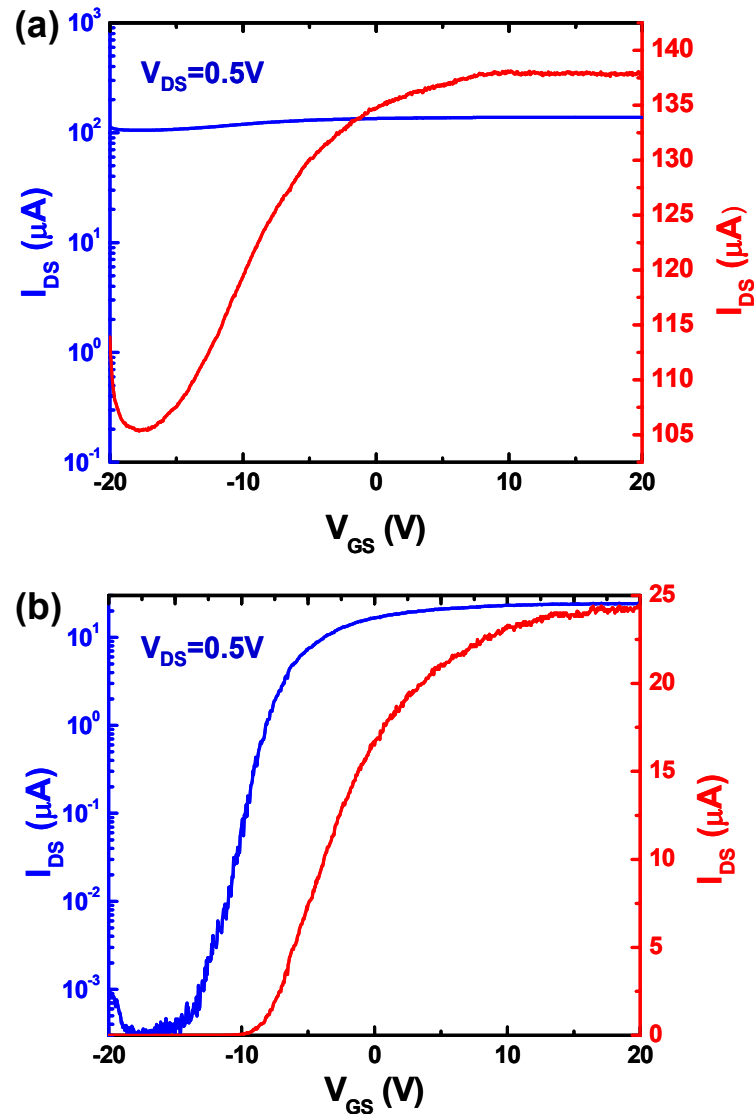


Figure 7.2. (a) Transfer characteristics of same ZB InAs NWFET device of Figure 7.1 (a) showing  $I_{on}/I_{off} < 2$  at  $V_{DS} = 0.5$  V, and (b) transfer characteristics of same WZ InAs NWFET device of Figure 7.1 (b) showing  $I_{on}/I_{off} > 10^4$  at  $V_{DS} = 0.5$  V.

whereas  $R_c$  (WZ) = 11280  $\Omega$ . TEM analysis indicates a thicker  $\text{In}_2\text{O}_3$  layer for the WZ NWs. Here, both types of wires (which are fabricated on the same chip) were dipped in concentrated buffered oxide etch (49%) for 15 seconds. (iii) Both types of NWFETs show an increase in the current at negative  $V_{GS}$ , below threshold voltage,  $V_t$ , owing to long surface state trapping/de-trapping time constants (on the order of tens of seconds)<sup>39</sup>

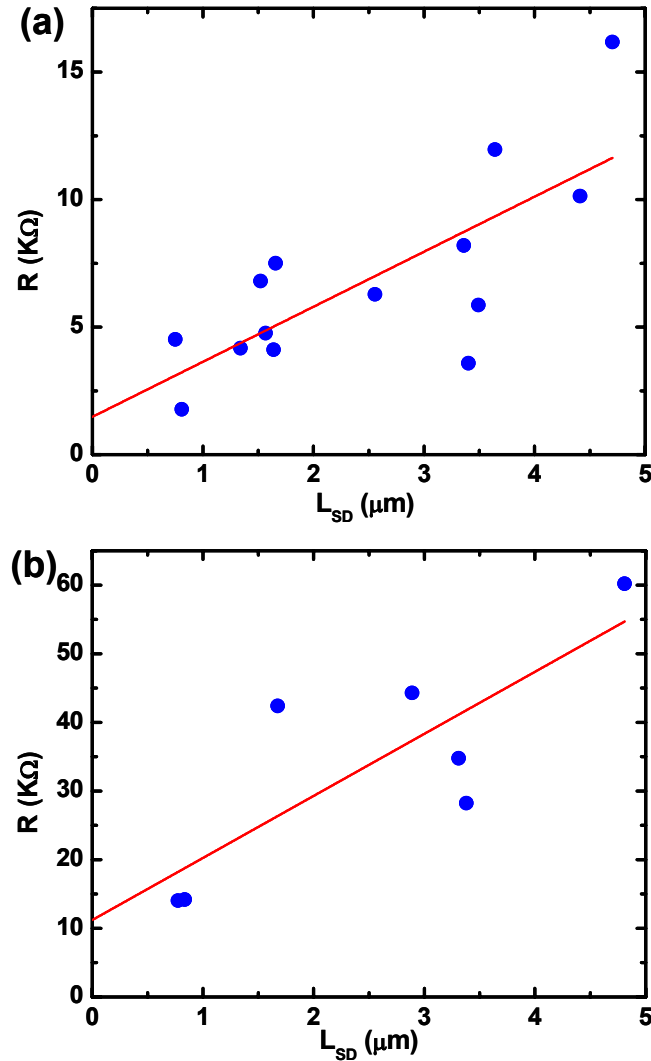


Figure 7.3. Plot of the NW resistance as function of NW length for (a) ZB and (b) WZ/ZB NW devices used to extract the contact resistance ( $R_c[110] = 1480 \Omega$  and  $R_c[0001] = 11280 \Omega$ ).

and ambipolar transport. These trends are observed for all NWFET diameters and lengths. As the channel length decreases, the gate transconductance, as expected, decreases as a function of  $1/L_{SD}$  as shown in Figure 7.4 and the  $I_{on}/I_{off}$  ratio is significantly reduced for WZ NWs. Figure 7.5 shows the output and transfer curves of a relatively short channel WZ InAs NWFET with  $L_{SD} = 835 \text{ nm}$ , determined from high

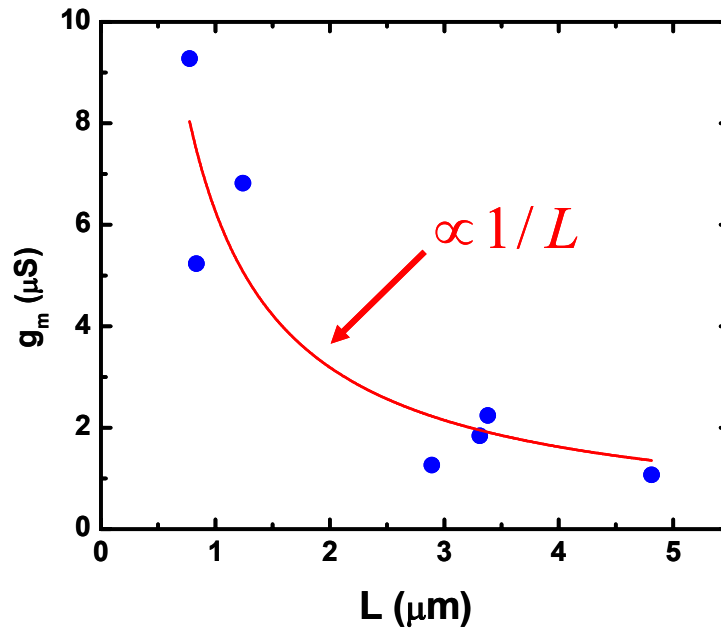


Figure 7.4. Plot of the extrinsic transconductance as function of gate length for the WZ InAs NWs showing  $1/L$  dependence.

magnification FE-SEM images after transport measurements. The output curves in Figure 7.5 (a) show breakdown characteristics, attributed to impact ionization,<sup>40</sup> for high  $V_{DS}$  values of a few hundred mV. The transfer curves in Figure 7.5 (b) show lower  $I_{on}/I_{off}$  ( $\sim 10$ ) when compared to the long channel case (Figure 7.2 (b)) due to short channel effects, which become severe at  $L_{SD} \sim 1 \mu\text{m}$  for this device structure under ideal conditions i.e. without taking into account interface state capacitance.<sup>41</sup> Here,  $L_{SD}$  is less than  $2(\epsilon_{InAs}/\epsilon_{SiO2} \cdot t_{ox} + D_{NW}) \sim 1 \mu\text{m}$  indicating that short channel effects are severe for this device;  $\epsilon$  is the dielectric constant,  $t_{ox}$  is the oxide thickness,  $D_{NW}$  is the NW diameter. In order to calculate the transport coefficients of these devices, we have to extract the intrinsic output and transfer curves by taking into account the series and leakage resistances. This is done based on a simple DC equivalent model that is discussed in

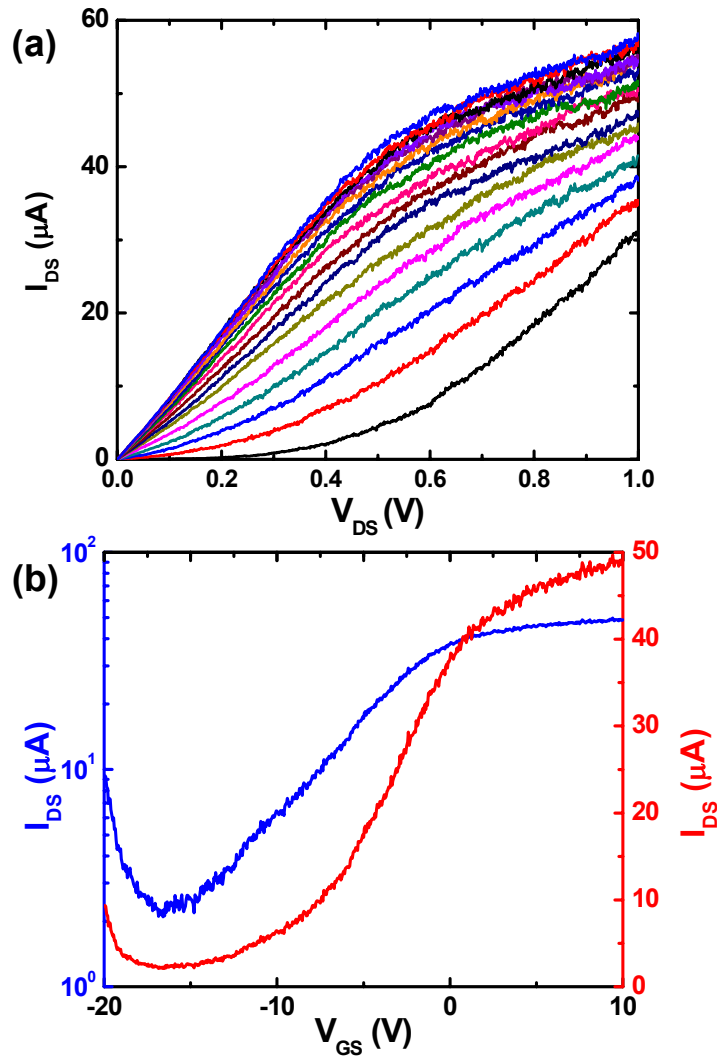


Figure 7.5. (a) Output characteristics of relatively short channel back-gate WZ InAs NWFET with  $L_{SD} \sim 835$  nm and  $D \sim 57$  nm; ( $V_{GS} = -20$  V to +20 V in 2.5 V step). (b) Transfer characteristics of same NW in (a) showing  $I_{on}/I_{off} < 10^2$  at  $V_{DS} = 0.5$  V.

detail in chapter 4. Here, the series resistance at the source (and drain) side is  $R_c/2$ . The leakage resistance is calculated from the output and transfer curves for each of the 17 devices under consideration. The leakage resistance  $R_{leak}$  is calculated from the output and transfer curves for each of the 17 devices under consideration ( $R_{leak} \sim 5 \times 10^3 \Omega - 10^5 \Omega$  for ZB NWs and  $2 \times 10^5 \Omega - 2 \times 10^9 \Omega$  for WZ NWs). These values are dictated by the

Table 7.1. Device dimensions and extracted transport coefficients for the ZB InAs NWFET devices:

Device	L $\mu\text{m}$	D nm	R K $\Omega$	$g_m$ $\mu\text{S}$	$\mu$ $\text{cm}^2/\text{V}\cdot\text{s}$	n $\text{cm}^{-3}$
D3	4.4	72	10.1	1.5	1610	$6.8 \times 10^{17}$
D7	3.6	53	12.0	1.8	1730	$1.1 \times 10^{17}$
D4	3.5	67	58.7	1.2	1360	$6.4 \times 10^{17}$
D18	3.4	81	35.9	2.8	4010	$4.1 \times 10^{17}$
D15	3.4	52	82.2	5.1	4630	$7.1 \times 10^{17}$
D14	1.7	38	27.1	2.7	1460	$1.5 \times 10^{18}$
D10	1.6	62	7.5	8.8	500	$3.5 \times 10^{17}$
D5	1.6	74	4.1	4.3	2400	$6.0 \times 10^{17}$
D13	1.5	97	6.8	3.2	1650	$7.4 \times 10^{16}$
D8	0.75	56	4.5	8.1	2600	$1.3 \times 10^{18}$

Table 7.2. Device dimensions and extracted transport coefficients for the WZ InAs NWFET devices:

Device	L $\mu\text{m}$	D nm	R K $\Omega$	$g_m$ $\mu\text{S}$	$\mu$ $\text{cm}^2/\text{V}\cdot\text{s}$	n $\text{cm}^{-3}$
C6	4.8	41	60.2	1.0	1330	$1.7 \times 10^{18}$
C1	3.4	61	28.2	2.2	1980	$8.6 \times 10^{17}$
C7	3.3	61	34.8	1.8	1350	$3.8 \times 10^{17}$
C5	2.9	51	44.3	1.2	880	$1.2 \times 10^{18}$
C4	1.2	53	60.2	5.4	2350	$3.3 \times 10^{17}$
C8	0.8	57	14.2	4.2	2120	$1.0 \times 10^{18}$
C2	0.7	45	14	8.4	1990	$4.1 \times 10^{17}$

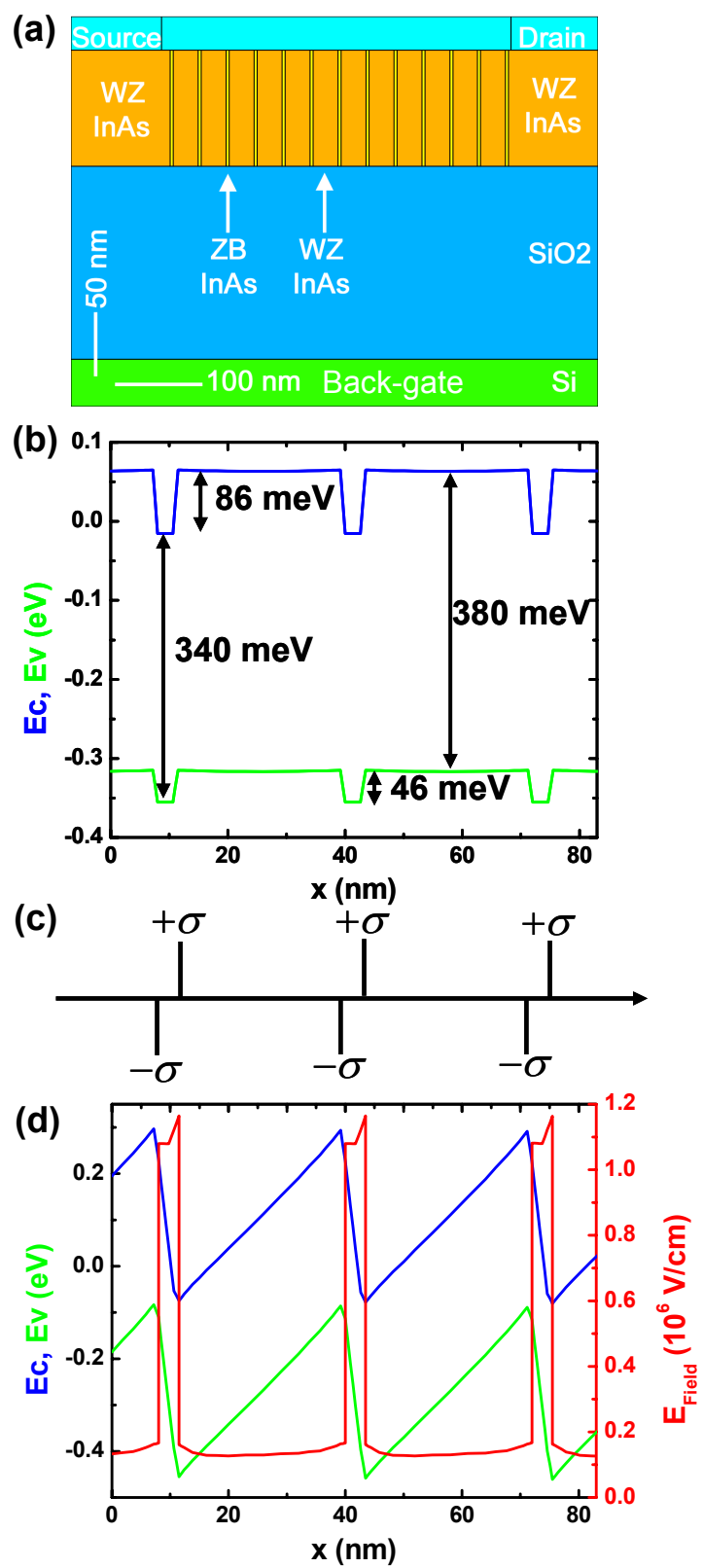
high  $I_{off}$  value for the ZB NWFET and the low one for the WZ NWFET. Tables 7.1 and 7.2 summarize the NWFETs device dimensions, measured resistance and transconductance, and extracted mobility and carrier concentration for all 17 ZB and WZ devices. The average values of the free carrier concentration and mobility are:  $n_{av}(\text{ZB}) = 6.4 \times 10^{17} \text{ cm}^{-3}$ ,  $n_{av}(\text{WZ}) = 8.5 \times 10^{17} \text{ cm}^{-3}$ ,  $\mu_{av}(\text{ZB}) = 2200 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $\mu_{av}(\text{WZ}) = 1700 \text{ cm}^2/\text{V}\cdot\text{s}$ . The slight difference in the mobility values and carrier concentration cannot explain the distinct subthreshold characteristics of the ZB and WZ NWFETs.

To explain these behaviors, we turn instead to the electronic structure of the WZ/ZB InAs interface. For bulk InAs, the band offsets are  $\Delta E_c = 86$  meV for the conduction band and  $\Delta E_v = 46$  meV for the valence band with staggered band-edge alignment at the WZ/ZB heterointerface.<sup>36</sup> Photoluminescence measurements on InAs-InP core-shell NWs<sup>42</sup> and InAs<sub>x</sub>P<sub>1-x</sub> NWs<sup>32</sup> indicate an energy bandgap increase of  $\sim 150$  meV (without subtracting strain-induced band shift) and  $\sim 120$  meV (by extrapolation to pure InAs), respectively. Theoretical predictions of the bandgap increase in WZ with respect to ZB InAs NWs suggest a lower value of  $\sim 55$  meV, which is close to that calculated for bulk InAs.<sup>36</sup> In this work, we assume bulk band-edge offsets as input parameters to a 2D Silvaco-Atlas simulator for calculating the current voltage characteristics of device structures with similar material compositions and thicknesses to those used in experiment.

### 7.5 2D Simulation of ZB and WZ InAs NWFETs

Figure 7.6 (a) shows the device structure used in the 2D simulations which consists of a highly doped n-type Si substrate, used as back-gate, a 100 nm thick SiO<sub>2</sub> layer, and an InAs channel with Ti/Al source-drain electrodes. The device shown in Figure 7.6 (a) represents the twinned WZ/ZB NWs with a 3.5 nm ZB section inserted every 28.5 nm of WZ sections, which was found as an average value over the entire length of the WZ NWs from the TEM studies. For simulation accuracy, the x-mesh spacing used was 0.8 Å in the ZB segments and 6 Å in the WZ segments restricting the channel length to a maximum of 400 nm. The energy bandgaps and electron affinities are adjusted such that the band offsets in the WZ/ZB heterointerfaces are equal to those of

Figure 7.6. (a) Device structure used for 2D Silvaco-Atlas simulation showing 3.5 nm ZB sections inserted every 28.5 nm WZ section based on HRTEM of Figure 3 (d) with a total  $L_{SD} = 400$  nm. (b) Energy band-edge profile of a small section along the channel length plotted at thermal equilibrium showing band-edge discontinuity and alignment at the WZ/ZB interface in the absence of interface charges. (c) Spontaneous polarization charge distribution at the WZ/ZB heterointerface. (d) Energy-band profile and electric field for the same section in (b) plotted in the presence of  $10^{13}$  cm<sup>-2</sup> spontaneous polarization charges.





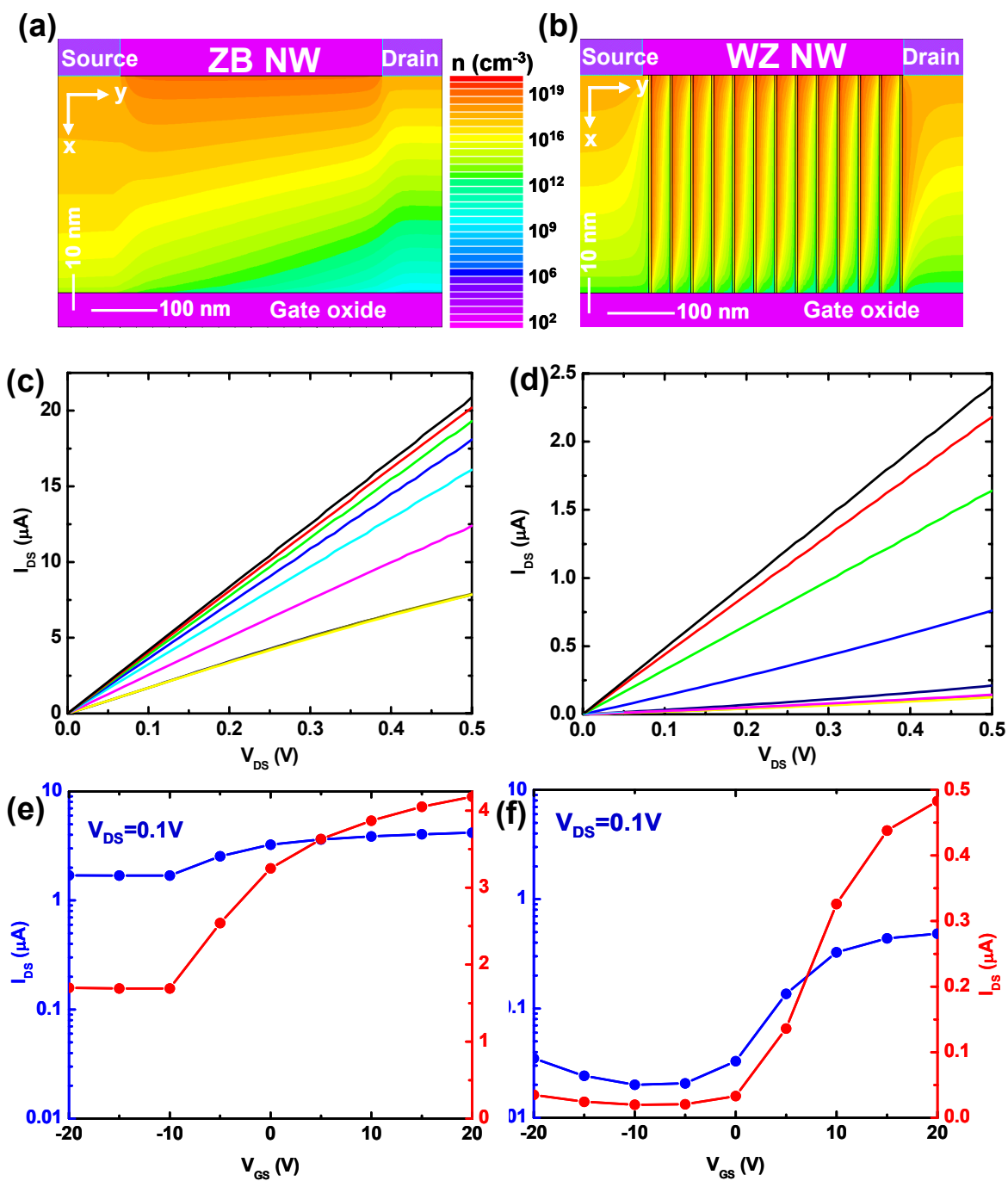
the bulk as depicted in Figure 7.6 (b).<sup>36</sup> The mobilities and contact resistances that were calculated in the experiment were input to the simulator in the case of pure ZB and WZ/ZB channels. A doping density of  $5 \times 10^{16} \text{ cm}^{-3}$  and donor-type<sup>43</sup> surface state density (fixed positive charges) of  $\sim 10^{12} \text{ cm}^{-2}$  were used to result in free carrier concentration similar to those extracted from experiments.<sup>44</sup> Large band offsets such as in the case of InAs NWs with InP segments inserted along their axis have led previously to improved subthreshold characteristics over those of homogenous InAs NWs.<sup>45</sup> Carrying out  $I$ - $V$  simulations for the device shown in Figure 7.6 (a) with these input parameters discussed above (including WZ/ZB band offsets) resulted in similar subthreshold characteristics to those of the pure ZB case. The band offsets for the WZ/ZB channel did not result in enhanced turn off characteristics similar to those obtained in experiment. Thus, band offsets alone can not explain the significant difference in the subthreshold characteristics between the ZB and the WZ/ZB NWs.

It is known that hexagonal crystals have non-zero spontaneous polarization that will lead to polarization fields and charges at the opposite  $\{0001\}$  faces of the crystal<sup>46</sup> as shown schematically in Figure 7.6 (c). Such polarization charges have not been considered before in the context of WZ III-V NWs. The presence of these spontaneous polarization charges, which are in the form of sheet charges perpendicular to the direction of current flow, will lead to electric field modulation across the channel length, in the absence (or presence) of any applied external fields. The negative polarization charges will compensate the positive ones that are induced by surface states, which typically result in electron accumulation at the InAs surface.<sup>47</sup> Figure 7.6 (d) shows a simulated plot of the field and energy band-edge profiles at thermal equilibrium for the device

structure in 7.6 (a) and in the presence of polarization charges at the WZ/ZB heterointerfaces that lead to accumulation and depletion at the opposite faces of the WZ crystals. The spontaneous polarization charge density for WZ InAs has not been calculated before. For hexagonal crystals such as GaN, AlN, InN, and ZnO, the spontaneous polarization charges are  $1.81 \times 10^{13} \text{ cm}^{-2}$ ,  $5 \times 10^{13} \text{ cm}^{-2}$ ,  $2 \times 10^{12} \text{ cm}^{-3}$ , and  $3.56 \times 10^{12} \text{ cm}^{-2}$ , respectively, all of which are comparable to  $10^{13} \text{ cm}^{-2}$ .<sup>48</sup> Therefore, we assume here a lower bound of  $10^{13} \text{ cm}^{-2}$  spontaneous polarization charge density for InAs, which was introduced at the edges of the WZ/ZB segments of the channel in the following simulations.

Figure 7.7 (a) and (b) show contour plots of the free carrier concentration in the ZB and WZ back-gate InAs NWFETs, which were obtained at  $V_{GS} = -20 \text{ V}$ ,  $V_{DS} = 0.5 \text{ V}$ , surface state density of  $10^{12} \text{ cm}^{-2}$  for both cases, and spontaneous polarization charge of  $10^{13} \text{ cm}^{-2}$  for the WZ/ZB channel. The top-portion of the ZB channel still shows electron accumulation, whereas field modulation due to the presence of spontaneous polarization charges in the WZ/ZB case leads to depletion that penetrates throughout the body of the channel. Figures 7.7 (c) – (f) show the output and transfer curves (at  $V_{DS} = 0.1 \text{ V}$ ) for both device structures. Similar trends to those obtained in experiment were reproduced in these simulations. Specifically, it can be seen that the ZB channel results in poor subthreshold characteristics and the WZ channel results in  $I_{on}/I_{off} > 10$ , which is consistent with that obtained experimentally for the short channel InAs NWFET case shown in Figure 7.7 (b). The current increase for negative  $V_{GS}$  below  $V_t$  is due to hole inversion at the gate side of the channel that results in ambipolar transport (transient

Figure 7.7. 2D simulation results showing contour plots of carrier concentration across the length and depth of an InAs slab with (a) pure ZB device and (b) WZ/ZB InAs heterostructure device. The contour plots are extracted at  $V_{DS} = 0.5$  V and  $V_{GS} = -20$  V showing stronger depletion in (b) penetrating deeper across the channel body. Output characteristics for (c) ZB devices and (d) WZ/ZB devices with  $V_{GS} = -20$  V to +20 V in +5 V step size. Transfer characteristics at  $V_{DS} = 0.1$  V for (e) ZB devices and (f) WZ/ZB devices. The trends observed in the output and transfer curves are similar to those measured on the fabricated FETs showing stronger depletion for the WZ devices with ZB segments inserted across the channel length. The current was normalized to a  $60 \times 60$  nm<sup>2</sup> slab with  $L_{SD} = 400$  nm.



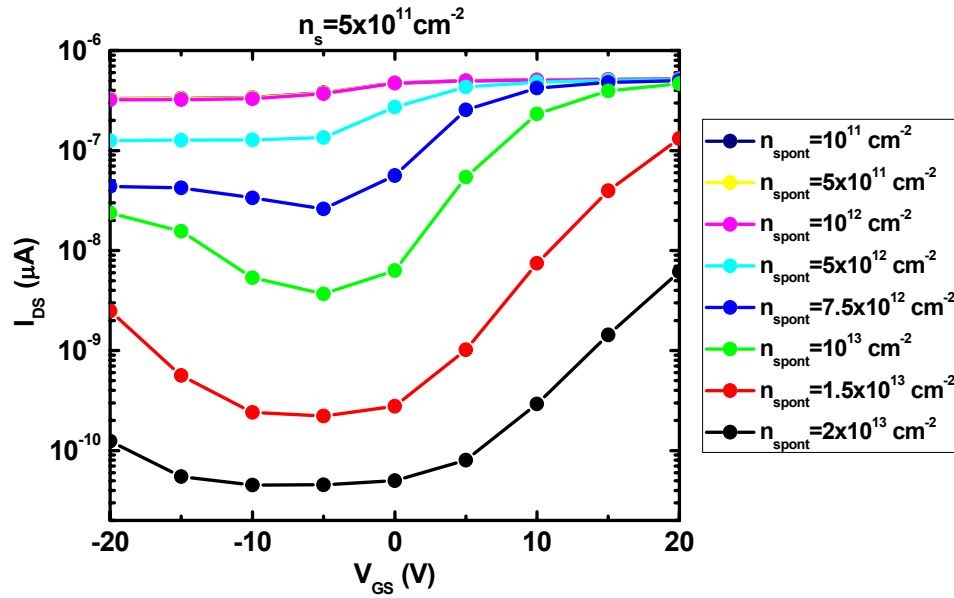


Figure 7.8. Simulation of the transfer curves for a WZ-ZB InAs NWFET of the same structure in Figures 7.6 (a) and 7.7 (b) at a constant surface state density of  $5 \times 10^{11} \text{ cm}^{-2}$  and different polarization charges of  $10^{11} - 2 \times 10^{13} \text{ cm}^{-2}$ .

effects are not considered in these simulations). The lower current values in the simulations for both ZB and WZ/ZB channels are most likely due to the underestimated mobilities in our measurements<sup>38</sup> and the different geometry between both. Nonetheless, the experimentally observed trends in the subthreshold characteristics are reproduced in simulation when the effect of spontaneous polarization charges is taken into account.

The spontaneous polarization charge density that was used in the simulations discussed above is  $10^{13} \text{ cm}^{-2}$ . To obtain a better understanding of what polarization charge density is required to deplete the InAs channel in the WZ/ZB NW, we have performed a set of simulations to calculate the  $I_{on}/I_{off}$  ratio by changing the surface state density in the range of  $10^{11} - 5 \times 10^{12} \text{ cm}^{-2}$  and assuming spontaneous polarization density of  $5 \times 10^{11} - 10^{14} \text{ cm}^{-2}$ . This is done again for a back-gate 400 nm InAs channel with 100 nm

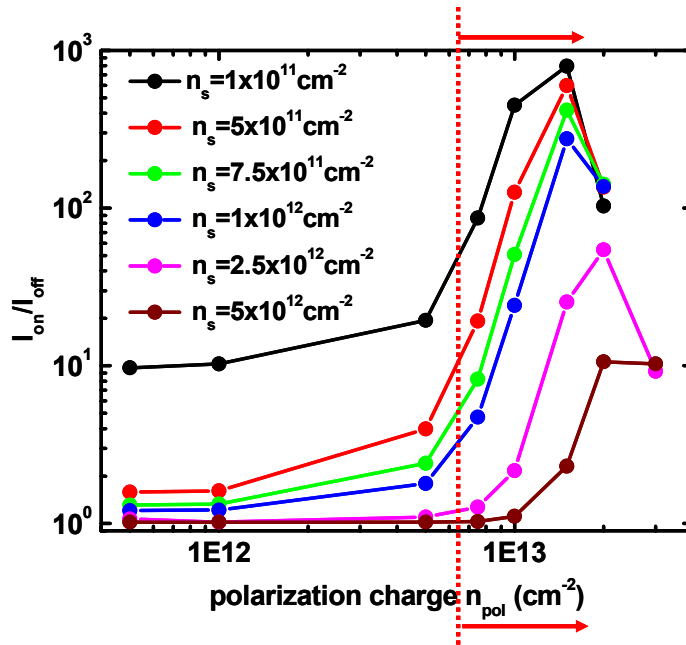


Figure 7.9. Plot of  $I_{on}/I_{off}$  as function of polarization charges at the WZ/ZB heterostructure for different surface-state (fixed positive charge) density simulated for a  $V_{DS} = 0.1$  V. A polarization charge density of  $\sim 10^{13}$   $\text{cm}^{-2}$  or higher is required to obtain strong current/carrier modulation in the channel for reasonable values of surface state densities.

thick  $\text{SiO}_2$  layer. One set of these simulations for a fixed surface state density of  $5 \times 10^{11}$   $\text{cm}^{-3}$  and variable polarization charge density is shown in Figure 7.8. It can be seen from Figure 7.8 that: (i) The  $I_{on}/I_{off}$  increases as the polarization charge increases with a shift in the threshold voltage toward positive values as  $n_{spont}$  increases. (ii) For  $n_{spont}$  of  $1.5$  and  $2 \times 10^{13}$   $\text{cm}^{-2}$ , the on current values drops when compared to  $n_{spont} \leq 10^{13}$   $\text{cm}^{-2}$ . At high  $n_{spont}$  of  $4 \times 10^{13}$   $\text{cm}^{-3}$ , the NW becomes totally depleted in the voltage range  $V_{GS} = -20$  V to  $+20$  V. From similar set of transfer curves but with different surface state densities, we can calculate the  $I_{on}/I_{off}$  ratio as function of polarization and surface charges as shown in Figure 7.9. For a surface state density  $\leq 2.5 \times 10^{12}$   $\text{cm}^{-2}$ , a polarization charge density of  $\sim 10^{13}$   $\text{cm}^{-2}$  is required to obtain significant current modulation in the InAs channel. This value is dependent on the width of the ZB segments (3.5 nm considered here) and their

density across the channel length. The values of surface state density are within what have been estimated before for InAs NWs<sup>38,44,45</sup> and those of spontaneous polarization charge density are also within what have been obtained for hexagonal crystals.<sup>48</sup> As the density of spontaneous polarization charges is increased, surface accumulation is further compensated and the threshold voltage shifts toward 0 V as shown in Figure 7.8. High densities of polarization charges ( $n_{\text{pol}} \geq 4 \times 10^{13} \text{ cm}^{-2}$ ) lead to complete depletion of the InAs channel, which explains the reduction in the  $I_{\text{on}}/I_{\text{off}}$  ratio for  $n_{\text{pol}} \geq 10^{13} \text{ cm}^{-2}$ .

## 7.6 Conclusions

In this chapter, we have correlated microstructure and transport properties of individual InAs NWs to elucidate the origin of dramatic differences in subthreshold current for NWFET's fabricated from InAs NWs grown on SiO<sub>2</sub>/Si and InAs (111) B substrates. From NWFET measurements and analysis, we found that pure ZB NWs grown on SiO<sub>2</sub>/Si exhibit poor subthreshold characteristics when compared to WZ NWs with small ZB segments grown on InAs (111)B. We attribute this difference to the presence of spontaneous polarization charges at the WZ/ZB interface. These polarization charges create negative fields that lead to depletion of the NW surface, surpassing carrier accumulation caused by interface charges. This is confirmed by 2D Silvaco-Atlas simulations in which the trends in the subthreshold characteristics for WZ/ZB NWs have been reproduced only when polarization charges of  $\sim 10^{13} \text{ cm}^{-2}$  at the WZ/ZB interface were inserted. These results provide new insights and considerations into the design of electronic devices utilizing VLS grown InAs NWs.

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## **8. FIELD DEPENDENT TRANSPORT PROPERTIES OF INDIUM ARSENIDE NANOWIRES**

### **8.1 Introduction**

The high electron mobility demonstrated recently in InAs nanowire field-effect transistors (NWFETs)<sup>1</sup> highlights the potential of such nanoscale devices for high performance electronic applications. Indeed, back-gate,<sup>2,3</sup> top-gate,<sup>4</sup> and wrap-gate<sup>5</sup> InAs based NWFETs have been already realized, and their low field transport properties have been reported. However, the vertical (gate-channel) and lateral (source-drain) field dependent transport properties in NWs and the consequences of high injection fields on device performance and morphology have not been fully explored. In this chapter, we discuss the field dependent transport properties of InAs NWFETs and highlight the effects of high injection fields on their transport behavior from current-voltage (I-V), transmission electron microscope (TEM) and scanning TEM (STEM) characterization and support our experimental observations and analysis with two dimensional (2D) electro-thermal simulations.

### **8.2 Summary of Results**

We present in this chapter detailed studies of the field dependent transport properties of InAs nanowire field-effect transistors. Transconductance dependence on both vertical and lateral fields is discussed. Velocity-field plots are constructed from a

large set of output and transfer curves which show negative differential conductance behavior and marked mobility degradation at high injection fields. Two dimensional electro-thermal simulations at current densities similar to those measured in the InAs NWFET devices indicate that a significant temperature rise occurs in the channel due to enhanced phonon scattering that leads to the observed mobility degradation. Scanning transmission electron microscopy measurements on devices operated at high current densities reveal Arsenic out-diffusion and crystal deformation in the subject nanowires.

### 8.3 Experiment

The InAs NWs used in this study were grown by organo-metallic vapor phase epitaxy on thermal SiO<sub>2</sub>/Si substrates at a growth temperature of 350 °C and a V/III ratio (AsH<sub>3</sub>/TMIn input molar ratio) of 10.<sup>6</sup> E-beam lithography was utilized to fabricate top-gate NWFETs from these NWs on 600 nm SiO<sub>2</sub>/n<sup>+</sup>-Si with a 73 nm ZrO<sub>2</sub>/Y<sub>2</sub>O<sub>3</sub> top-gate dielectric and 100 nm Al top gate.<sup>1</sup> Ti/Al (15 nm/85 nm) layers were then used to fabricate ohmic contacts. We have observed negative differential conductance in NWFETs fabricated from these NWs as well as from NWs grown on InAs(111)B substrates (growth temperature of 500 °C and a V/III of 10),<sup>7</sup> and in this chapter will discuss in detail the field dependent transport properties of top-gate InAs NWFETs.

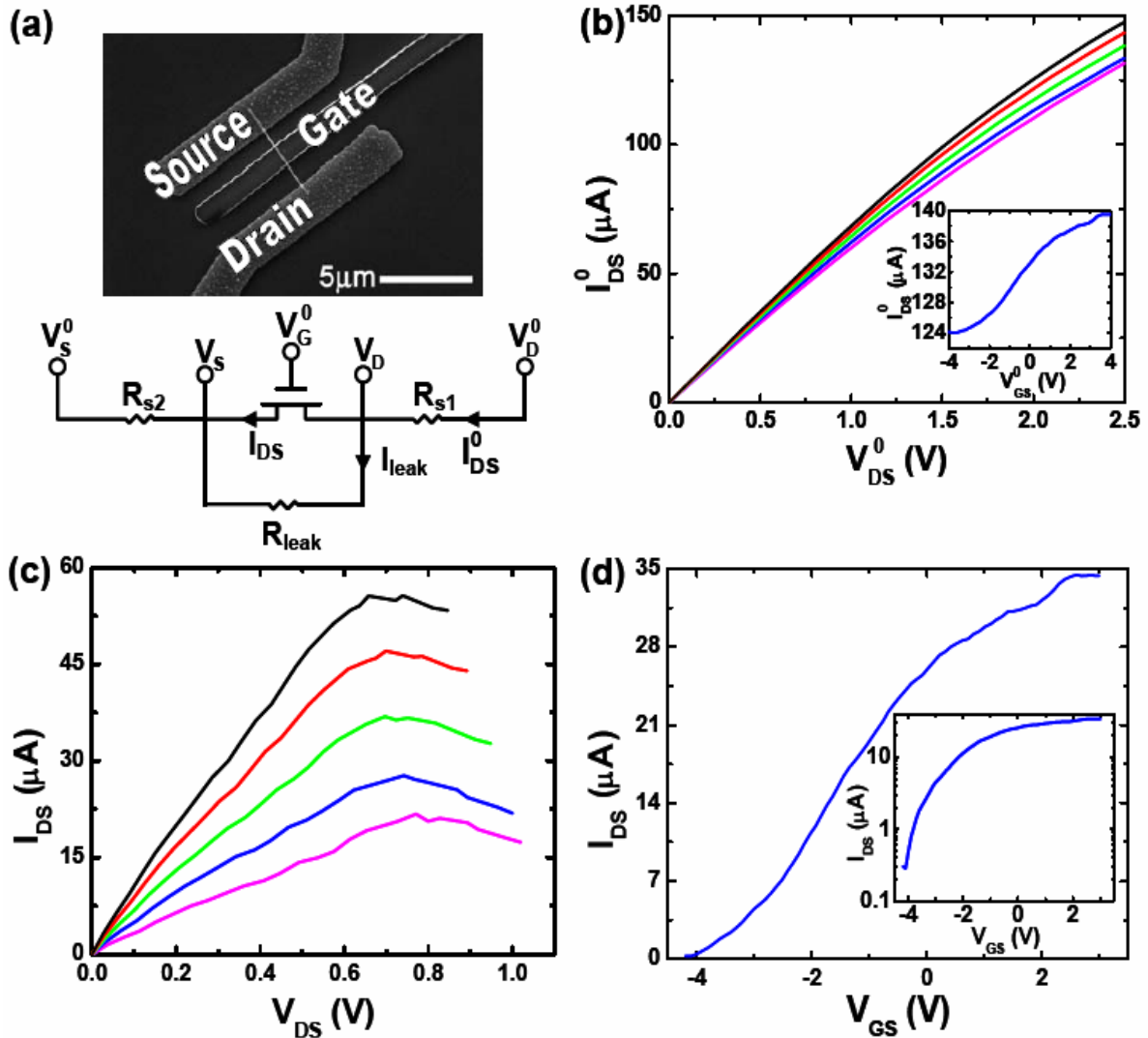


Figure 8.1. (a) FESEM image of a top-gate InAs NWFET and its corresponding DC equivalent circuit. (b) Measured output curves of an InAs NWFET device ( $D = 90\text{ nm}$ ,  $L_G = 0.97\mu\text{m}$ ,  $L_{SD} = 3.57\mu\text{m}$ ). Inset is the measured transfer curve for the same device. (c) Extracted output curves. (d) Transfer curves from (b) by taking into account series and leakage resistances. Inset is the extracted transfer curve plotted in logarithmic scale.

#### 8.4 Vertical and Lateral Field Dependent Mobility

Figure 8.1 (a) shows a representative field-emission scanning electron microscope (FESEM) image of a top-gate NWFET device and the corresponding equivalent DC circuit diagram.<sup>4</sup> Only the NW segment directly under the gate, of length  $L_G < L_{SD}$ , where

$L_{SD}$  is the source drain length, is considered to be the active portion of the NWFET device. Top-gated devices with extension regions are favored over devices with a gate overlapping the source/drain contacts to eliminate gate leakage currents when operating the devices at high fields, as well as to improve their breakdown characteristics.<sup>8</sup> However, the series resistances,  $R_{s1}$ , associated with the drain contact plus extension region, and the source counterpart,  $R_{s2}$ , dominate the measured  $I$ - $V$  characteristics shown in Figure 1 (b) for the following reasons: (i) the linear  $I$ - $V$  relation of the series resistances prevents observation of saturation in the output curves at high  $V_{DS}$ , and (ii) the source series resistance reduces the gate transconductance.<sup>9</sup> The gate transconductance is also decreased due to the presence of trap states at the dielectric-InAs interface which introduce an additional capacitance that reduces the gate field and prevent full depletion of the InAs NWFET channel.<sup>1</sup> Thus, high off-current values are expected. The unmodulated portion of the NW channel under the gate can be modeled as a leakage resistance,  $R_{leak}$ , obtained from the lowest measured  $I_{DS}$  at sufficiently negative  $V_{GS}$ . By considering the potential drops across the series resistances as well as the leakage resistance,<sup>4</sup> we are able to assess and extract the output and transfer curves inherent to the transport properties of the NW segment directly under the gate (See supporting material), as shown in Figures 1 (c) and 2 (d). Note that (i) a substantial voltage drop is associated with the source and drain segments, and the potential drop corresponding to the NW segment directly under the gate is only 30 – 45 % of the applied voltage, the magnitude of which also depends on the gate voltage bias; and (ii) for  $V_{DS}$  larger than 0.7 – 0.8 V, there is a decrease in current as  $V_{DS}$  is increased, i.e. negative differential conductance (NDC). We have also observed NDC in the extrinsic output curves of back-gate

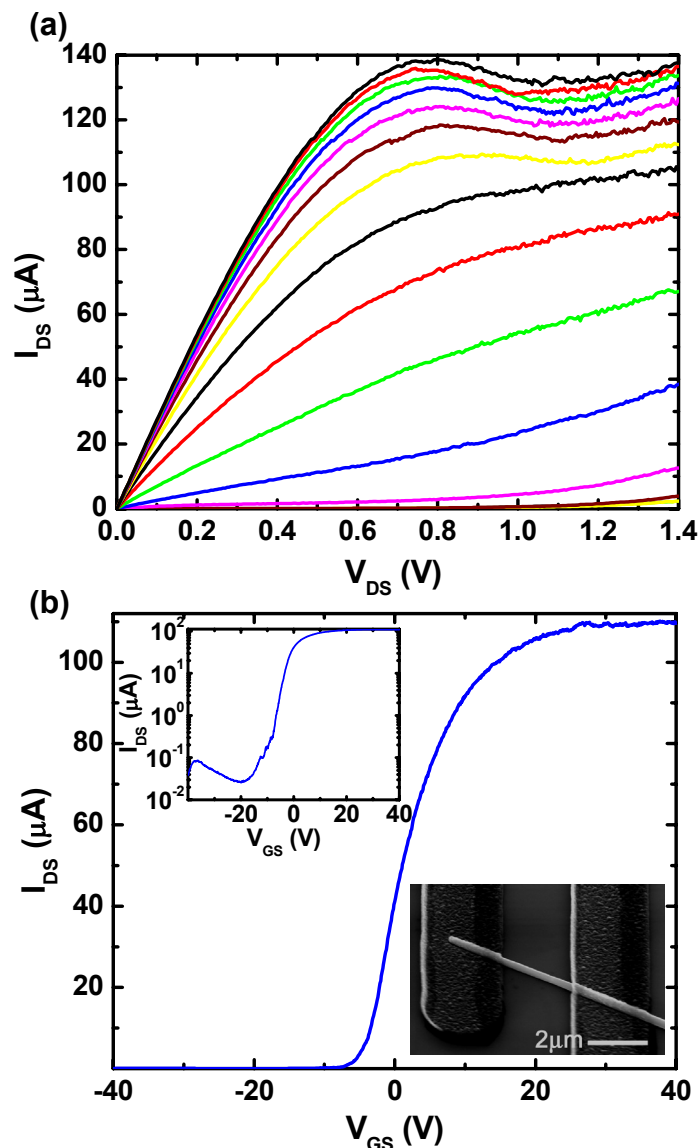


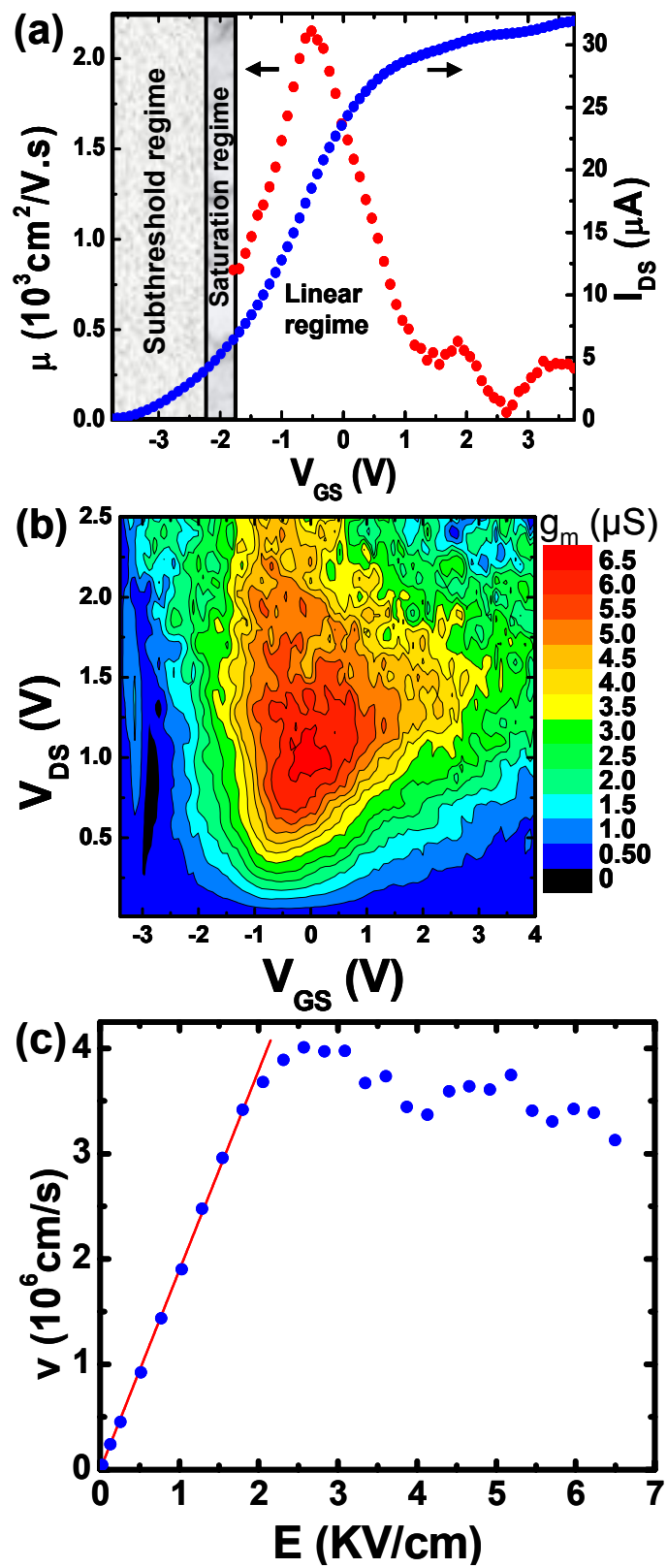
Figure 8.2. (a) Output characteristics of an InAs NWFET (Diameter=243nm,  $L=2.5\mu\text{m}$ ) for  $V_{GS} = -40$  V to +40 V with a +5 V step. (b) Transfer characteristics of the same device at  $V_{DS}=0.5$  V with inset of the same curve plotted on log scale. Bottom inset is a scanning electron microscope image of the back-gate NWFET device.

NWFETs fabricated from NWs grown on InAs (111)B substrates as illustrated in Figure 8.2.

Transfer curves are typically used to extract the dependence of the transconductance and mobility on gate voltage, as shown in Figure 8.3 (a) where the



Figure 8.3. (a) Plot of the extracted transfer curve and field-effect mobility  $\mu_{FE}(V_{GS})$  of an InAs NWFET ( $D = 72$  nm,  $L_G = 1$   $\mu\text{m}$ , and  $L_{SD} = 3.35$   $\mu\text{m}$ ) at  $V_{DS} = 0.5$  V. (b) Contour plot of the extrinsic transconductance measured with  $V_{GS}$  sweep for different applied  $V_{DS}$  from the device in Figure 8.1. (c) Velocity-field plot for same device in Figure 1 extracted from several transfer and output curves.



field-effect mobility ( $\mu_{FE} = g_m L_G^2 / CV_{DS}$ ) is plotted for  $V_{GS} \geq -1.9$  V, which corresponds to the linear operating regime. Here,  $g_m$  is the intrinsic transconductance,  $V_{DS}$  is the voltage drop across  $L_G$ , and  $C$  is the gate capacitance which is equal to the oxide capacitance in the linear regime.<sup>10</sup> Note that at both positive and negative gate voltages, the field-effect mobility is low and increases as  $V_{GS}$  approaches the flat band voltage,  $V_{fb}$ ,<sup>11</sup> which is typically less than 0 V due to the presence of positively charged donor-type surface states<sup>12</sup> that shift  $V_{fb}$  to negative values. The  $\mu_{FE}$ - $V_{GS}$  dependence shown in Figure 8.3 (a) follows the same trends as those observed in metal-oxide-semiconductor FETs<sup>13</sup> and heterojunction FETs.<sup>14</sup> For positive voltages in the accumulation regime,  $\mu_{FE}$  decreases due to surface roughness scattering.<sup>13,15</sup> For negative gate voltages below  $V_{fb}$  in the depletion regime, coulomb scattering due to fixed oxide charges, interface state charges, and ionized impurity charges reduces  $\mu_{FE}$ .<sup>16</sup> Coulomb scattering is dominant at low carrier densities and is reduced at higher densities due to screening of the charged centers' potential. The  $\mu_{FE}$ - $V_{GS}$  dependence is typically asymmetric with fast roll-off at voltages close to the threshold voltage.<sup>13,14</sup> For the InAs NWFETs, however, the large surface state density<sup>1</sup> leads to poor subthreshold characteristics and to the more symmetric appearance of the  $\mu_{FE}$ - $V_{GS}$  curve as shown in Figure 8.3 (a).

The transconductance and  $\mu_{FE}$  are functions of both vertical and lateral fields.<sup>10</sup> To reveal both field effects, we have constructed a 2D plot of the transconductance as a function of both  $V_{GS}$  and  $V_{DS}$ . Figure 8.3 (b) shows such an extrinsic transconductance map obtained from several  $I_{DS}$ - $V_{GS}$  curves measured for  $V_{DS}$  in the range of 0 V to 2.5 V. The vertical gate field dependence in this case is similar to that of Figure 8.3 (a), where

the extrinsic transconductance increases as  $V_{GS}$  approaches  $V_{fb}$ . However, as the lateral (source-drain) field is increased, we observe that the extrinsic transconductance increases linearly and peaks at some lateral field value, beyond which transconductance degradation takes place at a rate slower than that with the vertical field, which, to our best knowledge, has not been discussed in earlier NWFET transport studies. Reduction of the transconductance at high lateral fields explains the decrease in current in the extracted output curves of Figure 8.1 (b).

To assess the lateral field dependence of the transport behavior, we extract the electric field across the NW portion under the gate by taking into account the underlap and contact series resistances,  $R_{s1}$  and  $R_{s2}$ , and the leakage resistance,  $R_{leak}$ .<sup>4</sup>  $R_{s1}$ ,  $R_{s2}$ , and  $R_{leak}$  are dependent on  $V_{DS}$ , and their values are extracted for each  $V_{DS}$  biasing voltage and used in the subsequent field, velocity and mobility calculations ( $R_s$  varies in the range of 10.3 K $\Omega$  – 14 K $\Omega$  and  $R_{leak}$  in the range of 2.5 K $\Omega$  – 7 K $\Omega$ ). In the linear operating regime, the drift velocity  $v$  can be calculated according to

$$v = \frac{I_{DS}^0 (1 + (R_{s1} + R_{s2}) / R_{leak}) - V_{DS}^0 / R_{leak}}{C(V_{GS}^0 - V_T) / L_G - CI_{DS}^0 R_{s2} / L_G}. \quad (8.1)$$

If the series and leakage resistances are not taken into account, equation (8.1) simplifies to

$$v = \frac{I_{DS}^0}{C(V_{GS}^0 - V_T) / L_G}. \quad (8.2)$$

Equation (8.2) is typically used to obtain the field-effect mobility,  $\mu_{FE} = \frac{g_m^0 L_G^2}{CV_{DS}}$ , at small  $V_{DS}$  in NW and carbon nanotube transistors<sup>17</sup> by assuming  $v = \mu_{FE}E$ , with  $E =$

$V_{DS}/L_G$  being the lateral electric field and  $g_m^0 = \partial I_{DS}^0 / \partial V_{GS}^0 \big|_{V_{DS}=cst}$  the extrinsic transconductance. To extract the lateral field dependent velocity, the transfer curves are measured for  $V_{DS}^0$  values in the range of 0 V to 2.5 V, and  $v$  is then calculated at  $V_{GS}^0 = 0$  V using equation (8.1). The computed velocity values are plotted in Figure 8.3 (c) as function of lateral electric field. At low fields, the slope of the velocity field plot is the low field effective mobility, which is typically calculated from the conductance<sup>13</sup> as in equation (8.1) rather than the transconductance, and maintains a constant value of  $\sim \mu_{eff} = 1900 \text{ cm}^2/\text{V}\cdot\text{s}$  for  $0 \leq E \leq 1.5 \text{ KV/cm}$ . The drift velocity increases as the lateral field increases and reaches a peak velocity  $v_{peak} \approx 4 \times 10^6 \text{ cm/s}$ , which is lower than that of bulk InAs ( $\sim 4 \times 10^7 \text{ cm/s}$ ).<sup>18</sup> For  $E \geq 2.7 \text{ KV/cm}$ , the extracted carrier velocity decreases with further increase in the applied lateral field as shown in Figure 8.3 (c). The NDC behavior is consistent in the velocity-field plots computed for several  $V_{GS}^0$  values as have shown in Figure 8.4 and have been obtained from several devices fabricated separately on similar InAs NWs. From Figure 8.4, we can note that (i) the slope of the velocity-field plot ( $\mu_{eff}$ ) is lower as  $V_{GS}^0$  increases due to enhanced surface scattering, and (ii) the dip in the velocity at high fields is stronger for higher  $V_{GS}^0$  values due to higher current densities and enhanced thermal heating as we will show below.

Negative differential conductance and reduction of carrier velocity at high fields can arise for a number of reasons. First, intervalley scattering from the low-effective-mass direct conduction band minimum ( $\Gamma$ ) to higher effective mass, higher valley/ band minima ( $X$  or  $L$ ) may lead to NDC.<sup>8</sup> However, InAs has the largest energy separation between the conduction band minima among all high mobility III-V materials ( $E_{\Gamma L} = 0.73$

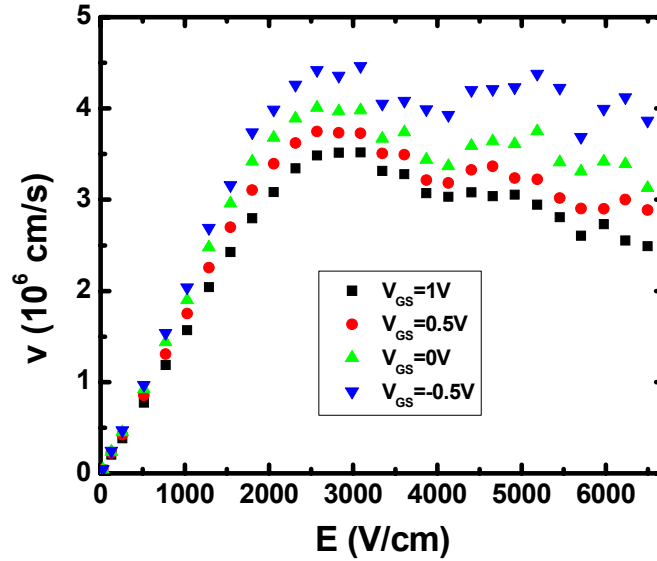


Figure 8.4. Velocity-field plots for same device in Figures 8.1 and 8.3 extracted from several transfer and output curves for different  $V_{GS}$ .

eV and  $E_{TX} = 1.02$  eV) resulting in minimal intervalley scattering. Second, intravalley or intersubband scattering where electrons lose momentum when scattered from one energy subband with high momentum to another equivalent energy subband with lower momentum may lead to NDC.<sup>9</sup> This can be important in one-dimensional nanostructures where energy subbands are quantized and equivalent-energy transitions are associated with larger momentum differences. Third, non-parabolicity in the energy-momentum band diagrams may lead to NDC, where electrons with high energy encounter increased effective mass and reduced momentum relaxation time, both of which reduce the electron mobility.<sup>18,19</sup> This effect is pronounced for small bandgap materials such as InAs. Fourth, enhanced phonon scattering and momentum relaxation to the lattice where the relaxation time is effectively reduced at high injection fields and may lead to NDC. Although little theoretical work has been done on NDC in low dimensional semiconductors, non-parabolicity in the energy-momentum band diagrams<sup>20</sup> and more recently hot phonon

distribution were suggested to dominate the NDC in carbon nanotubes.<sup>21</sup> While pulsed current-voltage characteristics could be used to eliminate heating effects,<sup>18</sup> these techniques are not readily available for NWs due to the large parasitic impedances that impose constraints on such fast pulsing procedures.<sup>2</sup> We show next through 2D electro-thermal simulations and STEM analysis on two-terminal InAs devices that thermal heating during normal device operating procedures is a dominant process that leads to the observed negative differential conductance behavior.

### **8.5 Electro-thermal Simulations and Effects of High Injection Fields**

We first consider the case of a 90 nm thick InAs slab atop SiO<sub>2</sub>/Si with Ti/Al top contact electrodes and dielectric passivation with Al top-gate similar to the actual device structure over which the negative differential conductance has been measured (Figures 8.1 and 8.3). The electro-thermal properties for this structure is simulated in Silvaco-Atlas by taking into account a 350 μm thick Si substrate and 200 μm extension of the contact electrodes and substrate around the NWFET device. In order to calibrate the measured current density to that of the simulated one, a contact resistance value of 350 Ω per electrode and a mobility value of 16000 cm<sup>2</sup>/V·s were found to give the best fit after several alterations. Both of these values are in good agreement with our extracted data from similar devices.<sup>1</sup> Extracted mobility values from NWFET measurements are apparent values that are influenced by the interface state capacitance, and can vary with  $V_{GS}$  sweep rate which determines the charge balance between carrier capture and emission from interface states.<sup>1</sup> Slow  $V_{GS}$  sweep rates have resulted in reduced hysteresis

and high mobility values of  $16000 \text{ cm}^2/\text{V}\cdot\text{s}$  which are believed to be the actual carrier mobility values in the channel.<sup>1</sup> For the carrier concentration, we have used a bulk concentration of  $5 \times 10^{16} \text{ cm}^{-3}$  and a positive fixed charge density of  $2.7 \times 10^{12} \text{ cm}^{-2}$ . These were used in a Schrödinger-Poisson solver to fit experimental values of carrier concentration for NWs with diameters in the range of 70 – 120 nm, and resulted in an average carrier concentration of  $\sim 8 \times 10^{17} \text{ cm}^{-3}$  (both measured and simulated) for a 90 nm InAs NW at  $V_{GS} = 0 \text{ V}$  and constant  $V_{DS} = 0.15 \text{ V}$ .<sup>22</sup> Figure 8.5 (a) shows excellent agreement between the measured and simulated current density using these input device parameters. This agreement between simulated and extracted values of contact resistance and mobility validates our extraction procedure and highlights the ability to form low resistance ohmic contacts and obtain decent mobility values in excess of  $10^3 \text{ cm}^2/\text{V}\cdot\text{s}$  from InAs NWs as demonstrated by us<sup>1</sup> as well as by other research groups.<sup>2,5</sup>

Figure 8.5 (b) shows a contour plot of the temperature profile across the active portion of the device when biased at  $V_{DS} = 2.5 \text{ V}$  resulting in a current density of  $2.3 \times 10^6 \text{ A}/\text{cm}^2$  and a peak temperature of 506 K. This is a significant increase in the device temperature that leads to enhanced phonon scattering and mobility degradation. Indeed, such an increase of  $\sim 200 \text{ K}$  above room temperature leads to a mobility degradation by a factor of  $\sim 2$  for carriers in InAs bulk with (100) surfaces.<sup>23</sup> Figure 8.5 (c) shows a line cut of the temperature profile across the channel length of the device starting at the source electrode ( $x = 0$ ) and ending at the drain electrode ( $x = 3.6 \text{ }\mu\text{m}$ ). The hottest regions in the channel where the temperature exceeds 500 K are located near the source electrode within a distance of  $\sim 250 \text{ nm}$ . This distance is of the order of the electron mean free path in our InAs NW and is consistent with length scales over which a constant



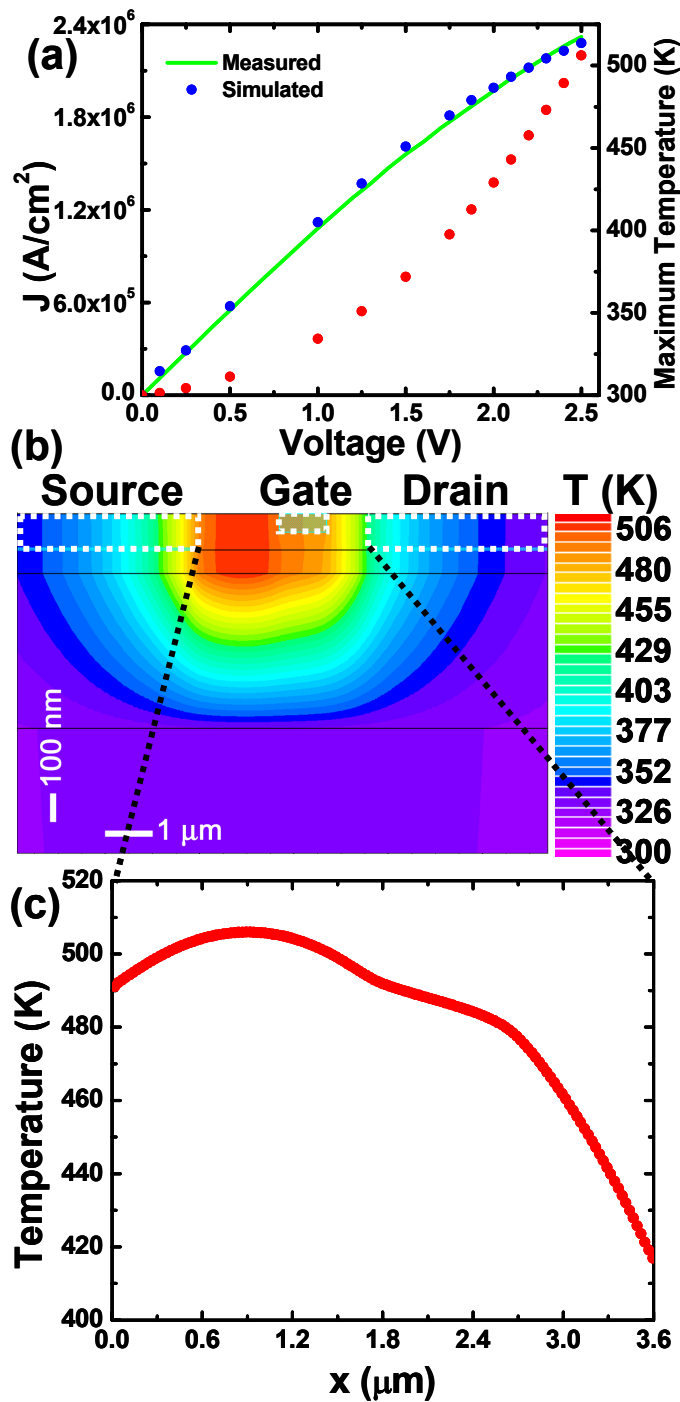


Figure 8.5. (a) Measured and simulated current density for a material stack similar to that of the device considered in Figures 8.1 and 8.3 ( $V_{GS} = 4$  V) along with the maximum temperature in the channel. Excellent agreement between the measured and simulated  $J$  is obtained for  $R_c = 700 \Omega$  and  $\mu = 16000 \text{ cm}^2/\text{V}\cdot\text{s}$ . (b) Contour plot of the lattice temperature and (c) line cut profile across the center of the channel starting at the source electrode ( $x = 0$ ), obtained from 2D Silvaco-Atlas electro-thermal simulations considering the same device material stack as that of Figures 1 and 2.

resistance in InAs NWs has been measured.<sup>24</sup> Following the  $\sim 250$  nm region, over which ballistic transport have been observed, onset of phonon scattering in the diffusive NW regions is expected to prevail. Electro-thermal simulations at different  $V_{DS}$  biases shows a power-law increase of temperature as function of current density as shown in Figure 8.5 (a) with peak temperatures near the source electrode.

We have also used Transmission Electron Microscopy (TEM) and Scanning TEM (STEM) on two-terminal InAs NW devices fabricated on a 100-nm  $\text{Si}_3\text{N}_4$  suspended membrane, suitable for TEM study, to observe morphological changes to the InAs NWs when exposed to high current densities. Figure 8.6 (a) shows  $I$ - $V$  characteristics of an InAs NW device ( $D = 33$  nm,  $L_{SD} = 1.5$   $\mu\text{m}$ ) up to different  $V_{DS}$  stresses. It can be noted from Figure 8.6 (a) that for the last  $V_{DS}$  stress bias of 2.2 V, the current values are lower than those of the previous stress voltage of 2.0 V, after which the current drops to zero at 1.98 V. The current density at which the NW breaks is  $\sim 10^7$  A/cm<sup>2</sup>. It is noteworthy that when normalized to the NW diameter, the current capacity of this InAs NW device is 3 A/mm and exceeds that of the highest ever reported value in any III-V channel material including that of the recent InGaAs MOSFET (1.05 A/mm).<sup>25</sup> This is despite the unoptimized device geometry and the lower heat dissipation in our device that was fabricated on a 100 nm  $\text{Si}_3\text{N}_4$  membrane suspended in air. Figure 8.6 (b) shows TEM images of the two-terminal InAs NW device used for this TEM study. It can be seen clearly that the discontinuity in the InAs NW device occurs at  $\sim 250$  nm distance from the source electrode, which is consistent with the simulations above and experimental measurements of the mean-free path in a similar InAs NW as discussed in chapter 6.<sup>24</sup> Figure 8.6 (c) shows a high resolution TEM (HRTEM) image of a section of the InAs

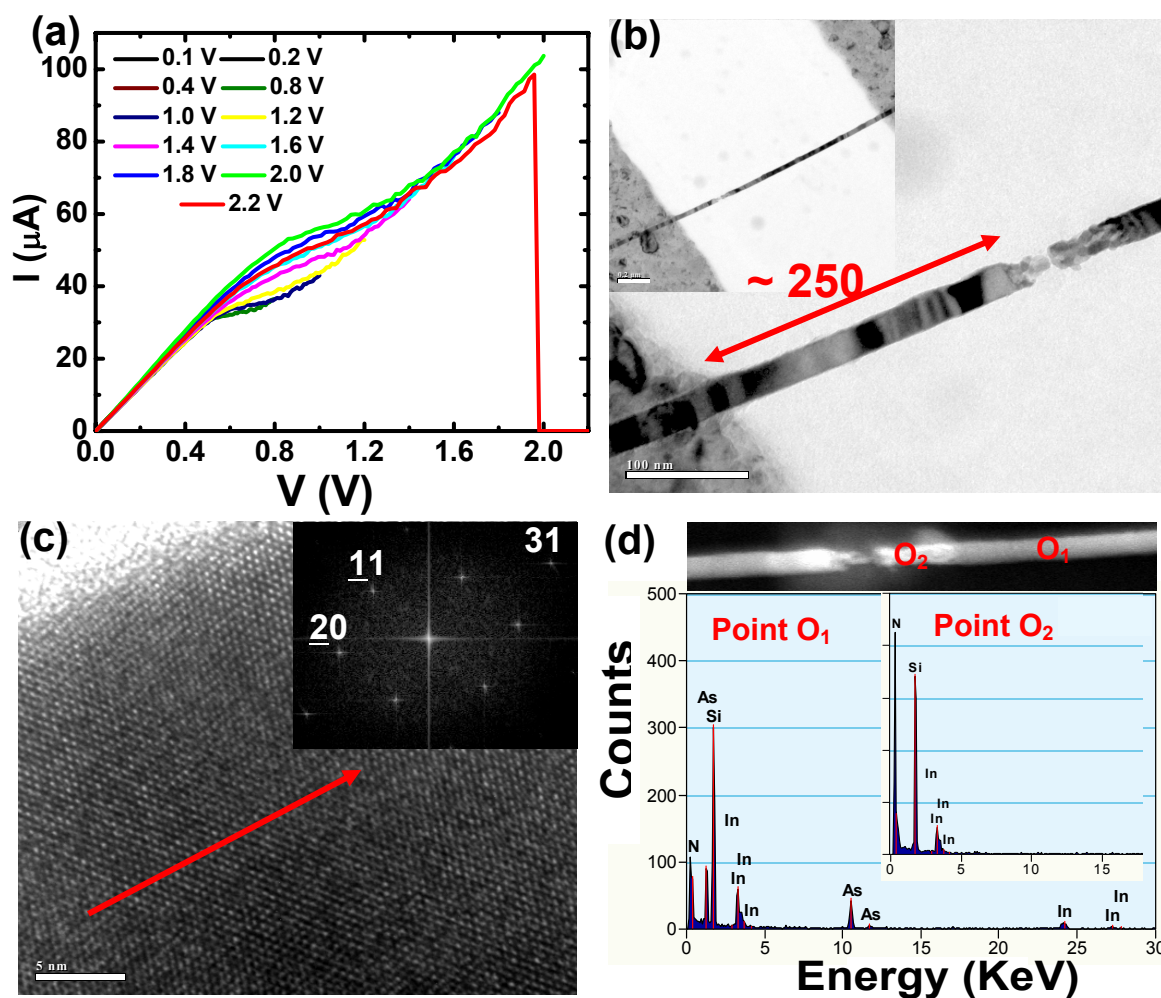


Figure 8.6. (a) Current voltage characteristics of a two-terminal InAs NW device fabricated on a 100 nm  $\text{Si}_3\text{N}_4$  TEM grid when biased up to different voltage biases. (b) TEM bright field image of the same device in (a) after performing the  $IV$  measurement.

NW used for this measurement and the corresponding diffraction pattern of the image showing a single crystalline zincblende structure with a  $\langle 31\bar{1} \rangle$  growth orientation. Figure 8.7 shows HRTEM images of the InAs NW device under consideration taken at the discontinuity region and showing transition from polycrystalline to single crystalline

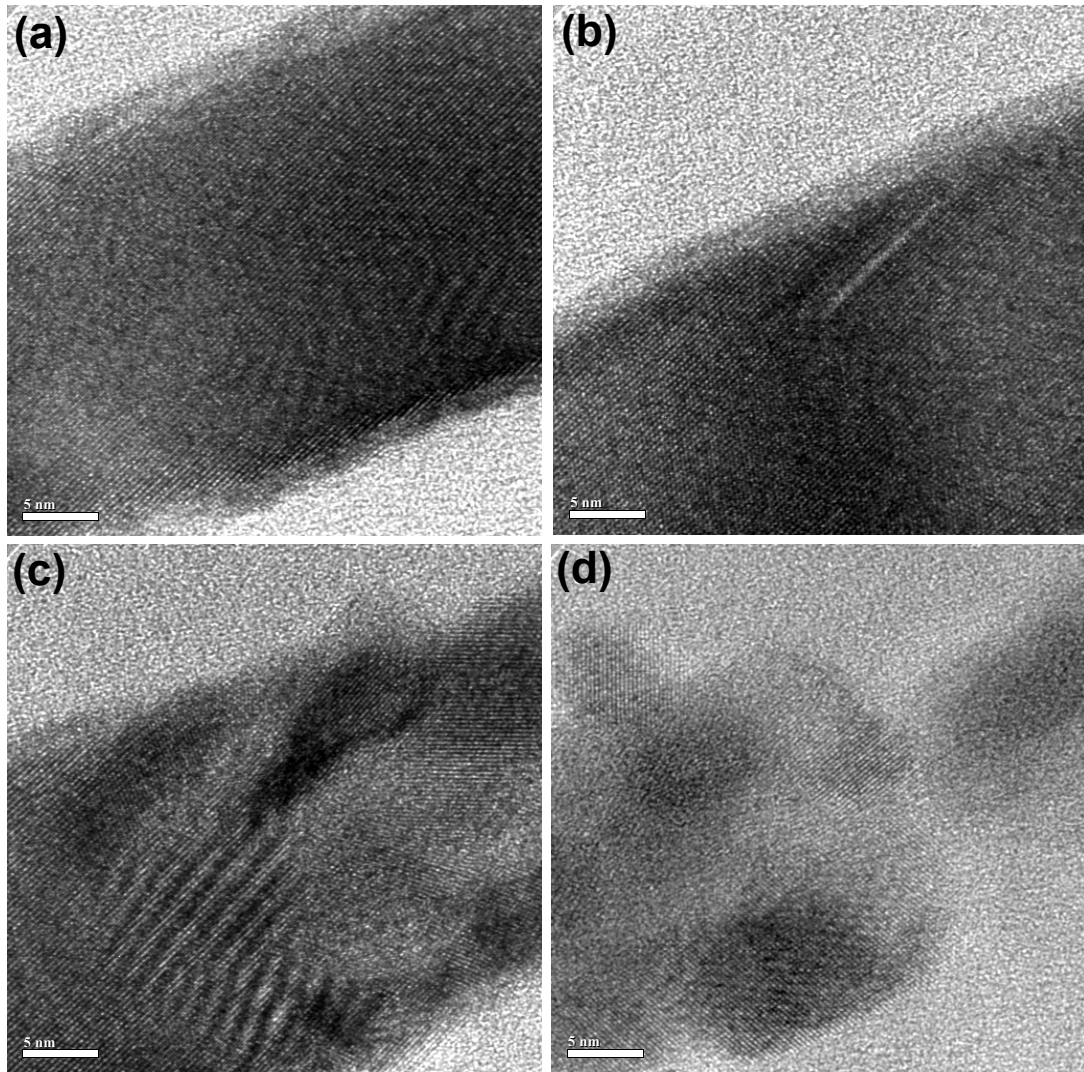


Figure 8.7. HRTEM images of the left portion of the InAs NW device shown in Figure 8.6 (b) from regions of (a) the leftmost portion of the characterized area moving toward (d) the NW discontinuity region. Scale bars are 5 nm.

regions as the distance from the discontinuous region toward the source electrode increases.

STEM analysis on the same two-terminal InAs NW device has been performed.

Figure 8.6 (d) shows a dark-field scanning image of the device with marked points ( $O_1$  &

O<sub>2</sub>) from which energy dispersive x-ray (EDX) analysis spectra were obtained. Both In and As peaks appear in the EDX spectrum of the NW region at point O<sub>1</sub> away from the breakage area. However, only In (in addition to Si and N from the nitride membrane) was detected at point O<sub>2</sub> of the NW region in close proximity to the breakage region. This suggests that upon exposure of the NW to high current density, the local heating in the NW at ~ 250 – 300 nm away from the source region leads most likely to As vaporization leaving In behind. The molten In left behind, which has a melting temperature of ~ 159 °C and a lattice constant of 4.59 Å,<sup>26</sup> freezes and shrinks in size forming a discontinuity in the NW at the decomposed region as can be seen in Figures 8.6 (b). The change of morphology at the breaking point is clearly seen from the HRTEM images in Figure 8.7. Note that this situation represents the extreme scenario where physical breakdown in the NW occurs. At slightly lower current densities than are required for breakage, we anticipate that local heating causes similar decomposition or irreversible morphological changes to the NW leading to a total reduction in the NW current. This situation is observed in Figure 8.6 (a) where the current-voltage characteristics show a lower slope (increased resistance) when comparing the measurement up to 2.0 V (where the NW is exposed to high current density) to that of up to 2.2 V just before it breaks. Measurements on similar two-terminal devices have shown that these high current values cannot be recovered after such high current density exposure consistent with permanent morphological changes to the NW and the irreversible negative differential conductance observed.

## 8.6 Conclusions

In this chapter, we have presented studies on the dependence of transport properties of top-gate InAs NWFETs on vertical and lateral fields and discussed transconductance degradation as a function of both fields. Negative differential conductance was observed in the measured and the extracted output curves and velocity-field plots from top-gate NWFETs. High injection fields induce morphological degradation to the NW due to heating effects and irreversible mobility degradation that were illustrated using TEM and STEM analysis. 2D electro-thermal simulations were used to highlight the temperature increase in the InAs NWFET devices that leads to enhanced phonon scattering and reduced mobilities. These results also suggest that thermal conductivity and thermal management are likely to be important issues in realizing the full potential of nanowire-based devices.

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## 9. VERTICAL INTEGRATION AND ELECTRICAL ISOLATION OF INDIUM ARSENIDE NANOWIRES ON INSULATOR ON SILICON

### 9.1 Introduction

Semiconductor nanowires (NWs) have allowed the realization of several key components for electronic and photonic systems including surround-gate field-effect transistors (FETs),<sup>1,2</sup> light emitting diodes,<sup>3</sup> photodetectors,<sup>4</sup> and waveguides.<sup>5</sup> However, for integrated functional systems, growth or post-growth assembly of NWs at specified locations is necessary but has remained challenging. NW growth at pre-determined locations suitable for direct device integration is desired. Typically, e-beam lithography or nano-imprint lithography are utilized to pattern growth seeds at specified locations followed by NW array growth.<sup>6</sup> Those arrays can then be used for device fabrication, such as vertical wrap-around gate FETs;<sup>7</sup> however, the presence of the semiconducting substrate beneath avoids electrical isolation and individual addressability of single NWs. NW Growth at pre-determined locations have also been achieved on (111) sidewall stripes etched on (110) substrates – resulting in the so-called NW bridges.<sup>8,9,10</sup> Individual addressability may be achieved with such technique; however with bulky contacts and associated complexity in device fabrication. Post-growth assembly of individual NWs as well as NW arrays have been demonstrated. Examples of these are fluidic alignment,<sup>11</sup> electric-field manipulation,<sup>12</sup> Langmuir-Blodgett alignment,<sup>13</sup> and sequential printing of NWs on various types of host substrates.<sup>14,15</sup> While these approaches may be suitable for heterogeneous integration that requires low temperature processing, such as integration to

flexible substrates,<sup>14</sup> none of these techniques is suitable for practical fabrication of dense and high performance devices that may compete with current planar devices. It has been argued that future technology nodes should make use of advancement of Si technology mainstream and thus, promising high performance devices should be integrated to Si substrates. Demonstrated growth of III-V NWs on Si,<sup>16,17,18,19</sup> may not represent the ideal candidates for future technology nodes due to the presence of potential barriers at the III-V/Si interface and lack of the ability for addressing single NW devices as well as the feasibility of multi-functions per chip. In this work, we develop and implement a novel integration scheme for III-V NWs to Si substrates that allows vertical integration, electrical isolation, and individually addressable III-V NWs on Si suitable for 3D circuit applications. This integration scheme utilizes the smart-cut® technique<sup>20</sup> – typically used for producing Silicon-on-Insulator (SOI) wafers – to transfer InAs (111)B layers onto SiO<sub>2</sub>/Si, followed by ordered growth of vertical and electrically isolated InAs NWs on InAs/SiO<sub>2</sub>/Si.

## 9.2 Summary of Results

The work presented in this chapter oversees practical III-V NW device integration on Si by implementing vertical and electrically isolated III-V NW growth on insulator on Si substrates, and bypasses any structural defects and transport barriers at the Si–III-V NW interface. For this purpose, we have used ion-cut induced layer transfer technique – typically utilized in silicon-on-insulator (SOI) fabrication– in which a donor InAs (111)B substrate was Hydrogen implanted at a specified projected implantation depth and

subsequently bonded to a thermally oxidized Si substrate. Upon temperature annealing, the Hydrogen trapped into the implantation-induced damage sites nucleates into gas bubbles that exfoliate the donor InAs substrate from the bonded structure and results in a thin InAs layer atop the SiO<sub>2</sub>/Si substrate. E-beam lithography was used to pattern Au growth seeds for organo-metallic vapor phase epitaxy (OMVPE) of InAs NWs as well as for patterning InAs discs beneath the grown InAs NWs. This has resulted in ordered, vertical, and electrically isolated InAs NW arrays on SiO<sub>2</sub>/Si suitable for individual NW addressing and device fabrication. The overall transfer and fabrication technique discussed here enables hetero-epitaxy of 3D III-V structures on Si and allows the realization of a variety of vertical devices with unprecedented control on the device geometry.

### 9.3 Experiment and Discussion

III-V NW integration to Si substrates is achieved utilizing a hybrid integration technique which combines wafer bonding with ion-implantation induced layer transfer procedures that have been successfully demonstrated earlier in integrating III-V waveguide photodetectors<sup>21</sup> and dual junction solar cells to Si.<sup>22</sup> 2” InAs (111)B substrates were cut into small pieces and glued to a 4” Si (001) wafer for H-implantation which was performed at 150 KeV and 25 KeV implantation energies and  $8 \times 10^{16} \text{ cm}^{-2}$   $5 \times 10^{16} \text{ cm}^{-2}$  doses with  $1.5 \text{ } \mu\text{A/cm}^2$  beam current and  $-15 \text{ } ^\circ\text{C}$  substrate temperature. The implantation energy is used to adjust the projected range for a given ion, mass and atomic numbers of both the ion and target material.<sup>23</sup> The low temperature is necessary to form

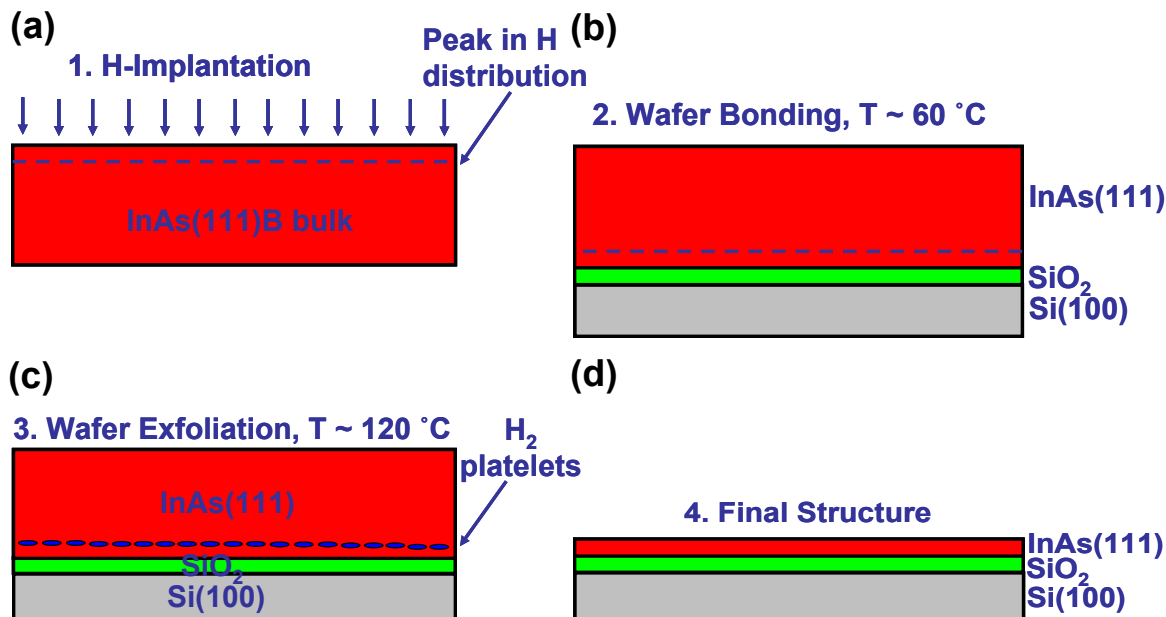


Figure 9.1. (a) – (d) Process flow for transfer of ion-implantation induced transfer layer to SiO<sub>2</sub>/Si.

point defects as effective trapping sites for Hydrogen ions and to avoid their spread/diffusion that may lead to surface blistering. These traps are believed to be Indium and Arsenic defects and Indium interstitials that lead to the formation of In-H and In-OH complexes.<sup>24</sup> The H-implantation results in ~ 1 μm and 170 nm projection depths for 150 KeV and 25 KeV, respectively. After ion-implantation (Figure 9.1 (a)), the InAs (111)B wafer is cut into 1x1 cm<sup>2</sup> pieces for the purpose of wafer bonding. An implanted InAs piece and a Si (100) wafer coated with a thermally grown oxide layer are cleaned using organic solutions and activated using O<sub>2</sub> plasma at 150 W for 30 s. The two pieces are then put into contact at room temperature in air and the bonded pair (Figure 9.1 (b)) is annealed on a hot plate at a temperature of at ~ 60 – 70 °C for ~ 10 hours to increase the bonding strength InAs/SiO<sub>2</sub>/Si structure. The temperature is then raised to ~ 120 °C to

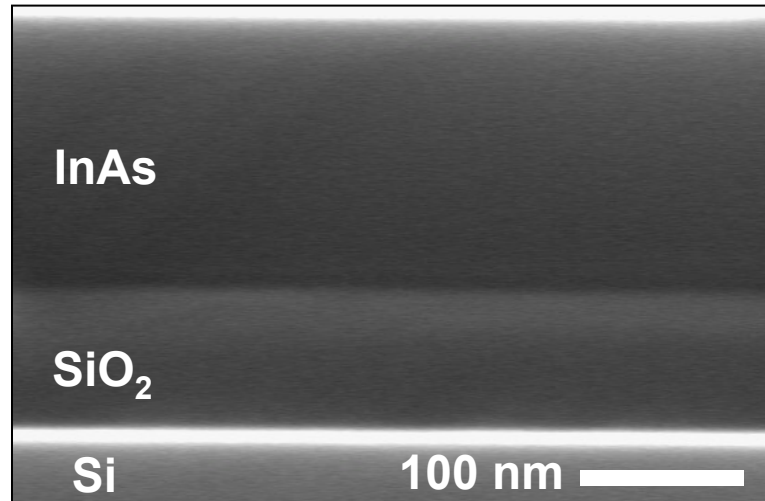
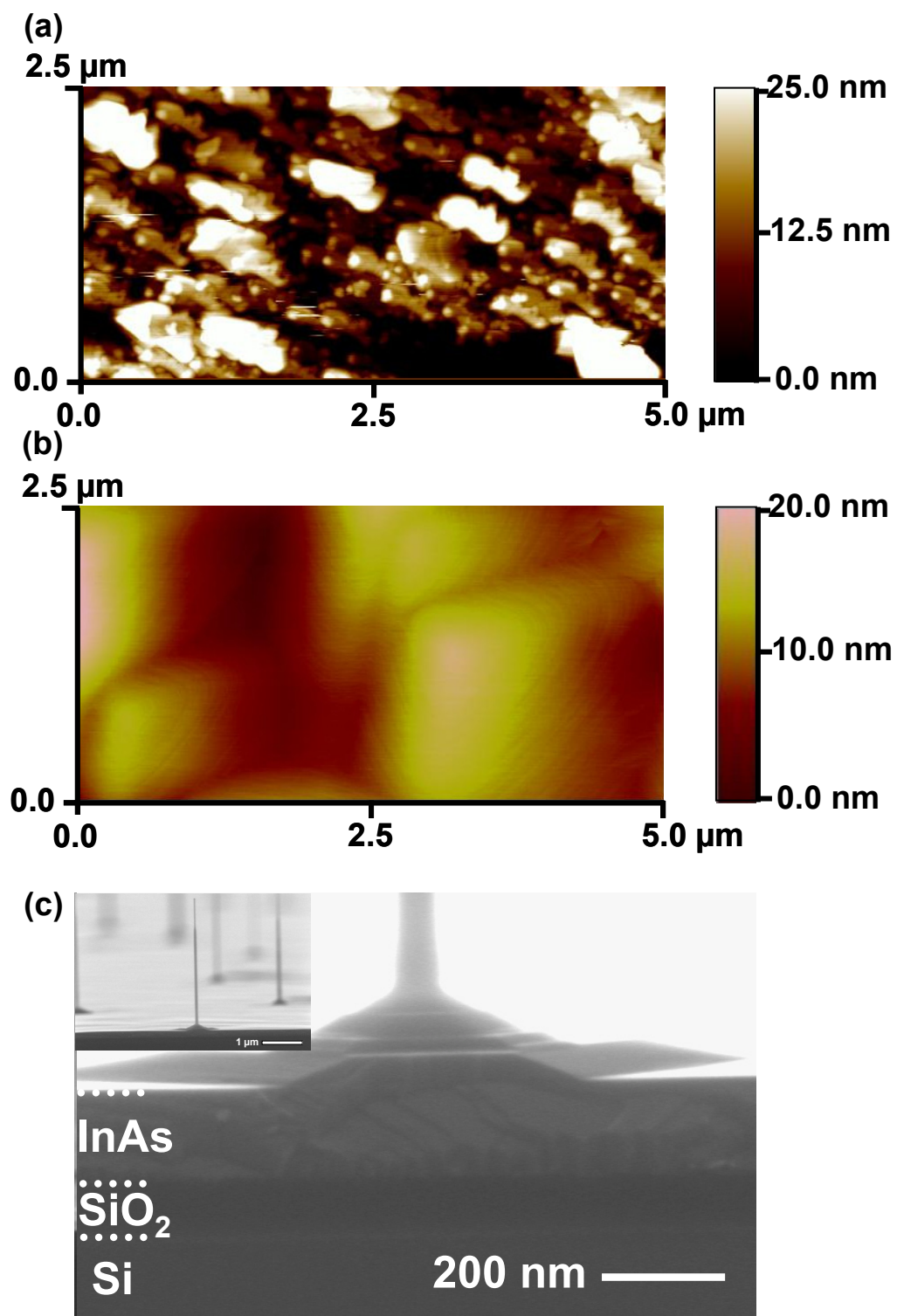


Figure 9.2. Cross-sectional FE-SEM image of the transferred InAs layer to SiO<sub>2</sub>/Si.

achieve hydrogen-induced layer exfoliation. The accumulation of trapped hydrogen around the projected range facilitates the formation and development of hydrogen platelets, as illustrated in Figure 9.1 (c), that eventually lead to exfoliation of the bonded structure near the projected depth (Figure 9.1 (d)). The final structure after layer transfer is shown in the cross-sectional SEM image of Figure 1 (e) consisting of ~ 170 nm thick InAs layer atop a ~ 70 nm SiO<sub>2</sub> layer on Si. This transferred structure is annealed at 450 °C in air for 1 hr under an external applied pressure of 1 MPa, to further increase the bonding strength for subsequent epitaxial growth.

The spread in the distribution of the implanted Hydrogen (i.e. straggle) results in a rough surface morphology directly after the ion-cut procedure. In addition, the Hydrogen implantation results in a damaged crystal structure at the surface (eg. ~ 100 nm thick damaged layer in InP implanted at 150 KeV and exfoliated at 150 °C).<sup>25</sup> Such a damaged

Figure 9.3. AFM topograph images of InAs on SiO<sub>2</sub>/Si (a) directly after ion-cut induced transfer, and (b) after wet etching of damaged layer and OMVPE thin film growth. (c) 85° FE-SEM image of InAs NWs grown on InAs/SiO<sub>2</sub>/Si. Inset is a zoom-in cross-sectional FE-SEM at the base of an InAs NW.



and rough surface is not suitable for NW growth due to the presence of the abundant nucleation sites that lead to surface growth instead of NW growth. Figure 9.3 (a) shows an atomic force microscope (AFM) topograph of the InAs surface directly after layer transfer to SiO<sub>2</sub>/Si with a rms surface roughness of ~ 9 nm. When 40 nm diameter Au colloids were deposited atop this surface and OMVPE growth was performed at conditions optimized for InAs NW growth on InAs (111)B surfaces, no NW growth was observed. Surface modification/repair is thus necessary for achieving NW growth. To obtain a surface suitable for NW growth, the samples were wet etched in a HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O (100:1:100) solution and thin film OMVPE growth was performed afterwards. The etching solution initially self-heated to ~ 47 °C and was left to cool down in a water bath to ~ 27 °C, at which a 1 nm/s etch rate was achieved. Thin film OMVPE growth followed for ~ 10 min leading to a reduced rms surface roughness of ~ 3 nm and a planarized InAs surface as shown in the AFM topograph in Figure 9.3 (b). 40 nm diameter Au colloids were deposited afterwards and OMVPE growth was performed for 6 min leading to efficient NW growth. Figure 9.3 (c) shows cross-sectional FE-SEM images of InAs NWs grown on InAs/SiO<sub>2</sub>/Si. This demonstrates that etching the damaged InAs layer and planarization of the transferred InAs surface enable InAs NW growth. Such surfaces also enable uniform NW growth with controlled lengths and diameters under conditions specified and discussed in chapter 3. For this, e-beam lithography was used to pattern a double layer of positive e-beam resist (MMA/PMMA) followed by 25 nm Au e-beam evaporation and lift off. Figure 9.4 (a) and (b) show FE-SEM images of ordered InAs NWs grown on InAs/SiO<sub>2</sub>/Si with ~ 60 nm diameter and 4 μm interspacing.



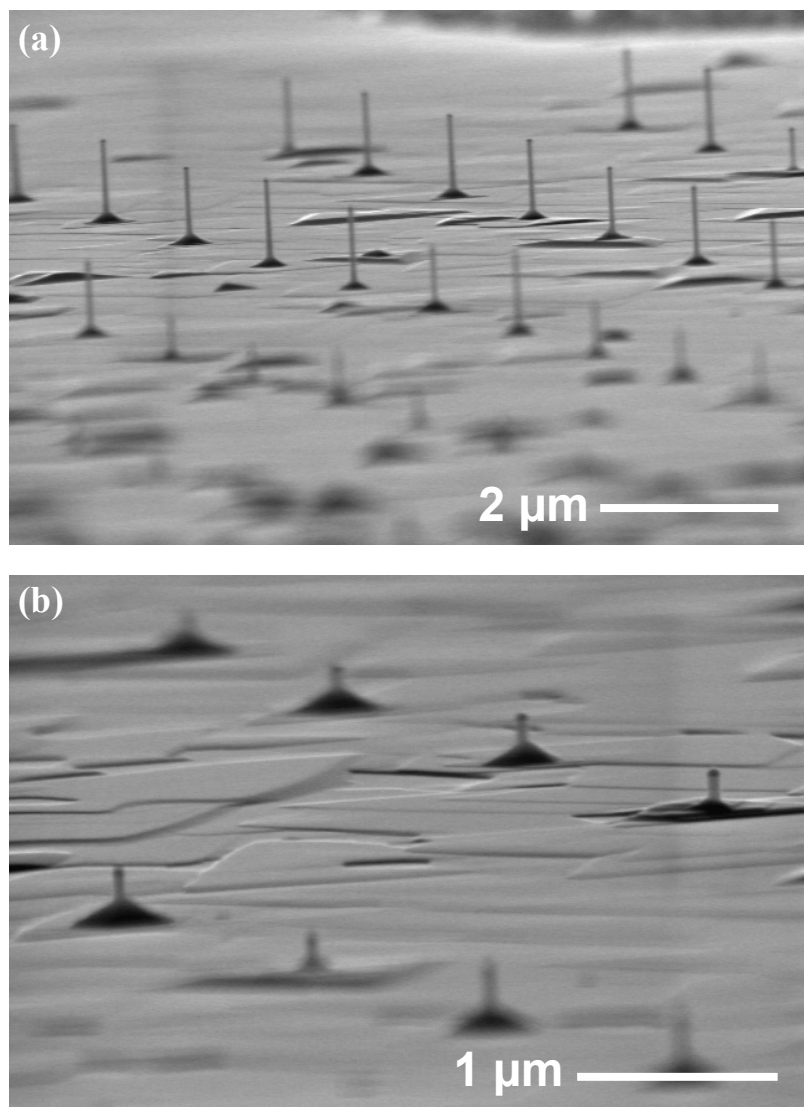


Figure 9.4. (a) and (b)  $85^\circ$  FE-SEM images of ordered InAs NW arrays grown on InAs/SiO<sub>2</sub>/Si.

For practical device integration into functional systems, electrical isolation between individual NW devices is necessary. After growth of the NW array shown in Figure 4.9 (b), we use another e-beam lithography step to pattern resist discs, aligned and centered on the InAs NW. Wet chemical etching in HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O solution was then used to etch the InAs layer down exposing the SiO<sub>2</sub> surface in the unprotected regions. Figures 9.5 (a) and (b) show FE-SEM images after the InAs etching step illustrating the ordered vertical InAs NW arrays on isolated InAs discs. This constitutes the first demonstration of individually addressable NWs. In addition, this whole structure is integrated on a Si substrate. Figure 9.5 (c) shows a close up FE-SEM image of an individual InAs NW at the center of an InAs disc on SiO<sub>2</sub> surface that is electrically isolated from other NWs in the array. The diameter of the InAs disc can be controlled by e-beam lithography and can be used to achieve low resistance ohmic contacts to the InAs NWs on SiO<sub>2</sub> substrate. This is necessary as InAs NWs grown directly on Si show non-linear  $I$ - $V$  characteristics when current is injected from the NW into the Si substrate and vice-versa, due to energy band-edge offsets at the InAs/Si heterointerface.<sup>26</sup>

The whole fabrication and growth processes presented here demonstrates electrical isolation of vertical III-V NWs integrated to Si substrates with a simple geometry and physics of operation for potential devices such as vertical III-V FETs on Si. The set back for this process is the requirement of extremely flat InAs and SiO<sub>2</sub> surfaces. 1 nm or larger rms surface roughness on either InAs or SiO<sub>2</sub> prevents bonding of the InAs layers to Si.

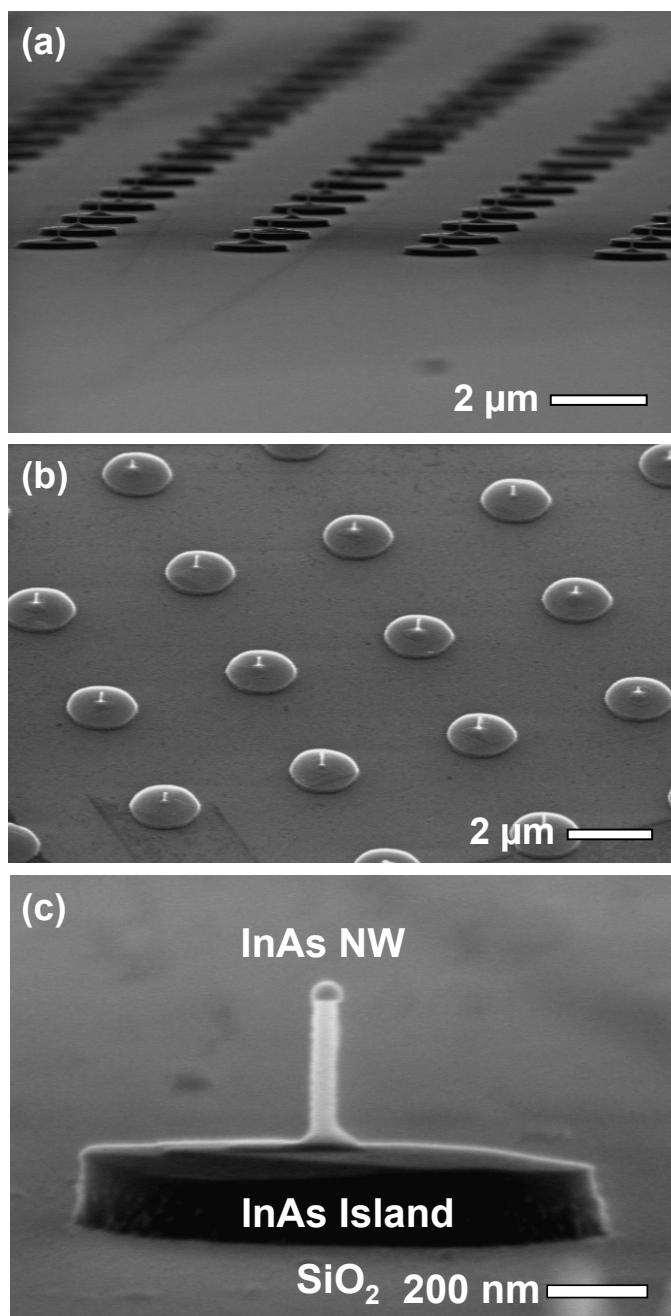


Figure 9.5. (a) 85° and (b) 45° angle-view FE-SEM images of vertical and electrically isolated InAs NWs on SiO<sub>2</sub>/Si. (c) Zoom-in FE-SEM image of an InAs NW with an InAs island at its base, sitting on SiO<sub>2</sub> substrate and electrically isolated for individual NW addressing.

## 9.4 Concluding Remarks

In this chapter, we briefly discussed current available methods and techniques for NW integration, none of which is ideal for practical 3D devices that may be inserted in future technology nodes. We presented a novel scheme for NW integration on Si substrates that counterparts SOI, and extends its concept to high performance III-V NWs on Si. This work also illustrates the first vertical and electrically isolated NWs with device architecture suitable for practical III-V NWFETs on Si. The capability of III-V NW growth on insulator on Si enables heterogeneous integration to CMOS technology for hybrid information processing. Specifically for electronic applications, the geometry of the NW permits the realization of surround-gate devices with better control over the channel electrostatics as the FET device dimensions scale further. The vertical surround-gate NWFET devices have been demonstrated by several groups using different materials. In order to realize vertical NW circuits and systems, a number of fundamental and technology related issues need to be addressed in time. These include (i) precise control over the NW morphology, crystallinity, and growth direction as well as accurate placement or growth of NWs at specified locations with high yield and reproducibility over large areas, (ii) integration to Si technology mainstream together with electrical isolation and individual addressability (as depicted in Figure 9.6 (b)) to allow versatile functionality, (iii) reduction of parasitic series- and metal contact-resistances at the source and drain regions as well as reduction of parasitic capacitances of contact leads (source/drain/gate) when integrated in 3D, and (iv) overcoming detrimental effects of surface states and improving the high-k III-V interface. As some of these issues also

evolve in the context of CMOS technology, research on NWs is going to benefit as well as contribute to addressing and overcoming these limitations.

Part of this chapter has been submitted for publication in *Appl. Phys. Lett.* 2008, S. A. Dayeh, P. Chen, Y. Jing, E. T. Yu, S. S. Lau, and D. Wang. The dissertation author is the first author of this paper.

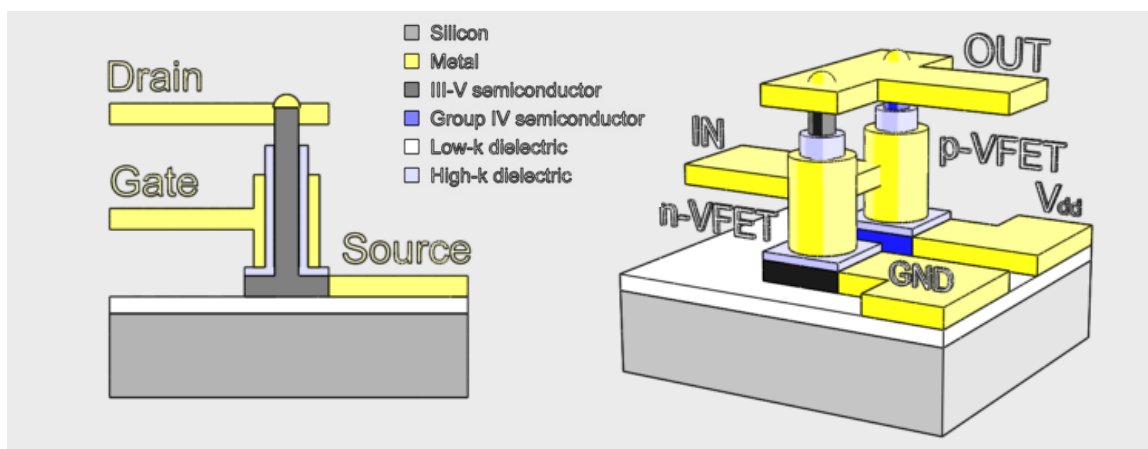


Figure 9.6. (a) Side-view cartoon of a vertical NWFET on insulator on Si. (b) Cartoon of vertical NWFET integration for complimentary function in an inverter configuration. The presence of the low-k dielectric atop Si allows NW isolation for versatile functionality.

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## Appendix I -- MATLAB Scripts for Calculating the 1D Electronic Properties in InAs Semiconductor Nanowires

### A.1 Plotting of the Radial Wavefunctions and E(k) Diagrams:

**%Constant Definitions**

```
clear all;
hbar=1.055e-34;Kb=1.38e-23;T=300;ni=1e15;
mh=0.41*9.1e-31;mn=0.023*9.1e-31;Eg=0.35*1.6e-19;
Ec=0.35*1.6e-19;Ev=0;Ei=Ec/2+3*Kb*T*log(mh/mn)/4;
```

**%75 nm Diameter InAs Nanowire is assumed**

```
r=35e-9;Lz=4e-6;
q=1.6e-19;m=mn;
n=1;
kz=n*pi/Lz;

x=0:0.1:20;
z(1,length(x))=0;t=0;d=0;
for i=0:1:10,
    xi=polypoly(x,Besselj(i,x),x,z);
    l=length(xi);
    for t=1:l,
        if xi(t,1)>1,
            d=d+1;
            xj(1,d)=xi(t,1);
        end
    end
end
```

```
x_m_n=sort(xj)/r;
E=Ec+hbar^2/2/m.*(x_m_n.^2+(pi/Lz)^2);
```

**% A 105 meV Ef is assumed; N is the number of modes whose value can be found in the workspace**

```
N=0;Emax=Ec+0.105*q;
t=0;
for i=1:length(x_m_n),
    if E(i)<Emax,
        t=t+1;
        xmode(t)=x_m_n(i),
    end
end
```



```

    Emode(t)=E(i);
    N=N+1;
end
end

```

### % Plot of the Radial Wavefunctions

```

figure (1);
rho=-37.5:0.01:37.5;
plot(rho,Besselj(0,xmode(1)*rho*1e-9),rho,Besselj(0,xmode(4)*rho*1e-9),rho,Besselj(0,xmode(9)*rho*1e-9),rho,Besselj(1,xmode(2)*rho*1e-9),rho,Besselj(1,xmode(6)*rho*1e-9),rho,Besselj(2,xmode(3)*rho*1e-9),rho,Besselj(2,xmode(8)*rho*1e-9),rho,Besselj(3,xmode(5)*rho*1e-9),rho,Besselj(4,xmode(7)*rho*1e-9),rho,Besselj(5,xmode(10)*rho*1e-9));Title('80nm');xlabel('z(nm)');
n=-150:0.1:150;kz=n*pi/Lz;
E1=(Ec+hbar^2/2/m.*(xmode(1).^2+(n.*pi/Lz).^2))./q;
E2=(Ec+hbar^2/2/m.*(xmode(2).^2+(n.*pi/Lz).^2))./q;
E3=(Ec+hbar^2/2/m.*(xmode(3).^2+(n.*pi/Lz).^2))./q;
E4=(Ec+hbar^2/2/m.*(xmode(4).^2+(n.*pi/Lz).^2))./q;
E5=(Ec+hbar^2/2/m.*(xmode(5).^2+(n.*pi/Lz).^2))./q;
E6=(Ec+hbar^2/2/m.*(xmode(6).^2+(n.*pi/Lz).^2))./q;
E7=(Ec+hbar^2/2/m.*(xmode(7).^2+(n.*pi/Lz).^2))./q;
E8=(Ec+hbar^2/2/m.*(xmode(8).^2+(n.*pi/Lz).^2))./q;
E9=(Ec+hbar^2/2/m.*(xmode(9).^2+(n.*pi/Lz).^2))./q;
E10=(Ec+hbar^2/2/m.*(xmode(10).^2+(n.*pi/Lz).^2))./q;

```

### % E(k) Plot

```

figure (2);
plot(kz*1e2,E1*1e3,kz*1e2,E2*1e3,kz*1e2,E3*1e3,kz*1e2,E4*1e3,kz*1e2,E5*1e3,kz*1e2,E6*1e3,kz*1e2,E7*1e3,kz*1e2,E8*1e3,kz*1e2,E9*1e3,kz*1e2,E10*1e3);

```

## A.2 Calculating the 1D Free Carrier Concentration in an InAs Nanowire

### %Constant Definitions

```

clear all;
hbar=1.055e-34;Kb=1.38e-23;T=300;ni=1e15;
mh=0.41*9.1e-31;mn=0.023*9.1e-31;Eg=0.35*1.6e-19;
Ec=0.35*1.6e-19;Ev=0;Ei=Ec/2+3*Kb*T*log(mh/mn)/4;

```

### %Wire dimensions

```

r=37.5e-9;Lz=2e-6;

```

```

q=1.6e-19;m=mn;
n=1;
kz=n*pi/Lz;

%Determine the zeroes of Bessel's function
x=0:0.1:20;
z(1,length(x))=0;t=0;d=0;
for i=0:1:10,
    xi=polyxpoly(x,besselj(i,x),x,z);
    l=length(xi);
    for t=1:1:l,
        if xi(t,1)>1,
            d=d+1;
            xj(1,d)=xi(t,1);
        end
    end
end

%Determine the number of modes
x_m_n=sort(xj)/r;
E=Ec+hbar^2/2/m.*(x_m_n.^2+(pi/Lz)^2);

N=0;Emax=Ec+0.105*q;

for i=1:1:length(E),
    if E(i)<Emax,
        N=N+1;
    end
end

%Determine the carrier concentration ns form the workspace
Ns=0;Ef=Ec+0.105*q;dE=Ec/100;Nc=1.16e17;k=1;l=0;gc=0;d=0;
for l=1:1:42,
    Em=E(l+1);
    En=E(l);
    dE=hbar^2/2/m.*((pi/Lz)^2);
    if En<Ef,
        for EE=En:dE:Em,
            d=d+1;
            En=En+hbar^2/2/m.*((pi/Lz)^2);
            if l==1,
                gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2;
            end
            if l==2,
                gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-2;
            end
        end
    end
end

```

```

end
if l==3,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2;
end
if l==4,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(4)))/pi/hbar*1e-2;
end
if l==5,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(4)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(5)))/pi/hbar*1e-2;
end
if l==6,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(4)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(6)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(6)))/pi/hbar*1e-2;
end
if l==7,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(4)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(5)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(6)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(7)))/pi/hbar*1e-2;
end
if l==8,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(4)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(5)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(6)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(7)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(8)))/pi/hbar*1e-2;
end
if l==9,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(4)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(5)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(6)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(7)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(8)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(9)))/pi/hbar*1e-2;
end
if l==10,
    gc=sqrt(2*mn/(En-E(1)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(2)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(3)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(4)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(5)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(6)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(7)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(8)))/pi/hbar*1e-
2+sqrt(2*mn/(En-E(9)))/pi/hbar*1e-2+sqrt(2*mn/(En-E(10)))/pi/hbar*1e-2;
end

```



```

        Ns=Ns+dE.*fc.*gc;
        Gc(d)=gc;
        ns(d)=Ns;
        en(d)=En;
    end

end

end

```

### A.3 Plotting the 1D Density of States in an InAs Nanowire

```

clear all;
m=0.023*9.1e-31;
hbar=1.055e-34;
q=1.6e-19;
L=2e-6;
W=80e-9;n=0;c=0;
l=0;
for nx=1:1:10,
    for ny=1:1:10,
        l=l+1;
        Emax(1,l)=hbar^2.*((nx)*(pi./W).^2+(ny)*(pi./W).^2)/2/m/q;
    end
end
Emax=sort(Emax);
deg=0;
l=1;k=1;deg(1,1)=1;
for i=1:1:nx*ny-1,
    if Emax(1,i)==Emax(1,i+1),
        k=k+1;
        Em(1,l)=Emax(1,i);
        deg(1,l)=k;
    else Em(1,l)=Emax(1,i);l=l+1;k=1;    %To make sure the first energy is recorded
    end
end
for j=1:1:length(Em)/2,
    if j<length(Em),
        Emx=Em(1,j+1);
    end
    dg=deg(1,j);
    if j==1, Emin=0;
    else Emin=Em(1,j);
    end

```

```

n=0;
for dE=Emin:0.0001:Emx,
    if j==1,
        n=0;plot(dE,n,'!');hold on;
    else
        kf=sqrt(2*m*dE*q/hbar^2);
        Lambda_f=2*pi./kf;
        n=dg.*sqrt(2*m/q/(dE-Emin))/pi/hbar*q*1e-9;
        plot(dE,n,'!');hold on;
    end
xlabel('E (eV)');ylabel('1D DOS (eV-1 nm-1)');title('1D Density of States at
Equilibrium');
end
end
end

```

## Appendix II – Silvaco Atlas Scripts for Simulating the Transport Properties of InAs Nanowires

### AII.1 Script for Calculating the Self-Consistent Schrödinger-Poisson Solutions in a 70 nm InAs Slab:

```
# Schrodinger-Poisson solution at zero bias
#
go atlas
#
mesh
#
x.mesh loc=0.0 spac=0.04
x.mesh loc=5.0 spac=0.04

y.mesh loc=0.0 spac=0.01
y.mesh loc=0.07 spac=0.005
y.mesh loc=0.14 spac=0.001
y.mesh loc=0.21 spac=0.001
y.mesh loc=0.28 spac=0.005
y.mesh loc=0.35 spac=0.01

region num=1 material=Si3N4 y.min=0.0 y.max=0.14
region num=2 material=InAs y.min=0.14 y.max=0.21
region num=3 material=Si3N4 y.min=0.21 y.max=0.35

#
elec num=1 material=Titanium name=source x.min=0.0 x.max=0.5 y.min=0.139
y.max=0.14
elec num=2 material=Aluminum name=gate x.min=2.0 x.max=3.0 y.min=0.0
y.max=0.13
elec num=3 material=Titanium name=drain x.min=4.5 x.max=5.0 y.min=0.139
y.max=0.14
elec num=2 material=Aluminum name=gate x.min=2.0 x.max=3.0 y.min=0.22
y.max=0.35
elec num=1 material=Titanium name=source x.min=0.0 x.max=0.5 y.min=0.210
y.max=0.211
elec num=3 material=Aluminum name=drain x.min=4.5 x.max=5.0 y.min=0.210
y.max=0.211

material material=InAs affinity=4.9
```

```

interf qf=1e12
doping uniform y.min=0.14 y.max=0.21 n.type conc=5.e16

model schrodinger.n eigens=20 fixed.fermi ^calc.fermi qy.min=0.05 qy.max=0.35
qx.min=2.0 qx.max=3.0 fermi new.eig num.direct=1 qminconc=1.0e13 srh incomplete

method itlim=20 nblockit=30 trap maxtrap=6 vsatmod.inc=0.01 carriers=0

output con.band val.band eigens=5

solve init

solve vgate=0
save outf=trr.str
tonyplot trr.str

log outf=trr_1.log

quit

```

## **All.2 Script for Simulating the Effects of Polarization Charges in Wurtzite InAs**

### **Nanowires:**

```

# Alteration of WZ-ZB crystal structure effect on the electronic properties
# of an InAs NW FET

```

```

go atlas

```

```

mesh

```

x.mesh	loc=0.0	spac=0.1
x.mesh	loc=0.8	spac=0.1
x.mesh	loc=0.9	spac=0.01
x.mesh	loc=0.99	spac=0.0008
x.mesh	loc=1.01	spac=0.0008
x.mesh	loc=1.0135	spac=0.0008
x.mesh	loc=1.028	spac=0.006
x.mesh	loc=1.042	spac=0.0008
x.mesh	loc=1.0455	spac=0.0008
x.mesh	loc=1.060	spac=0.006
x.mesh	loc=1.074	spac=0.0008
x.mesh	loc=1.0775	spac=0.0008



x.mesh	loc=1.092	spac=0.006
x.mesh	loc=1.106	spac=0.0008
x.mesh	loc=1.1095	spac=0.0008
x.mesh	loc=1.124	spac=0.006
x.mesh	loc=1.138	spac=0.0008
x.mesh	loc=1.1415	spac=0.0008
x.mesh	loc=1.156	spac=0.006
x.mesh	loc=1.17	spac=0.0008
x.mesh	loc=1.1735	spac=0.0008
x.mesh	loc=1.188	spac=0.006
x.mesh	loc=1.202	spac=0.0008
x.mesh	loc=1.2055	spac=0.0008
x.mesh	loc=1.220	spac=0.006
x.mesh	loc=1.234	spac=0.0008
x.mesh	loc=1.2375	spac=0.0008
x.mesh	loc=1.252	spac=0.006
x.mesh	loc=1.266	spac=0.0008
x.mesh	loc=1.2695	spac=0.0008
x.mesh	loc=1.284	spac=0.006
x.mesh	loc=1.298	spac=0.0008
x.mesh	loc=1.3015	spac=0.0008
x.mesh	loc=1.316	spac=0.006
x.mesh	loc=1.33	spac=0.0008
x.mesh	loc=1.3335	spac=0.0008
x.mesh	loc=1.348	spac=0.006
x.mesh	loc=1.362	spac=0.0008
x.mesh	loc=1.3655	spac=0.0008
x.mesh	loc=1.380	spac=0.006
x.mesh	loc=1.394	spac=0.0008
x.mesh	loc=1.3975	spac=0.0008
x.mesh	loc=1.4	spac=0.0008
x.mesh	loc=1.5	spac=0.01
x.mesh	loc=1.6	spac=0.1
x.mesh	loc=2.4	spac=0.1

y.mesh	loc=0	spac=0.01
y.mesh	loc=0.047	spac=0.01
y.mesh	loc=0.14	spac=0.005
y.mesh	loc=0.2	spac=0.005
y.mesh	loc=0.3	spac=0.01
y.mesh	loc=0.4	spac=0.01

region num=1 material=Si3N4 y.min=0.0 y.max=0.14

region num=2 material=SiO2 y.min=0.2 y.max=0.3

region num=3 material=InP x.min=0 x.max=1.01 y.min=0.14 y.max=0.2

```

region num=4 material=InAs x.min=1.01 x.max=1.0135 y.min=0.14 y.max=0.2
region num=5 material=InP x.min=1.0135 x.max=1.042 y.min=0.14 y.max=0.2
region num=6 material=InAs x.min=1.042 x.max=1.0455 y.min=0.14 y.max=0.2
region num=7 material=InP x.min=1.0455 x.max=1.074 y.min=0.14 y.max=0.2
region num=8 material=InAs x.min=1.074 x.max=1.0775 y.min=0.14 y.max=0.2
region num=9 material=InP x.min=1.0775 x.max=1.106 y.min=0.14 y.max=0.2
region num=10 material=InAs x.min=1.106 x.max=1.1095 y.min=0.14 y.max=0.2
region num=11 material=InP x.min=1.1095 x.max=1.138 y.min=0.14 y.max=0.2
region num=12 material=InAs x.min=1.138 x.max=1.1415 y.min=0.14 y.max=0.2
region num=13 material=InP x.min=1.1415 x.max=1.17 y.min=0.14 y.max=0.2
region num=14 material=InAs x.min=1.17 x.max=1.1735 y.min=0.14 y.max=0.2
region num=15 material=InP x.min=1.1735 x.max=1.202 y.min=0.14 y.max=0.2
region num=16 material=InAs x.min=1.202 x.max=1.2055 y.min=0.14 y.max=0.2
region num=17 material=InP x.min=1.2055 x.max=1.234 y.min=0.14 y.max=0.2
region num=18 material=InAs x.min=1.234 x.max=1.2375 y.min=0.14 y.max=0.2
region num=19 material=InP x.min=1.2375 x.max=1.266 y.min=0.14 y.max=0.2
region num=20 material=InAs x.min=1.266 x.max=1.2695 y.min=0.14 y.max=0.2
region num=21 material=InP x.min=1.2695 x.max=1.298 y.min=0.14 y.max=0.2
region num=22 material=InAs x.min=1.298 x.max=1.3015 y.min=0.14 y.max=0.2
region num=23 material=InP x.min=1.3015 x.max=1.33 y.min=0.14 y.max=0.2
region num=24 material=InAs x.min=1.33 x.max=1.3335 y.min=0.14 y.max=0.2
region num=25 material=InP x.min=1.3335 x.max=1.362 y.min=0.14 y.max=0.2
region num=26 material=InAs x.min=1.362 x.max=1.3655 y.min=0.14 y.max=0.2
region num=27 material=InP x.min=1.3655 x.max=1.394 y.min=0.14 y.max=0.2
region num=28 material=InAs x.min=1.394 x.max=1.3975 y.min=0.14 y.max=0.2
region num=29 material=InP x.min=1.3975 x.max=2.4 y.min=0.14 y.max=0.2
region num=30 material=Si y.min=0.3 y.max=0.4
#
elec num=1 material=Titanium name=source x.min=0.0 x.max=1.0 y.min=0.07
y.max=0.14
elec num=2 material=Titanium name=drain x.min=1.4 x.max=2.4 y.min=0.07
y.max=0.14
elect num=3 material=Aluminum name=gate y.min=0.38 y.max=0.4
contact name=drain current
contact name=drain resistance=5550
contact name=source current
contact name=source resistance=5550
#
material material=InAs affinity=4.9 mun=1700 EG300=0.34 epsinf=15.15
material material=InP affinity=4.8194 mun=1700 EG300=0.38 epsinf=15.5
material material=Titanium affinity=5.1
material material=SiO2 affinity=0.98 EG300=9.0
#
interf qf=1e12 x.min=0 x.max=2.4 y.min=0.14 y.max=0.142

```

interf qf=1e12 x.min=0 x.max=2.4 y.min=0.198 y.max=0.2

doping uniform x.min=0 x.max=2.4 y.min=0.14 y.max=0.2 n.type conc=5e16

doping uniform y.min=0.3 y.max=0.4 n.type conc=1e19

interface charge=-1e13 S.S x.min=1.01 x.max=1.01 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.0135 x.max=1.0135 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.042 x.max=1.042 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.0455 x.max=1.0455 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.074 x.max=1.074 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.0775 x.max=1.0775 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.106 x.max=1.106 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.1095 x.max=1.1095 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.138 x.max=1.138 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.1415 x.max=1.1415 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.17 x.max=1.17 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.1735 x.max=1.1735 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.202 x.max=1.202 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.2055 x.max=1.2055 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.234 x.max=1.234 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.2375 x.max=1.2375 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.266 x.max=1.266 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.2695 x.max=1.2695 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.298 x.max=1.298 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.3015 x.max=1.3015 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.33 x.max=1.33 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.3335 x.max=1.3335 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.362 x.max=1.362 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.3655 x.max=1.3655 y.min=0.14 y.max=0.2

interface charge=-1e13 S.S x.min=1.394 x.max=1.394 y.min=0.14 y.max=0.2

interface charge=1e13 S.S x.min=1.3975 x.max=1.3975 y.min=0.14 y.max=0.2

models srh print numcarr=2

method climitt=1e-4 maxtrap=10

output con.band val.band

#

#Solving for Output Curves

solve init

solve vgate=0

solve vgate=0 outf=wzzbpol\_tmp1

solve vgate=-2

solve vgate=-2.5

```
solve vgate=-5 outf=wzzbpol_tmp2
solve vgate=-10 outf=wzzbpol_tmp3
solve vgate=-15 outf=wzzbpol_tmp4
solve vgate=-20 outf=wzzbpol_tmp5
load infile=wzzbpol_tmp1
solve vgate=0
solve vgate=1
solve vgate=2.5
solve vgate=5 outf=wzzbpol_tmp6
solve vgate=10 outf=wzzbpol_tmp7
solve vgate=15 outf=wzzbpol_tmp8
solve vgate=20 outf=wzzbpol_tmp9
#
load infile=wzzbpol_tmp1
log outf=wzzbpol_1.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
##
load infile=wzzbpol_tmp2
log outf=wzzbpol_2.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
##
load infile=wzzbpol_tmp3
log outf=wzzbpol_3.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
##
load infile=wzzbpol_tmp4
log outf=wzzbpol_4.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
##
load infile=wzzbpol_tmp5
log outf=wzzbpol_5.log
solve name=drain vdrain=0 vfinal=0.1 vstep=0.01
#save outf=wzzbpol1e132p1e12n20.str
#tonyplot wzzbpol1e132p1e12n20.str
#
#quit
load infile=wzzbpol_tmp6
log outf=wzzbpol_6.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
#
load infile=wzzbpol_tmp7
log outf=wzzbpol_7.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
#
load infile=wzzbpol_tmp8
```

```

log outf=wzzbpol_8.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
#
load infile=wzzbpol_tmp9
log outf=wzzbpol_9.log
solve name=drain vdrain=0 vfinal=0.5 vstep=0.01
###
tonyplot -overlay wzzbpol_1.log wzzbpol_2.log wzzbpol_3.log wzzbpol_4.log
wzzbpol_5.log wzzbpol_6.log wzzbpol_7.log wzzbpol_8.log wzzbpol_9.log
###

#Solving for Transfer Curves

solve init
solve vdrain=0
solve vdrain=0.1
solve vgate=0
solve vgate=-1
solve vgate=-2.5
solve vgate=-5
solve vgate=-10
solve vgate=-20
log outf=wzzbj_idsvgs.log
solve name=gate vgate=-20 vfinal=20 vstep=5
###
tonyplot wzzbj_idsvgs.log
#
quit

```

### **AII.3 Script for Electro-Thermal Simulation in an InAs Nanowire:**

```

# self heat problem with large substrate thickness "350um"
# and 200um wide electrodes...
# The mobility and carrier concentration and contact resistance are adjusted
# to obtain the same current density of the device used for field-dependent
#transport properties at an external voltage of 2.1V where the current starts
# to degrade...
go atlas
#
mesh

x.mesh loc=0      spac=10
x.mesh loc=150   spac=5

```

```

x.mesh loc=180    spac=1
x.mesh loc=200    spac=0.05
x.mesh loc=203.5  spac=0.05
x.mesh loc=220    spac=1
x.mesh loc=255    spac=5
x.mesh loc=403.7  spac=10

```

```

y.mesh loc=0.0    spac=0.03
y.mesh loc=0.07   spac=0.03
y.mesh loc=0.14   spac=0.008
y.mesh loc=0.23   spac=0.008
y.mesh loc=0.83   spac=0.2
y.mesh loc=1.2    spac=0.5
y.mesh loc=20     spac=5
y.mesh loc=50     spac=10
y.mesh loc=100    spac=20
y.mesh loc=350    spac=35

```

```

region  num=1 material=Si3N4 y.min=0.0 y.max=0.14
region  num=2 material=InAs  y.min=0.14 y.max=0.23
region  num=3 material=SiO2  y.min=0.23 y.max=0.83
region  num=4 material=Si     y.min=0.83 y.max=350
region  num=5 material=Al     x.min=0 x.max=200 y.min=0.04 y.max=0.014
region  num=6 material=Al     x.min=203.6 x.max=403.7 y.min=0.04 y.max=0.014

```

```
#
```

```

elec    num=1 material=Titanium name=source x.min=0 x.max=200.0 y.min=0.13
y.max=0.14
elec    num=2 name=gate x.min=201.7 x.max=202.7 y.min=0.0 y.max=0.07
elec    num=3 material=Titanium name=drain x.min=203.6 x.max=403.5 y.min=0.13
y.max=0.14
electrode substrate

```

```

contact name=drain current
contact name=drain resistance=350
contact name=source current
contact name=source resistance=350

```

```

material material=InAs affinity=4.9 mun=16000
material material=Titanium affinity=5.1

```

```

interf qf=2.7E12 x.min=0 x.max=400
doping uniform y.min=0.14 y.max=0.23 n.type conc=5e16
doping uniform y.min=0.83 y.max=10 n.type conc=1.e19

```

```

#models      arora consrh auger bgn lat.temp
#impact      selb
models lat.temp

output con.band val.band

thermcontact number=1 y.min=350.0 ext.temper=300

#thermcontact number=2 x.min=0.0 x.max=1.0 y.min=0.04 y.max=0.05 ext.temper=300
#thermcontact number=3 x.min=4.6 x.max=5.6 y.min=0.04 y.max=0.05 ext.temper=300

solve outfile=temp.str
solve init
solve vgate=0
solve vgate=0.125
solve vgate=0.25
solve vgate=0.5
solve vgate=1
solve vgate=2
solve vgate=4
solve vdrain=0.1
solve vdrain=0.25
solve vdrain=0.5
solve vdrain=1.0
solve vdrain=1.25
solve vdrain=1.5
solve vdrain=1.75
solve vdrain=2.0
solve vdrain=2.1
solve vdrain=2.2
solve vdrain=2.3
solve vdrain=2.4
solve vdrain=2.5

save outf=selfheat.str
tonyplot selfheat.str

log outf=selfheat.log
quit

```

#### **AII.4 Script for 3D Simulation of an InAs-GaAs Heterostructure Nanowire:**

#This script allows potential and carrier concentration profiling from a 3D structure; IV curves could also be simulated using the same script and methods in AII.2

```
go devedit simflags="-3d"  
#Read 3D file from Devedit3d and start Atlas  
go atlas  
mesh inf=inasgaas0.str  
material material=InAs affinity=4.9  
material material=GaAs affinity=4.07  
material align=0.6  
contact name=gate work=4.95  
material material=InAs affinity=4.9  
  
model srh print  
model material=InAs conmob  
method gummel newton itlim=20 trap maxtrap=6  
output band.temp con.band val.band band.par  
  
solve init  
solve vgate=0  
solve vgate=-0.1  
solve vgate=-0.2  
solve vgate=-0.6  
solve vgate=-1  
solve vgate=-2  
log outf=planar_1.log  
solve vdrain=0.0  
solve vdrain=0.1  
solve vdrain=0.2  
solve vdrain=0.4  
solve vdrain=0.6  
solve vdrain=1.0  
solve vdrain=2.0  
save outf=heteronwb.str  
tonyplot3d heteronwb.str  
quit
```