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Electronic Transport in Novel Graphene Nanostructures

by

William Joy Gannett

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Physics

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Alex Zettl, Chair

Professor Feng Wang

Professor Oscar Dubon

Fall 2012

Electronic Transport in Novel Graphene Nanostructures

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Abstract

Electronic Transport in Novel Graphene Nanostructures

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Graphene, a single sheet of sp^2-bonded carbon atoms, is a two-dimensional material with an array of unique electronic, chemical, and mechanical properties. Applications including high performance transistors, chemical sensors, and composite materials have already been demonstrated. The introduction of chemical vapor deposition growth of monolayer graphene was an important step towards scalability of such devices. In addition to scalability, the exploration and application of these properties require the fabrication of high quality devices with low carrier scattering. They also require the development of unique geometries and materials combinations to exploit the highly tunable nature of graphene.

This dissertation presents the synthesis of materials, fabrication of devices, and measurement of those devices for three previously unexplored types of graphene devices. The first type of device is a field effect transistor made from chemical vapor deposited (CVD) graphene on hexagonal boron nitride (hBN) substrates. We demonstrate a significant improvement in carrier mobility from hBN substrates and are able to explore the sources of scattering in CVD graphene. The second type of device, fluorinated graphene transistors, allows us to examine doping and disorder effects from fluorination of the graphene crystal as well as electronic transport through unfluorinated folds in the graphene. With the third type of device we demonstrate a new route to graphene nanoribbon devices using both hBN flakes and BN nanotubes that may reduce disorder and allow precise measurements of quantum phenomena in graphene nanoribbons.

To all the great teachers I've had,
My parents first among them

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Acknowledgments

I'd like to begin by thanking my advisor, Alex Zettl, who has been a constant source of ideas for experiments and techniques throughout my graduate research. Alex's confidence in his researchers and his support of our ideas and goals has made his group a great place to work. I wish him the best in all of his pursuits, whether in lab or on mountaintops.

I'd also like to thank Gavi Begtrup and Brian Kessler, the two senior graduate students with whom I worked the closest. Coworkers and friends, I owe them for teaching me many lab techniques and for making long stretches in lab more bearable my first few years. I hope I was able to be as helpful to the graduate students below me.

The research presented herein could not have been performed without the help of Will Regan. He contributed ideas, interpretations, techniques, and more than a few late nights in lab. I have fond memories of drinking coffee, refining our catchphrases, and discussing politics, comedy, and music. I am confident that if anyone can figure out how to solve the energy crisis, it's him.

Many other members of the Zettl group have helped over the years. In no particular order, I'd like to thank Benji Alemán, Jian Hao Chen, Kris Erickson, Ashley Gibb, Çağlar Girit, Kwanpyo Kim, Willi Mickelson, and Seita Onishi. I'd also like to thank Allen Sussman for tolerating Will Regan and me.

Big thanks to Anne and Gee Gee for cheerfully keeping all of the important paperwork in order and making sure the wheels turn behind the scenes.

Thanks to Joey, Ryan, and Westin for so many evenings on the roof discussing science, movies, beer, or the crazies at the next table.

Thanks to Nick for the same, and for four great years on Francisco Street. Lots of fun evenings, and a few truly excellent parties. Our mutually cultivated interests in food and cocktails will have a lasting influence (on me and others) for many years to come.

Thanks to former Zettl group labmates Henry and Keith. I'm glad we've been able to stay close while pursuing different paths.

Thanks to the trivia team. We were often the best but always the most entertaining.

Thanks to Megan for her understanding and support. Here's to so many great weekends in Berkeley and in Eureka and many more to come.

Finally, I'd like to thank my family and especially my parents for their support the last 28 years. This would not have been possible without them.

Chapter 1

Introduction

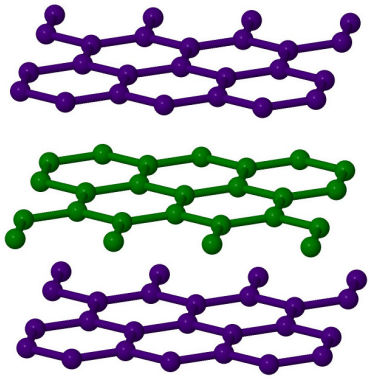

Figure 1.1: Graphite crystal lattice, showing layered structure

Graphite is ubiquitous in daily life, used as both a material for writing and a dry lubricant. Both of these applications benefit from graphite's crystal structure, seen schematically in figure 1.1. It consists of sheets of strongly bonded carbon atoms held together by weaker van der Waals interactions. The weak attraction between adjacent sheets allows them to slide smoothly over one another; this property enables graphite to lubricate sliding surfaces or slide over a writing surface.

A single sheet of the graphite crystal structure is called graphene and consists of carbon atoms that are sp^2-bonded to one another in a honeycomb shaped lattice. Because graphite has very strong bonds in two directions and very weak bonds in the third, it has highly anisotropic electronic, thermal, and optical properties [1, 2].

Graphene has risen to prominence as an interesting material for fundamental materials studies and applications due to its many unique physical properties. These include low carrier scattering, high mechanical strength, and a unique electronic structure, and many of these will be addressed in this dissertation.

1.1 Graphene history

As early as 1947, researchers were predicting some of the unique properties of graphene including its linear dispersion relation [1, 3]. Experimental investigations of these properties, however, did not follow for many years.

Boehm et al. demonstrated transmission electron microscopy (TEM) of few-layer samples produced by oxidation and exfoliation in 1962, but these were graphene oxide and not graphene [4]. In addition, their work was observational and did not make measurements beyond TEM micrographs. It was also shown in the 1970s and 80s that intercalation of graphite crystals with various other species could decouple the graphene layers and give the crystals very different properties from pure graphite [5].

The isolation of single sheets of graphene remained elusive into the new millennium. Philip Kim's group at Columbia had attempted to rub single sheets off a small graphite crystal with an AFM cantilever ("micromechanical exfoliation") but produced few-layer structures rather than graphene monolayers [6]. Walt de Heer's group at Georgia Tech had produced samples on silicon carbide by high temperature decomposition of the surface, but as of 2004 they were still multilayers [7].

In the end, it was Andre Geim's group at Manchester that first isolated graphene monolayers and performed electronic measurements on them [8, 9]. While it had not been the first attempt to fabricate samples of monolayer graphene, their fabrication technique (mechanical exfoliation, which will be addressed in section 3.1) seemed to spark the explosion of graphene research in 2005 that continues 7 years later.

The Manchester group fabricated their graphene samples by exfoliating graphite flakes with adhesive tape and transferring them to an oxidized silicon substrate. They identified the thinnest regions by optical microscopy, performed lithography to make contacts, and performed electronic measurements [8, 9]. The Nobel Prize in Physics in 2010 was awarded to Andre Geim and Konstantin Novoselov for this initial discovery as well as their subsequent exploration of its electronic properties, including its unique quantum Hall effect.

1.2 Unique properties

Much of the interest in graphene is due to its unique optical, mechanical, electronic, and chemical properties.

Graphene's in-plane sp^2 bonds give it a great deal of strength. Measurements by nanoindentation have found a Young's modulus of 1.0 TPa and a intrinsic strength of 130 GPa, making graphene "the strongest material ever measured" [10]. In principle, these properties combined with graphene's low mass density could lead to extremely high quality graphene resonators, although this has yet to be fully realized. Graphene's high strength has also led to its potential use in composite materials [11].

Graphene has a host of unique electronic properties. Its carrier concentration is

easily tunable from 10^{13} holes/cm^2 to 10^{13} electrons/cm^2, and even higher carrier concentrations are possible with chemical dopants or ionic gates. Concentrations less than 10^{11}/cm^2 are more difficult to achieve due to impurities and intrinsic disorder, which will be addressed later. Charge carriers in graphene also have a very high mobility, which allows measurement of phenomena such as the quantum Hall effect.

Graphene also has the unique distinction of being the easiest 2-D electron system to fabricate. The dimensionality of an electron gas has a strong influence on its properties, including emergent phenomena such as the integer and fractional quantum Hall effect and the quantum spin Hall effect. These effects were initially observed in two-dimensional electron gas systems (2DEGs) made at semiconductor interfaces. Some such measurements are possible in the inversion layer of silicon MOSFETs [12], but the most sophisticated were only achievable with epitaxially grown AlGaAs/GaAs heterostructures that form a 2DEG at their interface due to band bending [13]. Nobel prizes have been awarded for 2DEG samples made with each of these techniques.

With the introduction of graphene, a totally new method for 2DEG sample fabrication arose, accompanied by a completely new 2DEG band structure. Because of the high mobility of graphene samples and the relative insensitivity of carrier mobility to temperature, these effects can even be measured at room temperature [14].

1.3 Graphene research outline

When I began my graphene research with Brian Kessler, a fellow graduate student in the Zettl group, scalable growth of monolayer graphene films by chemical vapor deposition was extremely new. Our initial goal was to take advantage of the new scalability, make large batches of graphene devices, and measure them before and after various modifications, such as adding interesting functional groups or ferromagnetic stripes. We also wanted to reduce the carrier scattering in devices made with CVD graphene to allow scalable fabrication of devices that would exhibit more of graphene's exotic physics.

In chapter 2 I explore many of the physical properties of graphene in more detail. In chapter 3 I explain how graphene samples were fabricated, with an emphasis on CVD graphene growth and transfer. Chapters 4 through 7 each talk about a different project involving graphene devices, including graphene on boron nitride substrates and devices made from graphene folds. We were able to discover a much more scalable route to high mobility graphene devices (>10,000 cm^2/Vs) and fabricated and measured the highest mobility samples from chemical vapor deposited graphene at that time. We were also able to measure a variety of new graphene sample geometries and learned a great deal about graphene fluorination and nanoribbon fabrication.

Chapter 2

Graphene theory

2.1 Crystal structure

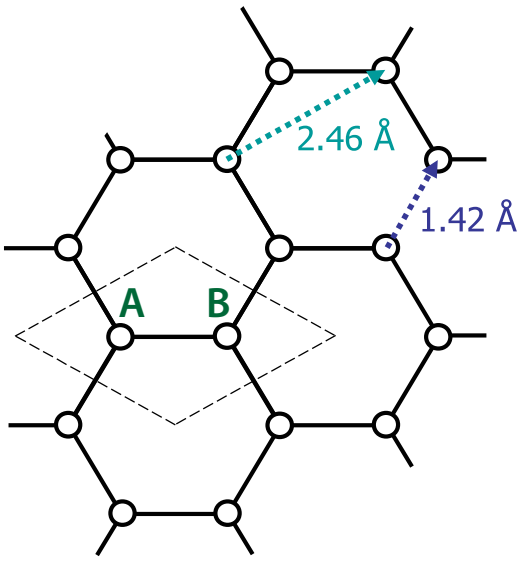

Figure 2.1: Schematic of graphene lattice, unit cell shown with dashed outline. The "A" and "B" atom locations in the unit cell are labeled.

The graphene crystal lattice consists of sp^2-bonded carbon atoms in a honeycomb arrangement, as seen in figure 2.1. The unit cell of graphene as shown here is a rhombus with internal angles of 60° and 120° and sides of length 2.461 Å [15]. Thus, the unit cell area is 5.245 Å^2 and the atomic areal density is 0.38 atoms/Å^2 or 3.81×10^{15} atoms/cm^2. When the graphene sheet is part of a graphite crystal, the stacked sheets are 3.37 Å apart [1]. The lowest energy stacking of the graphene sheets, as in graphite, is such that the lattice of adjacent individual sheets are alternatingly shifted

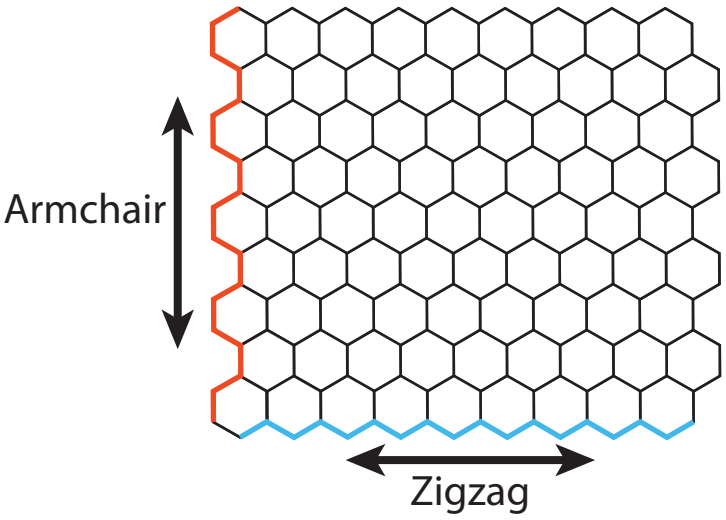

Figure 2.2: The two named directions and edges in graphene, armchair (shown in red) and zigzag (shown in blue).

by a third of a lattice constant, referred to as "AB" stacking or Bernal stacking. This can be seen in figure 1.1.

Graphene has two atoms per unit cell that are symmetric under inversion and reflection but not translations. As such, it is sometimes referred to as having two sublattices, A and B, each consisting of a triangular lattice of carbon atoms but shifted relative to each other. The A and B atoms are labeled in the unit cell in figure 2.1, and each sublattice is made up of the equivalent A or B sites in all other unit cells

While theoretical calculations often assume graphene to be an infinitely periodic crystal, actual samples always have edges. The edge structure of graphene monolayers can vary greatly from sample to sample, depending on the direction through the crystal and the chemical functionalization of the edge. The two simplest crystalline edge structures are zigzag and armchair, as shown in figure 2.2.[1] These edges are especially important for graphene nanostructures, such as nanoribbons, and in some cases may even dominate the electronic behavior.

2.2 Band structure

Starting from first principles, one can derive a band structure using the tight binding approximation [15].

[1] Usage of these terms for graphene sheets date back to at least 1989 [16].

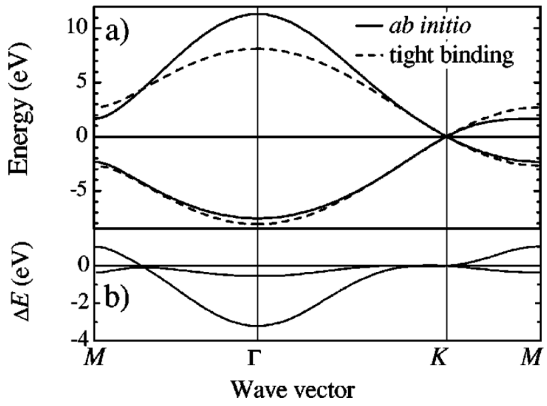

Figure 2.3: (a) Band structure of graphene calculated with both nearest-neighbor tight binding (dashed) and converged ab initio (solid) techniques. (b) Deviations of tight binding calculations from ab initio energies. From [15]

Tight binding using only nearest-neighbor hopping results in a band structure that is symmetric about zero energy, as seen in figure 2.3. This symmetry is incorrect, and second-hopping corrections to this give the band structure seen in figure 2.4 [15]. These calculations show an energy gap at the M-point of 4 eV and a gap at the Γ-point of almost 19 eV. The valence band is shown in blue and the conduction band in red.

The band structure is six-fold symmetric and exhibits no energy gap; the bands touch at the K- and K′-points. The Brillouin zone has six corners, but every corner is connected to two others by reciprocal lattice vectors. This means there are only two such unique "valleys" in the band structure. Alternatively, one can visualize the band structure in the reduced zone scheme where each corner only contains one third of a valley, and $6/3 = 2$ unique valleys.

A magnified view of a single K-point appears in figure 2.5. These points are commonly referred to as the Dirac points of graphene because the momentum-energy relationship is identical to the massless Dirac equation with a so-called "pseudospin" in place of the spin. The pseudospin degree of freedom is not an angular momentum but rather the phase relationship of the electron wavefunction between the two sublattices of graphene. This and the linear dispersion relation gives the wavefunction the same form as a relativistic spin-$\frac{1}{2}$particle.

The pseudospin is responsible for the suppression of carrier backscattering in graphene and thus also its high carrier mobility. Backscattering in graphene requires a carrier to be scattered from one valley to the other, but because of pseudospin differences between the valleys, the pseudospin must flip as well [17]. This requirement significantly reduces the probability of backscattering events. Given this interesting band structure, we'd like to explore the electronic properties more closely.

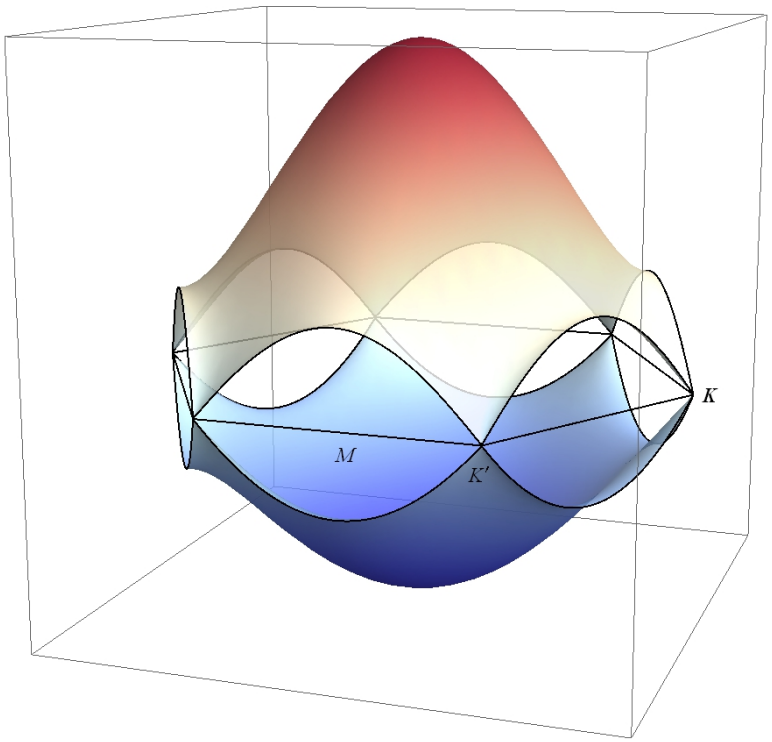

Figure 2.4: Graphene's band structure, calculated as per Reich et al. [15]. The K, K′, and M symmetry points are noted. The Γ point (at the origin) is omitted for clarity. The valence band is shown in blue and the conduction band in red.

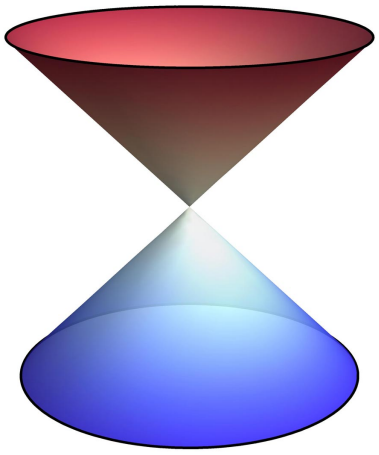

Figure 2.5: View of one of the K points of the graphene band structure. The energy of the bands are linear with the magnitude of the momentum about the K point. The slope of this cone is the Fermi velocity, which in this case is about $10^8\,\mathrm{cm/s} \approx c/300$.

2.2.1 Density of states

Around each Dirac point lies an isotropic band structure. This symmetry means that all of the occupied conduction states lie within a circle in the k_x-k_y plane with the radius equal to the Fermi wave vector. Given that the k-space volume of a single state is $(2\pi)^2/A$ (where A is the area of the sample), the total number of carriers in the material will be

$$N = 4 \cdot \frac{\pi k_F^2}{4\pi^2/A} = \frac{k_F^2 A}{\pi}, \tag{2.1}$$

where the additional factor of 4 comes from both the spin degeneracy of the graphene and the existence of two equivalent Dirac cones (i.e. the "valley" degeneracy). Thus, the Fermi wave vector k_F is only a function of the 2-D charge density n in the material, i.e.

$$k_F = \sqrt{\pi n}.$$

Using equation 2.1, we can also calculate the density of states, which is the difference in the number of occupied states between energies E and $E + dE$. We write N as a function of E_F rather than k_F

$$N = A \cdot \frac{E_F^2}{\pi \hbar^2 v_F^2},$$

where we have assumed linear dispersion around the Dirac points, $E_F = \hbar v_F k_F$. Thus, the density of states per unit sample area will be

$$D(E_F) = \frac{2\,|E_F|}{\pi \hbar^2 v_F^2} = \frac{2\sqrt{n}}{\sqrt{\pi}\,\hbar v_F}. \tag{2.2}$$

Note that this is linearly proportional to E_F and is therefore zero at the Dirac point, but is proportional to the square root of n.

2.2.2 Carrier mobility

The Drude model assumes that charge carriers in a material scatter frequently as they move through the medium [18]. This diffusive model of transport reduces the characterization of the transport to two parameters: the number of charge carriers (n) and the ease with which they move through the material (quantified as either mobility μ, mean scattering time τ, or mean free path λ).

We have seen that pseudospin can suppress backscattering, which leads to high mobilities and long mean free paths in graphene. However, the Drude model is generally still valid for graphene samples because the mean free paths are still significantly shorter than typical sample sizes. While mean free paths of up to 70 µm have been reported in nanoribbon samples [19], values around 1 µm are the highest for larger samples [20], and values of 10-50 nm are much more typical [21]. For typical graphene

FET devices larger that one micron (and in our case, often 5 to 10 microns), electrons undergo many collisions while traveling through the sample, and thus the diffusive scattering model holds.

In the Drude model, the conductivity σ is given by

$$\sigma = ne\mu \tag{2.3}$$

where n is the carrier concentration, e is the electron charge, and μ is the mobility of the charge carriers within the material. This expression holds for diffusive transport in general, but in the 2D case σ is the sheet conductivity and n is the carrier concentration per unit area.

The mobility μ is a measure of how easy it is for our carriers to move through the material. A high conductivity could be due to a few very mobile carriers, as in graphene, or due to many lower mobility carriers, as in most metals.

The physical interpretation of mobility is slightly more transparent if we recall that the current density $\vec{j}$ is given by $\vec{j} = ne\vec{v}$. Since $\vec{j} = \sigma\vec{E}$ (Ohm's law), it becomes clear that the mobility is the carrier drift velocity per unit electric field. The units of mobility reflect this: we most frequently use $\mathrm{cm}^2/\mathrm{Vs}$ as units of mobility, which can be rewritten as (cm/s)/(V/cm). The mobility scales with both the mean free path λ and the mean scattering time τ, but not necessarily linearly.

2.3 Scattering

Obtaining the form of the electronic transport is trickier and requires analysis of different scattering effects in graphene. Presently, I believe the best treatment of this is in the following review article by S. Das Sarma [21], and we will explore the most relevant parts here.

Beginning with Boltzmann transport in 2 dimensions and assuming the relaxation time approximation [18], we can derive that

$$\sigma = \frac{e^2}{2}\int d\epsilon' D(\epsilon')\vec{v}^2(\epsilon')\tau(\epsilon')\left(-\frac{\partial f(\epsilon')}{\partial\epsilon'}\right), \tag{2.4}$$

where $f(\epsilon')$ is our distribution function and τ is our scattering time. If we assume $k_BT \ll E_F$, $-\partial f/\partial\epsilon'$ becomes a Dirac delta function at the Fermi energy, making the integral trivial with $\epsilon' \to E_F$.

$$\begin{aligned}\sigma &= \frac{e^2 v_F^2}{2} D(E_F)\,\tau(E_F) \\ &= \frac{e^2}{\hbar}\frac{v_F}{\sqrt{\pi}}\sqrt{n}\,\tau(n)\end{aligned} \tag{2.5}$$

In the second line we have substituted equation 2.2 for E_F, and replaced the energy dependence with carrier concentration. The Fermi velocity is independent of the

carrier concentration (assuming we are near the Dirac point), which leaves the overall n-dependence as $\sqrt{n} \cdot \tau(n)$.

Note that the units of σ in this case are Ω^{-1} (or siemens) rather than $(\Omega{\cdot}\text{cm})^{-1}$. This is because σ is the 2-D "sheet" conductivity rather than the usual 3-D conductivity. The inverse of our 2-D conductivity is ρ, the sheet resistance, which has units of $\Omega/\square$ ("ohms per square"). In general, the conductivities and resistivities in this dissertation will be the 2-D versions unless otherwise specified.

The n-dependence of τ in equation 2.5 is not obvious, but we will begin by assuming there are two types of scatterers in graphene: those that are charged and therefore scatter carriers at long ranges, e.g. adsorbed ions or substituted dopants, and those that only scatter carriers at short range, such as lattice vacancies and other neutral defects.

2.3.1 Coulomb scattering

It can be shown that the Coulombic scatterers (i.e. those that are charged and scatter the carriers with their resulting field) have a scattering lifetime τ that is directly proportional to $\sqrt{n}$ [21, 22]. The exact relation depends on the dielectric environment of the graphene layer, but if we assume it has silicon dioxide on one side and vacuum on the other, the expression for σ simplifies to

$$\sigma_{\text{C}}(n) \approx \frac{20\, e^2}{h} \frac{n}{n_C}, \tag{2.6}$$

where n_C is the concentration of charged scatterers in or on the graphene [21]. The assumptions hold for both holes and electrons due to the symmetry of the system.

This equation gives us the well-known linear relation between conductivity and carrier concentration near the Dirac point. It is interesting to note that while this linear relation is often mentioned in the same breath as the linear dispersion relation of graphene, there is no fundamental connection between the "linearity" of the two. Rather, one factor of $\sqrt{n}$ comes from the band structure and the other from the Coulombic scattering, which dominates at lower carrier concentrations.

2.3.2 Short-range scattering

For purely short-range scatterers, calculations show that τ is inversely proportional to $\sqrt{n}$ and that the conductivity is given by

$$\sigma_{\text{SRS}} \approx \frac{4e^2\hbar\, v_F^2}{\pi n_s V_0^2}, \tag{2.7}$$

where n_s is the density of short-range scatterers and V_0 is the strength of the scattering potential with units of energy $\times$ area [21].

Note that this type of scattering is independent of carrier concentration.

2.4 DC transport

2.4.1 Scattering signatures

In practice, both types of scattering are present in graphene devices. Assuming that the presence of one type of scattering does not affect the other, we can use Matthiessen's rule and simply add the individual scattering rates, combining the effects into a single expression [18]. The scattering rates for each process are inversely proportional to their respective scattering lifetimes, giving us an expression for the overall scattering,

$$\frac{1}{\tau^*} = \frac{1}{\tau_1} + \frac{1}{\tau_2} + \cdots , \tag{2.8}$$

where τ^* is the effective scattering lifetime, and τ_i is the lifetime accounting only for scattering from process i.

If we combine just the Coulombic (eq 2.6) and short range (eq 2.7) scattering effects, we obtain an expression for total conductivity of the form

$$\sigma(n) = \left(\frac{1}{\sigma_{\mathrm{C}}(n)} + \frac{1}{\sigma_{\mathrm{SRS}}}\right)^{-1} = \left(\alpha\frac{n_C}{n} + \rho_{\mathrm{SRS}}(n_s)\right)^{-1} \tag{2.9}$$

where α is a proportionality constant and $\rho_{\mathrm{SRS}} = 1/\sigma_{\mathrm{SRS}}$, the resistivity from short range scattering alone. Our expression has dependence on n as well as the scatterer densities n_C and n_s.

This expression is plotted in figure 2.6 with three illustrative n_C values (10^{11}, 10^{12}, $10^{13}/\mathrm{cm}^2$), each in a different color.

While graphene is often said to have a linear σ-n (or σ-V_g) relationship, in reality it is frequently *sub*linear due to the presence of short range scatterers. This is illustrated in figure 2.6, where each colored pair of curves has the same charged scatterer density n_C but has $n_s = 0$ (dashed) or $n_s = 10^{11}$ (solid). The $n_s = 0$ curves are linear, but the presence of short range scatterers causes their slopes to decrease away from $n = 0$. These range from a drastic drop in the slope, when $n_s \approx n_C$, to an almost-undetectable difference when $n_s \ll n_C$.

2.4.2 Temperature dependence of scattering

Neither Coulombic scattering nor short range scattering are strongly affected by temperature [23, 24]. As long as $E_F \gg k_B T$, the electron distribution function is independent of temperature. Therefore, the strongest temperature dependence should be from phonon scattering because the phonon occupancy is itself strongly temperature dependent.

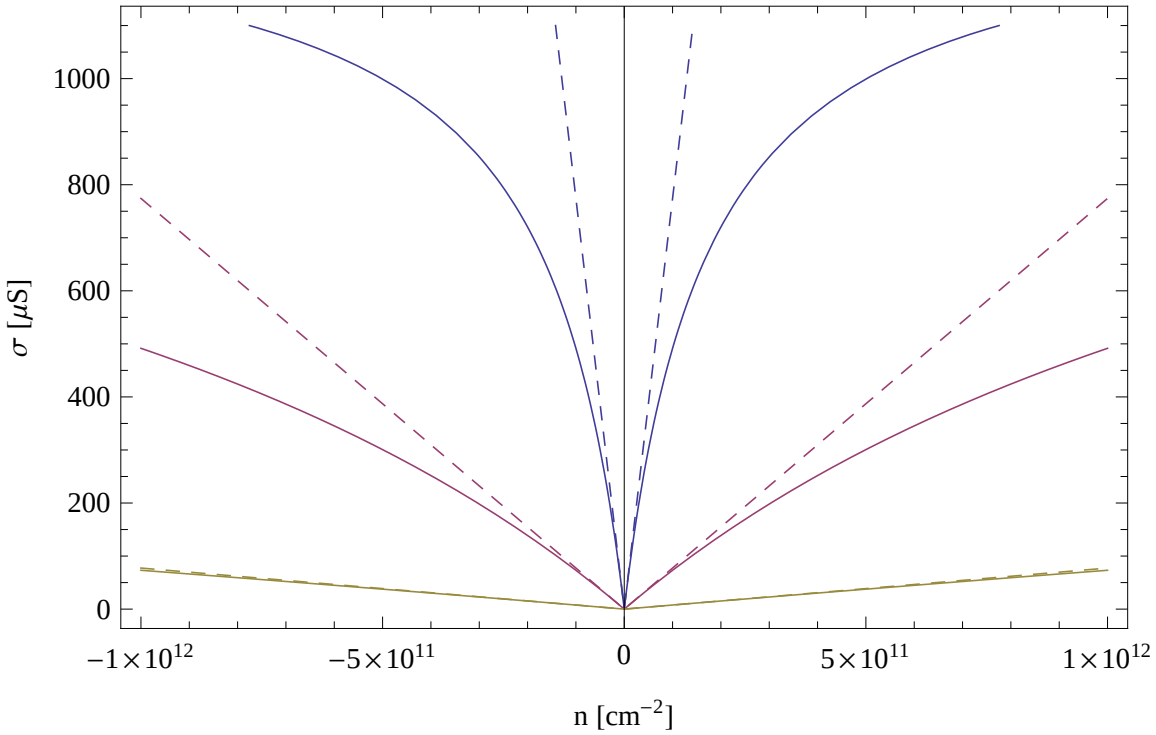

Figure 2.6: Calculated conductivity vs carrier density of monolayer graphene with varying scatterer densities (cm^{-2}): $n_i = 10^{11}$ (blue), 10^{12} (purple), 10^{13} (yellow), $n_D = 0$ (dashed), 10^{11} (solid). The resulting carrier mobilities (based on slope at low carrier density) are 50,000 cm^2/Vs, 5,000 cm^2/Vs, and 500 cm^2/Vs for blue, purple, and yellow, respectively. The range of carrier densities corresponds to a gate voltage range of about ±14 V (assuming the sample is gated through 300 nm of SiO_2).

2.5 Extracting parameters from transport data

For a graphene field effect transistor (GFET) made on an oxidized wafer of degenerately doped silicon, our independent controls are the source/drain current (or voltage) through the electrodes and the back gate voltage, which changes the potential of the silicon back plane. This conductive plane is one half a parallel plate capacitor, with graphene as the other half and the silicon dioxide dielectric in between.

By changing the voltage on this capacitor, we can change the charge density in the graphene in a predictable fashion. For 300 nm of silicon dioxide (a typical value), the specific capacitance is 115 $aF/\mu m^2$. This capacitance is equivalent to 7.2×10^{10} carriers/cm^2/V, which means for every volt applied to the gate, the density of charge carriers changes by $7.2\times10^{10}/cm^2$.

In practice, due to its external environment, the graphene is generally doped, meaning that when 0 V is applied to the gate there are still a significant number of charge carriers in the graphene. This can arise from localized charged impurities

such as metal atoms [23] or from other more diffuse species, including the substrate itself [25]. To get the graphene to its minimum conductivity (i.e. lowest number of carriers), these carriers must be removed by the electrostatic gate. For this reason, the conductivity minimum is often found at a gate voltage far from 0 V.

In this way, the carrier concentration at 0 V can be found by varying the gate voltage until the conductivity minimum is found.

For example, if the voltage needed to obtain the conductivity minimum is positive, that means negative net charge has been added to the gate to obtain an average n of 0, and thus the graphene was p-type when ungated at 0 V.

When the carrier concentration in graphene is tuned with an electrostatic gate, the Fermi energy moves as well, going above the Dirac point in the band structure when the graphene is electron doped and below when it is hole doped. When graphene is at its lowest value of n, the conductivity minimum, the Fermi energy lies at the Dirac point. For this reason, the voltage at which this conductivity minimum occurs is called the charge neutrality point voltage (since $n_e - n_h$ should equal zero) or the Dirac point voltage (since E_F lies, on average, at the Dirac point).

Our model thus far (figure 2.6) looks reasonably like data one obtains from an actual graphene device with one major difference: the conductivity minima we measure are far from zero, usually hundreds of µS. The model's conductivity of zero relies on the removal of all charge carriers from the entire sheet of graphene. This is, of course, impossible, as variations in gating and extrinsic dopants will create inhomogeneities that can not be removed.

We can attempt to account for this variation in our model by treating our graphene sheet as many strips of graphene in parallel, each with a different charge neutrality voltage. Given a distribution of charge neutrality voltages we can model the bulk response by averaging shifted and appropriately weighted conductivity curves from our single-doping model. Mathematically, this is equivalent to convolving our single-doping curve with the distribution function.

Figure 2.7 shows several such gated conductivity curves, each using a normal distribution of varying widths. A more rigorous model would have differently doped graphene in series as well, forming a continuous 2D network of randomly doped graphene. However, the broadening effect shown by this simple model would persist.

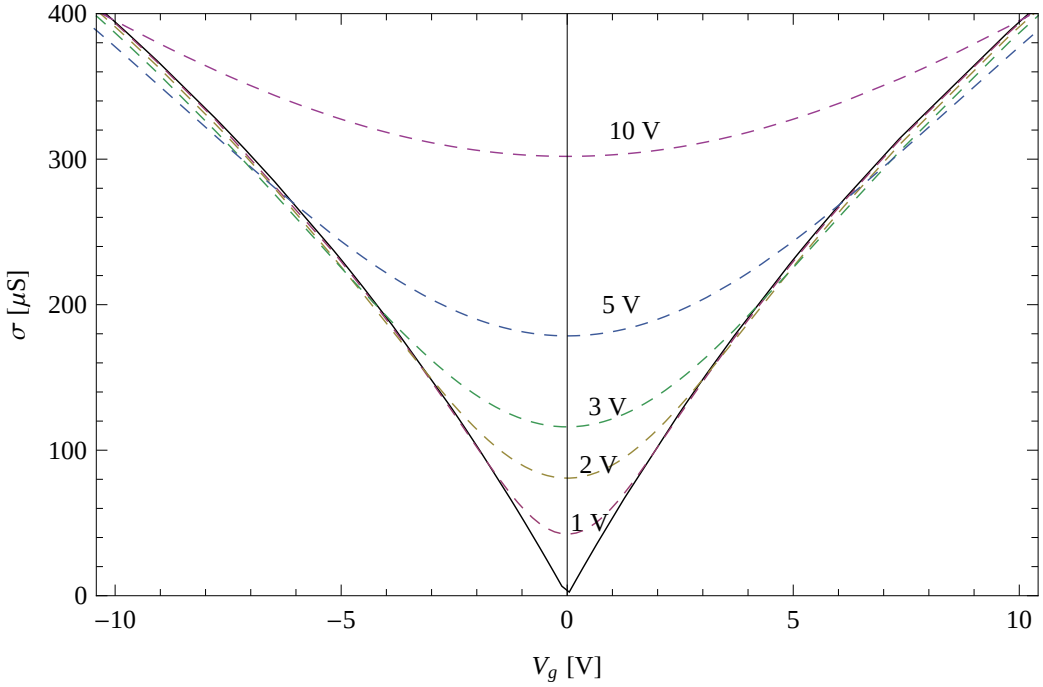

Figure 2.7: Simulations of variation in graphene doping. These were made by convolving the black curve ($n_C = 10^{12}/\text{cm}^2$, $n_s = 10^{11}/\text{cm}^2$, $n(V_g = 0) = 0$) with a Gaussian distribution. The Gaussian widths used are noted on the curves.

Chapter 3

Graphene synthesis

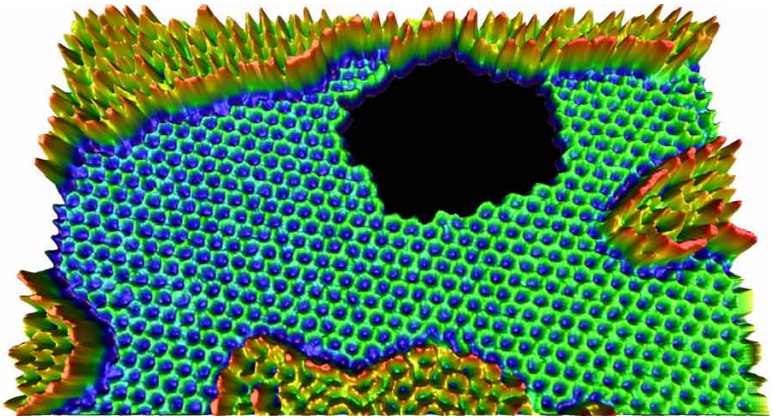

Figure 3.1: Image of monolayer graphene with a hole, taken by the Transmission Electron Aberration-corrected Microscope (TEAM) at NCEM, from Girit et al. [26].

The previous chapter explained some of the interesting properties of graphene, but how can this unique material be isolated and measured? The work in this chapter was done in close collaboration with Will Regan, a fellow graduate student in the Zettl group.

3.1 Exfoliation of graphite

The most well known way of producing graphene monolayers is the exfoliation of graphite which, as mentioned previously, was first reported by Geim and Novoselov [8, 9]. A more complete review the process of graphite exfoliation can be found in the dissertation of Çağlar Girit, a former graduate student in the Zettl group [27]. The standard exfoliation recipe Will Regan and I used follows. We used similar recipes for exfoliation of boron nitride, gallium selenide, and other semiconductors with layered crystal structures.

To begin, we cleaned silicon substrates with 300 nm of thermally grown oxide using piranha solution.[1] We rinsed the substrates several times with deionized water and blew them dry with nitrogen. We then placed them on a hot plate between 60°C and 100°C to further remove water.

We then cut a ∼15 cm piece of tape (3M Scotch Premium Transparent Film Tape 600, as recommended by [27]) and dropped a few graphite flakes on the adhesive side. We then pushed the two halves of the tape into contact and pulled them apart, repeating between 10 and 20 times until the graphite looked like it had covered most of the middle few centimeters of the tape.

We removed the silicon substrates from the hot plate at this time and let them cool slightly. The goal here was to minimize the amount of water adsorbed on the SiO_2, which occurs at lower temperatures, and to minimize the amount of adhesive residue that sticks to the substrate, which seems to increase at higher temperatures. A temperature of "warm but not hot to the touch" was usually the goal, most likely 40-50°C.

The tape and exfoliated graphite were then pushed down onto the substrates quickly and rubbed with a finger or rubber eraser until they had mostly cooled (∼30 seconds). To minimize the amount of tape residue, we let the samples sit at least overnight, and ideally longer. This exact mechanism was unknown, but we suspected it had to do with the adhesive layer relaxing and re-adhering to the backing layer of the tape.

Removing tape residue after exfoliation proved difficult, as the 3M 600 adhesive did not seem soluble in common lab solvents. This is why we paid so much attention to minimizing the tape residue during the exfoliation process.

When the tape was ready to be peeled, we held a flat edge (such a the dull side of a single-edged razor blade) against the tape and, pulling up one end of the tape, kept the straight edge at the point of delamination as the tape peeled from the substrate. This ensured even pressure across the tape.

After peeling, the sample was ready to be examined in the optical microscope to identify thin regions. See appendix A for an explanation and simulation of the optical contrast of graphene on oxide. This graphene exfoliation technique is more or less identical to our boron nitride exfoliation used later in this dissertation.

Figure 3.2 shows an example of an exfoliated bilayer graphene region. This sample shows several 30° and 150° angles, indicating a probable mix of zigzag and armchair edges.

[1] A piranha solution is a standard cleaning process for semiconductor fabrication. It consists of approximately 3:1 concentrated sulfuric acid to 30% H_2O_2. Extreme caution should be taken when mixing or using piranha solution, and proper training is absolutely required. Consult SOPs or experinced lab members, and always use the proper protective equipment!

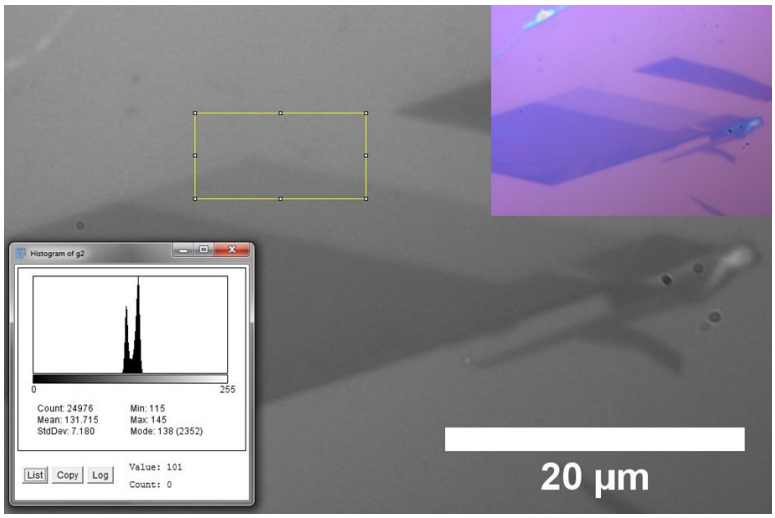

Figure 3.2: Optical image of exfoliated graphene. Inset top right is RGB image, main monochromatic image is the green channel. Inset lower left is a histogram of the green pixel intensities in the denoted region, showing that the region is most likely bilayer graphene (Courtesy Will Regan).

3.2 CVD graphene growth

By 2009, several different groups had demonstrated growth of multilayer graphene by chemical vapor deposition (CVD) [28–30], but consistent growth of monolayers remained out of reach. Work by Prof. Rodney Ruoff's group at the University of Texas at Austin showed that low pressure CVD (LPCVD) on copper foils produced nearly entirely monolayer graphene [31].

It was not difficult for us to reproduce this growth in a very short amount of time, since the Zettl group already had an operating LPCVD system for nanotube growth. Improvements to this growth recipe over time were largely made by Will Regan. This included splitting the growth into two stages: an initial low-flow growth stage to minimize nucleation and increase grain size, and a second higher-flow growth to fill the gaps between the larger grains. This was inspired by later results from the Ruoff group [32].

3.2.1 Foil growth recipe

A typical two-stage growth recipe for the Zettl group graphene CVD system follows. A schematic of this growth recipe appears in figure 3.3.

Twenty-five micron thick copper foil (from Alfa Aesar, #13382) was cut into ∼2 cm squares and placed in a quartz CVD tube in a Lindberg Blue M tube furnace. The tube was connected with KF flanges to the rest of the gas flow and vacuum system. A rough pump was used to pump on the CVD system, which typically had

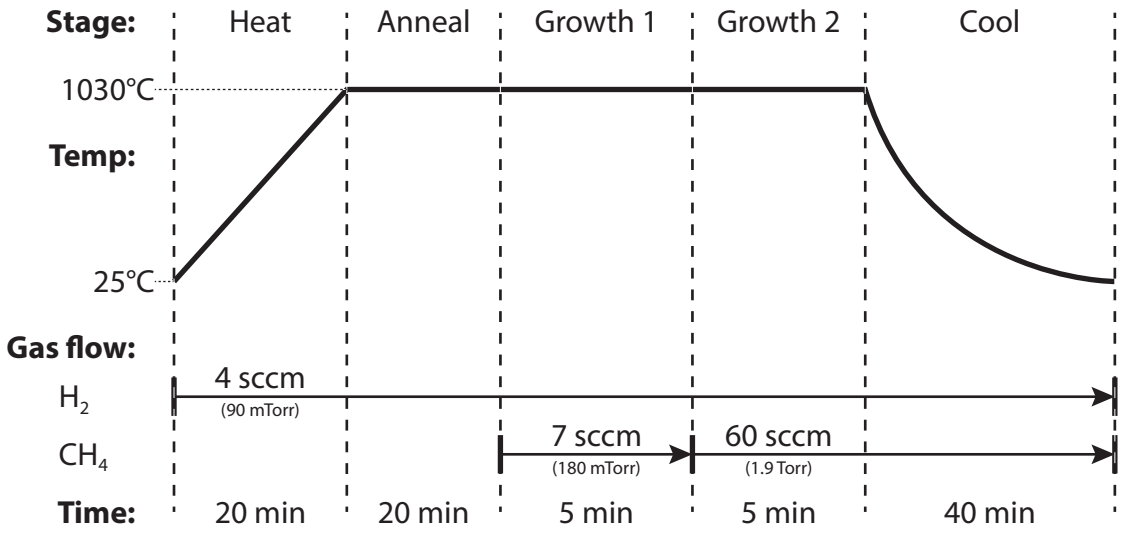

Figure 3.3: Diagram showing two-stage growth recipe for CVD graphene grown on copper foil.

a base pressure of 10 mTorr.

The first phase of the recipe was an anneal. We flowed ∼4 sccm H_2 (partial pressure 90 mTorr) and ramped the furnace temperature up to ∼1030°C. This temperature and flow was maintained for 20-30 minutes to remove contaminants, oxide, and water from the copper foil and tube.

At this time, we began the flow of methane at 7 sccm in addition to the continuing hydrogen. We maintained this temperature and flow for about five minutes, after which we increased the methane flow to 60 sccm. This was maintained for five more minutes.

At the end of this growth phase, the tube furnace was shut off and opened to cool the sample more quickly. Gas flow was maintained during this time to prevent oxidation at high temperatures.

After cooling, the sample was ready for use. For us, this always meant transferring the graphene to an insulating substrate, since transport measurements can not be performed while the graphene is on copper foil.

3.2.2 Post-growth transfer

After the monolayer graphene was grown on copper, it needed to be removed and transferred carefully so it would be clean and intact on the target substrate. Our technique for this transfer has evolved over time, and our final recipe follows below.

Once the graphene-coated copper was removed from the tube, it was coated on one side with a layer of poly(methyl methacrylate) (PMMA) by spin coating. This

layer acted both as a protective layer and as mechanical support for the graphene.

Etching

Recall that in the CVD tube, very little differentiated the top and bottom surfaces of the copper foil, and thus graphene grew on both. If the bottom layer was left until the copper etching, problems arose in the form of trapped gas bubbles and/or bilayer adhesion. Removal of this layer alleviated these problems.

The copper foil was placed PMMA-side-down in the reactive ion etcher and etched for 10-20 seconds at 50 W with 50 sccm O_2. This removed the bottom layer of graphene. The PMMA and underlying graphene remained due to the low power and short time of the oxygen etch.

The next step was copper etching. The copper foil was floated PMMA-side-up onto a bath of copper etchant. Sometimes it sank at this step due to wetting of the surface, but it could often be salvaged if it was retrieved and placed on the surface again. The etchant dissolved the copper foil after 30-60 minutes, depending on temperature and etchant concentration, leaving the PMMA film and a single graphene monolayer floating on the surface.

The initial etchant we used was an aqueous iron chloride ($FeCl_3$) solution. However, TEM studies showed contamination containing iron on graphene after etching, which we believed could only have come from the etchant [33].

Based on this, we changed to an aqueous sodium persulfate solution ($Na_2S_2O_8$, $\sim$0.1 g/mL) which seemed to contribute less contamination to the graphene. We have also experimented with ammonium persulfate ($(NH_4)_2S_2O_8$) and seen similarly low contamination.

Unfortunately the sodium persulfate came with its own problems. It generated far more bubbles in the solution while etching, some of which stuck to the graphene or PMMA film during transfer, creating adhesion problems. Additionally, there is evidence that the persulfate ion can cause crosslinking of the PMMA, making it more difficult to remove from the graphene [34].[2]

Transfer

The PMMA and graphene now needed to be rinsed and put on the target substrate. We transferred the PMMA film to at least two clean deionized water (DI) baths.

The details of the transfers are important, as excessive bending of the PMMA may damage the graphene and prevent subsequent adhesion to the substrate. We frequently used a Teflon-coated spoon to pick up the film and lower it back onto the DI bath. However, the hydrophobicity of the Teflon made the drop of etchant under the PMMA have a high curvature.

[2]This was first brought to my attention by Nick Petrone from James Hone's group at Columbia.

Other transfer tools included a piece of silicon wafer, a custom-made quartz spoon, and a plastic spoon from a campus café. These were chosen for their varying hydrophobic or hydrophilic surfaces, but it never seemed that one was consistently better than others. Minimizing regions of high curvature and rinsing the sample well seemed to be more important.

After it had been rinsed several times in DI water, the PMMA film is finally lifted off of the surface by the target substrate, most commonly 300 nm of SiO_2 on silicon cleaned with a piranha solution. At this point, there was a thick layer of water between the graphene and the substrate.

We experimented with different recipes for removing this layer of water. Twelve hours on a warm (60°C) hot plate seemed to work well, although at times we used vacuum oven treatments with good results.

Reflow

Before removing the PMMA, we found it beneficial to heat the sample up significantly to soften and reflow the PMMA film. This process is illustrated in figure 3.4. The PMMA is initially spun down on a rough copper surface, which typically exhibits deep striations, presumably from the rollers that make the foil. The surface roughness of the copper becomes the surface roughness of the graphene and PMMA once the copper is etched away, as seen in figure 3.4a and b. This means that upon transfer, it was possible that very little of the graphene was actually in contact with the substrate, as in figure 3.4c. By heating it up, the rough surface softened and relaxed into better contact with the target substrate, as shown in figure 3.4d.

We found this technique especially helpful for uneven substrates, such as boron nitride flakes or patterned SiO_2 on silicon. A typical reflow recipe was about 20 minutes on a hot plate at 185°C. Around the time we discovered this technique, similar results were published by the Ruoff group [35].

I feel that there is still room for improvement in these transfer techniques. One possible route is the use of semi-rigid frames on the PMMA that are not etched. This was demonstrated by Prof. James Hone's group at Columbia University. They used a frame of Kapton tape around the PMMA/graphene film to maintain its shape during the transfers and claimed positive results, but this has not presently been attempted in the Zettl group [36].

Relatively little work has been done on treatment of copper foils before CVD growth. I believe this is an area that would be easy to explore. The foils typically have striations on them several microns wide and deep, presumably from the foil rolling process, as shown schematically in figure 3.4. Mechanical polishing or electropolishing of the foil to flatten the surface could improve transfer and potentially reduce the number of locations to trap contaminants.

We also observed that the integrity of the graphene layer seemed to depend on the growth recipe. Graphene grown with only a low flow rate often resulted in very

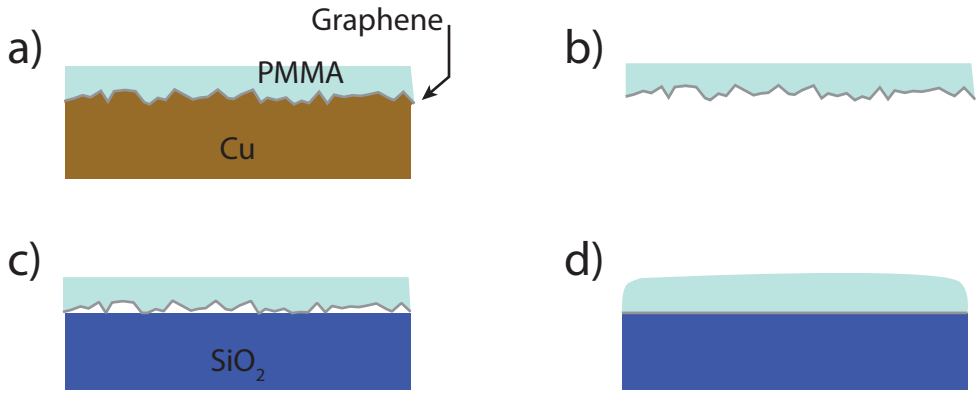

Figure 3.4: Illustration of PMMA reflow effect on transfer process. (a) Graphene grown on naturally rough copper foil is coated with PMMA. (b) The copper is dissolved, leaving the PMMA and graphene with a rough profile. (c) The graphene/PMMA film is transferred to a SiO_2 substrate, but makes very poor contact. If the PMMA were removed now, very little graphene would stick. (d) After heating, the PMMA relaxes its shape, allowing the graphene to make much better contact with the substrate. The sample is now ready to have the PMMA removed.

poor transfer. The same growth recipe with a second higher-flow growth step was much more intact after transfer. We attributed this to amorphous or polycrystalline regions between the larger grains that add to the strength of the sheet. Without these regions, gaps between the large grains caused the sheets to fall apart.

3.3 CVD growth on thin films

We were inspired to pursue growth of graphene on copper thin films for a number of reasons. First, if graphene is grown on copper on a dielectric surface, the copper dewets, forming islands and transferring the graphene to the dielectric [37]. This potentially allowed very clean fabrication of devices, since no PMMA was required as a transfer step. Second, it was possible that it could lead to scalable growth of suspended graphene devices. A schematic of such a fabrication route is shown in figure 3.6.

Performing CVD growth on thin films proved difficult. Thin films of copper, with and without sticking layers, deposited on silicon or SiO_2 showed severe damage after graphene growth in nearly all cases. We suspected this was due to alloying effects, or possibly carbothermal decomposition. Thin films of copper on sapphire wafers did not exhibit alloying but often dewetted from the surface at high temperatures, consistent with work done by Ismach et al. [37].

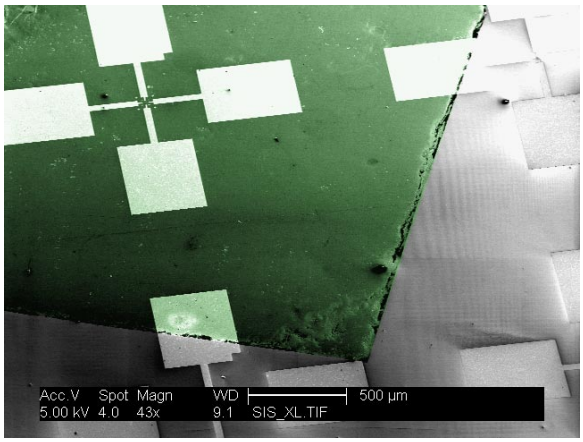

Figure 3.5: SEM image showing CVD graphene transferred onto contacts. The graphene-covered region is highlighted in green.

Fabrication of suspended devices as shown in figure 3.6 proved very difficult. After etching, if the devices were simply dried, the graphene bridges were destroyed. Critical point drying (CPD) in the Zettl group's Tousimis system did not produce a different result; no suspended graphene remained. One such collapsed structure appears in figure 3.7. The graphene is not visible, but the etched shape of the copper remains. The copper in the center shows that the device was underetched.

We were able to fabricate suspended structures if the PMMA mask was left in place after the copper etching, but contact with PMMA would likely adversely affect transport through the graphene structure. Preliminary transport measurements were performed, but gating the samples was impossible due to the insulating substrates. Measurements of the Hall effect or of van der Pauw structures were not performed.

3.4 Thin film copper on BN flakes

As will be explained in chapter 4, we spent considerable time trying to fabricate graphene devices on hexagonal boron nitride (hBN) substrates in order to increase the carrier mobility. Our attempts to grow graphene with CVD directly on hBN failed, usually forming either amorphous carbon films or nothing.

We had better results exfoliating hBN flakes onto either SiO_2 or sapphire substrates, evaporating thin copper films onto them, and then performing CVD growth. This was partially inspired by the results from Ismach et al. [37], which showed that dewetting of the copper could result in graphene films directly on the dielectric substrate.

Our recipe was as follows. We exfoliated hBN flakes onto both 300 nm SiO_2 on Si and c-cut sapphire substrates. We then thermally evaporated 300 nm of copper onto all substrates. Graphene was then grown on the samples with a two-stage growth

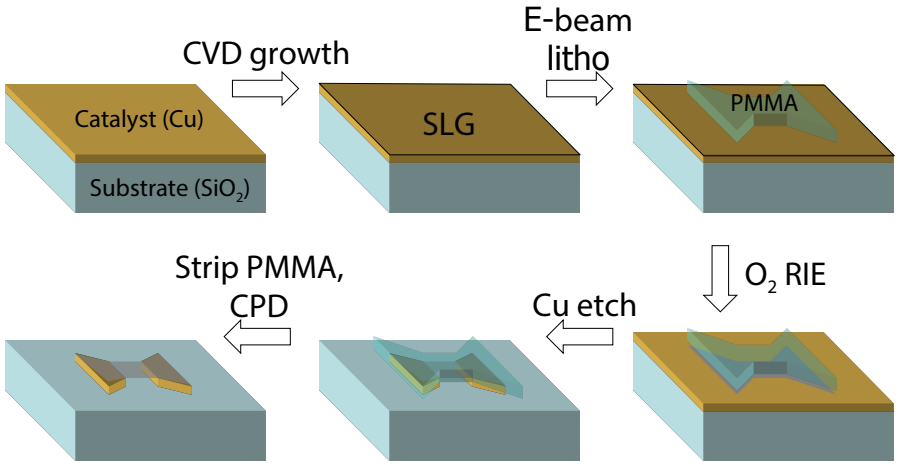

Figure 3.6: Schematic of thin film grown graphene device fabrication steps. A thin film of copper catalyst is deposited on an insulating substrate. Single layer graphene (SLG) is then grown on the copper with CVD techniques. A PMMA mask is then made with e-beam lithography, a "bowtie" shape is shown here. Oxygen etching removes all graphene not under the mask, and a copper etch removes all unprotected copper and underetches the center region of the mask. The PMMA is then stripped and the sample is dried, leaving a suspended area of graphene in the center.

recipe much like that in figure 3.3, but at a lower temperature (980°C) to reduce dewetting at this stage. After growth was complete, the temperature was raised to ∼1000°C to increase the rate of dewetting.

The resulting samples had many graphene patches of varying sizes on hBN flakes with no copper present. One such small patch appears in figure 3.9.

These patches also covered much larger areas on some samples. Figure 3.10 shows a hBN flake with higher coverage of graphene, and some regions several microns across. From this and other images, it appeared that the copper dewetting occurs first at the edges of BN flakes, possibly due to the high surface curvature at those locations. The copper crawls away from those edges into lower surface area (i.e. rounded) structures that tend to be either on or off of the hBN flakes rather than spanning the edges. The graphene that was initially even over the surface of the copper film somehow becomes pinned to the substrate and remains there as the copper recedes.

We did not attempt to make transport measurements on the resulting graphene devices due to both the small size of the graphene patches and the potential for shorting of devices by the remaining copper. This synthesis technique remains of interest, however, since copper can be removed by etchants and the small size is still within the capability of our lithography system.

We experimented very little with transferring graphene grown on thin copper films, since it presented few advantages over foil growth. One possible advantage, however,

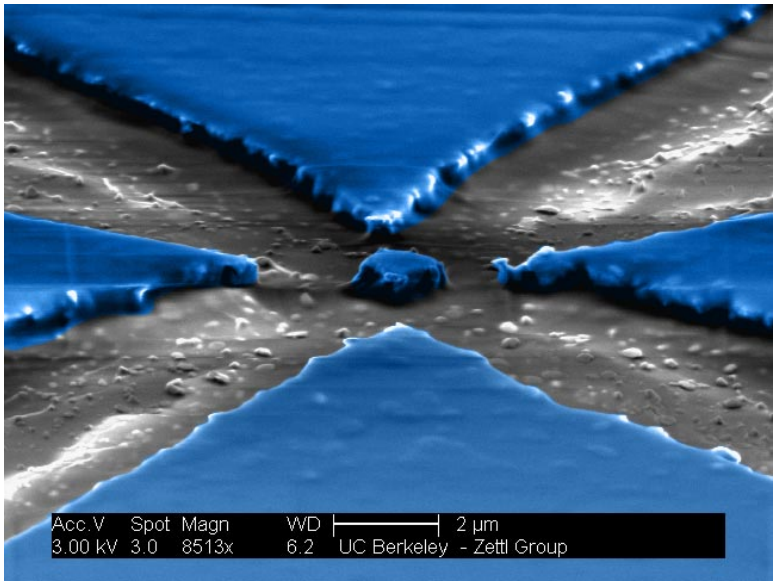

Figure 3.7: False color SEM image (at ∼45° tilt) of collapsed CVD graphene on copper thin film and sapphire. The unetched copper catalyst/contacts are colored blue, and the sapphire remains gray. From batch "GTC-D".

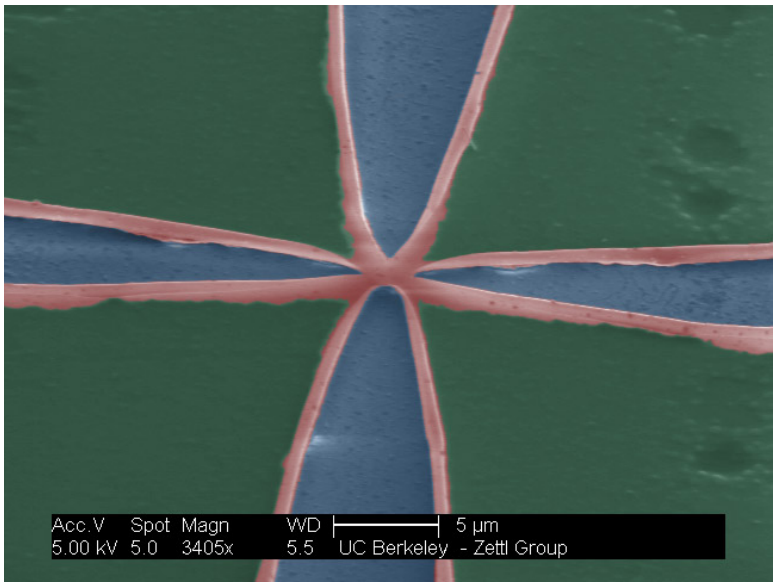

Figure 3.8: False color SEM image (at ∼45° tilt) of a graphene/PMMA bilayer with a van der Pauw geometry suspended on a sapphire wafer. The copper catalyst/contacts are colored green, bare sapphire is blue, and suspended graphene/PMMA is red. From batch "GTC-F".

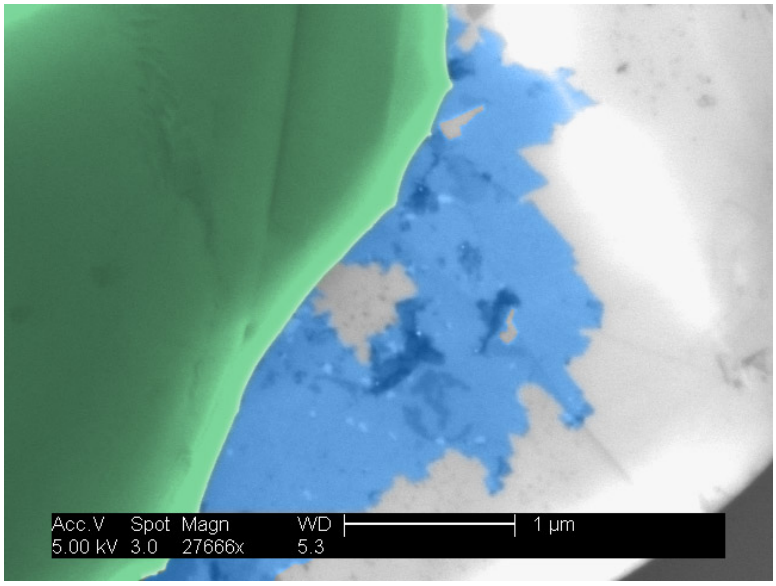

Figure 3.9: False color SEM image of CVD graphene grown on thin film copper on hBN flakes. The copper catalyst is green and the graphene (on hBN) is blue. The underlying sapphire substrate is only visible in the lower right corner.

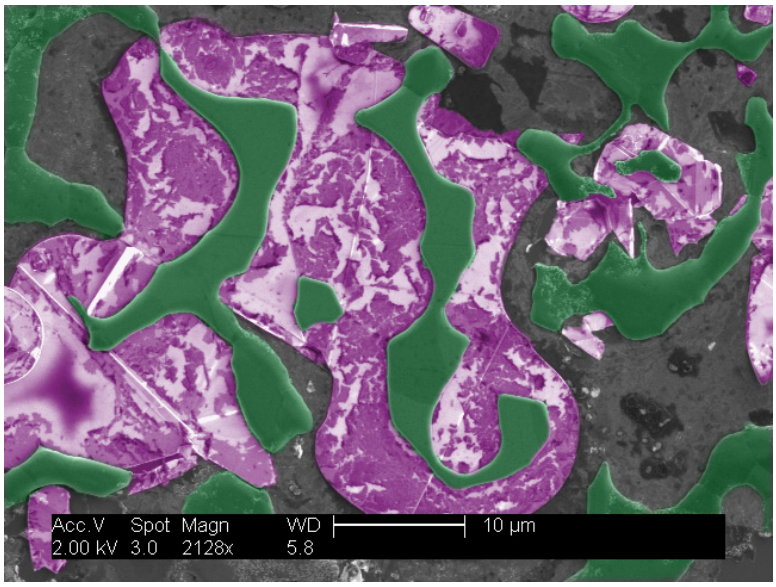

Figure 3.10: False color SEM image of CVD graphene grown on thin film copper on hBN flakes. The copper catalyst is green and the hBN flakes are purple. The darker patches on the flakes are mono- or multilayer graphene, and the bright areas are bare hBN.

is that resulting graphene could be much more planar than that from the foil, which could allow easier transfer to planar substrates and potentially even transfer without a sacrificial PMMA layer.

Our attempts to do so consisted of CVD growth on thin film copper followed by copper etching while the graphene/copper was being pushed into contact with a target substrate (typically oxidized silicon). We were unable to achieve any transfer in this fashion, but further research may produce successful transfers.

3.5 Other graphene production techniques

Many researchers have invested time and resources into several other graphene production techniques. The most notable is epitaxial growth on silicon carbide (SiC), wherein a SiC wafer is heated until the silicon atoms begin to sublimate from the surface. The remaining carbon atoms rearrange themselves into a graphene lattice on the surface. This technique has the advantage of being completely in situ, unlike tape exfoliation or CVD growth followed by transfer. This allows measurements to be made on very clean graphene, since the only extrinsic effects will be from the substrate [38, 39].

Chemical exfoliation of graphite to produce graphene in solution through various routes has also been attempted, but the quality of resulting products tends to be low, and deposition of monolayers can be challenging [11, 40]. The same holds true for reducing graphene oxide [41]. Both techniques do have the advantage of extreme scalability and thus may be useful for certain applications that don't require high mobility monolayers, such as sensors or composite materials.

Chapter 4

Graphene on boron nitride

4.1 Motivation for substrate improvements

Many of graphene's unique phenomena rely on its high mobility which, as mentioned previously, is due to its unique pseudospin properties of the band structure which suppress backscattering in the material. This effect has led to several phenomena of great interest, such as ballistic transport and quantum Hall effects at temperatures up to 300 K [14, 42–44].

Before the discovery of reliable CVD growth techniques for monolayer graphene [31, 45], graphene device fabrication represented a much larger investment of time and resources, as researchers had to hunt for individual graphene monolayers in an optical microscope [8, 9]. While it is possible to see monolayers, identifying them on a wafer among many thicker (and more visible) graphene flakes is very difficult.[1]

The discovery and subsequent development of CVD growth techniques on copper were inarguably a huge step forward for graphene device fabrication [31, 32, 45, 46]. With these relatively simple steps for growth and transfer, thousands or more graphene devices could easily be fabricated on a chip without any individually aligned lithography steps, eliminating the need for luck during exfoliation and the difficulty of hunting for monolayers with an optical microscope.

However, the carrier mobility of CVD graphene remained much poorer than exfoliated graphene. In the first year after its development, graphene grown on copper was still limited to mobilities of around 4000 cm^2/Vs [47], save for a single report of higher mobilities, with one sample reportedly 16,000 cm^2/Vs [32]. Devices made from exfoliation had mobilities of 10,000 cm^2/Vs from the beginning [8] and rose to over 200,000 cm^2/Vs within a few years [20, 42]. Improving the mobility in CVD graphene was a very high priority, but it remained unclear if the scattering was intrinsic to the graphene as-grown (from defects or grain boundaries) or if there were other factors

[1] The true cost of these devices including the effects of eye strain has, to my knowledge, not been calculated.

such as contamination or substrate affecting the transport. The source of scattering needed to be identified before making a focused effort to improve mobilities.

Motivated by results from the Crommie group that showed charge puddles in clean graphene devices on SiO_2 [48], we decided that the best way to explore these scattering processes would be to use a different substrate. An ideal substrate would be very flat to allow the graphene to be equally flat, chemically and electronically inert to avoid reacting with or doping the graphene, and insulating to allow electronic measurements to be made only through the graphene.

4.1.1 Boron nitride

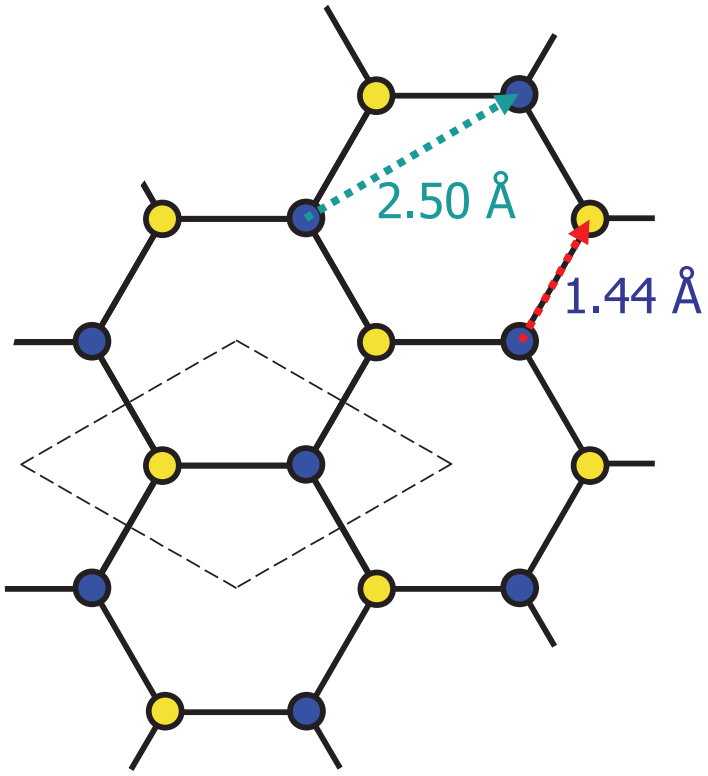

Figure 4.1: Schematic of boron nitride lattice, with boron and nitrogen atoms yellow and blue, respectively. One unit cell is outlined with a dashed line. Lengths from [49].

Hexagonal boron nitride (or hBN) is, in many ways, an ideal substrate for graphene devices. It is insulating, with a 5.97 eV direct bandgap [50] and a dielectric constant compatible with back-gating (ϵ = 3-4 according to [51, 52]). It is chemically very inert, and its strong in-plane bonds mean that it should perturb the graphene very

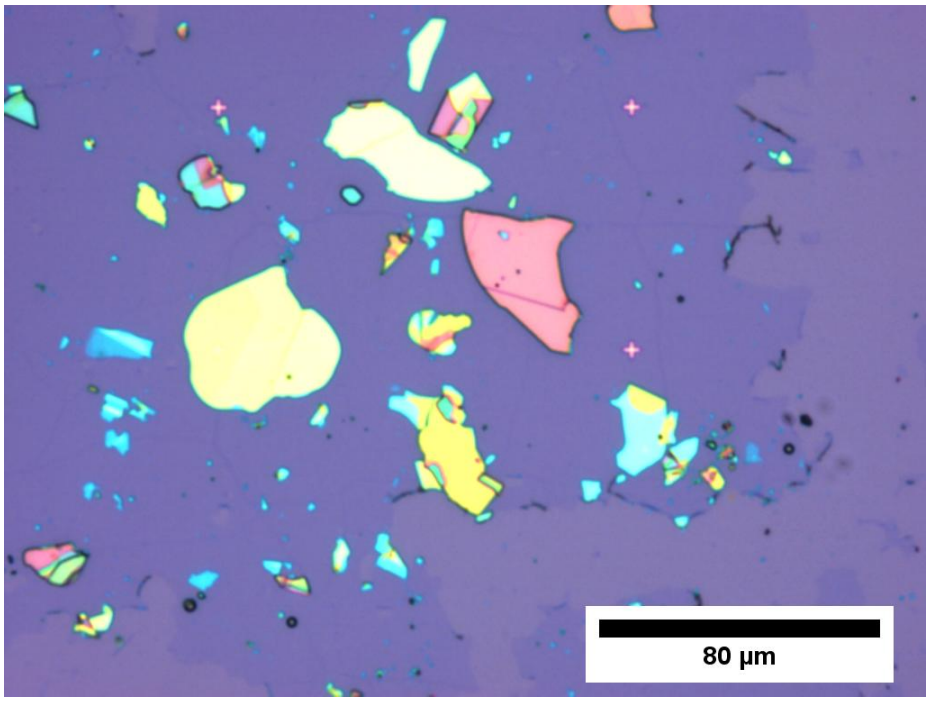

Figure 4.2: Optical image of hBN flakes exfoliated on 300 nm SiO_2. Graphene has been transferred on top of this sample, but this only slightly changed the appearance of the hBN flakes.)

little. Because of its planar crystal structure, hBN can be exfoliated onto substrates in the same manner as graphite, resulting in extremely flat, contamination-free planes. In this way, a hBN substrate would introduce much less disorder than typical SiO_2 substrates. The Zettl group had used hexagonal boron nitride in the past, including two microscopy studies of thin boron nitride layers [53, 54].

In addition to providing an inert clean surface, the crystal structure of hBN is also predicted to have a potentially interesting effect: because the lattice constants of graphene and hBN differ by only $\sim$1.8% [55], a stacked BN/graphene interface can have extended regions where each carbon sublattice is adjacent to only boron (or nitrogen) atoms. This can break the sublattice symmetry, which is theoretically predicted to open a bandgap in the graphene [56]. Such a bandgap would be extremely useful in improving the performence of graphene field effect transistors (FETs).

Unfortunately, any relative rotation between the crystals means the two sublattices are no longer on top of one another, which reduces this symmetry breaking effect. Furthermore, while 1.8% seems small, in practical terms it means that every 28 lattice spacings the sublattices are 180° out of phase. This eliminates the possibility of long-range graphene-BN stacking without the introduction of significant strain. While this potential for opening a gap is of great interest, fabricating BN-graphene interfaces that are rotationally aligned is no easy task.

Very recently, scanning tunneling microscopy was performed on graphene-on-BN structures that had a rotational mismatch. Such a mismatch led to a Moiré pattern visible in the microscope, which in turn acted as a periodic perturbation on the graphene, changing its band structure near the Dirac point [55]. This is presently the closest researchers have come to BN/graphene symmetry breaking.

While we were working on this project, results were published by Prof. James Hone's group at Columbia University measuring exfoliated graphene on BN [51]. Promisingly, they measured lower substrate doping and higher mobilities. However, CVD graphene on BN remained entirely unexplored, which allowed us the opportunity to be the first to examine this combination of materials.

Some of the work shown in this chapter was subsequently published in Applied Physics Letters [57].

4.2 Device fabrication

4.2.1 Fabricating graphene/hBN heterostructures

We began by preparing substrates consisting of 300 nm silicon dioxide on degenerately doped silicon (SQI arsenic doped, n-type, 1-5 mΩ cm) by fabricating a large array of Cr/Au alignment marks with electron-beam lithography and cleaning them with a piranha solution. The piranha improves adhesion between the hBN (or graphene) and the SiO_2, presumably by making the surface more hydrophilic.

We then used Scotch tape (Transparent film tape #600 from 3M) to exfoliate boron nitride flakes obtained from Dr. Takashi Taniguchi and Dr. Kenji Watanabe, researchers at NIMS in Japan who grew hBN from a high pressure solution of boron and nitrogen in barium [50]. Exfoliated graphene on an oxidized silicon substrate can be seen in figure 4.2.

To remove residual tape residue, we calcined the substrates in an open-ended quartz tube in a CVD furnace at 450°C for 2 hours. The tape residue and other contaminants burned off of the samples but the boron nitride was unaffected, as was confirmed by optical microscopy.

We grew graphene on 25 µm copper foil (Alfa Aesar #13382) using a two stage LPCVD growth process. We began by flowing 4 sccm H_2 over the copper foil and heated the furnace to 1030°C over about 20 minutes. The furnace stayed at 1030°C for another 20 minutes to clean and anneal the foil. The pressure was about 90 mTorr during this stage (compared to the base pressure of ∼10 mTorr).

We then began the slow growth stage, and flowed 7 sccm of methane for 5 minutes, raising the pressure to 280 mTorr. We then increased the methane flow to 60 sccm, which raised the pressure to 2 Torr. This was maintained for 5 more minutes, before we began cooling the system. The gas flow was maintained until the furnace temperature fell to 85°C, at which point we removed the copper foil from the furnace.

After growth, we spin coated the foil at 2000 rpm with PMMA (4% solution in anisole, referred to as A4) and baked it at 185°C for 30 minutes. This formed a thick (∼300 nm) polymer layer on one side of our foil. We then performed a reactive ion etch in the Zettl group's Plasma Etch system (50 W, 50 sccm O_2, 20 seconds) with the PMMA side down. This served to protect the graphene side under the PMMA while allowing the bare graphene side (now facing up) to be fully exposed to the plasma. This completely removed the unprotected graphene layer.

We then placed the sample copper-side-down onto an aqueous sodium persulfate solution (0.25 g/mL), making sure to float it on the surface. This was left for one hour so that the copper foil was fully etched away, leaving the graphene/PMMA floating on the surface. The samples were then transferred to two fresh deionized water baths to wash away the remaining etchant. All transfers were performed with a Teflon-coated lab spoon.

We used the freshly calcined hBN/SiO_2 substrates to lift the PMMA/graphene out of the water and placed the samples on a hot plate at 60°C for 4 hours to remove any residual water between the graphene and the substrate. After an overnight soak in acetone at room temperature to strip the PMMA, we were left with monolayer graphene covering most of the area of our boron nitride/silicon dioxide substrates.

Raman spectroscopy

At this time, we performed Raman spectroscopy on locations on and off the hBN using the Zettl group Renishaw Raman system. These results are shown in figure 4.3 with the spectrum of graphene on SiO_2 in blue and that of graphene on boron nitride in red. Differences between the two are apparent.

The graphene on SiO_2 shows a G-mode shift of 1595 cm^{-1} and a 2D shift of 2694 cm^{-1}, with a 2D/G ratio of 1.18 and a symmetric 2D line shape, consistent with other Raman studies of monolayer graphene [58] The graphene on hBN shows shifts of 1584 cm^{-1} and 2689 cm^{-1} with a ratio of 1.78. The hBN peak is also seen at its expected value of 1366 cm^{-1} [59] The softening of the G-mode and increased 2D/G ratio in graphene on hBN are both consistent with reduced external doping [60] and reduced substrate interaction [61], effects that are expected if the hBN underlayer is acting to isolate the graphene from the silicon dioxide.

The graphene on SiO_2 shows very little evidence of disorder in the form of a D-peak, which would appear at 1350 cm^{-1} [58]. The same observation can not be made for the graphene on hBN, since the hBN peak overlaps the D-peak location. However, since it is the same CVD graphene over the entire sample, we can assume that the rate of scattering processes that create the D-peak should be similar between the two, and thus absent in both.

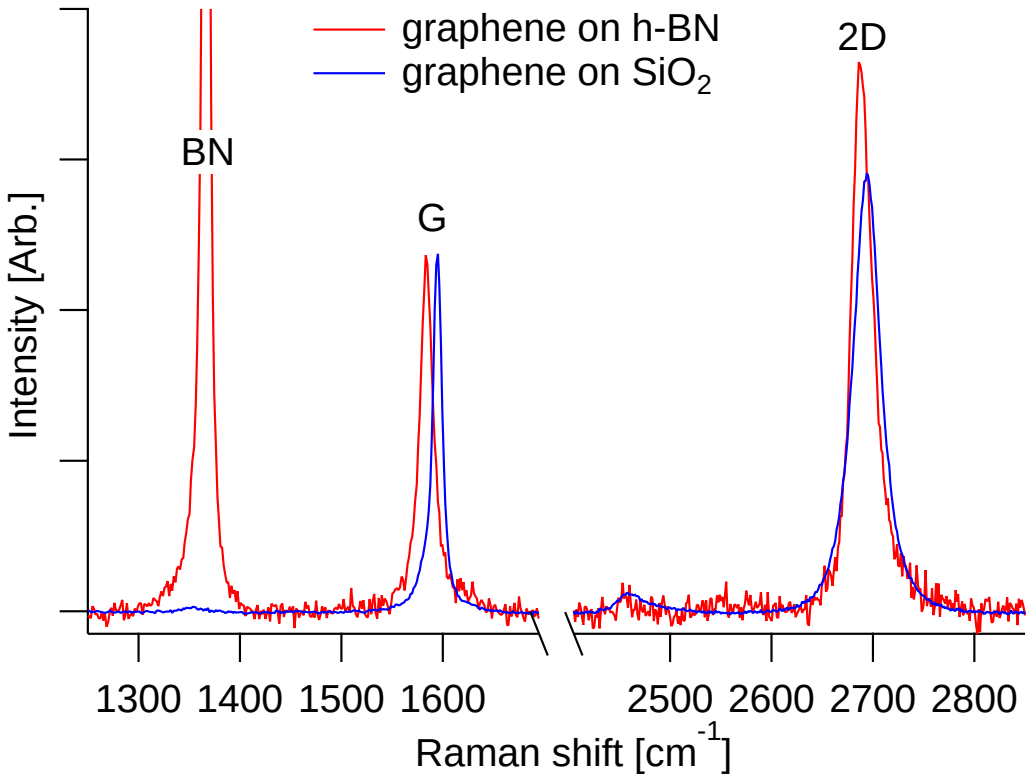

Figure 4.3: Raman spectrum of graphene on SiO_2 (blue) and hBN (red). The hBN peak is clearly visible at 1366 cm^{-1}. These data were collected with excitation from a 514 nm laser.

4.2.2 Lithography

Our substrates now had a mix of graphene on SiO_2 and graphene on boron nitride (on SiO_2). We mapped the devices in the Zettl group SEM with a 5 kV beam at spot 3, which allows the graphene, hBN, and oxide regions to be identified easily. After aligning the stage to the axes of the pre-patterned alignment mark array, we took a high-resolution image at 1000× at each alignment mark site. This was accomplished using the Nanometer Pattern Generation System (NPGS), which can be set up to automate sequences of image collection and stage moves. The images taken at 1000× only had a field-of-view of ∼210 µm, which means that given the 600 µm center-to-center distance of the alignment mark array, only about 12% of the sample area was mapped.

One such mapping image can be seen in figure 4.4. In this image, graphene covers the entire top half of the image and some of the bottom. The hBN flakes are apparent, and step edges on their surface are also visible. The four cross-shaped

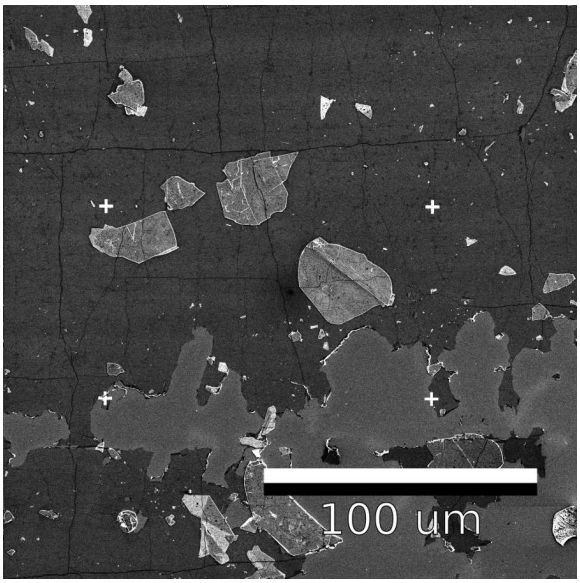

Figure 4.4: Exemplary SEM map image of CVD graphene on exfoliated hBN flakes.

alignment marks form a rectangle 120 µm by 70 µm. A connected network of dark lines is seen in the graphene; these are folds in the graphene and are discussed more in chapter 6.

The images were contrast-enhanced in image editing software (ImageJ or Adobe Photoshop) to make it easier to identify candidate regions for devices. We then made a DesignCad file that included each map image at the correct scale so contacts could be designed directly on top of the map image.

Criteria for these device locations included having clean, intact graphene, presence (or absence) of flat regions of hBN, absence of obvious contamination, and room to place large contact pads and leads. We designed a mix of devices, some on boron nitride and some on silicon dioxide. Once the patterns were designed, the rest of the sample processing followed as quickly as possible.

We performed electron beam lithography on the devices as explained in appendix B.1 to form an etch mask for each device. We etched the graphene into the desired Hall bar shape with the same reactive ion etch recipe as in section 4.2.1 (50 W, 50 sccm O_2, 20 seconds). The samples were then stripped in acetone and recoated with PMMA A4, and electron beam lithography was performed again to define the contact pattern. We then electron beam evaporated 4 nm Cr and 50 nm Au to form contacts.

A schematic of the sample fabrication steps appears in figure 4.5.

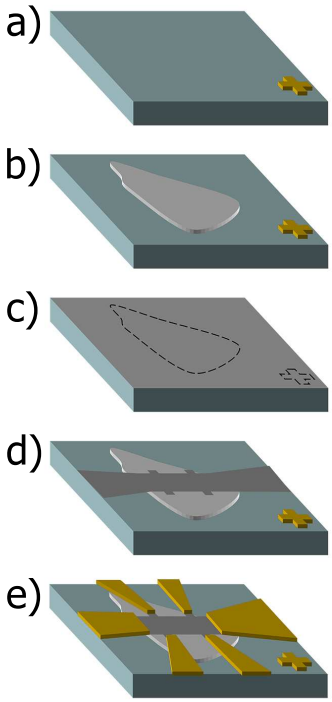

Figure 4.5: Schematic of graphene-on-BN field effect transistor (FET) fabrication. We (a) prepared substrates with gold alignment marks and (b) exfoliated boron nitride onto them. We then (c) transferred CVD graphene over the whole sample (d) performed lithography to etch it into a Hall bar, and (e) evaporated contacts onto the graphene.

4.3 Resulting devices

The final design of the devices were as shown in figure 4.6. They were 6-probe Hall bars for both redundancy and the possibility of future magnetoconductivity measurements. The graphene channels were 10 µm wide with 10 µm between the voltage probes, giving the device a 1:1 aspect ratio. Because they were fabricated on degenerately doped silicon with 300 nm of oxide, the devices with no hBN had back gate capacitances of $\sim$115 aF/cm^2. The devices on hBN had capacitances lower than this due to the additional hBN between the gate and the graphene, which we calculated using AFM measurements of the hBN flakes.

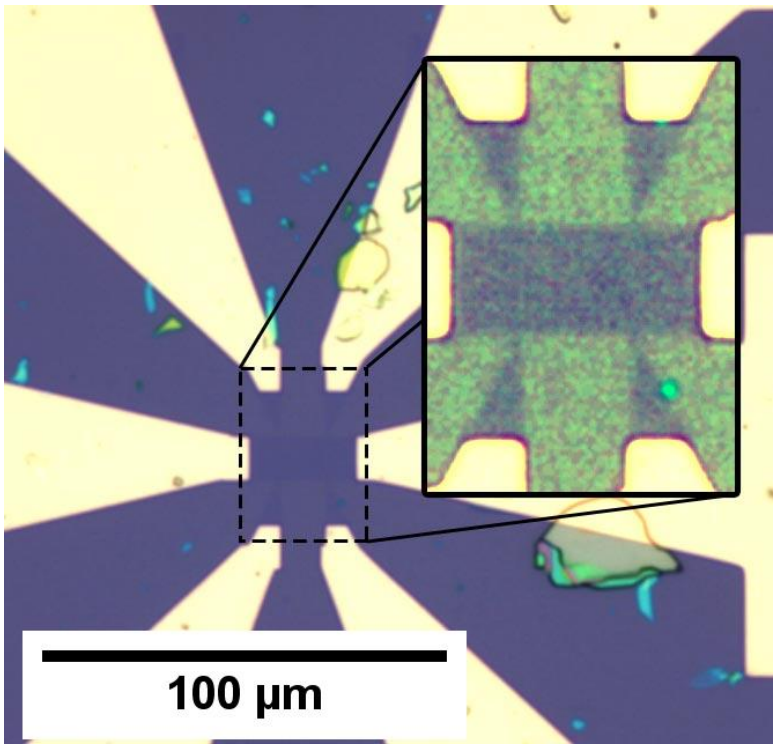

Figure 4.6: Optical micrograph of final graphene device on a SiO_2/Si substrate. Inset shows magnified and contrast enhanced version to highlight the graphene channel shape and probes.

4.4 Transport measurement setup

The devices were placed in a DesertCryo TTP4 high vacuum probe station with a flow cryostat and temperature controller and electronically connected to the sample stage with a dab of colloidal graphite (EMS Graphite Conductive Adhesive 154). We decided on a four-probe measurement to eliminate the effects of contact and probe resistance. To further eliminate noise, the measurements were made with a lock-in amplifier (Stanford Research Systems SR830).

We set the SR830's internal signal generator to output a 17 Hz sine wave at 1 V, which we connected to a 10 MΩ resistor. The resistor was then connected to one of the current leads on the graphene device while the other was grounded. Given the low output impedance of the SR830 (50 Ω) and the relatively low resistance of the graphene channel (∼100 Ω to 10 kΩ, depending on gate voltage and sample) the resistor turned the SR830 output into a 100 nA current source.

The two voltage probes on the graphene device were then connected to the A and B inputs on the SR830, which was set to differential measurement (A−B) mode. This ensured that the resulting measurement was only the voltage drop in the graphene channel between the voltage probes, and therefore a known geometry.

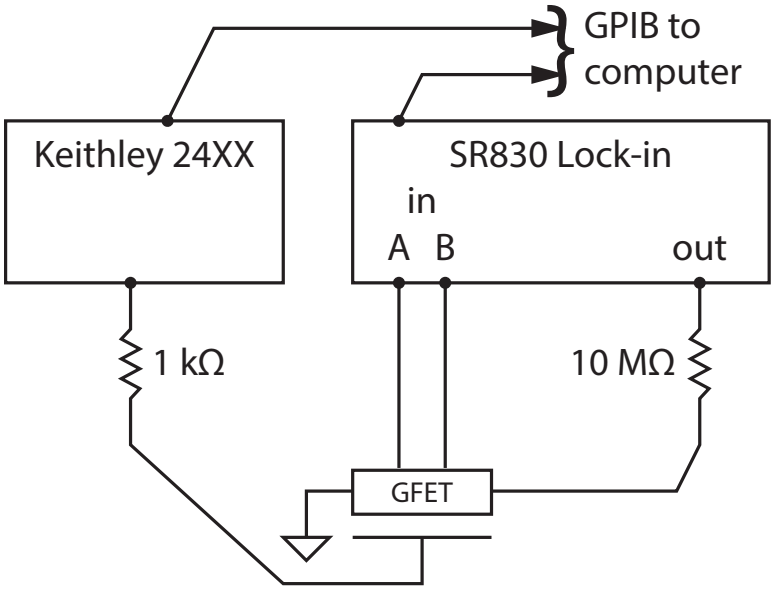

Figure 4.7: Schematic of measurement setup for a graphene field effect transistor (GFET) in the probe station.

The sample mounting plate in the probe station is electrically isolated from the rest of the chamber, allowing its voltage to be controlled by a triaxial connector on the underside of the probe station. We connected this to a Keithley 2400 sourcemeter.

Both the Keithley 2400 and the SR830 were connected to a computer running LabVIEW and interfaced with GPIB. The LabVIEW VI was a modification of one written by Brian Kessler and Çağlar Girit, former Zettl group graduate students. It controlled the Keithley and collected data from both the Keithley and the SR830, sweeping the gate voltage while measuring the leakage current as well as the amplitude and phase of the lock-in. This made it extremely easy to collect resistance versus gate voltage data for a given device.

4.5 Preliminary transport measurements

Of the ten devices designed and fabricated, nine survived for preliminary measurements: four devices on SiO_2 and five devices on boron nitride. We took gated conductivity measurements for all devices at both 300 K and 4.2 K to determine the temperature dependence of the scattering processes.

The mobilities as calculated from here on were derived from the slope of the conductivity versus gate voltage taken near the charge neutrality point. This technique assumed that the capacitance of the device was that of a simple parallel plate capacitor. This was reasonable given that the ratio of the "plate" width to separation

		300 K		4.2 K	
Substrate	Device #	V_D (V)	μ_e (cm^2/V·s)	V_D (V)	μ_e (cm^2/V·s)
SiO_2	23	-18	3700	17	4600
	31	2	3400	-1	4000
	32	0	3800	-2	5400
	33	-5	5300	-18	9000
hBN	43	-32	1600	-42	1700
	45	< -50	1100	< -50	1700
	51	-42	1800	< -50	3200
	54	-28	2800	-34	4600
	55	-41	2700	< -50	3600
	SiO_2 avg.	-5 ± 9	4100 ± 900	-1 ± 14	5800 ± 2000
	hBN avg.	$-39\pm 9^*$	2400 ± 900	$-45\pm 7^*$	3500 ± 1600

Table 4.1: Mobilities and Dirac point gate voltages of devices on SiO_2 and hBN at room temperature and 4.2 K. The values marked * are those that rely on values beyond the measurement range, so the upper limit, -50 V, was substituted. Thus, the averages themselves are upper limits.

was ∼33.

For the devices on boron nitride, the hBN flake under the graphene increased the separation between the silicon and the conducting channel. This changed the specific capacitance, which in turn changed the relationship between the carrier density n and the gate voltage. To compensate for this, we took height profiles of the underlying hBN flakes using an AFM. We then recalculated the capacitance as a parallel plate capacitor with a dielectric of 300 nm SiO_2 and the measured thickness of hBN, with a static dielectric constant of 4 [52] for the boron nitride.

4.6 Additional sample processing

4.6.1 Contamination observation

Our initial goal with this project was to produce high-mobility CVD graphene by using the highest quality substrates, but the data in table 4.1 are unremarkable. We thus decided that an annealing step was needed. This was borne from both prior work (Dean et al. [51]) and our own observations of graphene on boron nitride structures.

When CVD graphene samples were observed in the SEM, we frequently saw dark patches in the graphene, especially when the graphene was on a boron nitride substrate. Such patches can be seen in figure 4.8. At higher magnifications, these patches were observed moving and reforming under the beam. This was consistent with a layer of contamination between the graphene and boron nitride. These patches are not gen-

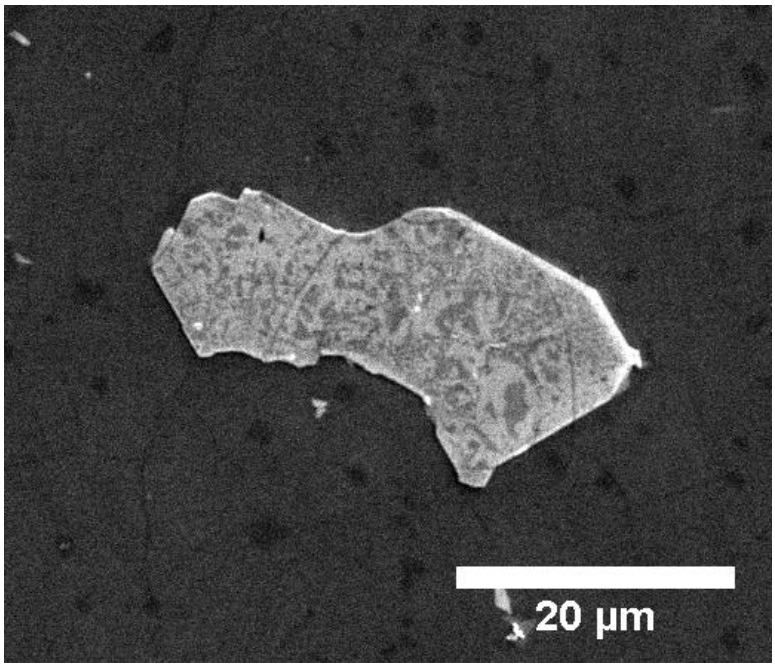

Figure 4.8: SEM image showing contamination between CVD graphene and boron nitride substrate.

erally seen under graphene on silicon dioxide, but it is presumably not due to a lack of contaminants. Instead the absence may be attributed to different wetting properties, a rougher interface, or poorer contrast in the SEM.

While we did not probe the composition of this contamination, other groups attributed similar observations to water or other contaminants trapped under graphene monolayers [62].

4.6.2 Annealing to remove contamination

Cleaning graphene devices after fabrication had been explored by a number of groups [20, 63]. In situ techniques, such as annealing the sample with Joule heating, had the advantage of limiting air exposure between annealing and measurement, something we were concerned with initially. We destroyed several devices using this technique. This may have been due to the inhomogeneity of CVD graphene. Exfoliated devices have few or no grain boundaries, while devices from CVD graphene usually have several. If these grain boundaries have high local resistivities, they may dissipate power in a much smaller area than the more crystalline exfoliated samples. These results caused us to explore tube furnace annealing as a potentially more reliable technique.

To remove the contamination, we annealed the sample in hydrogen, roughly following Dean et al. [51]. In the graphene growth tube furnace we flowed 410 sccm

		300 K		4.2 K		
	Device #	V_D (V)	μ_e (cm^2/V·s)	V_D (V)	μ_e (cm^2/V·s)	$\frac{\mu(\text{post-anneal})}{\mu(\text{pre-anneal})}$
SiO_2	23	23	2900	23	3300	0.72
	31	37	2400	45	2500	0.63
	32	30	3500	36	3000	0.56
	33	28	2400	no data		
hBN	43	−2	6700	−6	9200	4.8
	45	−1	5900	−3	8200	4.1
	51	−4	7600	−3	12400	3.3
	54	−2	15500	−2	28800	5.2
	55	−6	12900	−8	19900	4.4
	SiO_2 avg.	29 ± 6	2800 ± 500	35 ± 11	2900 ± 400	0.63 ± 0.08
	hBN avg.	−3 ± 2	9700 ± 4200	−4 ± 3	15700 ± 8700	4.4 ± 0.8

Table 4.2: Mobilities and Dirac point gate voltages of devices on SiO_2 and hBN at room temperature and 4.2 K, after an anneal at 340°C in H_2 and Ar. Device #33 did not survive cooling, and thus had no data at 4.2 K.

argon and 450 sccm hydrogen at atmospheric pressure. The temperature was raised to 340°C and held for 3.5 hours before cooling. We removed the sample from the tube at 65°C.

4.7 Post-anneal transport measurements

We again measured the devices in the probe station at both room temperature and 4.2 K. Gated conductivity plots for two devices (one each on hBN and SiO_2) are shown in figure 4.9, and extracted parameters from all such post-anneal results are shown in table 4.2.

Table 4.2 contains some very important findings. The devices on SiO_2 exhibited a significant change in doping after annealing, as seen by comparing table 4.2 with table 4.1. The charge neutrality voltages moved from −1 V pre-anneal to 35 V post-anneal at 4.2 K, a change of +36 V. The devices on hBN exhibited a similar shift, from −45 V to −5 V at 4.2 K, a change of +40 V. These post-anneal values correspond to carrier densities (at $V_g = 0$ V) of 2.7×10^{12} holes/cm^2 and 3.7×10^{11} electrons/cm^2 for graphene on SiO_2 and hBN, respectively.

The devices on boron nitride had consistently higher mobilities after the annealing than those on SiO_2, with the average mobility on hBN over five times higher than on oxide. These are examined in more detail in section 4.8.

We also collected temperature dependent conductivity data for the same graphene devices on SiO_2 and hBN. Unfortunately this occurred several weeks after the above data collection, and the device mobilities had degraded in that time, presumably from

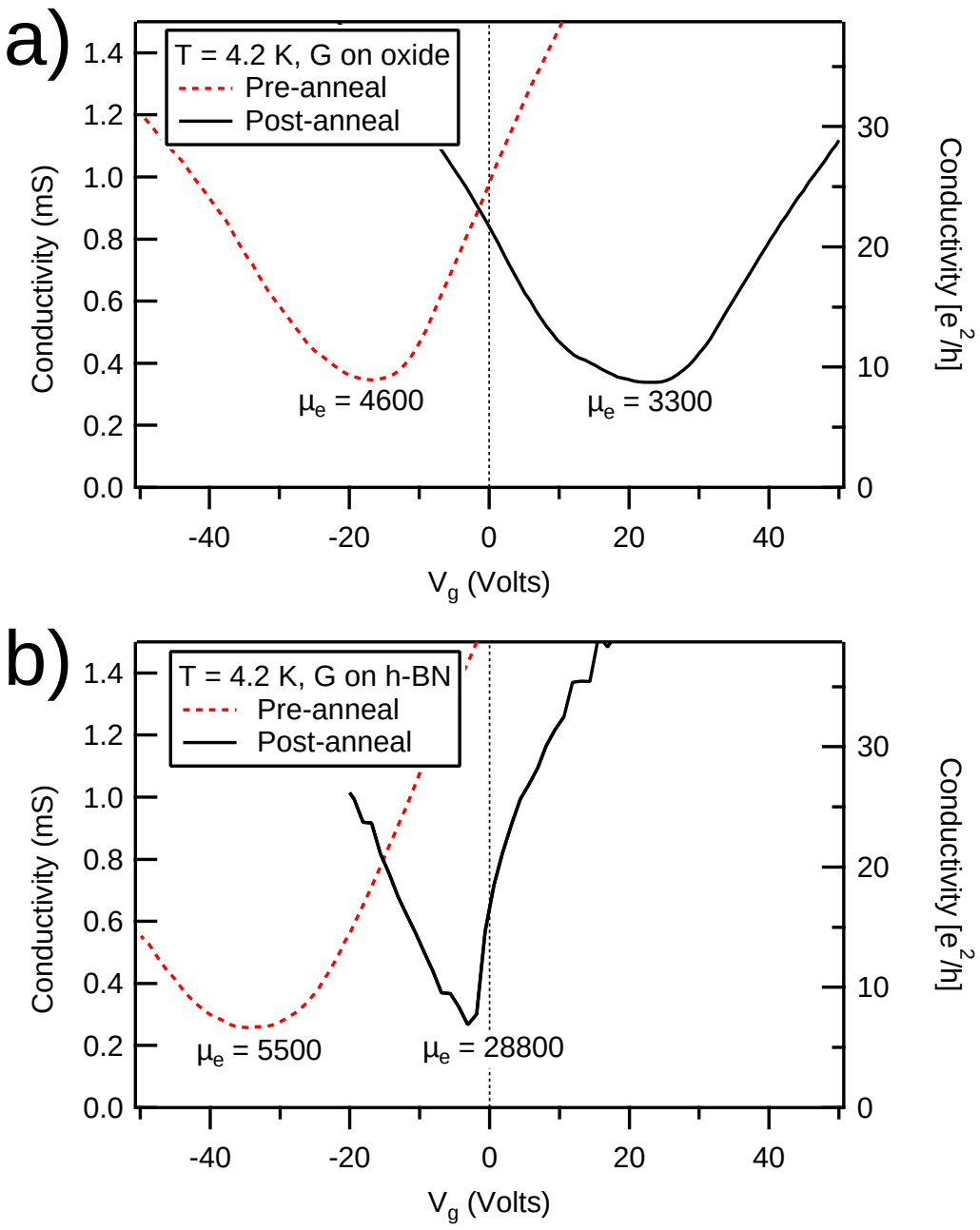

Figure 4.9: Conductivity vs gate voltage data for a device on (a) SiO_2 and (b) boron nitride (devices #23 and #54, respectively) [57].

exposure to air or other contaminants. We re-annealed them with the same recipe as in section 4.6.2 and collected data as before, this time stopping to collect data at a number of temperatures between 4.2 K and 293 K.

The data were collected in order of increasing temperature with an additional measurement at 293 K taken prior to cooling. The mobilities were still not as high as those in table 4.2, collected after the first anneal, presumably due to remaining contamination or irreversible damage to the sample from the anneal. Summaries of the temperature dependence data appear in figure 4.10 (mobilities versus temperature) and figure 4.11 (conductivity minima versus temperature).

4.8 Data analysis

4.8.1 Unannealed samples

Analyzing the data in table 4.1 with a t-test, we find that the unannealed graphene on boron nitride has lower mobility at room temperature than that on oxide with significance $p < 0.03$. This significance disappears at 4.2 K as the range of values increases for both sample sets. The relative shift in the Dirac point voltage remains significant in both cases.

The low temperature data have consistently higher mobilities than the room temperature data; this is consistent with less phonon scattering at lower temperatures. Since the mobilities are inversely proportional to the total scattering rates, we can attempt to quantify this phonon scattering in relative terms as follows.

The total scattering rate r can be separated into two parts: a temperature independent term, r_0, and a temperature dependent term that is negligible at 4.2 K, r_T. Based on our definition of the parts of r, we can assert that

$$\begin{aligned} \mu(300\,\mathrm{K}) &\propto \frac{1}{r_0 + r_T} \\ \mu(4.2\,\mathrm{K}) &\propto \frac{1}{r_0}. \end{aligned}$$

Since each equation has the same proportionality constant, we can now invert each and subtract to find

$$r_T \propto \frac{1}{\mu(300\,\mathrm{K})} - \frac{1}{\mu(4.2\,\mathrm{K})}, \tag{4.1}$$

allowing us to look at how scattering changes with temperature in the unannealed samples. These results are shown in table 4.3.

With a single exception, the hBN samples have higher temperature dependent scattering rates than samples on SiO_2. However, these are not statistically distinguishable ($p \sim 0.15$) due to the high variance. Differences between samples on different substrates would not be surprising, however, since substrate phonons are known to affect carrier scattering in graphene [64].

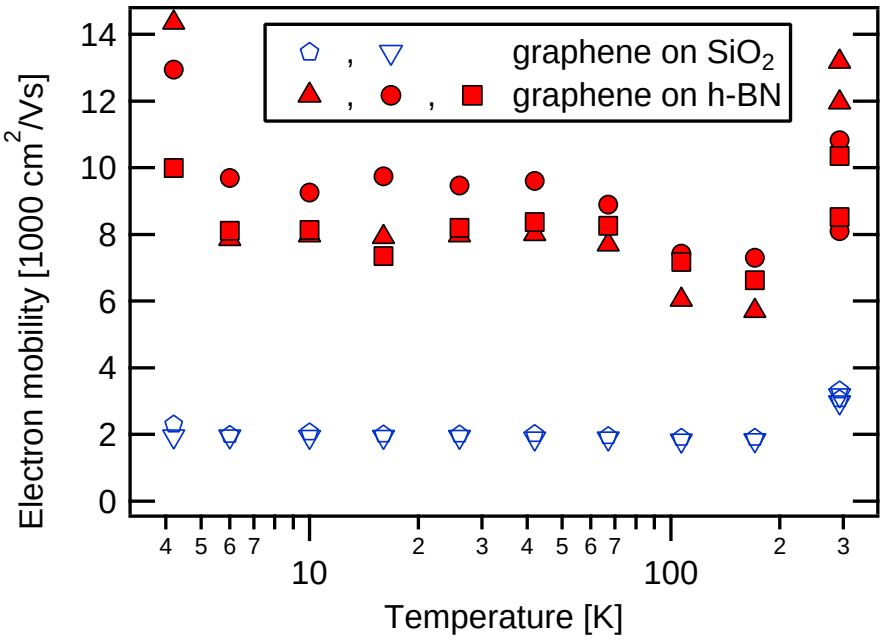

Figure 4.10: Electron mobilities of devices on SiO_2 (blue) and hBN (red) vs temperature from 4.2 K to 300 K [57].

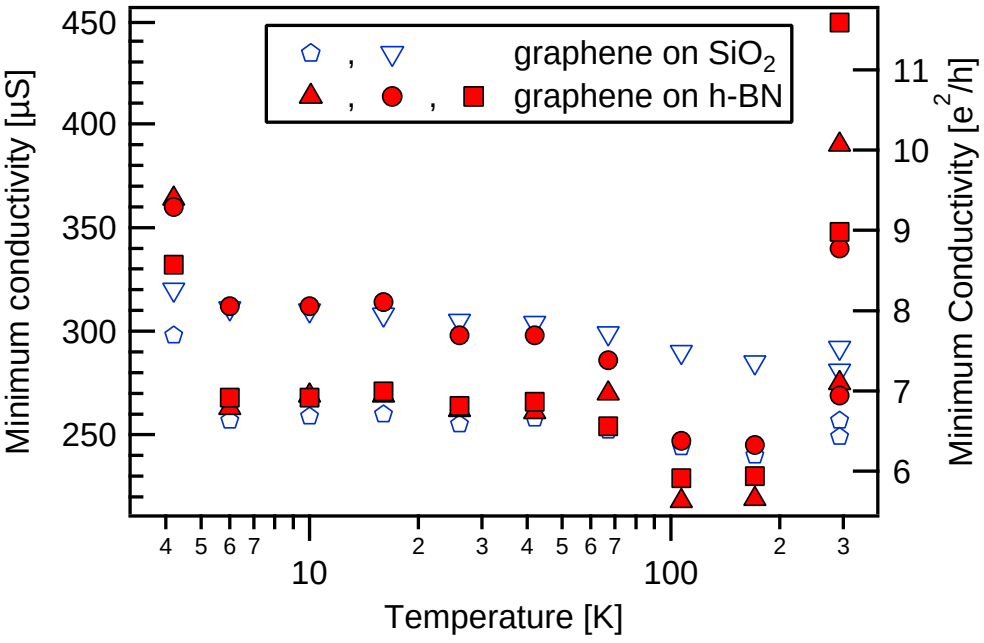

Figure 4.11: Conductivity minima of devices on SiO_2 (blue) and hBN (red) vs temperature from 4.2 K to 300 K [57].

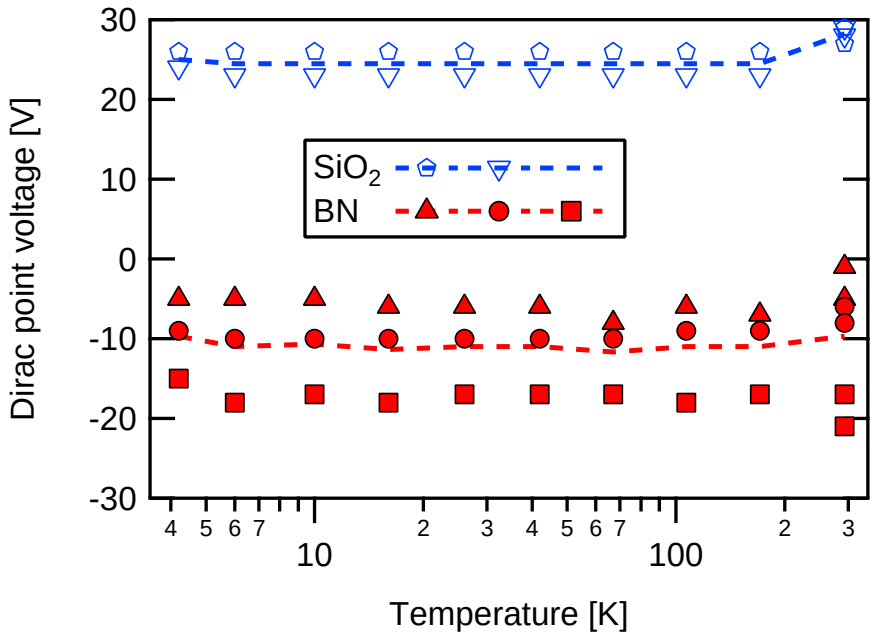

Figure 4.12: Dirac point voltage of devices on SiO_2 (blue) and hBN (red) vs temperature from 4.2 K to 300 K. Average voltages for each substrate appear as dashed lines.

Substrate	Device #	r_T (A.U.)
SiO_2	23	1.6
	31	1.4
	32	2.4
	33	2.4
hBN	43	1.0
	45	8.3
	51	6.3
	54	3.6
	55	2.3
	SiO_2 avg.	1.9 ± 0.5
	hBN avg.	4.3 ± 3.0

Table 4.3: Temperature dependent portion of scattering rates (normalized to device #43) calculated from mobility changes between room temperature and 4.2 K of unannealed devices.

Substrate	Device #	r_T (A.U.)
SiO_2	23	1.3
	31	0.51
	32	-1.5
hBN	43	1.3
	45	1.4
	51	1.6
	54	0.91
	55	0.83
	SiO_2 avg.	0.1 ± 1.3
	hBN avg.	1.3 ± 0.3

Table 4.4: Temperature dependent portion of scattering rates after annealing (normalized to device #43 pre-anneal, as in table 4.3) calculated from mobility changes between room temperature and 4.2 K.

Additionally, it is important to remember that while we calculated these numbers with phonon scattering in mind, they are in actuality the sum of all temperature-dependent scattering effects. This includes phonons but may also include effects such as adsorption of species on the sample at low temperatures, which may reduce the calculated number. This adsorption may itself be substrate-dependent as well.

4.8.2 Annealed samples

By performing the same analysis from table 4.3 on the post-anneal devices, we obtained the results shown in table 4.4. Most of the samples had close normalized scattering rate values, meaning that increasing the temperature introduces approximately the same scattering rate increase across all samples.

The noticeable exception to this is sample #32, which showed a decrease in mobility with reduced temperature. Looking back at table 4.2, we see that it was also the only sample to have a significant change in the Dirac point voltage between room temperature and 4.2 K. Both of these phenomena were consistent with the introduction of charged scatterers between the two measurements. One possibility was the adsorption of species from the measurement chamber as the sample was cooled, but it was not possible to show this conclusively.

Using this same concept, we can look at our temperature dependence data from figure 4.10 in a new way. Figure 4.13 shows the same data inverted, plotting μ^{-1} against temperature for both oxide (blue) and hBN (red) substrates as before. The graph also displays dashed lines through the average values for each substrate type at each temperature as a guide to the eye.

The boron nitride substrates have significantly less scattering than the SiO_2 sub-

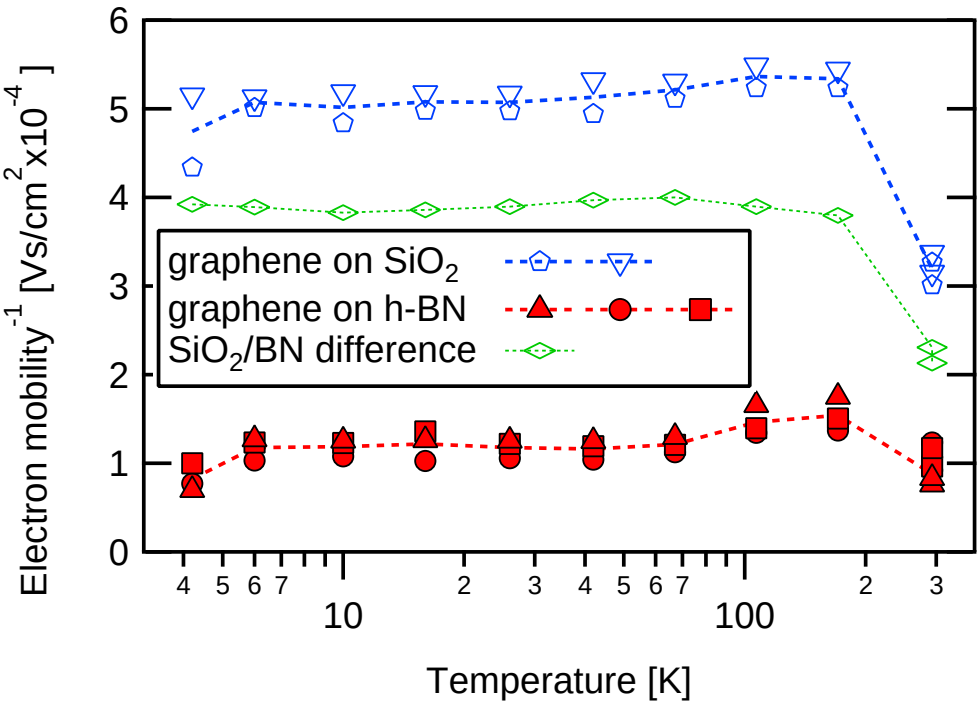

Figure 4.13: Inverse electron mobility ($\propto$ total scattering rate) vs temperature from 4.2 K to 300 K. Devices on SiO_2 appear blue and devices on hBN red. The dashed blue and red lines are the average values for each type of device at a given temperature. The green line is the difference between the oxide and hBN averages at each temperature and is referred to as the differential substrate scattering rate (DSSR).

strates, as expected. However, both sample types exhibit qualitatively similar temperature dependence, especially when looking at the dashed "average" line. Some of this is due to intrinsic rather than extrinsic effects. By Matthiessen's rule, these intrinsic scattering effects, which should be the same for both substrates, can be subtracted away if we look at the difference in the two scattering rates [18]. This difference between the average scattering on each substrate will be called the differential substrate scattering rate (DSSR) and is plotted in green in figure 4.13.

Except for the values at room temperature, the DSSR is very constant, with a standard deviation of 1.6% of the mean and no noticable trend. This is in contrast to the average data from each substrate, which have temperature-dependent variations that are both about 3 times larger than those of the DSSR. This means that the temperature dependent portion of the scattering in each device is largely substrate-independent, and in turn the substrate dependent portion is largely temperature independent.

The room temperature values are a special case, since all samples exhibited lower scattering at room temperature than the next-highest temperature (171 K= -102°C). This could be partially explained by cryosorption of material onto the sample, presumably water since no other common species would condense at such high temperatures. It is also possible that solvents from the carbon paint used to mount the samples could have lingered and recondensed on the sample, but water was certainly present as well. Water could have been introduced to the chamber any time samples were exchanged, desorbed from the chamber while pumped, adsorbed onto the sample when it cooled, and frozen in place.

If this were the case, we would expect to have seen temperature-dependent changes in doping on all samples. However, as figure 4.12 shows, there was only a very slight change in doping associated with the change in mobility. The samples on oxide had their mean Dirac point voltage change from approximately 28 V to 25 V going from 293 K to 171 K while the samples on hBN shifted from -10 V to -11 V. These correspond to carrier concentrations at $V_G = 0$ V changing by -3×10^{11} holes/cm^2 and $+1 \times 10^{11}$ electrons/cm^2 respectively. For comparison, an areal density of 10^{11}/cm^2 corresponds to approximately one carbon atom in 40,000 in the graphene lattice. While this trend held for four of the five samples, it is not statistically significant according to a pairwise t-test.

In addition, the previous data in tables 4.1 and 4.2 did not show this consistent shift. These data have been compiled into table 4.5, which includes differences between 4.2 K and 300 K for pre- and post-anneal data. Due to the large variance in the shifts, these are also not statistically significant and thus we can not make any additional conclusions about doping from cryosorption from this data.

To further explore the relationship between mobility and doping, electron mobility is plotted against voltage at the conductivity minimum in figure 4.14a. We would expect highly doped samples to have lower mobilities due to increased scattering from charged impurities and undoped samples to have higher mobilities due to less

		Pre-anneal		Post-anneal			
	Device #	300 K	4.2 K	300 K	4.2 K	$\Delta V_{D\ \mathrm{pre}}$	$\Delta V_{D\ \mathrm{post}}$
SiO_2	23	-18	17	23	23	35	0
	31	2	-1	37	45	-3	8
	32	0	-2	30	36	-2	6
	33	-5	-18	28		-13	
hBN	43	-32	-42	-2	-6	-10	-4
	45	< -50	< -50	-1	-3	0	-2
	51	-42	< -50	-4	-3	-8	1
	54	-28	-34	-2	-2	-6	0
	55	-41	< -50	-6	-8	-9	-2
	SiO_2 avg.	-5 ± 9	-1 ± 14	29 ± 6	35 ± 11	4 ± 22	5 ± 4
	hBN avg.	-39 ± 9	-45 ± 7	-3 ± 2	-4 ± 3	-7 ± 4	-1 ± 2

Table 4.5: Changes in Dirac point gate voltages at different temperatures, pre- and post-annealing. All units are Volts.

scattering. Our data appears to be qualitatively consistent with this, as all of the higher mobility samples have Dirac points near 0 V.

In figure 4.14b, we plot the inverse mobility, which as mentioned above is proportional to the total scattering rate, against the Dirac point location. The Dirac point should shift linearly with the introduction of charged scatterers, and the scattering rate should increase linearly as well. This means that assuming a given sample has mostly negative or mostly positive charged impurities, the inverse mobility versus Dirac point voltage plot should look V-shaped, increasing linearly away from the origin on both sides.

This is roughly what we see in figure 4.14b, especially for the post-anneal devices. The deviation of the pre-anneal devices from this model may have been due to the presence of both positive and negative charged scatterers, which introduced scattering but had their doping effects partially cancel. The annealing process then preferentially removed the n-type impurities, leaving only the p-type impurities.

4.8.3 Coulombic vs short range scattering

One final analysis we can perform is to compare the amount of short range scattering to the Coulombic scattering. This can be accomplished by fitting a curve to our gated conductivity data of the form seen in equation 2.9, where the short range scattering adds a resistivity independent of carrier concentration. The fit also includes a small constant conductivity offset, since the conductivity minimum is never zero. In this way, we can separate the effects of Coulombic scatterers from the short range scatterers. Three devices with suitable data were analyzed, all on hBN substrates.

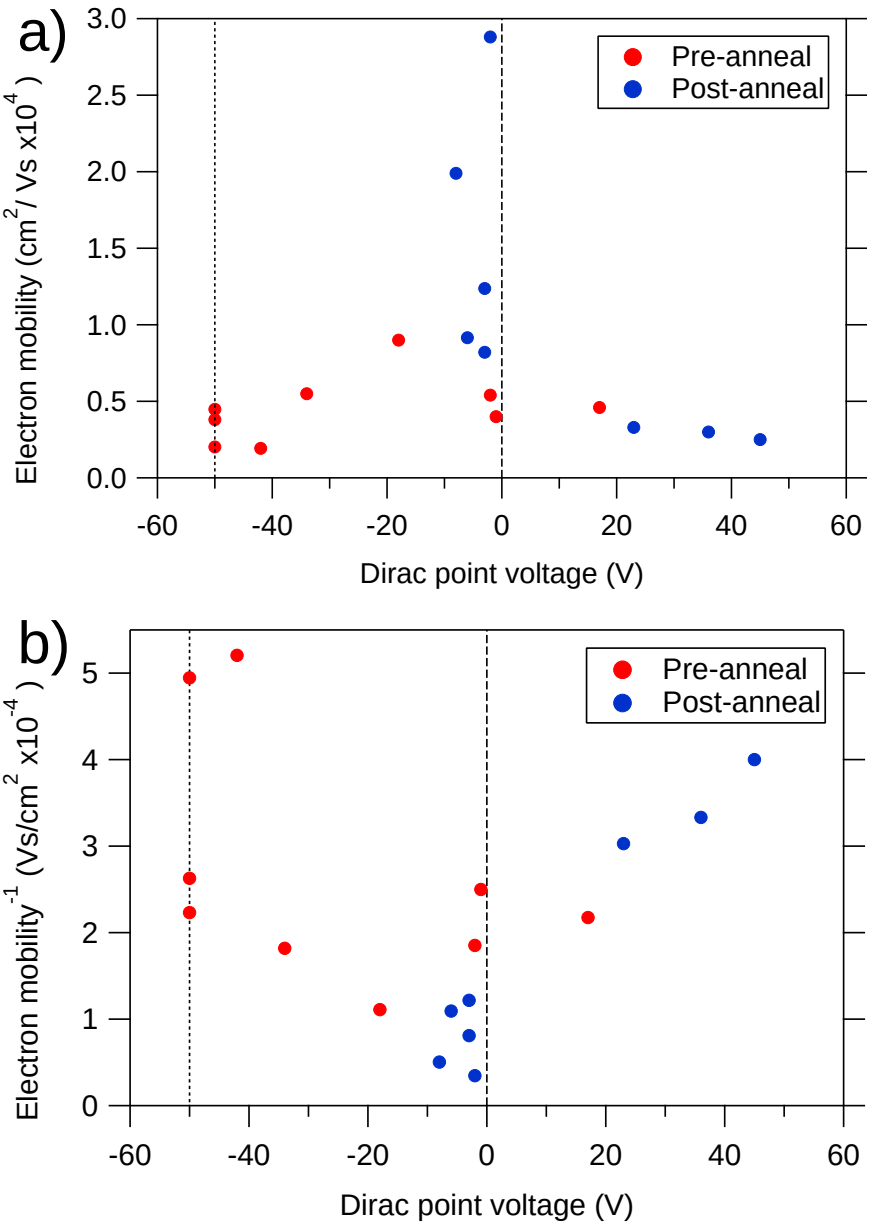

Figure 4.14: (a) Electron mobilities and (b) inverse electron mobilities vs Dirac point voltage for samples on both SiO_2 and hBN at 4.2 K. The vertical line at 0 V represents the location of minimally doped samples. The vertical line at -50 V represents the cutoff of our data; anything on that line in actuality lies an unknown distance to the left.

	μ_{total}		μ_{Coulomb}		% Coulombic	
Device	300 K	4 K	300 K	4 K	300 K	4 K
43	6440	13600	6670	9150	104%	67.5%
54	21500	36600	15500	28800	72.2%	78.8%
55	15400	25500	12900	19900	83.8%	78.0%

Table 4.6: Mobility data from linear fits (μ_{total}) and fits calculating mobility from Coulomb scattering alone (μ_{Coulomb}) for three devices on hBN substrates. Units of μ are cm^2/Vs.

Table 4.6 shows data from three devices on hBN. The percentage of scattering from Coulombic scatterers is calculated as $(1/\mu_{\text{Coulomb}})/(1/\mu_{\text{total}}) = \mu_{\text{total}}/\mu_{\text{Coulomb}}$. For some reason, the Coulomb mobility fit on sample 43 produced a lower mobility than the linear fit, and so the calculated percentage is greater than 100%. Other than that data point, the samples all have Coulomb scattering responsible for ∼70-80% of their total scattering at low carrier densities. Reducing either short range scatterers or charged scatterers should have a noticeable effect.

4.9 Conclusions

Our fabrication of graphene transistors on hBN and SiO_2 substrates gave us valuable data on the nature of scattering in CVD graphene and its promise for the future.

Because CVD graphene on hBN has a consistently higher mobility than the same CVD graphene on oxide, it is clear that the low mobility frequently measured on oxide is from extrinsic effects. Indeed, the intrinsic scattering in CVD graphene clearly allows devices to consistently have mobilities over 10,000 cm^2/Vs. This alone is very promising for CVD graphene.

However, the exact nature of this scattering on SiO_2 remains unclear. If it is merely scattering from the substrate itself, why is exfoliated graphene not also limited to mobilities of 3,000 cm^2/Vs on identical SiO_2? One possible explanation is that contaminants inherent to the CVD growth or the copper etching remain present on the SiO_2 substrates but are more easily removed from the hBN regions, causing a difference in the total scattering rates.

It is also important to point out that this work suggests that measuring the quality of CVD graphene (or its growth recipe) by making mobility measurements in FETs on SiO_2 is probably a poor method. Because extrinsic effects dominate, the mobility measurement is mostly an assessment of the interaction with the substrate. If graphene quality is to be determined by transport measurements, the substrate must scatter carriers at a rate lower than the graphene itself.

Exfoliated hBN has thus far been the best substrate for CVD graphene samples, but it is far from compatible with wafer-scale fabrication. If CVD graphene is to be in-

tegrated with wafer-scale technologies, more scalable substrates will be required. Possible examples include CVD hBN, well-passivated oxide layers, or Langmuir-Blodgett films. More research is required on all of these before high quality CVD graphene becomes truly scalable.

4.10 Graphene p-n junctions

As seen in table 4.5 and figure 4.12, there was a significant difference in carrier concentration between graphene devices on SiO_2 and hBN both before and after annealing. The devices on hBN were consistently more n-type at $V_g = 0$ than their oxide counterparts, with either more electrons or fewer holes.

This led to the idea that, regardless of what was causing the differences, a piece of graphene partially on hBN and partially on oxide would have two regions with very different carrier concentrations. By using a single back gate, one could then add or remove additional carriers until the hBN side was n-type and the oxide side was p-type, forming a p-n junction at the interface.

The measured differences between Dirac point voltages on hBN and SiO_2 were around 40 V, as seen in table 4.5. This 40 V difference meant that such a device could be gated such that one side had 1.4×10^{12} electrons/cm^2 (+20 V) and the other had 1.4×10^{12} holes/cm^2 (-20 V). A simple simulation of such a device is shown in figure 4.15, with the equal-carrier voltage defined as 0 V.

The simulation assumed that two differently doped squares of graphene are in series, for an overall device aspect ratio of 2:1. The dips in conductivity at the two Dirac points were still present, and between the two is a region of high conductivity, where each half has a relatively high carrier concentration. The existence of a depletion region was not modeled, and the interface between the two regions is ignored.

We can compare this simple simulation to an actual device that Will Regan and I fabricated. Electron micrographs of one device are shown in figure 4.16. The left half of the graphene is on boron nitride, and the right half is on SiO_2. Conductance data are shown in figure 4.17.

We did not attempt to make a sophisticated photocurrent measurement of this device. Due to the small size and low absorption of the junction region, we expected a response below the noise of our measurement setup. However, with the proper optical apparatus including a chopper and lock-in amplifier, such measurements may give us information about the p-n junction.

4.11 Collaborations

We were the first group to fabricate graphene devices on boron nitride substrates with an extremely scalable method. This led to a great deal of interest from other

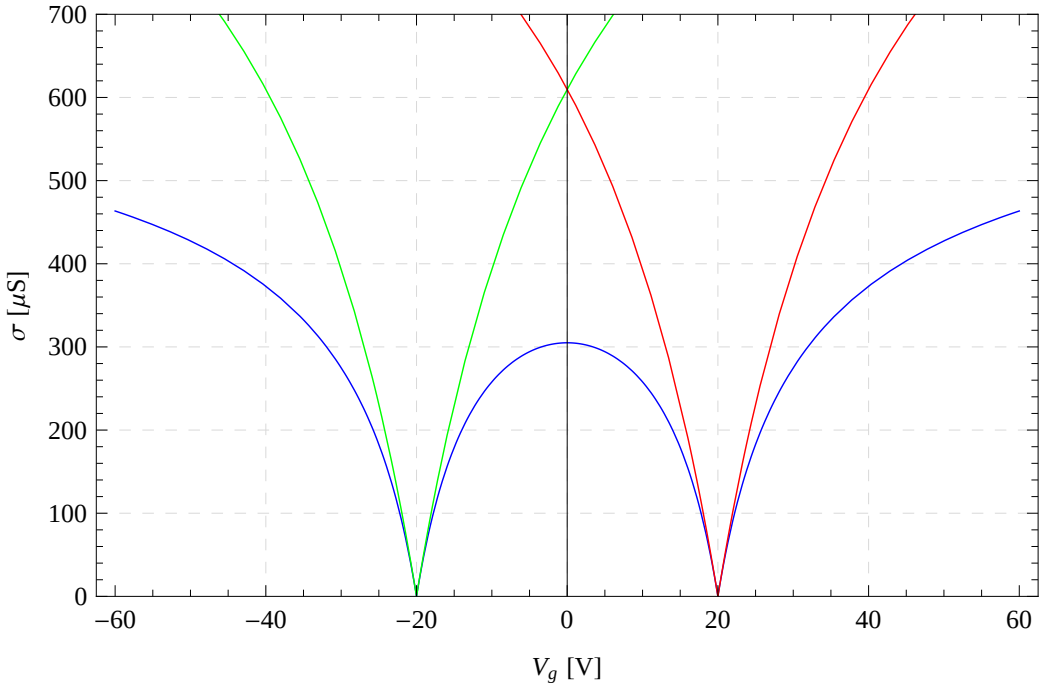

Figure 4.15: Simulated conductance of a graphene p-n junction gated through 300 nm of SiO_2. The carrier concentration in each half at $V_g = 0$ is 1.4×10^{12} electrons/cm^2 or holes/cm^2, giving the two halves a difference in Dirac point voltage of 40 V. The n-doped region is shown in green, the p-doped region is shown in red, and the whole device (both in series) is shown in blue. The simulated device has scatterer concentrations of 10^{12}/cm^2 and 10^{11}/cm^2 for charged and short range scatterers, respectively.

groups who wanted to make measurements on our devices with specialized characterization techniques.

4.11.1 STM of graphene on hBN

Dr. Regis Decker, a postdoctoral researcher in the Crommie group at UC Berkeley, was able to perform scanning tunneling microscopy (STM) on CVD graphene on hBN substrates [65], following work done previously in the Crommie group by Dr. Yuanbo Zhang et al. [48]. The work by Zhang et al. demonstrating the spatial extent of "charge puddles" was one of our initial motivations for experimenting with hBN as a graphene substrate. Dr. Decker's work was published at the same time as similar work by Xue et al. [66].

Regis had several important results, including the observation of a Moiré pattern that depended on the rotational mismatch between the graphene and hBN lattices. However, the most relevant to this chapter was the comparison of graphene on hBN and graphene on SiO_2 with an STM, seen in figure 4.18. Plotted are maps of to-

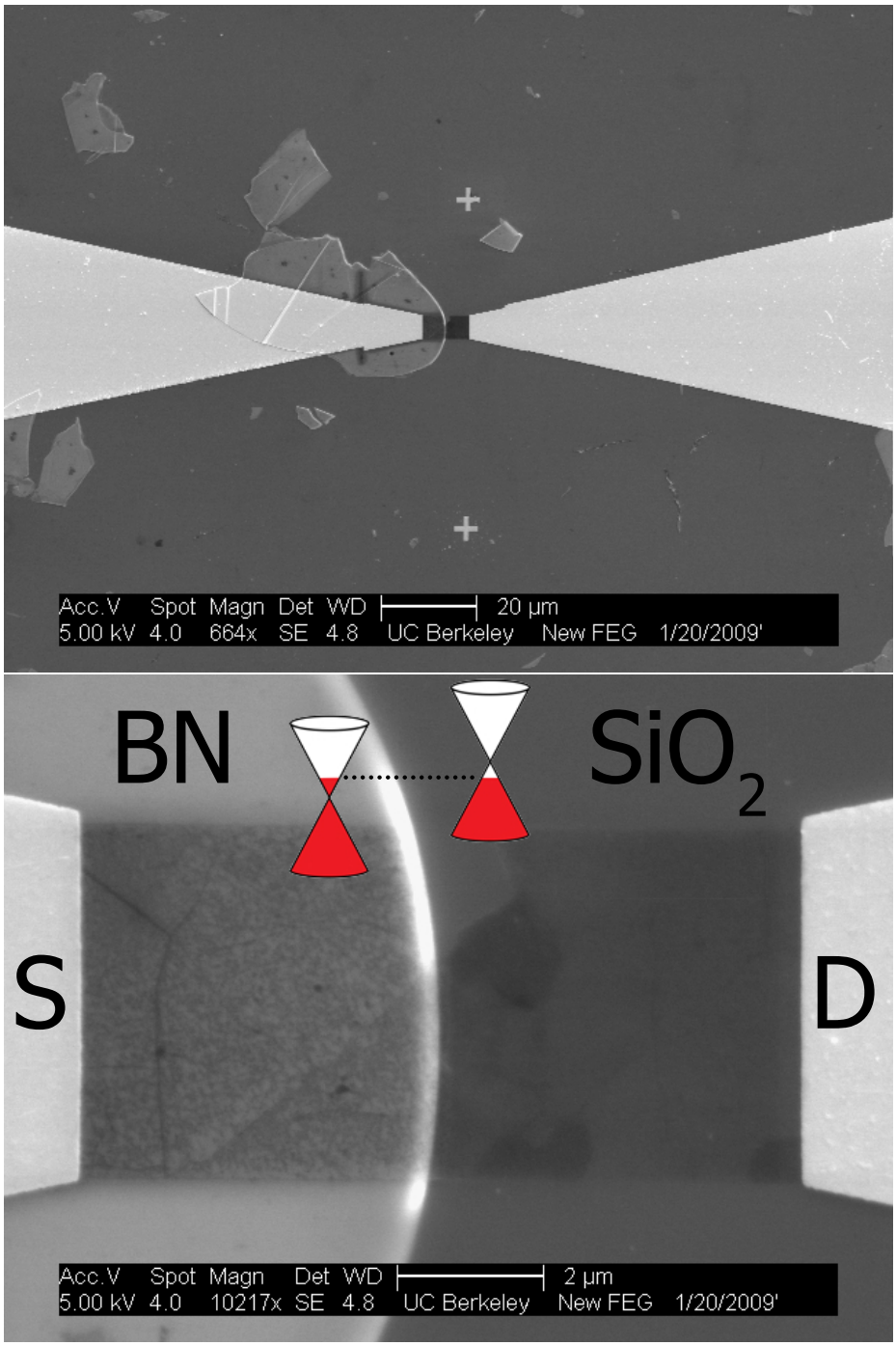

Figure 4.16: SEM images at two different magnifications of graphene p-n junction, half on hBN and half on SiO_2, with schematic Dirac cones shown.

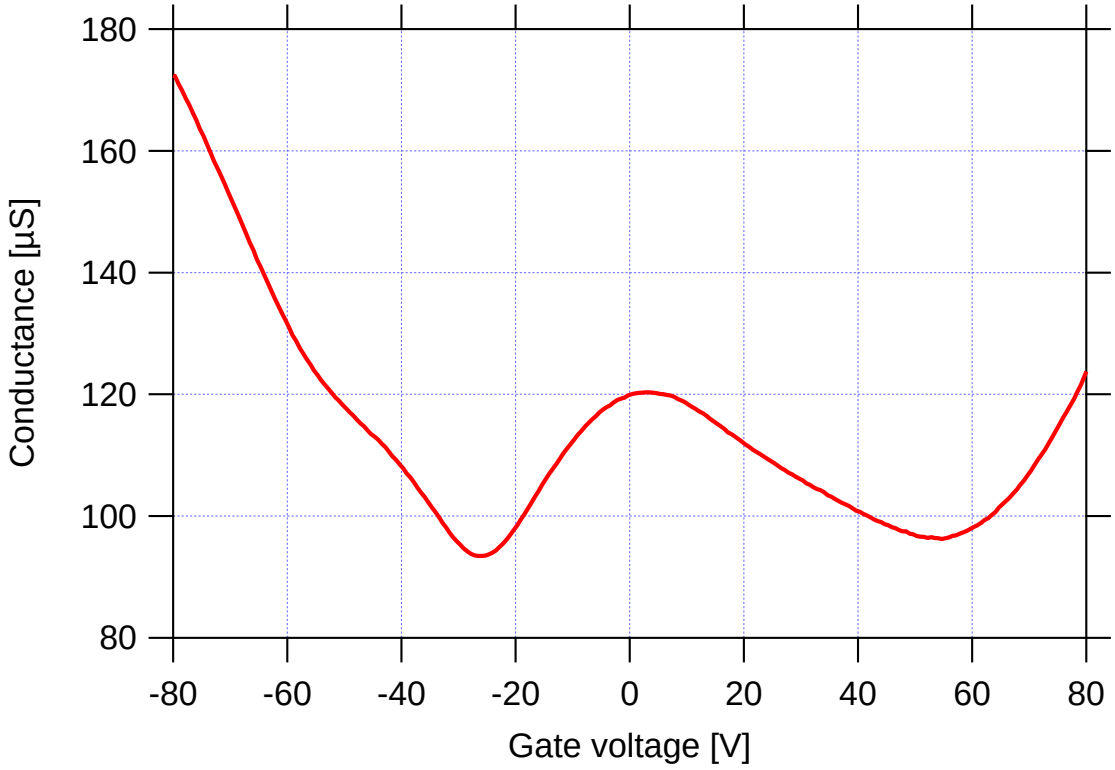

Figure 4.17: Gated conductance data of the graphene p-n junction shown in figure 4.16. (Sweep is from high to low V_g.)

pography (top) and charge density (bottom) on hBN (left) and SiO_2 (right). The differences between the hBN and SiO_2 substrates are immediately apparent. The graphene on SiO_2 had $\sim$100$\times$ more surface roughness than that on the hBN, which only varied by $\sim$10 pm.

Additionally, the variations in charge density were $\sim$2.5$\times$ smaller on hBN than on SiO_2, and significantly smaller than that over most of the scanned region. This flatness in the charge distribution was qualitatively consistent with the differences we measured previously in this chapter.

We can attempt a quantitative comparison as well. Previous samples on SiO_2 had an average post-anneal mobility of 2900 cm^2/Vs at 4.2 K (from table 4.2). Assuming the main contribution to scattering was from charged scatterers, we can use equation 2.6 and $\sigma = ne\mu$ to calculate that a mobility of 2900 cm^2/Vs corresponds to a charged scatterer density of $1.7\times10^{12}/cm^2$, which in turn corresponds to a mean scatterer separation of 8 nm. For devices on hBN, the same calculations give a mean scatterer separation of 18 nm.

If we assume that the charge density fluctuations measured by STM were due to the presence of the dispersed charged scatterers that caused our low mobility, we

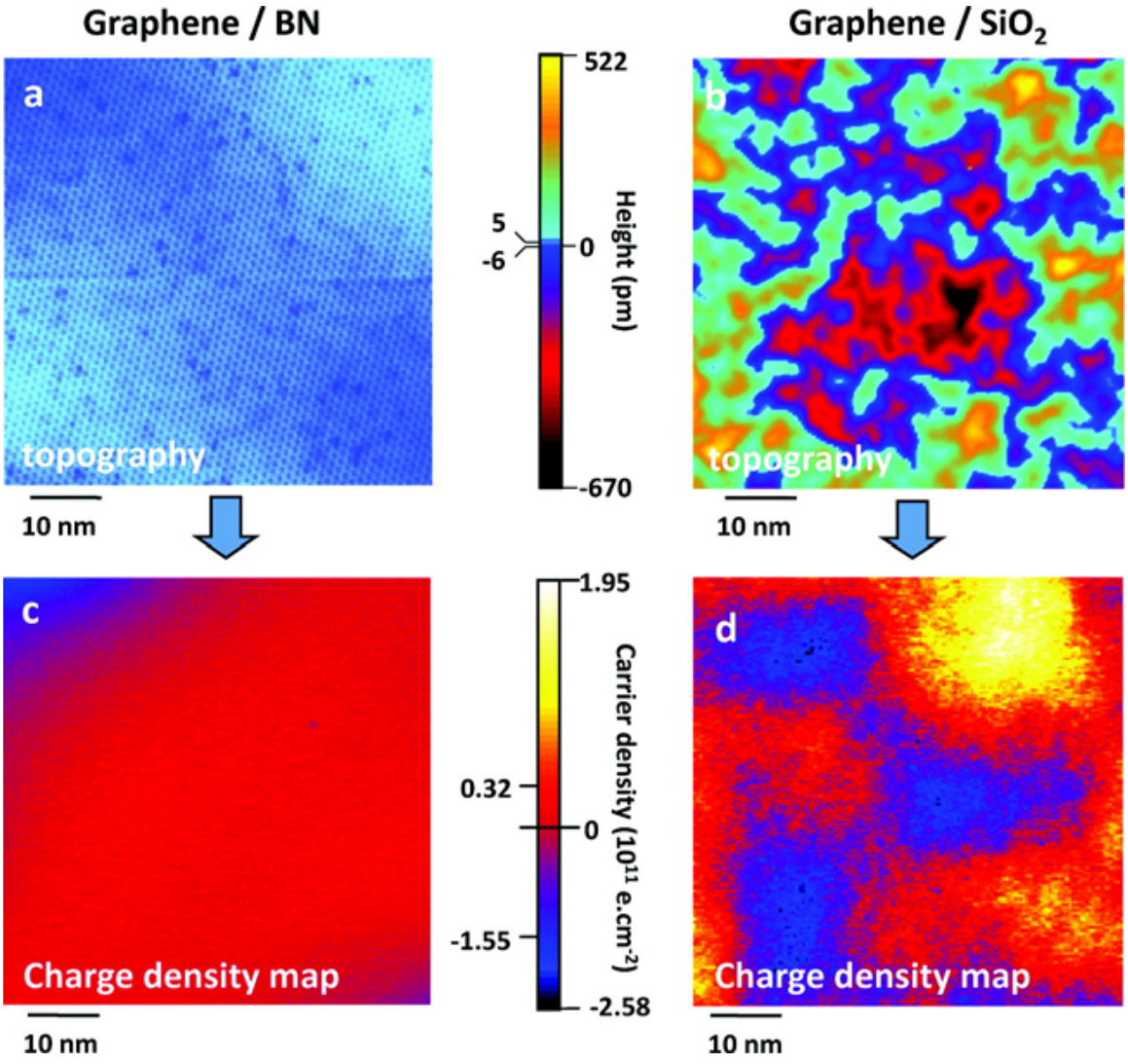

Figure 4.18: STM data from CVD graphene on hBN (a & c) and SiO_2 (b & d) taken by Decker et al. [65]. Note that on hBN, the topography is 100× flatter (a & b) and the charge density fluctuations are 2.5× smaller (c & d).

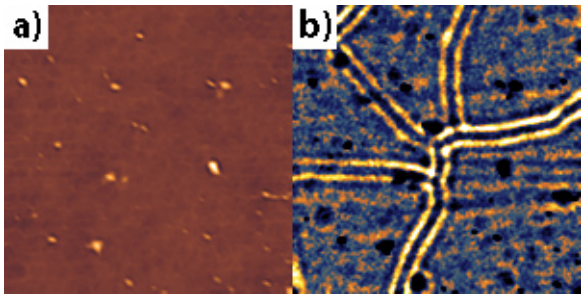

Figure 4.19: (a) AFM topography and (b) scanning plasmon interferometry of CVD graphene. (No scale provided.) There are lines that appear in the plasmon resonance data that do not appear in the topography at all. Image courtesy Zhe Fei, Basov Research Group, UCSD.

would expect the density of the fluctuations to roughly correspond to the density of scatterers. This did not seem to be the case. The graphene on SiO_2 had fluctuations separated by ∼20 nm, and the graphene on hBN had charge fluctuations further apart than the field of view, significantly larger than 18 nm.

One likely explanation is that while our electronic measurements were performed on samples many microns wide, the STM is looking at a small region of the sample and presumably one selected for its relative cleanliness. While that particular region of graphene on hBN is very clean, the charge fluctuation density may be higher when averaged over many square microns.

These data may not be fair to the true potential of SiO_2 as a graphene substrate. The 1000 pm roughness in particular suggests that either flatter SiO_2 could be used or significant contamination remains that could be prevented. Furthermore, improvements in SiO_2 surface crystallinity or passivation may improve the quality of the graphene-oxide interface and therefore improve carrier mobility.

Similar samples were also used by Yang Wang, a graduate student in the Crommie group, to examine quasiparticle behavior near Coulombic impurities in graphene on hBN [67].

4.11.2 Scanning plasmon resonance

Will Regan and I also fabricated CVD graphene samples on hBN for Zhe Fei, a graduate student in Dimitri Basov's group at UC San Diego. Their group performs near field optical measurements of graphene and related systems [68, 69]. Their technique measures the amount of infrared light reflected off of an AFM tip as it scans back and forth over the graphene. This reflection is dominated by the near field interactions of the tip and the sample, which allows accurate measurement of plasmons within the graphene. Further explanation can be found in [68] and [69].

Zhe Fei had several interesting results from the samples we prepared. The most

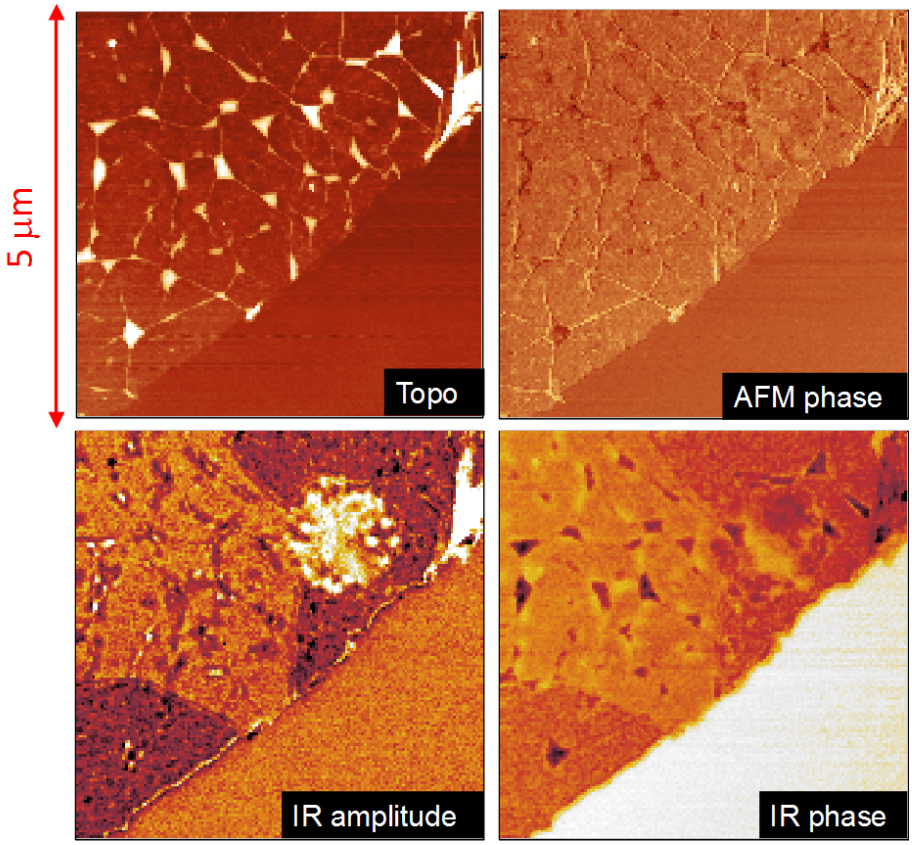

Figure 4.20: AFM and plasmon interferometry of a CVD graphene edge. The topography data clearly shows bulges and folds in the graphene. The IR response, including amplitude and phase, shows different behavior for different regions of the graphene. Image courtesy Zhe Fei, Basov Research Group, UCSD.

interesting was the observation of connected line structures in the plasmon signal from the CVD graphene. These structures were not visible at all in the AFM topography data, but showed up strongly in the plasmon data, as seen in figure 4.19. These data were consistent with grain boundaries in the CVD graphene. While they would be invisible topographically, they could disrupt the motion of carriers in the graphene that are responsible for the plasmonic response. Unfortunately there is not yet any independent confirmation of this. If true, it would potentially represent an easy way to map grain boundaries in graphene devices on substrates, something that is currently difficult to do.

Further plasmon interferometry data show other interesting behaviors. As seen in figure 4.20, certain regions of graphene exhibit different IR amplitudes and phases. The reasons for this are unclear, but different crystal orientations may have different plasmonic responses. The bright regions seen in the IR amplitude data may be due to trapped contaminants under the graphene, possibly from residual etchant.

Chapter 5

Folds in graphene

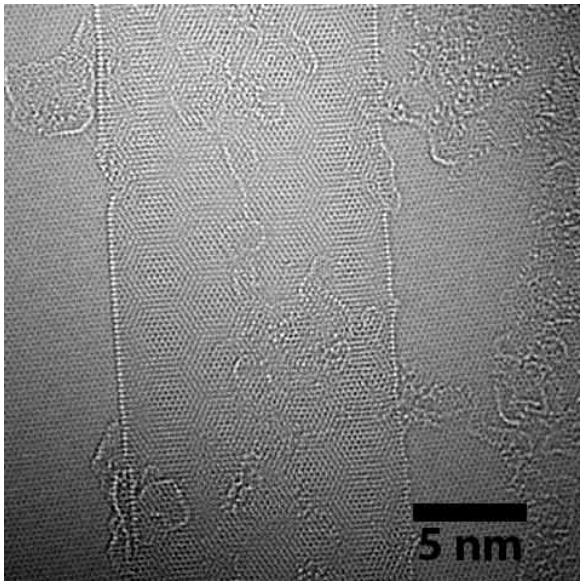

Figure 5.1: Image of fold in graphene taken with the TEAM 0.5 microscope at NCEM. A moiré pattern is visible in the center (trilayer) section. (Image courtesy Kwanpyo Kim [70].)

While preparing devices made from CVD graphene, we repeatedly noticed lines running through the graphene-covered regions that appeared dark in both SEM and optical images. Some such lines are visible in figure 4.4. The distribution and shape of these lines were consistent with folds but we did not investigate initially.

5.1 Microscopy on folds

Shortly thereafter, Kwanpyo Kim, a fellow graduate student in the Zettl group, notified us of transmission electron microscope (TEM) data showing the existence of folded structures in CVD graphene that had been transferred to TEM grids. One such TEM image is seen in figure 5.1. These results prompted further investigation of folds, both in the TEM and on surfaces.

5.1.1 AFM of fold

Benji Alemán, another Zettl group graduate student, and I performed AFM on the dark lines in graphene on flat BN substrates and recorded height profiles consistent with folded structures. One such AFM image appears in figure 5.2. The fold is faintly visible going from the top of the image (off the flake) to the bottom. This was also visible in both the optical microscope and in the SEM.

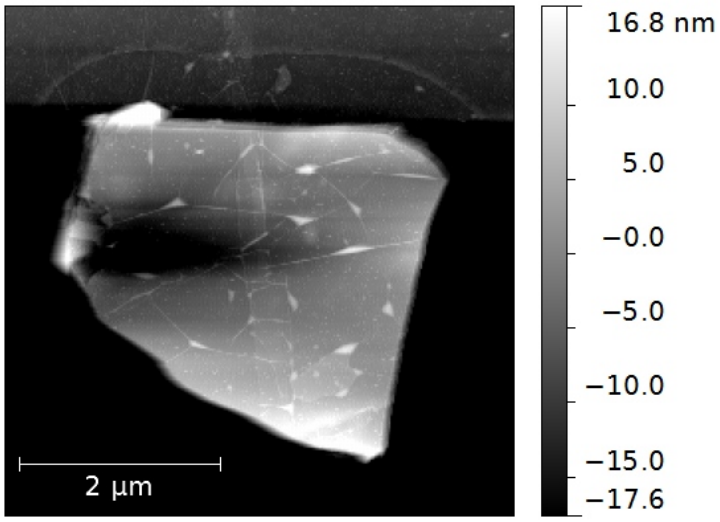

Figure 5.2: Top: AFM image of hBN flake with graphene fold running from top to bottom. The fold is also visible at the top of the image off the flake.

The height profile AFM data shown in figure 5.3 provided a great deal of information. Most prominent are the high peaks at either edge of the fold. This is probably due to the energy of curvature of the graphene. While it is energetically favorable for the graphene to lie flat against itself, this competes with the graphene's energy of curvature. The result is a rounded "bulb" when graphene folds back on itself. This structure is conceptually consistent with theoretical calculations that were performed by Marvin Cohen's group at UC Berkeley [71].

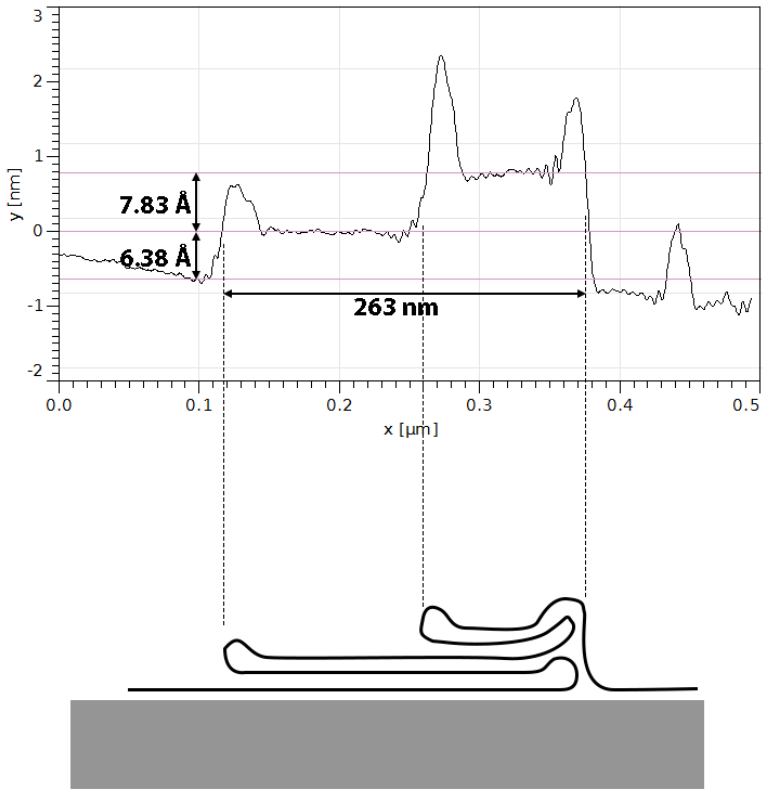

Figure 5.3: AFM data of fold shown in figure 5.2 showing that the first "tier" is 6.38 Å and the second is an additional 7.83 Å. A likely structure is shown below in black on a gray substrate. The profile was an average of 28 adjacent scans in a region of the fold relatively free of contaminants.

Also noticeable is that the fold is more complex than a simple pleat in the graphene sheet. Based on the height profile and an examination of the fold structure along its length, we developed the schematic seen in the bottom half of figure 5.3, a double pleat. (This identification was based on our observation that the top pleat "flops" back to the other side elsewhere on the sample.) Thus there were 3 distinct regions: a monolayer, a trilayer, and a pentalayer of graphene.

This complex fold structure gave the fold two different step heights. The first, going from the monolayer to the trilayer region, we measured a step height of 6.38 Å. This was close to the 6.7 Å that we would expect for the height of two layers of graphene. The second step, from the trilayer to pentalayer, was 7.83 Å, slightly larger than the bilayer step height. This was not surprising, since any trapped contaminants would increase the apparent height of the fold. Such contaminants on folds were later observed by Kwanpyo Kim.

5.1.2 TEM analysis of folds

By taking selected area diffraction data at a number of positions across a fold, Kwanpyo was able to confirm that the fold was an "S"-shaped "pleat" in the graphene sheet. The total diffracted intensity was three times higher in the middle of the fold than to the side of it. In addition, in the center there were three distinct sets of diffraction spots. Two were very close together, indicating that the two folds that made up the pleat were very near parallel. The third orientation was in the middle of the "S" and was a reflection of the graphene lattice over the symmetry vector of the fold.

Based on these observations, we realized that there were an enormous variety of possible fold structures, with different fold angles and crystal directions and stacking alignments. Some possible fold structures are shown in figure 5.5.

Theoretical electronic structure calculations were performed on a number of fold structures, but general conclusions were difficult due to the large unit cells of many folds. More details on the theoretical calculations appear in our paper, published in Physical Review B [70]. The folds that had band structures calculated were semimetallic; the valence and conduction bands shifted to overlap in the vicinity of the fold.

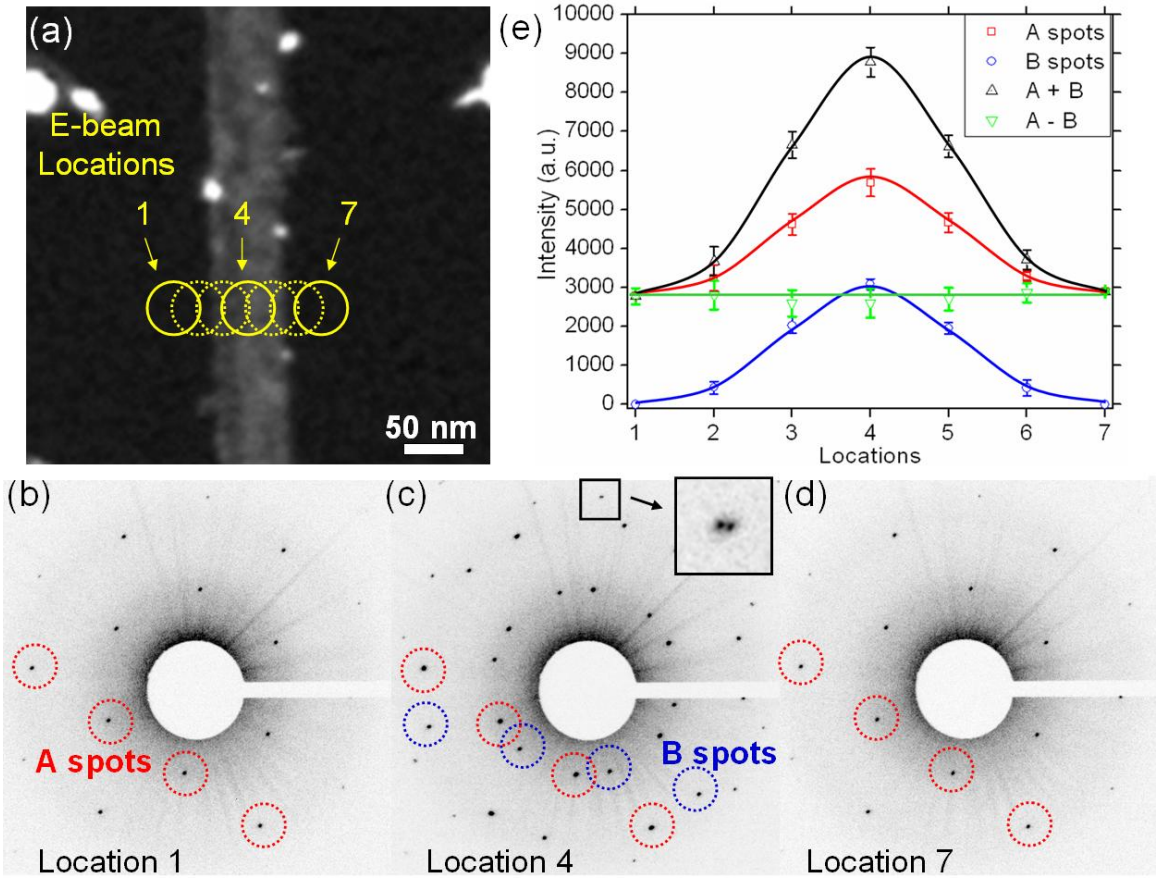

Figure 5.4: Analysis of graphene folds in TEM, from [70]. (a) Dark field image and the position of the seven beam spot locations. (b)(c)(d) Diffraction patterns at spot positions 1, 4, and 7 respectively. Note the presence of a different diffraction pattern (the "B" spots) at position 4. (e) Intensity of the "A" and "B" spots at each of the 7 positions. The twofold increase in the "A" spots at position 4 and the threefold increase in the total diffraction is consistent with an "S"-shaped fold in the graphene sheet.

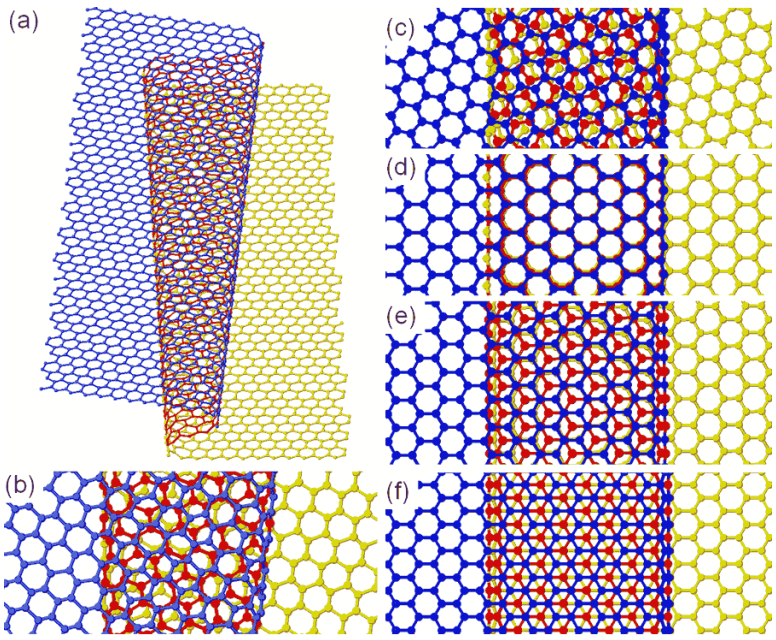

Figure 5.5: Rendered image of possible fold structures, courtesy Kwanpyo Kim. Top layers are blue, middle layers red, bottom layers yellow. (a)(b) Two folds with edges not parallel, showing a difference in the orientation of the blue and yellow regions. (c) A fold with parallel edges but at an angle relative to the graphene lattice. (d)(e)(f) Folds with symmetry vectors parallel to the zig-zag direction in graphene but with three different interlayer stackings.

5.2 Transport data

To learn more about the folds, we wanted to perform transport measurements. Given a simple "S" fold through a sheet of graphene there are two distinct ways of fabricating a device. These are both shown in figure 5.6 and ignore the crystal orientation of the graphene. Figure 5.6a shows a "parallel" fold geometry, where the direction of symmetry of the fold is parallel to the direction of the current. Figure 5.6b shows a "perpendicular" fold, where the direction of symmetry is perpendicular to the current. These two geometries likely have distinct transport properties in different magnetic field, temperature, and/or gating regimes.

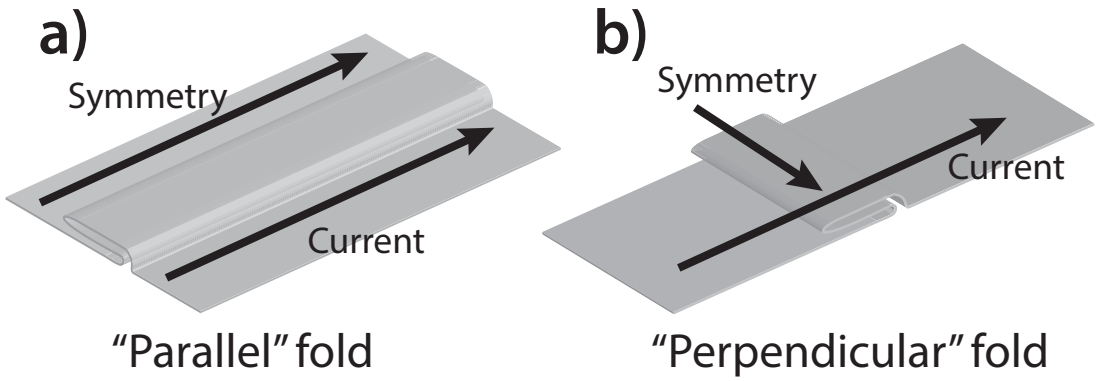

Figure 5.6: Schematics of fold device geometries. (a) "Parallel" devices have symmetry vectors parallel to the current that flows through them. (b) "Perpendicular" devices have symmetry vectors perpendicular to the current.

We fabricated a variety of devices with four probe configurations, 18 of which were measurable. They all had conduction channels 5 µm long and 1 µm wide. Some representative data appear in figure 5.7 for two devices, F42 and F75, which were perpendicular and parallel folds on SiO_2, respectively. They look fairly similar, although F75 has a higher slope and a higher minimum conductivity. The locations of the conductivity minima are slightly different, but both were typical for this family of devices.

Several devices, including F24, exhibited oscillations in their conductance when measured at low temperature. The origin of these oscillations is unknown. Some data showing this phenomenon appears in figure 5.8.

Twelve of the devices were perpendicular folds on SiO_2, three were perpendicular on hBN, one was parallel on SiO_2, one was parallel on hBN, and one control device had no fold at all. (This was clearly not an optimum distribution for a comparison of all of the sets.) A summary of the conductivity minima as measured at 4.2 K appears in table 5.1.

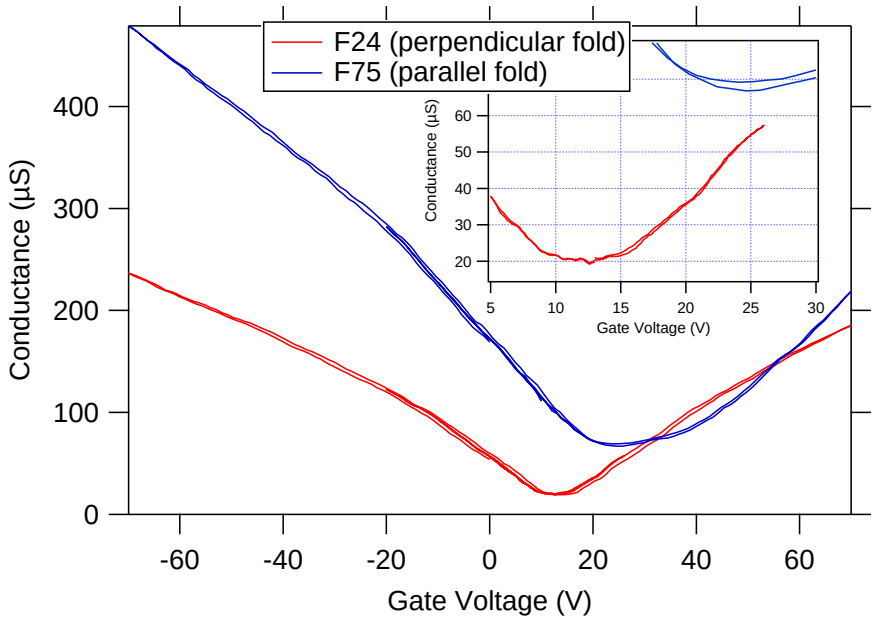

Figure 5.7: Conductance vs gate voltage for two different fold devices at 4.2 K. A perpendicular device (F24) is shown in red, and a parallel device (F75) in blue.

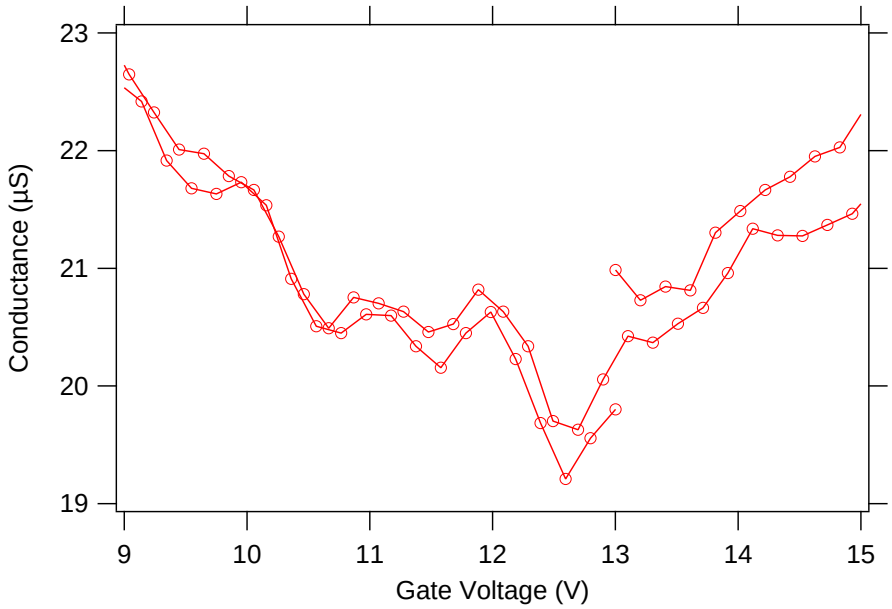

Figure 5.8: Magnification of conductance data of F24, which showed oscillations near its conductance minimum at 4.2 K.

Fold	Substrate	N	Cond. min.	
Parallel	BN	1	21	µS
Parallel	SiO_2	1	67	µS
Perp.	BN	3	30 ± 19	µS
Perp.	SiO_2	12	22 ± 5	µS
None	SiO_2	1	17	µS

Table 5.1: Conductivity minima for fold devices on hBN and SiO_2 at 4.2 K

There are not enough devices for statistics on the parallel folds or the control device. They are both consistent with the measurements made on the perpendicular folds on SiO_2, as are the perpendicular devices on BN. There is only one parallel fold device on SiO_2, but it is definitely not consistent with the perpendicular devices on SiO_2, and in fact differs by over 9 standard deviations. Since the difference in fold orientation is the only non-random difference between the samples, it seems probable that the presence of the fold affects the minimum conductivity.

This is consistent with a simple model of the sample's behavior. The parallel fold geometry is in some ways equivalent to a device made of bare graphene with an additional strip of graphene in parallel. Because of screening effects, this additional strip may be more difficult to gate than the rest of the graphene. In this way, you would expect parallel devices to have higher minimum conductivities and wider conductivity minima due to screening effects.

5.3 Fold ideas

There are still many fold-related experiments that we were unable to perform that may be a rich source of interesting physics.

We were able to show some intercalation of folds. Benji Alemán put a crystal of purified C_{60} in a sealed ampule with some graphene folds on a TEM grid, heated it up to allow vapor transport of the C_{60} molecules, cooled, and rinsed the grids with toluene to wash away excess C_{60}. He was able to identify a line of C_{60} molecules that had filled a single fold. A TEM image and schematic are shown in figure 5.9

While C_{60} in a graphene fold may not be as rich a system as other intercalant systems, it is a preliminary demonstration of what may be possible. Intercalant chains down the length of folds could act as conducting channels and be measured in parallel with graphene. Intercalants that made graphene insulating would be very interesting to measure in perpendicular devices, as they would strongly affect the overall conductance because the fold is in series with the rest of the graphene.

In addition to the chemistry of intercalation, the folds may have other interesting chemical properties. It is known that graphene's chemical reactivity can increase greatly when strained [72, 73]. Because extended folds give the graphene a strain

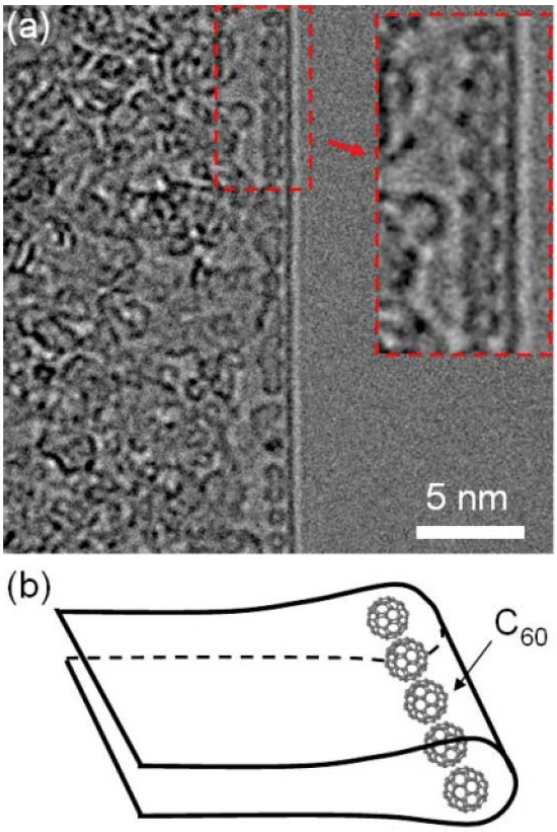

Figure 5.9: (a) TEM image of a singly folded graphene edge showing likely filling by C_{60}. (b) Schematic of such a fold filled with C_{60}. From [70]

field with long range translational symmetry, they may present a route to patterning functionalized structures over long ranges in graphene.

The increased chemical reactivity at fold edges combined with the right processing could create aligned rows of coupled nanoparticles many microns long. Chemical functionalizations of folds that open a bandgap could allow fabrication of isolated nanoribbons within graphene sheets. The use of folds for such engineering may prove to be an important technique in the graphene researcher's toolbox.

Chapter 6

Graphene fluorination

6.1 Introduction to fluorination

Graphene's band structure near the Dirac point gives it many interesting properties. For example, its lack of bandgap allows the charge carriers to be changed from p-type to n-type by modest electrostatic gating, and their concentration to be tuned continuously. However, this same zero-gap band structure severely limits the performance of graphene field effect transistors (FETs).

For silicon field effect transistors in their off state, the doped silicon conduction channel's Fermi level lies in the bandgap of the silicon. This greatly limits the off-state leakage current, which is necessary if the transistors are to have gain and not dissipate excessive power in their off state.

In graphene FETs, the off-state will have its lowest current when the Fermi channel lies, on average, at the charge neutrality point. However, even though the density of states is zero at graphene's Dirac point, the conductivity minimum never goes below $\sim e^2/h$ due to charge density fluctuations from the substrate or other contaminants [74]. This off-state current limits the on-off ratio of the transistor to much lower values than silicon FETs, typically $\sim$10 to 50 for our devices.

Overcoming this lack of bandgap and making transistors with higher on-off ratios has long been a goal of graphene researchers [75]. There have been several techniques proposed, including chemically functionalizing the graphene and narrowing the graphene channel width to form a nanoribbon, both of which have been predicted to open bandgaps in graphene [76, 77].

However, graphene fully functionalized with fluorine does not make the best transistor material. Studies have calculated the bandgaps of well-ordered graphene fluorides to be between 3 and 8 eV at high fluorine concentrations, too large for a transistor [78–82]. Theoretical calculations have shown smaller bandgaps for stoichiometries with less fluorine, but these may be much harder to make experimentally [77]. These calculations are consistent with experimental data [83, 84].

Fluorination may still have an interesting role to play in electronic devices. Re-

search done by Robinson et al. [77] at the Naval Research Laboratory showed that while fluorination of graphene eliminates its optical contrast on silicon, it did not seem to affect layers below the top layer. Presumably the top layer became fluorinated and acted as a passivation layer, preventing fluorination of those below, which retained their optical contrast and, presumably, electronic properties. This presented us with an interesting route to electronically investigate folds in graphene.

6.2 Grafold fluoride

Long parallel folds running through graphene sheets on substrates were first explored in depth by the Zettl group in 2011 [70]. Preliminary calculations performed by Marvin Cohen's group at UC Berkeley in the same paper showed that at least some of the folds had semimetallic band structures, but a full catalog of electronic properties for different chiralities had not yet been completed. Further information on graphene folds and some transport data through fold devices are covered in chapter 5.

This sparked discussion of how to properly isolate these structures for transport measurements. As fabricated, the folds were surrounded by graphene, which itself dominated the transport in the system. One possible technique was to destroy the conductivity in the outer layers of graphene by either plasma etching, functionalization, or complete graphene removal. We attempted plasma etching, which consistently damaged or destroyed all of the graphene. We also tried a technique reported by James Tour's group at Rice University wherein zinc was sputtered onto graphene and subsequently etched away, which removed the outermost graphene layer as well [85]. However, we were never able to successfully sputter zinc with equipment in the Zettl group.

At the time we did not have experience with graphene functionalization beyond simple oxidation [41]. However, there were a number of papers suggesting that fluorination with XeF_2 was simple and could provide the loss of conductivity we desired [77, 79]. While we did not have our own fluorination system, the XACTIX Xetch system in the Berkeley NanoLab was available. The specifics of the fluorination will be discussed more in section 6.5.

A schematic of a pristine fold in graphene is shown in figure 6.1a. Figure 6.1b shows the same fold post-fluorination, assuming that only the outer layer becomes fluorinated. The inner layers of the fold are preserved and ideally maintain their electronic properties.

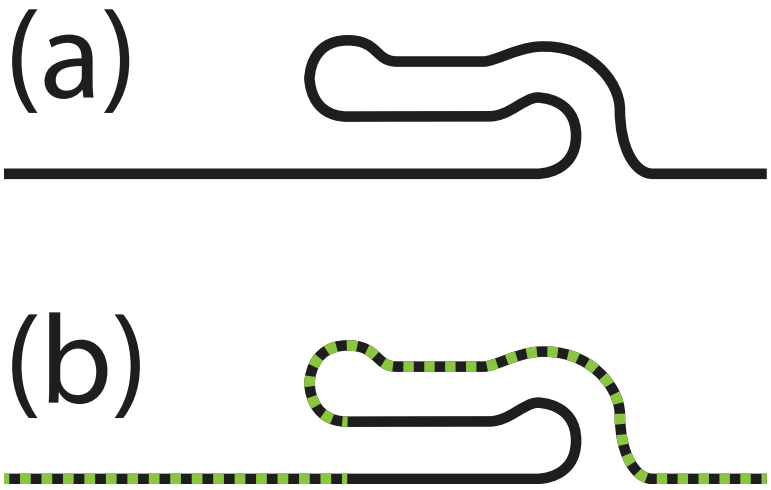

Figure 6.1: Schematics of (a) a cross section of a folded section of graphene and (b) the same region after fluorination. The fluorine is unable to penetrate the outer fluorinated layer, preserving the graphene within.

6.3 Fluorination background

6.3.1 Fluorination theory

There are several possible effects that happen as xenon difluoride reacts and the fluorine forms covalent bonds with otherwise pristine graphene. At low concentrations of fluorine, its high electronegativity will attract free electrons from the graphene and thus hole dope the sample. At higher concentrations, this doping will continue, but the charged fluorine groups and associated lattice distortions will become the dominant source of scattering in the sample, reducing carrier mobility [86].

At very high concentrations, there are two possible results, depending on the amount of introduced disorder. One is that there will be a transition from graphene to graphene fluoride, with the unfunctionalized carbon atoms behaving as defects within the otherwise well-ordered graphene fluoride crystal, which will have its own electronic properties.

The other possibility is that the fluorination will introduce substantial disorder to the system. This disorder could arise as sp^2 bonds become sp^3 from the functionalization, straining the graphene and forcing it to rearrange its in-plane bonds. It could also arise from the fluorine reacting in different ways with the graphene grain boundaries, defects, substrate, or contaminants, such that the basal graphene structure is irreversibly damaged.

Either of these outcomes would be compatible with our experiment, since either would eliminate the outer graphene's conductivity.

6.3.2 Previous fluorination experiments

While graphene research has been growing since 2006, fluorinated graphene remained largely unresearched until around 2010. The first experimental result in a transport-compatible configuration was in 2010 by Cheng et al. [87], which produced graphite fluoride by reaction of highly ordered pyrolytic graphite (HOPG) with 1 atm F_2 gas at 600°C for more than 36 hours. They then exfoliated the resulting material onto SiO_2 substrates to produce monolayers and multilayers and to deposit contacts. Their transport data showed a high degree of disorder, and they were unable to measure any effects from the graphene fluoride band. Instead, they measured variable range hopping transport, perhaps between fluorinated and unfluorinated regions [87].

Later in 2010, researchers at the Naval Research Laboratory published the first paper using XeF_2 as the fluorinating agent for graphene [77]. They used graphene grown with known CVD methods on copper foil, fabricated graphene FETs, and measured them before and after fluorination. Additionally, they measured them after defluorination with hydrazine, but this is less relevant to our research. They call the fluorinated sheets "perfluorographane" after the term "perfluoroalkanes," alkanes where every hydrogen has been replaced with a fluorine.

Robinson et al. [77] produced a number of results relevant to our research. First, their optical characterization showed that fluorinated monolayer regions lost their optical contrast against the SiO_2, presumably from a large change in the dielectric constant. Bilayer and multilayer regions, however, retained their contrast, suggesting that the XeF_2 is unable to penetrate the outer layers.

The transport measurements by Robinson et al. on graphene and fluorographene FETs left something to be desired. They only measured their samples in air at room temperature after various amounts of fluorination. Any information about air sensitivity or temperature dependence was not explored. While they claimed their samples do not react with air, they had no evidence that such reactions were not occurring prior to their initial measurements. They measured a greater than 1000-fold increase in the sheet resistance after 120 seconds of XeF_2 exposure, but after 240 seconds, the resistance was greater than the range of their parametric analyzer.

The same group later published a subsequent paper using polymer nanowires as masks for fluorination of graphene [88]. Two other papers to note are by Withers et al. [89] and by Nair et al. [79], which both report similar results using F_2-fluorinated graphite and XeF_2-fluorinated exfoliated monolayers, respectively. The paper by Nair et al. [79], in particular, has temperature dependent transport data with a nice analysis of the variable range hopping.

The transitions between different transport regimes as graphene is progressively more fluorinated were observed by [90]. Interesting magnetoresistance effects have been observed in fluorinated graphene as well [91].

Some research has been done on graphene fluorination using plasmas [92–94], but our attempts to do so resulted in destruction of the graphene.

6.4 Device fabrication

The first generation of graphene fold devices destined for fluorination were designed the same as our graphene FETs mentioned in chapter 4, except instead of selecting the cleanest region of the graphene we chose to align the devices to folds in the graphene. These folds are easily observed in the SEM as a web of dark lines. The devices were also made only on SiO_2 substrates rather than a mix of SiO_2 and BN. The graphene was grown in the Zettl group CVD furnace using techniques explained in section 3.2 and was transferred to precleaned substrates with alignment marks.

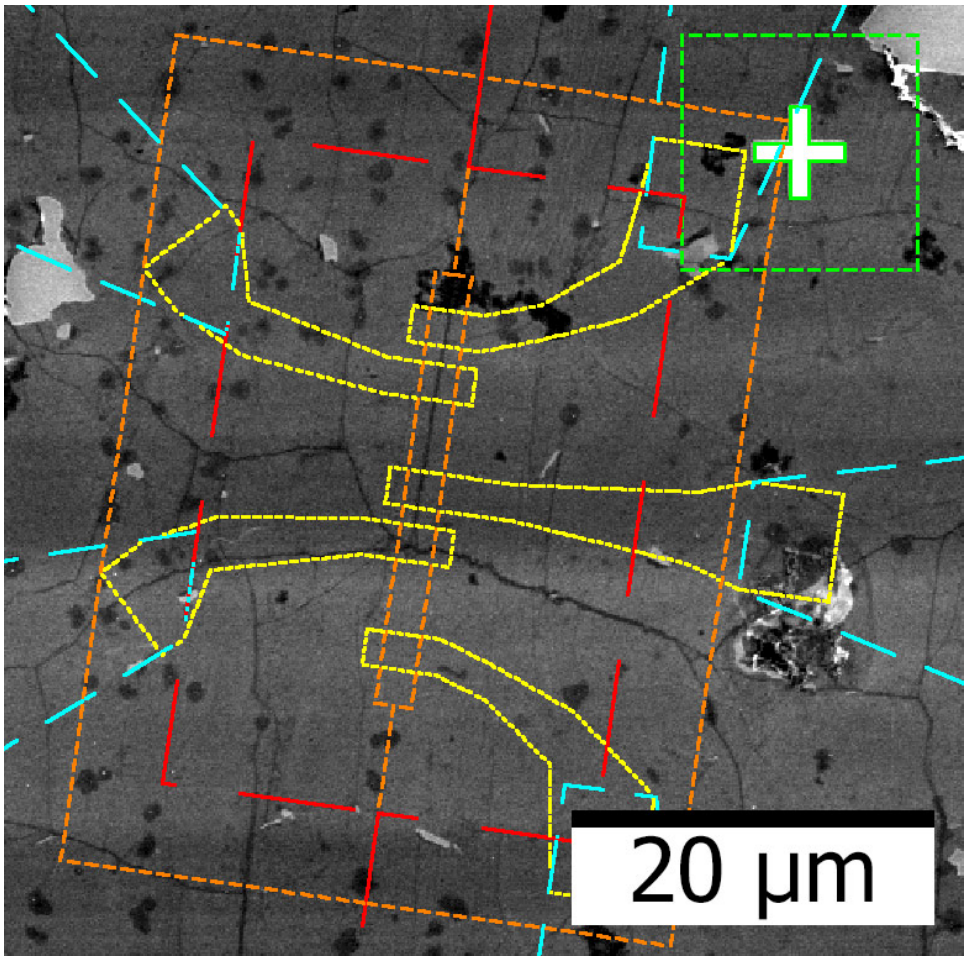

Figure 6.2: SEM map image of graphene fold device "GfoldB25" with overlay from the CAD software. Orange and red are etch masks, blue and yellow are contact masks, and green is for alignment. Folds are visible as dark lines in the graphene.

A mapping image with a CAD overlay of one such device appears in figure 6.2. The fold being contacted in that device runs approximately top-to-bottom in the image. The different colors reflect different layers in the CAD file, for writing the

etch mask (orange and red), for writing the contact mask (yellow and blue), and for alignment (green). The contacts were designed to allow four-probe measurement of the fold device with an additional contact to allow measurement of the bare graphene pre- and post-fluorination, seen here towards the bottom. The active regions of both the fold and bare graphene devices are 4 µm long and 2 µm wide.

6.5 Experimental design I: folds on SiO_2

The devices with the most successful data collection were from a chip called "GfoldB" and numbered 34, 44, and 45. These are referred to as B34, B44, and B45 for the rest of the chapter, and are the focus of the next several sections.

The electrode and etch design of these devices were identical to that shown in figure 6.2, allowing for 4-probe measurement of the fold and simultaneous monitoring of the bare graphene region. The graphene was etched as described in section 4.2.1, and the contacts were 5 nm Cr and 45.5 nm Au deposited in the Zettl group thermal evaporator. After fabrication but before electronic measurement, we measured the widths of each fold using atomic force microscopy (AFM).

AFM data for device B34 is shown in figure 6.3. The entire image is within the graphene area, and the fold is shown as the raised stripe in the center. Contamination was readily apparent in the form of bumps on the surface. The nature of this contamination was not known, but we suspected it was polymer residue, perhaps crosslinked from exposure to the persulfate used in the copper etching.

Based on this AFM data, we determined that device B34 had an average fold width of 108 nm with a standard deviation of 4 nm. Determination of the step height was very difficult due to the amount of contamination on the fold surface, but the mean height of the fold region was approximately 1.9 nm higher than the mean height of the graphene, with respective RMS roughness values of 1.3 nm and 1.5 nm.

This is significantly larger than the 0.7 nm expected for a simple, fully closed pleat. If the PMMA contamination adsorbed onto the exteriors of the graphene and fold identically, this would add the same quantity to both mean heights and thus should not contribute to the step height. If PMMA or other contamination were in the fold, it would make the fold thicker. Furthermore, there could also be tensioning effects that cause the fold to not sit completely flat on the surface.

6.5.1 XeF_2 system

After AFM characterization it was time to fluorinate the fold in a xenon difluoride atmosphere.

The XACTIX Xetch is a commercial XeF_2 system used mostly for dry etching silicon. This is particularly useful for underetching structures for nanoelectromechanical systems (NEMS). The principle of operation is simple. Xenon difluoride has a vapor

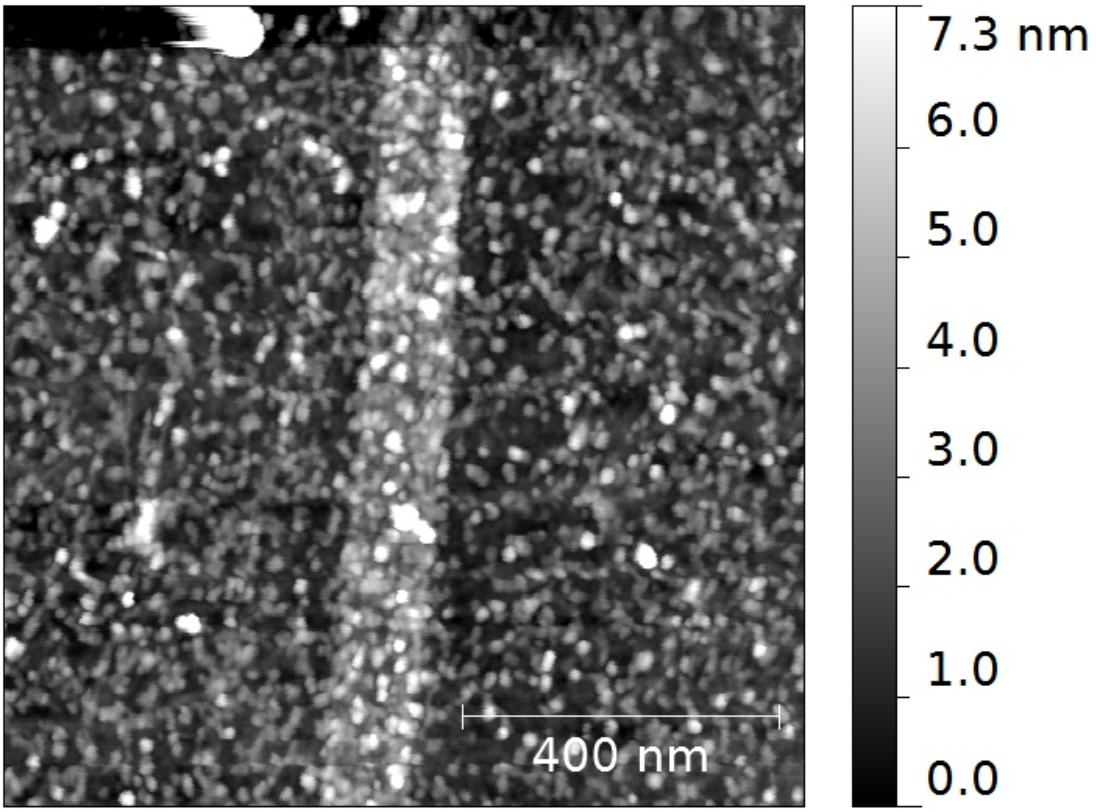

Figure 6.3: AFM image of a section of device "GfoldB34", used in fluorination experiments. The lighter region in the center is the fold and is ∼150 nm wide. The bumps in the image are contamination, possibly PMMA residue.

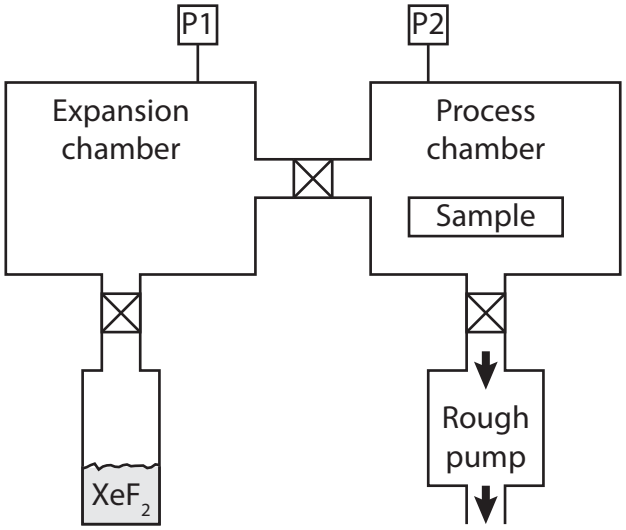

Figure 6.4: Simplified schematic of Xetch XeF_2 etching system. P1 and P2 are pressure gauges on the expansion and process chambers, respectively.

pressure of a few torr at room temperature. A container of XeF_2 is connected to an expansion chamber by a gate valve. This valve is opened until the XeF_2 pressure in the expansion chamber rises to the programmed setpoint. At this time, the XeF_2 valve is closed and a valve to the process chamber opens, allowing XeF_2 to diffuse to the sample. This continues for a programmed length of time, after which the gate valve to the pump opens, removing XeF_2 and etch products from both the expansion and process chambers. The process then ends or repeats as programmed.

Because it is designed for silicon etching and not light graphene exposure, the Xetch system has some quirks that introduce difficulties to our sensitive XeF_2 exposure process. This includes pumping the expansion chamber through the process chamber, potentially exposing the sample to extra XeF_2, as discussed below.

6.5.2 Fluorination of devices

Device B34 was used for a simple experiment: after a few fluorinations, could we distinguish between a device with a fold and a device without? The device went through four fluorination cycles, each with setpoints of 1 torr and 1 second.

However, due to the design of the Xetch, this did not mean the sample was exposed to 1 torr of XeF_2 for 1 second. Rather, for each cycle, the Xetch filled the expansion chamber with 1 torr of XeF_2 and then opened the valve between the expansion and process chambers. It then waited one second before opening the gate valve to the pump on both the process and expansion chamber. During the 1 second wait, the measured pressure in the process chamber rarely went above 0.1 torr. It is not known

if this was due to limited diffusion of the gas or a slow gauge response, but the exact process pressure during these runs remained a mystery.

This uncertainty was compounded by the pumping phase. After the Xetch opened the gate valve to the pump, it took about 30 seconds to pump the two chambers down to 0.0 torr. During this time, some degree of XeF_2 exposure was likely, although the only measurement available was the 0.0 torr measured in the process chamber.

Devices B44 and B45 were fluorinated on a similar schedule, with the Xetch set to 1 sec and 1 torr, although 17 cycles in total were completed. Because the silicon chip was not diced, B44 and B45 remained attached to one another, and we were able to study device variability with identical XeF_2 exposures.

6.6 Data I

The conductance data was collected using a setup very similar to that in chapter 4, using a Keithley sourcemeter to sweep the gate voltage while a lock-in amplifier measured the conductance.

6.6.1 Signature of bilayer fold isolation in B34

Figure 6.5 shows conductance data for the separate fold and graphene sides of the device over several fluorinations. The as-fabricated device is shown in red, and subsequent fluorination cycles are shown sequentially in orange, green, blue, and purple. The dashed lines are data from the bare graphene half of the device, and the solid lines are the data from the fold half. Figure 6.5(a) shows the data with a linear scale, and figure 6.5(b) shows the same data with a logarithmic conductance axis to enhance the detail at lower conductances.

The fold and bare graphene regions appeared very similar in the first four data sets. As the devices were fluorinated, the curves shifted to the right, consistent with the fluorine hole-doping the graphene. The data from the fold exhibited deviations from the usual v-shaped conductance. It was initially speculated that these could be due to differential fluorination of the fold surface, as large regions with different charge neutrality points connected in parallel can result in such wide curves. However, the most prominent deviations are in the first (red) data set, before any XeF_2 exposure, making this explanation insufficient.

The fourth fluorination, shown in purple, was a significant deviation from the previous runs. The bare graphene device showed a drop in conductance at the charge neutrality point from 100 µS to less than 0.5 µS, while the otherwise identical fold device had a drop from 100 µS to about 17 µS. These represent a fall in conductance from the initial device by a factor of 200 and a factor of 6, respectively.

The conductances and Dirac point voltages of device B34 over the four fluorinations are summarized in figure 6.6. The data show that the fold and bare graphene

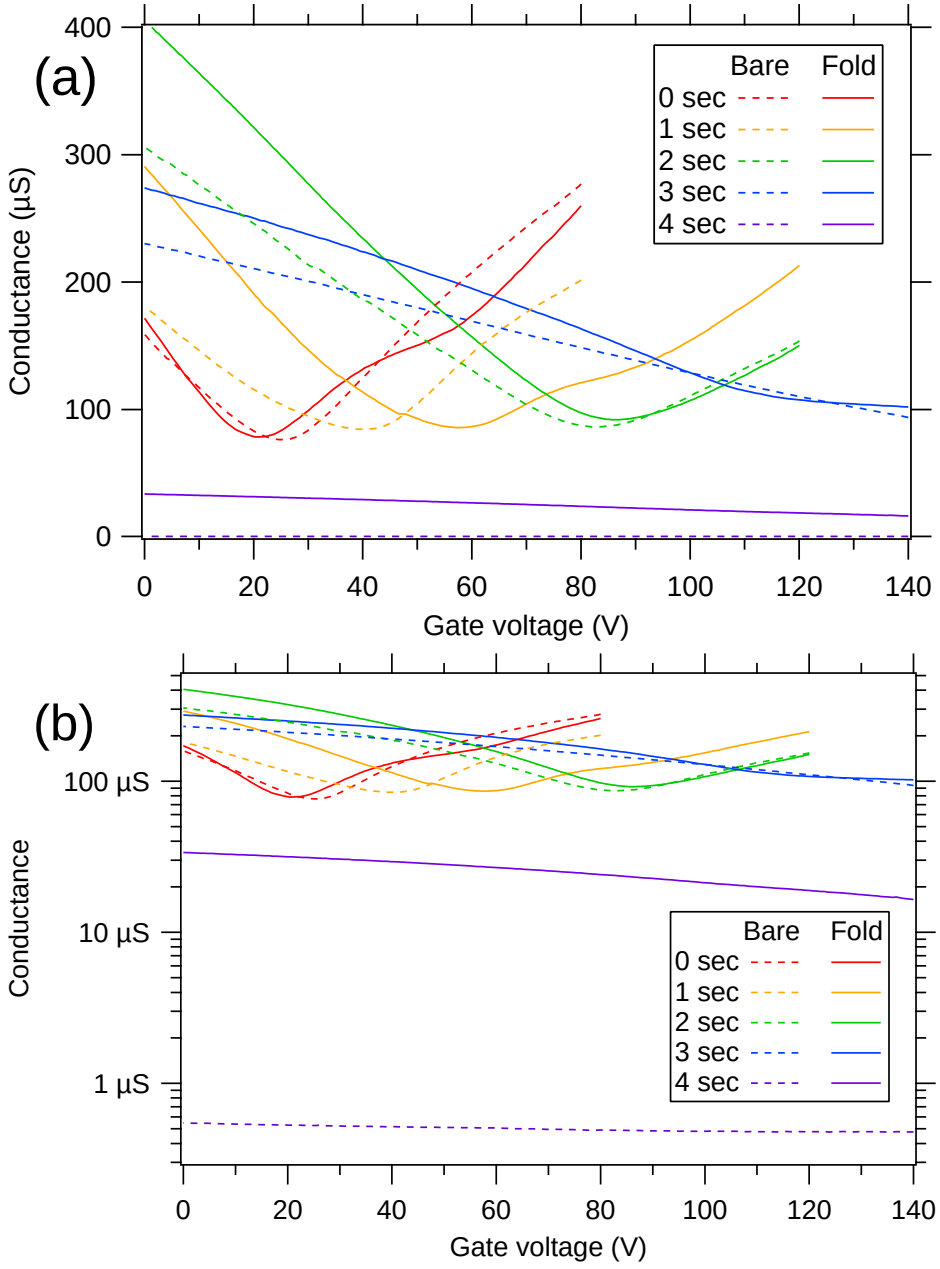

Figure 6.5: Conductance in device B34 before and after several fluorinations for both a folded region and a region of bare graphene. (a) shows the data with a linear scale, and (b) shows the same data with a logarithmic vertical axis.

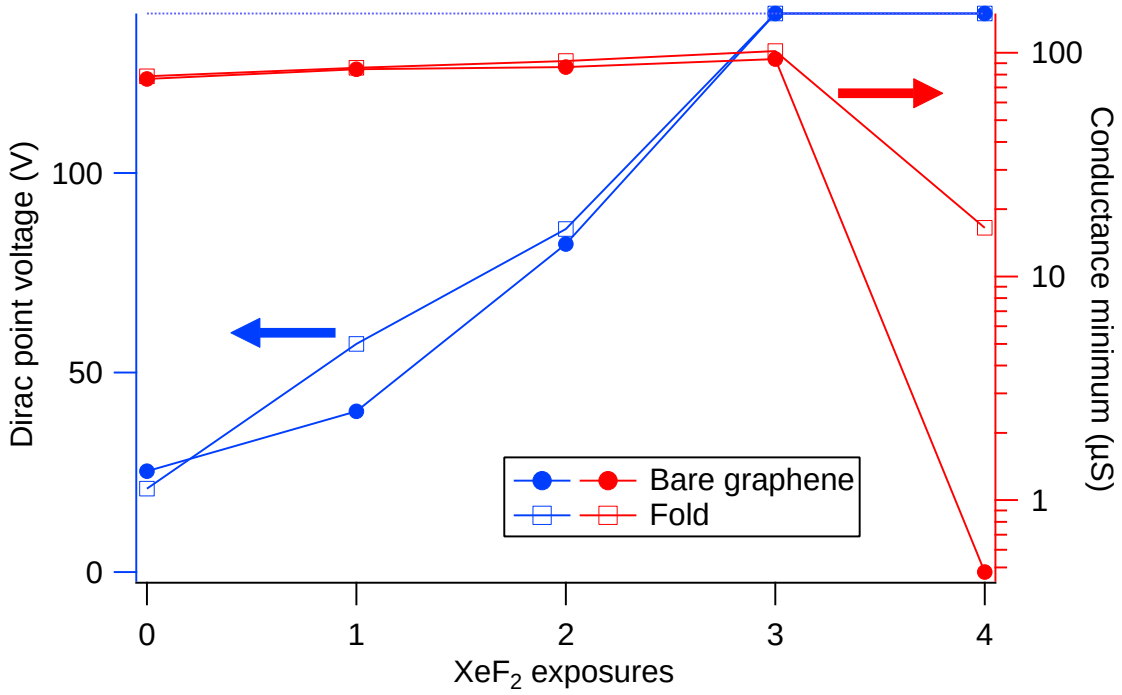

Figure 6.6: Plot of conductivity minima (right axis, red) and their respective voltages (left axis, blue) of device B34 before and after successive fluorinations for both the fold and for the bare graphene. The blue dotted line at top indicates the maximum voltage range measured; points on this line have unknown voltages of at least 140 V.

devices are very similar in terms of their conductance minima and voltages until the fourth XeF_2 exposure, after which the conductance minima diverge. This is consistent with the graphene in both devices becoming insulating due to fluorination, while the inner parts of the fold are protected from fluorination.

6.6.2 Further fluorination of B44 and B45

Due to the large number of fluorinations for devices B44 and B45, it is not possible to show all of the fluorination data on one graph. Instead, figure 6.7 shows the gated conductance of device B44 before fluorination, after 1 cycle of XeF_2, and after 17 cycles of XeF_2. It was initially surprising that the conductivity of the device after 17 cycles was higher than after one cycle, but this is consistent with the XeF_2 doping the sample without introducing further disorder. The corresponding plot for device B45 is similar to figure 6.7 and is shown in figure 6.8.

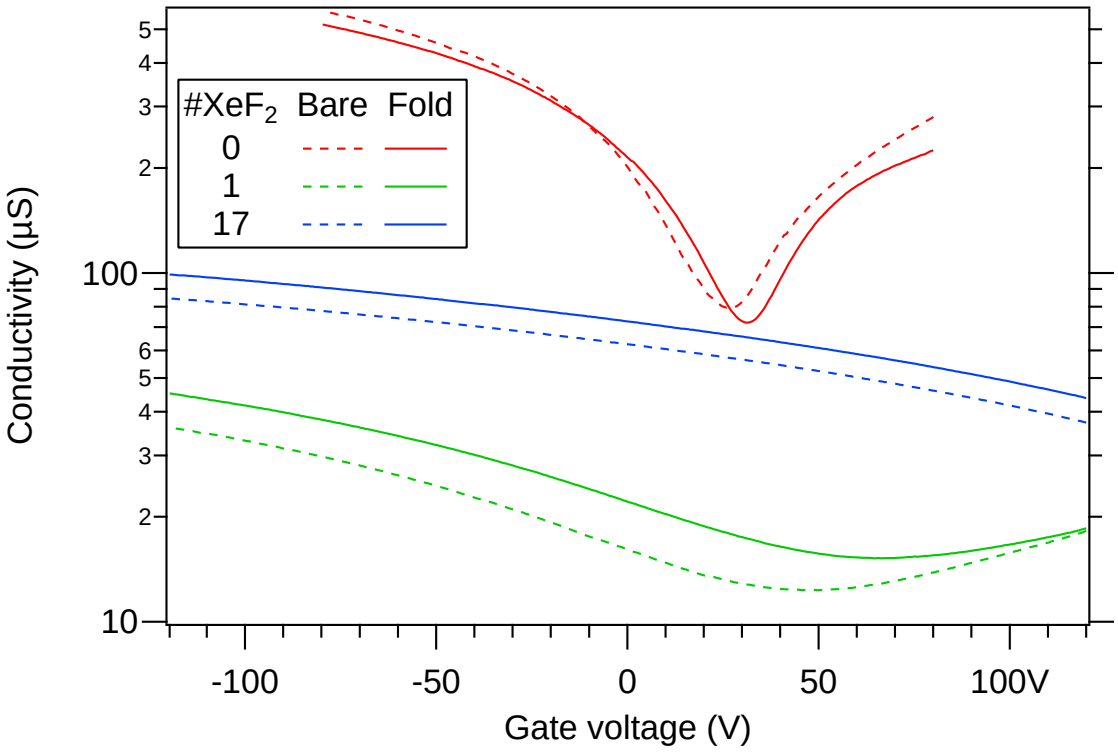

Figure 6.7: Gated conductance of device B44 at three different times: before XeF_2 exposure, after one exposure, and after 17 exposures. The graphene fold is shown with a solid line and the bare graphene is shown dashed. Data shown are gate sweeps from positive to negative voltage.

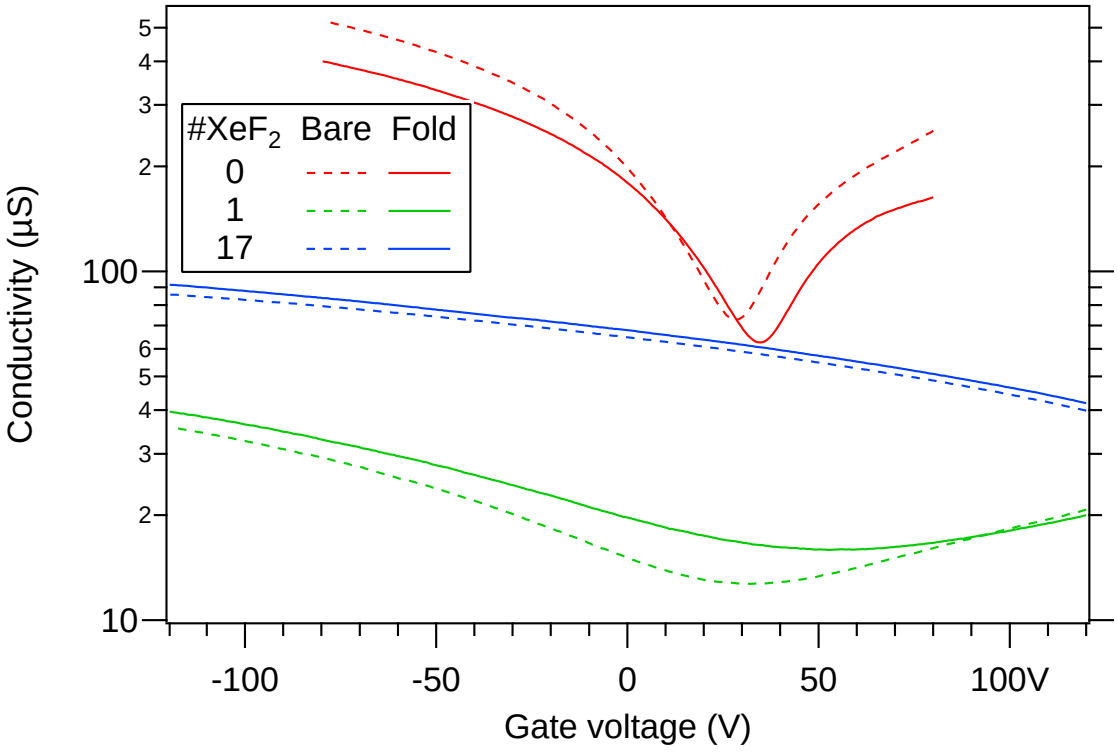

Figure 6.8: Gated conductance of device B45 at three different times: before XeF_2 exposure, after one exposure, and after 17 exposures. The graphene fold is shown with a solid line and the bare graphene is shown dashed. Data shown are gate sweeps from positive to negative voltage.

6.7 Analysis I

Because of the large number of fluorination cycles for devices B44 and B45, it is more illustrative to extract parameters from the curves for comparison rather than show the raw data. In figures 6.9 and 6.10 the conductivities of B44 and B45, respectively, are plotted at three different gate voltages against the number of fluorination cycles. The 0 V data points shown are from the positive-to-negative sweep direction.

In figures 6.9 and 6.10, the conductance of the fold side of the device is consistently higher than that of the bare graphene. Recall that the fold side contains a square of graphene the same size as the bare graphene side, and thus the conductance of the fold side should be approximately the sum of the bare graphene and an isolated bilayer fold. Assuming that the conductance of the graphene portions of each side are identical, we can extract the conductance of the fold by taking the difference of the two sides. These data appear in figures 6.11 and 6.12 for B44 and B45, respectively.

The conductance of the fold as calculated with this method is always positive, which is reassuring. In both devices, the fold conductance tends to increase with XeF_2 exposure, consistent with it becoming more hole doped from the surrounding graphene.

6.8 Experimental design II: in situ measurement and hBN substrates

With devices B34, B44, and B45, we noticed changes in doping depending on whether the data were taken in air or vacuum and how long the samples were in vacuum before measurement. To minimize this uncertainty, all measurements in section 6.6 were taken after samples had been pumping in the vacuum chamber overnight. Our concern regarding this variability was increased when we realized that the measurements of graphene fluorination performed by researchers at NRL were all performed in air [77]. We felt we could improve upon these measurements by measuring our samples in-situ. This would remove the effects of air exposure and allow us to better understand the interaction of the XeF_2 with the graphene.

6.8.1 Xetch electrical feedthrough

To measure the devices in situ, we needed electrical connections between the samples inside the Xetch system and our measurement equipment outside.

The Xetch is a commercial XeF_2 etching system, made for isotropic gas phase etching of silicon. As such, it was not designed with electronic measurements in mind. There were no feedthroughs that were not already occupied and no way to make new ones without cutting into the process chamber. We had three primary ideas of how to get signals through the wall of the process chamber.

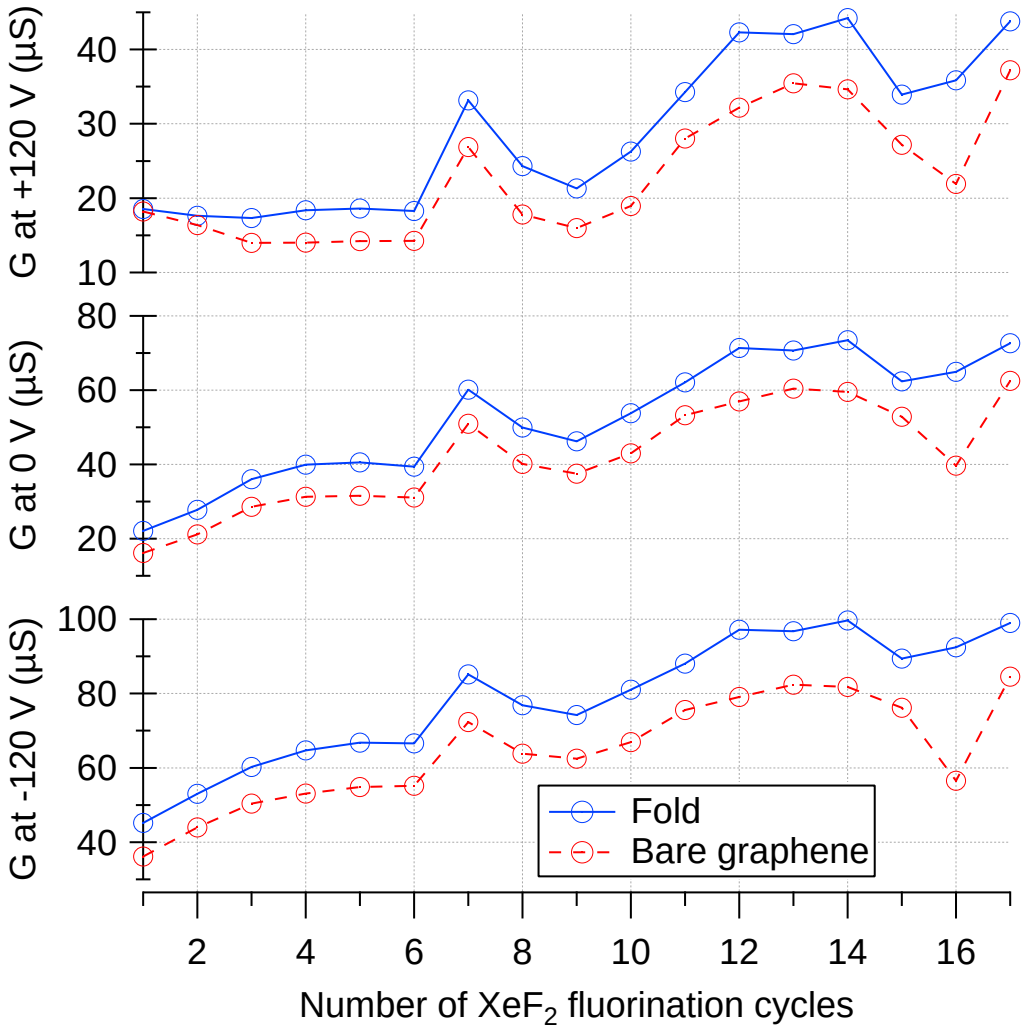

Figure 6.9: Conductance versus fluorination cycle for B44 fold (blue) and bare graphene (red) at gate voltages of +120 V (top), 0 V (middle), and -120 V (bottom).

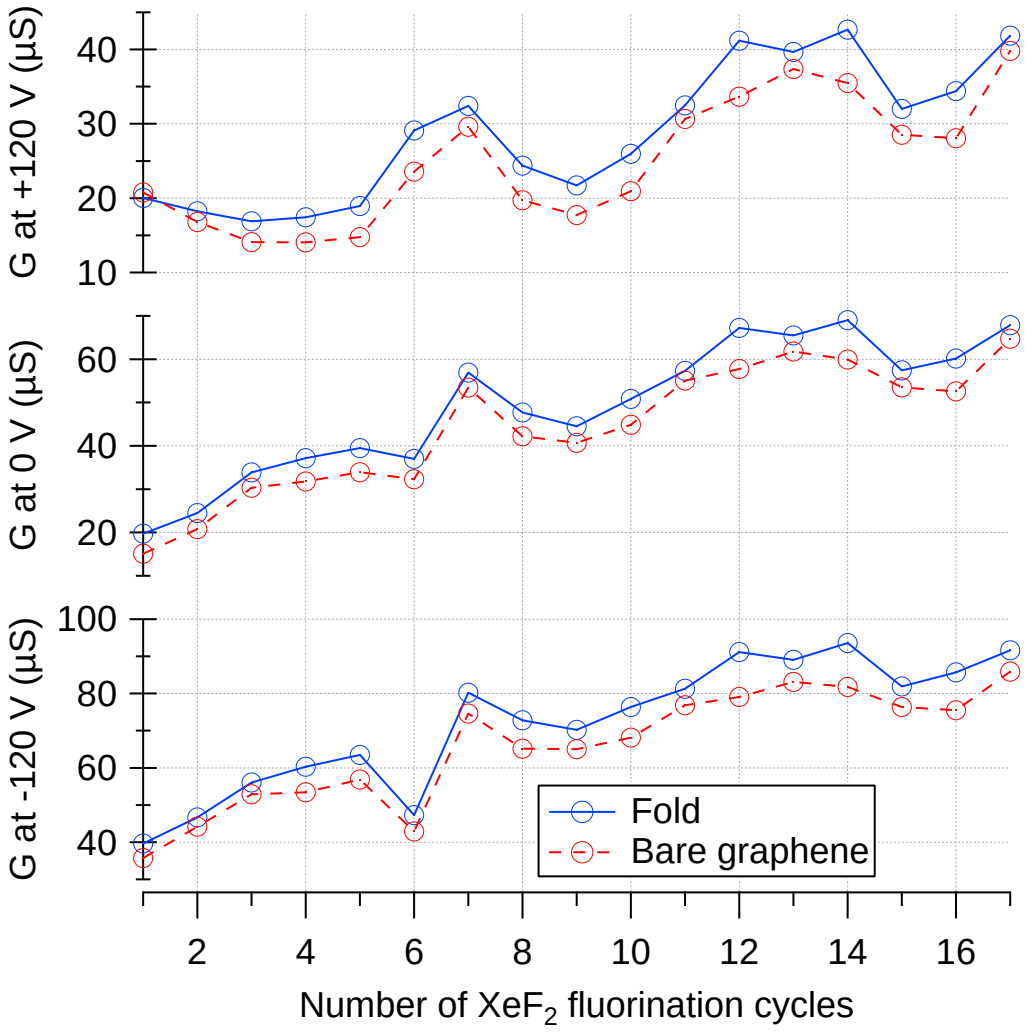

Figure 6.10: Conductance versus fluorination cycle for B45 fold (blue) and bare graphene (red) at gate voltages of +120 V (top), 0 V (middle), and -120 V (bottom).

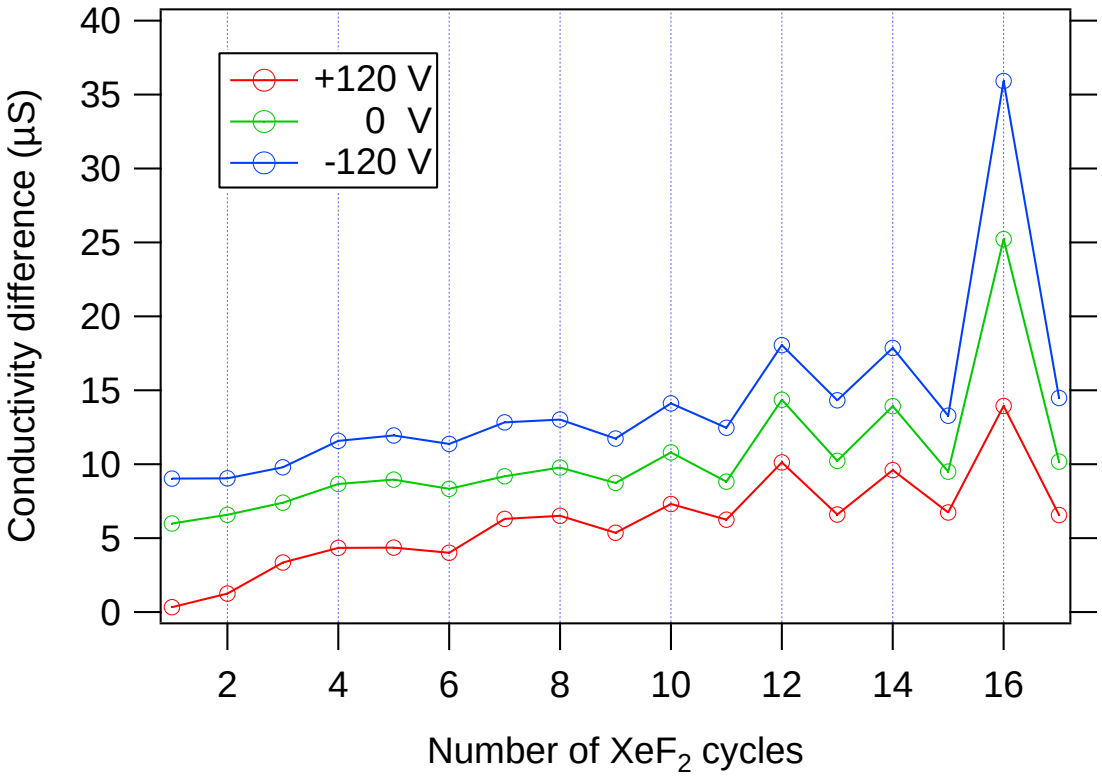

Figure 6.11: Plot of conductance differences between bare graphene and fold sides of B44 at gate voltages of +120 V (red), 0 V (green), and -120 V (blue) for each fluorination cycle.

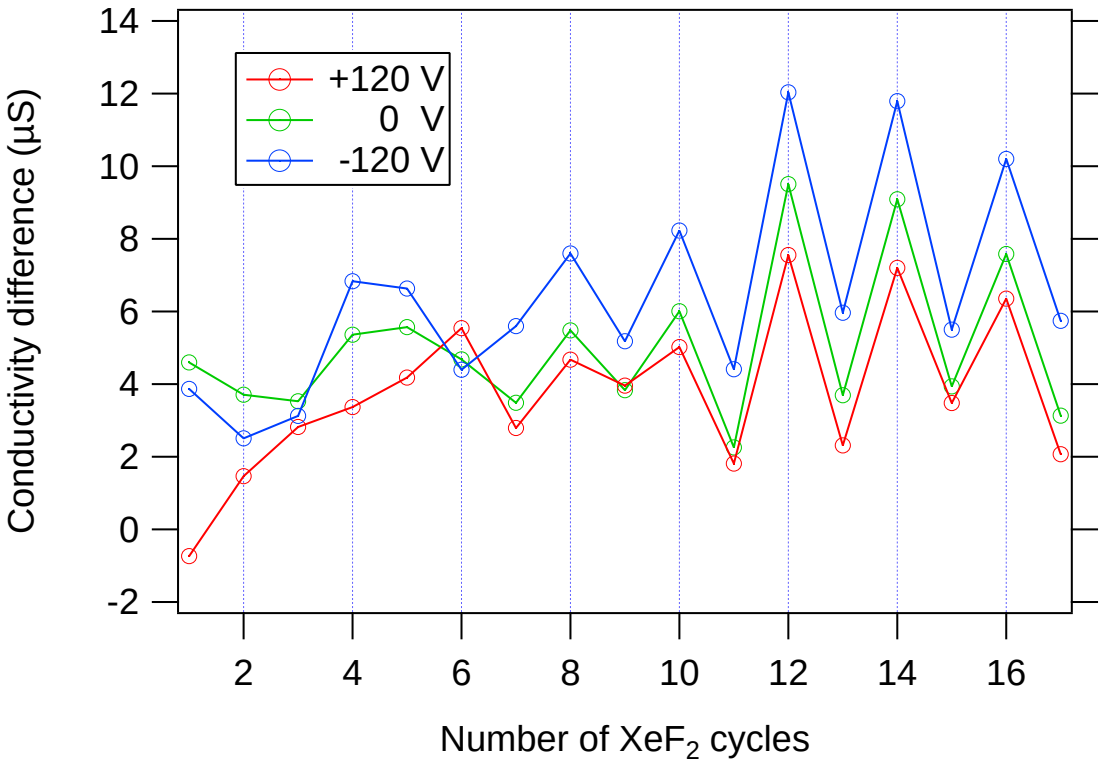

Figure 6.12: Plot of conductance differences between bare graphene and fold sides of B45 at gate voltages of +120 V (red), 0 V (green), and -120 V (blue) for each fluorination cycle.

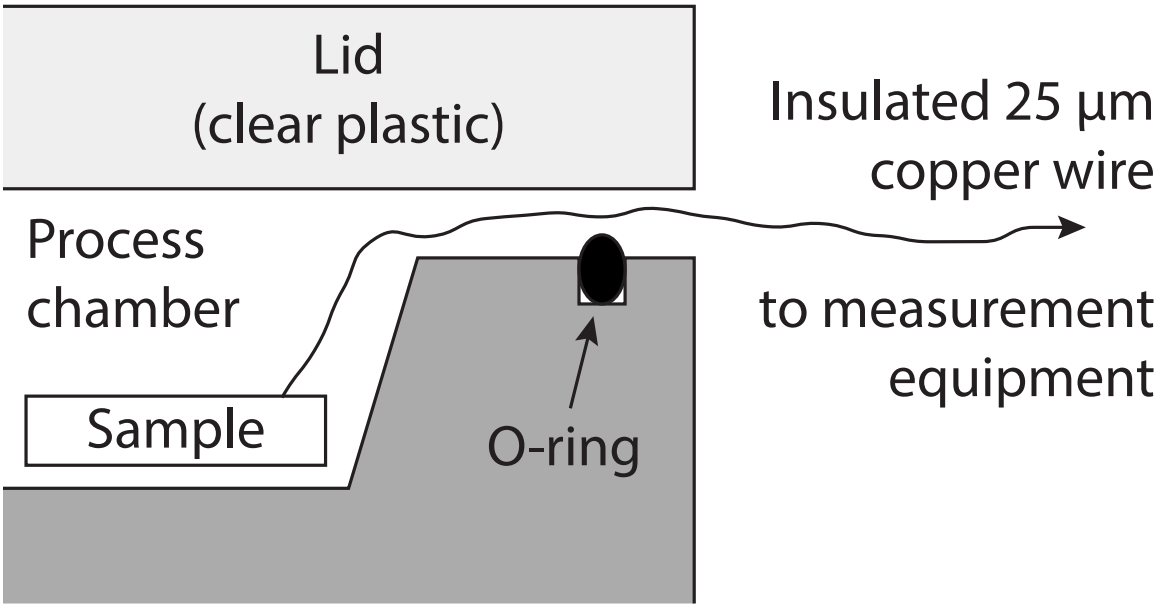

Figure 6.13: Schematic of Xetch lid seal, shown with lid slightly ajar and a single wire connecting to the sample. Not to scale.

Our first idea, inductive coupling, had the advantage of not requiring feedthroughs, but made it difficult to control the gate and source/drain independently. The second, a complete replacement of the lid with new feedthroughs, was problematic due to the difficulty in machining and fitting a duplicate. The lid construction is relatively complicated, with multiple layers of transparent plastic that route the process gases to a "showerhead" nozzle array. We would also be responsible for ensuring that the system was returned to perfect operating shape when we were done. The third idea was to simply close the lid on fine insulated wires and hope that the pliant o-ring was able to form a seal around the wire. Because of its simplicity, we decided to test the efficacy of this simple technique before exploring the complicated solutions.

The Xetch lid assembly is shown schematically in figure 6.13. The process chamber is on the left and the room is on the right. The vacuum seal is a large Viton o-ring recessed in a groove in the main part of the vacuum chamber. The lid is made of transparent plastic and presents a flat face against which the o-ring seals.

To test the wire "press-seal" technique, we prepared loops of wire to close in the Xetch lid. Two nominal sizes of wire, 25 µm (0.001 inches) and 51 µm (0.002 inches) were used in these initial tests. Both were from California Fine Wire Company, were

99.99% copper, and had insulation code "H-ML".[1] Based on specification sheets from the company, the 25 µm and 51 µm wires had actual outer diameter ranges of 30-36 µm and 61-69 µm [95], and insulation breakdown voltages of ∼300 V and ∼600 V [96], respectively. These insulations were more than sufficient for our <100 V gate voltages provided the insulation remained intact.

The wire loops were placed flat on the Xetch o-ring, making sure that they did not cross each other, and the lid was shut while the system began to pump. Neither gauge of wire changed the measurable base pressure of the system; in both cases it pumped down to "0.0 torr". The gate valve to the pump was then closed, isolating the evacuated process chamber and allowing air to leak in through the seal.

The 25 µm wire performed similar to the control experiment with no wire, with the pressure increasing by ∼0.1 torr in the first minute. The 51 µm wire performed significantly worse, with the pressure increasing to ∼1 torr over 1 minute. While this would likely still contain the XeF_2 to a safe degree, the possibility of air contamination and the resulting uncertainty in the partial pressure of XeF_2 made the 51 µm wire an undesirable choice. We instead chose the 25 µm wire, which was the largest wire that maintained the process chamber vacuum seal.

6.8.2 New sample holder design

To make measurements inside the Xetch, we also needed a mechanically strong way to attach long 25 µm wires to the sample. We decided to use carbon paint to affix the sample to a ceramic dual inline package (CerDIP). The resistance of the CerDIPs to XeF_2 was not known, but at the low exposures we were planning, it was not expected to affect their performance or structural integrity. The carbon paint provided electrical connection from the silicon back gate to the metal CerDIP sample surface, and from there we wirebonded from the CerDIP pads to the device contact pads and to the sample surface. Wirebonding was performed with the Zettl group Westbond wedge bonder using 25 µm aluminum wire. This was found to adhere much better to our evaporated gold contacts than a ball bonder using gold wire.

We bonded to only three pins on the CerDIP: the source, which was to be grounded, the drain, which would connect to our source-drain current source, and the gate, which would connect to our gate voltage source. All three pins connected to the same side of the CerDIP, so we were able to connect to it using a single strip connector with the same pin spacing as the CerDIP. The relevant pins on this connector were soldered to three 25 µm wires.

Removing the insulation from the fine wire was difficult; the polyimide did not seem to be affected by any common lab solvents. The most consistent method for exposing the bare wire was to produce as brief a flame as possible from a standard

[1] "ML" designates a certain polyimide formulation, and "H" designates a "heavy" application of insulation.

butane lighter and use it to quickly heat the fine wire. The wire needed to be heated enough to damage the insulation but not so long as to melt or oxidize the copper. In practice this was a very fine line, as the wire would melt and fall apart extremely quickly. Patience was required. After the insulation was damaged it could be wiped off with a Texwipe, leaving a visibly bare section of wire.

The other ends of the fine wires were soldered to pins that went into a purpose-built breakout box with grounding switches and 2 BNC connectors to connect to the voltage and current sources.

6.8.3 Graphene samples

The graphene samples for these experiments were fabricated identically to those in section 6.4 with one minor difference: most of the samples were fabricated on hBN flakes as described in chapter 4. This was to reduce extrinsic effects from the substrate, allowing us to more precisely examine the intrinsic graphene and subsequent fluorination effects. This change in substrates represented only a modest amount of additional work during the design stage, choosing folds that were on hBN instead of those on SiO_2.

6.8.4 Fluorination and measurement

After several failed attempts, possibly due to electrostatic discharge destroying devices, we were able to measure a sample in the Xetch before, during, and after fluorination. Sample J14, which was a parallel fold on a hBN substrate, was subjected to a number of short ($\sim$1 sec, $\sim$1 torr) XeF_2 pulses followed by longer exposures. The gate voltage, source-drain current, and data collection was handled entirely by a single Keithley 2602A controlled by a LabView VI written by Seita Onishi, a fellow graduate student in the Zettl group. The conductivity data were collected in the form of both gate voltage sweeps and time series data at a gate voltage of 0 V. Because the Keithley sourcemeter was making a simple 2-probe DC measurement with no averaging, the noise level was much higher than we previously measured with the lock-in amplifier. This noise level made no difference in extracting parameters such as Dirac point voltage or mobility from the data, however.

There were some issues with gate leakage during the measurement which limited our gate voltage to $\pm$5 V at some points. This caused several problems, as seen in our resulting data.

6.9 Data II

We collected a great deal of data during the fluorination: 245 data sets including gate sweeps and time series, and 14 separate exposures to XeF_2, varying in time and

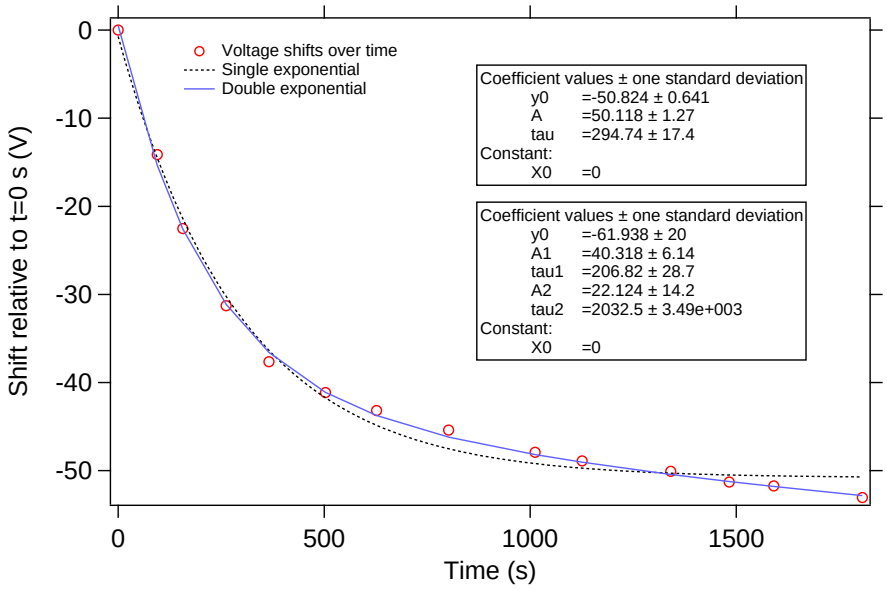

Figure 6.14: Shift in conductance over time, relative to the first data collected after fluorination (t=0 sec). Two different fits to the data are shown, a single and double exponential.

pressure.

6.9.1 XeF_2 desorption

The first interesting data collected were measurements of the gated conductance while pumping on the sample after fluorination. By observing changes over time, we were able to measure the rate of desorption of fluorine species from the sample.

A condensed version of these data appears in figure 6.14. Because the sample was already doped so much that the conductance minimum could not be measured, the shift from each data set was calculated by finding the difference in voltage for a fixed conductance value for each curve. The resulting data did not depend on what conductance value was selected, justifying our calculation method.

We assigned two different fits to the data, a single exponential and a double exponential. A single exponential could correspond to many processes, including the existence of a desorption barrier that is thermally activated. Any given adsorbed molecule would have a fixed probability per unit time of desorbing from the surface. The time constant calculated with this fit is around 300 seconds.

A double exponential fit the data slightly better, as seen in figure 6.14. Two exponentials would be consistent with the presence of two distinct types of bonding by the XeF_2 molecules. This would result in two different bonding strengths and therefore two different rates of desorption. The two time constants calculated with

this fit are around 200 and 2000 seconds, and the shift in the data at $t \to \infty$ is -62 V.

6.9.2 Further fluorination

We continued to fluorinate and take data, and the sample became more and more hole doped until the fluorine destroyed the conductance in most of the graphene and the conductivity dropped. Data from before fluorination, after two fluorinations, and after 14 fluorinations appear in figure 6.15a.

After two fluorinations, the conductance increased at all gate voltages, and the conductivity minimum moved far to the right. This was entirely consistent with strong hole doping from fluorine species on the graphene. There had not been enough fluorine exposure to damage the graphene, only enough to heavily dope it and increase scattering a relatively small amount.

After 14 fluorinations, something unusual happened. The conductance dropped, but the data appeared to have a gate response that looked like undoped graphene. These data are consistent with complete fluorination of the outer graphene layers of the fold in sample J14, removing all conductivity. With the outer layers passivated, the inner layers of graphene are protected and retain their conductivity despite subsequent fluorinations. The remaining conductance and gate response seen in figure 6.15 is only from the inner part of the fold.

A magnified view of the conductance minima of sample J14 pre-fluorination and after 14 fluorinations appears in figure 6.15b. Their conductance minima were both very close to zero, indicating very low net doping.

The conductance minimum of the sample pre-fluorination was 268 µS, and the conductance minimum after was 9.0 µS, a factor of 30 lower. Given that the graphene was originally 2.5 µm wide and assuming a bilayer fold is preserved, this corresponded to a fold width of approximately 80 nm, consistent with the ∼100 nm width observed with the SEM.

6.10 Conclusions

We have demonstrated fluorination of both bare graphene devices and folded devices, and shown tentative evidence that we can fluorinate graphene while preserving the fold underneath. There remains a great deal more work to be done with these devices. This includes repeating the fabrication to measure more devices and making more sophisticated measurements to understand the electronic structure of the devices we have fabricated. Our results show that current studies of graphene fluorination have only scratched the surface.

Further fluorination research may allow researchers to tune the band structure with spatial control as well. Preliminary experiments have shown defluorination of graphene by electron beam exposure, which could lead to complex graphene circuits

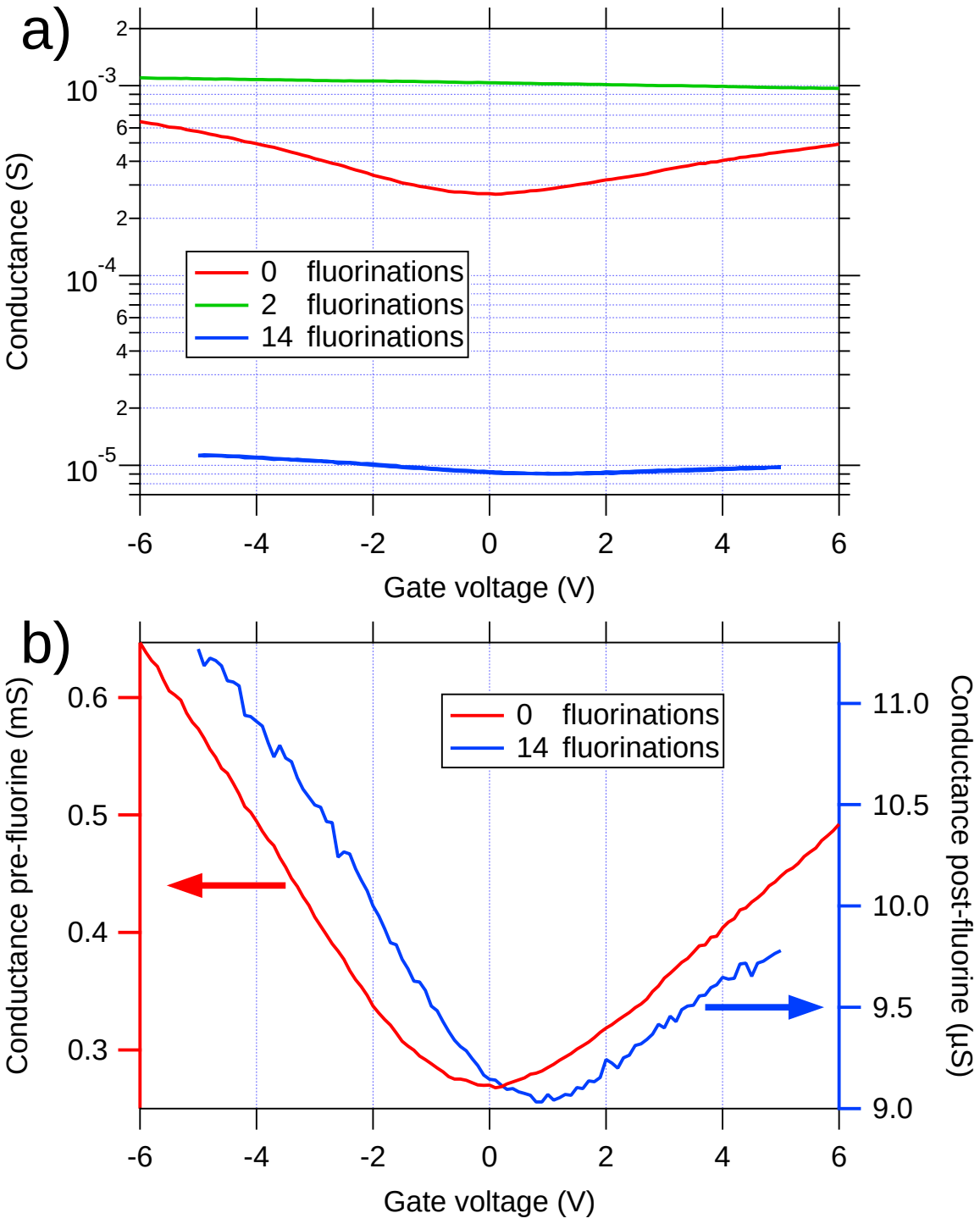

Figure 6.15: (a) Conductance of sample before XeF_2 exposure (red), after two exposures (green), and after 14 exposures (blue). (b) Magnified view of the conductivity minima of the pre-fluorination (red) and 14 fluorination (blue) data. Note the difference in scales (mS vs µS).

embedded in fluorographene sheets [97]. Such embedded structures are predicted to have interesting properties, including tunable effective masses [98]. Preliminary work has also been done showing selective fluorination with laser patterning of fluoropolymers on graphene, but this likely has lower resolution than electron beam patterning [99].

Fluorination of hBN may also prove promising. Theoretical calculations show that fluorinated hBN may have interesting electronic and magnetic properties [100, 101]. However, our initial attempts to fluorinate hBN with XeF_2 resulted in no measurable changes in the transport properties. Modifying the recipes by using higher temperatures or longer exposures may give better results.

Chapter 7

Graphene nanoribbons from BN nanotube masks

7.1 Graphene nanoribbons

As previously mentioned, opening a bandgap in graphene has long been a goal for researchers hoping to improve the performance of graphene transistors. One such technique is to fabricate graphene nanoribbons (GNRs). The lateral confinement can quantize the transverse momentum states, opening a band gap similar to that found in semiconducting carbon nanotubes [76].

7.1.1 Previous synthesis

Many techniques have been developed for fabricating graphene nanoribbons over the last six years, with varying yields and scalabilities.

Simple lithographic techniques, where nanoribbons are etched from bulk graphene using a polymer mask, are the most accessible for typical nanofabrication labs, since they require common equipment and materials including electron beam lithography and plasma etching [76].

Hongjie Dai's group at Stanford has developed two unique techniques for GNR synthesis. The first is liquid-phase exfoliation of graphite followed by stabilization and isolation of graphene nanoribbons using a polymer known as PmPV[1][102, 103]. The second is plasma etching of carbon nanotubes that are partially embedded in a polymer resist which masks the bottom half of the tube, protecting it from etching [104].

One additional technique is the "unzipping" of carbon nanotubes using highly reactive alkali atoms, which was first done by James Tour's group at Rice University [105].

[1] poly(m-phenylenevinylene-co-2,5-dioctoxy-p-phenylenevinylene)

7.1.2 GNR transport

Predicting the transport properties through graphene nanoribbons can be difficult due to the large number of structural variables. These include the crystalline orientation, dopants, defects, and edge functionalization.

The electron band structure of graphene nanoribbons can vary significantly between nanoribbons, much like the variability in single walled carbon nanotubes. It was calculated early on that the band structure of graphene nanoribbons is width- and chirality-dependent [106]. This should come as no surprise given the analogy to carbon nanotubes. In both cases a constraint is imposed on the electron wavefunctions in the material; for the nanotube, it must be periodic in the azimuthal direction, and for the nanoribbon, it must drop to zero outside the width. The geometric relationship between these constraints and the underlying graphene band structure determine the bands of the nanostructure.

Calculations also show that the electronic properties of GNRs can be extremely sensitive to the edge structure of the nanoribbon. This includes effects from edge functionalizations [107–109] which can strongly affect the existence of and transport through the edge states of the nanoribbon [110, 111].

While the above intrinsic properties can influence carrier transport through the nanoribbon, extrinsic factors can have an even larger influence. Because of the nanoribbon's narrow width and existing sensitivity to edge states, the system's behavior depends strongly on edge disorder. Calculations have shown that nanoribbons with edge disorder have conductivities far below that of nanoribbons with pristine edges, which is attributed to Anderson localization from scattering at the nanoribbon edges [112].

The structures modeled by Mucciolo et al. [112] are not unrealistic, especially for those nanoribbons made by reactive ion etching. Since it is a random process acting on the edge of the nanoribbon, one would not necessarily expect an ordered edge structure, and the presence of disordered edge functionalizations would likely reduce the conductivity further.

In addition to the chemical structure of the edges, interactions with the substrate can strongly affect nanoribbon transport. It is well known that silicon dioxide substrates can locally dope graphene, with length scales around 10 nm [48, 65]. Contaminants on the sample can contribute further disorder, which is discussed in depth in chapter 4.

In the case of "bulk" graphene gated to an overall neutral charge density, carriers then find themselves in a 2-D percolative network. If a nanoribbon with width less than the length scale of the disorder is put in the same environment, the reduced dimensionality significantly changes the nature of transport. Instead of a well-connected network of p- and/or n-type regions, the conducting channel is a chain of many p- and n-type sections in series, as illustrated in figure 7.1.

This reduced dimensionality leads to Coulomb blockade behavior in the conducting

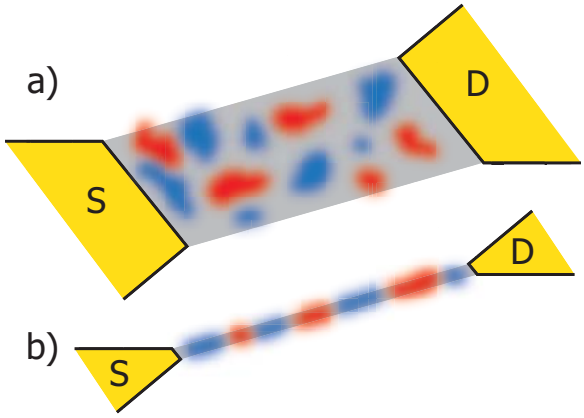

Figure 7.1: Schematic of the effect of substrate doping on graphene nanoribbons and larger graphene devices. a) Impurity effects on 2D samples. b) Impurity effects on quasi-1D samples.

channel, with transport dominated by carriers hopping between adjacent graphene quantum dots.

This hopping transport will appear as a "transport gap," where at lower gate and source/drain voltages, the conductivity of the system is very low [113, 114]. This may appear deceptively consistent with the response of a system with a bandgap because, unlike in 2D graphene, there will be no conductivity over a wide range of gate or source/drain voltages.

As a result, interpreting graphene nanoribbon data and distinguishing a true bandgap from a transport gap can be difficult. Optical studies, which are very useful for bulk bandgap measurements, are very difficult for samples one atom thick and ∼10 nm wide.

Many transport experiments have been performed on graphene nanoribbon or nanoconstrictions. At low temperatures Coulomb diamonds have been observed, presumably due to contamination or other disorder [113–116].

7.1.3 Improvements

All of the fabrication techniques mentioned above require steps that can contaminate the resulting nanoribbons, whether from polymer residue [76, 102, 104] or other contaminants from liquid-phase treatment [102, 105]. A fabrication method that preserved the cleanliness of the nanoribbon would facilitate the identification of true bandgaps, since the reduction in disorder could eliminate the transport gap. Suspending graphene nanoribbons would be the best way of reducing surface interactions. However, their fragility made this extremely difficult, so we attempted to

do the next best thing: use a very clean and flat substrate for the nanoribbon. To date, all measurements of graphene nanoribbons have been performed either on SiO_2 substrates or with suspended nanoribbons, which are difficult to gate and very fragile. The ideal geometry for a nanoribbon measurement would not be suspended but on a very clean material that introduced no scattering at the interface.

7.2 Experimental design

The design of these devices was inspired by our own prior work described in chapter 4 and that of Prof. James Hone's group at Columbia University, which showed that graphene's interface with boron nitride introduced very little scattering [51, 57]. Etch masks used previously by other groups were made of materials such as polymers or nanowires that could introduce scattering. Boron nitride seemed like the ideal material to use if the underlying graphene was to be kept as clean as possible. The boron nitride could even be left in place on the graphene device while measurements were made, giving the graphene further protection from its environment. While this technique was potentially applicable to larger transistors by using hBN flakes above and below the graphene as in [44], we focused on the use of boron nitride nanotubes as etch masks for graphene nanoribbons.

The design and fabrication herein were performed with Will Regan, a fellow graduate student in the Zettl group.

7.2.1 Boron nitride nanotubes

Boron nitride nanotubes (BNNTs) are the 1-D allotrope of boron nitride much as carbon nanotubes are the 1-D allotrope of carbon. One or more sheets of the hexagonal material is rolled into a tube along one of many allowed rolling directions, creating a structure that has periodicity around the azimuth and longitudinal translational symmetry. A longitudinal view of one possible single-walled BNNT appears in figure 7.2.

The electronic properties of BNNTs were first predicted at UC Berkeley by Marvin Cohen and Steve Louie's groups in 1994 and they were first synthesized in the Zettl group the following year [117–119]. Boron nitride nanotubes are virtually always multiwalled, and in some cases are reported to form facets with helical symmetry [120].

Hexagonal boron nitride has a very large bandgap ($\sim$6 eV [50]), and BNNTs have similarly large bandgaps ($\sim$5–6 eV [117, 118]). It has been predicted that there are ways of reducing the bandgap of BNNTs by various means, including chemical functionalization or strain [122, 123]. In these experiments, the high resistance of the BNNTs allows them to be left in place on graphene nanoribbons and not affect subsequent electronic measurements.

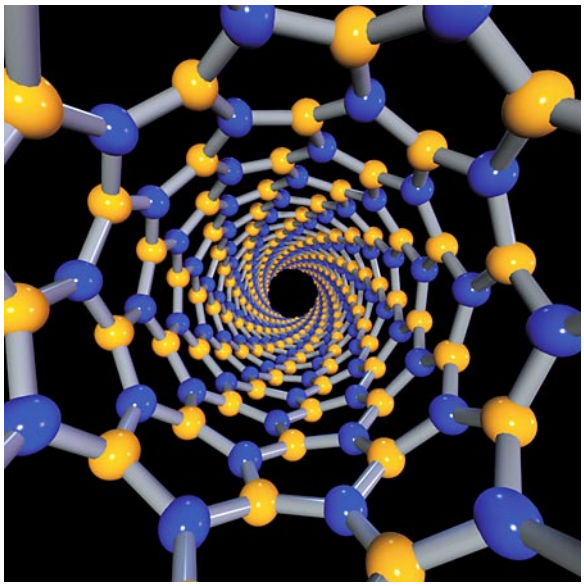

Figure 7.2: Rendering of a BN nanotube down its axis, from [121].

7.3 Fabrication I: Nanoribbons on SiO_2

The goal of fabricating these devices was to produce the cleanest possible graphene nanoribbons in a form that could easily be electronically characterized. We wanted to randomly deposit high-quality BNNTs on clean areas of graphene and perform lithography to deposit metal contacts aligned to the nanotubes. The metal would make contact to the graphene, and the sample would then go through a light oxygen plasma etch. The metal would protect the graphene underneath it, as would the boron nitride nanotube. Since the nanotube is an insulator, any electronic transport between the contacts would be exclusively from the graphene nanoribbon. A schematic of this fabrication appears in figure 7.3.

There were several key questions prior to fabrication of these devices. First was whether to use exfoliated or CVD-grown graphene. Exfoliated graphene would be higher quality with larger crystal domains and less contamination, but using CVD graphene would result in several orders of magnitude more potential devices due to the much greater coverage of graphene monolayer on the substrate. We decided to initially use exfoliated graphene in hopes that it would form cleaner devices, and because we believed we needed only a handful of devices to measure.

The only other considerations in fabricating our devices were the channel length and the number of electrodes. For these devices, we placed 4 electrodes with 500 nm gaps between each. This allowed the possibility of either 2-probe or 4-probe measurements.

We mechanically exfoliated graphite using Scotch tape onto silicon wafers with 300 nm of thermally-grown oxide that had been cleaned in a piranha solution. After

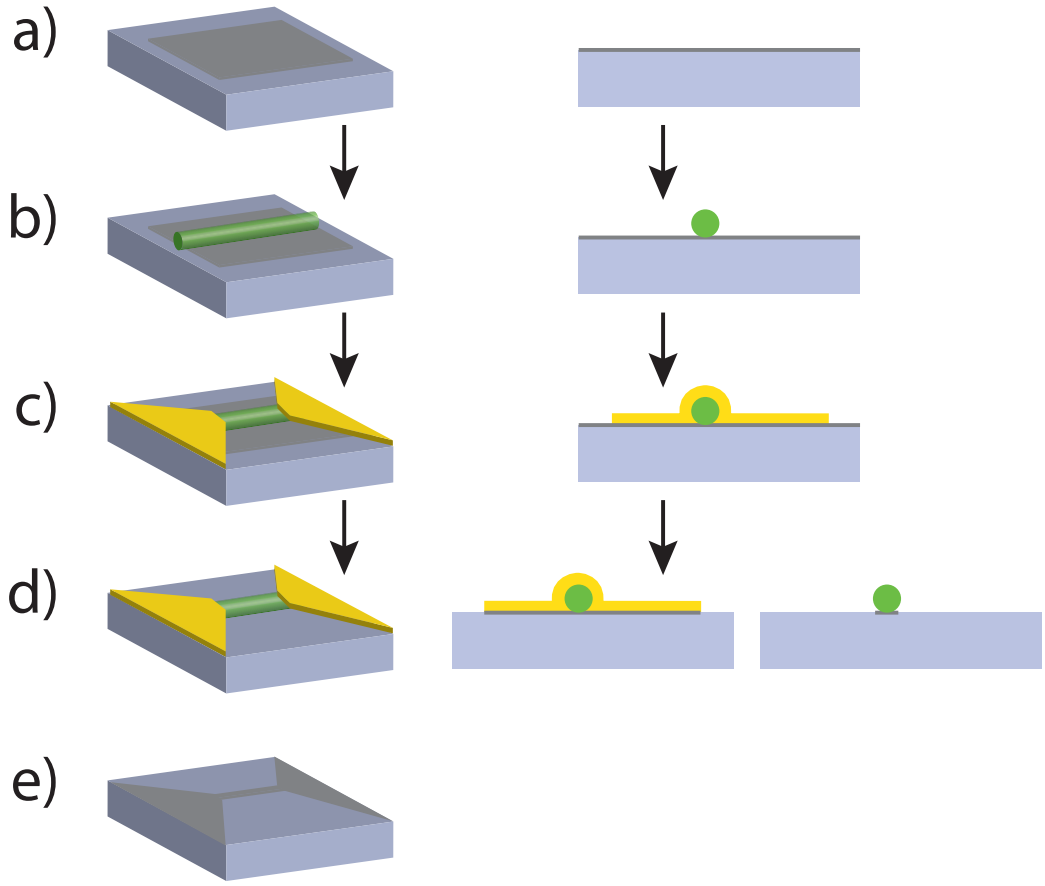

Figure 7.3: Schematic of fabrication of graphene nanoribbon devices from BNNT masks. The left column shows a perspective view, the right shows a cross section. (a) Graphene is transferred onto a clean piece of SiO_2 by mechanical exfoliation or PMMA transfer. (b) BNNTs are deposited randomly on the sample by spin casting. (c) After mapping, contacts are deposited through a mask defined by e-beam lithography. (d) The sample is etched in an oxygen plasma, removing the graphene everywhere except under the contacts and under the BNNT. Both of these instances are shown in the cross section. (e) The final device as in (d) but shown without contacts or BNNT to illustrate the final shape of the graphene.

removing the tape, we found several candidate monolayer regions using optical microscopy. We then sonicated a solution of BNNTs suspended in isopropyl alcohol for a few minutes and spin-cast ∼200 µL at 5000 rpm. The BNNTs used were CVD-grown by Michael Rousseas, a fellow graduate student in the Zettl group. They were labeled "CVD2" and had stated diameters of 20-50 nm.

We mapped the previously identified monolayer regions in both the optical microscope and the SEM. The density of BNNTs was close to ideal; there was approximately one candidate BNNT per monolayer graphene region and very little overlap between

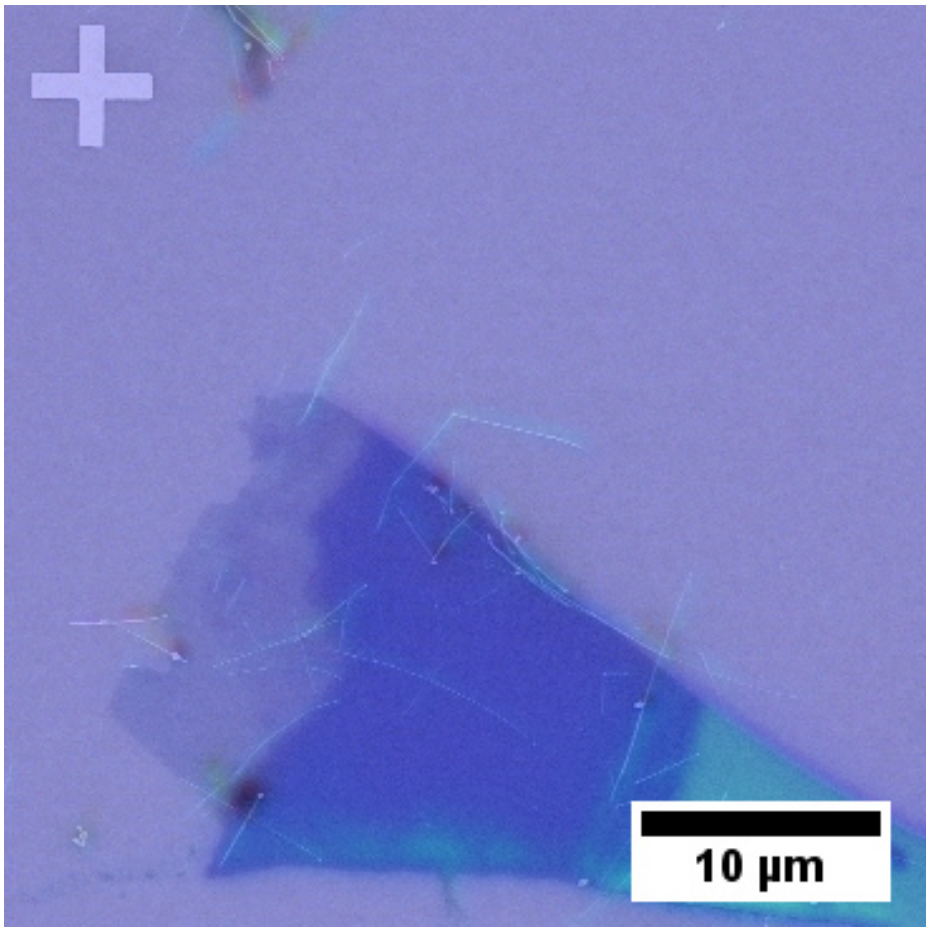

Figure 7.4: Boron nitride nanotubes on mechanically exfoliated graphene on SiO_2. The image is a composite of optical and SEM images taken of device B1. The region on the left is a monolayer, as determined by optical contrast, and a number of BNNTs are visible on it.

BNNTs. This made device design straightforward.

Figure 7.4 shows boron nitride nanotubes on a graphene monolayer in a combined optical and SEM image. The monolayer was identified by both optical contrast and Raman spectroscopy. The BNNTs were sometimes visible in the optical microscope, but SEM mapping was needed to obtain sufficient accuracy for lithography.

After patterns were designed, we performed the single lithography step and evaporated Cr/Au to form contacts. The devices were then etched with the Zettl group reactive ion etcher using our "standard" graphene etch recipe: 50 W, 50 sccm O_2, 20 seconds. This removed all graphene that was not under the contacts or the BN nanotube. One completed device appears in figure 7.5

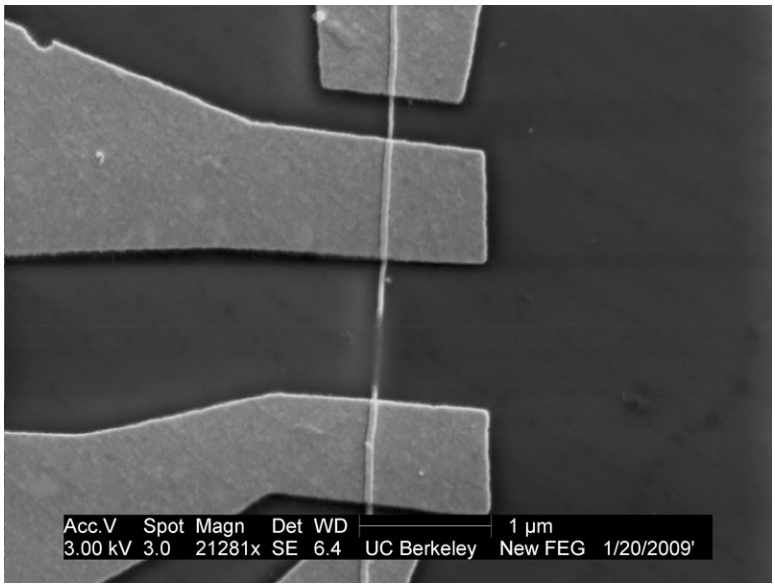

Figure 7.5: SEM image of a BNNT-masked graphene nanoribbon device after contact deposition and reactive ion etching.

7.4 Measurement I

After fabrication, we were left with one surviving monolayer device, B1, shown in figure 7.4. We measured device B1 in the cryogenic probe station as described in section 4.4 but with a lock-in amplifier using a two-probe configuration. After preliminary conductivity measurements at room temperature, we cooled the sample to 78 K by transferring liquid nitrogen through the flow cryostat. We then took additional measurements, which appear in figure 7.6.

As a control, we also fabricated devices using the exact same recipe but without the graphene transfer, performing lithography to wire up bare BNNTs. We then performed identical transport measurements on the control devices. We measured no current, supporting our claim that the data shown in figure 7.6 are from the graphene underneath the BNNT.

7.5 Analysis

The data shown in figure 7.6 have several interesting features. There is a large amount of hysteresis in the data; for the ± 80 V sweep, the conductance minimum changed location by about 60 V depending on which direction the gate was swept. The exact cause of this was unknown, but because the conductance was not a single-valued function of the gate voltage, it is likely that the gate field moved charged species below or around the graphene. This had often been observed in graphene

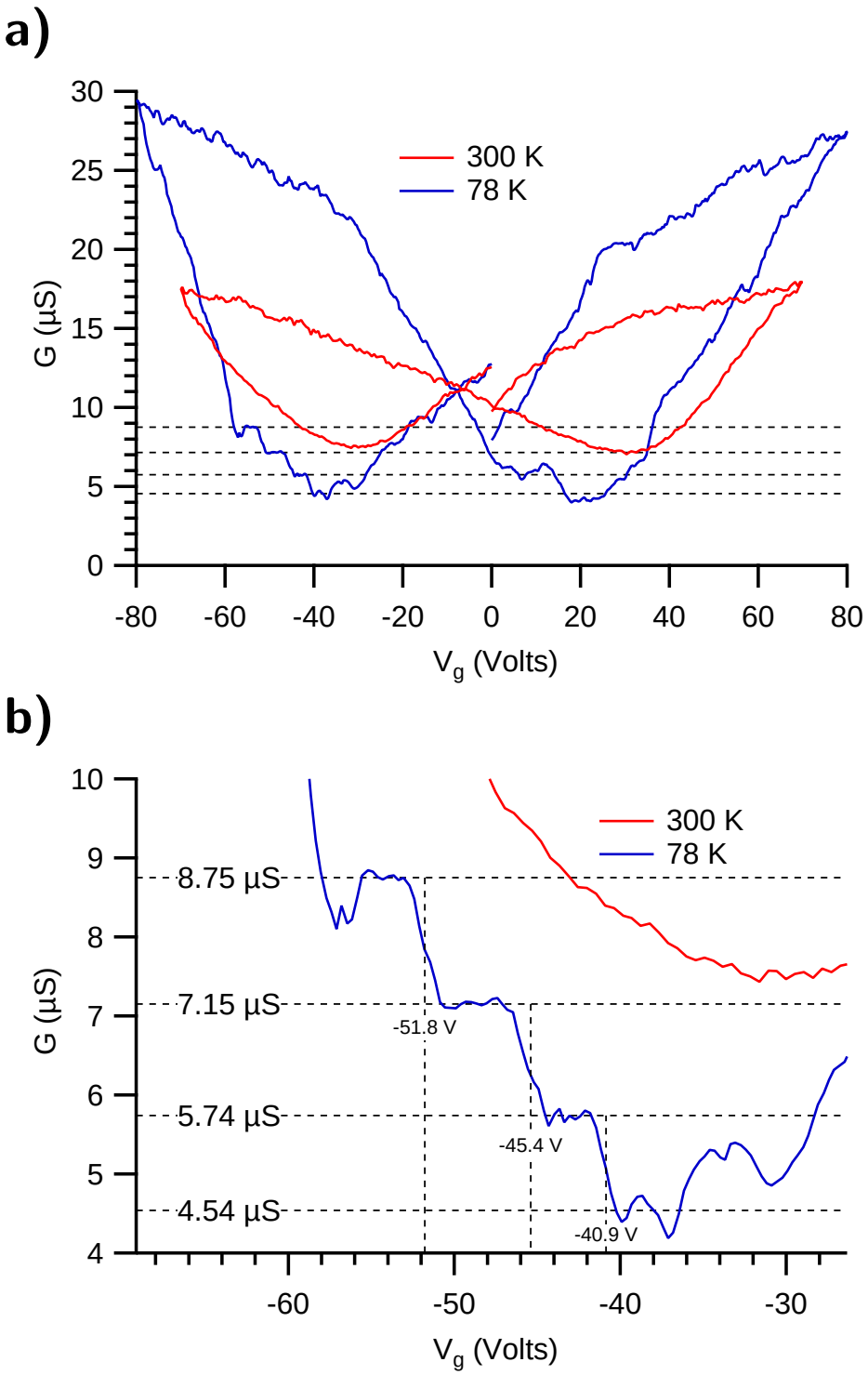

Figure 7.6: (a) Gated conductance data through a graphene nanoribbon under a boron nitride nanotube. (b) Magnification of "steps" in the above conductance data.

devices, especially in ones with contamination.

The value of the conductance minimum for this device is 4.5 µS, significantly less than typical devices with 1:1 aspect ratios. This lower conductance is consistent with the graphene becoming a nanoribbon. Given that square devices typically have conductance minima around 300 µS, we can crudely estimate the aspect ratio of this sample to be $300/4.5 \approx 70$. Given that the electrode spacing was 500 nm, we calculate a width of about 8 nm. Note that this calculation assumed the graphene under the BN nanotube remained unaffected by the plasma etching, which we had no independent way of measuring.

The most unique feature of these data is the appearance of steps in the conductance with changes in gate voltage, as can be seen in the magnified plot in figure 7.6b. The steps are 1.4 ± 0.2 µS in magnitude, far less than the quantum of conductance, $2e^2/h = 77.5$ µS, which would be the magnitude of conductance steps in the Landauer-Buttiker regime [124]. However, the step size is still large compared to the overall conductance. The conductance values of the steps, normalized to the conductance minimum, are 1.26, 1.57, and 1.93, representing differential increases of 26%, 24%, and 22% respectively.

Of equal importance are the locations of the step changes in terms of voltage, which are noted in figure 7.6b. The changes in conductance occur at -51.8 V, -45.4 V, and -40.9 V, which means the differences in voltage are 6.6 V, 6.4 V, and 4.5 V, if we include the drop in conductivity at around 58.4 V.

This step structure is similar to features seen by researchers at IBM in graphene nanoribbons fabricated by etching patterned with hydrogen silsesquioxane (HSQ) masks [125]. They attributed these conductivity features to sub-band formation caused by the narrow nanoribbons. It is difficult to confirm that this is the origin of the features we measured without width-dependent measurements or a more direct measurement of the band structure. Such measurements would be very difficult, however, as the nanoribbon width is not easy to measure under the BNNT.

7.5.1 Capacitance of nanoribbons

It is also difficult to convert these gate voltages into carrier concentrations. Our derivation of that relationship in chapter 2 relied on the fact that the typical gated graphene geometry was very close to a parallel plate capacitor. Because our graphene is no longer much larger than the separation between the "plates" of the capacitor, the fringing field is no longer negligible and the capacitance calculation is no longer trivial. Additionally, the carrier concentration is no longer uniform across the surface of the graphene due to the geometry.

A calculation of the charge density and capacitance for this geometry was performed by Nishiyama and Nakamura [126]. Their calculations rely solely on b, the ratio of the electrode gap to the nanoribbon width, which is about 40 given our above width calculation. This is substantially higher than the values of b used by Nishiyama

and Nakamura, which were no higher than 10 [126].

For wide graphene samples on 300 nm of SiO_2, the specific capacitance is $\epsilon/d \approx 115$ aF/μm^2. For a sample that is 8 nm wide (which clearly violates the parallel plate condition), this gives a capacitance-per-length of 0.92 aF/μm.

Using the equations from Nishiyama and Nakamura [126], we obtain a capacitance-per-length of

$$C = C_0 C_n = \frac{\epsilon}{b}\left[1 + 1.9861 b^{0.8258}\right].$$

Before we substitute a number for b, the dielectric environment of the graphene, half oxide and half vacuum, leads to an additional correction [126]

$$\epsilon_{\text{eff}} = \frac{\epsilon + 1}{2} + \frac{\epsilon - 1}{2\sqrt{1 + 10b}},$$

which equals 2.52 assuming $\epsilon = 3.9$ for SiO_2 and $b = 40$. Thus, our final capacitance-per-length becomes $2.7\,\epsilon_0 = 23.9$ aF/μm, about 26 times higher that that calculated by the parallel plate equivalent specific capacitance. This value is less than the 43 aF/μm calculated capacitance for a 4 nm radius wire in SiO_2, 300 nm away from a conducting plane.

Thus, for a given dielectric and gate voltage, a nanoribbon will have a much higher induced charge density than a wide graphene sheet. Furthermore, the charge density will be quite inhomogeneous, with the charge density many times higher at the edges than in the middle of the nanoribbon (see figure 3 of Nishiyama and Nakamura [126]). Unfortunately, Nishiyama and Nakamura do not give numerical data nor equations for the charge density, so it is difficult to make specific predictions. However, we can still calculate an average carrier density based on the capacitance, which again assuming an 8 nm ribbon, will be 2.0×10^{12} cm^{-2}/V, around 28 times higher than that from the parallel plate limit.

Using this average capacitance number, the conductivity changes at voltage steps of 6.6 V, 6.4 V, and 4.5 V corresponded to changes in carrier concentration of approximately 1.3×10^{13}, 1.3×10^{13}, and 9.0×10^{12}, respectively. Again, the carrier concentration on the nanoribbon edges may have been significantly higher.

7.6 Fabrication II: Nanoribbons on hBN

The data in section 7.4 left questions as to which features were from disorder and which were from the band structure of the nanoribbon. In order to better understand the physics of these nanoribbon structures, we wanted more thorough measurements. Specifically, we were hoping to make measurements demonstrating Coulomb blockade, or absence thereof, in the nanoribbons to characterize their inhomogeneity.

We decided to fabricate new devices, again using boron nitride nanotubes as etch masks, but using CVD graphene and boron nitride substrates. The CVD graphene

would be more scalable, which would hopefully result in more than one final device to measure. Based on prior work [57], we hoped that the CVD graphene on hBN would also have mobility comparable to exfoliated graphene on SiO_2, but with fewer charged impurities. These devices were fabricated with the assistance of Seita Onishi, a graduate student in the Zettl group.

We fabricated the devices very similarly to the work described in section 7.2, with CVD graphene transfer replacing the graphite exfoliation. After the oxygen plasma etching, the devices were annealed in a hydrogen atmosphere as in section 4.6 and put in the probe station under vacuum.

7.7 Measurement II

The measurement for this series of devices was decidedly more sophisticated than the gate sweeps described in section 7.4. We wanted to measure the differential conductance, dI/dV, for the nanoribbons at a range of source-drain biases and gate voltages. This required our excitation to be a small AC component on top of a larger DC offset, measured by a lock-in amplifier, and varied independently of the gate.

Our resulting setup is shown in figure 7.7. We used a Rigol DG5072 signal generator that was capable of outputting a sine wave with a large DC offset. The signal went through a 1000:1 voltage divider to reduce the magnitude of the voltage from $\sim$1 V to $\sim$1 mV. This voltage signal then went to the source of the GNR device. The device drain was connected to the SR830 lock-in current input. This input has an impedance of 1 kΩ, which is much lower than the device impedance and is therefore negligible.

The measured current from the lock-in divided by the voltage signal from the divider was dI/dV, the differential conductivity. The DC offset of the Rigol was then varied, as was the gate voltage from the Keithley 2400. This resulted in data in the form of a 2-D surface plot. The LabView VI used to control the equipment and collect the data was largely written by Seita Onishi.

Based on measurements made by Todd et al. [115], Han et al. [114], and Gallagher et al. [113] on similar nanoribbon structures, we expected to see features with gate voltages near the conductivity minimum and source/drain voltages of 5 to 50 mV.

Preliminary room temperature data of one unannealed device (L24) is shown in figure 7.8. In the lower plot, the conductivity minimum is clearly visible at -14 V. Neither plot shows dependence on the source-drain bias, indicating ohmic behavior.

Room temperature data for a second, annealed device (L32) appear in figure 7.9. The conductivity minimum voltage is much closer to zero in this case, showing that the sample is less doped. Similar data at 4 K for the same device appear in figure 7.10, and data for a smaller range of gate voltages appear in figure 7.11.

The data shown in these figures are not particularly revealing of the underlying physics, and very few features are present in the data.

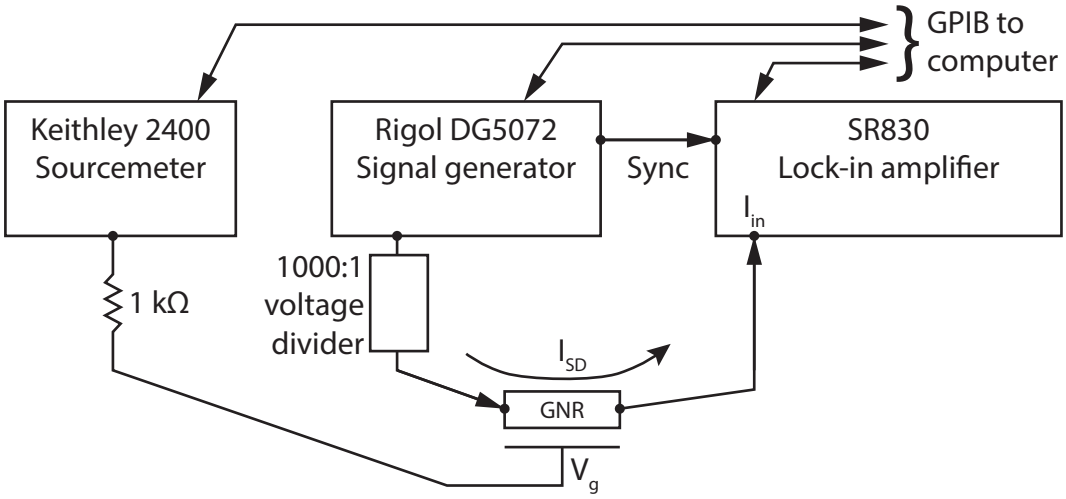

Figure 7.7: Schematic of dI/dV transport measurements on graphene nanoribbon devices.

The data collection was done by varying the source-drain bias while at a fixed gate voltage, and then repeating at a different gate voltage. The displayed data are only the high-to-low sweeps of both source and gate voltages. This corresponds to bottom-to-top and right-to-left for most of the figures in this section.

Vertical stripes such as those seen in figure 7.10 are consistent with physical effects that are very sensitive to gate voltage but also effects such as varying contact resistance from thermal contraction of the probes. It is difficult to distinguish between the two.

There are inconsistencies between overlapping data sets, such as figures 7.10 and 7.11. The origin of this discrepancy is unclear but is also consistent with data that is varying more randomly in time than with the input signals.

7.8 Conclusions

We have seen hints of physically interesting phenomena in the form of steps in the conductivity of graphene nanoribbons, but we have been unable to positively identify their origin. Much of this may be due to varying contact resistance due to our 2-probe geometry. It is possible that a 4-probe measurement may give better data, but the transport measurements made in references [113–115] were 2-probe measurements.

Other possible improvements include measuring with wirebonded leads to limit changes in resistance from moving probes. Also, being able to change the direction of the data collection (i.e. sweeping the source at a given gate voltage or sweeping the

gate at a source voltage) would provide information on how much of the data were due to the sample properties and how much was due to drift in time.

Measuring a larger number of samples would also be preferable. This represents a problem in terms of fabrication, due to our low yield, and in terms of measurement speed, which would need to be increased drastically if a series of samples were to be measured.

Finally, researchers have shown evidence that high temperature hydrogen plasma treatment can etch graphene into nanoribbons with zigzag edges [127, 128]. Combining BNNT substrates and masks with this etching method may provide a route to atomically precise, extremely clean, and potentially scalable graphene electronics.

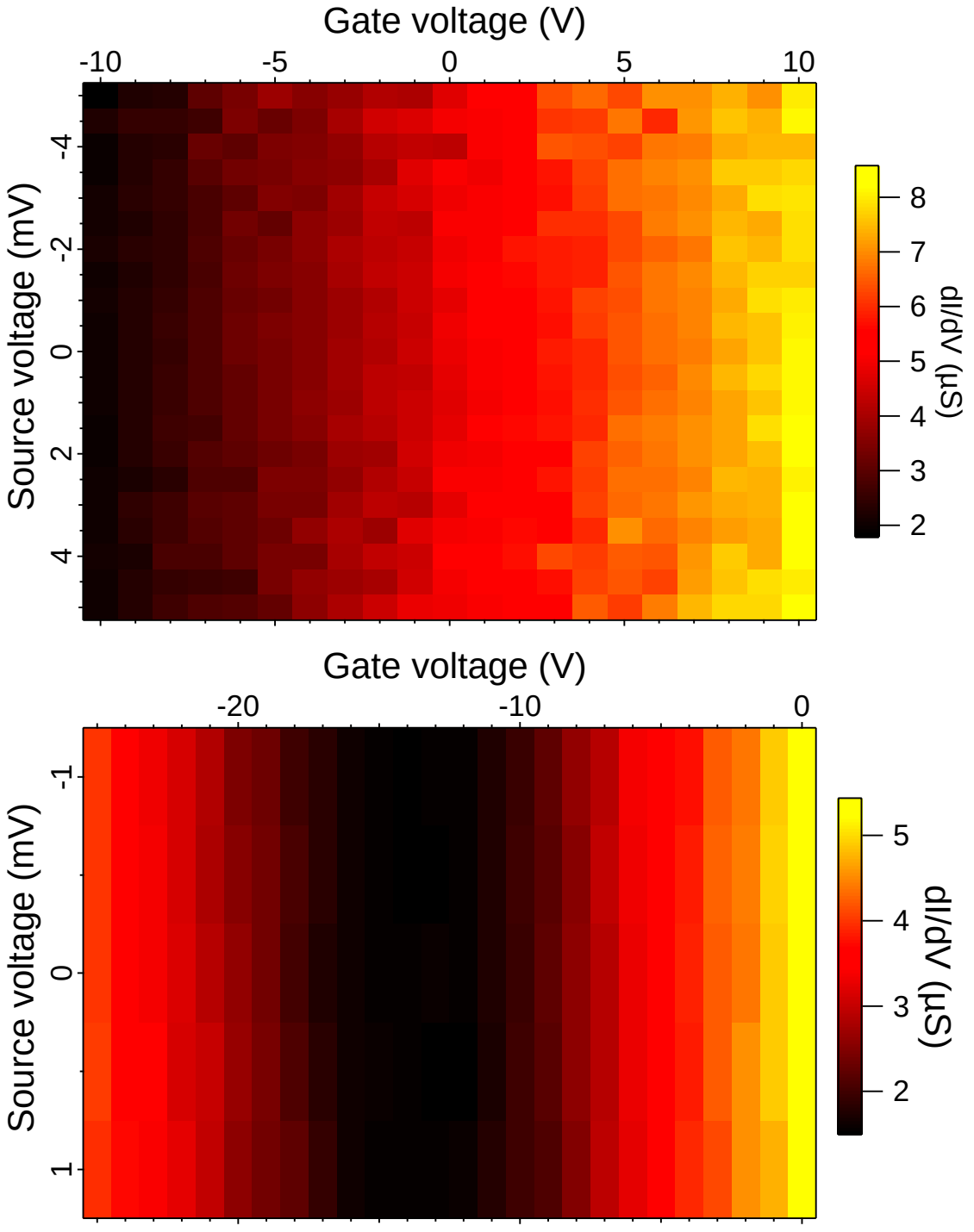

Figure 7.8: Room temperature dI/dV data for graphene nanoribbon L24 over different gate voltage and source voltage ranges. The bottom data contains the charge neutrality point at ~ -14 V.

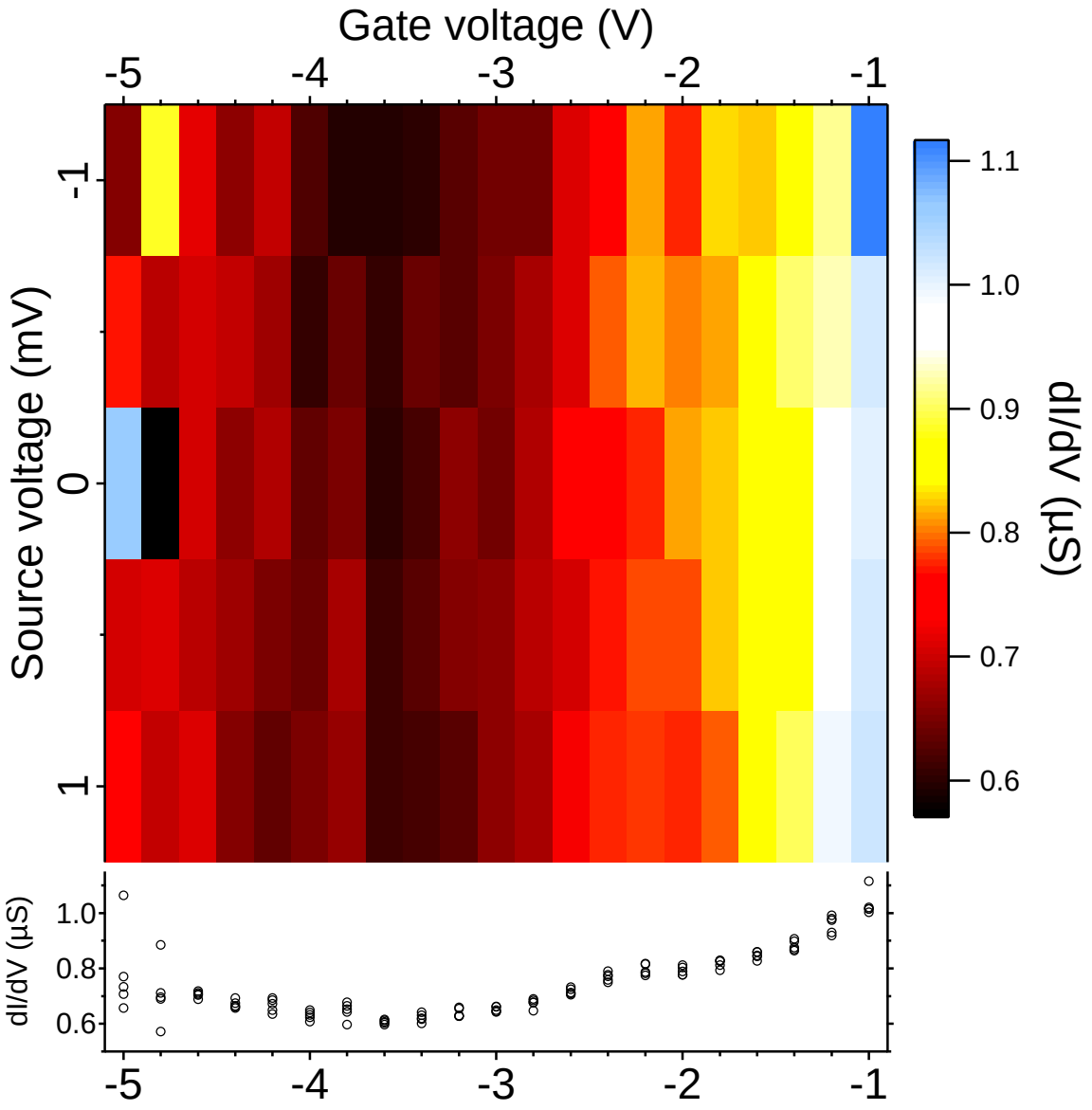

Figure 7.9: Room temperature dI/dV data for graphene nanoribbon L32 over different gate voltage and source voltage ranges. The bottom plot is the same data, plotted as dI/dV vs gate voltage.

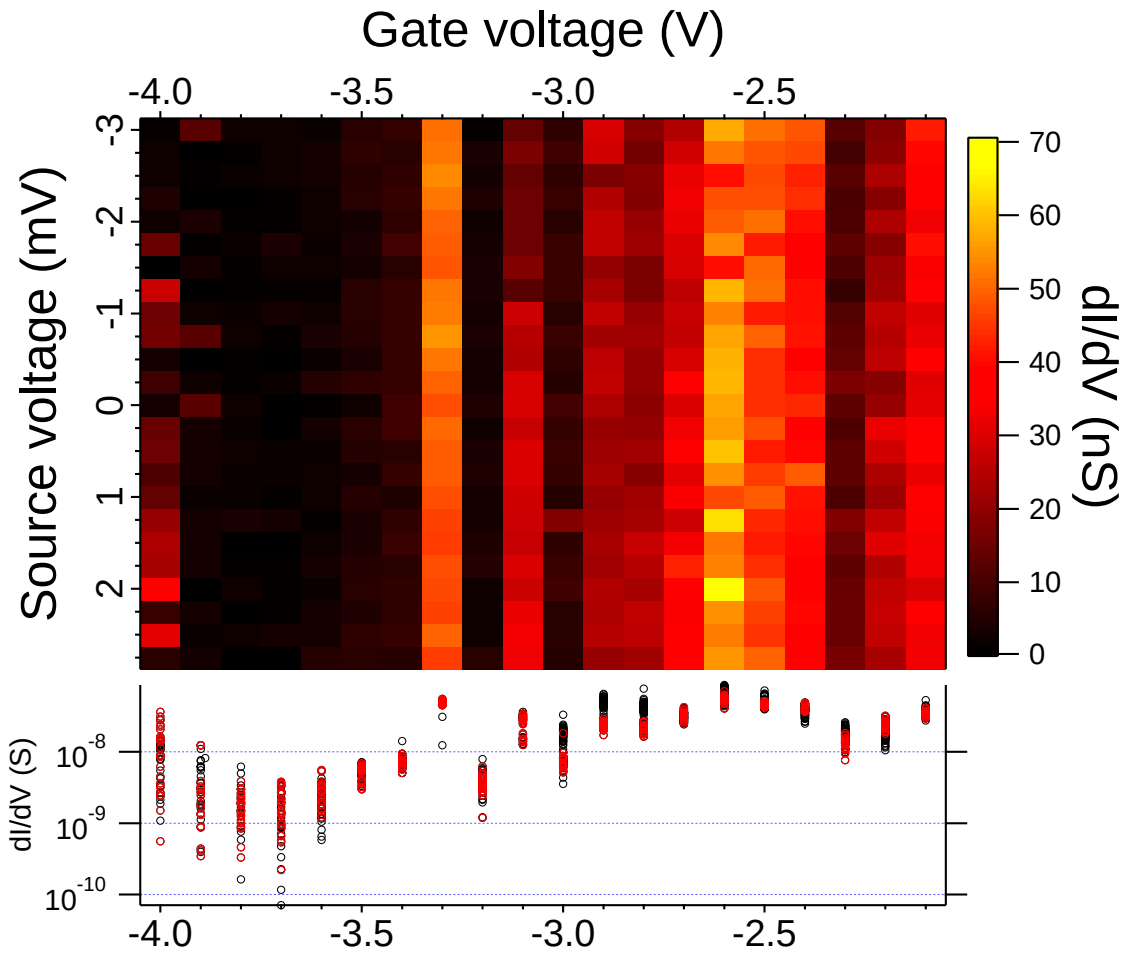

Figure 7.10: dI/dV data at 4 K for graphene nanoribbon L32 over a gate voltage range of -4 to -2 V. The bottom plot shows the data above in red and data from the other sweep directions in black.

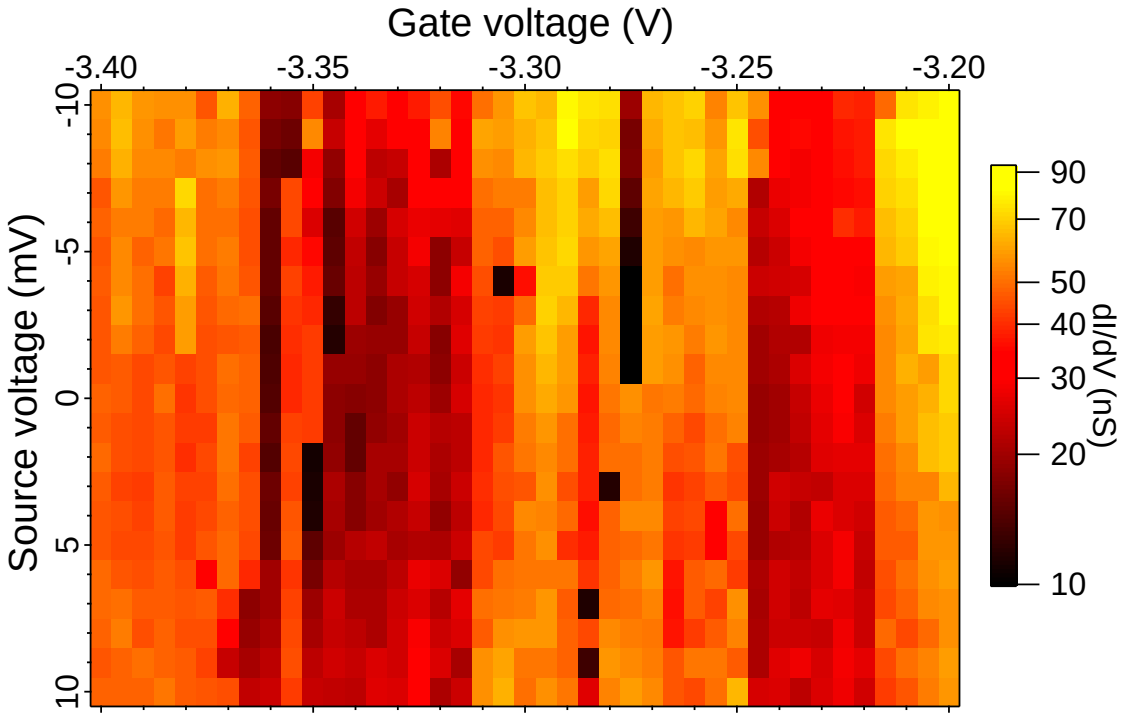

Figure 7.11: dI/dV data at 4 K for graphene nanoribbon L32 over a smaller gate voltage range, -3.4 to -3.2 V.

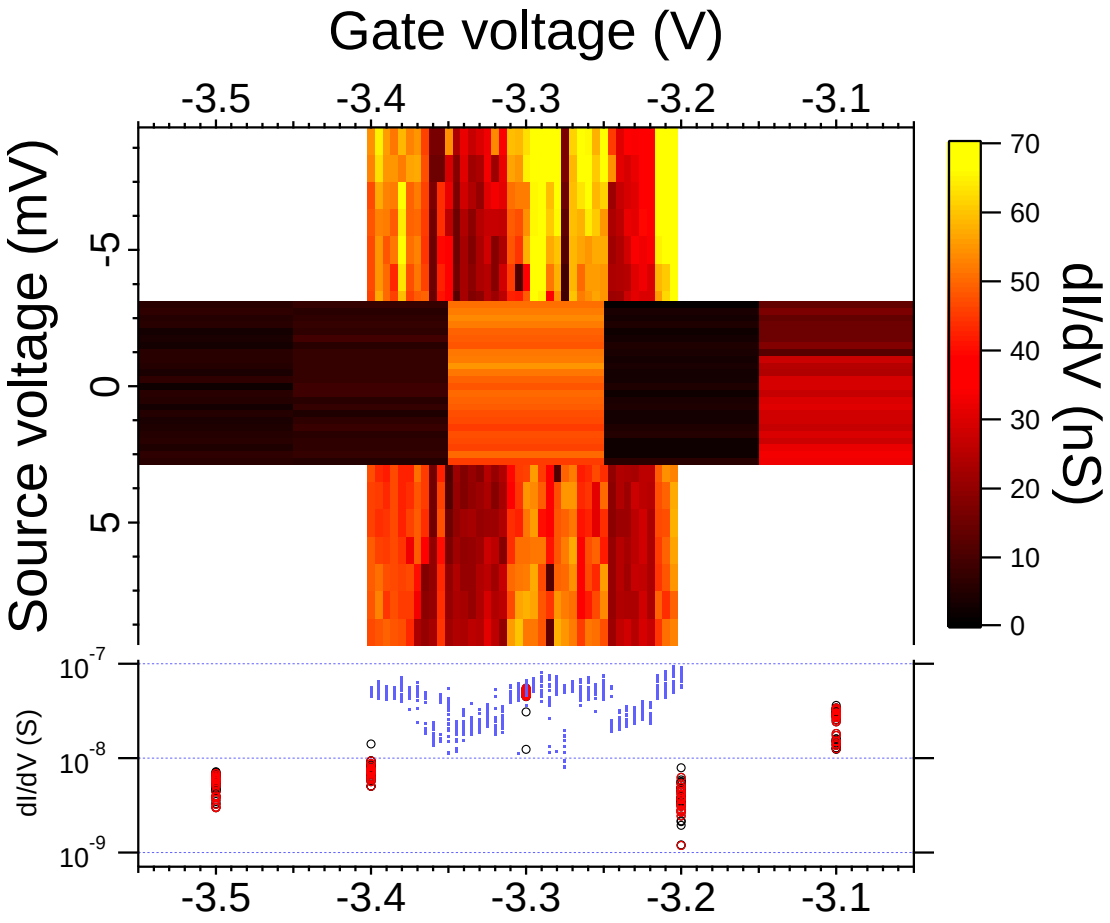

Figure 7.12: dI/dV data at 4 K for graphene nanoribbon L32, showing both wide and narrow gate sweep data. The bottom plot shows both sets of data.

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Appendix A

Graphene optical visibility

One interesting property of graphene is the visibility of even a single monolayer to the human eye when on dielectric substrates. CVD monolayers are wide enough to be seen with the naked eye; exfoliated monolayers can be seen under optical microscopes with no additional aids. Because this visibility is an interference effect, it only occurs for certain thicknesses of the underlying oxide. Three hundred nanometers is the most common thickness, as it provides good contrast and is thin enough to grow easily but not so thin that gate leakage becomes a common problem. This optical contrast is rather straightforward to derive and we will do so roughly following Blake et al. [129].

Assume that light of wavelength λ is incident from above on a stack of 3 different dielectrics, numbered 1 to 3 from top to bottom. The vacuum above we will label as "layer" 0, and we will assume layer 3 is very thick. The thickness and index of refraction of each layer i are given by d_i and n_i, respectively. This is shown schematically in figure A.1.

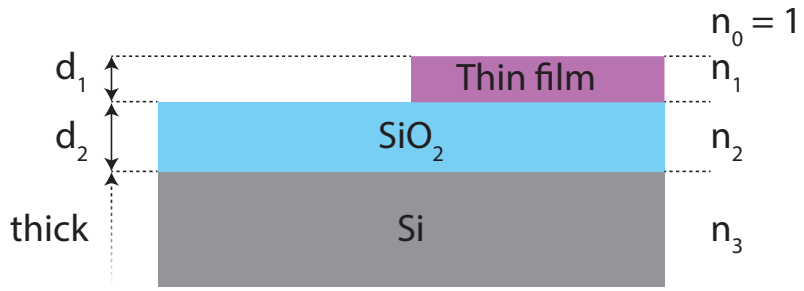


Figure A.1: Diagram of layers used in calculating optical visibility of thin films.

A.1 Constrast calculations

As stated in [129], the reflected intensity fraction is given by

$$R = \left| \frac{r_1 e^{i(\phi_1+\phi_2)} + r_2 e^{-i(\phi_1-\phi_2)} + r_3 e^{-i(\phi_1+\phi_2)} + r_1 r_2 r_3 e^{i(\phi_1-\phi_2)}}{e^{i(\phi_1+\phi_2)} + r_1 r_2 e^{-i(\phi_1-\phi_2)} + r_1 r_3 e^{-i(\phi_1+\phi_2)} + r_2 r_3 e^{i(\phi_1-\phi_2)}} \right|^2, \tag{A.1}$$

where each r is the relative index of refraction between two adjacent media

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1}, \qquad r_2 = \frac{n_1 - n_2}{n_1 + n_2}, \qquad r_3 = \frac{n_2 - n_3}{n_2 + n_3},$$

and ϕ_i is the path length through layer i in radians, given by $2\pi n_i d_i/\lambda$. While it is not mentioned by Blake et al. [129], this can be derived using the transfer matrix method common for thin film optics, and should hold generally for any two layers on a third substrate.

The fraction of light reflected is not enough to determine the visibility of thin flakes. For this, we must compare the value reflected from a location "on" a flake to one "off" the flake (or in this specific case, compare the reflectance for graphene on SiO_2 on silicon to that of the adjacent SiO_2 on silicon with no graphene). In the absence of graphene, equation A.1 reduces to

$$R_0 = \left| \frac{r_2 e^{i\phi_2} + r_3 e^{-i\phi_2}}{e^{i\phi_2} + r_2 r_3 e^{-i\phi_2}} \right|^2, \tag{A.2}$$

where we have called this no-graphene reflectance R_0. To quantify the visibility of the flake, we define the contrast C as

$$C = \frac{R_0 - R}{R_0}, \tag{A.3}$$

where R_0 and R both depend on the wavelength of incoming light as well as the relevant physical properties of the materials.

One can see that if the flake appears brighter than the underlying substrate at a given wavelength, the contrast will be negative. If it appears darker, the contrast will be positive.

We can now use these equations to calculate the contrast of monolayer graphene on a substrate. The wavelength λ and the oxide thickness d_2 are left as independent variables. The dielectric constants of all materials can be obtained from handbooks, but care should be taken to make sure that they are the in-plane optical dielectric constants, particularly for anisotropic layered structures.

We performed these calculations for three materials, graphene, hBN, and gallium selenide (GaSe), a layered semiconductor that we thought might have promise as a thin semiconductor material. We will begin here with calculations on graphene.

For graphite in the visible range, the complex index of refraction $n - ik$ is well approximated by $2.6 - 1.3i$ [129, 130]. Because the electric field is in the graphene plane, it seems reasonable to assume that the in-plane properties will be similar to those of graphite since the layers are weakly coupled.

For silicon dioxide, Blake et al. [129] use a value of $n(\lambda = 400 \text{ nm}) \approx 1.47$ but cite the Handbook of Optical Constants of Solids [130] which has $n(\lambda = 400 \text{ nm}) \approx 1.55$ and flat to within 1% over the optical range. The reason for this discrepancy is unclear, but we will stick with $n = 1.55$.

To maximize accuracy, we converted some the discrete data points to continuous functions that would interpolate the data points from [130]. For silicon, an empirical fit to [130] gives us:

$$n = 3.39 + 58100e^{-\lambda/36} + 6.23e^{-\lambda/246}$$
$$k = 0.011 + 0.422e^{-(\lambda-383)/10.5} + 0.380e^{-(\lambda-383)/65}.$$

The choice to use exponentials was merely for simplicity.

Figure A.2 shows some calculated contrast values for monolayer graphene on SiO_2. There is no scale, but the range is from approximately 0 to 0.15. Figure A.3 shows cross sections of figure A.2 for graphene on 300 nm of SiO_2 and for light with wavelength 550 nm (green).

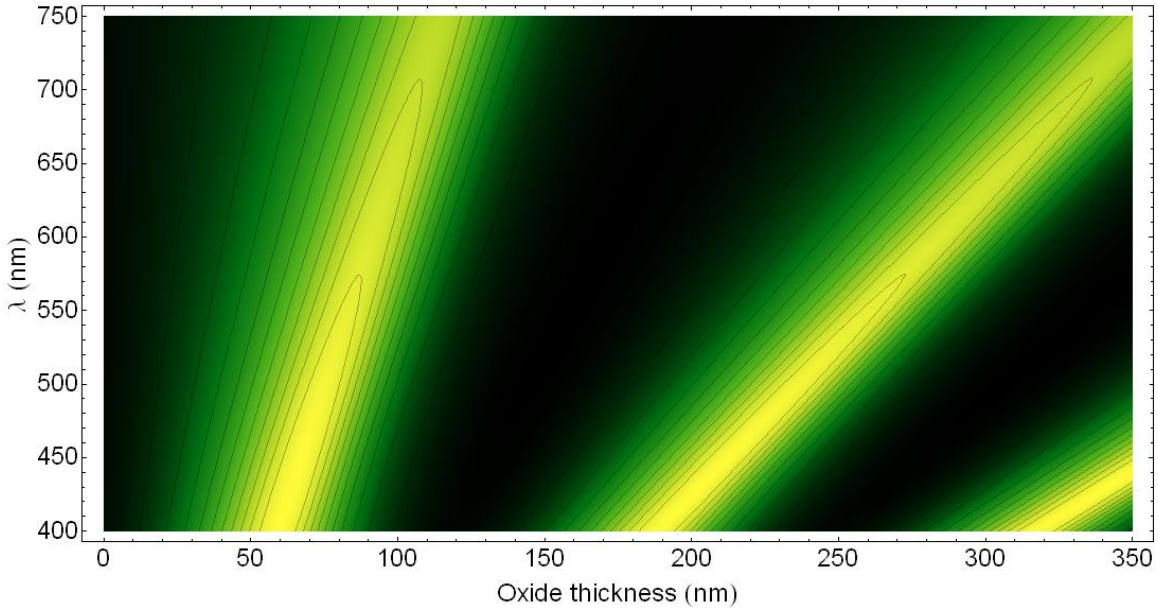


Figure A.2: Simulation of graphene contrast on an oxidized silicon wafer. The brightest regions have a contrast of about 0.15, the lowest are near zero.

These results match those calculated by other groups reasonably well [129].

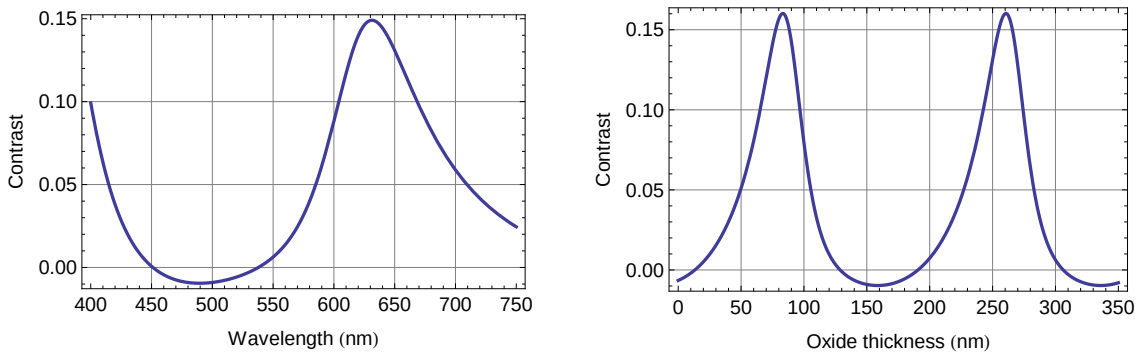


Figure A.3: Cross sections of the 2D plot in figure A.2 with 300 nm of SiO_2 (left) and $\lambda = 500$ nm (right).

We can also move to slightly more sophisticated calculations. The camera on the optical microscope is an mvBlueFox-121CU. The spectral response of the red, green, and blue channels can be estimated from the specifications sheet. We can then numerically integrate this against the wavelength-dependent contrast for a given oxide thickness and a spectral density of the light source to give a number for each RGB channel that should be proportional to the camera response. We can then multiply these by the known RGB color of bare oxide to simulate how the graphene layer should appear.

For simulating hBN contrast, we used a constant index of refraction of $n = 2.2$, following [59]. This is quite different from the measured values in [130], which range from 1.54-1.60 in the visible. However, because we are using hBN made by Dr. Taniguchi and Dr. Watanabe at NIMS, we will use the value measured by Gorbachev et al. [59] on the same hBN.

Note that even under optimal conditions, the contrast of a hBN monolayer is significantly lower than a graphene monolayer. These results are consistent with Gorbachev et al. [59].

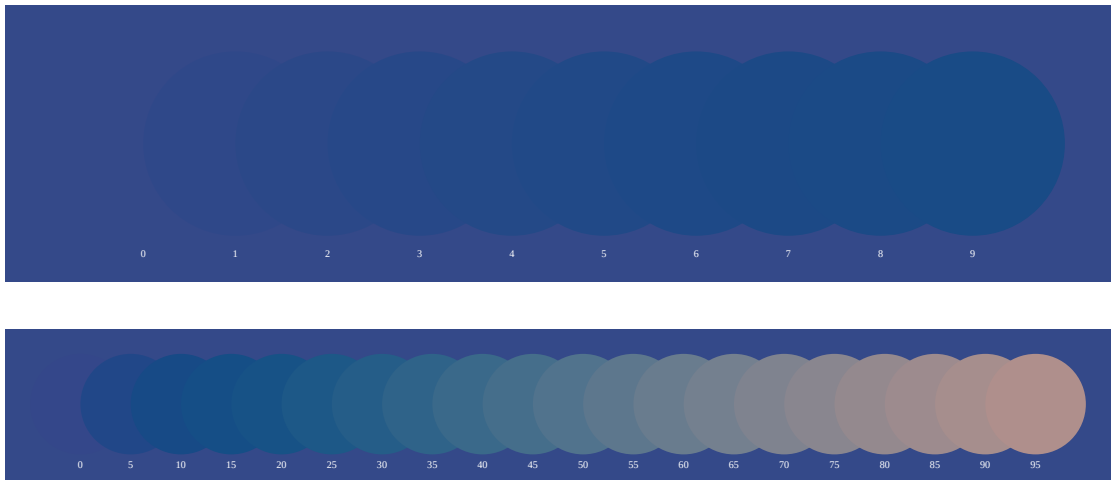


Figure A.4: Simulated optical image of graphene on 300 nm of SiO_2. The top row is 0 to 9 layers of graphene, and the bottom row is 0 to 95 layers. The contrast difference for few layers may not be obvious (or visible at all) depending on the method of display.

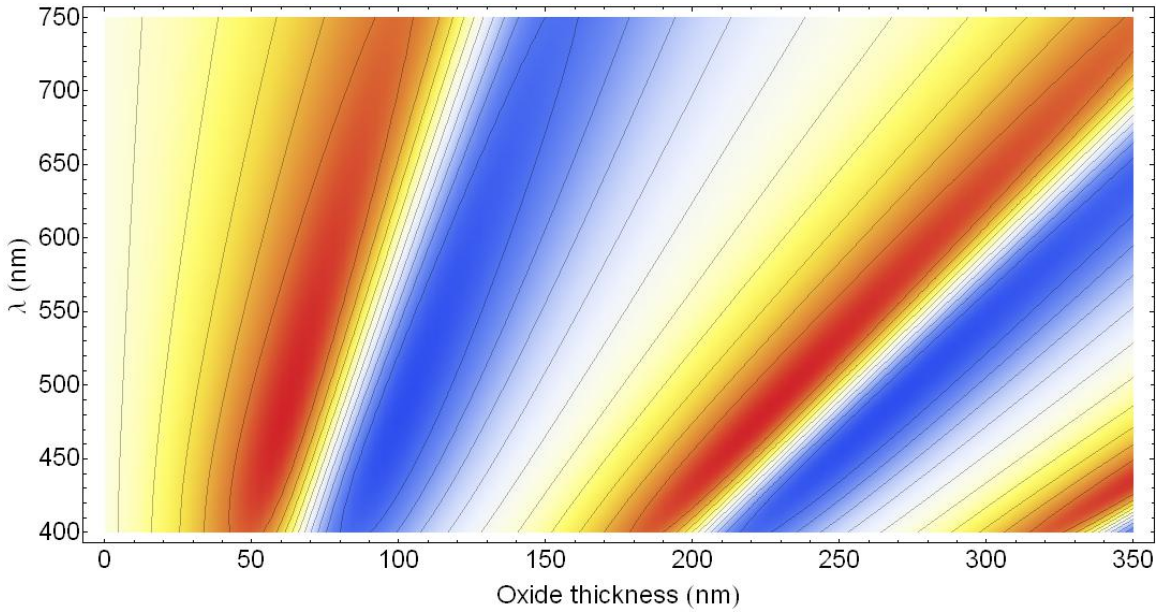


Figure A.5: Simulation of hBN contrast on an oxidized silicon wafer. The red regions have a contrast of $\sim$0.03 (darker than the SiO_2) and the blue regions have a contrast of about -0.3 (brighter than the SiO_2). The white regions have zero contrast.

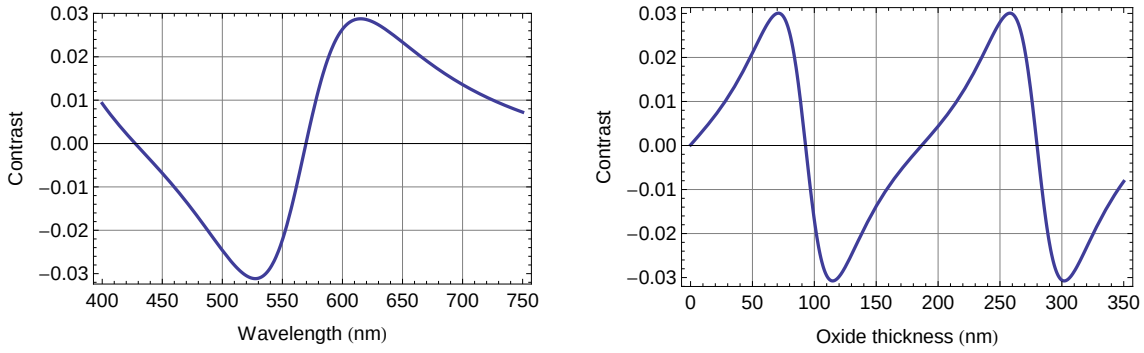


Figure A.6: Cross sections of the 2D plot in figure A.5 with 300 nm of SiO_2 (left) and $\lambda = 500$ nm (right).

Figure A.7: Simulated optical image of graphene on 300 nm of SiO_2. The top row is 0 to 9 layers of hBN, and the bottom row is 0 to 95 layers. Few-layer hBN is all but invisible in this simulation.

A.2 Mathematica code

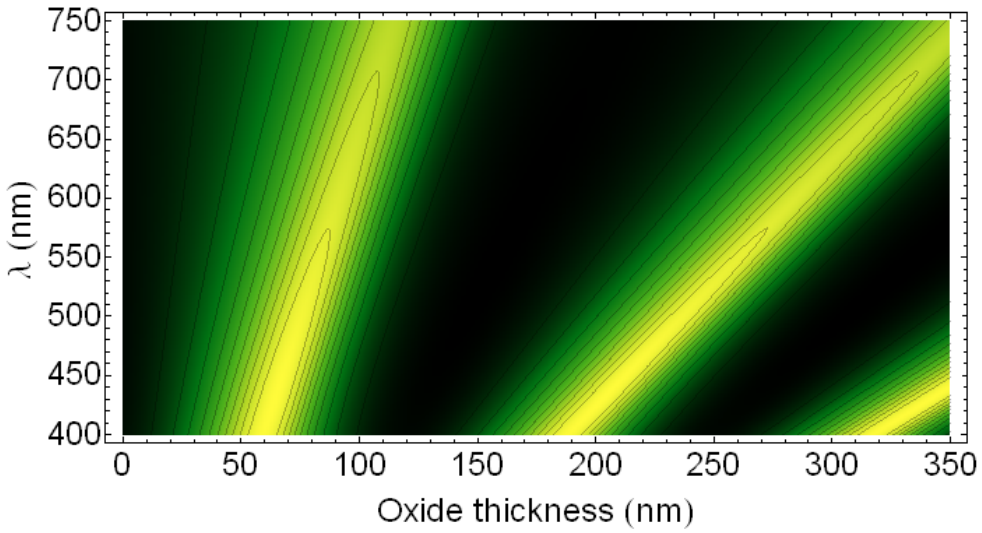
Below is some example code I wrote for Mathematica (in this case, version 8.0) that allows simulation of the optical contrast of thin films on oxidized silicon, which is extremely useful for gated thin film devices:

```
In[1]:= ClearAll["Global`*"]
In[2]:= (*This all sets up the physics for regions 0 (vacuum),
  1 (thin film of interest),
  2 (silicon dioxide),and 3 (silicon):  *)
  r1 = (n0 - n1) / (n0 + n1);
  r2 = (n1 - n2) / (n1 + n2);
  r3 = (n2 - n3) / (n2 + n3);
  ϕ1 = 2 π d1 n1 / λ;
  ϕ2 = 2 π d2 n2 / λ;
In[7]:= R := Abs[(r1 Exp[I (ϕ1 + ϕ2)] + r2 Exp[-I (ϕ1 - ϕ2)] +
        r3 Exp[-I (ϕ1 + ϕ2)] + r1 r2 r3 Exp[I (ϕ1 - ϕ2)]) /
      (Exp[I (ϕ1 + ϕ2)] + r1 r2 Exp[-I (ϕ1 - ϕ2)] +
        r1 r3 Exp[-I (ϕ1 + ϕ2)] + r2 r3 Exp[I (ϕ1 - ϕ2)])]^2
In[8]:= (*things that don't change between G and bare region*)
  n0 = 1; (*Vacuum*)
  n1 = 2.6 - 1.3 I; (*Graphene*)
  n2 = 1.55; (*SiO2*)
  n3 = 3.39 + 58100 E^(-λ / 36) + 6.23 E^(-λ / 246) -
     I (0.011 + 0.422 E^(-(λ - 383) / 10.5) +
        0.380 E^(-(λ - 383) / 65)); (*Silicon*)

In[12]:= R0 = R /. d1 → 0 ; (*no Graphene for reflectance R0*)
  Rg = R /. d1 → 0.337;(*Graphene thickness for reflectance Rg*)
In[14]:= Needs["PlotLegends`"]
  (*All of the "Rasterize[]" that follow are for PDF rendering
   for inside the thesis and are not generally necessary*)
```

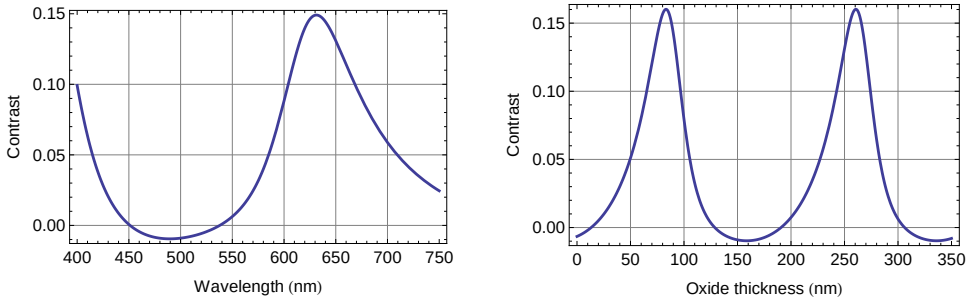
In[15]:=
```
Rasterize[
 DensityPlot[(R0 - Rg) / R0, {d2, 0, 350}, {λ, 400, 750},
  PlotPoints → 200, ColorFunction → "AvocadoColors",
  MeshFunctions → {#3 &}, Mesh → 10, AspectRatio → 1 / 2,
  FrameLabel → {"Oxide thickness (nm)", "λ (nm)"},
  LabelStyle → Directive[Large, FontFamily → "Helvetica"]]
 , ImageSize → 700]
```

Out[15]=



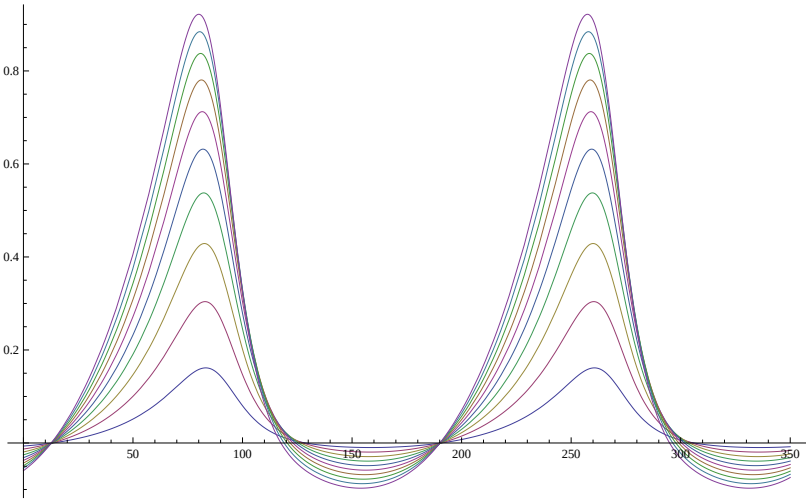
In[16]:=
```
(* Plot slices through 300 nm
 thickness and 550 nm wavelength *)
GraphicsGrid[{{Plot[(R0 - Rg) / R0 /. d2 → 300,
    {λ, 400, 750}, Frame → True, GridLines -> Automatic,
    FrameLabel → {"Wavelength (nm)", "Contrast"},
    LabelStyle → Directive[Medium, FontFamily → "Helvetica"],
    PlotStyle → Directive[Thick]], Plot[(R0 - Rg) / R0 /. λ → 550,
    {d2, 0, 350}, Frame → True, GridLines -> Automatic,
    FrameLabel → {"Oxide thickness (nm)", "Contrast"},
    LabelStyle → Directive[Medium, FontFamily → "Helvetica"],
    PlotStyle → Directive[Thick]]}}]
```

Out[16]=



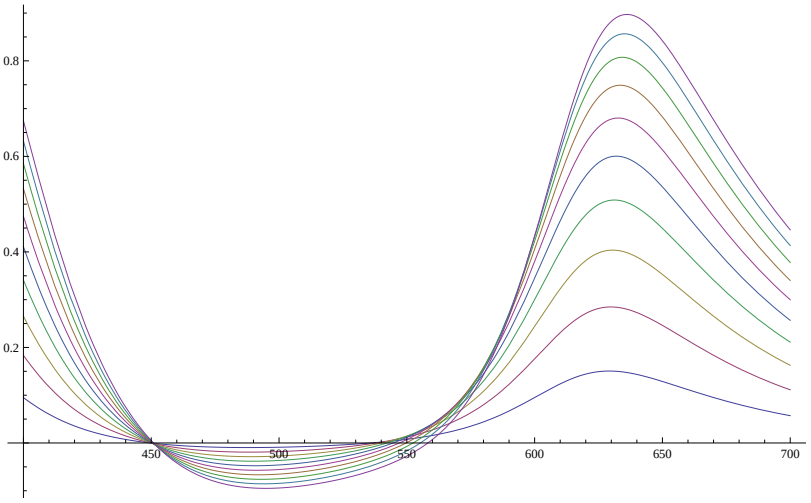
In[17]:=
```
(*Contrast curves vs oxide thickness at λ=550 nm *)
Plot[Evaluate@Table[
   (R0 - R) / R0 /. λ → 550 /. d1 → n * 0.34, {n, 1, 10}], {d2, 0, 350}]
```

Out[17]=



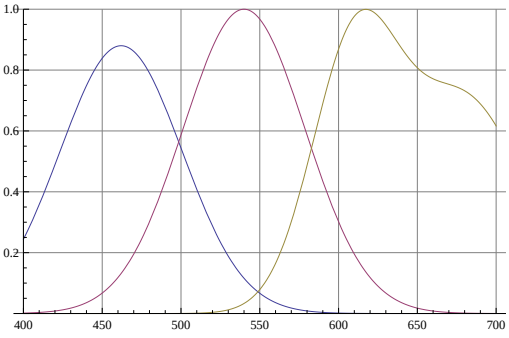
In[18]:=
```
(*Contrast curves vs wavelength
 at oxide thickness of 299 nm *)
Plot[Evaluate@Table[(R0 - R) / R0 /. d2 → 299 /. d1 → n * 0.34,
   {n, 1, 10}], {λ, 400, 700}]
```

Out[18]=



In[19]:=
```
(*Response of R, G,
and B channels of Zettl group optical microscope camera*)
FB = 0.88 * Exp[-(λ - 462)^2 / 3000];
FG = Exp[-(λ - 540)^2 / 3000];
FR = 0.84 Exp[-(λ - 610)^2 / 1500] + 0.7 Exp[-(λ - 680)^2 / 3000];
Plot[{FB, FG, FR}, {λ, 400, 700},
 PlotRange → {0, 1}, GridLines → Automatic]
```

Out[22]=

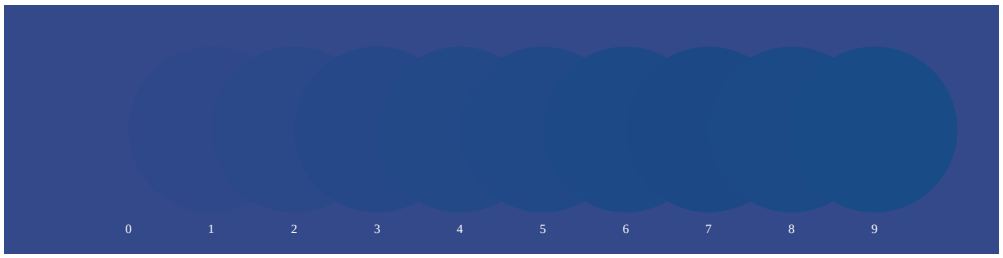


In[23]:=
```
(*Make a matrix of RGB contrasts for 0-
 9 layers of graphene*)
ProgressIndicator[Dynamic[n], {0, 20}]
MAT = Table[
   Re[(NIntegrate[CC * R0 /. d2 → 300, {λ, 400, 700}] - NIntegrate[
        CC * R /. d2 → 300 /. d1 → n * 0.34, {λ, 400, 700}]) /
     NIntegrate[CC * R0 /. d2 → 300, {λ, 400, 700}]],
   {n, 0, 10}, {CC, {FR, FG, FB}}];
```

Out[23]=

In[25]:=
```
(*Display simulated color of 0-9 layers,
starting with bare oxide = {52,73,138} *)
Graphics[{RGBColor[{52 / 256, 73 / 256, 138 / 256}],
  Rectangle[{-.5, -1.5}, {11.5, 1.5}],
  Table[{RGBColor[(1 - MAT[[n]]) * {52 / 256, 73 / 256, 138 / 256}],
    Disk[{n, 0}], White, Inset[n - 1, {n, -1.2}]}, {n, 1, 10}]}]
```

Out[25]=



Appendix B

Fabrication recipes

B.1 Lithography

For all lithography performed for the research in this dissertation, the following recipe was followed unless otherwise specified.

1. The sample was coated with poly(methyl methacrylate) (PMMA) by spinning a commercially availably 4% PMMA solution in anisole (MicroChem 950PMMA A4) onto the sample at ∼3000 rpm.[1]

2. The sample was placed face-up on a clean glass slide on an adjacent hot plate, set to 185°C. This was to both remove the anisole solvent in the PMMA and to bring the PMMA layer above its glass transition temperature. It was left on the hot plate for 20 minutes[2] before removing the slide and substrate to cool.

3. The surface of the sample was scratched with tweezers or a micromanipulator probe near the large alignment marks. This provided surface features to focus on and made a "trail" to the alignment marks that could be followed in the SEM without exposing the bulk of the sample.

4. The sample was placed in the Zettl group SEM. After beam current measurement, the SEM was focused using the scratches and rotated correctly using "Align x" or "Align feature" commands on the alignment marks.

5. I started the NPGS run file, with non-stop writing mode on, global rotation correction off, and X-Y focus control off.[3]

[1] The resulting thickness is not extremely sensitive to angular speed, see spin curves available from MicroChem [131].

[2] Twenty minutes may be more than necessary; MicroChem recommends a pre-bake of only 60-90 seconds [131]. However, short bake times had been correlated with subsequent liftoff problems, and, coincidence or not, I have maintained the 20 minute bake.

[3] X-Y focus control can definitely improve lithography results, but for flat samples a few mm across with micron-scale features, it does not seem to be necessary.

6. NPGS alignment was performed with the following settings:

   Spot 1, 200 nm spacing, 2 reads. Magnification set ∼10% lower than maximum allowed by NPGS field-of-view calculation.[4]

7. NPGS pattern was written, with small features (closest to the device) at spot 1 and the rest (leads and contact pads) at spot 5. The parameters are shown in the following table:

	Magnification	Spacing	Area dose
Spot 1	∼10-20% below max	15 nm	350 µC/cm^2
Spot 5	∼10-20% below max	50 nm	375 µC/cm^2

   There are a few errors during the NPGS process that can occur at this time. Problems with the pattern file can generally be found ahead of time by processing the run file in error check mode. (This catches problems like polygons that are not closed or have self-intersecting boundaries.) Problems during the actual pattern writing that were not caught by an error check are generally due to alignment shifts that are too large. These can be alleviated by making sure the magnification is low enough to give a good margin of error.

8. The sample was removed from the SEM, and kept as dark as possible until ready to develop.[5]

9. The sample was developed by immersion in developer consisting of one part methyl isobutyl ketone (MIBK) and three parts isopropyl alcohol (IPA) with light agitation for 120 seconds. The sample was then transferred to IPA for no less than 30 seconds, and blown dry with a nitrogen gun.

10. The resulting PMMA mask was inspected in the optical microscope located in 123 Birge. Common (and potentially fatal-to-sample) problems at this stage could include:

    - Overexposure: features are enlarged and corners are rounded by dilation.
    - Underexposure: PMMA remains on inside of corners and other extreme edges of pattern.
    - SEM magnification set wrong (i.e. anything other than "Display"): features are wrong size.

[4] Ideally this is the same magnification as the subsequent spot 1 writing, to prevent shifts between different magnifications.

[5] I have not tested the effects of fluorescent lights or direct sunlight on PMMA masks, but it is generally trivial to keep them away from such lights for all but the shortest times.

- Blanker not functioning: unexpected circles appear at center of pattern location.
- Alignment failure: pattern is rotated or shifted relative to desired location.
- "IPA" was actually acetone: PMMA is no longer on substrate.

There are also undesirable occurrences with less fatal effects on the sample:

- Alignment exposure: alignment marks are noticeably exposed, which is not a problem unless exposed region overlaps an area where the mask must stay intact.
- Debris within exposed regions: this is not a problem unless they cause loss of continuity.

11. The sample was now ready for deposition, etching, or other processing.

B.2 Graphene etching

Due to graphene's chemical inertness, it is not etched by most wet chemical processes. However, removal of graphene is necessary for patterning devices.

We found oxygen etching in the Zettl group reactive ion etcher to be the quickest and easiest way to remove graphene. This recipe was used for etching CVD graphene on the copper catalyst as well as for patterned etching of devices. The settings below were used for most etches:

Gas	Flow rate	Power	Time
O_2	50 sccm	50 W	20 sec

Often, the 50 sccm of O_2 was split between the two mass flow controllers as 25+25 sccm. This was initially done due to a suspected leak in one of the MFCs and never changed. Putting one gas through two MFCs in this fashion is specifically contraindicated in the RIE manual.

B.3 Other notes

- I strongly recommend NPGS for mapping of prospective devices, particularly when dealing with larger numbers of devices (e.g. a 4x4 array). There are NPGS runfiles that use PGImage to do this.
- TIFFs used in DesignCad must be 8-bit and not 16-bit, but the TIFFs collected by our PGImage scripts are 16-bit. Some conversion is required. ■