Fluxless Tin Bonding Process With Suppressed Intermetallic Growth

Shou-Jen Hsu and Chin C. Lee

***Abstract*— Soldering is a process that joins two metal parts with a low-melting-point metal or alloy, called solder. It is widely recognized that intermetallic compound (IMC) formation is essential for the solder to bond to metals. The IMC layer grows during soldering. It grows further during usage, in particular, at temperature near the solder melting temperature. Extensive IMC growth can result in reliability issues. A reason is that IMC is much less ductile than the solder and does not deform as much as the solder to manage the coefficient of thermal expansion mismatch between the parts joined. In this paper, we looked into and developed a soldering process to fabricate IMC-less solder joints. The fundamental concept is to choose a barrier metal that can bond to solder without forming IMC with the solder. With our experience and Cr–Sn phase diagram, Cr is selected as the barrier metal. Several bonding experiments have been performed and the preliminary results show that high quality Sn joints could be produced with a little IMC formation before high-temperature aging. After aging at homologous temperature of 0.9 of Sn for 100–200 h, Cu_6Sn_5 and Cu_3Sn IMCs are observed. They are caused by the penetration of molten Sn through microcracks or pinholes on the Cr layer to react with the underlying Cu. In production environment, the density of microcracks and pinholes can be greatly reduced to inhibit IMC growth, making the realization of solder joints without IMC a possibility.**

***Index Terms*— Intermetallic, soldering, tin.**

I. Introduction

SOLDERING is a metallurgical bonding process that joins two metals together using another metal or alloy having relatively low melting point and good wettablility. It has been widely used at different levels of electronics packaging and serves the purposes of electrical connection, heat transport, and mechanical support [1]–[3]. It is well known that solder bonds to metals by forming intermetallic compounds (IMCs) on the interfaces. The IMCs formed between copper (Cu) and tin (Sn)-containing solder are Cu_6Sn_5 and Cu_3Sn [4]. The Cu_3Sn grows adjacent to Cu and Cu_6Sn_5 forms adjacent to the solder. Likewise, the only IMC detected between nickel (Ni) and Sn-containing solder is Ni_3Sn_4 [3]. The IMC forms in layer structure and grows gradually during reflow processes or the service life.

It was well recognized that excessive intermetallic growth could deteriorate the joint reliability [5], [6]. IMCs do not deform so easily as the solder in providing plastic strain to accommodate mismatch in the coefficient of thermal expansion (CTE). Extensive IMC growth reduces the solder thickness and thus increases the shear strain of the bonded structure. Furthermore, metal/IMC interfaces often act as sites for crack initiation and propagation. It has been reported that, due to the difference in the intrinsic diffusivity of Cu and Sn in Cu_3Sn layer, Kirkendall voids form at the Cu/Cu_3Sn interface or within the Cu_3Sn layer [7]–[11]. These voids raise reliability concern because excessive void formation increases the possibility of joint fracture. In addition, spalling of Cu_3Sn or $(Ni,Cu)_3Sn_4$ of Cu was observed between high-lead 95Pb5Sn solder and Cu or Ti/Cu/Ni under bump metallization [12], [13]. Accordingly, the electronic industry has attempted various techniques to reduce the IMC growth. An obvious approach is to solder at the lowest possible temperature for the shortest possible time [14]. The most successful technique is to coat Cu electrodes with a Ni layer [2], [15]. Popular Ni coating methods are electrolytic plating process and electroless Ni immersion gold process. During the soldering process, molten Sn reacts with Ni to form Ni_3Sn_4, which grows much more slowly compared with Cu_6Sn_5 [15], [16]. In extensive IMC growth, the entire Ni layer is consumed and turned into Ni_3Sn_4, which now observes Cu electrodes. Therefore, IMCs, such as $(Ni,Cu)_6Sn_5$ and $(Ni,Cu)_3Sn$, show up [17].

In many applications, higher solder joint operating temperature provides an edge. A guideline for the maximum operation temperature of solder joints is at the homologous temperature of 0.8 [18]. At this temperature, even the aforementioned Ni coating method is not good enough. Thus, we searched for techniques that prevent IMC growth but a little is yet reported. However, the results [19]–[21] reported by our group suggest that Sn solder can strongly bond to the Cr deposited on silicon (Si) chip without forming IMC at the Sn/Cr/Si interface. To evaluate this technique in high-power devices, alumina substrates with direct-bonded Cu (DBC) are selected for bonding study. DBC alumina substrate has excellent thermal conductivity, high electrical isolation, and lower CTE, making it widely used in high-power electronics [22]. In this paper, DBC alumina substrates are bonded to Cu substrates using fluxless Sn process. The bonded samples are annealed at 182 °C, corresponding to 0.9 homologous temperature of tin, for different times to investigate the IMC growth. The samples are then examined using scanning electron microscope (SEM) and

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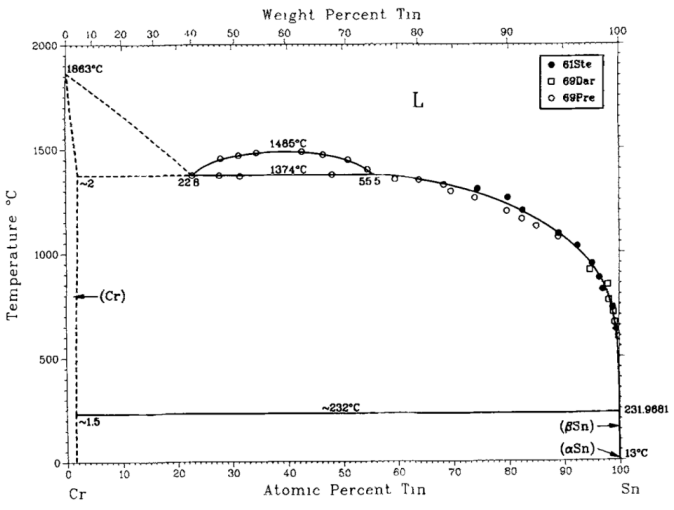


Fig. 1. Cr–Sn binary phase diagram [24].

energy-dispersive X-ray (EDX). In the following, the design concept and experimental procedures are presented. The experimental results are reported and discussed. A summary is then given.

II. Design Concept and Experimental Procedures

The design concept is first presented. Our previous experimental results have shown that Sn strongly bonds to Si chips coated with Cr [19]–[21]. Sn atoms bond to Cr atoms without forming IMC at the Si/Cr/Sn interface. Fig. 1 shows the Cr–Sn phase diagram [23]. It is observed that Cr and Sn do not react to form intermetallics. The solubility of Cr in molten Sn is only 3×10^{-4} at. % at 232 °C. Furthermore, the solubility of Sn in solid Cr is approximately 2 at. % Sn even at temperature as high as 1374 °C. Accordingly, Cr is selected as the barrier metal between Sn and Cu to inhibit IMC growth. Alumina with DBC is deposited with thin Cr and Cu layers. Cu substrates are also coated with thin Cr and Cu. The alumina substrate is bonded to the Cu substrate using fluxless Sn process. The samples are annealed at 182 °C, corresponding to homologous temperature of 0.9 for Sn, for different times to evaluate the IMC growth.

Cu substrates of 25.4 mm × 12.7 mm × 0.8 mm (width × length × thickness) are cut from 99.9% mirror-finished Cu sheet. Zirconium-doped alumina substrates of 15.66 mm × 20.07 mm × 0.25 mm (width × length × thickness) have DBC of 15.54 mm × 19.05 mm × 0.20 mm (width × length × thickness) on both sides. The Cu substrates and DBC alumina substrates are degreased with acetone and then etched in acetic acid at 35 °C to remove native oxide. Both the Cu substrate and the DBC alumina substrate are deposited with Cr and Cu sequentially by E-beam evaporation in a single run without breaking the vacuum. The Cr layer is employed as the barrier layer that blocks the liquid–solid reaction between molten Sn and the DBC or between molten Sn and Cu substrate during the bonding process. Cr layer of different thickness is used to examine its blocking ability versus thickness. The thin Cu deposited over the Cr layer protects the Cr layer from oxidation and also acts as seed layer in the subsequent electroplating step. The Cu substrates with Cr/Cu are electroplated with 70-μm-thick Sn in a stannous bath at 40 °C. During the bonding process, the DBC alumina substrate and the as-plated Cu substrate are held together with two 50-μm-thick Cu spacers in between to control the Sn joint thickness. The assembly is mounted on a graphite platform inside a chamber. A pressure of 25 psi is applied on the assembly to ensure intimate contact. The chamber is pumped down to 80 mtorrs and the graphite platform was then heated. The bonding process is conducted between 227 °C and 240 °C with different reflow times. The heating rate and the cooling rate are is 0.16 °C/s and 0.06 °C/s for the sample with reflow time of 290 s, and the heating rate and the cooling rate are 0.16 °C/s and 0.13 °C/s for the sample with reflow time of 180 s. After bonding, the heater is turned off and the assembly is allowed to cool down naturally to room temperature in vacuum environment. No flux is applied during the bonding process.

TABLE I
Samples of DBC Alumina Substrate Bonded to Cu Substrate Using Fluxless Sn at 240 °C Reflow Temperature

Sample designation	Cr thickness (nm)	Cu thickness (nm)	Reflow time (seconds)	Aging temperature (°C)	Aging time (hours)
A	100	200	290	-	-
B	500	100	180	-	-
C	500	100	180	182	10
D	500	100	180	182	100
E	500	100	180	182	200

It is well known that IMCs form during the soldering process by liquid–solid reaction. The IMCs grow further during multiple solder reflows. Afterward, the IMCs continue to grow during the service life of the electronic devices. This IMC growth during usage can be severe when the service temperature is high. To investigate the time-dependent solid-state IMC growth mechanism at the joint interfaces, several samples are subjected to accelerated aging test at various aging time at 182 °C, corresponding to Sn homologous temperature of 0.9. Table I lists a series of samples made with different Cr/Cu thicknesses, different reflow time, and various aging time. The microstructures are examined by SEM equipped with a backscattered electron image detector. The chemical compositions are analyzed using EDX spectroscopy. The bonded samples are mounted in epoxy, sectioned using slow-speed diamond saw, ground with 800 and 1200 grit SiC paper, and mechanically polished with alumina suspension to prepare the cross-sectional SEM samples.

III. Experimental Results and Discussion

In the first bonding design, designated as sample A in Table I, the thickness of E-beam deposited Cr and Cu is 100 and 200 nm, respectively. The DBC alumina substrate was bonded to Cu substrates under the condition described in the previous section. Fig. 2 shows the cross-sectional SEM images of the sample. As can be observed in Fig. 2(a), the DBC alumina substrate is well bonded to the Cu substrate. It is also observed that, in Fig. 2(c) and (d), IMC layers are formed at the DBC/Cr/Sn interface and the Sn/Cr/Cu substrate interface.

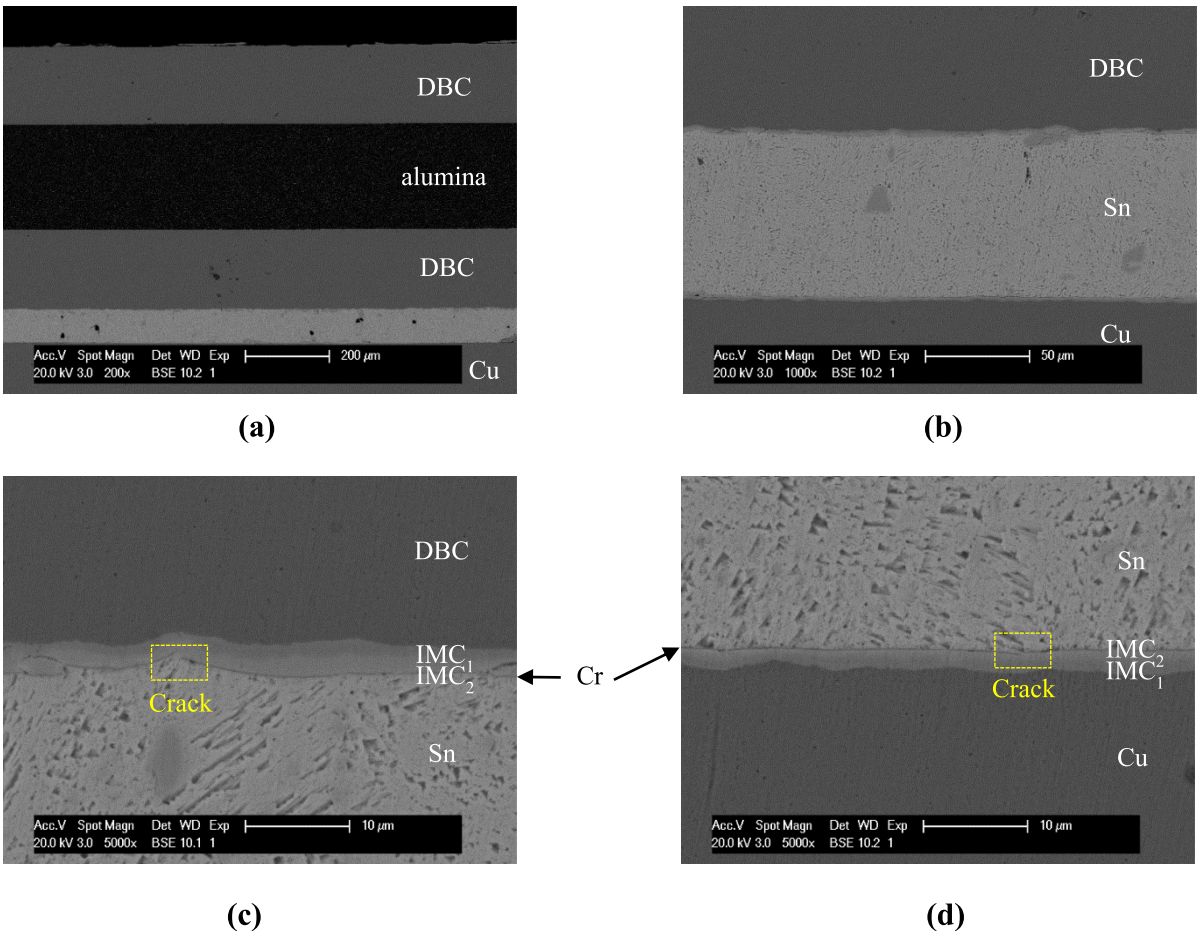


Fig. 2. Cross-sectional SEM images of sample A described in Table I at (a) low magnification (200×), (b) low magnification (1000×), (c) high magnification (5000×) at DBC/Cr/Sn interface, and (d) high magnification (5000×) at Sn/Cr/Cu substrate interface.

TABLE II
TYPICAL CTE VALUES OF THE MATERIALS [23]

Materials	Coefficient of thermal expansion (ppm/°C)
DBC alumina substrate	9.3
Cu substrate	17
Cr	4.9
Sn	22

The IMC layer thickness is about 3–4 μm at the DBC/Sn interface and 2–3 μm at the Sn/Cu substrate interface. Each IMC layer includes two distinct sublayers that are comprised of different IMCs. As shown in Fig. 2(c) and (d), there are some cracks within the thin Cr layer. It was suspected that the cracks formed during the heating and cooling processes since there is considerable CTE mismatch between Cr and DBC alumina substrate or between Cr and Cu substrate. Table II lists the typical CTE values of the materials [23]. Therefore, a Cr layer of 100 nm is too thin and too fragile to withstand the deformation because Cu has larger expansion or contraction than Cr during the soldering process. During the bonding process, the molten Sn penetrates through the cracks in the Cr layer to reach the Cu layer, thus forming IMC layers across the entire interfaces. This observation provides a clue that the Cr layer is indeed a critical factor.

To strengthen the Cr layer, its thickness was increased from 100 to 500 nm. Prior to the bonding experiment, a Cu substrate E-beam deposited with 500-nm Cr and 100-nm Cu, and electroplated with 30-μm Sn layer was first examined using SEM. Fig. 3 shows the cross-sectional images of an as-deposited sample. The 500-nm Cr layer between Sn and Cu substrate is clearly observed. Its thickness is uniform. The top surface of the electroplated Sn layer is uneven due to the limitation of the electroplating process. The second bonding design was then implemented. The sample was designated as sample B in Table I. The DBC alumina substrate was bonded to Cu substrates under the similar condition as in sample A, whereas the reflow time was decreased from 290 to 180 s. Fig. 4 shows the cross-sectional SEM images of sample B. No voids or gaps are found, showing that the DBC alumina substrate is well bonded to the Cu substrate all over the cross section. It is worth noting that there are no distinct IMC layers formed at the interfaces. The IMC formation is localized at a few locations on the DBC/Cr/Sn interface. The locations are marked as types I and II. Type I represents IMC formation between the Cr and Sn layers. It is caused by the diffusion of

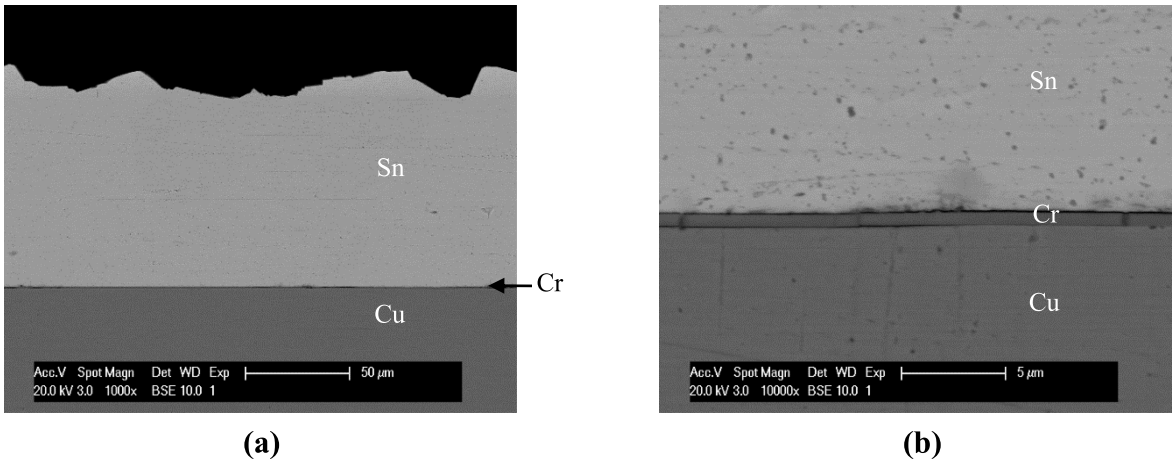


Fig. 3. Cross-sectional SEM images of a typical as-plated Cu substrate at (a) low magnification (1000×) and (b) high magnification (10000×). The substrate was E-beam deposited with 500-nm Cr and 100-nm Cu and was electroplated with 30-μm Sn.

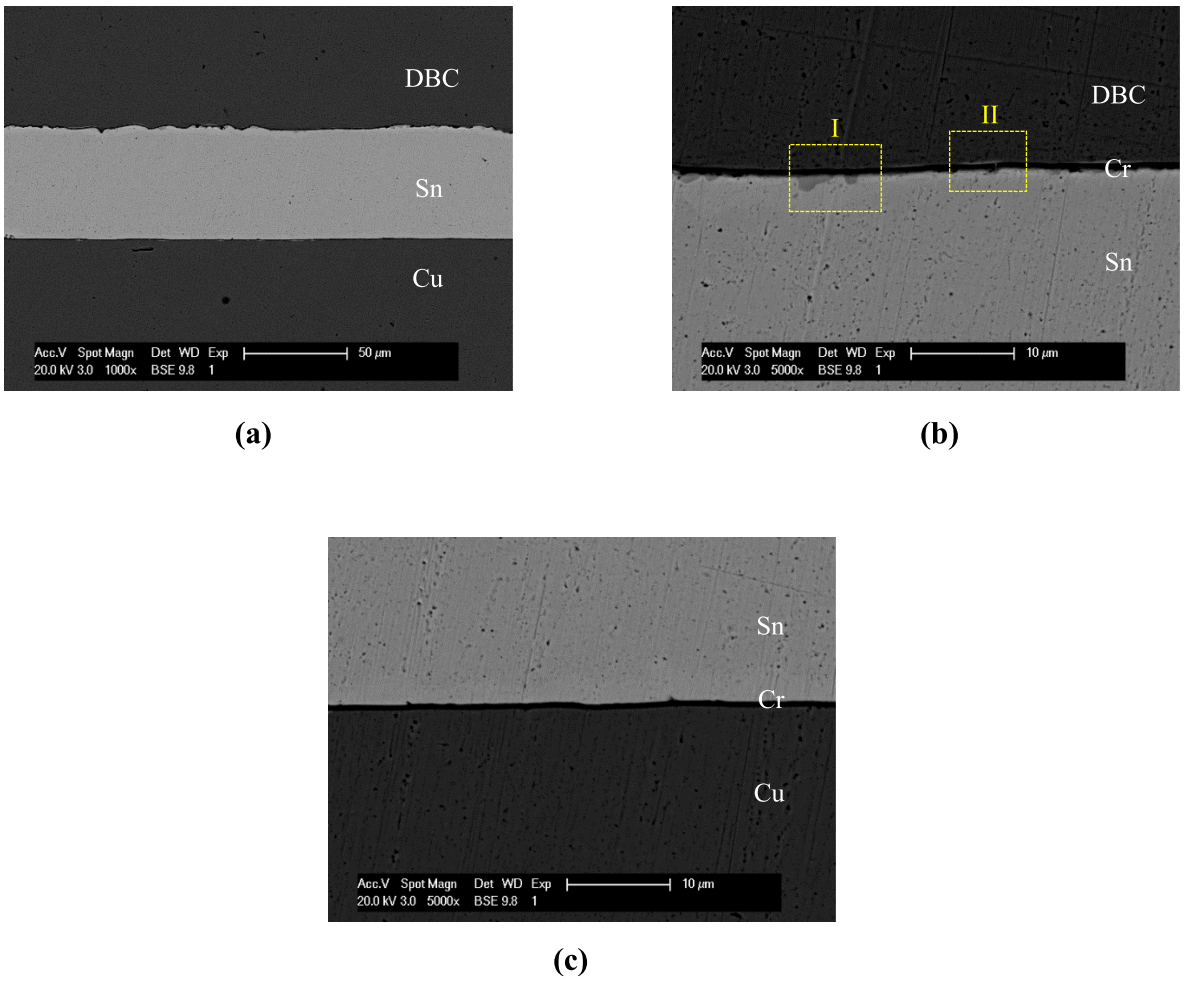


Fig. 4. Cross-sectional SEM images of sample B described in Table I at (a) low magnification (1000×), (b) high magnification (5000×) at DBC/Cr/Sn interface, and (c) high magnification (5000×) at Sn/Cr/Cu substrate interface.

Cu atoms through a microcrack or pinhole in the Cr layer to reach and react with the molten Sn. Type II represents IMC formation between the Cr and Cu layers. It is caused by diffusion of molten Sn through a microcrack or pinhole in the Cr layer to reach the Cu layer and react with it. Other than a few localized IMC formations, there is no IMC along the interface between Cu and Cr and that between Cr and Sn. Fig. 5 shows the EDX element mappings of sample B. Distinct

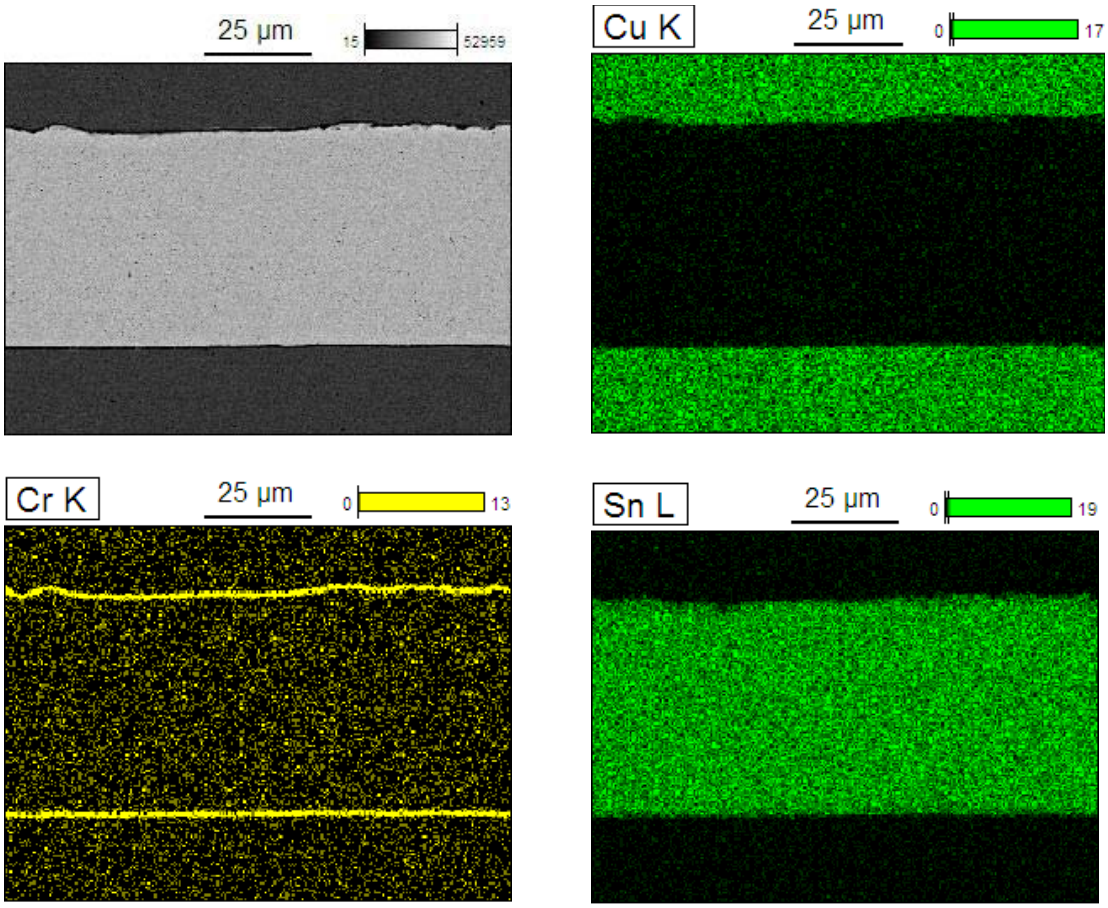


Fig. 5. Cross-sectional SEM image and element mappings of sample B described in Table I.

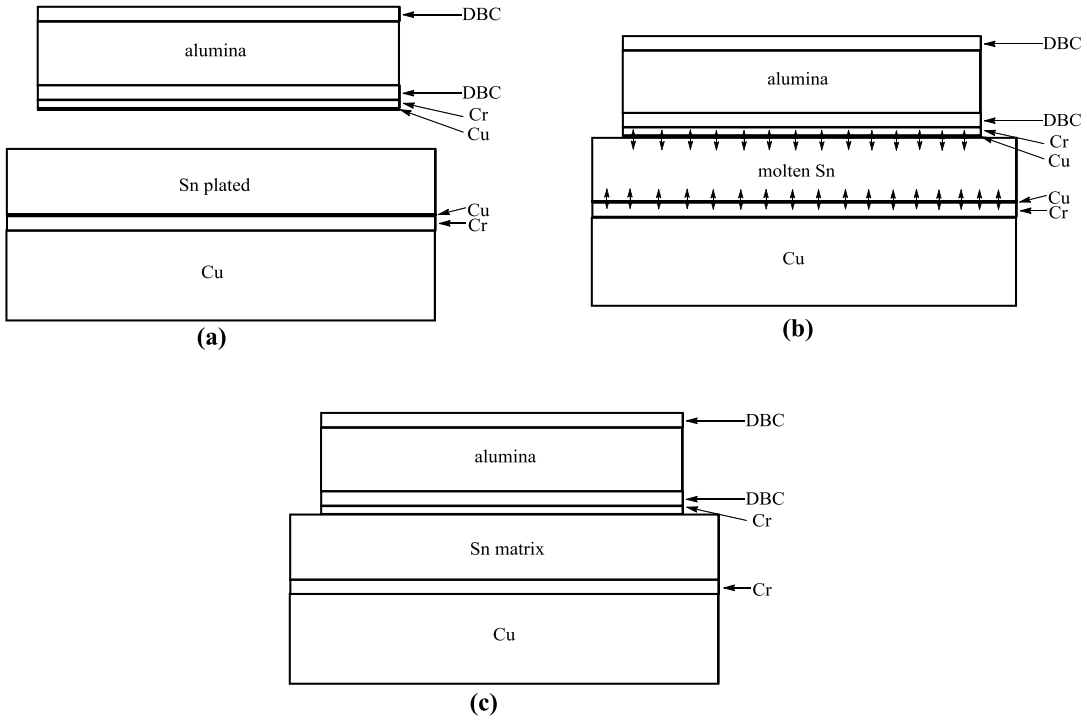
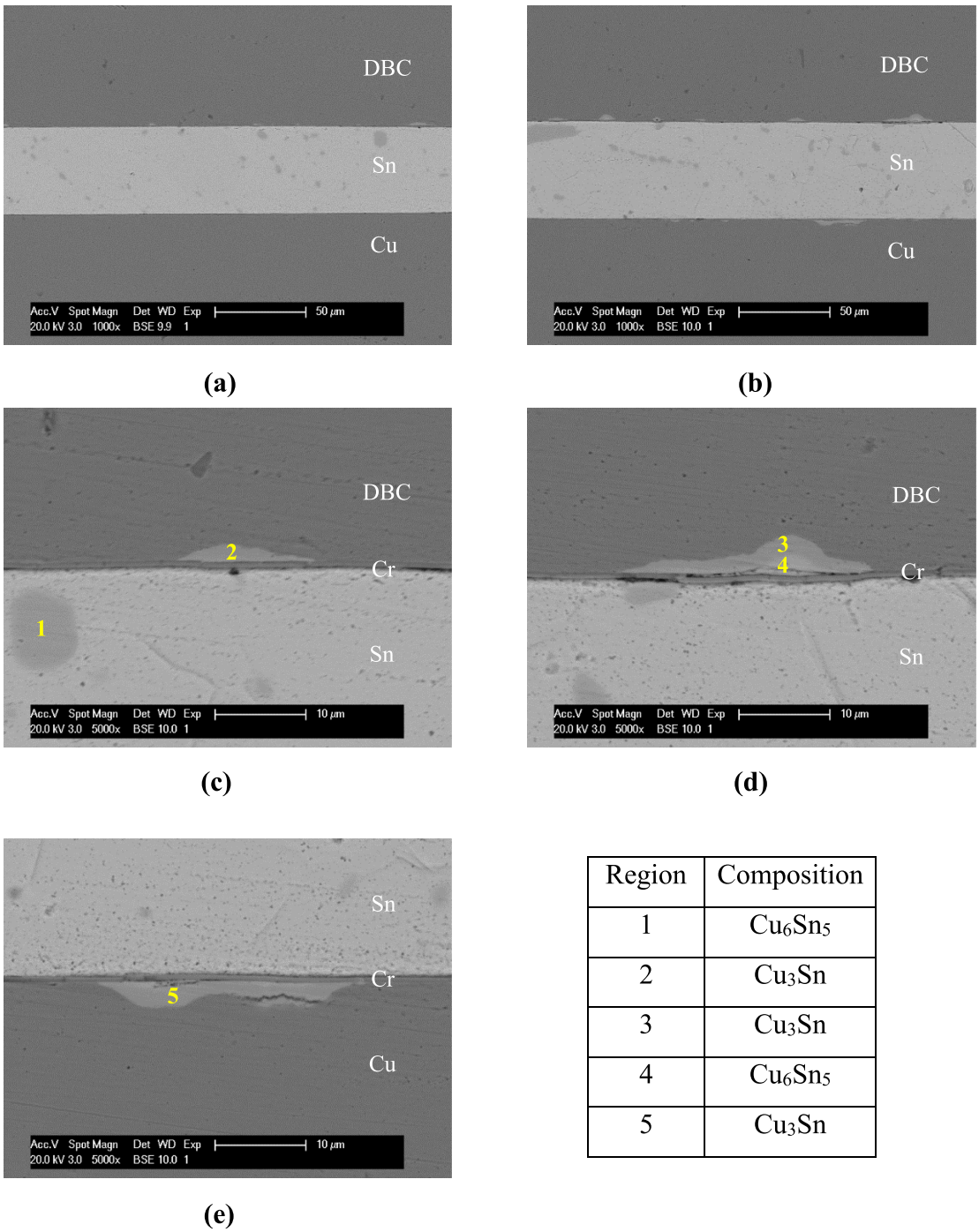


Fig. 6. Schematics illustrating the fluxless bonding mechanism. (a) As deposited. (b) Above melting temperature of Sn. (c) After cooling down to room temperature.

Cr layers on both interfaces are detected, suggesting that the Cr layer did not react with the molten Sn, as predicted by the Cr–Sn phase diagram, Fig. 1.

Fig. 6 shows the schematics of the bonding mechanism. As temperature goes above Sn melting point, Sn melts and the molten Sn begins to react with thin Cu layers both on

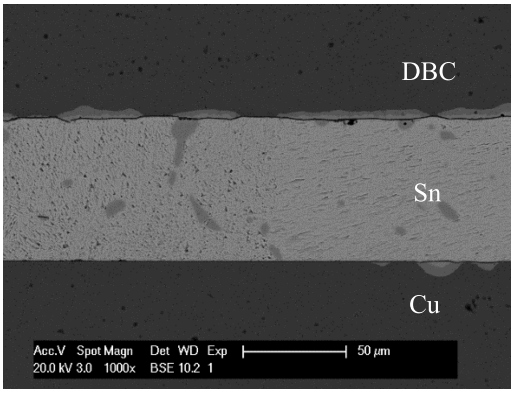


Region	Composition
1	Cu_6Sn_5
2	Cu_3Sn
3	Cu_3Sn
4	Cu_6Sn_5
5	Cu_3Sn

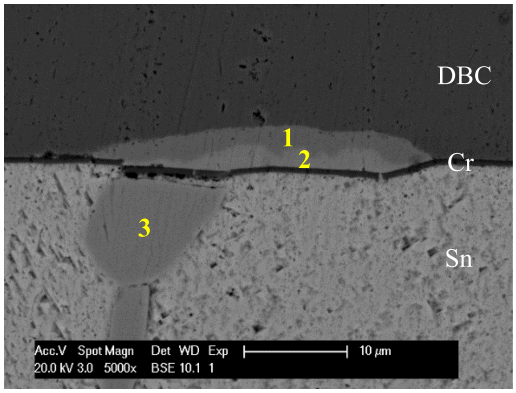
Fig. 7. Cross-sectional SEM images of sample C described in Table I at (a) low magnification (1000×) of the portion where IMC formation occurs only at DBC/Cr/Sn interface, (b) low magnification (1000×) of the portion where IMC formation occurs at DBC/Cr/Sn and Sn/Cr/Cu substrate interfaces, (c) and (d) high magnification (5000×) at DBC/Cr/Sn interface, and (e) high magnification (5000×) at Sn/Cr/Cu substrate interface.

the DBC alumina layer and on the Cu substrate. At first, the molten Sn dissolves the thin Cu layers and contacts the Cr layer and bonds to the Cr. It is noted that only when the thin Cu layer is dissolved in the molten Sn matrix would the fresh Cr layer be exposed to and bond to the molten Sn. No flux is needed to remove the native oxide on Cr because Cr was never exposed to the air either in the E-beam evaporation process or in the bonding process. With the Cr–Sn phase diagram [24], as shown in Fig. 1, there is no stable intermetallic phases exist in this system. Thus, the Cr layer can bond to Sn without forming IMC. As temperature goes down, solidification begins, resulting in a structure of DBC/alumina/DBC/Cr/Sn/Cr/Cu substrate, as shown in Fig. 6(c).

To investigate IMC growth at high temperature, samples fabricated with the same procedures as sample B were subjected to aging test at 182 °C with various times. This temperature corresponds to a homologous temperature $T_m = 0.9$ for Sn. Fig. 7 shows the cross-sectional SEM images of the sample



(a)



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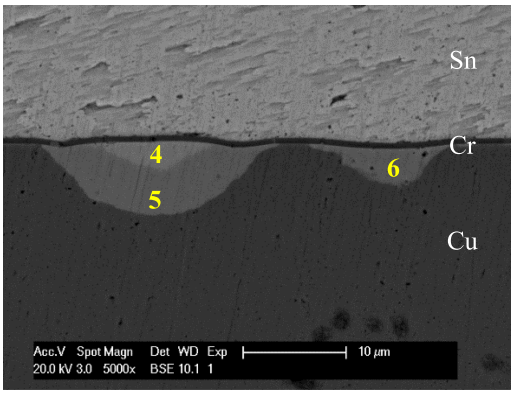


(c)

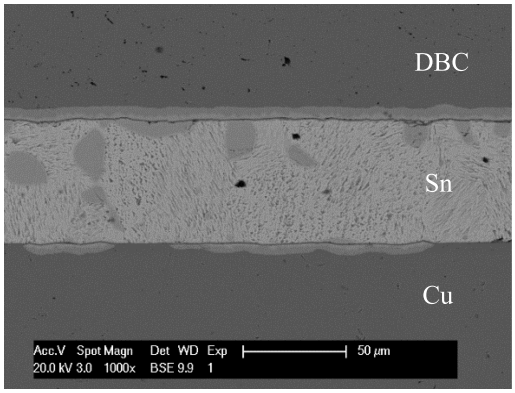
Region	Composition
1	Cu_3Sn
2	Cu_6Sn_5
3	Cu_6Sn_5
4	Cu_6Sn_5
5	Cu_3Sn
6	Cu_3Sn

Fig. 8. Cross-sectional SEM images of sample D described in Table I at (a) low magnification (1000×), (b) high magnification (5000×) at DBC/Cr/Sn interface, and (c) high magnification (5000×) at Sn/Cr/Cu substrate interface.

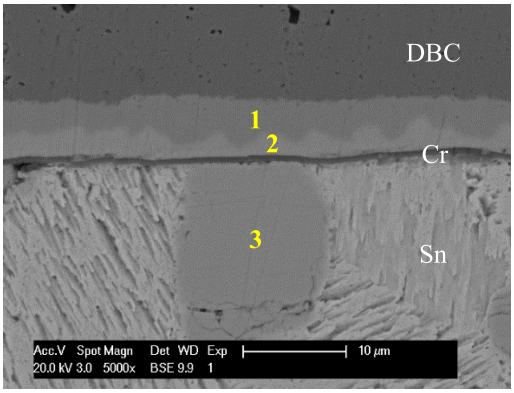
aged for 10 h. Fig. 7(a) shows one portion where the IMC formation occurs only at the DBC/Cr interface. Fig. 7(b) shows another portion where the IMC formation occurs at both interfaces. With the SEM images, IMC forms locally surrounding a microcrack or a pinhole. It does not grow into an entire layer throughout the bonding interface. Fig. 7(c)–(e) shows the IMC regions in more detailed. According to the EDX analysis, the IMC composition of region 1 inside the Sn joint corresponds to Cu_6Sn_5. This isolated IMC region was likely caused by the E-beam deposited 200-nm Cu layers originally on Cr, which were dissolved by the molten Sn and reacted with it to form the IMC. The compositions of the IMC formed at regions 2–4 (the DBC/Cr interface) are Cu_3Sn, Cu_3Sn, and Cu_6Sn_5, respectively, showing that Cu_3Sn forms initially, followed by the formation of Cu_6Sn_5 during the solid-state IMC growth at the aging temperature. The only type of IMC formed at region 5 (the Cr/Cu substrate interface) is Cu_3Sn, which means that IMC growth is faster and more severe at the DBC/Cr interface than the Cr/Cu substrate interface.

Fig. 8 shows the cross-sectional SEM images of the sample aged at 182 °C for 100 h. The composition of the IMC formed at region 1, 5, and 6 is Cu_3Sn and the composition of the IMC formed at regions 2–4 is Cu_6Sn_5. It is clearly observed that the growth of IMCs at DBC/Cr and Cr/Cu substrate interfaces mainly continues in lateral direction and the size of Cu_6Sn_5 IMCs formed inside the Sn solder becomes larger. Fig. 9 shows the cross-sectional SEM images of the sample aged at 182 °C for 200 h. The composition of the IMC formed at regions 1 and 5 is Cu_3Sn and the composition of the IMC formed at regions 2–4 is Cu_6Sn_5. The IMC layer spreads out along the lateral direction at the boundary between DBC and Cr or between Cr and Cu substrate, but the rate of growth in vertical direction is not as fast as in lateral direction. It appears that Sn atoms diffuse through the microcrack or the pinhole on the Cr layer and spread along the interface between Cr and Cu. The thickness of the IMC layer is around 7 μm.

The microcracks and pinholes are probably caused by surface defects and contaminations. Before depositing Cr and Cu layers in a vacuum chamber, the Cu substrates and DBC alumina samples were cleaned and prepared in a typical laboratory environment. Small surface defects and contaminations are very difficult to avoid. When Cr layer is deposited over these defects and contaminations, it does not bond and adhere to the underlying Cu. At the defect sites, the Cr film is weak and can be easily penetrated by the molten Sn during the



(a)



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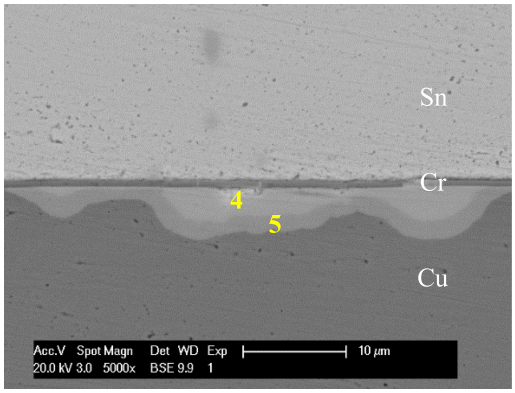

(c)

Region	Composition
1	Cu_3Sn
2	Cu_6Sn_5
3	Cu_6Sn_5
4	Cu_6Sn_5
5	Cu_3Sn

Fig. 9. Cross-sectional SEM images of sample E described in Table I at (a) low magnification (1000×), (b) high magnification (5000×) at DBC/Cr/Sn interface, and (c) high magnification (5000×) at Sn/Cr/Cu substrate interface.

bonding process and subsequent aging. In production environment, the defects and contaminations can be eliminated. Thus, there should be very few cracks and pinholes on the Cr layer. IMC formation caused by penetration of molten Sn through the cracks or pinholes, shown in Fig. 7, can be minimized.

IV. Conclusion

In this paper, a fluxless bonding process between DBC alumina substrates and Cu substrates was developed with suppressed IMC formation at the bonding interfaces. It is a new process that deviates from the conventional soldering principle of requiring IMC formation as necessary condition of successful soldering. Numerous publications have reported that extensive IMC growth results in reduced solder joint reliability. This is particularly serious in flip-chip technology using solder bumps. In our high-power electronic module project, we are looking to increase the operating temperature of solder die attach to a homologous temperature of 0.8. For pure Sn solder, this corresponds to 131 °C. High operating temperature allows us to raise the heat sink or coolant temperature. The hurdle of achieving high solder operating temperature is the extensive IMC growth. To suppress IMC growth at high temperature, Cr is selected as the barrier layer between Sn and the underlying Cu. After bonding, the Sn joints indeed have a little IMC. After high-temperature aging at 182 °C for 100–200 h, IMCs grow laterally along the Cr/Cu interface. Careful SEM and EDX evaluations have shown that the Sn atoms penetrate through microcracks or pinholes on the Cr layer to reach Cu and react with the Cu. The Sn atoms further diffuse along the Cr/Cu interface to spread the IMC growth in the lateral direction. The 500-nm Cr layers are still there after the aging processes, showing that Cr does not react with either Cu or Sn. The microcracks and pinholes are caused by defects that often stay on the substrate surfaces cleaned and prepared in a typical laboratory. In production environment, the microcracks and pinholes can be eliminated. Solder joints without intermetallic formation are thus potentially achievable.

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