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Los Angeles

Additive Enhancements for Solution Processed Metal Oxide Thin Film Transistors

A thesis submitted in partial satisfaction

of the requirements for the degree Master of Science

in Materials Science and Engineering

by

Philip Jwo Li

2018

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2018

ABSTRACT OF THE THESIS

Additive Enhancements for Solution Processed Metal Oxide Thin Film Transistors

by

Philip Jwo Li

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2018

Professor Yang Yang, Chair

Solution processed metal oxide semiconductors have attracted much attention as a promising class of materials to be used as the channel material in thin film transistors due to its transparency, high mobility, scalability, and low cost of manufacturing. Nevertheless, there are still major challenges in terms of processing, device performance and stability that need to be overcome before this process can be implemented for large scale production. In this thesis, several chemical additives and their effects on film formation, processing temperature and electrical parameters such as field effect mobility, on-off ratio and threshold voltage shifts under PBS stress tests were investigated. In particular, the addition of ethylene glycol, acetylacetone, and acetic acid were investigated in a metal oxide precursor solution. It was demonstrated that ethylene glycol significantly improved the wettability of the concentrated IGZO solution and resulted in a minimal contact angle of 3.8 degrees. This allowed for coating a concentrated metal

oxide precursor solution (0.5M) five times the baseline concentration while still maintaining high film formation quality. The addition of acetylacetone allowed for low annealing temperatures (less than 300°C) through the combustion synthesis route and serves as a protection group to prevent premature formation of metal oxide network in solution. Finally, the addition of acetic acid improved the solubility of the metal precursor in the solution and allowed for higher concentrations of metal precursor to be dissolved in solution, which becomes important if higher viscosity precursors for thick films are needed. The addition of these additives produced devices with near zero turn on voltage, excellent on-off ratio ($>10^7$), and superior stability (less than eight volts of threshold voltage shift at 10,000 seconds of PBS). The findings in this thesis present improved synthesis routes for solution processed semiconductors and open new possibilities for the fabrication of flexible electronic devices and next generation large scale consumer electronics.

The thesis of Philip Jwo Li is approved.

Ximin He

Yu Huang

Yang Yang, Committee Chair

University of California, Los Angeles

2018

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List of Abbreviations

2-ME	2-Methoxyethanol
AM	Active Matrix
AOS	Amorphous Oxide Semiconductor
CBM	Conduction Band Minimum
DFT	Density Functional Theory
FET	Field Effect Transistor
FT-IR	Fourier Transform Infrared
IGZO	Indium Gallium Zinc Oxide
I_{ds}	Drain-Source Current
IPA	Isopropyl Alcohol
IV	Current-Voltage
IZO	Indium Zinc Oxide
LCD	Liquid Crystal Display
LTPS	Low Temperature Polysilicon
MOS	Metal Oxide Semiconductor
OLED	Organic Light Emitting Diode
PBS	Positive Bias Stress
SS	Subthreshold Swing
SSE	Solid State Energy
TFT	Thin Film Transistor
UV	Ultraviolet

VBM	Valence Band Maximum
V_{ds}	Drain-Source Voltage
V_{gs}	Gate-Source Voltage
YIZO	Yttrium Indium Zinc Oxide
ZTO	Zinc Tin Oxide

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1. Introduction

1.1 Motivation

In the recent years, there has been considerable research conducted in solution processed semiconductors both in the organic and inorganic fields to realize large area printed and flexible electronics.[1] Solution processing offers novel deposition methods that minimize waste, lower fabrication costs, and bring about new functionality to devices traditionally manufactured using vacuum deposition processes. [2] Conventional electronics that use single crystal silicon wafers suffer from high capital costs and barriers to scaling to large area processing. Mechanical flexibility and transparency are also key challenges that traditional silicon wafers will have difficulty overcoming.

In terms of candidate semiconductor materials, there has been considerable work done in the organic semiconductor field.[3] Recent works demonstrate high compatibility of organic semiconductors with various solution processing methods including spin coating, inkjet printing, and gravure printing.[4]Simple electronics have also been demonstrated using these techniques, including thin film transistors and electronic paper. Nevertheless, organic semiconductors still suffer from instabilities with the environment due to their sensitivity to moisture and ambient air and also lack the field effect mobility requirements to satisfy high performance electronics.[5]Amorphous metal oxide semiconductors have been investigated as a new class of materials to overcome the difficulties faced by organic semiconductors while providing high field effect motilities and ambient stability. This new class of material offers high transparency and electrical conductivity and can be used with the same solution processing methods that allow for low cost deposition and fabrication of large area flexible electronics. [6] The predominant

method for forming these amorphous oxide films has been with the wet chemical, sol-gel synthesis method. Nevertheless, this sol-gel processing method usually requires a high temperature annealing step that makes it incompatible with low cost polymer substrates. Much research efforts have been devoted in recent years to overcome this high temperature annealing method with various success. Notable methods include chemical modifications in the sol-gel formulation through a combustion processing route or varying the anneal treatment using UV assisted high energy activation.[7] Thus for the full realization of low cost and large area solution processing, the sol-gel metal oxide formation chemistry must be thoroughly understood.

1.2 Objective

The purpose of this work is to investigate the effects of various chemical additives in the sol-gel formulation and how the combination of these additives can deliver thin film transistors with higher performance and greater stability. The mechanisms that these additives undergo in the formulation along with the mechanisms that affect the final thin film transistor device performance will also investigated.

2. Background

2.1 Thin Film Transistor Principles

2.1.1 Structure

The basic working structure of a thin film transistor utilizes three terminals to modulate the current that flows between the source and drain terminal. The gate electrode is responsible for modulating or regulating the current that flows through the source/drain electrodes through a field effect. This field effect is achieved when a voltage is applied between the gate and source electrodes creating a capacitive effect through an injection of carriers close to the dielectric/semiconductor interface.[8] A diagram of a typical thin film transistor and possible layout structures are shown in Figure 1.

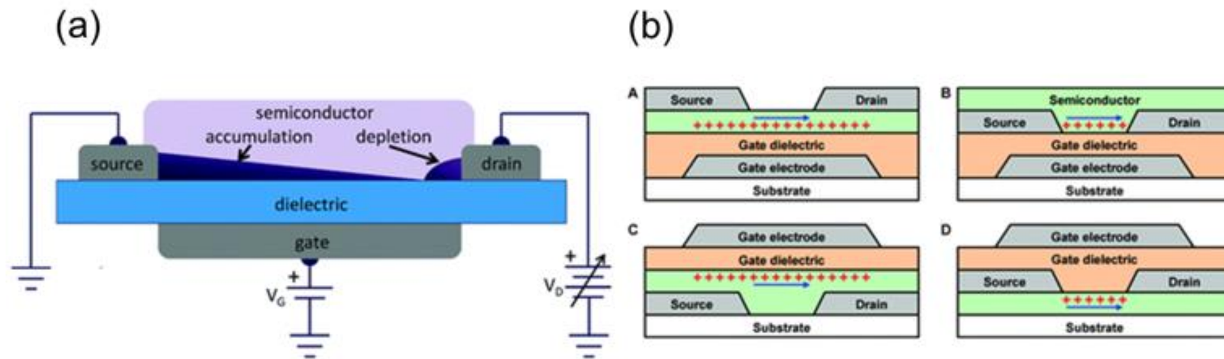

Figure 1 (a) Schematic of a thin film transistor (b) Schematic cross-sections of the four principle thin-film transistor structures. The carrier channel is schematically shown in red. A: Bottom-gate (inverted) staggered TFT; B: Bottom gate (inverted) coplanar TFT; C: Top-gate staggered TFT; D: Top-gate coplanar TFT.[9]

The typical structure of an amorphous oxide semiconductor TFT involves a channel layer connected by a source and drain electrode with a dielectric layer that separates the gate and the semiconductor. Depending on the type of layout the TFT employs, the gate could be on the top

or bottom. The other variation is the placement of the source and drain electrode, which can also be on the top or bottom, depending on if it is a top contact or bottom contact device. These variations of gate and electrode placement lead to the four different variations of device layout shown in Figure 1. Each type of configuration has its advantages and disadvantages and will be discussed shortly. Part (a) of Figure 1 describes the mode in which the TFT operates. In the n-type enhancement mode, the source electrode will be grounded and a positive voltage will be applied to the gate. This will induce an accumulation of carriers at the semiconductor/dielectric interface. A positive drain bias in relation to the grounded source electrode will generate an electric field within the semiconductor layer and force carriers to flow from source to drain. [8] Similarly, in a p-type enhancement mode, the opposite polarities will be applied to each of the terminals and the majority carrier in the semiconductor will be hole carriers.

As mentioned previously, each of the four different TFT configurations offer its own advantages and should be selected according to the specific application. For amorphous silicon TFT's, the staggered bottom-gate configuration was chosen in order to protect the semiconductor layer from the constant backlight used for the liquid crystal display (LCD) backlight.[8] On the other hand, the coplanar top-gate structure was usually selected for polysilicon TFT's in order to meet high processing temperature and flat continuous film criteria. Bottom-gate devices will reveal the semiconductor layer to the ambient conditions and may result in higher instabilities, but this configuration allows for easy surface modifications of the semiconductor and are have been used in biosensor type applications. As can be seen, each type of architecture offers a unique benefit and the specific application should be taken into account when selecting the configuration to be implemented.

2.1.2 Thin Film Transistor Device Physics

To understand the device physics behind a thin film transistor, it is convenient to reference the theory of a field effect transistor since much of the physics can be applied. The basic building block for a metal oxide semiconductor field effect transistor (MOSFET) is the MOS capacitor. The MOS capacitor is the heart of the MOSFET and is responsible for controlling the amount of accumulated charges at the semiconductor/dielectric interface. Figure 2 shows a typical diagram for a MOS capacitor.

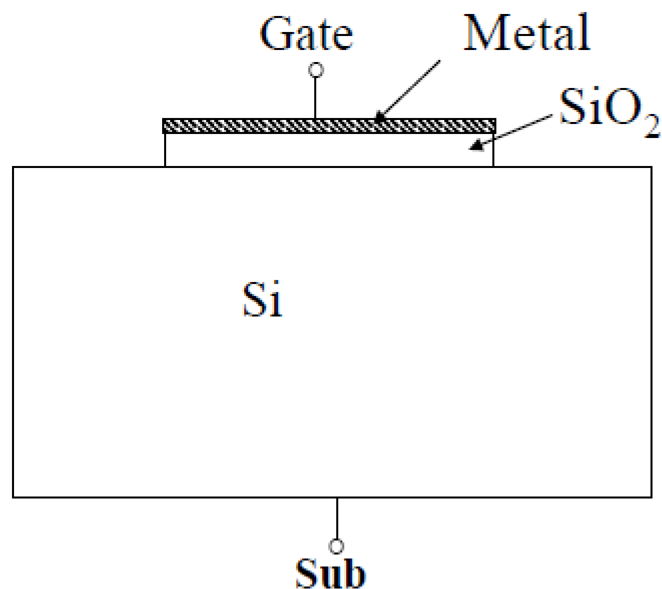

Figure 2: Diagram of typical metal oxide semiconductor capacitor with one terminal on the gate and the other connected to the substrate. The excellent insulating properties of the silicon dioxide gate insulator layer prevent a DC current from flowing between the two terminals. [10]

The MOS capacitor shown in Figure 2 employs a silicon substrate and silicon dioxide as gate insulator. The silicon oxide serves as an excellent insulator and prevents any DC current from flowing when a bias is applied to the two terminals. The two terminals of this device are connected to the gate and to the substrate. Note that in this figure, the silicon substrate could be either n-type or p-type.

Upon applying a bias to the two terminals, an electric field will be induced in the oxide. If this electric field were to penetrate into the semiconductor, the majority carriers in the semiconductor would experience a force to move towards the semiconductor/oxide interface.[11] To describe the electric field in the oxide layer, the one dimensional Poisson equation can be employed.

$$\frac{d^2\phi}{dx^2} = \frac{-\rho(x)}{\epsilon_s} \quad \text{(2.1)}$$

$\rho(x)$ is the volume charge density, $\varphi(x)$ is the electric potential, and ε_s is the permittivity of the semiconductor. The volume charge densities can be further defined as

$$\rho(x) = q(p(x) - n(x) + N_D) \quad \text{(2.2)}$$

$$\rho(x) = q\left\{p_i \exp\left(\frac{-q\phi(x)}{kT}\right) - n_i \exp\left(\frac{-q\phi(x)}{kT}\right) + N_D\right\} \quad \text{(2.3)}$$

By integrating the Poisson equation over the length of the depletion region, the electric field in the semiconductor can be obtained.

Once the electric field in the semiconductor is known, the energy band diagrams can be drawn to further understand how carriers are interacting under an applied gate bias. Figure 3 shows the energy-band diagrams of the MOS system when a negative bias is applied to the gate. The conduction and valence band edges bend as shown in the figure. The negative bias applied on the gate terminal with respect to the substrate raises the energy level on the gate side and causes the conduction and valence bands to bend upward. This is reflected as an induced electric field that penetrates into the semiconducting layer and causes the majority carrier electrons to be repelled away from the interface.[12] This repelling of majority carrier electrons induces the positive space charge region shown in 3(a).

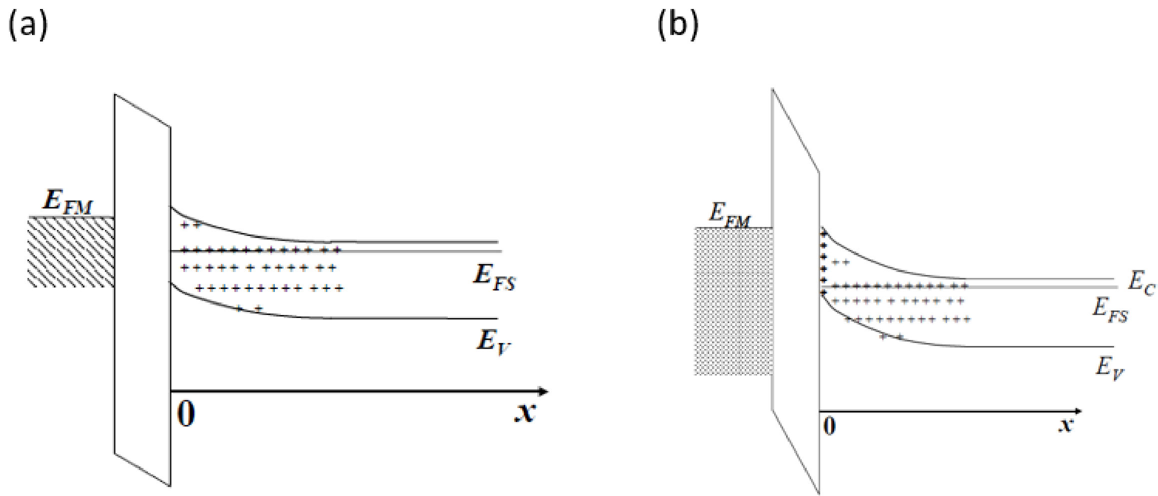

Figure 3: Energy band diagrams for MOS capacitor with n-type substrate under (a) depletion and (b) inversion.[10]

Upon applying an even larger negative bias at the gate, the minority carrier holes are attracted to the interface and inversion is achieved. At the point of inversion. The valence band edge has overlapped with the intrinsic Fermi level of the bulk semiconductor and is defined as onset of inversion. The sufficiently large negative bias at the gate has resulted in an inversion layer of holes at the interface and the semiconductor surface has been inverted from n type to p type.

The width of the induced space charge region can be calculated if the doping concentration of the semiconductor is known.

$$x_{dT} = \left(\frac{4\epsilon_s\phi_{fp}}{eN_a}\right)^{1/2} \qquad (2.4)$$

$$\phi_{fp} = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \qquad (2.5)$$

X_{dT} is the maximum space charge width at the inversion point and φ_{fp} is the potential difference between the Fermi level and the intrinsic Fermi level in the bulk.

The threshold voltage is defined as the applied gate voltage required to achieve the threshold inversion point.[11] In essence, it is the condition when the surface potential is equal to two times the bulk potential. The threshold voltage can be calculated as follows.

$$V_{TN} = V_{oxT} + 2\phi_{fp} + \phi_{ms} \quad (2.6)$$

$$V_{TN} = \frac{|Q_{SD}(\max)|}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_p \quad (2.7)$$

Where ϕ_{ms} is the metal semiconductor work function difference, C_{ox} is the capacitance in the oxide layer, and Q_{SD} is the maximum charge in the depletion region. [11]

Finally, it is useful to have an idea of the surface charge density as a function of surface potential. Figure 4 shows the variation of surface charge density for p-type Si MOS (accumulation charge and inversion charge) as a function of surface potential.[10] At the flat band, the total charge is zero. To the right of flat band, it is the depletion region when the static charges are revealed forming the space charge region before the inversion charges have been formed yet. The weak inversion region is not as well defined but ends when the surface potential is equal to two times ϕ_p. After the onset of weak inversion crosses the threshold voltage, the surface charge density increases rapidly as the surface charge has been inverted. At this point, the minority carriers have accumulated at the interface and results in a rapid exponential increase in surface charge density. On the left side of the flat band, the accumulation regime also has an exponential dependence on surface potential and is due to the accumulation of majority charge carriers existing in the bulk.[13]

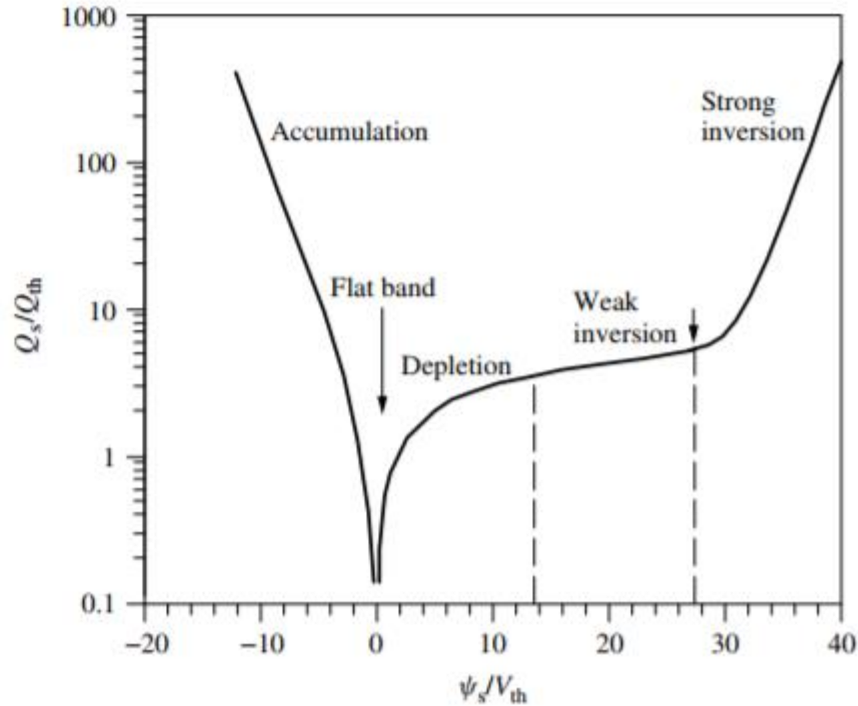

Figure 4: Variation of surface charge density for p-type Si MOS (accumulation charge and inversion charge) as a function of surface potential.[10]

2.1.3 Key Device Metrics

It is important to understand the key device metrics that are frequently used to evaluate thin film transistor performance. The two most common current-voltage (IV) characteristics that are measured are the transfer curve and the output curve. Figure 5 (a) is a plot of drain current versus drain voltage with varying gate voltages and is known as the output curve. In Figure 5 (b), the drain current is plotted against the gate voltage with a specified drain voltage and is known as the transfer curve. Each of these curves have specific parameters that can be extracted and used to quantify device performance.

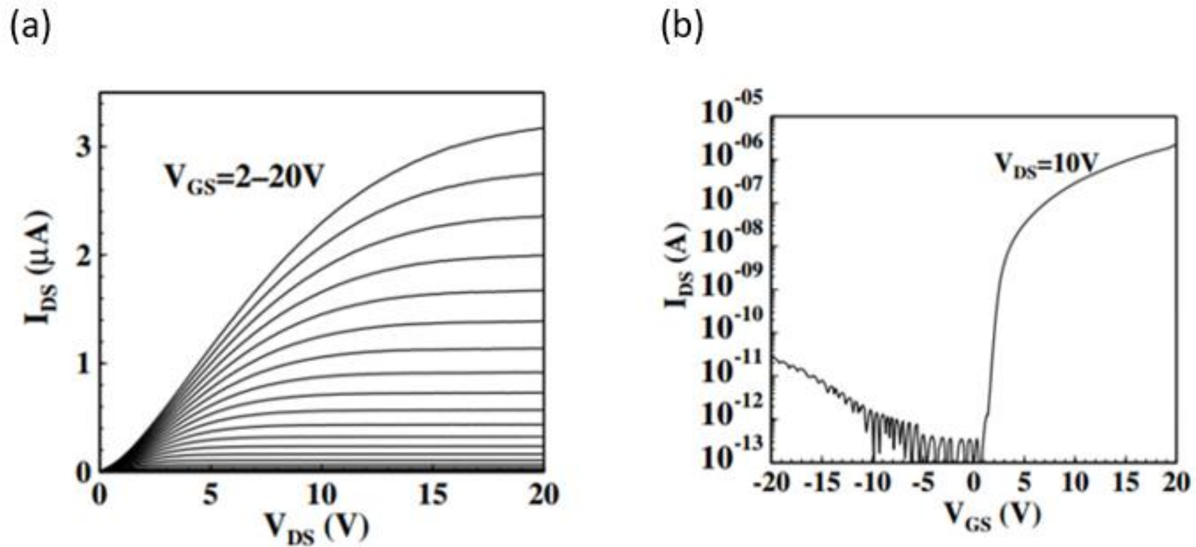

Figure 5: (a) Output and (b) transfer curves for a-Si TFT with channel width and length of 28 and 6 µm, respectively.[14]

A few major metrics that are usually defined for a TFT include field effect mobility, threshold voltage, on/off ratio and subthreshold swing. Each of these parameters may vary depending on the device structure, fabrication process, channel material, and the quality of the interface both at the dielectric/semiconductor interface and the semiconductor/electrode interface.[8] Typically, an ideal TFT will have high mobility, near zero threshold voltage and a small subthreshold swing.

Carrier mobility is a parameter that characterizes how easily a charge carrier can flow in a material under a given electrical field. This parameter will affect the maximum drain current of a device.[15] Typically, the intrinsic mobility can be measured for a bulk material using a Hall measurement. This type of mobility is known as the Hall effect mobility. Nevertheless, typical mobilities for TFT's are not reported using Hall effect mobility due to non-idealities caused by scattering of charge carriers by the trapped charges in the dielectric, interface states and the surface roughness. Instead, the field effect mobility is usually the reported metric for thin film transistors.

Threshold voltage is the gate voltage that allows a conductive channel to form at the dielectric/semiconductor interface.[16] This value is somewhat arbitrary and has been defined a few different ways. The common method is to use a linear extrapolation from the transfer curve at the point that corresponds to the maximum slope. The intersection of the linear extrapolation with the x-axis is defined as the threshold voltage. This parameter plays a significant role in device operation and is a key parameter for describing when the device is turned on. For enhancement mode n-type TFT's the threshold voltage will be positive. Similarly, a negative threshold voltage will be observed in p-type enhancement mode TFT's. Enhancement mode is usually the preferred mode of operation due to less complicated circuit design and power dissipation minimization.

The on/off ratio is calculated by dividing the maximum drain current by the minimum drain current. The minimum drain current is given by the off state current of the device, usually reported as the leakage current through the source electrode. The maximum drain current is reported as the on state current usually in the saturation regime of the device. When operating the TFT as an electrical switch, it is usually desirable to have a device with an on/off ratio greater than 10^6.

Subthreshold swing measures how efficiently the TFT switches between the on state and off state. It is defined as the inverse of the maximum slope obtained from the transfer curve, usually reported as the gate voltage needed to change the drain current by one order of magnitude. A steep slope corresponding to a low value for subthreshold swing (less than 100 mV dec^{-1}) is desired for reducing the operating voltage for the device.

2.2 Metal Oxide Semiconductors

Amorphous oxide semiconductors have been used extensively in recent years as the channel material for thin film transistors due to their compatibility with large areas, ultra-high definition, and fast frame rate.[17] They are highly sought after in the display industry as an increasing need is placed on high performance back planes for switching pixels on and off. Amorphous oxide semiconductors are capable of replacing amorphous silicon technology in active matrix liquid crystal displays (AMLCD) as well as replacing low temperature polysilicon (LTPS) in active matrix organic light emitting diodes (AMOLED) displays.[18] For many years, a-Si was sufficient for serving as the switching element for LCD technologies despite its low mobilities. Amorphous silicon backplanes boasted better uniformity and reproducibility in large area displays at a lower cost. Nevertheless, it was not capable of driving AMOLED's as higher end consumer electronics pushed to even higher display resolutions.[19] On the other hand, amorphous oxide semiconductors do not have grain boundaries and can also be processed at low temperatures in environmentally friendly and relatively low cost facilities.[20] For these reasons, much research efforts have been focused on AOS materials to be used in TFT backplanes. Their superior mobilities, optical transparency, reliability and low cost of manufacturing have placed them in the spotlight for next generation display applications.[21] One iconic example of AOS that has been researched extensively is Indium Gallium Zinc Oxide (IGZO).The discovery of IGZO has been widely credited to Hosono et al. for their work in comparing silicon and IGZO in the crystalline and amorphous phases and explaining the apparent differences in mobility from an atomic bonding perspective.

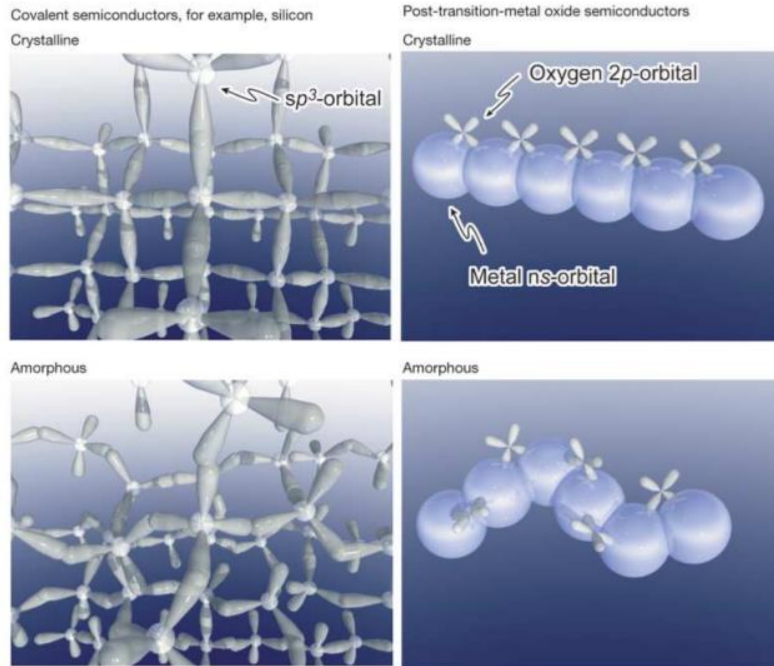

Figure 6: Comparison of mobilities for silicon and IGZO in the crystalline and amorphous phase from an atomic bonding perspective. [14]

Figure 6 describes the differences of bonding in AOS materials and silicon in the crystalline and amorphous phase. In the crystalline phase, silicon can achieve high carrier mobilities due to the effective overlapping of sp^3 orbitals. Nevertheless, in the amorphous phase, the sp^3 orbitals cannot align due to lack of directionality and result in poor overlap. This poor overlapping of orbitals results in the observed very low carrier mobility. For IGZO, even in the amorphous phase, the metal s orbitals are large and isotropic, allowing for good overlap even when there is lacking ordered structure. This allows IGZO and other AOS materials to preserve decent mobilities even in the amorphous phase. [22] The selection of zinc, gallium, indium and tin is due to their low cost and non-toxicity. Back in 1996, Hosono et al. proposed the cation candidates to be used in designing oxide semiconductors based on electron configurations.

The combination of these abundant and nontoxic elements have been attempted to create binary, ternary and quaternary compounds to be used as the active layer in thin film transistors. The

most widely studied binary compounds are tin oxide, zinc oxide, indium oxide, and gallium oxide. However, binary compounds tend to perform poorly in terms of device performance in areas such as high electrical resistivity, poor stability and low on-off ratios.[23] Reasons include the tendency for binary compounds to crystallize, giving rise to grain boundaries that scatter free carriers and degrade device reliability. By combining multiple components, the tendency to crystallize can be combated and provide an easier route for synthesizing amorphous films. If we consider IGZO as an example, the zinc and indium oxide have been reported as having tendencies to form polycrystalline phases.[24] On the other hand, indium zinc oxide and zinc gallium oxide are more likely to be amorphous. This is due to differing ionic charges and sizes that disturb the formation of the crystalline phase and favors the formation of the amorphous phase.

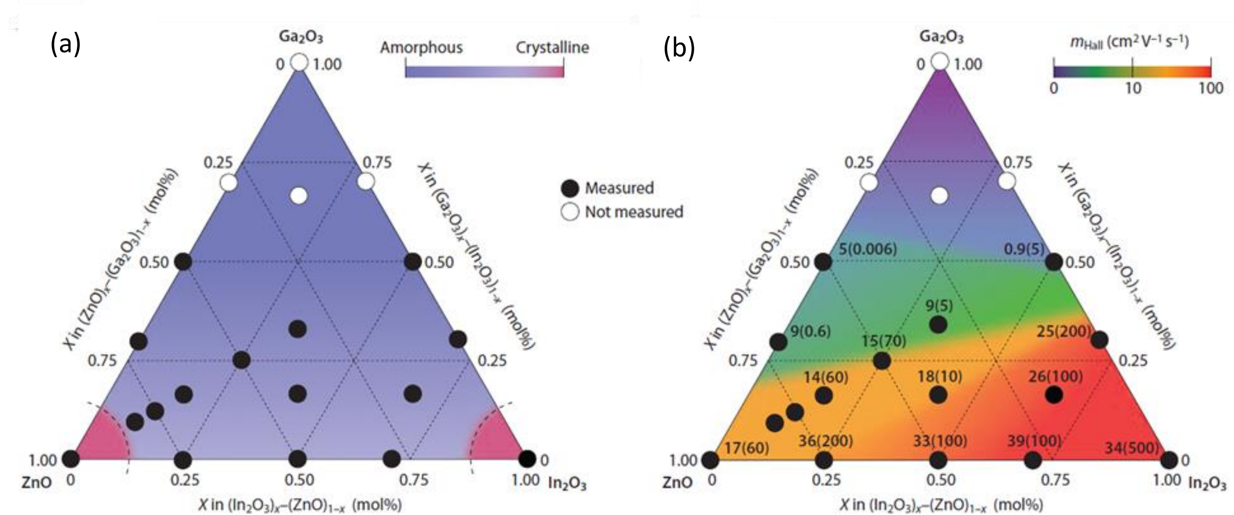

Figure 7: Crystallinity of representative metal oxide semiconductor and each hall mobility.[24]

Figure 7 presents an easy way to compare the crystallinity and hall mobilities when combining different oxides. In choosing materials for the TFT channel layer, it is favorable to reduce the carrier concentration. This will aide in stability and lowering the off state current. In choosing

elements to suppress carrier concentration, those with solid-state energies (SSE) above the ionization energy should be selected. This is the reason gallium was selected as the electron suppressing cation in IGZO.

The nature of AOS materials and their bonding structure as compared to amorphous silicon allow the former to have better electrical performances. For amorphous silicon, the origin of mobility is hopping conduction rather than band conduction, so the mobilities of amorphous silicon TFTs are typically around 1 $cm^2 V^{-1} s^{-1}$.[8] The conduction band minimum (CBM) and valence band maximum (VBM) of amorphous silicon are formed by sp^3 hybridized orbitals and tend to have strong spatial directionality. In a disordered amorphous structure, deep and highly localized states form below the conduction band and above the valence band. This disorder results in carriers needing to migrate by hopping conduction and result in low field effect mobilities. On the other hand, as mentioned previously, the bands in AOS materials are formed by spherically overlapping metal cation s orbitals and are not significantly disrupted in the amorphous phase. This allows band conduction to still occur in the amorphous phase, resulting in field effect mobilities to exceed 10 $cm^2 V^{-1} s^{-1}$. These theories are consistent with the band structures when running density functional theory (DFT) calculations. In addition, amorphous IGZO is expected to have a lower off-state leakage current than amorphous silicon due to its wider band gap.

In selecting the elements for designing TFT channel materials, multicomponent compounds with cations of different solid state energies will offer higher stability and better uniformity than binary compounds. [25] Similarly, it can be beneficial to incorporate cations with different sizes. It is necessary to incorporate cations such as indium and tin to form broad-spreading conduction band maximums even in the amorphous phase. In addition, including cations with solid state energies lower than -4.5 eV will enable better control of electron concentrations to improve

device stability. Bond dissociation energies are another method used to select cations for metal oxide semiconductors. The idea is to select cations that form a strong bond with oxygen and can be used as oxygen stabilizers. The control of oxygen is important as oxygen vacancies are responsible for the carrier concentrations in the semiconductor. Thus, selecting elements such as boron, aluminum or yttrium can be good oxygen stabilizers.[26] There have been several reports of YIZO thin film transistors with electrical properties matching that of IGZO TFT's. The incorporation of these cations allow covalent-ionic hybrid AOS materials and can lead to devices with high mobility, stability and low hysteresis.

2.3 Deposition Methods

Many different types of metal oxide semiconductors have been researched including zinc oxide, indium oxide, indium zinc oxide (IZO), indium gallium zinc oxide (IGZO), tin oxide, and copper oxide.[27] The approach of depositing these oxides and the methods for the phase formation largely fall in to two categories: vacuum based deposition and solution based deposition. Examples of vacuum based deposition include thermal evaporation, sputtering, atomic layer deposition and physical vapor deposition.[28] The most widely used solution based deposition method is the sol-gel method. Each of these methods have their advantages and importance, but here we will only briefly discuss two of the representative methods. Sputtering will be discussed as the representative method of vapor to solid phase transformation and the sol-gel method will be discussed as the representative method of liquid to solid phase transformation. It is useful to have a working knowledge of the concepts behind phase formation for metal oxide semiconductors.

2.3.1 Vacuum Based Deposition

Vacuum based deposition methods have been widely used in the semiconductor and microelectronics manufacturing industry. This is the traditional method for fabrication and is the most widely adopted method in industry. Table 1 shows a few representative vacuum based deposition methods and their typical operating pressures.

Table 1: Representative vacuum based deposition methods and their typical operating pressures[29]

Vacuum Level	Pressure (Torr)	Deposition Method
Atmospheric – Low Vacuum	760 - 25	Chemical Vapor Deposition
Medium Vacuum	$25 – 10^{-3}$	Thermal Evaporation
High Vacuum	$10^{-3} – 10^{-9}$	Magnetron Sputtering
Ultra-high Vacuum	$10^{-9} – 10^{-12}$	Molecular Beam Epitaxy

One of the representative methods of vacuum based deposition is sputtering deposition. Sputtering has been widely used to deposit metal oxide materials. Among the class of sputtering techniques, a popular method is magnetron sputtering. The basic principle of sputtering takes advantage of the momentum exchange between the ions and target atoms by collisions.[30] In this process, an ionized gas is produced when a voltage is applied between the electrodes. This applied electric potential induces a collision between accelerated electrons and the neutral carrier gas. When enough energy is present in the collision, the neutral gas can become ionized and produce even more carriers in the process. The newly generated electrons can then be accelerated to ionize more neutral gas and the process continues. Eventually, when enough of the plasma has been generated, the ion bombardment covers the entire cathode surface and begins to collide into the target. A certain number of collisions into the target will exceed the surface binding energy

of the target and begin to eject atoms. Specifically, when the ion bombardment into the target has enough kinetic energy to overcome the surface binding energy, atoms are ejected from the solid target and can then travel to the substrate for deposition.[17] There are many advantages that sputtering deposition offers. First, the phase transformation occurs at near room temperature, so even temperature sensitive substrates such as polymers can be compatible with this method. Second, the carrier gas and atmosphere pressure can be changed during the deposition, allowing for many versatile conditions to be used. One common technique is to modify the oxygen to nitrogen ratio in the carrier gas to adjust the amount of oxygen vacancies in the film. These advantages lend itself as a powerful tool for metal oxide materials and has been widely adopted in industry.

2.3.2 Solution Processed Deposition

Solution based deposition methods have been extensively investigated in recent years due to its low cost and scalable fabrication techniques. The predominant method for solution based deposition is the sol-gel method. Many kinds of metal oxides have been synthesized using sol-gel processing such as zinc oxide, IGZO, ZTO and indium gallium oxide.[31] Many of the common metal oxides that are used in sputtering can also be adopted in sol-gel deposition. The basic process relies on a phase transformation of materials from liquid precursors to a colloidal suspension known as the sol and finally to a network structure known as the gel. The first step for sol-gel chemistry involves forming the sol from the precursors through a hydrolysis step followed by a condensation step. Through polycondensation, metal-oxo-metal or metal-hydroxy-metal bonds are formed. Next removal of excess solvent in combination with shrinking of the gel network and then annealing the film creates a dense xerogel or aerogel.[32] This gel can be classified into five major categories: colloidal, metal-oxane polymer, metal complex,

polymerizable complex and crosslinking polymers. For metal oxide synthesis, metal salts are dissolved in a solvent to form the basic precursor solution. This precursor solution will then undergo the hydrolysis, condensation and densification steps previously mentioned. It transforms the precursor solution into a metal oxide network upon the final annealing step. The advantages of sol-gel deposition include control over the stoichiometry of the precursor and allowing for different complex materials to be synthesized. Furthermore, it allows for good control of particle size and film morphology. As mentioned previously, one of the main reasons for pushing for solution based deposition is the low cost and scalability. Many different deposition methods have been investigated with the sol-gel chemistry including spin coating, spray coating, dip coating and inkjet printing.[33]

3. Experimental Methods

3.1 Substrate Cleaning

Silicon wafers are purchased from WaferPro in 100 mm sizes doped with boron (p++) with <100> crystal orientation. The thickness is 500 microns with a 1000 angstrom silicon oxide layer. The resistivity of the wafers are 0.005 ohm/cm. Each wafer is cut into 1.5 cm by 1.5 cm square sized substrates. The wafers were cleaned with a two step process. First, they are immersed in acetone and sonicated in ultrasonic treatment for 15 minutes to remove organics, dust, and oil residues. Second, they are immersed in isopropanol (IPA) and also sonicated for 15 minutes. Once finished, the substrates are kept in the IPA solution for storage until ready for use.

3.2 Precursor Solution Preparation

Precursor solutions for the semiconducting layer in this work comprised of either indium oxide (In_2O_3) or indium gallium zinc oxide (IGZO). The concentrations of the solutions were either 0.1

M for the baseline or 0.5 M for the concentrated solutions. A summary of the compositions of the precursor solutions and the additives used are shown in Table 1. The 0.1 M indium oxide baseline precursor solution was prepared by dissolving 300.8 mg of indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$, Aldrich, 99.999%) in 10 mL of 2-methoxyethanol (2-ME, Aldrich, 99%). To make the 0.1 M indium oxide additive enhanced solution, 100 µL of ethylene glycol (Sigma, anhydrous, 99.8%) and 1.2M of acetic acid (CH 3 COOH, EMD, 99.7%) was added to the baseline indium oxide precursor solution. The 0.1 M IGZO precursor solution was prepared by dissolving 225.6 mg of indium nitrate hydrate, 21.3 mg of gallium nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$, Aldrich, 99.999%) and 31.5 mg of zinc nitrate hydrate ($Zn(NO_3)_2 \cdot xH_2O$, Aldrich, 99.999%) in 10 mL of 2-ME. The molar ratio of the IGZO solution was 9:2:1 of In, Ga and Zn. 200 µL of acetylacetone (AcAc, Aldrich, 99%) and 70 µL of ammonium hydroxide (aq.)(NH_4OH, 28% NH_3 in water, Aldrich, 99.99%) were added to all solutions and stirred for over 12 hours. The 0.5M concentrated solutions were made with the same procedure as described above and increasing the loading of metal precursors by five times. Pristine solutions of 0.1 M indium oxide and IGZO without additives were also made for comparison. All solutions are filtered through a 0.2 µm PTFE syringe filter (GE, Trevose, PA, USA) and stored in a dark, ambient environment under room temperature.

Table 2: Composition of precursor solutions

Solution	Precursor	Additives
In_2O_3 (pristine)	$In(NO_3)_3$	None
In_2O_3 (additive enhanced)	$In(NO_3)_3$	Acetylacetone, ethylene glycol, acetic acid
IGZO (9:1:2) (pristine)	$In(NO_3)_3$, $Ga(NO_3)_3$, $Zn(NO_3)_2$	None
IGZO (9:1:2) (additive enhanced)	$In(NO_3)_3$, $Ga(NO_3)_3$, $Zn(NO_3)_2$	Acetylacetone, ethylene glycol, acetic acid

3.3 Fabrication of Devices

The thin film transistors are fabricated with the bottom gate top contact structure. Using this architecture, the silicon wafer serves as the gate and the thermally grown oxide serves as the gate insulator. This type of device will have the global gate structure and share a common gate insulator. The substrates are blow dried with nitrogen after removing from the storage in IPA. Before spin coating, the substrates are treated in UV-ozone chamber (184.9 nm (10%) and 253.7 nm (90%)) for 20 minutes to remove organic residue and improve wettability of the substrate. After the UV treatment, about 35 μL of the desired precursor solution is dispensed onto the substrate and spun at 3000 rpm for 30 seconds. Once complete, the substrates are removed and immediately baked on a hot plate at 100°C for one minute to prevent pinhole formation and remove excess solvent. Once the baking is finished, the films are annealed on a hotplate at 300°C for one hour to complete the metal oxide formation. After annealing, all samples are allowed to cool to room temperature gradually to prevent thermal stress induced cracking. The 100 nm aluminum source and drain electrodes are deposited by thermal evaporation (power controlled by Sorensen Power Supplies DCR 7-300B) through a shadow mask at a pressure of 5×10^{-6} Torr. The deposition rate was controlled at 1.5 angstroms/sec. The shadow mask also defines the area of the channel region and each device has a channel width of 1000 μm and length of 200 μm. The devices are stored in a sealed container and kept at room temperature.

3.4 Device Characterization

3.4.1 Transfer characteristics

Transfer characteristics were measured in ambient air with a probe station and Agilent 4155C semiconductor analyzer controlled with Keysight EasyExpert software. Three probes were used

to connect the source, drain, and gate electrodes. The transfer curves were obtained by sweeping the gate-source voltage from -30V to 40V with a step size of 100 mV and maintaining a constant drain-source voltage of 20V. The EasyExpert software controls the data acquisition and records the drain-source current, linear mobility, saturation mobility, and maximum drain current for each measurement. Other electrical parameters such as on-off ratio, subthreshold swing, and threshold voltage can be calculated using the data obtained.

3.4.2 Stress and reliability characteristics

High current and high voltage stress tests are standard methods to determine the reliability of a device. This process subjects the device under extended periods of high current or high voltage conditions to simulate the long term operating conditions the device may undergo. High voltage stress can be divided into positive/negative stress as well as illuminated stress. In this work, the devices are subjected to positive bias stress (PBS). To do the PBS testing, the device is connected in the same way as measuring the transfer characteristics. A constant positive bias of 20V on the gate is maintained for 10000 seconds with single sweep measurements taken at 100, 200, 500, 1000, 2000, 5000 and 10,000 seconds. The resulting transfer curves can be analyzed and relevant parameters such as the threshold voltage shift can be extracted from the data.

4. Results and Discussion

4.1 Device Structure

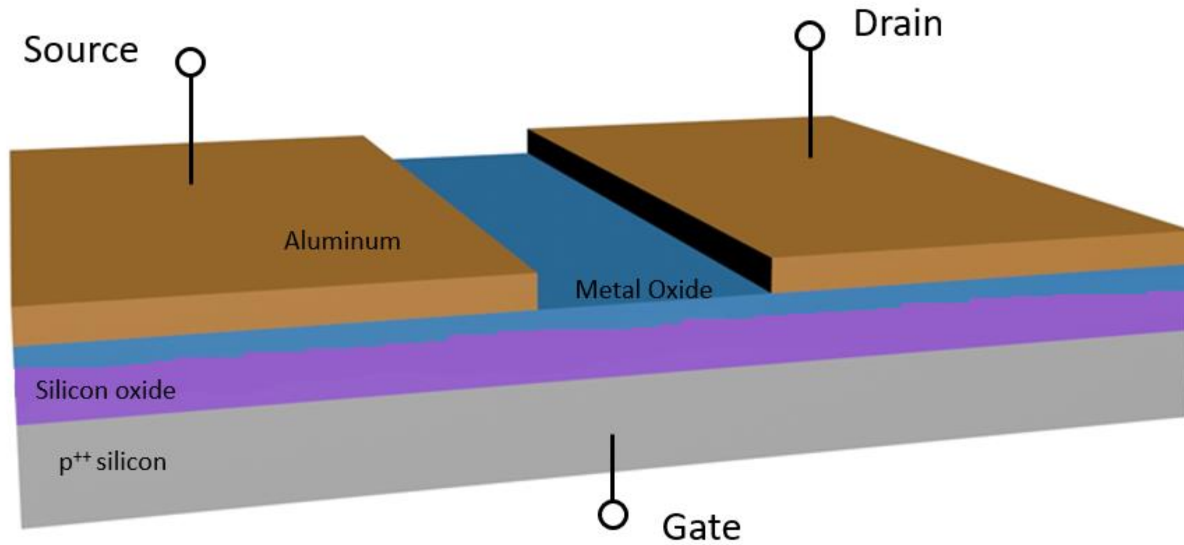

Figure 8: Schematic structure of bottom gate, top contact TFT device used in this work

Figure 8 shows the representative device structure used in this study. The device architecture employs the bottom gate, top contact structure and has three terminals. The bottom gate is heavily doped (p^{++}) silicon and the gate insulator is a 100 nm thick thermally grown silicon oxide. The active layer metal oxide layer is either indium oxide or IGZO and the top contacts are 100 nm of thermally evaporated aluminum patterned using a shadow mask.

4.2 Additive Enhancements

One of the major concerns when employing a solution based processing method is the wettability that the precursor solution has with the substrate. Having good wettability between the precursor solution and substrate allows for better film quality and less defects such as pinhole formation. Furthermore, when adjusting the ratios of metal precursors in the solution, having good

wettability will allow the film to have a closer ratio to what was originally intended in the precursor solution. There are many methods to improve the wettability of the substrate. Since the substrate used in this study is silicon dioxide, a hydrophilic interaction will increase the wettability with the substrate. One of the common methods to increase the hydrophilic character of the surface is to use UV/ozone treatment. The high energy light provided by the UV removes some of the organic residues on the surface and enhances hydrophilic character. In addition, the ozone produced in the chamber will also modify the surface energy of the surface for better hydrophilic interaction. In addition to using UV light as a wettability promoter, there are chemical additives that can be incorporated into the precursor solution to promote wettability. In this case, one such chemical additive used was ethylene glycol. The idea behind using ethylene glycol is due to the presence of dangling bonds that are present on the surface of the silicon oxide. These dangling bonds can interact with the two hydroxyl groups on ethylene glycol that create favorable bond interactions. This bond formation will lower the surface energy between the silicon oxide substrate and the precursor. One visual inspection technique to verify the increased wettability is to observe the rate of spreading on the wafer when dispensing the solution on the substrate. For pristine solutions, the 2-methoxyethanol solvent is generally hydrophilic but the rate of spreading on the substrate is slow. Upon the addition of ethylene glycol, the rate of spreading on the substrate surface increases rapidly. Nevertheless, this is simply a visual inspection that is difficult to quantify. In order to quantitatively determine the surface effects of ethylene glycol in this system, we have used a contact angle measurement system. As shown in Figure 9, the IGZO additive enhanced solution nearly completely wets the silicon wafer, displaying a contact angle of 3.8 degrees. The figure on the right displays the contact angle for water on the same silicon substrate for reference.

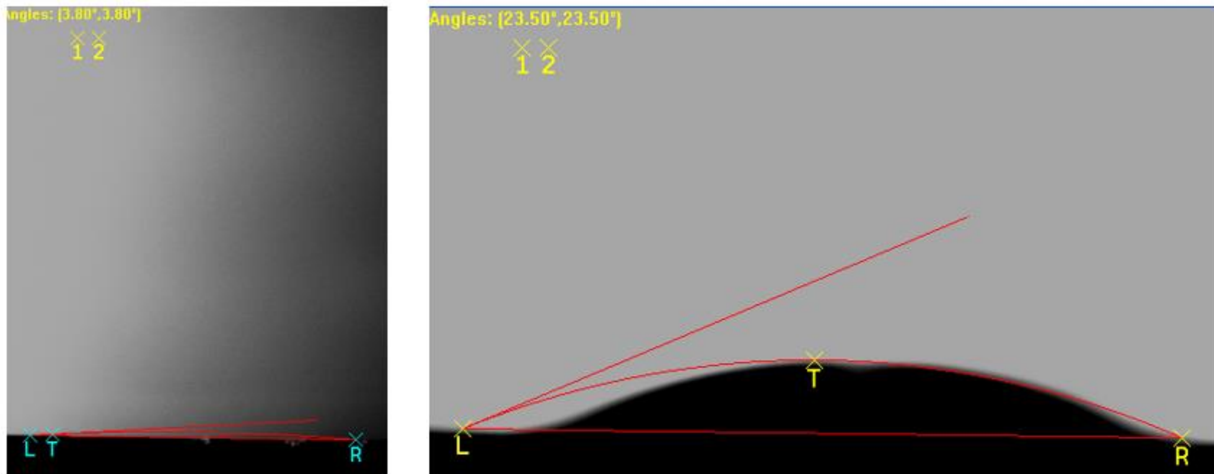

Figure 9: Contact angle measurement for IGZO additive enhanced (left) solution and water (right) as reference.

The water droplet exhibits more hydrophobic behavior than the IGZO solution with ethylene glycol enhancements and forms a contact angle of 23.5 degrees with the substrate.

One major concern when utilizing solution processed amorphous oxide semiconductors is the annealing temperature that is required to form the oxide. Traditionally, the conventional process requires supplying external heat through an oven or hot plate to constantly provide energy to overcome the activation energy barrier. The oxide formation reaction is endothermic and requires the constant addition of energy throughout the anneal process to be sustained. Furthermore, these temperatures are usually above 400°C, making them incompatible with polymer and other soft substrates. In order to overcome this problem, the addition of acetylacetone as a chemical additive is employed in this study. The idea behind the addition of acetylacetone is to convert the oxide formation process from an endothermic one to an exothermic process. The addition of acetylacetone changes the reaction into a combustion reaction, with the acetylacetone serving as fuel and the nitrate anions from the metal precursor serving as the oxidizer. In addition, the employment of acetylacetone has two major effects.

First, acetylacetone will serve as the fuel for the combustion reaction, allowing for an in situ method for generating heat throughout the anneal process. This combustion process is an exothermic reaction, so much less heat is required to overcome the activation energy barrier. Also, once overcome, the reaction will sustain itself without the need to constantly supply external heat energy. This will significantly lower the temperature required for the anneal step. Second, acetylacetone will serve as a chelate for the metal precursors in the solution. The chelating complex will stabilize the metal and prevent premature metal-oxo networks from forming. A premature formation of metal-oxo network will degrade the film deposition process and lead to more defects and possibly an inactive device. To confirm the effects of the acetylacetone in the film formation, an FT-IR spectra of the film at different conditions was performed. As can be seen in Figure 10, the initial spun film contains major peaks at 1300 cm^{-1} and 3300 cm^{-1} corresponding to the hydroxyl groups and organic and carbonyl groups that are present in the film.[7] Even after the post bake at 100°C for one minute, these peaks are still largely remaining. That is reasonable since the baking step is simply to remove the excess solvent after the film has been spin coated. The red line in Figure 10 corresponds to the spectra after the anneal step of 350°C. It is apparent that both the original peaks have disappeared, corresponding to the conversion of these organic and hydroxyl groups to the final oxide film. The final additive that was incorporated in the precursor solution is acetic acid. This chemical additive was selected to help increase the solubility of the metal nitrate precursors in the solvent. In higher concentrations of metal precursors, it becomes difficult to fully dissolve in the 2-ME solvent. Incorporation of acetic acid allows for higher amounts of metal precursor in the solution, which can be useful when trying to tune viscosity, film thickness, and other electrical parameters in the device.

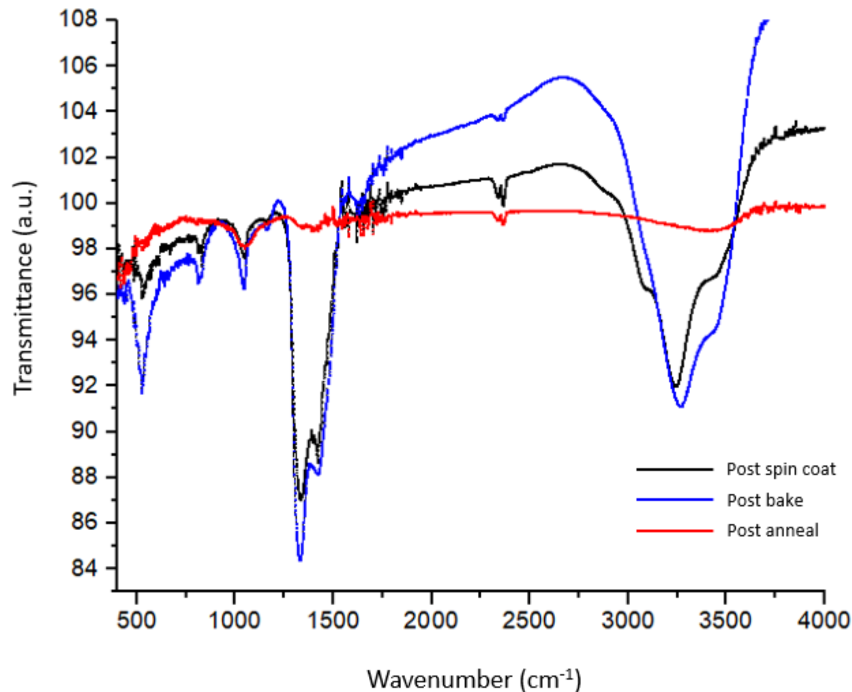

Figure 10:FT-IR spectra of post spin coating (black), post bake (blue) and post anneal (red) of additive enhanced IGZO film

Finally, acetic acid also supports the long term stability of the solution, allowing for more consistent and reproducible results even after being stored for long periods of time.

4.3 Device Performance

One parameter that affects solution processed TFT performance a lot is the annealing temperature and time that is used to form the amorphous oxide semiconductor channel. As previously mentioned, the activation energy needed to overcome the oxide formation barrier is large and usually requires large amounts of externally supplied energy. In using the combustion method, the activation energy barrier is overcome by an in situ generation of heat as the film is being formed. The idea of using the combustion method for local generation of heat relies on the nitrates as the oxidizer and acetylacetone as the fuel. With this in mind, it is possible to design an

experiment where the oxidizer and fuel ratio are varied along with different annealing temperatures to see the effect on the final device performance. One logical place to start is to match the oxidizer and fuel atomic ratio in the solution precursor. Since the amount of nitrate anions are fixed depending on the concentration of metal, the ratio can be adjusted by varying the amount of acetylacetone added. In this case, a temperature study was conducted based on matching oxidizer and fuel ratios with a metal concentration of 0.15M. Four different annealing temperatures were used (150°C, 200°C, 250°C, and 300°C) each annealed for one hour and the transfer curves of each of the devices is plotted in Figure 11. As can be seen, the device performance varies greatly depending on the annealing temperature used. For the 150°C device, not enough thermal energy was supplied to the film to overcome the formation energy barrier of converting initial sol precursor to final oxide network. The device never manages to turn on for the entire sweep of gate voltage from negative 30 to positive 40 volts. In the next device, just a mere 50 degrees more dramatically enhances the device from completely inactive to possessing transistor-like characteristics. Nevertheless, for this device, the turn on voltage is largely positive and the hysteresis is exceeding ten volts. This can be due to partial conversion of precursor network to metal oxide network, leading to large amounts of oxygen vacancies and organic contaminants still within the film. These impurities make the device unstable and difficult to operate. In the next device, the 250°C device has much less hysteresis and is capable of reaching nearly one milliamp of current. This level of current is important for driving high end consumer electronics such as in the active matrix OLED TFT backplane. Finally, taking a look at the 300°C device, the turn on voltage and hysteresis levels are similar to the 250°C device, but one thing that is apparent is the increased levels for off current and on current.

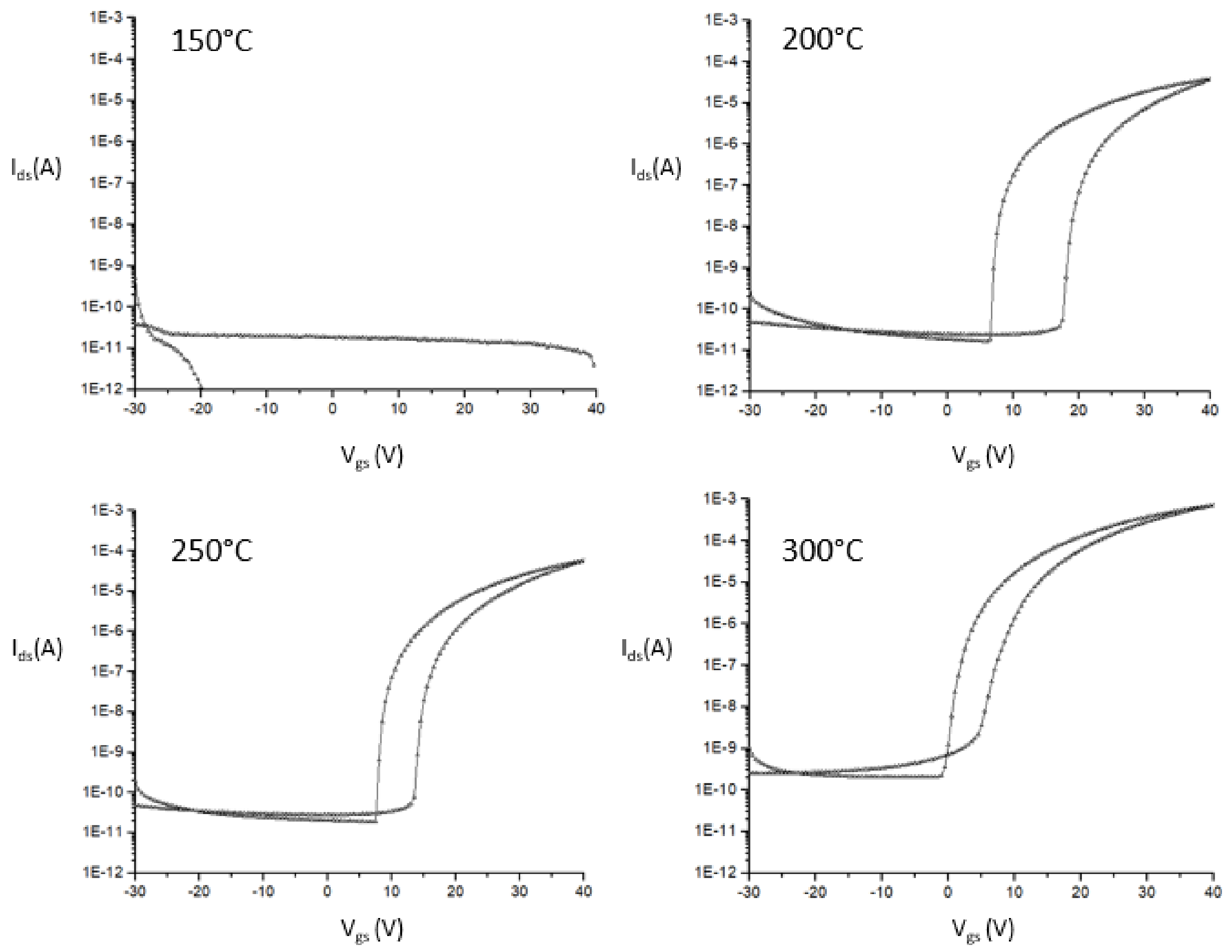

Figure 11: Transfer curve characteristics for four different annealing temperatures of solution processed indium oxide TFT's with matching fuel and oxidizer ratios for initial precursor solution.

The on current has now increased beyond one milliamp which is good in terms of device performance. Nevertheless, the tradeoff is the increase in leakage current, which has crept up to nearly one nano-amp. The higher anneal temperature provides thermal energy for oxygen atoms to detach from the metal oxide lattice and creating oxygen vacancies which ultimately increases carrier concentration. This will increase the on and off current, so even though a larger turn on current is achieved, the on/off ratio remains about the same. This can then become a design choice for whether the end user would like to have higher currents to drive larger loads at the

expense of a larger leakage current, or would prefer more modest current levels with a small leakage current.

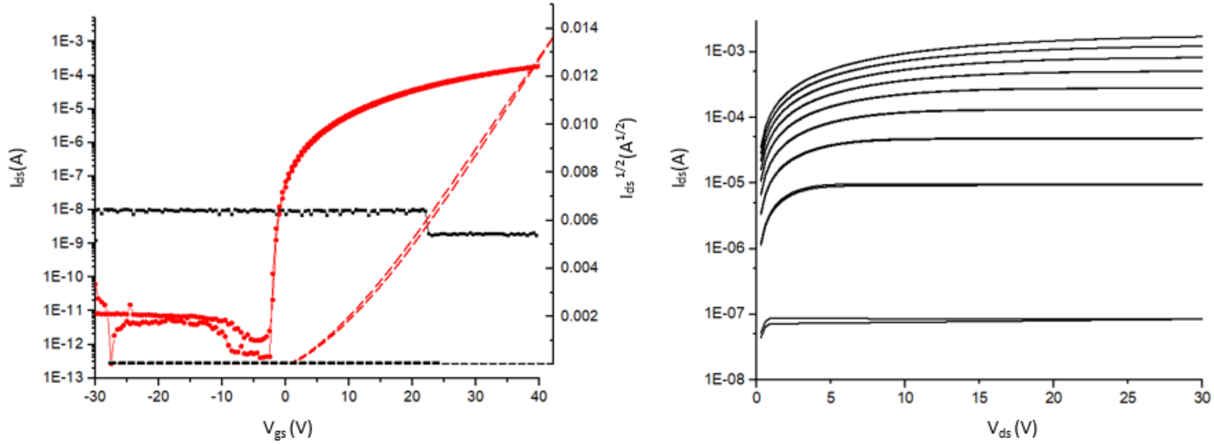

Figure 12: Transfer (left) and output (right) curves for pristine and additive enhanced IGZO TFT

Next, IGZO devices were fabricated with and without additives to determine the effects of additives on final device performance. The transfer and output characteristics are plotted in Figure 12. For the transfer curve, the red lines correspond to the additive enhanced device and the black lines correspond to the pristine device. The y-axis on the left is the drain current plotted on a log scale. On the right side, the y-axis plots the square root of the drain current. The square root of the drain current plotted against gate voltage is a common technique to extract the threshold voltage of a device. Here it is plotted simply for reference. Taking a look at the transfer curves, it is apparent that the additives do a lot for the IGZO device. Without the addition of additives, the device never turns on and does not exhibit transistor behavior. Upon the addition of additives, the device turns on promptly near zero volts and displays high on/off ratio, on current and minimal hysteresis. The additives in this case not only lower the activation energy barrier for good metal oxide formation, they also promote better film formation leading to denser

films and less defects. These important factors are reflected in the final device characteristic, as minimal hysteresis is an important indicator of low defect levels in the film.

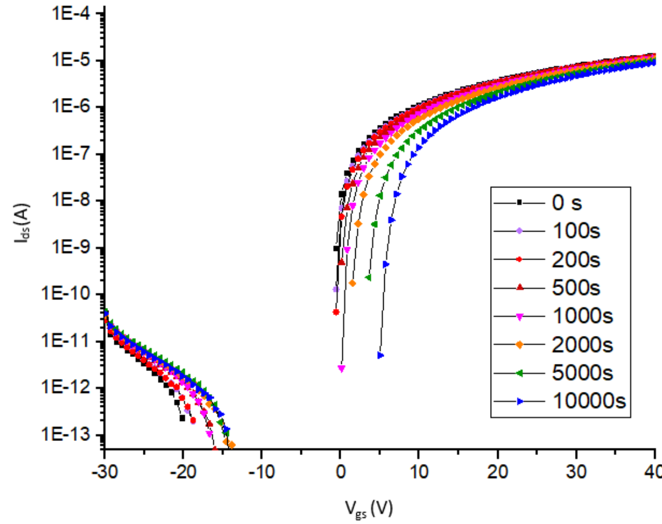

Figure 13: Transfer curve characteristics and threshold voltage shift of IGZO TFT under PBS stress test

One of the final tests to perform on a device is the stress and reliability testing. This test is important in characterizing how the long term behavior of the device will be after undergoing high operating loads. The method of stress testing employed on this device is the positive bias stress test. This operation supplies a 20V bias between the gate and source terminal and the drain current is measured at regular time intervals. In this work, the total amount of time used to stress the device was 10,000 seconds. The constant voltage on the gate induces strong electric fields through the insulator layer and in to the semiconductor layer. The carriers are forced to the semiconductor-insulator interface for long periods of time and also leads to injection of carriers in to the defect states within the interface. Since the carriers in IGZO are electrons, once these carriers become trapped in the defect states, it becomes more difficult for the interface to allow the flow of carriers due to repulsive interactions. This induces a positive shift in gate voltage for the amount of voltage that needs to be additionally supplied for the same amount of current to

flow. These shifts in gate voltage also correspond to a shift in threshold voltage which is one of the main degradations to the device. As can be seen in Figure 13, these shifts become apparent above 500 seconds of stress. Upon completion of the stress test, the device has shifted more than seven volts since the initial turn on position before stressing. This number gives an estimate to the quality of the film (related to the amount of defect states at the interface) as well as the long term reliability of the device if it were to operate in for example a display backplane application.

4.4 Proposed Mechanism

From a device perspective, it is apparent that the addition of acetylacetone as an additive dramatically enhances device performance and lowers the anneal temperature required to fabricate a TFT with high quality electrical characteristics. These electrical measurements are further supported by the FT-IR spectra, where the combustion synthesis mechanism clearly shows the removal of organic impurities in the film upon annealing. It is now important to investigate the mechanism that governs the effects of acetylacetone addition. Rim and coworkers have proposed the idea of chelation between the acetylacetone and the metal cation in solution, where the process of metal ligand formation can be catalyzed by either acid or base.[7] In that scenario, the acetylacetone in solution can exist as an equilibrium between the keto and enol isomer. The addition of acid or base as a catalyst can push the equilibrium to the enol side and assist in the formation of metal ligand formation.

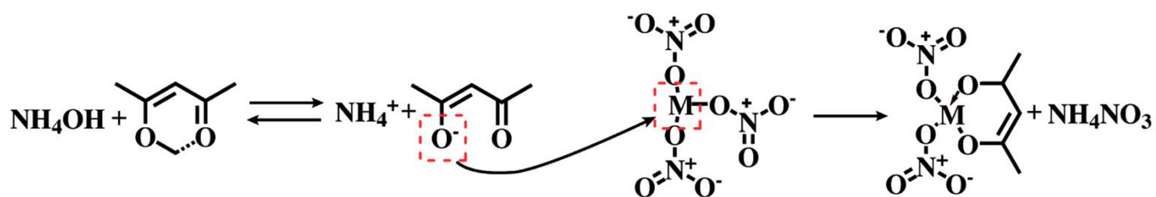

Figure 14: Chemical structure of a metal organic precursor synthesized via complexation reaction[7]

As shown in Figure 14, the acetylacetone can displace the nitrate cations and bind with the metal center, forming a stable metal complex. In this case, the base used to catalyze this reaction is ammonium hydroxide. The metal complex can serve as a protecting group to prevent premature formation of metal-oxo network formation, which may affect film quality if present before the spin coating procedure. Upon the addition of heat, the metal complex can dissociate and allow the combustion reaction to occur, with acetylacetone serving as the fuel and the nitrate anions serving as oxidizer. This pathway then lends itself to an exothermic reaction that can continually produce heat on its own while annealing is occurring. The byproducts produced of combustion such as water and carbon dioxides can then leave the film in the vapor phase.

The other mechanism that is of interest is the threshold voltage shift observed during the high voltage PBS stress test. This is important because if the device shifts in threshold voltage too much beyond an acceptable value, the circuit would not behave as designed since the transistor would not be able to turn on at the provided voltage. The origin of this shift in threshold voltage is based on the idea of charge trapping at the interface that induces repulsion, making it more difficult for charge carriers to be transported. The other aspect that is responsible for the degradation of the device that is less often considered is the intrinsic joule heating (self-heating) effects that are present during the high voltage and high current stress tests. This idea of self-heating during the operation of the device can exacerbate the effects of defect induced instability and lead to higher shifts in threshold voltage. This mechanism can be tied in with the area of the channel, specifically looking at the gate width as a function of temperature in the channel. These scenarios were modeled and simulated using COMSOL Multiphysics simulation and are shown in Figure 15.

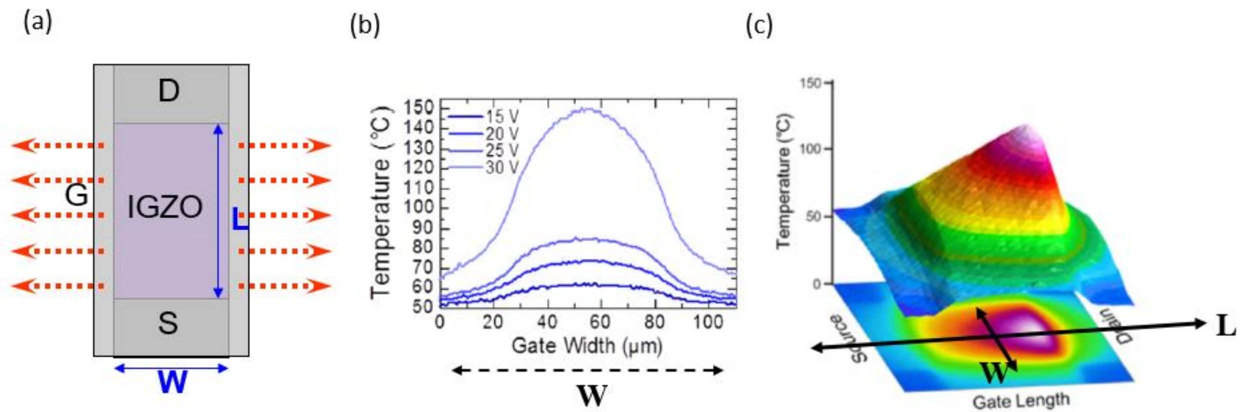

Figure 15: (a) Schematic of heat dissipation in a TFT as a function of gate width (b) Channel temperature plotted along the axis of gate width at several representative gate voltages (c) COMSOL Multiphysics simulation of the temperature distribution in the channel

Figure 15(a) is a schematic of heat dissipation in the IGZO TFT as a function of the gate width. As can be seen, the larger the gate width becomes, the more difficult it is for heat to be dissipated in the device. This is also supported by the plot in (b) which shows that the center of the device usually sees the highest temperatures due to difficulties in heat dissipation. Figure 15(b) plots the temperature along the axis of the gate width at various representative gate voltages. Finally, the areal distribution in the device is simulated with the z-axis representing the temperature throughout the device. One interesting thing to note is the peak temperature centered near the drain side of the device. This is due to the large positive voltage usually applied on the drain side inducing a large electric field on the drain end. When electrons are in this field, they are quickly accelerated and bombard the drain side with rapid velocities. This large amount of carrier bombardment induces heat generation on the drain end. As a result, the reliability issues are usually observed to be degradations on the drain end.

5. Conclusions

Much work has been done on the advancement for solution processed transistors with high performance and scalability for large area electronics. In this work, the effects of additive enhancements has been investigated on the effects of film formation, processing temperature, and electrical parameters such as mobility, on-off ratio, and threshold voltage shifts under PBS stress test. In particular, the effects of ethylene glycol, acetylacetone, and acetic acid were investigated in a metal oxide precursor solution. It was demonstrated that ethylene glycol dramatically improved the wettability of the concentrated IGZO solution and resulted in a minimal contact angle of 3.8 degrees. This helps to improve film formation quality and allow for higher concentrations of metal precursor to be dissolved in solution while still maintaining hydrophilic interaction on the substrate. The addition of acetylacetone allowed for the fabrication of high performing TFT's at low annealing temperatures (less than 300°C) through the combustion synthesis route that was previously not possible with conventional additive free precursors. Acetylacetone also serves as a protecting group to prevent premature formation of metal oxide network in solution. Finally, the addition of acetic acid improved the solubility of the metal precursor in the solution and allowed for higher concentrations of metal precursor to be dissolved in solution, which becomes important if higher viscosity precursors for thick films are needed. The addition of these three additives produced devices with near zero turn on voltage, excellent on-off ratio ($> 10^7$), and superior stability (less than eight volts of threshold voltage shift at 10,000 seconds of PBS). These improvements open new possibilities for fabrication of flexible electronic devices and next generation large scale consumer electronics.

6. Future Work

The primary objective in this work was to investigate the effects of chemical additives in the precursor and how they affected device performance. There was no optimization of the device relating to architecture or physical parameters of the device. Other types of device architecture such as top gate bottom contact could be investigated to compare the effects on device performance. Experiments could also be performed where the gate length and width are varied to study fringe field effects and self-heating effects.

All of the devices used in this work were global gate devices, meaning every single transistor shares the same gate and gate insulator. Future experiments could utilize patterning methods to fabricate local gate and gate oxides for individual transistors. That would help to decrease gate leakage and improve stability during stress tests. The transistors could also be passivated to minimize the effects of moisture induced instability during device operation.

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