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UNIVERSITY OF CALIFORNIA SANTA BARBARA

Design of III-Nitride Hot Electron Transistors

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

Geetak Gupta

Committee in charge: Professor Umesh K. Mishra, *Chair* Professor Mark J. W. Rodwell Professor Steven P. DenBaars Professor Debdeep Jena, Cornell University

December 2015

The Dissertation of

Geetak Gupta is approved:

Mark J. W. Rodwell

Steven P. DenBaars

Debdeep Jena

Umesh K. Mishra, Committee Chair

November 2015

Design of III-Nitride Hot Electron Transistors

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by

Geetak Gupta

Dedicated to my parents Dr. Rajeev Gupta and Vibha Gupta

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Geetak Gupta

CURRICULUM VITAE

Geetak Gupta

Research Interests

Solid-State Device Physics, High-frequency Amplifiers, Power electronics, Digital Electronics, Energy Efficiency, III-N Devices.

Education

2015	Ph.D. in Electrical and Computer Engineering GPA 4.0			
	University of California Santa Barbara			
2013	M.S. in Electrical and Computer Engineering GPA 4.0			
	University of California Santa Barbara			
2010	B.Tech. in Electrical and Computer Engineering CPI 9.8/10.0			
	Indian Institute of Technology Kanpur			
Experience				
2010-2015	Graduate Student Researcher			
	University of California Santa Barbara			
Winter-Spring	Teaching Assistant, Semiconductor Device Physics			
	University of California Santa Barbara			
Summer 2009	Undergraduate Researcher			
	University of California Santa Barbara			
Honors				
2010 Best B.Tech. Project, Electrical Engineering				
	Indian Institute of Technology Kanpur			
2010	Sridhar Memorial Prize (Best student, B.Tech. EE)			
	Indian Institute of Technology Kanpur			

2010	TODAI-IIT Scholarship (Awarded to two final year students at IITK)		
	Indian Institute of Technology Kanpur		
2006-07, 2007-08,	Academic Excellence Award		
2008-09	Indian Institute of Technology Kanpur		
2006	All India rank 1 in National ISC Board Examinations		
	St. Mary's Academy, Meerut		

Journal Publications

- [1] **Geetak Gupta**, Elaheh Ahmadi, Umesh K. Mishra, "Establishment of the design space of III-N hot electron transistors for high current gain and extraction of mean free path using base thickness scaling," Submitted to EDL, 2015.
- [2] Matthew Laurent, Geetak Gupta, Donald J. Suntrup III, Umesh K. Mishra, "Barrier Height Inhomogeneity in Quarternary III-N Schottky diodes," Submitted to JAP, 2015.
- [3] Chirag Gupta, Yuuki Enatsu, **Geetak Gupta**, Umesh K. Mishra, "High breakdown voltage p-n diodes on GaN on sapphire by MOCVD," Submitted to PSS, 2015.
- [4] Donald J. Suntrup III, **Geetak Gupta**, Haoran Li, Stacia Keller, Umesh K. Mishra, "Barrier height fluctuations in InGaN polarization dipole diodes," *Applied Physics Letters*, 107, 173503, 2015.
- [5] Donald J. Suntrup III, Geetak Gupta, Haoran Li, and Umesh K. Mishra, "Measuring the signature of bias and temperature-dependent barrier heights in III-N materials using the hot electron transistor," *Semiconductor Science and Technology*, 30, 105003, 2015.
- [6] Riccardo Soligo, Srabanti Chowdhury, **Geetak Gupta**, Umesh K. Mishra, and Marco Saraniti, "The Role of the Base Stack on the AC Performance of GaN Hot Electron Transistor," *IEEE Electron Device Letters*, 36, 669-671, 2015.
- [7] Geetak Gupta, Elaheh Ahmadi, Karine Hestroffer, Edwin Acuna, and Umesh K. Mishra, "Common Emitter current gain >1 in III-N HETs with 7nm GaN/InGaN base," *IEEE Electron Device Letters*, 36, 439-441, 2015.
- [8] Geetak Gupta, Matthew Laurent, Haoran Li, Donald J. Suntrup III, Edwin Acuna, Stacia Keller, and Umesh K. Mishra, "Design Space of III-N Hot Electron Transistors using AlGaN and InGaN polarization-dipole barriers," *IEEE Electron Device Letters*, 36, 23-25, 2015.

- [9] Donald J. Suntrup III, **Geetak Gupta**, Haoran Li, and Umesh K. Mishra, "Measurement of the hot electron mean free path and the momentum relaxation rate in GaN," *Applied Physics Letters*, 105, 263506, 2014.
- [10] Matthew Laurent, Geetak Gupta, Steven Wienecke, Azim Muqtadir, Stacia Keller, Steven DenBaars, and Umesh K. Mishra, "Extraction of net interfacial polarization charge from Al_{0.54}In_{0.12}Ga_{0.34}N/GaN high electron mobility transistors grown by metalorganic chemical vapor deposition," *Journal of Applied Physics*, 116, 183704, 2014.
- [11] **Geetak Gupta**, Matthew Laurent, Jing Lu, Stacia Keller, and Umesh K. Mishra "Design of polarization-dipole-induced isotype heterojunction diodes for use in III-N hot electron transistors," *Applied Physics Express*, 7, 014102, 2014.
- [12] Shalini Lal, Jing Lu, Geetak Gupta, Brian Thibeault, Steven P. Denbaars, and Umesh K. Mishra "Impact of Gate-Aperture Overlap on the Channel-Pinch-off in InGaAs/InGaN-based Bonded Aperture Vertical Electron Transistor (BAVET)," *IEEE Electron Device Letters*, 34, 1500, 2013.
- [13] Jing Lu, Dan Denninghoff, Ramya Yeluri, Shalini Lal, **Geetak Gupta**, Matthew Laurent, Stacia Keller, Steven P. DenBaars, and Umesh K. Mishra, "Very high channel conductivity in ultra-thin channel N-Polar GaN/(AlN, InAlN, AlGaN) high electron mobility hetero-junctions grown by metalorganic chemical vapor deposition," *Applied Physics Letters*, 102, 232104, 2013.
- [14] Sansaptak Dasgupta, Jing Lu, Nidhi, Ajay Raman, Christophe Hurni, Geetak Gupta, James S. Speck, and Umesh K. Mishra, "Estimation of Hot Electron Relaxation Time in GaN using Hot Electron Transistors," *Applied Physics Express*, 6, 034002, 2013.
- [15] Seshadri Kolluri, Stacia Keller, Dave Brown, Siddharth Rajan, Geetak Gupta, Umesh K. Mishra, "Influence of AlN interlayer on the anisotropic electron mobility and the device characteristics of N-polar AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors grown on vicinal substrates," *Journal of Applied Physics*, 108, 074502, 2010.

<u>Conference Publications</u>

- [1] Geetak Gupta, Elaheh Ahmadi, Umesh K. Mishra, "Common Emitter Current Gain >1 in III-N Hot Electron Transistors by Enabling GaN/InGaN Base Scaling Using Novel Base Contact Methodology," *International Symposium on Compound Semiconductors*, Santa Barbara, June 2015.
- [2] Matthew Laurent, Donald J. Suntrup III, Geetak Gupta, Stacia Keller, Umesh K. Mishra, "Measurement of AlInGaN/GaN Schottky Diode Barrier Height by

Temperature-dependent Current-Voltage Measurements," *International Symposium* on Compound Semiconductors, Santa Barbara, June 2015.

- [3] Chirag Gupta, Enatsu Yuuki, **Geetak Gupta**, Stacia Keller, Umesh K. Mishra, "Ultra-Low N-Type Doping and High Breakdown Voltage (Field ~ 1.5MV/cm) in GaN P-N Diodes Grown on Sapphire by MOCVD," *International Symposium on Compound Semiconductors*, Santa Barbara, June 2015.
- [4] Donald J. Suntrup III, **Geetak Gupta**, Haoran Li, Stacia Keller, Umesh K. Mishra, "Measurement of the hot electron mean free path in GaN," *APS March Meeting*, San Antonio, Texas, 2015.
- [5] Matthew A. Laurent, Geetak Gupta, Azim Muqtadir, Stacia Keller, Umesh K. Mishra, "Extraction of Net Interfacial Polarization Charge from MOCVD-grown AlInGaN/GaN Heterostructures," *Electronic Materials Conference*, Santa Barbara, USA, June 2014.
- [6] **Geetak Gupta**, Matthew Laurent, Donald J.Suntrup III, Stacia Keller, Umesh K. Mishra, "Estimation of hot-electron mean free path in GaN using a III-N Hot Electron Transistor," *Electronic Materials Conference*, Santa Barbara, USA, June 2014.
- [7] Geetak Gupta, Matthew Laurent, Haoran Li, Donald J.Suntrup III, Edwin Acuna, Stacia Keller, Umesh K. Mishra, "Common Emitter operation of III-N HETs using AlGaN and InGaN polarization dipole induced barriers," *Device Research Conference*, Santa Barbara, USA, June 2014.
- [8] **Geetak Gupta**, Jing Lu, Stacia Keller, Umesh K. Mishra, "Reduction of reverse bias leakage using polarization induced barriers in III-N Isotype Heterojunctions for use in III-N Hot Electron Transistors," *International Workshop on Nitrides*, Sapporo, Japan, October 2012.
- [9] **Geetak Gupta**, Jing Lu, Shalini Lal, Stacia Keller, Umesh K. Mishra, "CF₄ Plasma Treatment for Leakage Reduction in N-Polar III-N Hot Electron Transistors with Collector-Up Structure," *International Symposium on Compound Semiconductors*, University of California Santa Barbara, CA, USA, August 2012.
- [10] Jing Lu, Dan Denninghoff, Matthew Laurent, Geetak Gupta, Stacia Keller, Steven P. Denbaars, Umesh K. Mishra, "Influence of a Thin InAlN Cap Layer on the Device Performance of N-Polar InAlN/GaN MISHEMTs Grown by MOCVD," *International Symposium on Compound Semiconductors*, University of California Santa Barbara, CA, USA, August 2012.
- [11] Geetak Gupta, Jing Lu, Ajay Raman, Sansaptak Dasgupta, Stacia Keller, Umesh K. Mishra, "DC Characteristics of N-Polar AlGaN/GaN/AlGaN Collector Up Hot Electron Transistors," *Electronic Materials Conference*, Pennsylvania State University, College Park, PA, USA, June 2012.
- [12] Seshadri Kolluri, Stacia Keller, Dave Brown, Siddharth Rajan, **Geetak Gupta**, Umesh K. Mishra, "Influence of AlN interlayer on the anisotropic electron mobility and the device characteristics of N-polar AlGaN/GaN MIS-HEMTs grown on vicinal

substrates," *International Symposium on Compound Semiconductors*, University of California Santa Barbara, CA, USA, August 2009.

Invited Talks

- [1] Geetak Gupta, Matthew Laurent, Donald J. Suntrup III, Haoran Li, Stacia Keller, Umesh K. Mishra, "Design and Fabrication of III–N Hot Electron Transistors," *Nitrides Seminar*, University of California Santa Barbara, February, 2014.
- [2] Geetak Gupta, Jing Lu, Sansaptak Dasgupta, Matthew Laurent, Stacia Keller, Umesh K. Mishra, "III–N Hot Electron Transistors," *Teledyne Scientific and Imaging*, Thousand Oaks, CA, USA, April 2013.
- [3] Umesh K. Mishra, Dan Denninghoff, Jing Lu, **Geetak Gupta**, "Recent Advances in High Frequency Semiconductor Devices," *Lester Eastman Conference*, Brown University, Providence, RI, USA, August 2012.

ABSTRACT

Design of III-Nitride Hot Electron Transistors

Geetak Gupta

III-Nitride based devices have made great progress over the past few decades in electronics and photonics applications. As the technology and theoretical understanding of the III-N system matures, the limitations on further development are based on very basic electronic properties of the material, one of which is electron scattering (or ballistic electron effects). This thesis explores the design space of III-N based ballistic electron transistors using novel design, growth and process techniques. The hot electron transistor (HET) is a unipolar vertical device that operates on the principle of injecting electrons over a high-energy barrier (ϕ_{BE}) called the emitter into an n-doped region called base and finally collecting the high energy electrons (hotelectrons) over another barrier (ϕ_{BC}) called the collector barrier. The injected electrons traverse the base in a quasi-ballistic manner. Electrons that get scattered in the base contribute to base current. High gain in the HET is thus achieved by enabling ballistic transport of electrons in the base. In addition, low leakage across the collector barrier (I_{BCleak}) and low base resistance (R_B) are needed to achieve high performance. Because of device attributes such as vertical structure, ballistic transport and low-resistance n-type base, the HET has the potential of operating at very high frequencies. Electrical measurements of a HET structure can be used to understand high-energy electron physics and extract information like mean free path in semiconductors.

The III-Nitride material system is particularly suited for HETs as it offers a wide range of $\Delta E_c s$ and polarization charges which can be engineered to obtain barriers which can inject hot-electrons and have low leakage at room temperature. In addition, polarization charges in the III-N system can be engineered to obtain a high-density and high-mobility 2DEG in the base, which can be used to reduce base resistance and allow vertical scaling.

With these considerations in mind, III-N HETs had been explored in our research group earlier and gave us encouraging common base IV characteristics. Common emitter transistor operation was, however, not observed due to high R_B and I_{BCleak}. This thesis discusses several design and process challenges associated with the HET in general and specific to the III-N system. Many of these challenges like R_B, I_{BCleak}, and high energy injection were solved using novel combinations of hetero-structure and polarization engineering, device fabrication, and growth. Common-Emitter operation (with current gain ~ 0.1) was demonstrated in III-N HETs for the first time using injection and collector barriers induced by AlGaN and InGaN polarization-dipoles. In order to improve current gain, different parts of the III-N HET base which contribute to scattering, were identified. A novel base contact methodology using selective etching of GaN with respect to AlN was developed to enable base scaling. Aggressive scaling of all parts of the base was then used to increase current gain. A maximum gain of ~3.5 was demonstrated using a 1.5nm AlN layer as the emitter, 2nm GaN base and 2nm In_{0.2}Ga_{0.8}N as the collector P-D. This is the highest reported DC current gain in III-N HETs to date. The III-N HET structure was also used to extract the mean free path of hot-electrons ($\lambda_{mfp} = 6nm$) in GaN. The extracted value of mean free path has significant implications for any scaled devices which use ballistic or quasi-ballistic electron transport. We believe that the work presented in this dissertation provides a pathway for high gain in III-N HETs and eventual realization of their high frequency potential.

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1 INTRODUCTION

There has been a huge progress in the field of III-Nitride based technologies in the past few decades. This material system has been researched since the 1970s[1], but difficulties in developing a viable growth technique limited the progress. It first attracted widespread attention with the demonstration of the InGaN-based blue light-emitting diode (LED) and laser in the mid-1990s[2], [3]. Since then, tremendous progress has been made towards both understanding of nitride material properties[4], [5] and growth[6], [7] as well as fabrication of electronic[8] and photonic devices with excellent performance.

Nitride semiconductors have a very unique set of properties making them attractive for various applications. Broadly, the major applications of III-N based technologies can be classified into four categories namely, blue/green LASERs, LEDs, power electronics, and RF electronics (Figure 1.1). The large direct bandgap (0.7eV to 6.2eV) that can be covered with the Al-In-Ga-N alloy system allows the use of these semiconductors in further advancing the LED and laser technology from UV[9] to infrared frequencies. In recent years, there has been demonstration of green lasers operating at 535 nm[10] using InGaN quantum wells. Nitride-based solar cells[11] have recently demonstrated excellent external quantum efficiency and spectral response. Besides favorable optoelectronic properties, the III-Nitrides also possess excellent electronic transport properties. Due to the presence of high spontaneous and piezoelectric polarization in the III-Nitride system, high charge density 2DEG with ~1-2x10¹³ cm² charge and ~2000 cm²/V.s mobility have been demonstrated[12].

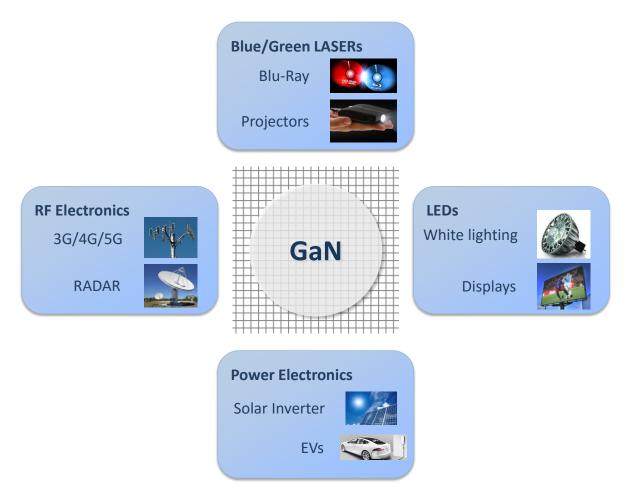


Figure 1.1 Applications of III-Nitride material system based technologies

The presence of polarization also enables some unique design possibilities. Excellent high frequency performance of InAlN/GaN based Ga-Polar HEMTs with maximum $f_T \sim 450$ GHz and maximum $f_{MAX} \sim 550$ GHz[13] have been obtained recently. Power densities of 32W/mm at 4GHz (55% PAE)[14] and 10W/mm at 40GHz (34% PAE)[15] have been demonstrated in Ga-Polar HEMTs. N-Polar III-N HEMTs offer the unique advantage of a built in back barrier and the ability to scale channel thickness both of which can improve gate control and provide significant advantages for scaling. AlGaN/GaN based N-Polar HEMTs have shown $f_T.L_G$ product of 16.8 GHz.µm ($L_G = 40$ nm)[16] and InAlN/GaN based N-Polar HEMTs have

recently shown $f_T \sim 200$ GHz and $f_{MAX} \sim 400$ GHz[17]. Power density of 12W/mm at 4GHz (55% PAE)[18] have also been shown in N-Polar HEMTs. In the area of power electronics, III-Nitride based devices, due to their capabilities of supporting high breakdown voltage and low on resistance, R_{on} , have already emerged as an efficient and important technology for various applications[19].

Despite the remarkable progress in III-Nitride based device technologies, the pathway to obtaining ultra-high frequency ($f_T > 500$ GHz) transistors based on the InAlGaN/GaN HEMT technology is unclear. The low electron saturation velocity in the 2DEG combined with parasitic delays[20], [21] could limit the possibility of obtaining an ultra-high frequency III-N HEMT with considerable breakdown voltage and hence high output power. Bipolar devices (HBT) in the III-N system have shown high gain and high breakdown voltages, but have limited high-frequency performance benefits. The major issue in the III-N HBT is the presence of a p-type layer which has very low conductivity due to the deep acceptor nature of Mg in GaN[22]. This has prevented widespread use of bipolar devices in the III-Nitrides.

Towards this goal, we explore III-Nitride based Hot Electron Transistors. The Hot Electron Transistor (HET) is a vertical unipolar device operating in a regime where high electron velocities via quasi-ballistic transport are attainable. Even though scattering rates are high in the III-Nitrides, current gain is achievable in the HET as discussed in Chapter 3-5. With appropriate scaling technologies and reduction of parasitic delays the III-N HET could be used as an ultra-high frequency device as discussed later in this chapter and in Chapter 6.

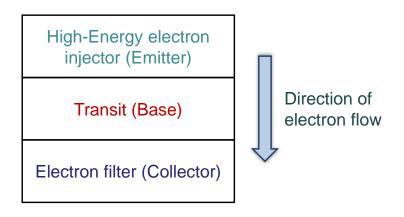


Figure 1.2 General Description of a HET

The complex non-equilibrium electron transport in the device and its dependence on several scattering mechanisms also makes the HET an extremely interesting scientific tool to understand fundamental electron transport in the III-Nitrides. This chapter discusses the basic operation principles of a HET, the family of HET designs, key advantages provided by the III-N system for HETs, and a discussion on the potential uses of a III-N HET.

1.1 Hot Electron Transistor Operation

The most general description of a HET consists of three distinct regions (Figure 1.2), a highenergy electron injector (emitter), a transit region (base), and an electron energy filter (collector). The emitter, in non-equilibrium, injects electrons into the base (hot electrons) such that they have a high energy compared to the thermal energy when they enter the base. The base has a thermal population of electrons (cold electrons) either due to bulk doping or some other means (modulation doping, polarization doping etc.). The thermal population of electrons in the base effectively screens the collector from the emitter. As the injected hot electrons traverse the base, they suffer from scattering which can be elastic or inelastic and finally they

reach the collector. The collector acts as an energy filter for electrons at the collector edge of the base. It allows hot electrons to go across but blocks cold electrons for a wide range of non-equilibrium across it. Electrons which have suffered from scattering in the base therefore are not hot enough to cross the collector and get reflected back. These electrons eventually become part of the cold electron population in the base and contribute to base current. The electrons at the collector edge of the base which have sufficient energy, make it across the collector and form the collector current. The next few pages briefly discuss phenomenon related to each part of the transistor to develop a general understanding of a HET. This will enable discussions on advantages/disadvantages of various HET designs in different material systems until a more detailed description is developed in later chapters (Chapter 5 in particular).

Hot Electron Injection

The hot electron injector is typically made using an energy barrier e.g. tunnel barrier, resonant tunnel barrier, superlattice etc. The simplest emitter is a unipolar diode with a heterojunction, schottky or electrostatic barrier at the emitter-base interface. This ensures that electrons entering the base have energy greater than or equal to the barrier height. As the emitter-base junction is forward biased, electrons are injected into the base by thermionic emission over this barrier. The general approach to calculating currents in a quantum mechanical model is by using,

$$J_{z} = \frac{2q}{(2\pi)^{3}} \iiint \frac{1}{\hbar} \frac{\partial E(k)}{\partial k_{z}} T_{A-B}(E(k,z),k) f_{A}(E(k)) \left(1 - f_{B}(E(k))\right) dk_{x} dk_{y} dk_{z}$$

where J_z is the electron current flowing from region A \rightarrow B and f_A and f_B are the Fermi-levels in the two regions. In order to evaluate this expression, the first thing needed is the tunneling probability of electrons across the emitter barrier. Since these structures are uniform along the x and y dimensions, the electron momentum is conserved along x and y as electrons transit across the emitter-base interface. The transmission probability therefore depends only on the electron k_z and the E(k,z)¹. E(z) is basically the band diagram of the system. Near conductionband minima, E(k) is a simple parabolic relationship. With these three idealizations, it is possible to write a computer code for calculating transmission probability across arbitrary structures². Even with the transmission probability, a complicated integral has to be performed to calculate J_z . With a few more approximations i.e. parabolic bands on both sides, $(1-f_B) \sim 1$, and the Boltzmann approximation, the contributions of the k_x and k_y components to J_z can be integrated independently. All that is left is the k_z integral which can be performed numerically. Results of such calculations for actual HET structures will be presented later. To summarize, since k_x and k_y are conserved, hot electron injection only produces shifts in the $\langle k_z \rangle^3$ of the electron distribution. Consider the case of a simple step-down potential with a thermal distribution of electrons on the higher-potential side (left side). To the left of the step, $\langle k_x \rangle =$ $\langle k_{v} \rangle = \langle k_{z} \rangle = 0$ and $\langle \Delta k \rangle \sim kT$. As electrons cross the barrier, $\langle k_{x} \rangle = \langle k_{v} \rangle = 0$, but $\langle k_{z} \rangle \sim kT$.

 $^{^{1}}$ E(k,z) is a description of the electron potential energy as a function of momentum and position.

² Code for calculation of transmission probability and current density across arbitrary band diagrams written by Trey Suntrup.

 $^{^{3}}$ <k> is the ensemble average momentum of the electron distribution.

 $\sqrt{2m\phi_{EB}/\hbar^2}$, where ϕ_{EB} is the height of the step. Thus, in a HET, hot-electrons entering the base have a large k_z compared to k_x and k_y.

Hot Electron Collection

The collector in a HET can also be made using an electron energy filter like tunnel barrier, resonant tunnel barrier, superlattice etc. The simplest collector is again a unipolar diode with a heterojunction, schottky or electrostatic barrier at the base-collector interface. Just like the emitter barrier, the collector barrier too acts as a k_z filter. Only electrons with a high enough k_z have high transmission probabilities across the collector. The collector also has a drift region with an electric field that sweeps away collected electrons towards the collector contact layer.

Base Transit

The base is a transit region where a fraction of the injected hot-electrons suffer from scattering events due to various interaction mechanisms. The fraction that suffers from scattering events is determined by the length of the base, the average scattering rate of electrons in the base, and the electron velocity. The scattering mechanisms can be elastic (ionized impurities, alloy etc.) or inelastic (inter and intra-valley acoustic and optical phonons etc.). Elastic scattering mechanisms result in momentum relaxation but not energy relaxation whereas inelastic scattering events can result in both. Since both emitter and collector barriers are k_z filters, the HET is sensitive to energy as well as momentum relaxation. As hot-electrons enter the base, they have a high $\langle k_z \rangle$. During base transit, therefore, the hot-electron $\langle k_z \rangle$ decreases due to scattering events. A fraction of the injected electrons thus gets reflected at the collector. It can

be assumed that these reflected electrons eventually fully relax in energy and momentum to become part of the thermal electron population in the base. The hot-electron scattering process is discussed in more detail in Chapter 4.

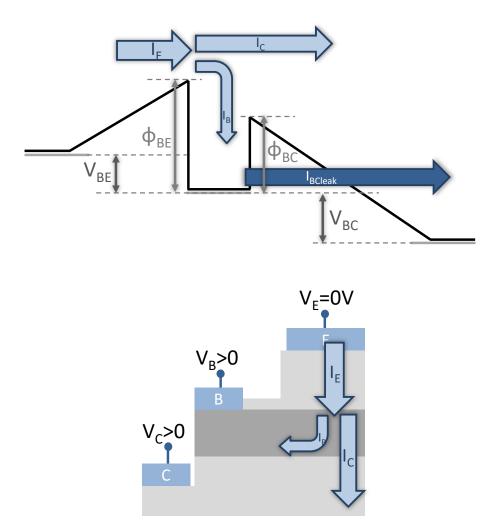


Figure 1.3 (a) Schematic conduction band-diagram and (b) Layer structure illustrating the various electron current paths in a HET under normal bias conditions

Non-Equilibrium Fermi Levels and Transistor Action

The HET has three Fermi-levels, emitter, base and collector which are controlled via external sources of voltage or current. This means that in each of these three regions, the density of electrons is high enough for there to be a well-defined Fermi-level. The only reason, thus, for having a large thermal population of electrons in the base is to provide a constant Fermi-level across the entire base. If the electron density/mobility is low, the Fermi-level will change along the direction of current flow and result in resistive voltage drops which degrade device performance. The device structure used for a HET is a double-mesa structure (Figure 1.3) which means that J_E and J_C flow vertically while J_B flows laterally. Thus, the base resistance (R_B) is a sum of contact resistance and lateral sheet resistance. The emitter resistance however is a vertical resistance.

Transistor action in a HET is achieved by fixing the emitter Fermi-level to ground ($V_E = 0V$), applying a small positive bias on the base ($V_B > 0$) and a larger positive bias on the collector ($V_C > V_B$). The positive bias on the base results in a net flow of electrons from the emitter towards the base. The electron distribution changes as electrons traverse the base and the final distribution is partially relaxed in energy and momentum. A fraction of the final electron distribution is thus unable to make it across the collector barrier and gets reflected back. This forms the base current (J_B) of the device. The fraction of the electron distribution with a large enough k_z that makes it across the collector barrier, forms the collector current (J_C). As V_B is increased, the forward bias across the emitter-base junction (V_{BE}) increases, thus resulting in more current injection (higher J_E). The J_C and J_B increase proportionally resulting

in the first primary property of a transistor called *transconductance*. To a first order, J_C and J_B do not change as V_C is increased, thus resulting in the second primary property of a transistor called *saturation*. With these two properties, it is possible to call the device a *transistor*. In reality, as V_C is increased, J_C increases thus resulting in output conductance (R_{out}). In addition, the leakage of thermal electrons from the base across the collector (J_{BCleak}) increases with V_C . The V_C at which the J_{BCleak} becomes comparable to J_C is termed as the breakdown voltage (V_{Cbr}). Therefore, for the HET to be a *useful transistor*, a few more conditions need to be imposed.

1.1.1 Design Principles

DC Performance

In order to design a HET that is useful at DC, a few more parameters are defined here. Transfer ratio (α) is defined as $\alpha = J_C/J_E$ and current gain (β) is defined as $\beta = J_C/J_B$. For good DC performance, $\alpha \sim 1$ and β as large as possible are needed. This ensures that most of the injected electrons are collected and the device gain is high. A large V_{Cbr} (or low J_{BCleak}) is needed for a large saturation regime and low R_B is required for uniform biasing of the entire device area.

Using these additional DC metrics, the design space for HETs can be further narrowed down. A thin base $t_B < L_{mfp}$ (scattering mean free path for hot-electrons) is needed to ensure ballistic transport of hot-electrons and thus, maximum α . Quantum mechanical reflection of hot-electrons at the collector barrier can occur even if the electron energy is larger than the

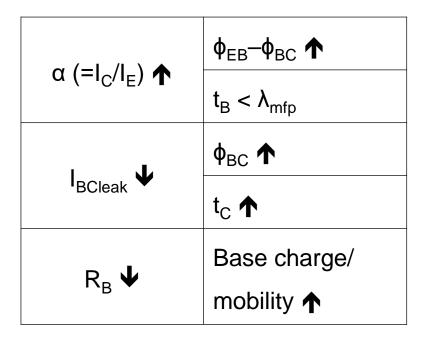


Figure 1.4 Design tradeoffs in a HET for DC performance

collector barrier height. A large difference between emitter and collector barrier heights (ϕ_{EB} - ϕ_{BC}) is therefore required to reduce the effect of such reflections. A large collector barrier height (ϕ_{BC}) and thickness (t_C) are needed to block leakage currents across the collector and thus reduce J_{BCleak}. In order to reduce R_B, high electron concentration and mobility are required in the base. From the summary in Figure 1.4, it is clear that there are a few tradeoffs inherent to even the most general HET. A large ϕ_{BC} decreases J_{BCleak} but also decreases α and β since the injection energy (ϕ_{EB}) has to be larger than ϕ_{BC} for high gain. A thin base increases α and β but can also result in higher R_B.

AC Performance

	Transit 🗸	$t_{b} \Psi$, $t_{c} \Psi$
f _⊤ ↑	C _{cb} ↓	t _c ↑
	Charging $oldsymbol{\Psi}$	I _c ♠
	R _B ↓	
f _{max} ♠	C _{cb} ↓	t _c ↑

Figure 1.5 Tradeoffs in a HET for high-frequency performance

This part discusses the general tradeoffs inherent to the HET for RF performance. The highfrequency figures of merit for a transistor are the current gain cutoff frequency f_T and the power gain cutoff frequency f_{MAX} . Both of these are defined in terms of parameters of the small signal equivalent circuit which is very similar to that of an HBT.

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + \frac{\partial V_{BE}}{\partial J_C} (C_{je} + C_{cb}) + C_{cb} (R_{ex} + R_C)$$
$$f_{MAX} = \sqrt{\frac{f_T}{2\pi R_{bb} C_{cb}}}$$

The f_T is divided into two parts, transit delays and RC delays. The first term is the base transit delay and its value is $\tau_B = t_B/v_B$, where t_B is the base thickness and v_B is the ballistic velocity of electrons in the base. To a first order, the ballistic velocity can be approximated by just the

<u>Chapter 1 Introduction</u>

group velocity of electrons at the injection energy. The second term is the collector transit delay and its value is $\tau_{\rm C} = t_{\rm C}/2v_{\rm s}$, where $t_{\rm C}$ is the collector thickness and $v_{\rm s}$ is the saturated electron velocity in the collector drift region. The third term contains the capacitances of each junction and the dynamic resistance of the device. The final term is an RC delay related to the base-collector capacitance. In order to increase $f_{\rm T}$, thus, $v_{\rm B}$ and $v_{\rm s}$ need to be large. The capacitances are inversely proportional to the thickness of the barriers. Therefore, the barrier thicknesses need to be large for low capacitances. The device needs to be operating at high current densities for low dynamic resistance. Finally, the parasitic resistances need to be small. To increase $f_{\rm MAX}$, low base resistance and low $C_{\rm cb}$ are needed. As summarized in Figure 1.5, this introduces additional tradeoffs in the device design. $t_{\rm C}$ is one of the most critical parameters as it plays a role in determining J_{BCleak}, $\tau_{\rm C}$, and $C_{\rm cb}$.

1.2 Historical Perspective on HETs

A brief introduction to the Hot Electron Transistor family is presented below. Since most textbooks and review articles do not have an adequate description of these devices, this section serves as a brief introduction to the several transistor topologies which can be termed as Hot Electron Transistors keeping in mind the description in the earlier section. The base transit and collection mechanism is very similar for most of the HET topologies made in the past. This classification is therefore based on the different injection mechanisms used for HETs.

1.2.1 Tunnel Injection

The emitter-base current in this class of HETs is a tunneling current through a barrier, either by direct tunneling or Fowler-Nordheim tunneling. Historically, the first proposal of a hot electron device was made by Mead[23] in 1961. His proposed device, the MOMOM (metaloxide-metal-oxide-metal) transistor, was based on electrons tunneling through a thin oxide into a high energy state in the metal base (Figure 1.6).

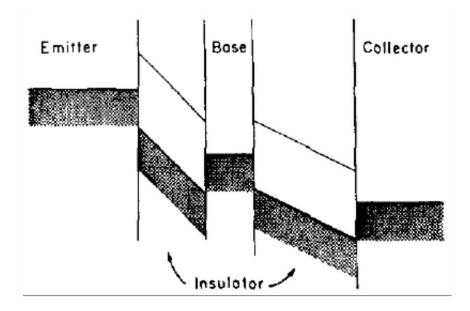


Figure 1.6 The MOMOM (metal-oxide-metal-oxide-metal) HET[23]

These high-energy electrons were then able to surmount the second oxide barrier and get collected in the metal electrode. The oxides used here were Al_2O_3 and Ta_2O_5 . The MOMOM was a potentially fast device for two main reason; it employed a thin base region which resulted in low transit times for the injected electrons and the metal base layer enabled low R_B . Since the mean free path of hot electrons in metals is short, and pinhole-free thin metal layers were difficult to fabricate, current gain was not demonstrated in these transistors. The low injection

and collection efficiency due to traps resulted in the discontinuation of further research in these devices.

The hot electron camel transistor was proposed by Shannon in 1979[24]. The injection mechanism here was based on tunneling of electrons across a metal-semiconductor junction. The entire structure was made from Si. The simplest structure used a Schottky metal on top of an n+ base layer as the injector. Another structure had a thin p+ layer between the metal

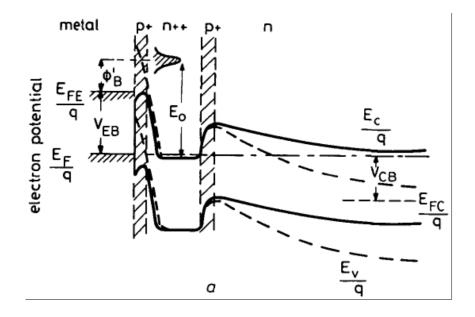


Figure 1.7 The Hot-Electron Camel Transistor[25]

and the n+ base in order to increase injection energy (Figure 1.7)[25]. The collector for both cases was a 'camel' diode which was an n-p-n unipolar diode. The collector barrier height was determined primarily by the doping and thickness of the p-type layer. A maximum current gain of 10 was demonstrated in these devices. However, a large output conductance was observed in the transistors and the large current gain was obtained only at large collector bias.

The THETA (tunneling hot electron transistor amplifier) was proposed by Heiblum in 1981[26]. The device structure employed a thin layer of $Al_{0.35}Ga_{0.65}As$ as a tunnel emitter. An n-type GaAs layer with an ohmic metal contact on top was used as the source of electrons as opposed to a schottky metal contact in the previous designs. The base collector heterojunction was graded to reduce quantum mechanical reflection, and an $Al_{0.25}Ga_{0.75}As$ layer was used as the collector (Figure 1.8). A maximum current gain of 50 was demonstrated in these devices. The THETA was also used as a spectrometer to measure the energy spectrum of the injected

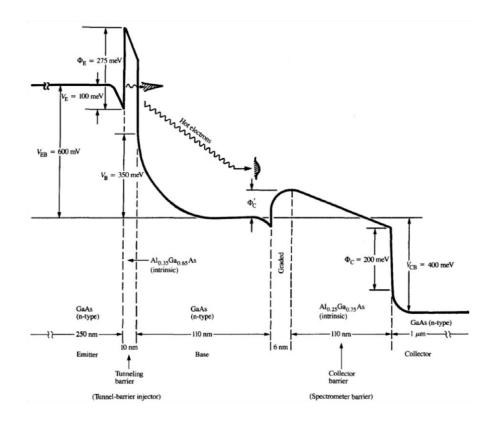


Figure 1.8 Tunneling Hot Electron Transistor Amplifier (THETA)[26]

hot electrons[27]. The low Γ -L valley separation in the III-As material system however limited the possibility of high injection energies. Also, as the barrier heights achievable in

AlGaAs/GaAs heterojunctions are small, the THETA was typically operated at 77K or lower thereby severely limiting its use in practical applications.

Recently, III-N HETs using tunnel injection have also been demonstrated (Figure 1.9)[28]. These transistors operate at room temperature and have demonstrated differential current gain ($\delta I_C / \delta I_B > 1$). However, the differential gain was observed only at very high collector bias and for a very small range of base current. The DC gain was < 1 and the devices suffered from very high output conductance. At present, III-N HET research is still in its early

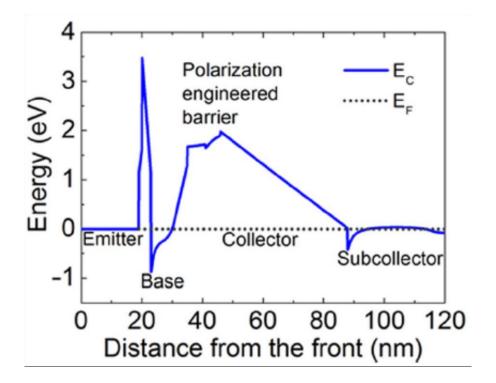


Figure 1.9 III-N Tunneling HET[28]

stages and the fundamental material properties of III-Nitrides allow for plenty of room for improvement. This work will expand upon the design methodology for III-N HETs and show

that room temperature DC gain with low output conductance and reasonable breakdown can indeed be achieved.

1.2.2 Resonant Tunnel Injection

This class of HETs use a resonant tunneling diode structure to inject electrons into the base at a specific energy. As an extension, some designs also use a superlattice diode structure to inject electrons into the base at a specific energy.

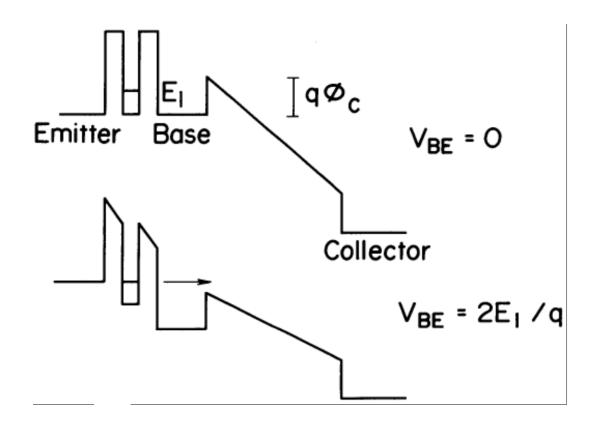


Figure 1.10 Resonant Tunnel HET[29]

The first Resonant Tunnel HET was demonstrated by Yokoyama in 1985 using an Al_{0.33}Ga_{0.67}As/GaAs/Al_{0.33}Ga_{0.67}As resonant tunnel diode as the hot electron injector[29]. The base was just n-type doped GaAs and the collector was again Al_{0.2}Ga_{0.8}As (Figure 1.10). The

emitter diode here exhibited a negative differential resistance which is expected in a Resonant Tunnel diode structure. This transistor had a current gain of 5. Using InGaAs/InAlAs RT structures, the current gain was increased to > 10[30]. High frequency performance with $f_T =$ 121GHz was also demonstrated[31]. These transistors were however operated at 77K or lower thus limiting their use in practical applications.

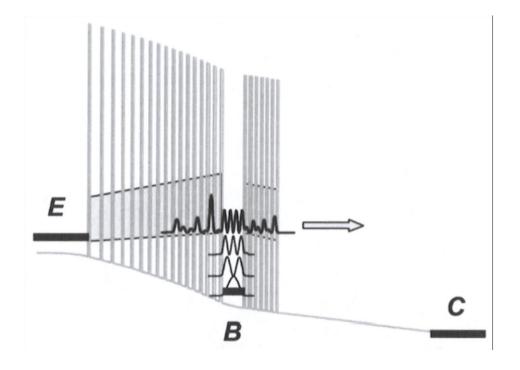


Figure 1.11 Superlattice HET[32]

Superlattice injectors were introduced very recently by Daoud in 2008[32]. This transistor used an InAs/AlSb superlattice as the hot electron injector and collector (Figure 1.11). A maximum current gain of ~5 was demonstrated at room temperature. High frequency performance with $f_T = 75$ GHz and $f_{MAX} = 88$ GHz was also shown[33]. The breakdown voltage of these devices, however, was only ~1V due to the small barrier heights achievable in this material/design.

1.2.3 Thermionic Injection

This class of HETs use thermionic injection similar to a schottky diode in order to inject hot electrons into the base. The electrons entering the base thus have an energy greater than the barrier height.

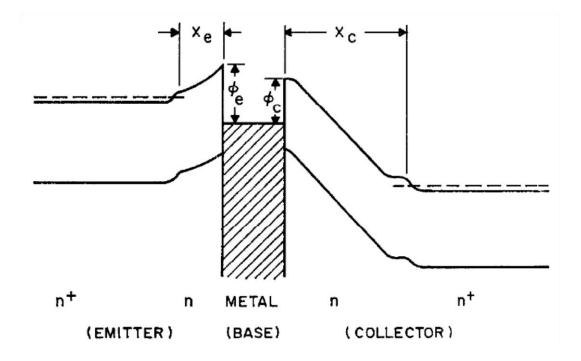


Figure 1.12 Semiconductor-Metal-Semiconductor (SMS) HET[34]

Metal base transistors which employ thermionic rather than tunneling injection of hot carriers into the base, were proposed by Geppert[35], Atalla[36] and Sze[34] in 1962 in the form of a semiconductor-metal-semiconductor (SMS) structure (Figure 1.12). The current gain was higher in these structures as compared to the MOMOM structures, but was still smaller than 0.5. This was related to various transport factors including the quantum mechanical reflection of electrons across the base-collector barrier.

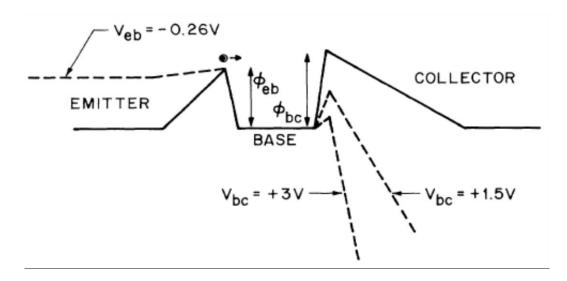


Figure 1.13 Planar doped barrier HET[37]

Unipolar diodes made using n-p-n structures (planar doped barriers) have also been used to implement emitter and collector barriers to construct a HET. Shannon demonstrated this transistor using Si in 1981[25] with a current gain of ~ 20 at RT. The transistor however had very high output conductance. Hayes demonstrated it using GaAs in 1985[37] and performed hot electron spectroscopy measurements using the HET structure (Figure 1.13). These measurements were performed at 4.2K.

In 1987, Levi demonstrated room temperature operation of a thermionic HET using an AlSb/InAs heterostructure for hot-electron injection[38] (Figure 1.14). The high base-collector barrier due to the InAs/GaSb heterojunction of 0.8 eV facilitated room temperature operation of this HET by reducing the J_{BCleak} . Gain of ~ 10 was demonstrated at room temperature thus making this structure the highest performance HET of all. However, HETs still lagged behind vertical bipolar devices like the InP/InGaAs HBT in terms of current

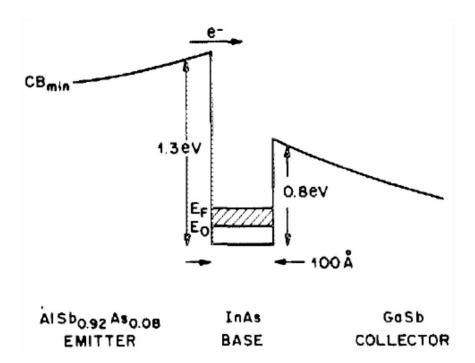


Figure 1.14 InAs/IIISb HET[38]

density, output conductance, and high frequency performance thus leading to a decline in research interest in HETs.

1.3 Motivation for III-N HETs

A discussion on the potential applications of HETs is incomplete without a serious discussion on HBTs as the two devices are very similar in many aspects. The HBT is a device capable of high drive currents and high gain. The vertical structure enables it to have great scalability. In contrast to the HET, HBTs in material systems like III-As, III-P, Si/Ge have shown excellent DC performance with very high gain and low base resistance. They have also shown excellent performance for applications in high frequency circuits beyond 100GHz[39], [40] and the f_{MAX} of InP HBTs has crossed 1THz[41].

HBTs in the III-N system, however, have had very limited success. The key contributing factor to this has been the lack of high conductivity in p-type layers in the III-N material system. The p-type dopant of choice in the III-N system is Mg which has a very high activation energy (~200meV) resulting in ~ 1% ionization[42]. Thus, it is very difficult to obtain layers with low sheet resistance. Although some solutions like polarization doping have been proposed, their full potential is yet to be realized. GaN being wide bandgap also makes it very difficult to find metals with a large enough work function to make a low barrier p-type contact. Thus, the high frequency performance of III-N HBTs is severely limited at present.

III-N HEMTs, on the other hand, have shown excellent performance for high-frequency and high-power circuits in the millimeter wave regime. f_{MAX} of ~500GHz has been demonstrated in III-N HEMTs. This success can be attributed to the presence of high density/mobility 2DEGs and large $\Delta E_c s$ available in the III-N system. HEMTs in the III-As/III-P material systems have also shown excellent high frequency performance with maximum f_T > 600GHz[43] and f_{MAX} >1THz[44].

HETs have been used extensively as scientific tools to investigate materials properties of several material systems. However, HET technologies in all previously explored material systems have not been able to compete with existing HBT and HEMT technologies for high frequency applications. The HET topologies discussed earlier have a few limitations. III-As based HETs typically suffer from high leakage currents at room temperature due to small barrier heights. The same issue exists for metal-semiconductor HETs based on GaAs or Si. Metal-oxide based HETs suffer from high trap densities at interfaces. The best performing HET in the past has been the AlSb/InAs/GaSb structure[38] with a gain of 10 at room

temperature. However, the devices demonstrated had relatively large output conductance and low current density. The structure also did not have much room for vertically scaling the base to increase gain without heavily sacrificing base resistance. In conclusion, at the time, HBTs provided a much better method of achieving high gain, low base resistance, low output conductance, and high current density simultaneously.

A III-N based HET offers the unique opportunity to achieve high gain and breakdown at room temperature along with vertical scalability and high-frequency performance unachievable in previous HET designs. Being a unipolar device, the HET can potentially have much lower base resistance compared to a bipolar III-N device. Ballistic operation can enable electron velocities much higher than vertical bipolar or lateral HEMTs. The presence of polarization in the III-N system also provides some key advantages. Polarization induced 2DEG in the base with high mobility (~1500 cm²/Vs), and high density (~2x10¹³ cm⁻²) can be used to achieve very low base resistance[45]. Polarization dipoles can also be used to induce barriers in the system without too much build-up of strain[46], [47]. The III-N system also has high ΔE_{cs} , making it a suitable material system for the HET.

1.3.1 High-Frequency Amplifier

The RF metrics for a III-N HET are very similar to the III-As/III-P HBT. It has been shown in HBTs that the key requirements to achieve THz operation are,

• Ultra-low Contact Resistances: Contact resistivities of the order of $10\Omega\mu m^2$ are required for all contacts. Low contact resistances of similar order of magnitude have

been shown to the III-Nitrides by using high n-type doping[48] and low band-gap InGaN[49].

- Low Base Resistance: Self-aligned process for low access resistance and a base sheet resistance of the order of 1 kΩ/sq. is typically required. Base resistance is more important for f_{MAX} and can be reduced by lateral scaling. Low sheet resistances have been shown in 2DEGs in III-N HEMTs[45]. However, in a HET, low base 2DEG resistance is required irrespective of emitter bias. This aspect is discussed in more detail later.
- High Current Density: J_C ~ 1 MA/cm² (or 10 mA/μm²) is required for low dynamic resistance. Owing to high density of states in the III-N system, theoretically, these numbers are achievable. The specific design used to achieve HETs in the III-N system, however, can introduce some complications as discussed in later chapters.
- High Collector Velocity: Collector transit delay forms a major portion of the total device delay (affects f_T) and hence a high collector velocity is required. Here, III-N HETs are at a slight disadvantage compared to III-As/III-P HBTs as the saturated drift velocity in III-N system is lower. This is a material constraint and will eventually determine the high-frequency potential of the device.

The key ingredients for high-frequency performance in HETs are present in the III-N system. Full band Monte-Carlo simulations for III-N HETs predict $f_T > 100$ GHz for current densities of ~ 100kA/cm²[50]. However, at this point it is difficult to make any strong claims regarding the ultimate high-frequency potential of HETs. As discussed later in this thesis, the specific device designs will play a key role in determining whether the high-frequency potential can be

realized practically. A more detailed discussion on the high-frequency tradeoffs for III-N HETs is presented in Appendix B.

1.3.2 Probe for Material Properties

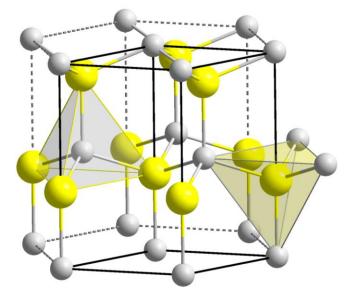


Figure 1.15 Wurtzite crystal structure of GaN and related alloys

III-Nitrides have a wurtzite type crystal structure which lacks inversion symmetry thus, giving rise to some of the most interesting properties of this material system. The electronic band structure of the III-N system has been studied theoretically in detail and many key aspects are well understood. However, there is no way to directly measure the behavior of high energy electrons. The HET can be used as a spectroscopic tool enabling us to probe high energy electron behavior directly using electrical measurements.

The transit length of electrons can be changed by varying the base thickness. With a longer transit distance, more electrons are likely to get scattered and not cross over the collector[51], [52]. Keeping the injection and collector barrier fixed, the mean free path of hot-

electrons can be extracted from transfer ratio vs base thickness for the given energy window. This experiment repeated for different energy windows can yield a very detailed measurement of high energy scattering rates in the III-N material system.

The energy distribution of hot-electrons can also be mapped by a slightly different structure[37]. If the collector barrier is made higher than the emitter barrier, none of the injected electrons get collected. As the collector bias is increased, the collector barrier gets lowered allowing more electrons to pass through. The exact electron distribution as a function of energy (collector barrier) can thus be extracted.

Since the collector of a HET is just an energy spectrometer for hot-electrons, it can be used it to study changes in injection energy of the HET. As demonstrated later, the best injection barrier for III-N HETs is a polarization-dipole based barrier. Lateral fluctuations in composition and thickness of the dipole layer can lead to non-uniformities in injection barrier height and thus injection energy of the hot-electrons. Defects like threading dislocations can provide pathways for electrons to be injected at energies lower than the injection barrier. Such non-uniformities can be observed and studied quantitatively using the collector of a HET as a spectrometer for injection energy[53]. The HET can therefore also be used to study material properties like defects and non-uniformities.

Electron velocity in the base can be calculated by subjecting the device to a magnetic field perpendicular to transport direction[54]. A magnetic field decreases the electron k_z and increases k_x and k_y thus decreasing current gain. The amount of decrease in k_z (and gain)

depends on the electron velocity. Thus, group velocity vs energy can be mapped out for GaN using only electrical measurements of a III-N HET.

1.4 Synopsis of Dissertation

This thesis is organized as follows,

- Chapter 1 introduces the Hot Electron Transistor and its operation and design principles. It also gives a brief history of the HET family and discusses the potential applications of a III-N based HET.
- Chapter 2 discusses the design of a HET in the III-N system using polarization-dipoles.
 Common emitter operation (β ~ 0.1) is shown for the first time in III-N HETs using this design methodology.
- Chapter 3 introduces a novel device design and process using AlN as an etch stop layer for base contacts, in order to enable base scaling. Current gain ~ 3.5 is demonstrated using this AlN based design.
- Chapter 4 describes hot-electron transport in detail and discusses the experiments conducted to find hot-electron mean free path.
- Chapter 5 discusses an InGaN quantum well HET design for high gain and discusses some challenges associated with the growth of such a structure. The conclusion and future directions are presented in Chapter 6.

2 III-N HET DESIGN AND COMMON

EMITTER OPERATION

This chapter introduces the basics of III-N HET design in order to derive the design constraints for good DC performance. Polarization engineering is a strong tool used in III-N HET design and its role is discussed in detail here. All the designs discussed in this thesis are simulated using BandEng, a self-consistent 1D Poisson-Schrodinger solver. The HET requires two unipolar back to back diodes such that there is a potential well formed in between. The simplest diode designs in the III-N system can be made using polarization-dipole (P-D) or heterojunction barriers. Both these methods can be used to design either of the two diodes needed for a HET.

The P-D barrier uses the basic concept of dipole charges to induce barriers in the conduction band. Planar doped barriers also use a similar concept to form barriers but the dipoles are formed by alternating p and n type ionized dopants. The barrier height is roughly proportional to the dipole moment of the charges. Using dopants, however, it is very difficult to achieve very large dipole moments as the doping concentration required is large. Consider for example a dipole composed of ionized dopants of both polarities where the width of the ionized dopant layer is the same for both (Figure 2.1).

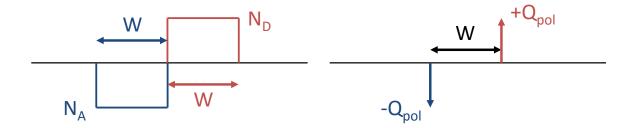


Figure 2.1 Charge profile of planar-doped and polarization-dipole barriers

Charge neutrality implies, $N_A W = N_D W \Rightarrow N_A = N_D$. The potential barrier due to such a charge distribution is then, $\phi_B = \frac{q}{\epsilon} N_A W^2$ and the dipole moment of this charge distribution is $p = N_A W^2$. Therefore, in order to induce a barrier of 1.5eV, the required dipole moment can be calculated to be $p \cong 7.5 \times 10^6 \ cm^{-1}$. If there are no restrictions on W, then even a low dopant density can be used to achieve the required barrier over a large distance. However, as we will see later, in a ballistic electron device, distance is a strong constraint and it is preferred to induce barriers over as small distances as possible. Figure 2.2 shows the doping concentration required as a function of dipole thickness in order to induce a 1.5eV barrier. The required doping is extremely large and difficult to practically realize. The same barrier can also be induced by a P-D layer (say AlGaN) sandwiched between two GaN layers. The polarization discontinuity between the materials leads the formation of a net polarization charge at the interface of GaN/AlGaN. The polarity of the charge is opposite for the two interfaces thus forming a dipole. As the Al fraction in AlGaN increases, the net polarization charge induced at the interface increases. Figure 2.2 also shows the Al fraction required to induce the same 1.5eV barrier using an AlGaN P-D layer. By using AlN and AlGaN, it is thus possible to achieve very large barriers over extremely thin dipole layers. The same argument applies for

InGaN induced barriers. P-Ds are therefore an extremely strong tool that is special to the III-N material system. It should be noted that in real P-D barriers, the use of heterojunctions also introduces ΔE_{Cs} in the band diagram which complicate the picture, however, the argument presented here still holds.

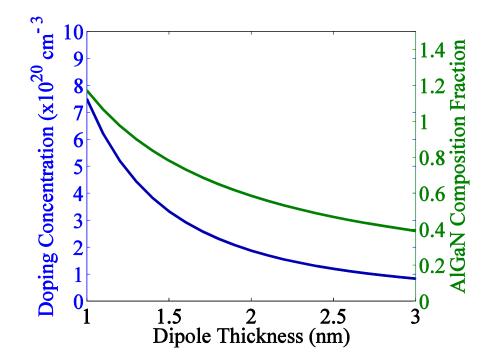


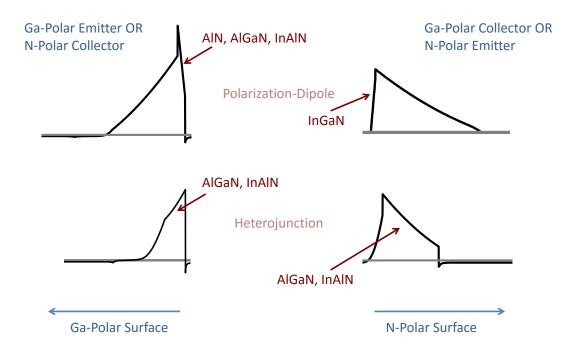
Figure 2.2 Comparison of a 1.5eV barrier induced by planar doping and polarization dipoles. The required doping concentration and AlGaN composition are plotted as a function of the dipole thickness.

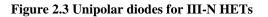
Heterojunction barriers are formed over a distance that is practically zero. P-D barriers on the other hand need a finite dipole thickness to form a barrier. For ballistic devices where distance is a strong constraint, heterojunction barriers can therefore have a significant advantage over P-D barriers. However, in III-Nitrides, heterojunctions cannot be decoupled from polarization discontinuities. Additional band engineering is needed to mitigate any negative effects that might result from polarization. Another issue with heterojunction diodes

in the III-N system is that most AlInGaN alloys are strained to GaN and have a finite critical thickness before the material loses its structural integrity. The implications of such issues on specific HET designs will be discussed throughout this thesis.

To summarize, there are 4 possible III-N HET designs within this framework (Figure 2.3) and 4 additional designs if the polarity of the structure is reversed (Figure 2.4). This thesis will focus only on the four Ga-Polar HET designs. A detailed discussion on the advantages/disadvantages of N-Polar HETs is presented elsewhere[52][53]. For the purpose of this discussion, it is sufficient to state that N-Polar HETs are at a disadvantage to Ga-Polar HETs in terms of current gain. Theoretically, any of these designs could be used to make a working transistor, however, taking into account III-N growth and DC figures of merit, some designs can have significant advantages. This chapter discusses Design 1 and Design 2 in detail to find out the best collector barrier design for a III-N HET.







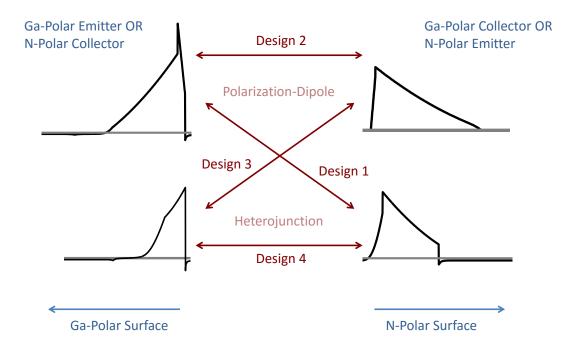


Figure 2.4 III-N HET Designs

2.1 AlGaN based Design

The growth and electrical characteristics of AlGaN/GaN heterostructures have been extensively studied in the III-N HEMT community. This motivated the use of AlGaN based Design 1 as the first design to be investigated in this work. Design 1 was also used to study III-N HETs in previous work[55].

The E-B barrier (top barrier) here is formed by a thin high composition AlGaN layer which acts as an electrostatic polarization-dipole. The height of this barrier can be increased by increasing the AlGaN thickness or composition. Due to a net positive polarization charge at the E-B interface, electrons accumulate in the base to form a 2DEG which can provide high base conductivity. The base here is a GaN layer. The B-C barrier (bottom barrier) is also formed by an AlGaN layer. The negative polarization-charge at the B-C interface partially depletes base charge. The height of the B-C barrier is thus a sum of the depletion potential and the ΔE_c between GaN and AlGaN. As discussed earlier, a thick collector barrier can help reduce J_{BCleak}, however, in this design since the collector barrier is made entirely of AlGaN, its thickness is limited by the amount of strain that the layer can handle before strain relaxation. For a 30% AlGaN layer, the critical thickness is 20-30nm [56]. The depletion of base charge due to negative polarization charge at the B-C interface degrades base resistance. Hence, this design adds two more tradeoffs on top of the ones that are present in the general HET.

2.1.1 Growth and Fabrication

Previous work used primarily MBE as the growth technique[57]. It has been shown that MBE has high vertical leakages due to presence of Ga metal in threading dislocations[58]. This work, therefore, starts out with MOCVD as the growth technique. The device structure grown by MOCVD uses a $Al_{0.45}Ga_{0.55}N$ polarization-dipole to form the E-B barrier. This layer was intended to be pure AlN but due to unintentional Ga incorporation during growth, it turns out to be AlGaN[59] (Figure 2.5). Since the Ga incorporation is unintentional, the higher growth rate of AlGaN in comparison to AlN results in an AlGaN layer thicker than what was intended i.e. an intended 4nm AlN layer could turn out to be ~ 8nm ~ 50% AlGaN. A 15% AlGaN layer is added on top in order to increase the 2DEG density. The B-C barrier is formed using a 20nm 30% AlGaN layer. The GaN base thickness used here is 15nm. Figure 2.6 shows the detailed layer structure and resulting conduction band-diagram of the structure grown.

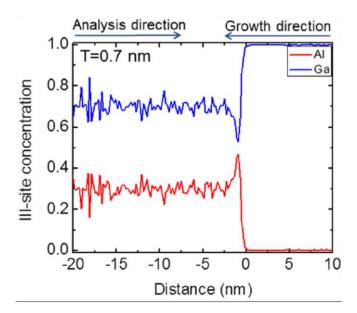


Figure 2.5 Atom Probe of MOCVD grown AlN layers[59]



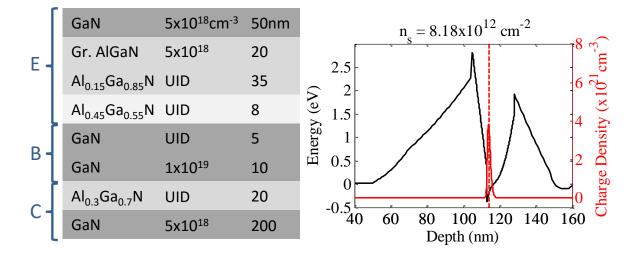


Figure 2.6 (a) Layer structure and (b) band diagram of AlGaN based HET

To test this structure, individual diodes were first grown on both Bulk GaN (Lumilog) and GaN on Sapphire. The diode structures were processed by a simple RIE etch and ohmic contact deposition. The full HET structure was then grown on Bulk GaN to test transistor performance.

Fabrication of the HET began with BCl_3/Cl_2 (20/5sccm, 10mT) based low power (15W) RIE timed to stop within 20nm of the 45% AlGaN layer (Figure 2.7). This preserves the base 2DEG in the access regions of the device. The GaN etch rate using this chemistry was measured to be ~ 6nm/min. The etched surface was very smooth (< 1nm RMS roughness) even after 15min of etching. This etch also showed very little selectivity between GaN and AlGaN. A second etch, using the same conditions, was used to etch into the GaN base layer and was followed by deposition of Al/Au base contacts. Small variations in etch rate, lack ofprecise values of layer thicknesses, lack of etch selectivity, and small errors in the AFM measurements for etch calibration make this step the most tricky and critical step of the entire process. Since the base thickness is only ~ 10nm, an error of even a few nanometers can result

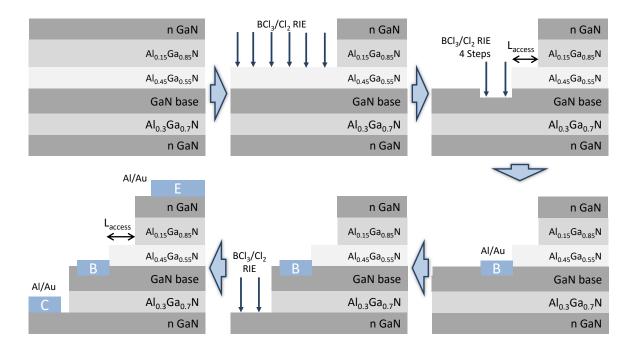


Figure 2.7 Process Flow for the III-N HETs

in an excessive under-etch or over-etch both of which can be disastrous for the HET. Therefore, across the sample, different dies with different etch times for the second etch were fabricated simultaneously to ensure that at least some of them form ohmic base contacts. This two-step etch process for base contacts was developed as a part of this work. A final etch was performed to expose the collector contact layer. This was followed by emitter and collector ohmic contact deposition in the same step.

2.1.2 Diode and Transistor Results

The E-B diode was rectifying on both Bulk GaN and Sapphire with a difference of ~ 3 orders of magnitude between forward and reverse currents at 5V bias (Figure 2.8a)[46]. The key difference between the two substrates was lower reverse leakage and absence of kinks in forward bias regime on Bulk GaN. The B-C diode was barely rectifying when grown on

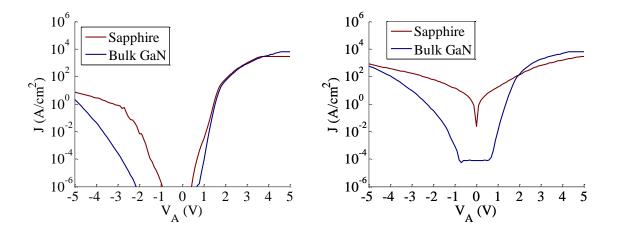


Figure 2.8 I-V characteristics of (a) E-B and (b) B-C diodes grown separately on both Bulk GaN and Sapphire

Sapphire (Figure 2.8b). On Bulk GaN the diode showed clear rectification. It could hold only \sim 3V however before reverse leakages became comparable to forward current.

The base contacts on the full transistor structure were not ohmic. They exhibited a very large turn on voltage before any appreciable current flow. When measured in Common Base (CB) configuration, the transistor had saturating IV characteristics with $\alpha \sim 1$ (Figure 2.9a). The β extracted from Gummel Plot was however < 1 (Figure 2.9b). However, in the Common Emitter (CE) configuration, only leakage was observed (Figure 2.9c). The lack of CE modulation contradicts the seemingly high gain observed in CB. This discrepancy, which was also observed in the previous work done on III-N HETs, is discussed in detail next.



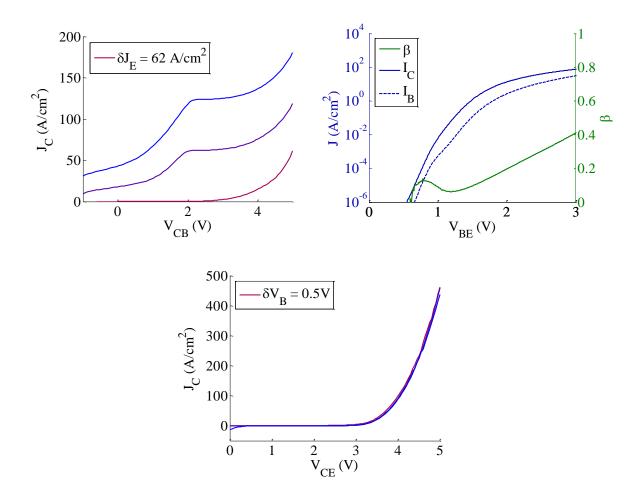


Figure 2.9 (a) Common Base (b) Gummel Plot and (c) Common Emitter characteristics of the AlGaN HET

2.1.3 Issues

The first clue to understanding the discrepancy lies in the base contacts. To understand the cause of non-ohmic base contacts, we look closely at the device structure and fabrication steps. The base charge in our III-N HET design is primarily due to a 2DEG at the emitter-base interface induced by the AlGaN polarization-charge in the emitter layer structure. The bottom part of the base layer is depleted due to the presence of a net negative polarization-charge at

the GaN/AlGaN interface. In order to form base contacts, we etch away the emitter layer completely under the base contact thus resulting in a loss of the 2DEG under the base contact. Since the rest of the base is completely depleted due to the back-side polarization-charge, the net result is a complete lack of charge under the base contacts.

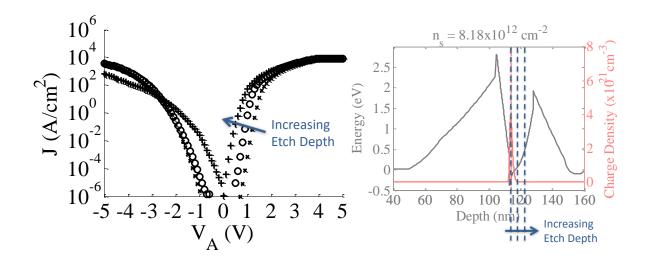


Figure 2.10 (a) I-V characteristics and (b) band-diagram of the B-C diode with increasing etch depth clearly showing barrier lowering

To test this hypothesis, B-C diodes were measured on fabricated HET structures. In the two-step etch process for base contacts, different etch depths were used for the second etch into the GaN base layer. As a result, the B-C diodes have varying GaN thickness on top (Figure 2.10). With increasing etch depth, a decrease in FB turn-on of the B-C diodes was observed. This confirms that the base contact is sitting on top of a completely depleted GaN layer. The potential drop in the depleted layer decreases as etch depth increases thus decreasing the B-C diode turn-on. The lack of ohmic base contacts can thus be explained by absence of charge below the base contact.

Assuming that there is an infinite resistance (no-contact) between the extrinsic and intrinsic base, its effect on device IV characteristics can by analyzed. As mentioned in Chapter 1, the lack of a well-defined fermi-level in the base violates one of the fundamental provisions for the device to act as a transistor.

Common Base

Figure 2.11 shows the bias configuration of a Common-Base measurement where the base is grounded, J_E is increased in steps, and V_{CB} is swept for each J_E . Normally, part of the injected J_E would flow into the base and rest into the collector. However, since the lateral current flow through the base is blocked due to infinite resistance, all the J_E has to flow into the collector resulting in $\alpha \sim 1$. Any base current measured is just a result of forward/reverse bias across the extrinsic base-collector diode and not due to the intrinsic device. In this case, $J_E \sim J_C$ is just a function of the two-terminal bias across the emitter and collector. For a fixed J_E , therefore, the V_E should adjust itself such that the measured V_{CE} is constant.

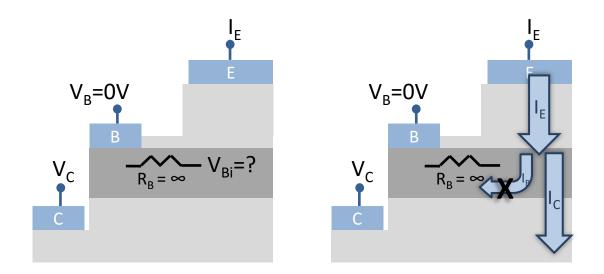


Figure 2.11 Effect of base resistance on Common Base measurement

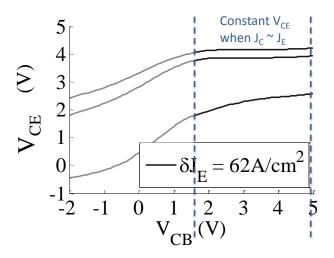


Figure 2.12 Measured VCE during CB measurement

Figure 2.12 shows that the measured IV data indeed confirms this. To summarize, it is possible to observe saturating CB characteristics with $\alpha \sim 1$ even if the intrinsic α of the device is much lower.

Gummel Plot

In a Gummel Plot measurement, the extrinsic base and collector are grounded and a negative potential is applied on the emitter (Figure 2.13). Normally, this would inject electrons from the emitter, part of which go into the base and rest into the collector.

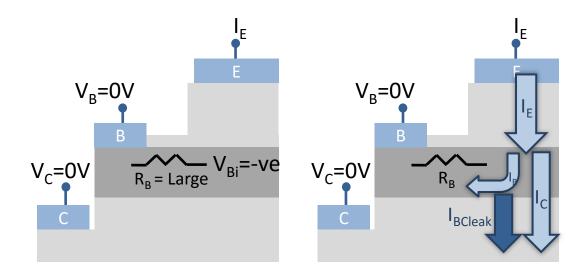


Figure 2.13 Effect of base resistance on Gummel Plot

Since the base and collector are grounded, the effect of reverse leakage between the two should be absent. However, if the lateral R_B is large, there is resistive voltage drop across the base laterally ($V_{Bi} = V_B - I_B R_B$). This is further aggravated if the transistor has low gain and the I_B is large. The presence of a lateral voltage drop in the base implies that even though the extrinsic base and collector terminals are grounded, the intrinsic base-collector junction is actually reverse biased. The measured J_C is thus a sum of the intrinsic hot-electron current and the leakage current from base to the collector. The gain extracted from a device with large R_B using Gummel Plot measurement can therefore be very large and not at all indicative of the intrinsic transistor gain.

Common Emitter

In Common-Emitter configuration, the emitter is grounded and I_B is injected into the base in steps (Figure 2.14).

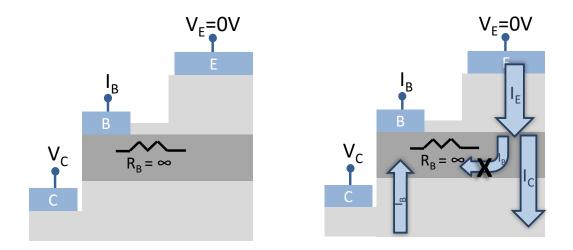


Figure 2.14 Effect of base resistance on Common Emitter measurement

Normally, this injected I_B sets the base fermi-level (or the V_B) to a value such that the current from electron relaxation in the base exactly equals the supplied I_B . In this case, however, since no current can flow from the intrinsic base to the extrinsic base, the extrinsic V_B adjusts itself such that all the I_B comes from the collector. Now the $J_E \sim J_C = f(V_{CE})$ and since the V_{CE} is varying, non-saturating IV characteristics are observed. CE measurement can also be performed by modulating base voltage rather than base current. If base resistance is large, no change in emitter current should be expected as V_B is increased (Figure 2.15a). As V_{CE} is

increased, I_B is just the leakage current of the extrinsic B-C diode. The I_C and I_E are almost identical at large V_{CE} (Figure 2.15b and c). Common-Emitter modulation is therefore the strongest test of transistor action and is the best way to accurately extract current gain and transfer ratio.

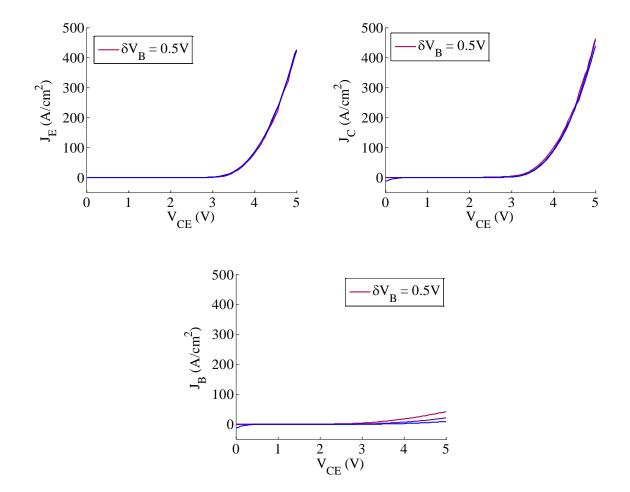


Figure 2.15 CE characteristics of the HET

2.2 AlGaN and InGaN P-D Design

The previous section proved that the absence of transistor action in HETs was a direct result of lack of charge below base contacts. A new design is therefore needed where there is charge below the base contact layer even after etching away the emitter. Design 2, introduced in the beginning of this chapter, offers a potential solution to this problem. This design uses polarization-dipoles (P-Ds) to induce both barriers, AlGaN in the emitter and InGaN in the collector[47]. The E-B barrier structure used here is identical to the one in the last section. The collector barrier is made of an InGaN polarization dipole next to the base and a thick UID GaN layer below the InGaN. The InGaN polarization-dipole provides an electrostatic potential barrier and the UID GaN layer provides a thick barrier to reduce leakage. Since the UID GaN is unstrained to the bulk, it can be grown as thick as needed to reduce leakage currents. Also, the presence of a positive polarization charge at the GaN base/InGaN interface results in a small accumulation of charge as opposed to depletion of charge in Design 1. Thus, by using Design 2, reduction in base resistance, base-collector leakage and strain in the collector can be achieved simultaneously.

2.2.1 Growth and Fabrication

In order to test this HET design, three structures with 4nm, 6nm and 8nm of 45% AlGaN (E1, E2, and E3 respectively) as the E-B P-Ds were grown. The increase in injection barrier with thicker AlGaN should be reflected in the transistor characteristics. The GaN base thickness used here is 15nm. The collector barrier is formed by a 5nm 10% InGaN layer as the P-D

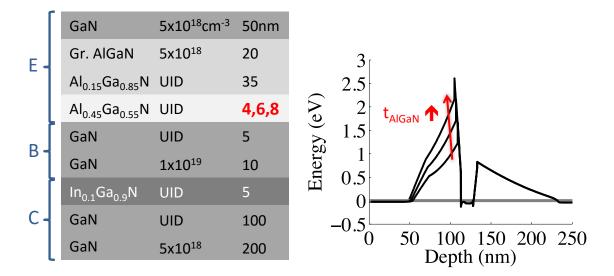


Figure 2.16 (a) Layer structure and (b) band diagram of Ga-Polar HET design 2

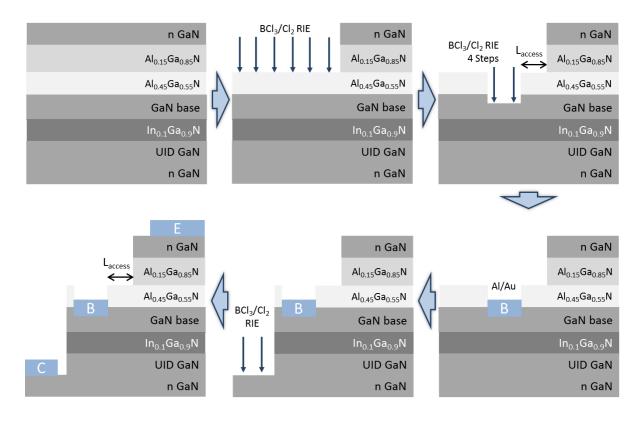


Figure 2.17 Process flow for the AlGaN and InGaN P-D HET

followed by 100nm UID GaN. The detailed layer structure and conduction band diagram are shown in Figure 2.16. Growth was done by MOCVD on Bulk GaN. The fabrication process was identical to the one described for Design 1 (Figure 2.17).

2.2.2 Diode and Transistor Results

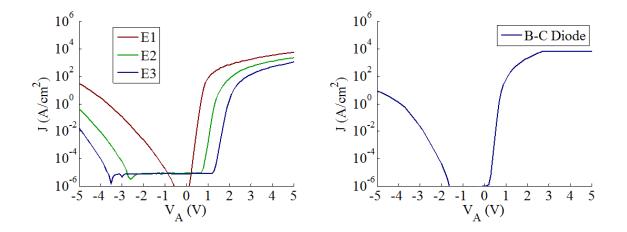


Figure 2.18 (a) E-B and (b) B-C diode IV characteristics measured on the HET

The E-B diode was rectifying and the forward bias turn-on increased with the AlGaN thickness as expected (Figure 2.18a). The ideality factors measured were much larger than unity therefore making it difficult to predict the barrier height from IV measurements. The physical origin of high ideality factors is still under investigation, but we believe that it could be a result of factors like tunneling across the AlGaN layer and barrier height fluctuations. The B-C diode was well rectifying with very low ideality factor of ~ 1.2 (Figure 2.18b). The extracted barrier height (assuming a Richardson constant of $26A/cm^2K^2$) was ~ 0.9eV which matched well with simulated numbers. The reverse leakage was > 2 orders of magnitude smaller than the AlGaN B-C diodes in design 1. This reduction can be attributed mainly to the thicker B-C barrier enabled by the lack of strain.

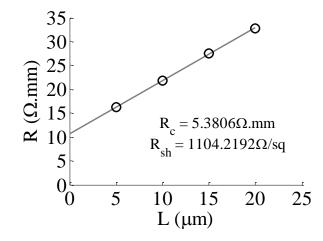
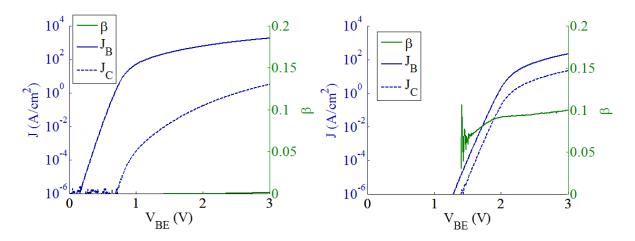


Figure 2.19 TLM measurements of the base layer

The base contacts exhibited ohmic behavior and base contact resistance $R_{Bc} = 5.4\Omega$.mm, and base sheet resistance $R_{Bsh} = 1100\Omega/sq$ were extracted from TLM measurements (Figure 2.19). Gummel Plot measurements yielded a $\beta < 0.01$ for E1 and it increased by an order of magnitude to $\beta \sim 0.1$ for E3 (Figure 2.20). A similar trend was seen in CE characteristics where E1 exhibited no modulation while clear modulation was seen in E3 with a $\beta \sim 0.1$ (Figure 2.21). The current gains extracted from different measurement techniques (Gummel, CB, CE) agreed well with each other for all transistors. The increase in current gain with AlGaN P-D thickness is attributed to an increase in emitter barrier height and consequently hot-electron injection energy. CE modulation, as discussed earlier, is a clear indication of transistor action. This is therefore the first demonstration of transistor action in III-N HETs. The next section discusses different aspects of the CE IV characteristics, their physical origin, and their role in DC performance.







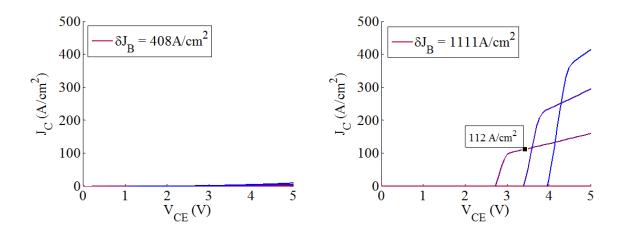


Figure 2.21 CE characteristics of (a) E1 and (b) E3

2.3 Common Emitter Operation

Using the common emitter characteristics of the III-N HET (Figure 2.22), the different regimes of operation and their physical origin can be identified.

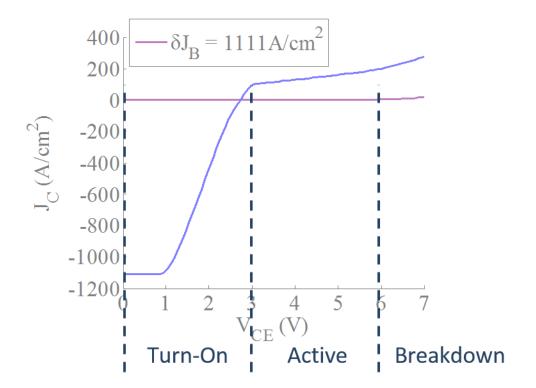


Figure 2.22 Common Emitter operation regimes of a HET

2.3.1 Turn-On

In the turn-on regime, the J_C is negative as shown in Figure 2.22. At zero V_{CE}, for some injected base current, the V_B is positive. In this situation, both the E-B and B-C diodes are forward biased. The B-C diode, having a smaller forward turn-on compared to the E-B diode due to its smaller barrier height, can supply a much larger current at the same forward bias. All the injected J_B therefore comes from the forward biased B-C junction at V_{CE} = 0V resulting in a negative J_C. As V_{CE} is increased, the B-C junction eventually becomes reverse biased.

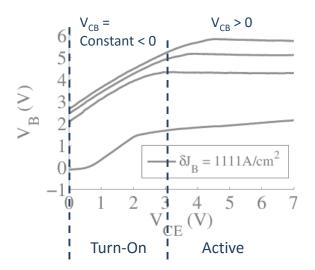


Figure 2.23 Variation of V_B with V_{CE} in CE configuration

The injected J_B now comes from the fraction of injected electrons (J_E) that are scattered in the base. To put this differently, for low V_{CE}, the only way to maintain the J_B boundary condition is for the V_B to be positive and track the V_C such that V_{CB} = Constant < 0. All the J_B here is a result of the forward biased B-C diode. As V_{CE} is increased, the V_B keeps on becoming more and more positive in order to maintain the V_{CB} until the V_{BE} becomes large enough to start injecting electrons from the emitter. A fraction of these injected electrons scatter in the base and supply part of the J_B. Now there is no need to maintain the negative V_{CB} and the V_B stops increasing thus allowing the V_{CB} to become positive and reverse bias the B-C junction. All the injected J_B is now supplied by the fraction of J_E relaxing in the base. The recorded V_B during the measurement indeed confirms this trend (Figure 2.23). The transition of the source of J_B also marks the transition from turn-on regime to the active regime of the transistor. The V_{CE} at which active region begins, matches with the V_{CE} at which V_B becomes constant. A turn-on regime is therefore to be expected in a HET. Ideally, if resistive voltage drops in the base are

negligible, and the ideality factors of both diodes are unity, then $V_{turn-on} \sim (\phi_{EB} - \phi_{BC})$. $V_{turn-on}$ should also be independent of the J_B. However, a large R_B coupled with low α can result in deviations from ideal behavior. The emitter can see only the intrinsic base potential while the collector can see both the intrinsic and extrinsic base potential as a result of the double mesa structure of the device. Due to lateral resistive voltage drops in the base, a larger positive V_B is required on the extrinsic base terminal to achieve an intrinsic V_{BE} which can support the fixed J_B. This results in an extrinsic B-C diode that is more forward biased and thus a larger V_{CE} is needed to transition from turn-on to the active regime. The dependence of V_{turn-on} on J_B can also be explained by presence of a finite R_B. With reduction in these non-idealities, a desirable reduction in turn-on regime is expected.

In order to explicitly show that the origin on negative J_C at low V_{CE} is due to forward biasing of the B-C diode, a thin AlGaN P-D was inserted on the collector side of the UID GaN layer below the base. This makes the B-C barrier more rectangular and should prevent injection of thermal electrons from collector to base. Only hot-electrons from the emitter can cross such a rectangular B-C barrier. The layer structure and band diagram for this device is shown in Figure 2.24. CE measurements of structures with and without the AlGaN P-D in the collector clearly show that the negative current at low V_{CE} vanishes with the insertion of the AlGaN layer (Figure 2.25). The transfer ratio of the device stays almost same. The overall device turnon increases as more V_{CE} is needed before the drift field in the collector sweeps the injected hot-electrons to the collector contact.



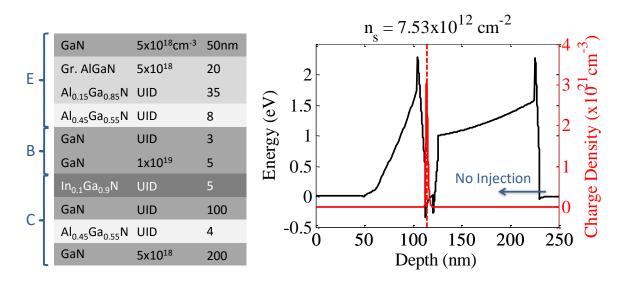


Figure 2.24 (a) Layer structure and (b) Band diagram of HET structure with rectangular collector

barrier

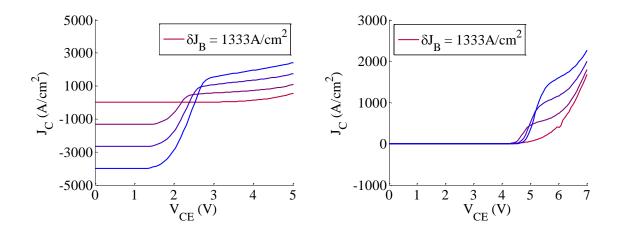


Figure 2.25 CE characteristics (a) without and (b) with the rectangular collector barrier

2.3.2 Active

In the active regime, there are three major parameters that need discussion i.e. gain, output conductance and current density.

Gain

Current gain in a HET can be increased by increasing injection energy, reducing collector barrier, and reducing base thickness. All three methods have some constraints attached to them.

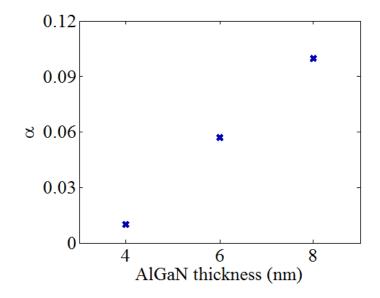


Figure 2.26 Transfer ratio as a function of AlGaN thickness

Injection energy is primarily limited by the materials that can be grown which can form a high enough barrier with GaN to inject hot electrons. Presently, an AlGaN layer is being used as a polarization-dipole (P-D) to inject hot-electrons. Figure 2.26 shows the increase in gain observed by increasing AlGaN thickness. This trend predicts that a very large AlGaN thickness would be required to achieve high gain. Strain limitations prevent the growth of such thick AlGaN layers and thus place a constraint on increasing current gain using this technique.

CHAPTER 2 III-N HET DESIGN AND COMMON EMITTER OPERATION

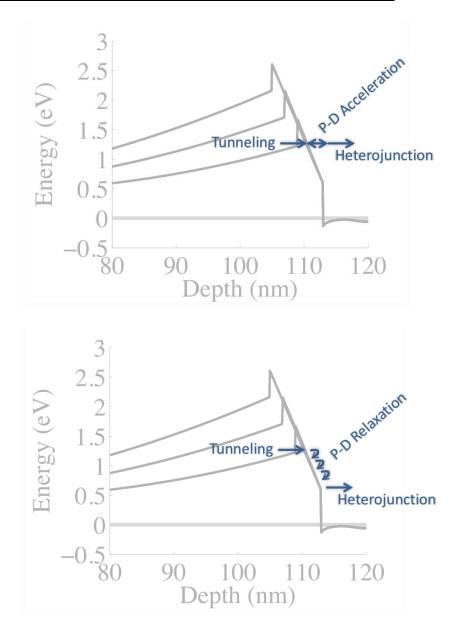


Figure 2.27 Hot-Electron Injection using low % AlGaN P-D (a) Ideal case (b) Real case

During the injection process, electrons first tunnel across the tip of the AlGaN barrier, they then accelerate over the thickness of the polarization-dipole, and finally they gain additional energy from the AlGaN/GaN heterojunction (Figure 2.27a). However, if the P-D thickness is large, electron relaxation in the P-D layer itself could be significant. Instead of

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accelerating over the P-D thickness, electrons could just move along the conduction band due to high scattering rate. In this case, majority of the hot-electron energy comes only from the heterojunction (Figure 2.27b). The P-D field can, therefore, only give a small boost in energy to the electrons. In order to increase the injection energy, materials with a higher P-D field or larger ΔE_c , like AlN or InAlN are needed. The next chapter will discuss this in more detail.

Reducing the collector barrier height can also increase gain but only at the cost of increasing B-C leakage. Since the InGaN P-D in the collector has a finite thickness, electron relaxation could be happening in that layer too. By using higher InGaN composition, the same barrier height could be achieved using a thinner P-D. This would lead to higher gain due to reduction in transit distance.

The presence of a polarization-induced 2DEG allows reduction in GaN base thickness without compromising base charge, and thus enabling higher gain. However, the base contact resistance needs to remain low with base scaling, in order to measure transistor characteristics. Experiments towards this goal will be described in the next chapter.

Output Conductance

The origin of output conductance in an ideal HET ($R_B = 0$) is drastically different from the conventional HBT. In a bipolar transistor, as the V_C is increased (for $V_E = 0$ and a fixed positive V_B), the neutral base thickness shrinks because of an increase in the B-C depletion region. This increases the gradient of electron concentration in the base leading to a higher J_E and J_C . The J_B decreases slightly due to the smaller number of mobile electrons in the base for recombination. Since the increase in depletion region and thus the increase in currents is

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directly related to the base doping, output conductance in an HBT can be easily linked to the Gummel Number (number of mobile holes in the base).

In a HET, since the current flow in the base is ballistic transport rather than diffusion, the boundary conditions on hot-electrons in the base are very different. In an HBT the V_{BE} sets only the excess electron concentration at the emitter side of the neutral base. The J_E is completely dependent on the base thickness (in the drift diffusion limit). In a HET, the V_{BE} specifies both the hot-electron concentration and the hot-electron velocity in the base thus fixing the J_E irrespective of the base thickness. On the collector side, depending on the energy distribution of hot-electrons, part of them get reflected back and part of them go through. Unlike an HBT, there is no boundary condition on the electron density at the collector edge of the base. Any increase in J_C with V_C therefore cannot be linked to J_E . All the increase in J_C comes at the expense of J_B because at larger V_C the transmission probability of hot-electrons across the collector barrier increases. Conceptually, this might sound like B-C leakage, but it's not since these are hot-electrons and are not part of the thermal distribution in the base which cause B-C leakage. This is precisely the property that has been used to perform hot-electron spectroscopy using HETs in the past. With improvements in current gain, output conductance of the HETs can be expected to decrease.

Current Density

Large current density is required for achieving very high-frequency performance. One limitation on current density can be due to series resistance effects in the emitter and base. In this chapter, the device geometry used for fabricating the first III-N HETs was ~ $50x50\mu m^2$

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emitter area. Such large device areas with low aspect ratio can result in emitter crowding effects and reduce current density. The next chapter will use a more scaled device geometry (~ 1x100 μ m²) for HET fabrication. Current density can also be limited by the fact that in the present HET design, electrons have to tunnel across the AlGaN P-D layer for injection. In the absence of resistive effects, the current density will ultimately be limited by the tunneling probability across the emitter P-D layer. This aspect is discussed in more detail in Chapter 4.

2.3.3 Breakdown

Transistor breakdown here is defined as the V_{CE} at which the J_C at zero current injection becomes comparable to the J_C during current injection. The breakdown mechanism is the increase in leakage currents across the B-C barrier due to thermionic emission, tunneling or thermionic field emission. A higher and thicker collector barrier is therefore needed for higher breakdown. Higher collector barrier can adversely affect gain but the collector thickness can easily be increased by just increasing the UID GaN thickness and making sure that the unintentional doping in that layer is low. Threading dislocations in GaN can also play a significant role in increasing leakage currents. Growth on Bulk GaN is therefore preferred although it is much more prohibitive in terms of cost and area. Since the HET doesn't use the full bandgap of GaN, the high breakdown voltages achievable in GaN p-n junctions are not easily realizable here.

2.4 Summary

To summarize, this chapter identified the best way to design III-N HETs taking into consideration various device performance metrics such as gain, leakage and base resistance. An AlGaN and InGaN P-D based design was shown to be the most optimal for these metrics. Common emitter transistor operation ($\beta \sim 0.1$) was demonstrated for the first time in III-N HETs by using this design. Finally, a discussion on the physical origin of various aspects of device characteristics was presented.

3 BASE THICKNESS SCALING FOR CURRENT GAIN

In the last chapter, transistor operation was demonstrated in III-N HETs for the first time. An analysis of the transistor characteristics was presented in order to understand the physical origin of different regimes, and to suggest methods to improve performance. With a baseline data and basic understanding of the III-N HET, this chapter tackles the problem of low current gain by exploring the effect of base scaling on current gain. The problems of base resistance (contact and sheet) and B-C leakage have to be tackled simultaneously with current gain, in order to achieve a useful device. An integrated approach of device design, growth and fabrication is thus needed.

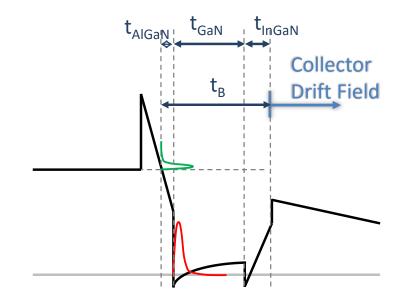


Figure 3.1 Definition of base thickness in a III-N HET. Red curve is the 2DEG electron population in the base and green curve is the hot-electron population

As hypothesized in the last chapter, hot-electrons can scatter not only in the GaN base region but also in the field-accelerated/retarded regions of P-Ds. All these scattering events can lead to energy and momentum relaxation thus affecting gain. The base thickness is thus defined as the total distance where hot-electrons can scatter and become part of the thermal electron distribution in the base (t_B = field accelerated region of the AlGaN P-D + GaN base + InGaN P-D) as shown in Figure 3.1. This chapter presents the results of scaling all three components of the base thickness. The GaN thickness can be reduced by just changing the growth time of that layer. In order to shrink the P-D layers, however, the alloy composition also needs to be increased in order to maintain the same barrier heights. Towards this goal, use of pure AlN and high composition InGaN are also introduced here. A new base contact process is also presented in Section 3.2 which is compatible with base scaling.

3.1 GaN Scaling with AlGaN P-D

This section presents results on GaN base thickness scaling using the same design, growth and process presented in the last chapter. The only difference being that the growth here was done on Sapphire due to unavailability of bulk GaN substrates. The two samples presented here have 15nm and 10nm GaN thickness in the base (B1 and B2 respectively). Figure 3.2 shows the layer structure of the two samples. Smaller lateral device dimensions ($2x150 \mu m^2$) were used for lower base resistance and higher current density.

Ε-	GaN	5x10 ¹⁸ cm ⁻³	50nm
	Gr. AlGaN	5x10 ¹⁸	20
	Al _{0.15} Ga _{0.85} N	UID	35
	Al _{0.45} Ga _{0.55} N	UID	8
В-	GaN	UID	5
	GaN	1x10 ¹⁹	5,10
	In _{0.1} Ga _{0.9} N	UID	5
C-	GaN	UID	100
	GaN	5x10 ¹⁸	200

CHAPTER 3 BASE THICKNESS SCALING FOR CURRENT GAIN

Figure 3.2 Layer Structure of III-N HETs with scaled GaN base using AlGaN and InGaN P-D barriers

3.1.1 Device Performance

The B-C diodes showed a rectification of ~ 2 orders of magnitude between forward and reverse currents (Figure 3.3). The B-C diode rectification is worse than the Bulk GaN HETs presented in the last chapter due to growth on Sapphire. However, it is still enough to observe and analyze transistor IV characteristics.

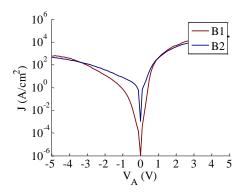


Figure 3.3 Diode IV characteristics of the B-C diode on B1 and B2

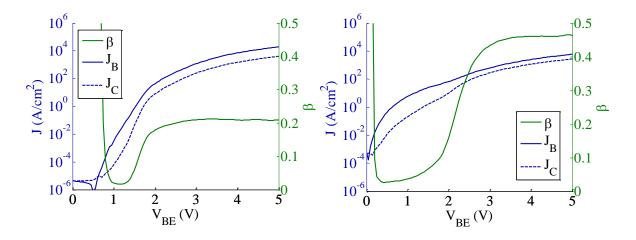


Figure 3.4 Gummel Plot of the III-N HETs (a) B1 and (b) B2

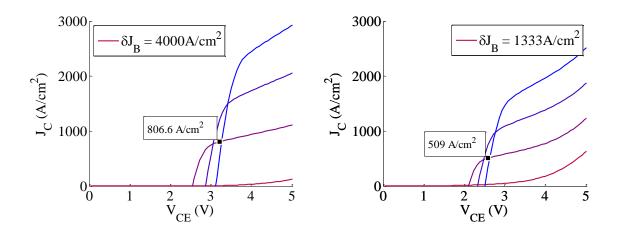


Figure 3.5 CE IV characteristics of the III-N HETs (a) B1 and (b) B2

For sample B1, the β obtained from Gummel Plot (Figure 3.4a) and CE characteristics (Figure 3.5a) was 0.2, which is very similar to the β obtained on Bulk GaN. The slight difference in β between sapphire and Bulk GaN can be attributed to variations in barrier heights due to changes in AlGaN or InGaN compositions. This can happen as a result of differences in calibrations for the two substrates. As the base thickness is reduced to 10nm, an increase in β to 0.45 (Figure 3.4b and Figure 3.5b) was observed, due to reduced scattering in the base. Low R_{Bsh} of 1000 Ω /sq., measured for base thickness of 10nm, is enabled by the use of InGaN polarization-

dipole to induce the collector barrier. However, base contact resistance increased to > 10Ω .mm for B2 from ~ 5Ω .mm for B1. The next section discusses the issues with this base scaling approach in detail and introduces a new method of base contacts compatible with base scaling.

3.2 GaN Scaling with AlN P-D

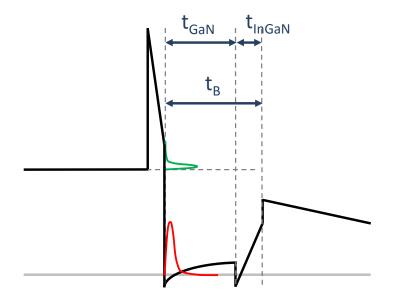


Figure 3.6 Base thickness (t_B) for emitter barrier using AlN P-Ds. Red curve is the 2DEG electron population in the base and green curve is the hot-electron population.

In the last chapter, high vertical leakages in MBE were stated as the reason for moving to MOCVD based growth for HETs. It has been shown that growth of GaN in Ga-rich regime by PAMBE leads to formation of Ga droplets which fill up threading dislocations and thus form leakage paths[60]. A recent paper by Ahmadi et al.[61] shows similar vertical leakages in Schottky diodes grown by PAMBE, MOCVD and Ammonia. Since PAMBE can also be used to grow pure AlN layers, it is now the preferred growth technique for III-N HETs.

The base contact process used in the previous section involved etching through the entire emitter and partially into the GaN part of the base using a timed etch. While this worked out to a reasonable degree for $t_B > 10$ nm, scaling t_B to dimensions < 10nm does not allow for using timed etches and etching into the base. Some sort of etch stop process is needed. In the III-N system, the only selective etch process with very low roughness and very high selectivity is a BCl_3/SF_6 etch that etches GaN and stops on AlGaN[62]. This happens due to the formation of a non-volatile AlF₃ layer on Al containing layers which prevents further etching. Coincidentally, the HET structure uses an AlGaN P-D layer on top of the GaN base which can be used as an etch stop. However, ohmic contacts to the base 2DEG cannot be achieved by this alone. The concept of ohmic contact between two regions with their own fermi-levels requires the presence of a lot of charge in both regions and a high transmission probability between them. If base contacts are deposited on top of the AlGaN P-D layer after a selective etch, the condition of having charge on both sides (metal electrons on one and base 2DEG on the other side) is satisfied. However, since \sim 6-8nm AlGaN is needed to achieve the required injection barrier, the tunneling probability is low across that layer. Thus, the second condition for ohmic contacts is not satisfied. If the AlGaN layer is partially etched to increase tunneling probability, the 2DEG charge decreases. This tradeoff has previously been observed in Ga-Polar HEMTs[63]. Tunneling probability is proportional to exponential of square root of barrier height as opposed to exponential of barrier thickness. Switching to an AlN layer as opposed to 50% AlGaN therefore solves multiple problems at once (Figure 3.7). The same injection barrier heights can be achieved using much thinner layers (1-2nm). This allows the use of selective

etch to put base contacts extremely close to base 2DEG. The tunneling probability is expected to be higher than thick 50% AlGaN. The 2DEG remains unharmed by the selective etch

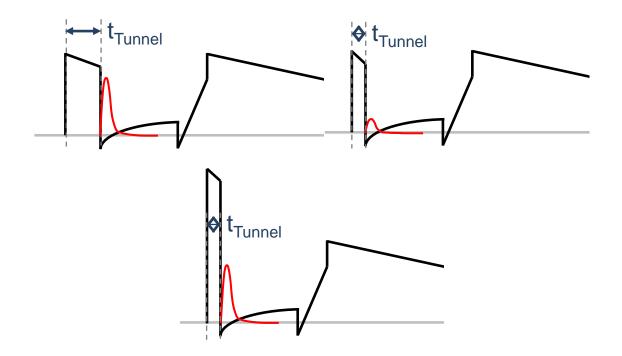


Figure 3.7 Schematic band-diagram for tunnel contacts to the base 2DEG using (a) thick AlGaN (b) thin AlGaN and (c) thin AlN

process[64][65]. Also, using AlN, the field accelerated region of the P-D can be eliminated completely as discussed earlier.

3.2.1 Fabrication

The process steps are illustrated in Figure 3.8. A non-selective BCl_3/Cl_2 low power RIE is used to etch ~70% of the emitter material. This forms the access region of the device. The rest of the emitter is etched using a BCl_3/SF_6 selective etch in the base contact region to stop on the AlN layer. This is followed by a 10 minute 400°C anneal in N₂ to decompose the AlF₃

layer[66]. The base contacts were deposited after this anneal. Emitter and collector contacts can be deposited before or after this anneal step. All devices presented from now on use a pure

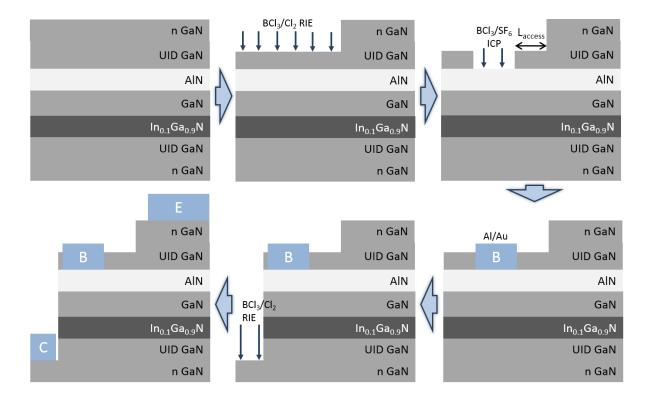


Figure 3.8 Process Flow for tunnel contacts to a HET structure

AlN layer with this tunnel contact process technique. More details about the etch parameters are presented in Appendix A.

3.2.2 Structure and Growth

Figure 3.9 shows the device structure that was used to determine the effect of GaN scaling with an AlN P-D emitter. A 5nm GaN layer above the AlN was modulation doped to increase base charge and reduce R_B . The 15% AlGaN in the emitter used previously for higher base charge

was removed in order to facilitate the etch stop process. MBE was used as the growth technique as it has been shown to be the best technique for growth of pure AlN layers[59]. Two structures of different GaN thicknesses of 8nm and 2nm (B1 and B2 respectively) were grown in a Varian Gen-II MBE system, equipped with conventional thermal effusion cells for

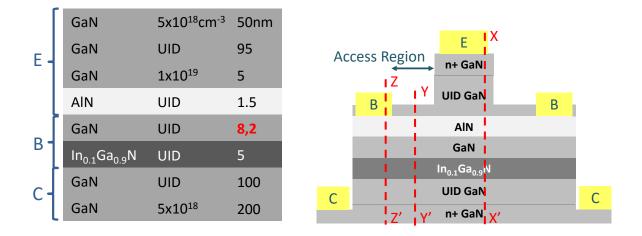


Figure 3.9 (a) As grown and (b) processed structure of MBE grown III-N HETs with AlN emitter

Al, Ga, and In sources and a Veeco Unibulb radio frequency (RF) plasma N source. The N source consisted of ultra-high-purity (99.9995%) N₂ gas flowing at 0.7 sccm through the RF-plasma source with 250 W RF power, which corresponded to a growth rate of 4.4 nm/min for metal-rich GaN layers. Substrate temperature was measured by an optical pyrometer calibrated using the melting point of Al. HET structures were grown on GaN templates on Sapphire with a threading dislocation density of $\sim 5 \times 10^8$ cm⁻². After growing the collector at 700°C, the growth was interrupted to decrease the temperature to 570°C for growth of InGaN. A LT GaN layer (4 and 1nm for B1 and B2 respectively) was then grown at the same temperature to protect the InGaN layer from decomposition. The necessity of having this layer sets a boundary

condition on the minimum possible base thickness achievable using the growth technique described here. The temperature was then raised to grow the rest of the base and the emitter.

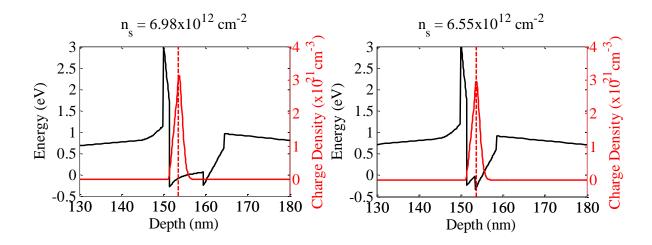


Figure 3.10 Band-diagram of (b) B1 and (c) B2 along XX' showing the base 2DEG charge in red. The dotted red line represents the 2DEG centroid.

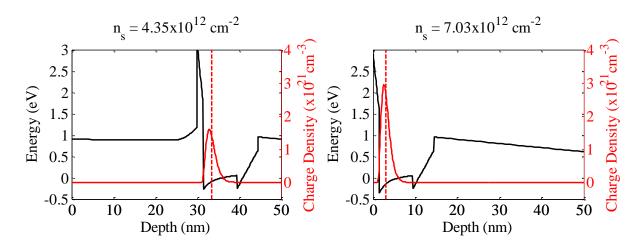


Figure 3.11 Band-diagram of the III-N HETs in regions (a) YY' and (b) ZZ'

3.2.3 Device Performance

The E-B and B-C diodes show rectifying behavior for both samples (Figure 3.12). The B-C diode leakage for B1 was almost same as the MOCVD grown B-C shown in the last section. This proves the viability of MBE as a growth technique for III-N HETs. The barrier heights

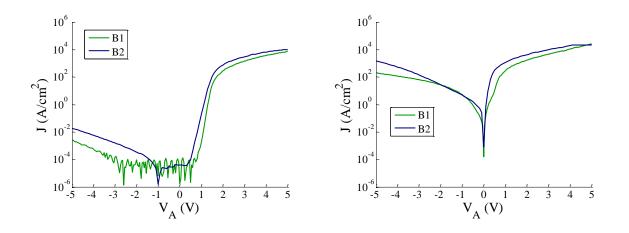


Figure 3.12 (a) E-B and (b) B-C diode I-V characteristics for samples B1 and B2

Sample	R _{Bc,noAnneal} (Ω.mm)	R _{Bc,Anneal} (Ω.mm)	$R_{Bsh}\left(\Omega/sq ight)$
B1	6.3	0.49	1787
B2	3.75	1.44	3550

Table 3.1 Base resistance

from band diagram simulations are ~1.2eV and ~0.9eV for E-B and B-C barriers respectively. The base contact resistance (Table 3.1) shows a drastic decrease after the 400°C anneal. Even though the anneal is theoretically supposed to only remove the AlF₃ layer formed after the selective etch, part of the AlN might also be getting oxidized and removed in the subsequent acid dip. The exact reason for the reduction in contact resistance is therefore not fully clear. It was also observed that the same anneal conditions (if performed after emitter and collector

contact deposition) helped in improving contact resistances of the emitter and collector too. The measured base sheet resistance for sample B2 was much higher than B1. Since the modulation doping for both samples is the same and simulated 2DEG charge is also almost

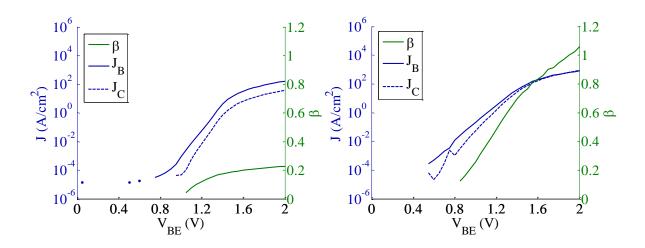


Figure 3.13 Gummel plot of samples (a) B1 and (b) B2

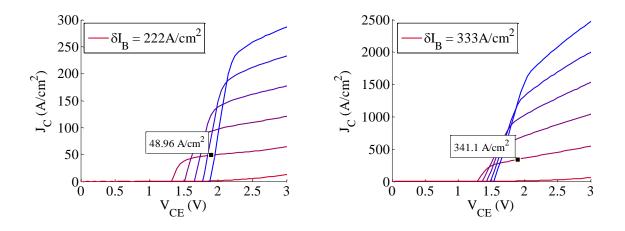


Figure 3.14 CE I-V characteristics of (a) B1 and (b) B2

identical, the increase in sheet resistance can be attributed to alloy scattering due to increased overlap of the 2DEG with the InGaN layer in B2 (Figure 3.10).

The current gain extracted from Gummel Plot was ~0.2 and ~1 for B1 and B2 respectively (Figure 3.13). A more accurate method of verifying transistor action and extracting β is base current controlled CE characteristics[47], where β is defined as the ratio of J_C and J_B. In order to minimize spurious contributions to gain from leakage currents, a V_{CE} after the knee voltage but before onset of leakage is chosen for gain extraction. The β extracted from CE characteristics of the HETs presented here is 0.22 (=48.96/222) for B1 and 1.02 (=341.1/333) for B2 (Figure 3.14)[67]. Common base measurements (not shown here) also yielded the same β for both samples. This agreement between different measurement techniques shows that the extracted $\beta > 1$ is accurate. Since the only difference between the two samples is the GaN thickness, the increase in gain can be directly attributed to the decrease in t_B from 13nm to 7nm. Further scaling of the base thickness might be required to achieve higher gain. This is the first demonstration of CE current gain in III-N HETs.

3.3 InGaN Thickness Scaling

In the last section, current gain in III-N HETs was demonstrated using a novel base contact technique which enables base scaling. However, growth limitations prevented further scaling of the GaN base layer because a thin GaN cap is required in order to protect InGaN from the high growth temperature of AlN. This section focuses on scaling the InGaN P-D thickness (and hence t_B) using growth of higher composition InGaN layers.

3.3.1 Structure and Growth

Figure 3.15 shows the device structure and band diagram. In order to shrink the InGaN thickness while maintaining a similar B-C barrier height, the InGaN composition needs to be increased. Therefore, a 2nm 20% InGaN layer is used instead of a 5nm 10% InGaN layer in the last section. This results in a reduction in t_B from 7nm to 4nm. The two structures have almost the same B-C barrier height.

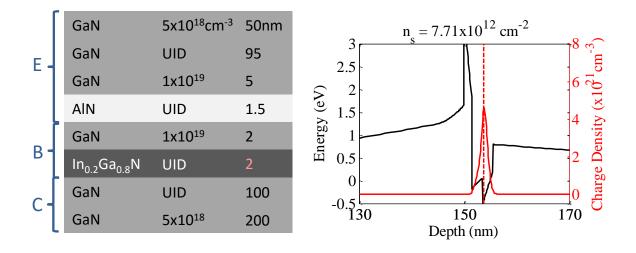


Figure 3.15 (a) Layer Structure and (b) Band-Diagram of III-N HET with 20% InGaN collector

The growth methodology was also the same as last section. Again, since the AlN layer is grown at higher temperature than InGaN, there is a need for a LT GaN cap on top of the InGaN layer to preserve the quality of the InGaN. The GaN base layer in this structure is n-type doped. Without base doping, ohmic contacts to the base layer could not be obtained. With base doping too, the contacts did not become strictly ohmic (a slight non-linearity was seen) but were very close. The exact cause behind this effect cannot be isolated at present. The next part discusses a few possible reasons that could lead to non-ohmic base contacts.

3.3.2 Device Performance

The emitter diode exhibited very well rectifying behavior (Figure 3.16). The B-C diode, however, had high leakage even though the GaN cap is the same as last section. One reason behind this could be the fact that 20% InGaN is grown at even lower temperature than 10% InGaN. The GaN cap thickness required before AlN growth could therefore be larger for 20%

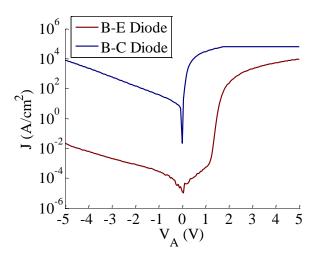


Figure 3.16 Diode I-V characteristics of the III-N HET

InGaN. This was also corroborated by the fact that when the GaN cap was decreased to 1nm instead of 2nm (in a separate experiment), the B-C diodes became almost shorts. Another reason for high leakage could be barrier lowering due to the high confinement in the base. As the base quantum well become narrower, the ground state energy increases along with the Fermi-level in the base, thus reducing the effective collector barrier height.

The base contacts were not perfectly ohmic thus preventing the extraction of base resistance. Since the base contacts depend on tunneling, it is preferable to have a high tunneling probability from the base 2DEG to the base contact layer. With a 2nm GaN cap, as the InGaN

composition is increased, the 2DEG shifts towards InGaN due to the lower potential in the InGaN layer. This could be one of the reasons responsible for the lack of ohmic base contacts in this sample.

The lack of perfectly ohmic base contacts and high B-C leakage, though detrimental for device performance, do not prevent the extraction of gain from CE I-V (see discussion in

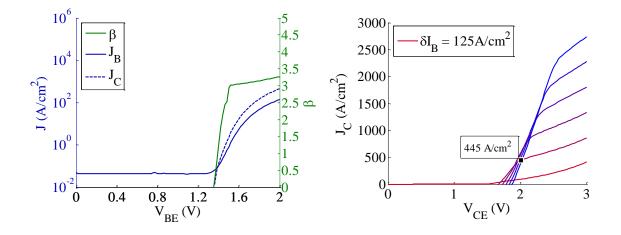


Figure 3.17 (a) Gummel Plot and (b) CE I-V characteristics of the III-N HET

Chapter 2). The gain extracted from Gummel Plot is ~ 3.3 (Figure 3.17a). The CE I-V characteristics of the device also exhibit a gain of ~ 3.5 near the knee voltage (Figure 3.17b). The fact that at a fixed V_{CE} the collector current increases when base current is injected shows that the device behaves as a transistor.

The use of P-D design with AlN as a tunnel contact enabled such aggressive scaling of the base and resulting in gain ~3.5. This is the highest DC current gain demonstrated in III-N HETs at present. Still, the lack of good base contacts and the high B-C leakage call for more improvements in design, growth and processing. The next chapter discusses extraction of mean free path in order to predict the base thickness required to achieve gain > 10.

3.4 Summary

To summarize, this chapter explored the effect of base thickness on current gain in III-N HETs. The base thickness was reduced in three steps. First, the GaN thickness was reduced from 15nm to 10nm using an AlGaN P-D emitter. Maximum gain achieved was ~ 0.45. After this, it was determined that a change in design and process was required for further scaling. This led to a pure AlN P-D emitter which acted as an etch stop for base contacts. The GaN thickness was further scaled all the way to 2nm using this technique. Maximum gain achieved was ~ 1. Finally, the InGaN thickness was decreased from 5nm to 2nm by increasing its composition from 10% to 20%. With a total base thickness of 4nm now, the gain achieved was ~ 3.5. This is the highest DC current gain reported in III-N HETs and is enabled by the novel combination of design, growth and processing techniques introduced here.

4 HOT ELECTRON TRANSPORT IN III-

NITRIDES

A deep understanding of hot-electron transport is critical for future development of hotelectron devices. In devices, traditionally, we are used to looking at currents as a function of electric fields and electron densities and electron densities as a function of energy. This is referred to as the drift diffusion model of transport where,

$$\boldsymbol{J_n} = qn\mu_n \mathbf{E} + qD_n \boldsymbol{\nabla}_r n$$
$$\frac{\partial n}{\partial t} = \frac{1}{q} \boldsymbol{\nabla}_r \cdot \boldsymbol{J_n} - (G - R)$$

The drift diffusion model however presents a very simplistic picture of electron transport in materials which is not valid for extreme non-equilibrium. Drift diffusion model assumes that even in non-equilibrium, the electron density follows a Fermi-Dirac like distribution with a quasi-fermi level which is different from the equilibrium fermi level. At low fields, low electron concentrations and long timescales, this assumption is valid as electrons are still in local equilibrium with the lattice. If any of these assumptions break down, the drift diffusion model is no longer valid.

The Boltzmann Transport Equation (BTE) provides a more general formalism of classical transport. The drift diffusion model is only a special case of BTE. The BTE describes the time and space evolution of a distribution function (f) under different kinds of non-equilibrium. It was originally developed for ideal classical gases but is applicable to electrons

CHAPTER 4 HOT ELECTRON TRANSPORT IN III-NITRIDES

in solids too. The BTE can be used to describe electron transport in cases where the local equilibrium assumption is no longer valid and the electron distribution does not follow the Fermi-Dirac shape.

$$\frac{\partial f}{\partial t} + \frac{\mathbf{p}}{m} \cdot \nabla_{\mathbf{r}} f + \mathbf{E} \cdot \frac{\partial f}{\partial \mathbf{p}} = \left(\frac{\partial f}{\partial t}\right)_{coll}$$

While BTE is closer to describing hot-electron transport, it still does not capture some key components of the physics. Any quantum mechanical behavior of electrons cannot be included into BTE. For example, quantum mechanical reflection of electrons, anisotropic and energy dependent effective mass of electrons, multiple scattering mechanisms each having their own anisotropy and energy dependence and more. Also, for most real cases BTE is very difficult to solve analytically. Most electron transport today is therefore described using Monte Carlo (MC) simulations, an algorithm for modelling random processes. MC simulation uses generation of random numbers following some probability distribution function to describe hot-electron physics. With good knowledge of material properties like effective mass and scattering rates, MC simulation is the most powerful and accurate tool to understand hotelectron physics. The previous chapters mostly focused on empirical results as the guideline for improving device performance. This chapter has multiple goals, first, to qualitatively visualize the behavior of hot-electrons in solids using 3D momentum-space (k-space) plots, second, to present experimental data on extraction of mean free path using III-N HETs, and finally, to use this understanding and present a comprehensive picture of the design space of III-N HETs.

4.1 Qualitative description of hot electrons

4.1.1 Monte Carlo simulations

MC simulations are typically used to model the ensemble behavior of entities whose properties change as a result of random events. This involves generation of random numbers that follow some given probability distribution and updating the properties of the entities whenever such random events happen. Once this is done, the ensemble properties can be extracted by averaging over a large number of entities. In this case, the entities are electrons, the random events are scattering events, and the properties are position and momentum.

Full band MC simulators exist for various semiconductors which can be used to exactly model the behavior of real devices. However, to get insight into the process of scattering, it is more useful to work with a highly idealized situation. In order to accomplish this, a simple MC simulator was written in MATLAB closely following the methodology explained by Lundstrom[68]. The algorithm and the approximations used are described next.

Algorithm

Each electron in the system is assigned five properties. The electron momentum in three directions (k_x , k_y , and k_z), total electron energy, and electron position along +z direction. All of these properties are updated as the electrons pass through various stages of the simulator.

The MC simulator developed here consists of four basic parts. (1) Initialization, where, given the E_c - E_f , electrons are randomly assigned states such that they obey Fermi-Dirac

CHAPTER 4 HOT ELECTRON TRANSPORT IN III-NITRIDES

statistics. The number of electrons used in the simulator can be chosen here. (2) An electron filter which acts as the injector. Given a transmission probability vs energy for the injector, the properties of the initialized electrons are updated according to the laws of QM as they are injected into the base. (3) A MC simulator where properties of each electron are updated according to randomly generated scattering events with a mean scattering time. (4) An electron filter which acts as the collector. All the electrons that have travelled a certain specified distance (base thickness) are passed through this filter in order to calculate transfer ratio of the transistor.

Approximations

A mentioned before, electrons are assumed to behave as QM particles for the injection and collection part of the simulation. However, for the scattering part, electrons are assumed to be localized wave packets with well-defined position and momentum expectation values. QM spreading of these wave packets with time is assumed to be negligible. Bands are assumed to be parabolic and isotropic. Only one scattering mechanisms with anisotropic momentum relaxation and a finite energy relaxation is implemented for now. This is aimed to mimic some properties of polar optical phonon scattering in III-Nitrides. However, it is meant to be just a qualitative visual aid and does not capture fine details of the electron-phonon scattering process. With all these approximations, the MC simulation program becomes quite simple to write and the results are easy to interpret.

4.1.2 k-space maps of Hot-Electrons

Initialization

Electrons are uniformly distributed in the k-space such that their density obeys the Fermi-Dirac distribution. Only electrons with positive k_z are populated as the device is assumed to be along the z direction. Figure 4.1 shows the distribution of electrons in the k-space. Figure 4.2 shows the energy in +z direction and the total electron energy. Since the parallel momentum is conserved during injection and collection, it is important to track the momentum/energy in all directions separately.

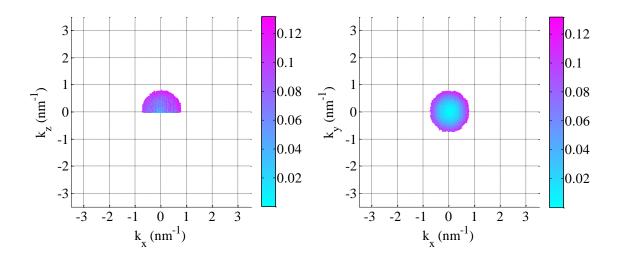


Figure 4.1 k-Space maps of electrons after Initialization

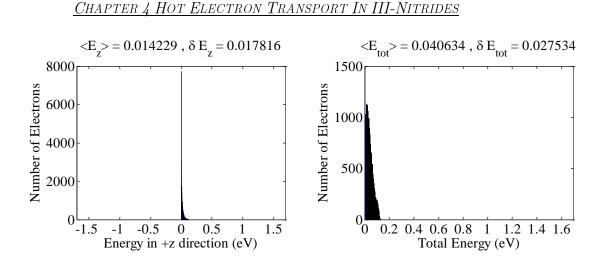


Figure 4.2 Distribution of electrons vs (a) Energy in +z direction and (b) Total Energy

Injection

The injection mechanism is assumed to be across a step-down potential of 1.5eV. The k_x and k_y (parallel momenta) are conserved as electrons cross this heterojunction. The transmission probability as a function of k_z is given by, $T = \frac{2\sqrt{k_{z1}k_{z2}}}{k_{z1}+k_{z2}}$.

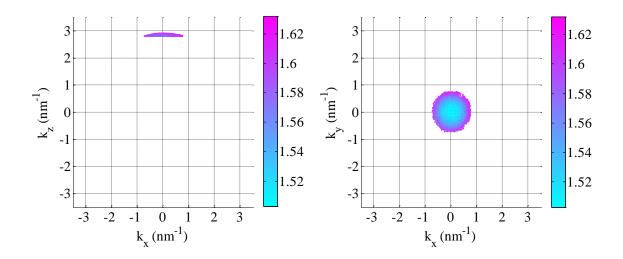
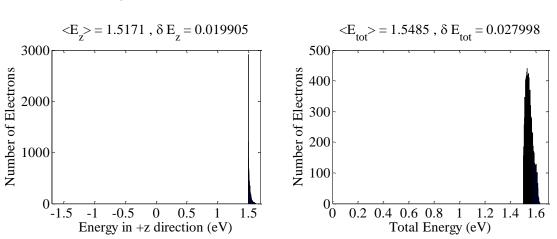


Figure 4.3 k-Space maps of electrons after Injection



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Figure 4.4 Distribution of electrons vs (a) Energy in +z direction and (b) Total Energy

The k-space and energy plots clearly show that a step down potential only introduces shifts in k_z and E_z . All the change in E_{tot} comes due to change in E_z .

Base Transit

The time of free flight for each electron is generated according to a Poisson distribution with mean scattering time of 10fs. After the time of free flight, the electron position is updated using the group velocity (m^{*} = 0.2). The electron k are updated according to the scattering mechanism. In the present case, the scattering process is assumed to reduce total electron energy by 0.2eV and randomly change the electron direction using a normal distribution with an angular spread of $\pi/4$. This results in anisotropic momentum relaxation and finite energy relaxation. Polar LO phonon scattering in GaN behaves in a similar way except the energy relaxation is 92meV and the anisotropic momentum relaxation follows a very complex function.

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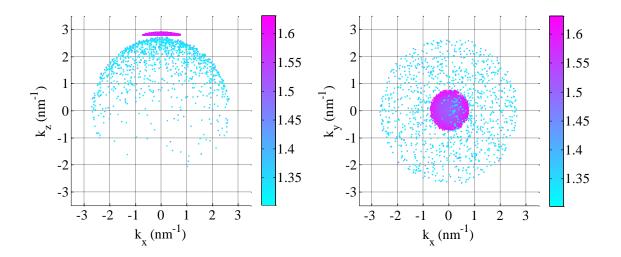


Figure 4.5 k-Space maps after ~ 1fs transit time

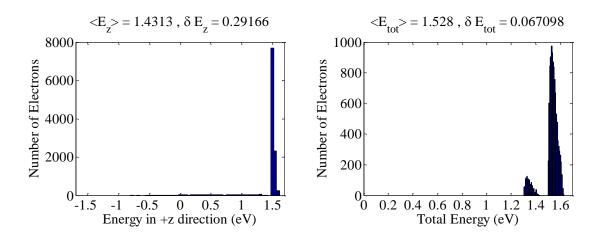


Figure 4.6 Distribution of electrons vs (a) Energy in +z direction and (b) Total Energy after ~ 1fs transit time

The plots in Figure 4.5 and Figure 4.6 show the electrons after a time step of ~ 1fs and the plots in Figure 4.7 and Figure 4.8 show the electron distribution after ~ 10fs.

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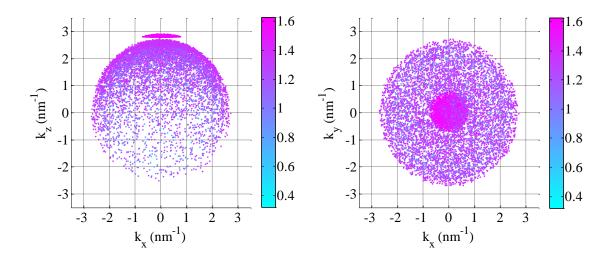


Figure 4.7 k-Space maps after ~ 10fs transit time

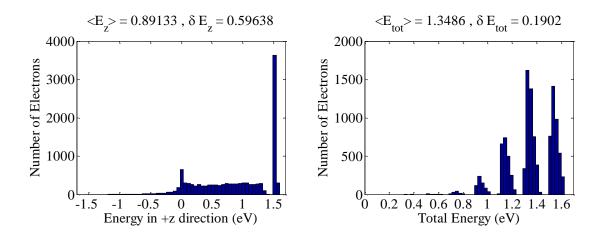


Figure 4.8 Distribution of electrons vs (a) Energy in +z direction and (b) Total Energy after ~ 10fs transit time

The k-space plots show that in a HET, electrons start out being highly directional and with time, get more uniformly distributed across the k-space and occupy smaller and smaller shells in the k-space. This is also clearly visible in the energy distributions where the E_z and E_{tot} distributions shift towards zero with time. The E_{tot} distribution shifts in discrete steps as the scattering process here is designed to lose 0.2eV for every scattering event.

Collection

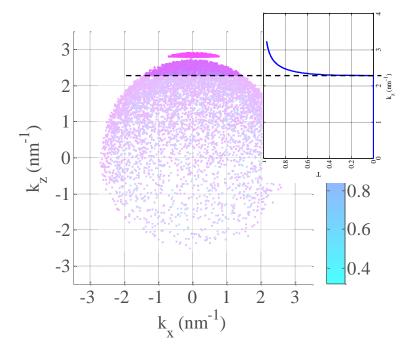


Figure 4.9 Collector transmission probability vs kz superimposed on the electron distribution

In order to calculate transfer ratio, the data for all electrons that have travelled a certain distance, equal to base thickness, is put together and passed through the collector filter. Since the collector filter is also a k_z filter, momentum relaxation plays a big role in determining the transistor α . Figure 4.9 shows the transmission probability as a function of k_z superimposed on the k-space distribution of electrons.

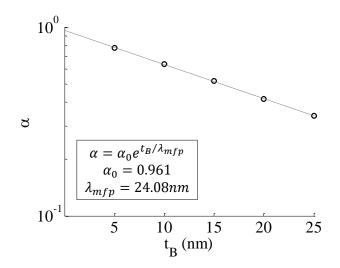


Figure 4.10 MFP using a 1.5eV injection with a 1eV collector barrier

This exercise can be repeated for multiple base thicknesses. When the resulting transfer ratio vs base thickness profile is plotted, it turns out to follow an equation of the form, $\alpha = \alpha_0 e^{-\frac{t_B}{\lambda_{mfp}}}$ (Figure 4.10). The slope gives a quantity called ballistic mean free path and the intercept gives the transfer ratio at zero base thickness. This form also makes intuitive sense as scattering processes follow the Poisson distribution. Just like nuclear decay has a half-life, hot-electron scattering has a scattering time or mean free path.

The λ_{mfp} is a measure of how fast the transfer ratio decays with base thickness. It depends on multiple phenomena like different scattering mechanisms, electron velocity, and difference between the two barriers. The α_0 depends mainly on the difference between emitter and collector barriers. These MC simulations are not meant to be taken for their quantitative prediction power. The main purpose of doing these simulations is (a) to develop an intuitive visual understanding of electron scattering in solids and, (b) to motivate the use of an exponential equation for fitting device results.

4.2 Scattering and Mean Free Path

4.2.1 Definition and Mechanisms

Mean free path can be defined in several ways. The three important definitions to consider are given as follows,

- Empirical Definition: The empirical mean free path is defined as the slope (exponential) measured from a plot of α vs t_B extracted from hot-electron transistors.
- **Strong Theoretical Definition:** Here, mean free path is extracted using full band Monte Carlo simulations of hot-electron transistors using known material parameters.
- Weak Theoretical Definition: This mean free path is obtained by just multiplying the mean momentum relaxation time and the electron group velocity at the given injection energy.

The focus of this section is on extracting the empirical mean free path using III-N HETs and comparing the extracted quantity to the weak theoretical definition of mean free path. Before proceeding to MFP measurements on HETs, a review of different hot-electron scattering mechanisms and rates is presented.

Optical Phonon Scattering (Polar interaction)

The polar interaction of optical phonons (POP) is theoretically anisotropic where momentum relaxation rate could be much slower than scattering rate. Theoretical scattering rate for POP scattering stays relatively constant with energy while momentum relaxation rate drops with

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energy because the initial momentum is higher at higher energy. Since momentum relaxation is what is ultimately important for HETs, polar interaction favors long mean free paths. The longitudinal polar optical phonon, theoretically, has the fastest scattering rates of all mechanisms in the III-N system. The electron-phonon scattering threshold for GaN is 92meV[69]. The theoretically calculated LO phonon emission rate in GaN is 10fs[69], [70]. However, very few experimental measurements exist and the extracted scattering rate using femtosecond pump-probe techniques are larger than the theoretical values by an order of magnitude (200 - 300fs)[71], [72]. The explanation for this discrepancy has been phonon reabsorption due to the presence of hot-phonons when the carrier density is large. Also, many of these measurements extract energy relaxation and not momentum relaxation which is the more relevant parameter for HETs. Energy relaxation using LO phonons is slow as the energy emitted through each phonon is just 92meV.

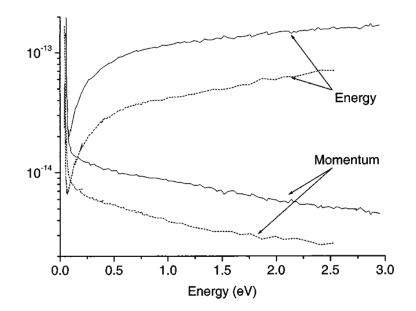
Optical Phonon Scattering (Deformation potential interaction)

Deformation potential interaction (ODP) is isotropic i.e. momentum relaxation rate is same as scattering rate and the scattering rate increases with energy. While at low energies ODP scattering rate is much smaller than POP scattering rate, at higher energies (> 1.5eV) it can become higher than POP momentum relaxation rate[73].

Intervalley Phonon Scattering

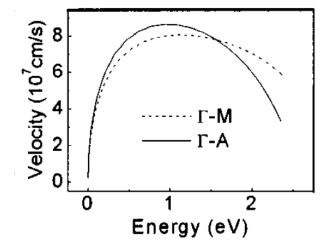
Intervalley scattering also happens as a result of POP scattering. Once the satellite valleys are energetically available, electrons scatter into them and thus increase momentum relaxation

rate. The Γ – L separation in GaN has been theoretically calculated to be > 2eV[74], [75]. Again, experimental measurements for these are few in number and do not agree well with theoretical predictions. Experimentally measured intervalley separation in GaN is ~ 1.2eV[72], [76]. Intervalley scattering rate in GaN has been measured to be ~ 100fs[72].



 $Figure \ 4.11 \ Average \ energy \ and \ momentum \ relaxation \ rates \ in \ GaN \ (solid) \ and \ AlN \ (dotted) \ as \ a$

function of electron energy[73]



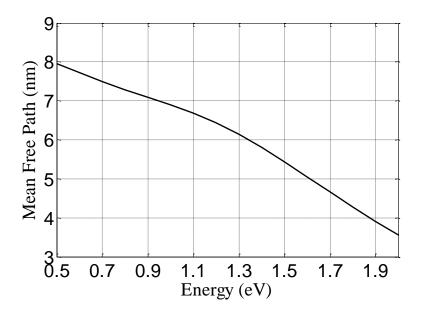


Figure 4.12 Group velocity of electrons as a function of electron energy[77]

Figure 4.13 Mean free path in GaN using the weak theoretical definition

To sum this all up, at low energies where intravalley POP scattering dominates, momentum relaxation rates in GaN can be ~ 10fs or higher. As the electron energy increases, momentum relaxation rate in GaN decreases from 8fs at 1eV to 5.9fs at 2eV (Figure 4.11). Figure 4.12 shows the electron group velocity as a function of energy. Using the weak theoretical definition, the hot-electron mean free path can be estimated by just multiplying these two quantities together (Figure 4.13). The trend of decreasing mean free path with higher injection energy has many implications for the III-N HET. Since the collector barrier has to block leakage currents and be smaller than injection energy for high gain, it sets a lower bound on injection energy. The upper bound is set by decrease in mean free path and hence gain at very high energies.

4.2.2 λ_{MFP} in GaN using HETs

As seen in the last section, the transfer ratio of a HET is essentially a measure of the momentum relaxation that happens in the base. It was also shown that the transfer ratio vs base thickness

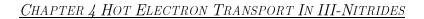
can be fit to an equation of the form, $\alpha = \alpha_0 e^{-\frac{t_B}{\lambda_{mfp}}}$. Here, III-N HETs are used to extract transfer ratio as a function of base thickness and fit it to this equation. Since the base thickness consists of GaN and the PDs, it is very difficult to change all of them simultaneously. Therefore, the only variable that is changed here is the GaN thickness in the base. The λ_{mfp} extracted is thus the MFP in GaN and α_0 is the α at zero GaN thickness.

MOCVD AlGaN P-D Emitter

Е-	GaN	5x10 ¹⁸ cm ⁻³	50nm
	Gr. AlGaN	5x10 ¹⁸	20
	Al _{0.15} Ga _{0.85} N	UID	35
	Al _{0.45} Ga _{0.55} N	UID	8
В- С-	GaN	UID	5
	GaN	1x10 ¹⁹	3,7,11
	In _{0.1} Ga _{0.9} N	UID	5
	GaN	UID	100
	GaN	5x10 ¹⁸	200

Figure 4.14 Layer structure used for the MOCVD mean free path series

The HET design used for extracting MFP in MOCVD grown material is the one introduced in Chapter 2. The structure used for the MFP experiment is described in Figure 4.14.



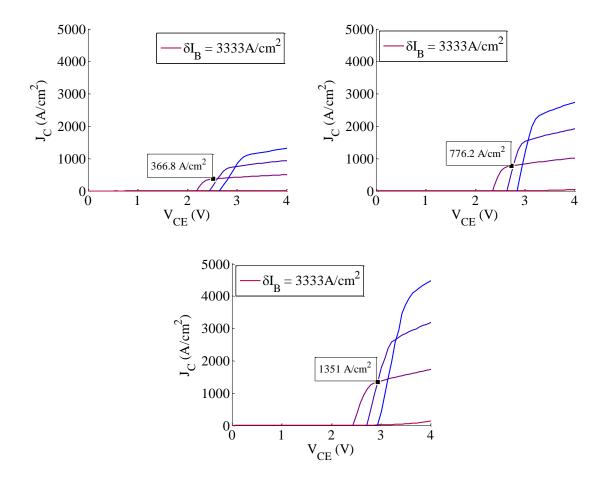


Figure 4.15 CE characteristics showing the currents near knee voltage for the MOCVD samples

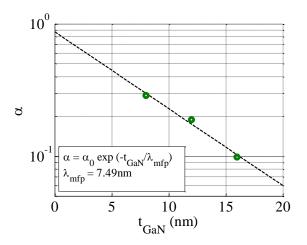


Figure 4.16 MFP on MOCVD material

The α for each sample is extracted from CE characteristics near the knee voltage as shown in Figure 4.15. Figure 4.16 shows the resulting fit. The extracted λ_{mfp} is 7.49nm. Due to electron relaxation in the AlGaN P-D layer, the injection energy here is unclear. It is therefore difficult to make any statements about the momentum relaxation time.

	GaN	5x10 ¹⁸ cm ⁻³	50nm
E -	Gain	SXIO °CIII °	John
	GaN	UID	95
	GaN	1x10 ¹⁹	5
	AIN	UID	1.5
	GaN	UID	2,4,8
B	In _{0.1} Ga _{0.9} N	UID	5
c -	GaN	UID	100
	GaN	5x10 ¹⁸	200

MBE AIN P-D Emitter

Figure 4.17 Layer structure of the MBE HETs for extracting MFP with 1.5nm AlN

The design used here is the one introduced in Chapter 3 (Figure 4.17). The extracted λ_{mfp} for these samples is 6.04nm (Figure 4.18, Figure 4.19).



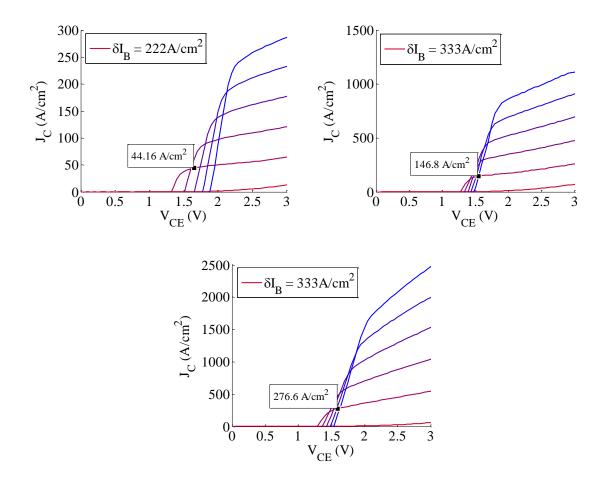


Figure 4.18 CE characteristics showing the currents near knee voltage for the MBE samples

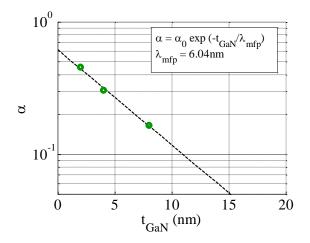


Figure 4.19 MBE MFP with 1.5nm AlN

The major purpose of this section, apart from extracting mean free path, is to guide future device scaling. Figure 4.20 shows the present HET design with three major parameters i.e. t_{AIN} , t_{GaN} , and t_{InGaN} .

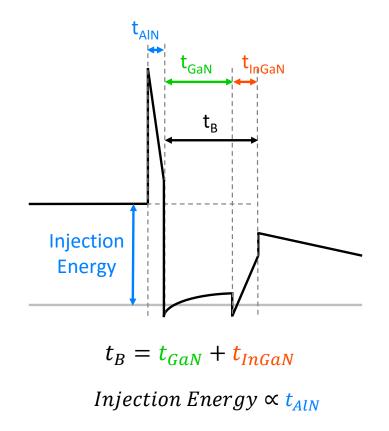


Figure 4.20 Design parameters for the III-N HET

Figure 4.21 shows the effect of all three parameters on the transfer ratio of the device. Scaling t_B clearly has an exponential effect on α and the fit predicts a $\beta \sim 10$ at t_B = 3nm. The exponential scaling also demonstrates a transport regime limited by hot electron scattering. The fact that the α_0 here is > 1 implies that as the device is scaled further, the hot-electrons will be fully ballistic and the device α with stop increasing exponentially with t_B. In this

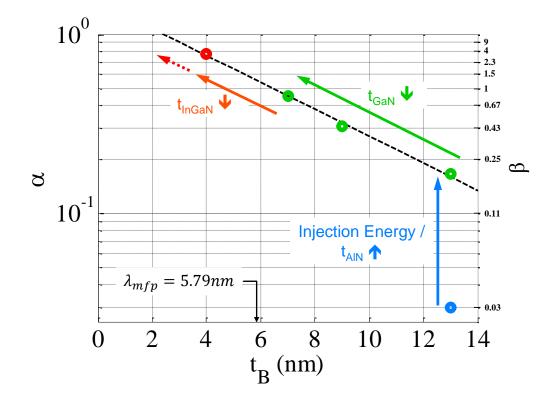


Figure 4.21 Design space of the III-N HET

regime, the device α will primarily be dependent on quantum mechanical reflections at the collector barrier.

The MFP numbers presented here are very different from the numbers extracted from similar experiments done by Dasgupta et al.[78] which estimated MFP ~ 40nm in GaN and exhibited an increasing trend with injection energy. The reason behind this discrepancy is believed to be the lack of CE operation in the HETs used for MFP extraction in the previous experiment. As a result CB measurements were used to estimate α . The discussion in Chapter 2 shows that in presence of high R_B, CB measurements can result in extraction of artificially large α . The experiments presented in this work, therefore, are much more accurate in their estimation of MFP and the extracted numbers closely agree with theoretical MFP (Figure 4.13).

4.3 Hot Electron Injection and Collection

The primary focus of the previous section was to understand hot-electron transport and use experimental mean free path measurements to guide future device design. This section discusses hot electron injection and collection which are very important aspects of the device. Hot electron injection determines several important device metrics like injection energy, gain and current density. We have already seen how the collector barrier adds to base thickness. This section discusses the quantum mechanical reflections at the collector barrier and their impact on device gain.

4.3.1 Injection

The emitter barrier formed by the AlN P-D layer provides several advantages over alternative designs in terms of ease of growth and processing. However, the injection mechanism for such a barrier is very complex in comparison to a simple Schottky barrier. By using bias dependent calculations of transmission probability and current density (software developed by Trey Suntrup at UCSB), it is clear that the AlN P-D barrier behaves like a thermionic injection barrier where the barrier height is ϕ_{EB} (Figure 4.22). However, since electrons near the emitter fermi level have to tunnel across the AlN layer before being injected, the tunneling probability plays a key role in determining maximum current density. Figure 4.23 shows the transmission probability across some AlN diodes at flat-band (when the conduction band in the emitter

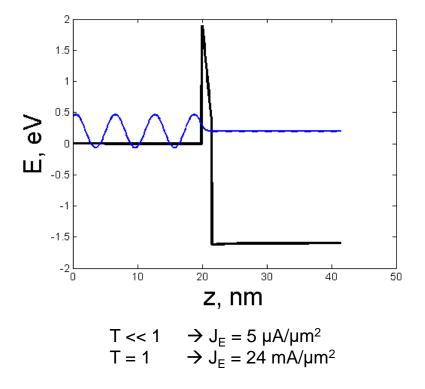


Figure 4.22 Injection of hot-electrons across the AlN barrier

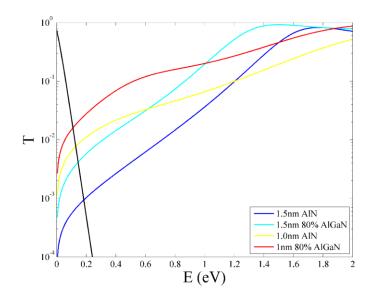


Figure 4.23 Transmission probability across the AlN layer. Black line represents Fermi distribution

GaN is flat). The AlN tunneling probability can thus suppress the current density by as much as 2-3 orders of magnitude. Current density calculations show that the maximum theoretical current density for such diodes is $\sim 10 \text{ kA/cm}^2$.

Chapter 6 discusses some design improvements in the emitter barrier structure to enable much larger current densities. Here, the focus is on finding experimental evidence of suppression of current density. The current density in HETs is primarily limited by base resistance at present so it is not the right tool to study current density. AlN P-D diodes can be used to understand limits on current density. The equation for current transport across a thermionic barrier is,

$$J_E = A^* T^2 e^{-\frac{q\phi_B}{k_B T}} \left(e^{\frac{qV}{k_B T}} - 1 \right)$$

where A^* is the Richardson constant and is equal to, $4\pi em^*k^2/h^3$. Since this is just dependent on material constants, it can be easily calculated for most materials. The derivation of this equation, however, assumes a transmission probability of 1 for any electrons with more energy than the barrier. For complex barrier structures like the HET emitter barrier, transmission probability is much smaller than 1. When re-derived for cases where transmission probability is lower than 1, the new thermionic equation is,

$$J_E = A^{**}T^2 e^{-\frac{q\phi_B}{k_B T}} \left(e^{\frac{qV}{k_B T}} - 1 \right)$$

where A^{**} is the new Richardson constant and is equal to the product of the regular Richardson constant and an effective transmission probability across the AlN layer. The A^{**} can be extracted using diode measurements and can provide a good estimate of the effective

transmission probability. In order to test this, AlN diodes were grown and fabricated followed by temperature dependent I-V characterization. For a simple thermionic barrier, the Richardson plot can readily give A* and ϕ_B by extracting J_S (extrapolated current at zero bias) from I-V characteristics at each temperature and performing a linear fit to $\ln(J_S/T^2)$ vs q/k_BT using,

$$\ln\left(\frac{J_S}{T^2}\right) = \ln(A^*) - \frac{q}{k_B T}\phi_B$$

For real diodes, however, lateral fluctuations in barrier height influence the Richardson plot by introducing a second order term. The current equation now becomes,

$$\ln\left(\frac{J_S}{T^2}\right) = \ln(A^*) - \left(\frac{q}{k_B T}\right)\phi_B + \left(\frac{q}{k_B T}\right)^2 \frac{\sigma_s^2}{2}$$

A second order fit to this equation yields A^* , ϕ_B , and σ_s (variance in barrier height). Figure 4.24 shows such a fit for a 1.5nm AlN diode.

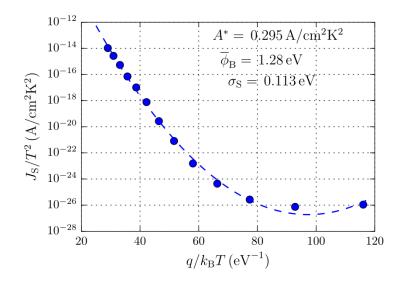


Figure 4.24 Richardson Plot of emitter diode with 1.5nm AlN

The extracted A* of ~ $0.295 \text{ A/cm}^2\text{K}^2$ is two orders of magnitude lower than the theoretical A* for GaN. Using this same technique on an InGaN diode yields an A* that is very close to ideal. This is very clear evidence of the effect of tunneling on the current density in HETs.

4.3.2 Collection

The collector barrier formed by the InGaN P-D influences device characteristics in multiple ways. As part of the base thickness, it has a direct effect on current gain as discussed in Chapter 3. In addition, it forms the collector barrier which affects current gain and leakage. Leakage characteristics across the collector barrier depend on the barrier height but are also a strong function of dislocation density. This section will focus only on the effect of collector barrier on current gain by using theoretical calculations of quantum mechanical reflections.

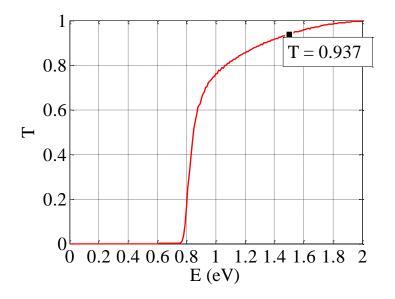


Figure 4.25 Quantum mechanical reflections at the InGaN barrier

Figure 4.25 shows the simulated transmission probability across the InGaN collector barrier. The simulated injection energy in the HETs using 1.5nm AlN emitter is ~ 1.5eV. The collector transmission probability is ~ 0.937 at this energy corresponding to a current gain of ~ 15. In addition, as the collector barrier is reverse biased, the transmission probability across it increases thus increasing the current gain. The design space picture now looks like Figure 4.26, where the horizontal lines show maximum α for different injection energies.

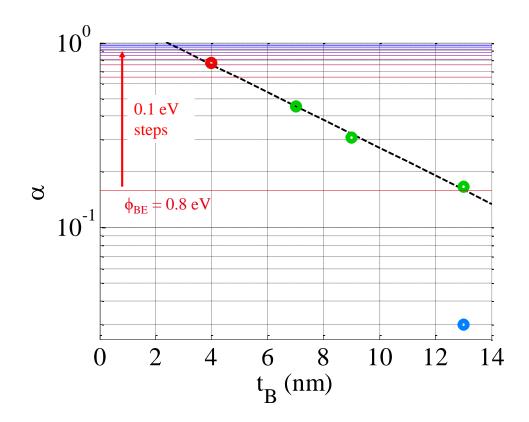


Figure 4.26 Transfer ratio as a function of injection energy for fixed collector barrier

4.4 Summary

To summarize, this chapter first used 3D k-space maps generated using an MC simulator to develop an intuitive understanding of scattering processes for hot-electrons. This was also used to motivate the use of an equation of the form $\alpha = \alpha_0 e^{-\frac{t_B}{\lambda_m f p}}$ for extraction of mean free path. Experiments on III-N HET structures grown on MOCVD and MBE were performed to extract MFP. The MOCVD structures used an AlGaN P-D as the emitter while the MBE structures used an AlN P-D. The extracted values were in close agreement with theoretically calculated MFP. These measurements were used to predict a current gain of ~ 10 at t_B = 3nm. Finally, the implications of injection and collection mechanism on the device characteristics were discussed. Suppression of current density due to tunneling in AlN diodes was demonstrated using temperature dependent measurements.

5 HIGH COMPOSITION INGAN QUANTUM WELL HET

In Chapter 3 the focus was on shrinking the base thickness using an AlN/GaN/InGaN design. The GaN interlayer was used as a transitional layer to change growth conditions from InGaN like to AlN like. The minimum achievable GaN thickness was ~2nm (limited by leakage issues) using that growth paradigm. Also, the 2nm InGaN (20%) used earlier was not enough to achieve a low I_{BCleak} . The minimum total base thickness is thus ~ 4-5nm for the growth methodology used in the last chapter. Even with all these limitations, gain of 3.5 was demonstrated by scaling the hot-electron transit distance to 4nm.

Even though gain of 3.5 is sufficient to test the high-frequency potential of III-N HETs, the focus of this chapter is still on exploring the limits of DC current gain. With $\beta = 3.5$ or $\alpha =$ 0.78, 22% of the injected current still goes into the base. As we look to increase current density in the future, the resistive voltage drops in the base caused by the base current can pose a serious problem. This problem is even more severe in HETs compared to HBTs as the base charge depletes with emitter bias in HETs thus degrading R_B too. It is therefore extremely important to find the right design for high DC current gain if the III-N HET is to be a useful transistor in the future. Chapter 4 predicted current gain ~ 10 at total base thickness of 3nm. The focus of this chapter is on coming up with a HET design, growth and process which can help achieve a 3nm base.

5.1 InGaN QW HET Design

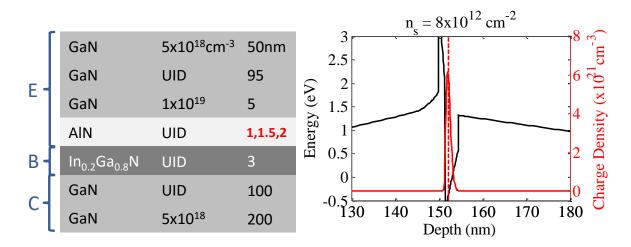
Since InGaN and AlN are such different materials in terms of their structural and electronic properties and also growth regimes, in order to shrink the base further, the growth regimes for these layers need to be closer. This will help in reduction/elimination of the GaN layer in the base. Growth of InGaN under AlN like conditions is extremely difficult if not impossible. In this chapter, therefore, the focus is on growth of AlN at InGaN growth temperature. This potentially allows for further scaling of the base for higher gain by removing the GaN interlayer. Since the AlN layer is grown at LT now, the B-C leakage issue can also be potentially mitigated. The next sections discuss the experiments performed towards this goal.

5.2 Conductivity of 2DEG at AlN/InGaN Interface

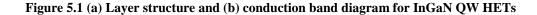
All experiments in this section use a different MBE (Gen930) because of some growth issues with the machine used in the previous chapters (GenII). As always, the machine condition was tested by growing individual LT AlN and InGaN diodes. The diode IV characteristics were rectifying by > 2 orders of magnitude with turn-on voltages close to expected values.

5.2.1 Structure, Growth, and Results

The device structure and band diagram is shown in Figure 5.1. Three samples with different AlN thicknesses are used for this experiment in order to find out the optimum AlN thickness



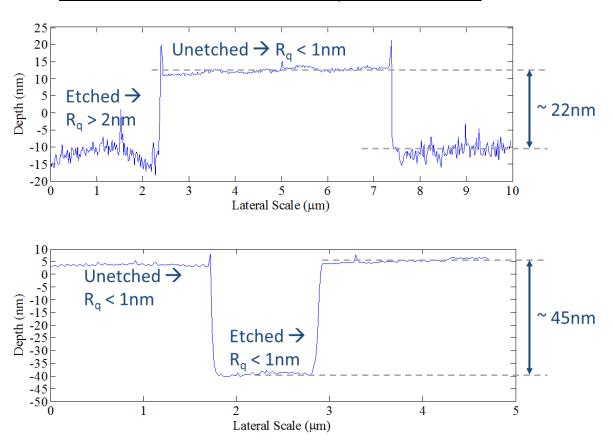
CHAPTER 5 HIGH COMPOSITION INGAN QUANTUM WELL HET



for gain. The InGaN thickness used is 3nm as it gave lower leakage compared to 2nm InGaN in separately grown diode structures.

The growth of this structure is very similar to MBE HETs describe earlier except for the AlN layer. After the growth of InGaN, the substrate temperature and In flux were kept the same and Al cell shutter was opened. The In does not incorporate into the crystal but serves as surfactant to enable growth of smooth AlN even at the growth temperature of InGaN. After AlN growth, the 5nm modulation doped GaN layer was also grown at the same temperature and then a growth interrupt was introduced in order to raise substrate temperature. Separate diode and test structures showed good rectification in the individual diodes and good surface morphology for LT AlN and InGaN layers when grown separately.

The process flow for these devices was also identical to the flow described in Chapter 3. After fabrication, however, the transistors showed no modulation in CE biasing. This is strange because the diodes when grown separately were rectifying. Also, the B-C diode when

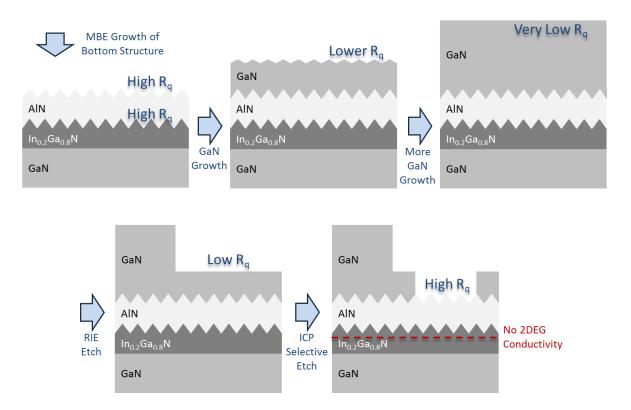


CHAPTER 5 HIGH COMPOSITION INGAN QUANTUM WELL HET

Figure 5.2 AFM images of (a) AlN/InGaN HET after the selective etch (b) co-loaded GaN template with the same selective etch duration

measured on the transistor had low leakage. The answer lies in the fact that base TLMs showed non-ohmic behavior and very high resistance. As a result of bad base contacts, the intrinsic device was not biased at all. This effect seems to be quite similar to what was seen in Chapter 2. The lack of base contacts can be due to either the contacts or the base 2DEG itself.

To further investigate the cause of non-ohmic base contacts, surface morphology of the structure was examined. The surface roughness of the structures before processing was < 1nm. After the first RIE etch, there was no marked increase in the roughness. However, after the selective etch which is supposed to stop on AlN, very high roughness > 2nm was observed.



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Figure 5.3 Schematic showing the evolution of surface morphology with growth and processing.

At the same time, GaN templates and GaN/AlN/GaN structures subject to the same selective etch process showed very good surface morphology with roughness less than or equal to 1nm. Figure 5.2 shows the measured AFM results after the selective etch. The difference in etch depth measured on the HET and a co-loaded GaN template clearly shows that the etch selectively stops on AlN. This indicates that the roughness measured after the selective etch on HETs is in fact the roughness of the AlN layer itself. This roughness is unobservable on the as grown epi because the surface morphology recovers when 150nm GaN is grown on top of the AlN layer. Figure 5.3 shows a schematic of how the roughness originates, gets masked by growth and again manifests after the selective etch. The lack of base conductivity can therefore

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be directly related to the bad surface morphology of the AlN surface. The next part describes experiments to understand the origin of this issue and potential solutions.

	GaN	UID	5	H1	H2	H3
Channel -	AIN	UID	2	LT	LT	HT
	GaN	UID	0,1	NA	LT	LT
	In _{0.1} Ga _{0.9} N	UID	10	LT	LT	LT
	GaN	UID	>100			
	GaN	S. I.				

5.2.2 AlN/InGaN HEMTs

Figure 5.4 Layer structure and growth conditions of the AlN/InGaN HEMTs

Figure 5.4 describes the HEMT structures used in this experiment. These structures are meant to model the conductivity of the base region of the HET. One of the possible causes for lack of conductivity, as discussed previously, is the roughness of AlN surface. Since the AlN layer when grown separately under the same growth conditions does not show an increased roughness, it indicates that the degradation in morphology is somehow caused by the growth of AlN on InGaN specifically. In order to conclusively prove this, three samples were grown using MBE. The first sample (H1) was similar to the HET structure used in the last section i.e. 2DEG at AlN/InGaN interface. The second sample (H2) has a 1nm LT GaN layer in between the InGaN and LT AlN layers. The third sample (H3) also has a 1nm LT GaN layer, however, the AlN is grown at HT after a growth interrupt. To test the channel conductivity, Indium-dot

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Hall measurements were performed on these HEMTs and charge density and mobility was extracted. Table 5.1 summarizes the results of these Hall measurements.

Sample	Mobility (cm ² /V.s)	Charge (cm ⁻²)	$R_{sh}\left(\Omega/sq\right)$
H1	NA	NA	∞
H2	200	8x10 ¹²	4000
H3	400	8x10 ¹²	2000

Table 5.1 Summary of charge and mobility of AlN/InGaN HEMTs

As expected, sample H1 exhibited no channel conductivity while both H2 and H3 had reasonable mobility and charge. With the insertion of just 1nm LT GaN interlayer, the surface morphology was recovered and the channel conductivity increased. Sample H3 had even better mobility indicating that the LT AlN by itself degrades the mobility too. However, a growth interrupt to raise substrate temperature just 1nm away from InGaN might be very bad for B-C leakage in HETs. For HEMTs this structure works only because the back barrier is semi-insulating GaN.

To conclude, this experiment proves that growth of AlN on InGaN causes degradation in morphology of that interface leading to no conductivity in the channel. The physical mechanism of this degradation could be intermixing. Since the Al-N bond is much stronger than In-N, growth of AlN directly on InGaN could result in Al displacing the In from the InGaN layer.

5.3 Summary

This chapter introduced a new HET design which can potentially scale the base to 2-3 nm dimensions. The new design uses an InGaN layer as the base and collector barrier simultaneously. However, issues with the morphology of AlN/InGaN interface prevented the formation of a conductive 2DEG. The evidence strongly suggests the presence of intermixing at AlN/InGaN interface. The intermixing was readily eliminated by insertion of a thin LT GaN and InGaN. Further investigation is required to implement the HET with a thin LT GaN interlayer. In addition, the exact relationship between growth conditions/methodology and intermixing needs to be explored.

6 CONCLUSION AND FUTURE WORK

6.1 Conclusion

The work presented in this dissertation can be summarized in the following few points.

- Chapter 1 discussed the operation and design principles of a general HET. A discussion on the HET family of transistors was then presented and used to motivate the use of the III-N system for studying HETs. The two major reasons for studying a HET are, building a high-frequency transistor and, understanding hot-electron physics in the III-N system.
- Chapter 2 introduced a new HET design using polarization-dipoles and used it to demonstrate transistor action in III-N HETs for the first time. The maximum β achieved was ~ 0.1.
- Chapter 3 focused on scaling the base thickness by reducing the GaN thickness in the base, moving from AlGaN to AlN in the emitter, and increasing InGaN composition. A new method of making base contacts via tunneling through the AlN layer was introduced in order to enable base scaling. The maximum β achieved was ~ 3.5 using a 4nm GaN/In_{0.2}Ga_{0.8}N base.
- Chapter 4 was focused on studying mean free path: first qualitatively using MC simulations, then quantitatively using existing literature, and finally empirically using

III-N HETs. In addition, the implications of injection and collection mechanism on device characteristics were discussed.

• In Chapter 5, a III-N HET with AlN grown directly on InGaN was attempted for high gain. It was discovered that intermixing at the AlN/InGaN interface highly degraded conductivity. A thin GaN interlayer was then introduced to preserve the interface quality.

Despite all the design, growth, and process constraints, and the fast scattering rates in III-Nitrides, this thesis has been successful in demonstrating high current gain (~ 3.5) in III-N HETs for the first time.

6.2 Future Work

Based on all the understanding developed in this work, this section looks at some avenues of future exploration that will be extremely important to take the III-N HET to the next level.

6.2.1 Base Resistance

As discussed in Chapter 1, base resistance is one of the most important parameters for highfrequency operation. Since the mobility in the InGaN base will be limited due to alloy scattering, high base charge is critical in order to achieve low R_B in III-N HETs. Also, since the base charge reduces with emitter bias, it is important that charge is introduced in a way that it remains independent of device bias. III-N HEMTs rely on high 2DEG charge only at zero gate bias and the 2DEG gets depleted with gate bias. Therefore, the problem of

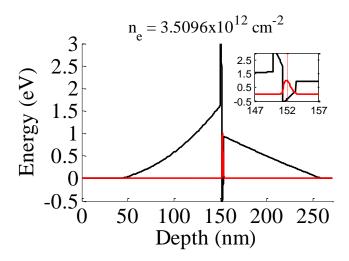


Figure 6.1 Basic InGaN QW HET with doping only in the n+ emitter and collector contact layers. maintaining high 2DEG charge at all bias values has never been attempted and would require some novel design and growth techniques. Different methods of introducing base charge in a III-N HET are discussed next. The baseline structure for comparing base charge is an InGaN QW HET structure (Figure 6.1).

Base Doping

Simply doping the base does very little to increase base charge as the E_f is very high above the E_c in the 2DEG region. Any dopants in the region won't be ionized at all thus severely limiting the amount of charge that can be introduced by simple doping. This is verified by band-diagram simulations (Figure 6.2) which show a very modest increase in base charge even after heavily doping the base. Empirically, however, base doping has been seen to improve base contacts in highly scaled III-N HETs (Chapter 3).

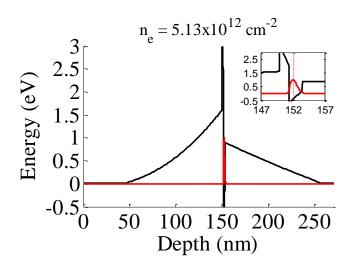


Figure 6.2 HET with InGaN QW doped at 5e19 cm⁻³

Modulation Doping

Modulation doping is the technique of introducing charge in a QW by doping remotely in a barrier region of the structure. Since the HET has an InGaN QW with barriers on both sides, there are multiple ways of modulation doping for base charge.

• Emitter GaN layer : Modulation doping the emitter GaN layer is the easiest method of introducing base charge and was used in Chapter 3. However, as the emitter bias is increased for current injection, any doping in the emitter GaN layer will no longer remain depleted. Thus, the charge introduced into the base will eventually go away (Figure 6.3). This also leads to an important insight that modulation doping must be introduced in regions that will always be depleted no matter what the bias conditions are.



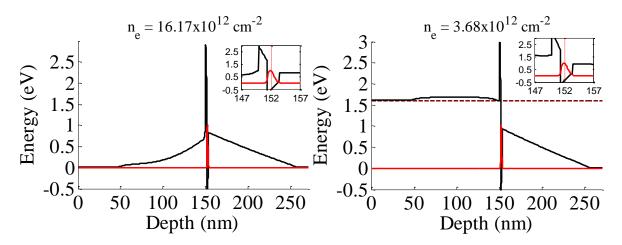


Figure 6.3 Modulation doping in a 2nm GaN layer next to the AlN at 5e19 cm⁻³ (a) at equilibrium and (b) at 1.6V emitter bias.

Emitter AlN : This layer in the emitter remains depleted irrespective of emitter bias since it has a large ΔE_c with GaN. Addition of dopants to the AlN would ensure that all of them result in base charge at all bias conditions (Figure 6.4). The limits of doping AlN without degrading material quality, thus, need to be studied.

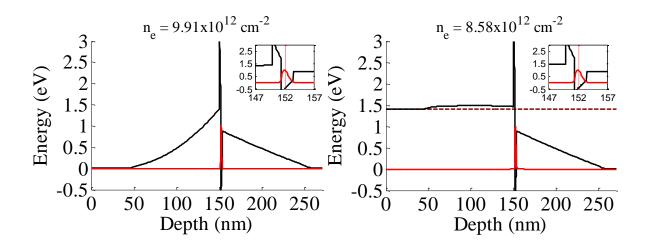


Figure 6.4 Modulation doping in the AlN at 5e19 cm⁻³ (a) at equilibrium and (b) at 1.4V emitter bias.

Base : A thin GaN layer can be introduced in the middle of the InGaN base (inset in Figure 6.5). Since this layer has a ΔE_c with InGaN, any dopants in this layer will result in base charge that does not deplete with bias. However, addition of GaN increases base thickness thus affecting the gain. This tradeoff needs to be investigated.

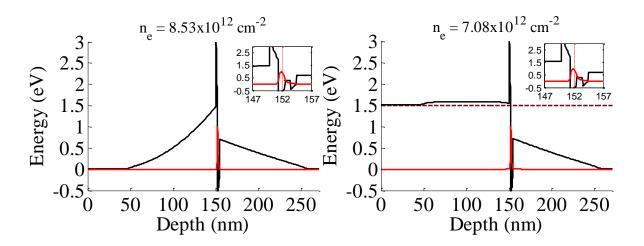


Figure 6.5 Modulation doping in a 1nm GaN layer at 5e19 cm⁻³ in the middle of the InGaN base (a) at equilibrium and (b) at 1.5V emitter bias.

Collector GaN : Since the B-C diode is always reverse biased, doping the collector GaN also results in base charge that does not decrease with bias. However, doping the collector reduces the effective tunneling thickness for the base 2DEG into the collector. This will result in higher leakage currents and is therefore not the best method of introducing base charge.

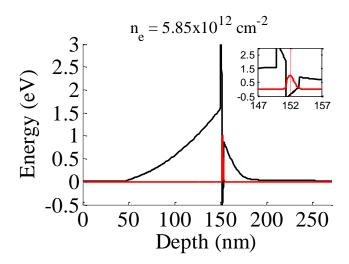


Figure 6.6 Collector GaN doped at 1e18 cm⁻³

Polarization Graded Collector : Polarization fields can be used to counter the issue of reduction in tunneling distance due to collector doping. In other words, instead of a UID GaN layer, the collector can be made using either an InGaN→GaN or a GaN→AlInGaN graded layer. The polarization fields in such collector layers can be used to engineer a collector barrier with large tunneling distance for low leakage and high doping for low R_B. A collector with GaN→AlInGaN grading can also be used to construct a rectangular collector barrier which does not inject current into the base.

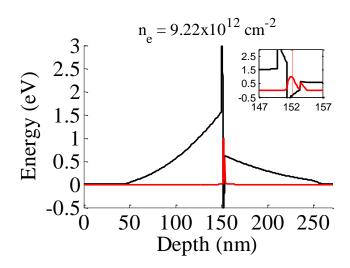


Figure 6.7 Collector GaN replaced by graded layer from 5% InGaN to GaN doped at 5e17 cm⁻³ A HET design with AlN doping and a graded and doped collector barrier can therefore be used to introduce ~ 1×10^{13} cm⁻² base 2DEG charge which is not depleted by emitter bias.

6.2.2 Breakdown Voltage

Breakdown voltage is low in III-N HETs for two primary reasons. First is the presence of defects which assist tunneling leakages and reduce breakdown voltage. Second is the very nature of vertical unipolar devices. In vertical devices, any voltage applied across the B-C junction rapidly increases the fields across that region. In contrast, lateral devices like the HEMT split the applied drain bias into two fields. The vertical field which can cause gate-drain leakage gets pinned while the lateral field keeps increasing. Unipolar devices also do not use the full bandgap of the material system. Instead only the conduction band is used to engineer barriers which block leakage. Therefore, HETs in the III-N system have such low breakdown voltage in spite of the presence of a large bandgap.

CHAPTER 6 CONCLUSION AND FUTURE WORK

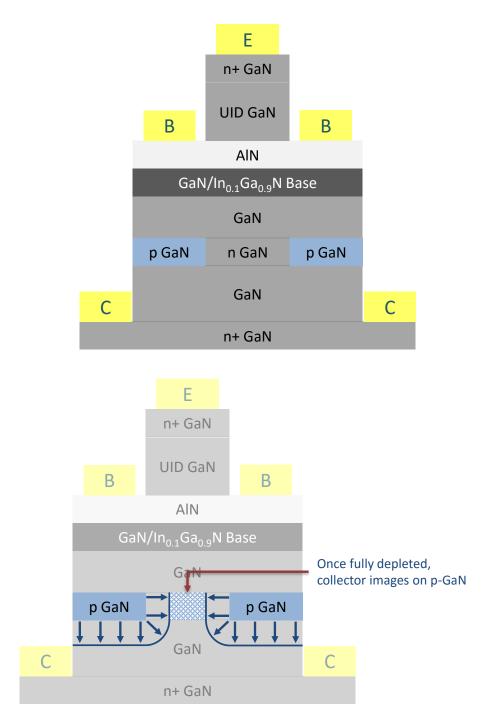


Figure 6.8 High breakdown voltage III-N HET (a) structure and (b) mechanism

Growth on bulk GaN with low dislocation density can be used to reduce defect related leakages. However, in order to achieve the breakdown fields of III-N p-n diodes in a III-N

HET, novel device structures are needed. One such structure is shown in Figure 6.8. This structure uses a 2D p-n junction below a standard HET structure to pin the electric fields in the B-C region of the HET. This can be used to transfer the breakdown from a B-C tunneling breakdown to a p-n junction breakdown. Growth and fabrication of complex structure like this will introduce additional tradeoffs and constraints. Novel techniques in growth and processing will have to be explored in order to achieve the maximum possible breakdown in III-N HETs. Reasonable breakdown voltages (~10V) can still be achieved by growth on bulk GaN.

6.2.3 RF Operation

With good base resistance and reasonable breakdown voltage, development of high-frequency devices can be attempted. Some of the important questions that need to be answered during this development process are highlighted below. A more detailed discussion on the high-frequency tradeoffs for III-N HETs is presented in Appendix B.

Current Density

High current density of the order of ~ $1MA/cm^2$ (for low dynamic resistance) has been shown to be critical for ultra-high-frequency operation of HBTs. Similar requirements also apply for HETs. The current densities demonstrated in this work have been of the order of a few kA/cm². Huge improvements are thus required on this front. The AlN barrier which is used for hotelectron injection can limit the current density due to low tunneling probability across that layer. Since the presence of this layer is critical for hot-electron injection and also for basecontacts it cannot be removed. Also, no other device designs exist at present which can enable

high energy injection and contacts to a scaled base at the same time. The best method, therefore, for improving current density is to remove the AlN tunneling choke by the use of resonant tunneling. This can be done by introducing a thin GaN layer in the middle of the AlN layer. A quasi-bound state is formed in this thin GaN QW which enables resonant tunneling. The thickness of the GaN layer needs to be tuned such that the resonant tunneling energy coincides with the E_f in the emitter. This would ensure maximum injection current.

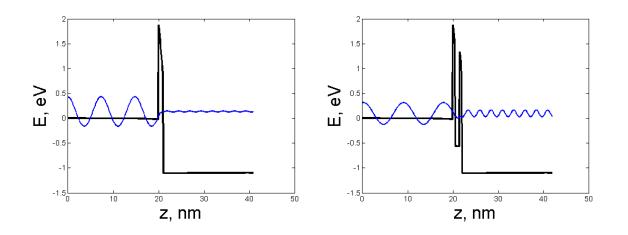


Figure 6.9 Wavefunction transmission probability with (a) 1nm AlN barrier and (b) resonant tunnel barrier with 1nm GaN between the AlN

Figure 6.9 shows the electron wavefunction near the Fermi-level for an emitter diode biased at maximum voltage. The insertion of a thin GaN layer in the AlN increases transmission probability by several orders of magnitude. This is clearly visible in Figure 6.10a where the peak transmission probability shifts closer to the Fermi-level as GaN layer thickness is increased. Beyond a certain GaN thickness, the lowest quasi-bound state shifts lower and a second quasi-bound state at high energy appears. The maximum current density calculated for

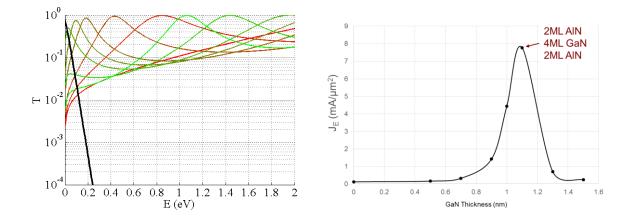


Figure 6.10 (a) Transmission probability (red→green is increasing GaN thickness, black is Fermi-Dirac distribution) (b) Maximum current density at different GaN interlayer thicknesses

different GaN thicknesses (Figure 6.10b) shows the presence of an optimal thickness which can theoretically give current density ~ 0.8MA/cm².

Another way of improving current density is to use a heterojunction emitter with a large ΔE_c to GaN. In order to achieve a thermionic emission barrier using a heterojunction, graded layer need to be used. One example of such an emitter would be a graded and doped AlGaN layer followed by a constant composition AlGaN layer. This can result in a triangular barrier with potentially high current density. Graded InAlN could also serve as an emitter for a HET as it offers the advantage of lattice matching and large ΔE_c . The major issue with such barriers though is the lack of a reliable base contact process. The selective etches used previously for the thin AlN emitter structure cannot work for a graded heterojunction emitter structure.

Self-Aligned Process

Current density and base resistance can also be improved by lateral device scaling. Base contact resistance would need to be reduced by using regrowth[79]. Also, a self-aligned

process will be required to reduce base access resistances. Emitter and collector resistances can be reduced by increasing n-type doping. Figure 6.11 shows what a scaled self-aligned HET structure for RF measurements might look like.

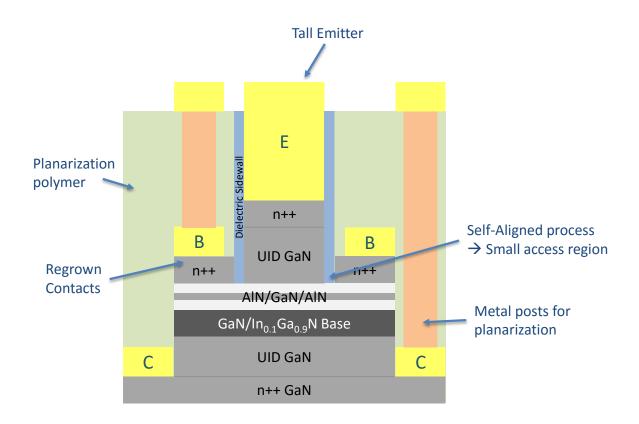


Figure 6.11 Potential device structure of a RF III-N HET

Collector thickness

As collector thickness is increased, the capacitance and leakage reduce however the transit delay across the collector increases. This tradeoff exists both in HBTs and HETs for RF operation. Since the drift velocity of electrons in the collector is low in GaN compared to other material systems, the collector delay will become more and more important as we try to push the device to higher frequencies.

7 **References**

- [1] J. I. Pankove, E. A. Miller, and J. E. Berkeyheiser, "GaN electroluminescent diodes," in *1971 International Electron Devices Meeting*, 1971, vol. 17, pp. 78–78.
- [2] S. Nakamura, T. Mukai, and M. Senoh, "Candela-class high-brightness InGaN/AlGaN double-heterostructure blue-light-emitting diodes," *Appl. Phys. Lett.*, vol. 64, no. 13, p. 1687, Mar. 1994.
- [3] S. Nakamura, S. Pearton, and G. Fasol, *The blue laser diode: the complete story*. 2000.
- [4] I. Vurgaftman and J. R. Meyer, "Band parameters for nitrogen-containing semiconductors," *J. Appl. Phys.*, vol. 94, no. 6, p. 3675, Aug. 2003.
- [5] J. Wu, "When group-III nitrides go infrared: New properties and perspectives," J. *Appl. Phys.*, vol. 106, no. 1, p. 011101, Jul. 2009.
- [6] B. Heying, R. Averbeck, L. F. Chen, E. Haus, H. Riechert, and J. S. Speck, "Control of GaN surface morphologies using plasma-assisted molecular beam epitaxy," J. Appl. Phys., vol. 88, no. 4, p. 1855, Aug. 2000.
- [7] S. Keller, G. Parish, J. J. Xu, B. P. Keller, S. P. DenBaars, and U. K. Mishra, "Gallium nitride based high power heterojunction field effect transistors: process development and present status at UCSB," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 552– 559, Mar. 2001.
- [8] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 13–15, Jan. 2006.
- [9] V. Adivarahan, W. H. Sun, A. Chitnis, M. Shatalov, S. Wu, H. P. Maruska, and M. A. Khan, "250 nm AlGaN light-emitting diodes," *Appl. Phys. Lett.*, vol. 85, no. 12, p. 2175, Sep. 2004.
- [10] J. W. Raring, E. M. Hall, M. C. Schmidt, C. Poblenz, B. Li, N. Pfister, D. Kebort, Y.-C. Chang, D. F. Feezell, R. Craig, J. S. Speck, S. P. Denbaars, and S. Nakamura, "State-of-the-art continuous-wave InGaN laser diodes in the violet, blue, and green wavelength regimes," in *SPIE Defense, Security, and Sensing*, 2010, p. 76860L– 76860L–10.

- [11] C. J. Neufeld, N. G. Toledo, S. C. Cruz, M. Iza, S. P. DenBaars, and U. K. Mishra, "High quantum efficiency InGaN/GaN solar cells with 2.95 eV band gap," *Appl. Phys. Lett.*, vol. 93, no. 14, p. 143502, Oct. 2008.
- [12] O. Ambacher, "Growth and applications of Group III-nitrides," J. Phys. D. Appl. Phys., vol. 31, no. 20, pp. 2653–2710, Oct. 1998.
- K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos, and M. Micovic, "Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 2982–2996, Oct. 2013.
- [14] Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by Field Plate Optimization," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004.
- [15] T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "High-power AlGaN/GaN HEMTs for Ka-band applications," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 781–783, Nov. 2005.
- [16] Nidhi, S. Dasgupta, D. F. Brown, S. Keller, J. S. Speck, and U. K. Mishra, "N-polar GaN-based highly scaled self-aligned MIS-HEMTs with state-of-the-art f<inf>T</inf>.L<inf>G</inf> product of 16.8 GHz-µm," in 2009 IEEE International Electron Devices Meeting (IEDM), 2009, pp. 1–3.
- [17] D. Denninghoff, J. Lu, E. Ahmadi, S. Keller, and U. K. Mishra, "N-polar GaN/InAlN/AlGaN MIS-HEMTs with 1.89 S/mm extrinsic transconductance, 4 A/mm drain current, 204 GHz f<inf>T</inf> and 405 GHz f<inf>max</inf>," in 71st Device Research Conference, 2013, pp. 197–198.
- [18] S. Kolluri, S. Keller, S. P. Denbaars, and U. K. Mishra, "N-polar GaN MIS-HEMTs with a 12.1-W/mm continuous-wave output power density at 4 GHz on sapphire substrate," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 635–637, May 2011.
- [19] Y.-F. Wu, R. Coffie, N. Fichtenbaum, Y. Dora, C. S. Suh, L. Shen, P. Parikh, and U. K. Mishra, "Total GaN solution to electrical power conversion," in 69th Device Research Conference, 2011, pp. 217–218.
- [20] D. S. Lee, X. Gao, S. Guo, D. Kopp, P. Fay, and T. Palacios, "300-GHz InAlN/GaN HEMTs With InGaN Back Barrier," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1525–1527, Nov. 2011.

- [21] K. Shinohara, D. Regan, I. Milosavljevic, A. L. Corrion, D. F. Brown, P. J. Willadsen, C. Butler, A. Schmitz, S. Kim, V. Lee, A. Ohoka, P. M. Asbeck, and M. Micovic, "Electron Velocity Enhancement in Laterally Scaled GaN DH-HEMTs With <formula formulatype='inline'><tex Notation='TeX'>\$f_{T}\$</tex></formula> of 260 GHz," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1074–1076, Aug. 2011.
- [22] L. McCarthy, I. Smorchkova, Huili Xing, P. Kozodoy, P. Fini, J. Limb, D. L. Pulfrey, J. S. Speck, M. J. W. Rodwell, S. P. DenBaars, and U. K. Mishra, "GaN HBT: toward an RF device," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 543–551, Mar. 2001.
- [23] C. A. Mead, "Operation of Tunnel-Emission Devices," J. Appl. Phys., vol. 32, no. 4, p. 646, 1961.
- [24] J. M. Shannon, "Hot-electron camel transistor," *IEE J. SolidState Electron Devices*, vol. 3, no. 5, p. 142, 1979.
- [25] J. M. Shannon and A. Gill, "High current gain in monolithic hot-electron transistors," *Electron. Lett.*, vol. 17, no. 17, p. 620, 1981.
- [26] M. Heiblum, "Tunneling hot electron transfer amplifiers (theta): Amplifiers operating up to the infrared," *Solid. State. Electron.*, vol. 24, no. 4, pp. 343–366, Apr. 1981.
- [27] M. Heiblum and M. V. Fischetti, "Ballistic hot-electron transistors," *IBM J. Res. Dev.*, vol. 34, no. 4, pp. 530–549, Jul. 1990.
- [28] Z. Yang, Y. Zhang, D. N. Nath, J. B. Khurgin, and S. Rajan, "Current gain in sub-10 nm base GaN tunneling hot electron transistors with AlN emitter barrier," *Appl. Phys. Lett.*, vol. 106, no. 3, p. 032101, Jan. 2015.
- [29] N. Yokoyama, K. Imamura, S. Muto, S. Hiyamizu, and H. Nishi, "A New Functional, Resonant-Tunneling Hot Electron Transistor (RHET)," *Jpn. J. Appl. Phys.*, vol. 24, no. Part 2, No. 11, pp. L853–L854, Nov. 1985.
- [30] N. Yokoyama, K. Imamura, H. Ohnishi, T. Mori, S. Muto, and A. Shibatomi, "Resonant-tunneling hot electron transistor (RHET)," *Solid. State. Electron.*, vol. 31, no. 3–4, pp. 577–582, Mar. 1988.
- [31] T. Mori, T. Adachihara, M. Takatsu, H. Ohnish, K. Imamura, S. Muto, and N. Yokoyama, "121 GHz resonant-tunnelling hot electron transistors having new collector barrier structure," *Electron. Lett.*, vol. 27, no. 17, p. 1523, 1991.
- [32] T. Daoud, G. Boissier, J. Devenson, G. Sabatini, L. Varani, A. Baranov, and R. Teissier, "Conception and fabrication of InAs-based hot electron transistor," in 2008

References

20th International Conference on Indium Phosphide and Related Materials, 2008, pp. 1–4.

- [33] H. Nguyen van, J. C. Moreno, a. N. Baranov, R. Teissier, and M. Zaknoune,
 "Submicrometer Process and RF Operation of InAs Quantum Hot-Electron Transistors," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 797–799, Jun. 2012.
- [34] S. M. Sze and H. K. Gummel, "Appraisal of semiconductor-metal-semiconductor transistor," *Solid. State. Electron.*, vol. 9, no. 8, pp. 751–769, Aug. 1966.
- [35] D. V. Geppert, "The metal-base transistor," *IRE Trans. Electron Devices*, vol. 9, no. 6, pp. 507–507, Nov. 1962.
- [36] M. M. Atalla and R. W. Soshea, "Hot-carrier triodes with thin-film metal base," *Solid. State. Electron.*, vol. 6, no. 3, pp. 245–250, May 1963.
- [37] J. Hayes, A. Levi, and W. Wiegmann, "Hot-Electron Spectroscopy of GaAs," *Phys. Rev. Lett.*, vol. 54, no. 14, pp. 1570–1572, Apr. 1985.
- [38] A. F. J. Levi and T. H. Chiu, "Room-temperature operation of hot-electron transistors," *Appl. Phys. Lett.*, vol. 51, no. 13, p. 984, 1987.
- [39] H. Kroemer, "Heterostructure bipolar transistors: What should we build?," J. Vac. Sci. *Technol. B Microelectron. Nanom. Struct.*, vol. 1, no. 2, p. 126, 1983.
- [40] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta, R. Lin, D. Lin, and M. Rodwell, "InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2203–2214, Oct. 2011.
- [41] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser, and M. J. W. Rodwell, "130nm InP DHBTs with ft >0.52THz and f<inf>max</inf>>1.1THz," in 69th Device Research Conference, 2011, pp. 281–282.
- [42] P. Kozodoy, S. Keller, S. DenBaars, and U. Mishra, "MOVPE growth and characterization of Mg-doped GaN," J. Cryst. Growth, vol. 195, no. 1–4, pp. 265–269, Dec. 1998.
- [43] D.-H. Kim and J. A. del Alamo, "30-nm InAs Pseudomorphic HEMTs on an InP Substrate With a Current-Gain Cutoff Frequency of 628 GHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 830–833, Aug. 2008.
- [44] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and a. Fung, "Sub 50 nm InP HEMT device

with Fmax greater than 1 THz," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 3, pp. 609–611, 2007.

- [45] J. Lu, D. Denninghoff, R. Yeluri, S. Lal, G. Gupta, M. Laurent, S. Keller, S. P. Denbaars, and U. K. Mishra, "Very high channel conductivity in ultra-thin channel N-polar GaN/(AlN, InAlN, AlGaN) high electron mobility hetero-junctions grown by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 102, no. 2011, pp. 2011–2016, Jun. 2013.
- [46] G. Gupta, M. Laurent, J. Lu, S. Keller, and U. K. Mishra, "Design of polarizationdipole-induced isotype heterojunction diodes for use in III–N hot electron transistors," *Appl. Phys. Express*, vol. 7, no. 1, p. 014102, Jan. 2014.
- [47] G. Gupta, M. Laurent, H. Li, D. J. Suntrup, E. Acuna, S. Keller, and U. K. Mishra, "Design Space of III-N Hot Electron Transistors Using AlGaN and InGaN Polarization-Dipole Barriers," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 23–25, Jan. 2015.
- [48] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. Xing, "InAlN/AlN/GaN HEMTs With Regrown Ohmic Contacts and <formula formulatype='inline'><tex Notation='TeX'> \$f_{T}\$</tex></formula> of 370 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 988–990, Jul. 2012.
- [49] S. Dasgupta, D. F. Brown, F. Wu, S. Keller, J. S. Speck, and U. K. Mishra, "Ultralow nonalloyed Ohmic contact resistance to self aligned N-polar GaN high electron mobility transistors by In(Ga)N regrowth," *Appl. Phys. Lett.*, vol. 96, no. 14, p. 143504, 2010.
- [50] R. Soligo, S. Chowdhury, G. Gupta, U. Mishra, and M. Saraniti, "The Role of the Base Stack on the AC Performance of GaN Hot Electron Transistor," *IEEE Electron Device Lett.*, vol. PP, no. 99, pp. 1–1, 2015.
- [51] C. Crowell and S. Sze, "Ballistic Mean Free Path Measurements of Hot Electrons in Au Films," *Phys. Rev. Lett.*, vol. 15, no. 16, pp. 659–661, Oct. 1965.
- [52] D. J. Suntrup, G. Gupta, H. Li, S. Keller, U. K. Mishra, D. J. S. Iii, G. Gupta, H. Li, S. Keller, and U. K. Mishra, "Measurement of the hot electron mean free path and the momentum relaxation rate in GaN," *Appl. Phys. Lett.*, vol. 105, no. 26, p. 263506, Dec. 2014.
- [53] D. J. Suntrup III, "PhD Dissertation," 2015.

- [54] K. Imamura, S. Muto, N. Yokoyama, M. Sasa, H. Ohnishi, S. Hiyamizu, and H. Nishi, "Characterization of GaAs/AlGaAs hot electron transistors using magnetic field effects on launched-electron transport," *Surf. Sci.*, vol. 174, no. 1–3, pp. 481–486, Aug. 1986.
- [55] S. Dasgupta, A. Raman, J. S. Speck, and U. K. Mishra, "Experimental Demonstration of III-Nitride Hot-Electron Transistor With GaN Base," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1212–1214, Sep. 2011.
- [56] S. R. Lee, D. D. Koleske, K. C. Cross, J. A. Floro, K. E. Waldrip, a. T. Wise, and S. Mahajan, "In situ measurements of the critical thickness for strain relaxation in AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 85, no. 25, p. 6164, Dec. 2004.
- [57] S. Dasgupta, "Growth, Fabrication and Characterization of III-Nitride Hot Electron Transistors," 2011.
- [58] H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and Al[sub 0.25]Ga[sub 0.75]N/GaN grown by molecularbeam epitaxy," J. Appl. Phys., vol. 99, no. 2, p. 023703, 2006.
- [59] B. Mazumder, S. W. Kaun, J. Lu, S. Keller, U. K. Mishra, and J. S. Speck, "Atom probe analysis of AlN interlayers in AlGaN/AlN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 102, no. 11, p. 111603, 2013.
- [60] E. J. Miller, D. M. Schaadt, E. T. Yu, X. L. Sun, L. J. Brillson, P. Waltereit, and J. S. Speck, "Origin and microscopic mechanism for suppression of leakage currents in Schottky contacts to GaN grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 94, no. 12, p. 7611, 2003.
- [61] E. Ahmadi, D. J. Suntrup, C. Lund, J. S. Speck, and U. K. Mishra, "Study and comparison of reversed-bias leakage current in GaN Schottky diodes grown by plasma-assisted and ammonia molecular beam epitaxy," *Submitt. to J. Cryst. Growth*, 2015.
- [62] D. BUTTARI, A. CHINI, A. CHAKRABORTY, L. MCCARTHY, H. XING, T. PALACIOS, L. SHEN, S. KELLER, and U. K. MISHRA, "SELECTIVE DRY ETCHING OF GaN OVER AlGaN IN BCL 3 /SF 6 MIXTURES," *Int. J. High Speed Electron. Syst.*, vol. 14, no. 03, pp. 756–761, Sep. 2004.
- [63] P. Parikh and U. Mishra, "Gallium nitride based diodes with low forward voltage and low reverse current operation," *US Pat. 6*,949,774, vol. 2, no. 12, 2005.
- [64] L. Shen, Y. Pei, L. McCarthy, C. Poblenz, a. Corrion, N. Fichtenbaum, S. Keller, S. P. Denbaars, J. S. Speck, and U. K. Mishra, "Deep-recessed GaN HEMTs using selective

References

etch technology exhibiting high microwave performance without surface passivation," 2007 IEEE/MTT-S Int. Microw. Symp., pp. 623–626, Jun. 2007.

- [65] S. Kolluri, D. F. Brown, M. H. Wong, S. Dasgupta, S. Keller, S. P. DenBaars, and U. K. Mishra, "RF Performance of Deep-Recessed N-Polar GaN MIS-HEMTs Using a Selective Etch Technology Without Ex Situ Surface Passivation," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 134–136, Feb. 2011.
- [66] S. Huang, H. Chen, and K. J. Chen, "Effects of the fluorine plasma treatment on the surface potential and Schottky barrier height of Al[sub x]Ga[sub 1-x]N/GaN heterostructures," *Appl. Phys. Lett.*, vol. 96, no. 23, p. 233510, 2010.
- [67] G. Gupta, E. Ahmadi, K. Hestroffer, E. Acuna, and U. K. Mishra, "Common Emitter Current Gain >1 in III-N Hot Electron Transistors With 7-nm GaN/InGaN Base," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 439–441, May 2015.
- [68] M. Lundstrom, *Fundamentals of Carrier Transport*. Cambridge University Press, 2009.
- [69] K. Wang, J. Simon, N. Goel, and D. Jena, "Optical study of hot electron transport in GaN: Signatures of the hot-phonon effect," *Appl. Phys. Lett.*, vol. 88, no. 2, p. 022103, 2006.
- [70] B. Lee, K. Kim, M. Dutta, and M. Stroscio, "Electron–optical-phonon scattering in wurtzite crystals," *Phys. Rev. B*, vol. 56, no. 3, pp. 997–1000, Jul. 1997.
- [71] H. Ye, G. W. Wicks, and P. M. Fauchet, "Hot electron relaxation time in GaN," *Appl. Phys. Lett.*, vol. 74, no. 5, p. 711, 1999.
- [72] S. Wu, P. Geiser, J. Jun, J. Karpinski, D. Wang, and R. Sobolewski, "Time-resolved intervalley transitions in GaN single crystals," *J. Appl. Phys.*, vol. 101, no. 4, p. 043701, 2007.
- [73] C. Bulutay, B. Ridley, and N. Zakhleniuk, "Electron momentum and energy relaxation rates in GaN and AlN in the high-field transport regime," *Phys. Rev. B*, vol. 68, no. 11, p. 115205, Sep. 2003.
- [74] Y. C. Yeo, T. C. Chong, and M. F. Li, "Electronic band structures and effective-mass parameters of wurtzite GaN and InN," *J. Appl. Phys.*, vol. 83, no. 3, p. 1429, 1998.
- [75] M. Goano, E. Bellotti, E. Ghillino, G. Ghione, and K. F. Brennan, "Band structure nonlocal pseudopotential calculation of the III-nitride wurtzite phase materials system. Part I. Binary compounds GaN, AlN, and InN," *J. Appl. Phys.*, vol. 88, no. 11, p. 6467, 2000.

- [76] J. Iveland, L. Martinelli, J. Peretti, J. S. Speck, and C. Weisbuch, "Direct Measurement of Auger Electrons Emitted from a Semiconductor Light-Emitting Diode under Electrical Injection: Identification of the Dominant Mechanism for Efficiency Droop," *Phys. Rev. Lett.*, vol. 110, no. 17, p. 177406, Apr. 2013.
- [77] M. Wraback, H. Shen, S. Rudin, E. Bellotti, M. Goano, J. C. Carrano, C. J. Collins, J. C. Campbell, and R. D. Dupuis, "Direction-dependent band nonparabolicity effects on high-field transient electron transport in GaN," *Appl. Phys. Lett.*, vol. 82, no. 21, p. 3674, 2003.
- [78] S. Dasgupta, J. Lu, N. Raman, C. Hurni, G. Gupta, J. S. Speck, and U. K. Mishra, "Estimation of Hot Electron Relaxation Time in GaN Using Hot Electron Transistors," *Appl. Phys. Express*, vol. 6, no. 3, p. 034002, Mar. 2013.
- [79] K. Shinohara, D. Regan, A. Corrion, D. Brown, S. Burnham, P. J. Willadsen, I. Alvarado-Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden, D. Chang, V. Lee, A. Ohoka, P. M. Asbeck, and M. Micovic, "Deeply-scaled selfaligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency," 2011 Int. Electron Devices Meet., vol. 2, no. D, pp. 19.1.1–19.1.4, Dec. 2011.

8 APPENDIX A

Process flow for HETs using the AlN etch stop and tunnel contact method.

	Ga Face HET	•			
	Sample #				
	Grower				
1	Alignment Marks		GEETAK_HET	_v3_P2	ALIGN (0, 3.4)
	Dies				
	Clean	Acetone		3'	
		IPA		3'	
		DI		3'	
	Dehydration	Bake	115°C	3'	
	PR	SPR 955	3Krpm	30"	
		Bake	90°C	1'	
		Cool		1'	
	Expose	GCA6300		1.5"	
	Bake	100°C		1'	
	Develop	AZ300MIF		45"	
	•	DI		2'	
	Observe				
	Etch	RIE#5	GEET_HPE	6'	70-75nm/min
	PR Removal	1165 US	 80°C	10'	
		IPA		3'	
		DI		3'	
2	Emitter etch		GEETAK_HET	_v3_P2	EISOP (0, 0)
	Dies				
	Clean	Acetone		3'	
		IPA		3'	
		DI		3'	
	Dehydration	Bake	115°C	3'	
	PR	SPR 955	3Krpm	30"	
		Bake	90°C	1'	
		Cool		1'	
	Expose	GCA6300		1.2"	
	Bake	100°C		1'	
	Develop	AZ300MIF		45"	
	•	DI		2'	
	Observe				

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	Etch	RIE#5	GEET_CLN			
			GEET_LPE		~6nm/min	
	PR Removal	1165 US	80°C	10'		
		IPA		3'		
		DI		3'		
	AFM					
3	Pad Oxide		GEETAK_HET	v3 P2	PADOXN (34 -34)
•	Dies				1700701	
	Clean	Acetone		3'		
	Clean	IPA		3'		
		DI		3'		
	Debydration	Bake	115°C	3'		
	Dehydration PR	OCG825		30"		
	ГÑ		5Krpm	30		
		Bake	95°C	1 ¹		
		SPR 955	3Krpm	30"		
		Bake	90°C	1'		
		Cool		1'		
	Expose	GCA6300		1.5"		
	Bake	100°C		2'		
	Develop	AZ300MIF:	DI 2:1	1'30"		
		DI		2'		
	Observe					
	Oxide	Ebeam#1	SiO2	200nm		
	1.10. 00	1165				
	Liftoff	Down	80°C	>2hrs		
		Spray with	pipette			
		IPA		3'		
		DI		3'		
4	Deee le clatier			5		
4	Base Isolation		GEETAK_HET	_v3_P1	BISOP (3.4	i, U)
	Dies	A = = (= = = =				
	Clean	Acetone		3'		
		IPA		3'		
		DI		3'		
	Dehydration	Bake	115°C	3'		
	PR	SPR 955	3Krpm	30"		
		Bake	90°C	1'		
		Cool		1'		
	Expose	GCA6300		1.2"		
	Bake	100°C		1'		
	Develop	AZ300MIF		45"		
		DI		2'		

	Observe				
	Etch	RIE#5	GEET HPE	3'	70-75nm/min
	PR Removal	1165 US	80°C	10'	
		IPA		3'	
		DI		3'	
	AFM				
5	Contacts		GEETAK_HE1	_v3_P1	CCONT (3.4, -3.4)
					ECONT (0, 0)
	Dies				
	Clean	Acetone		3'	
		IPA		3'	
		DI		3'	
	Dehydration	Bake	115°C	3'	
	PR	OCG825	5Krpm	30"	
		Bake	95°C	1'	
		Cool		1'	
		SPR 955	3Krpm	30"	
		Bake	90°C	1'	
		Cool		1'	
	Expose	GCA6300		1.5"	
	Bake	100°C		2'	
	Develop	AZ300MIF:	DI 2:1	1'30"	
	•	DI		2'	
	Observe				
	Descum	O2	300mT,100W	15"	
	HCI Dip	HCI:DI 1:3		1'	
	Metal Deposition	Ebeam#4	Al/Au	250/2500Å	
		1165			
	Liftoff	Down	80°C	>2hrs	
		Spray with	pipette		
		IPA		3'	
		DI		3'	
6	Base Contact Etch		GEETAK_HET	「_v3_P1	BCONTN (-3.4, 0)
	Dies				
	Clean	Acetone		3'	
		IPA		3'	
		DI		3'	
	Dehydration	Bake	115°C	3'	
	PR	SPR 955	3Krpm	30"	
		Bake	90°C	1'	
		Cool		1'	
	Expose	GCA6300		1.2"	
	Bake	100°C		1'	

	Develop	AZ300MIF		45"		
		DI		2'		
	Observe					
	Etch	ICP#1	Clean	10'		
			Condition	2'		
			Etch			
	PR Removal	1165 US	80°C	10'		
		IPA		3'		
		DI		3'		
	AFM					
7	Base Contact		GEETAK_HE	 Гv3_Р1	BCONTN (-3.4, 0)
	Dies					
	Clean	Acetone		3'		
		IPA		3'		
		DI		3'		
	RTA	Test	400°C, N2	30"		
		Anneal	400°C, N2	10'		
	PR	OCG825	5Krpm	30"		
		Bake	95°C	1'		
		Cool		1'		
		SPR 955	3Krpm	30"		
		Bake	90°C	1'		
		Cool		1'		
	Expose	GCA6300		1.5"		
	Bake	100°C		2'		
	Develop	AZ300MIF:	DI 2:1	1'30"		
		DI		2'		
	Observe					
	HCI Dip	HCI:DI 1:3		1'		
	Metal Deposition	Ebeam#4	Al/Au	250/2500Å		
	Liftoff	1165 Down	80°C	>2hrs		
		Spray with	1			
		IPA	·	3'		
		DI		3'		

Etch rates for various RIE and ICP etches used here are tabulated below. All these etches use a BCl₃ pre-treatment to remove any oxide layers from the GaN surface.

BCl ₃ Pre-treatment	Power	Pressure	Flow	Time
RIE#5 High Power	100W	10mT	10	1'
RIE#5 Low Power	50W	10mT	10	2'
ICP#1 Low Power	200/60W	1.33Pa	10?	2'

Material	Machine	Gas	Power	Pressure	Flow	Rate	Selectivity
GaN	RIE#5	Cl ₂	100W	10mT	10	70- 75nm/min	None
GaN	RIE#5	BCl ₃ /Cl ₂	15W	10mT	20/5	6nm/min	None
GaN	ICP#1	BCl ₃ /SF ₆	200/30W	5Pa	20/5	10nm/min	>100
GaN	ICP#1	BCl ₃ /SF ₆	200/60W	5Pa	20/5	35nm/min	>100
GaN	ICP#2	BCl ₃ /SF ₆	200/30W	5Pa	20/5	35nm/min	>100

The most critical part of the process is the selective etch. Typically epitaxial growth has ~10% error in layer thicknesses. The BCl₃/Cl₂ RIE before the selective etch should take this error into account and under-etch accordingly. Similarly, the amount of over-etch in the BCl₃/SF₆ ICP etch should be governed by the error in layer thickness and etch selectivity. In general it is not advisable to over etch too much as the AlN layer is very thin and the post selective etch anneal step might etch some of the AlN.

Stepper alignment usually drifts within a few days after the weekly calibration. Since the process is short enough to be finished in 3-4 days, it is advisable to time the process with the weekly stepper alignment.

In addition to this, the mask is also capable of fabricating HETs with GSG contact pads. The additional steps are listed below.

	Ga Face HET Pads	GSG				
	Sample #					
	Grower					
1	Oxide + Via		GEETAK_HE	Г_v3_Р2	VIA (-3.4, :	3.4)
	Dies					
	Clean	Acetone		3'		
		IPA		3'		
		DI		3'		
	Dehydration	Bake	115°C	3'		
	Oxide Deposition	PECVD#1/2	200nm			
			Co-Load Si Dummy			
	Clean	Acetone		3'		
		IPA		3'		
		DI		3'		
	Dehydration	Bake	115°C	3'		
	PR	SPR 955	3Krpm	30"		
		Bake	90°C	1'		
		Cool		1'		
	Expose	GCA6300		1.2"		
	Bake	100°C		1'		
	Develop	AZ300MIF		45"		
		DI		2'		
	Observe					
	Oxide Etch Cal	ICP#1	Dummy Si	SiOCInCt +	SiOvert	
	Oxide Etch	ICP#1	Real Sample			
	PR Removal	1165 US	80°C	10'		
		IPA		3'		
		DI		3'		
2	Pad Deposition		GEETAK_HET	Г_v3_Р1	BONDPAD 3.4)	D (-3.4,

Dies				
Clean	Acetone		3'	
	IPA		3'	
	DI		3'	
Dehydration	Bake	115°C	3'	
PR	HMDS	3krpm	30"	
	OCG825	5Krpm	30"	
	Bake	95°C	1'	
	Cool		1'	
	SPR 955	3Krpm	30"	
	Bake	90°C	1'	
	Cool		1'	
Expose	GCA6300		1.5"	
Bake	100°C		2'	
Develop	AZ300MIF		1'30"	
	DI		2'	
Observe				
Descum	O2	300mT,100W	15"	
HCI Dip	HCI:DI 1:3		1'	
Metal Deposition	Ebeam#4	Ti/Au	250/2500Å	
Liftoff	1165 Down	80°C	>2hrs	
	Spray with pipette		10'	
	IPA		3'	
	DI		3'	

9 Appendix B

This appendix presents a discussion on the high-frequency potential of III-N based HETs. Presented below (Figure 9.1) is a charge control analysis of the HET which results in an equation for current gain cutoff frequency (f_T). The power gain cutoff frequency (f_{MAX}) equation can be derived from the small signal model.

$$\begin{aligned} \tau_{BE} &= \frac{\Delta Q_{BE}}{\Delta I_E} \approx \frac{C_{BE}\Delta V_{BE}}{\Delta I_C} = C_{BE} \left(\frac{k_B T}{q I_C}\right) = C_{BE} r_e \\ \tau_B &= \frac{\Delta Q_B}{\Delta I_C} = \frac{q(\Delta n t_B)}{q(\Delta n v_B)} = \frac{t_B}{v_B} \\ \tau_{BC} &= \frac{\Delta Q_{BC}}{\Delta I_C} = \frac{C_{BC}\Delta V_{BC}}{\Delta I_C} = C_{BC} \left(\frac{\Delta V_{BE} + \Delta I_C (R_E + R_C)}{\Delta I_C}\right) = C_{BC} (r_e + R_E + R_C) \\ \tau_C &= \frac{t_C}{2v_C} \\ \frac{1}{2\pi f_T} &= \tau = \tau_{BE} + \tau_B + \tau_{BC} + \tau_C = \frac{t_B}{v_B} + \frac{t_C}{2v_C} + r_e (C_{BE} + C_{BC}) + C_{BC} (R_E + R_C) \\ \frac{1}{2\pi f_T} &= \tau_b + \tau_c + \frac{kT}{qI_c} (C_{je} + C_{cb}) + \frac{C_{cb} (R_{ex} + R_c)}{RC_2} \\ \end{bmatrix} \\ f_{MAX} &= \sqrt{\frac{f_T}{8\pi R_{bb} C_{cbi}}} \end{aligned}$$

Figure 9.1 Charge Control Analysis and the equations of $f_{\rm T}$ and $f_{\rm MAX}$ for a HET

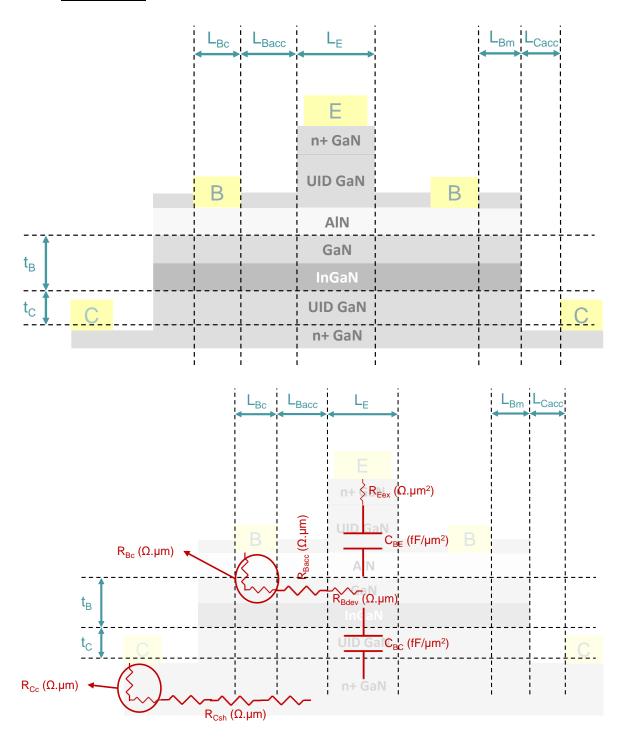


Figure 9.2 Layer structure of the III-N HET with the appropriate dimensions, resistances and

capacitances

<u>Appendix B</u>

Figure 9.2 shows the layer structure of a typical III-N HET as discussed in Chapter 3. The device resistances and capacitances along with the appropriate dimensions are indicated. By doing TLM measurements of emitter, base and collector layers, the respective contact and sheet resistances can be extracted. In addition, using the layer thicknesses, the device capacitances can be estimated (assuming dielectric constant of 8). Figure 9.3 summarizes all the device parameters that are required for calculating the frequency performance. Some of these parameters like the velocity of hot electrons in the base is assumed from theoretical calculations found in literature.

Dimensions			
L _E	2 µm		
L _{Bacc}	1 µm	Resistance	
L _{Bc}	5 µm		
		R _{Bc}	1445 Ω.µm
L _{Bm}	1 µm	R _{Bsh}	3551 Ω/sq
L _{Cacc}	1 µm	R _{Ec}	8370 Ω.µm²
t _B	4 nm	R _{Evert}	635 Ω.µm²
t _C	100 nm	R _{Cc}	140 Ω.µm
W	100 µm	R _{Csh}	27 Ω/sq

		Others	
Capacitance		V _B	8x10 ⁷ cm/s
C _{BE}	35.4 fF/µm ²	v _c	1x10 ⁷ cm/s
C _{BC}	0.71 fF/µm ²	J _C	10 μA/μm²

Figure 9.3 Device parameters of the III-N HET

<u>Appendix B</u>

The current density is assumed to be $1kA/cm^2$ (or $10 \ \mu A/\mu m^2$). Using the parameters in Figure
9.3, the device delays can be extracted.

Parameter	Value)	Delay	Value		Percentage
			т _в	0.005	ps	0.003
			т _с	0.5	ps	0.3
C _{BE}	7080	fF				
C _{BC}	1132	fF	RC ₁	106	ps	66.5
I _C	2	mA				
R _E	45	Ω	PC	52	2	22.4
R _C	1.9	Ω	RC ₂	53	ps	33.1
			Total	160.4	ps	

f _T	0.99 GHz
f _{MAX}	0.9 GHz

Figure 9.4 Device delays and estimation of high-frequency figures of merit for the III-N HET

The calculated device delays show that RC_1 is the dominant delay and RC_2 is the second largest. The resulting f_T is ~ 1GHz. The f_{MAX} in reality is expected to be lower than the calculated value as the effect of degradation of R_{Bsh} due to emitter bias in the active device region has not been taken into account. In order to achieve a f_T of 500GHz, the total device delays need to be ~ 0.32ps. Since the device structure at present is not optimized at all for high frequency, the total delay is orders of magnitude larger. To improve this, several changes (as discussed in Chapter 6) are required. The goal of this appendix is to estimate the effect of these changes on the high-frequency performance.

<u>Appendix B</u>

Next step is to implement a scaled device structure with high emitter doping and regrown base contacts. In addition, modulation doping for high base charge is added to reduce the effect of R_{Bsh} degradation under bias. In order to model this effect, it is assumed that R_{Bsh} increases by 50% under the active device area under normal bias conditions. While this is not the most accurate way of modelling the device behavior, it captures some of the physics and is good enough for rough estimates.

Dimensions					
L _E	0.5	μm			
L _{Bacc}	0.05	μm	Resistance		
L _{Bc}	0.5	μm		200	Qum
L _{Bm}	0.05	μm	R _{Bc}		Ω.µm
L _{Cacc}	0.05	μm	R _{Bsh}) Ω/sq
		P	R _{Ec}	500	Ω.µm²
t _B	4	nm	R _{Evert}	10	$\Omega.\mu m^2$
t _C	100	nm	R _{Cc}	140	Ω.µm
W	2	μm	R _{Csh}	27	Ω/sq

		Others	
Capacitance		V _B	8x10 ⁷ cm/s
C _{BE}	35.4 fF/µm ²	v _c	1x10 ⁷ cm/s
C _{BC}	0.71 fF/µm ²	J _C	50 μΑ/μm²

Figure 9.5 Device parameters of the III-N HET with scaled structure, high emitter doping, regrown base

contacts, and modulation doped base

Parameter	Value		Delay	Value		Percentage	
			Т _В	0.005 ps		0.02	
			т _с	0.5	ps	2.3	
C _{BE}	35.4	fF		19.6	ps	91.4	
C _{BC}	2.4	fF	RC ₁				
I _C	0.05	mA					
R _E	510	Ω	DC	1.33	ps	6.2	
R _C	41	Ω	RC ₂				
			Total	21.5	ps		

f_T 7.4 GHz f_{MAX} 21.6 GHz

Figure 9.6 Device delays and estimation of high-frequency figures of merit for the III-N HET

As indicated in Figure 9.6, with scaling and higher doping, the RC₂ component of delay is drastically reduced. RC₁ is lower mainly because of the higher current density used for this structure (~ $5kA/cm^2$). Base resistance doesn't directly affect f_T but can degrade current density by lateral resistive voltage drops. The higher current density assumed here is to take into account the reduction in base resistance. Theoretically, the maximum current density achievable using this structure is ~ $10kA/cm^2$. The reduction in base resistance by regrown contacts, modulation doping, and lateral scaling translates to a huge improvement in the device f_{MAX} . This shows the importance of modulation doping for reduction in base resistance.

As parasitic resistances are reduced, the dominant delay quickly becomes RC_1 due to the low current density in the device. Chapter 6 suggested the use of resonant tunneling to improve the current density to > 500kA/cm².

Parameter	Value		Delay	Value		Percentage	
			т _в	0.005	5 ps	0.2	
			т _с	0.5	ps	24.6	
C _{BE}	35.4	fF		0.19	ps	9.7	
C _{BC}	2.4	fF	RC ₁				
I _C	0.05	mA					
R _E	510	Ω		1.33	ps	65.4	
R _C	41	Ω	RC ₂				
			Total	2.03	ps		

f _T	78.4 GHz
f _{MAX}	70 GHz

Figure 9.7 Device delays and estimation of high-frequency figures of merit for the III-N HET

Figure 9.7 shows that RC_1 drops by 2 orders of magnitude as the current density is increased by the same factor. This quickly makes RC_2 and τ_C the dominant device delays. With appropriate lateral scaling and reduction in parasitic resistances, RC_2 can also be made smaller than τ_C .

To summarize, this section showed that the total delay for the present III-N HET is ~ 160ps. Total delay < 1ps is required for very high-frequency operation. In order to improve f_T and f_{MAX} , the key requirements are,

APPENDIX B

- Self-aligned process for small parasitic resistances and capacitances
- High emitter doping
- Regrown base contacts
- Lateral scaling to improve f_T and f_{MAX} together
- Modulation doped base for good f_{MAX}
- High current density enabled by resonant tunneling or heterojunction injection

Most of these requirements can be satisfied by process and growth optimizations. While these optimizations are not trivial, they do not pose any fundamental challenges. The steps which are absolutely necessary are the modulation doped base and high current density emitter. Without these steps, the device will have fundamental limits on high-frequency performance. Chapter 6 has already discussed some ideas to achieve these steps. With these changes, it is possible to push the III-N HET to its high-frequency performance limits.