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III-V Multigate Non-Planar Channel Transistor

Simulations and Technologies

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Electrical Engineering

by

Kun-Huan Shih

2012

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ABSTRACT OF THE DISSERTATION

III-V Multigate Non-Planar Channel Transistor Simulations and Technologies

By

Kun-Huan Shih

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles. 2012

Professor Chi On Chui, Chair

As the relentless scaling of conventional Si CMOS transistors continues, it becomes more and more challenging to further increase device drive current and reduce leakage current and power consumption. III-V multigate non-planar channel transistors have emerged as a promising contender in the post-Si era due to its high carrier mobility and superior electrostatic control of the non-planar structure. For device design, current Technology Computer Aided Design (TCAD) modeling, however, fails to accurately predict device behaviors in decananometer dimensions.

Further, for the analog/RF applications, parasitics engineering plays a determining role in an ultrathin body structure but the conventional symmetric source (S) / drain (D) architecture restricts design and optimization versatility. Moreover, for III-V transistors fabrication, the device-level co-integration capability is crucial but still not mature in current technology.

In this work, a systematic methodology is developed to calibrate TCAD hydrodynamic model against Monte Carlo (MC) simulation in the quasi-ballistic regime. Good fits of both I_{DS}-V_{GS} and I_{DS}-V_{DS} curves have been demonstrated at various device dimensions. This methodology facilitates an accurate and time-efficient device simulation. Secondly, we explore a GaAs accumulation mode vertical transistor for asymmetric S/D design and optimization. Separate control of S/D spacer thickness and underlap length can be implemented and their individual impact on analog performance is discussed. Device design guidelines for different analog/RF metrics improvement are presented. Thirdly, we develop a VLSI-compatible top down process with co-integration capability in III-V multigate non-planar channel transistor fabrication. Nanowires are patterned by photolithography and etching of a source substrate and transferred to another receiving substrate by transfer stamping. A VLSI cleanroom tool is used in the transfer process to accurately position nanowires. This technique yields large arrays of aligned GaAs nanowires, and facilitates device-level co-integration of III-V multigate non-planar channel transistors on the same substrate with close proximity and overlay accuracy.

The dissertation of Kun-Huan Shih is approved.

M.-C. Frank Chang

Oscar Stafsudd

Suneel Kodambaka

Chi On Chui, Committee Chair

University of California, Los Angeles

2012

This dissertation is dedicated to

my family

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List of Symbols

α_2	Gate control indicator
C_D	Depletion capacitance
C_{GD}	Gate to drain capacitance
$C_{GD,\text{int}}$	Intrinsic gate to drain capacitance
$C_{GD,para}$	Parasitic gate to drain capacitance
C_{GG}	Total gate capacitance
$C_{GG,\text{int}}$	Intrinsic gate capacitance
$C_{GG,para}$	Parasitic gate capacitance
C_{GS}	Gate to source capacitance
C_{it}	Interface capacitance
C_Q	Graphene quantum capacitance
$C_Q{}'$	Effective graphene capacitance
C_{ox}	Oxide capacitance
C_{tot}	Measured total capacitance
C_{tr}	Trap charges capacitance in graphene
D	Damping factor in Lombardi model

D_n	Electron diffusivity
$D_{T,n}$	Electron thermal diffusivity
$D_{T,p}$	Hole thermal diffusivity
E_C	Conduction band energy
ε	Dielectric constant
f_n^{hf}	Heat flux coefficient
$f_{\max}$	Maximum oscillation frequency
f_T	Cutoff frequency
Φ_n	Electron quasi-Fermi level
Φ_p	Hole quasi-Fermi level
g_d	Drain conductance
$g_{d,\text{int}}$	Intrinsic drain conductance
g_m	Transconductance
$g_{m,\text{int}}$	Intrinsic transconductance
$g_{m,\max}$	Maximum transconductance
I_{DS}	Drain current
$I_{DS,sat}$	Drain saturation current
λ_0	Near-equilibrium mean-free-path for backscattering

λ_2	Neutral length
J	Current density
l_{crit}	Critical length in Lombardi model
κ	Dielectric constant
κ_T	Thermal conductivity
l	Critical length for backscattering under high drain bias
L_{ch}	Channel length
L_T	Transfer length
m_n	Electron effective mass
m_p	Hole effective mass
n	Electron density
n^*	Charged impurities density
n_G	Electron density caused by the gate potential
Q	Charge
Q_0	Charge at the virtual source
Q_{heat}	Heat flux
R_c	Contact resistance
$R_{c\text{-tot}}$	Total contact resistance

R_D	Drain parasitic resistance
R_{net}	Net recombination rate
R_{out}	Output resistance
R_S	Source parasitic resistance
R_s	Sheet resistance
r_n	Energy flux coefficient
r_{sat}	Channel backscattering coefficient in the saturation region
ρ_c	Specific contact resistivity
$\rho_{c\text{-edge}}$	Specific contact resistivity of an edge contact
$\rho_{c\text{-plane}}$	Specific contact resistivity of an out-of-plane contact
S_n	Electron energy flux
SS	Subthreshold swing
s	Probability of specular scattering at the channel/dielectric interface
τ_E	Energy relaxation time
τ_m	Momentum relaxation time
τ_n	Electron energy relaxation time
μ_{ac}	Mobility due to surface acoustic phonon scattering
μ_{sr}	Mobility due to surface roughness scattering

$\mu_{ballistic}$	Ballistic mobility
μ_n	Electron mobility
μ_0	Doping-dependent mobility
μ_p	Hole mobility
v	Carrier velocity
v_0	Velocity at the virtual source
v_c	Velocity from thermal component
v_d	Velocity from drift component
v_F	Fermi velocity
v_{sat}	Saturation velocity
v_{th}	Thermal velocity
V_{ch}	Surface potential
V_{DD}	Power supply voltage
V_{GT}	Gate overdrive
V_t	Threshold voltage
W	Semiconductor body thickness
W_n	Electron kinetic energy density
Z	Device width

List of Acronyms

ALD	Atomic layer deposition
AM	Accumulation mode
BEOL	Back end of line
BG	Back gate
BJT	Bipolar junction transistor
BTBT	Band to band tunneling
BTE	Boltzmann transport equation
CMOS	Complementary metal oxide semiconductor
CNT	Carbon nanotube
CT	Contact
D	Drain
DD	Drift diffusion
DG	Double gate
DIBL	Drain-induced barrier lowering
DS	Drain-side spacer
DU	Drain-side underlap

FET	Field-effect-transistor
GIDL	Gate-induced drain leakage
HD	Hydrodynamic
HEMT	High electron mobility transistor
JL	Junctionless
LPCVD	Low pressure chemical vapor deposition
M1	Metal1
MC	Monte Carlo
M/G	Metal-to-graphene
MOG	Metal-oxide-graphene
MESFET	Metal-semiconductor field-effect-transistor
MLG	Multilayer graphene
MOSFET	Metal-oxide-semiconductor field-effect-transistor
NW	Nanowire
PBT	Permeable base transistor
PDMS	Polydimethylsiloxane
PMD	Pre-metal dielectric
RCS	Remote coulomb scattering

RPS	Remote phonon scattering
RTA	Rapid thermal anneal
S	Source
SCE	Short channel effect
SLG	Single-layer graphene
SOI	Silicon-on-insulator
SS	Source-side spacer
SU	Source-side underlap
TCAD	Technology Computer Aided Design
TLM	Transmission line model
TMA	Trimethylaluminium
VLS	Vapor-liquid-solid
VRG	Vertical replacement gate

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PUBLICATION

- K.-H. Shih and C. O. Chui, “Analog/RF Performance and Optimization of Vertical III-V Double Gate Transistor,” *submitted to IEEE Trans. Electron Dev.,* 2012.
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Chapter 1
Introduction

1.1 Scaling Limitations of Conventional Si MOSFETs

Si complementary Metal-Oxide-Semiconductor (CMOS) transistors have been aggressively scaled over the past fifty years for continuous pursuit of higher switching speed and a larger density of devices on a chip [1]. On-state drive current, off-state leakage current and power consumption, etc. are critical device parameters for circuit applications, and there normally involves a trade-off among these metrics in device design and optimization [2]-[4]. As the relentless scaling continues, it becomes more and more challenging to further increase device drive current and reduce leakage current and power consumption.

In conventional planar Si transistors, high substrate doping is required to effectively suppress short channel effect (SCE) and maintain adequate electrostatic control. High doping, however, reduces carrier mobility due to Coulombic scattering. Although mobility is not a well-defined quantity in a deeply-scaled devices where velocity overshoot and quasi-ballistic transport may dominate under high drain bias, it is proved that the saturated region drive current

is related to low-field mobility [5]-[7]. The reason is as follows. The saturation current is given by

$$I_{DS,sat} = ZC_{ox}v_{th}(\frac{1-r_{sat}}{1+r_{sat}})(V_{GS}-V_t) \quad (1)$$

where Z is device width; C_{ox} is oxide capacitance; v_{th} is thermal velocity; V_t is threshold voltage and r_{sat} is the channel backscattering coefficient in the saturation region. r_{sat} can be expressed as [7]

$$r_{sat} = \frac{l}{l+\lambda_0} \quad (2)$$

where λ_0 is the near-equilibrium mean-free-path for backscattering, and l a critical length for backscattering under high drain bias. High low-field carrier mobility yields a larger mean-free-path (λ_0) and therefore reduces the backscattering from the channel back to the source. Consequently, saturation current can be improved by higher low-field carrier mobility.

On the other hand, reducing device leakage current and power consumption are paramount in nowadays ultra-low power nanoelectronics applications. The overall device leakage comprises the following main components.

(1) Subthreshold leakage: At gate voltages below the threshold voltage, no inversion charge is formed at the device surface so drift current conduction is zero. Carriers from the source, however, are able to diffuse through the channel and reach the drain. The conduction mechanism is similar to that in a bipolar junction transistor (BJT), and the

leakage current is called subthreshold leakage. Subthreshold swing (*SS*) is a metric indicating the sharpness of the on-off switching of a device and is given by

$$SS = 2.3\frac{kT}{q}(1+\frac{C_D + C_{it}}{C_{ox}}) \quad (3)$$

where C_D and C_{it} represent depletion capacitance and interface capacitance, respectively. Increasing doping in conventional Si MOSFETs increases C_D and therefore degrades *SS*. Off-state leakage current and standby power consumption are both increased due to a worse *SS* for a given threshold voltage of the device. A larger threshold voltage can be used to effectively suppress leakage current and standby power consumption but degrades drive current as well since the gate overdrive (V_{GT} = V_{DD}-V_t, where V_{DD} is power supply voltage) is reduced. Increasing V_{DD} enhances the gate overdrive but increases the dynamic (switching) power consumption of CMOS circuits.

$$P_D = CV_{DD}^2 f \quad (4)$$

where *C* is the capacitance between the output node and the ground; *f* is the frequency.

(2) Junction leakage: Junction leakage exists in a reverse-biased PN junction. If substrate doping is high, (e.g., heavily doped halo implant and n^+ drain), band-to-band tunneling (BTBT) increases rapidly and dominates the PN junction leakage current [8]-[9] under high drain bias.

(3) Gate-induced drain leakage (GIDL): GIDL occurs at off-state when gate voltage (V_{GS}) is zero and drain voltage (V_{DS}) is at high bias. Under this circumstance, a high electric field exists between the gate and drain because of the ultrathin gate dielectric and field crowding [10]-[11] and depletes the heavily doped n^+ drain. Carriers are generated in the depletion region by avalanche processes and constitute the drain leakage current. Higher substrate doping enhances the field crowding so GIDL is increased [10].

(4) Gate tunneling leakage: As the gate dielectric thickness is aggressively scaled down, electron tunneling current through an ultrathin gate dielectric (by Fowler-Nordheim tunneling [12] or direct tunneling [13]) becomes enormously large. In advanced transistors, high-κ material has replaced silicon dioxide as a gate dielectric to effectively suppress the gate leakage current.

As mentioned, higher doping to suppress SCE in conventional Si MOSFETs reduces on-current, and increases subthreshold leakage, junction leakage and GIDL. Further, ultra-shallow junction is normally implemented in conventional Si MOSFETs to suppress SCE as well. The resultant high source (S) / drain (D) parasitic series resistance, however, degrades the drive current. Consequently, these scaling limitations and trade-offs among V_{GT}, drive current, leakage current and power consumption renders conventional planar Si CMOS transistors questionable in fulfilling the device requirements in the coming generations.

In order to solve these fundamental issues and extend “Moore’s Law”, alternative materials and novel transistor structures may need to be employed. For example, advanced high mobility channel materials, such as strained Si, SiGe, Ge and III-V, have been extensively explored for the past two decades to improve device drive current and overall performance [14]-[18]. Also, ultrathin body or multigate non-planar structures are proposed to suppress SCE and improve leakage current and power consumption, thanks to the excellent electrostatic control offered by the geometry [19]-[21]. Channel doping is therefore lowered and carrier mobility is improved correspondingly. These material/structure innovations to improve device performance and power consumption are illustrated in Fig. 1.1. As now of year 2012, tri-gate Si FinFET structure has been commercialized by Intel in the 22 nm technology node. Non-planar III-V MOSFET has been under active development by many research groups [22]-[24].

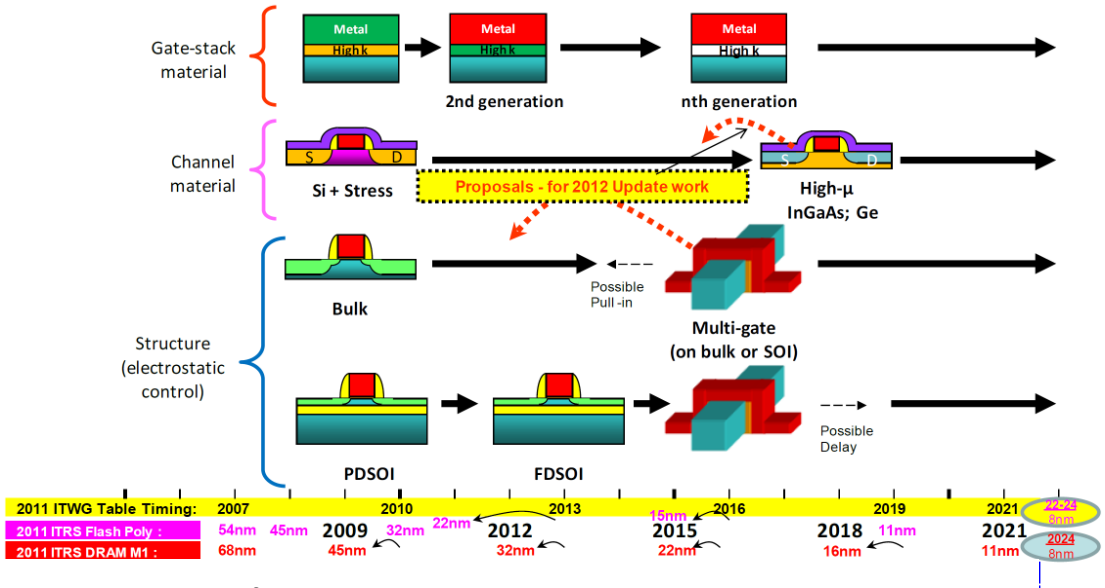


Figure 1.1 Simplified transistor roadmap illustrating the material and structure innovations to improve device performance and power consumption [1].

Based on the technological trend mentioned above, III-V multigate non-planar channel transistors have emerged as a promising contender in the post-Si era due to its high carrier mobility and superior electrostatic control of the non-planar structure. In the present work, we conduct III-V multigate non-planar channel transistor research in the following aspects: Technology Computer Aided Design (TCAD) simulation modeling, analog/RF performance optimization, and experimental fabrication technique.

1.2 Demand for III-V Multigate Non-Planar Channel Transistor Research

Some of the main challenges of the III-V multigate non-planar channel transistor lie in the lack of an accurate and time-efficient TCAD modeling of the device, parasitics engineering and optimization, and fabrication technology with device-level co-integration capability. This section outlines these challenges.

1.2.1 Accurate and Time-Efficient TCAD Modeling

Device simulation has been used to study device behaviors for decades. An accurate device simulation not only helps understand the physics behind but also reduce time and cost of conducting experimental studies.

To “unveil” device behaviors, equations regarding both electrostatics and carrier transport need to be solved in a simulator. Poisson equation is the most fundamental equation describing the electrostatics in a semiconductor. It is expressed as

$$\nabla \cdot \varepsilon \nabla V = -(p - n + N_D^+ - N_A^-) \tag{5}$$

Correspondingly, Boltzmann transport equation (BTE) is the most fundamental equation governing the carrier transport in the semi-classical domain. It is given by

$$\frac{df}{dt} = -\vec{v} \cdot \nabla_{\vec{r}} f - \vec{F} \cdot \nabla_{\vec{k}} f + \frac{\partial f}{\partial t}\Big|_{coll} + R(\vec{r}, \vec{k}, t) \tag{6}$$

where f is the carrier distribution function, depending on the position ($\vec{r}$), momentum ($\vec{k}$) and time (t); $\vec{v}$ is velocity; $\vec{F}$ is force; $\partial f / \partial t\big|_{coll}$ is the rate of change due to carrier collision (scattering); $R(\vec{r}, \vec{k}, t)$ is the particle generation/recombination rate. Once the distribution function is solved, various physical quantities can be obtained, such that

$$n(\vec{r}, t) = \frac{1}{V} \sum_k f(\vec{r}, \vec{k}, t), \text{ carrier density} \tag{7}$$

$$\vec{J}(\vec{r}, t) = -\frac{q}{V} \sum_k \vec{v}(\vec{k}) f(\vec{r}, \vec{k}, t), \text{ current density} \tag{8}$$

$$W_n(\vec{r}, t) = \frac{1}{V} \sum_k E(\vec{k}) f(\vec{r}, \vec{k}, t), \text{ energy density} \tag{9}$$

The calculation of the distribution function, $f(\vec{r}, \vec{k}, t)$, is not trivial. The most direct and accurate solution to the BTE is based on Monte Carlo (MC) method [25]-[26]. It involves the simulation of particle trajectories rather than the direct solutions of partial differential equations [27]. Its formidable computational cost, however, greatly limits its practical applications for

device design.

Other than MC method, solving the BTE directly is difficult. Several useful balance equations, however, can be derived by weighing different moments to the BTE [27]-[28]. For example, carrier density balance equation can be derived as

$$\nabla \cdot \vec{J}_n = qR_{net} + q\frac{\partial n}{\partial t} \tag{10}$$

where R_{net} is the net recombination rate. Carrier density balance equation is exactly the Continuity equation, which describes charge conservation. Momentum balance equation can be derived by weighing momentum to the BTE and given by

$$\frac{\partial \vec{J}_n}{\partial t} = \frac{-2(-q)\nabla \cdot \overleftrightarrow{W}_n}{m^*} + \frac{q^2 nE}{m^*} - \frac{\vec{J}_n}{\tau_m} \tag{11}$$

where $\overleftrightarrow{W}_n$ is tensor of the kinetic energy density; τ_m is the momentum relaxation time. Similarly, energy balance equation can be derived by weighing energy to the BTE and given by

$$\frac{\partial W}{\partial t} + \nabla \cdot \vec{S}_n = \vec{J}_n \cdot \nabla E_C - \frac{W_n - W_0}{\tau_E} \tag{12}$$

where S_n is energy flux; τ_E is the energy relaxation time.

The carrier density balance equation introduces the variable of current density (Eq. (10)); the momentum balance equation introduces kinetic energy density (Eq. (11)) and energy balance equation introduces energy flux (Eq. (12)). Therefore, a new unknown variable exists in the hierarchy of balance equations and the solution to this infinite set of balance equations is actually

the solution to the BTE itself [27]-[28].

Hence, it is necessary to truncate this infinite iteration and make some simplifying assumptions to the balance equations in order to obtain a closed form of equation. For instance, one applies relaxation time approximation in the momentum balance equation and assumes the carriers and lattices are in thermal equilibrium and the electric field gradient is small. With all these assumptions, momentum balance equation can be simplified to the well-known drift-diffusion (DD) equations,

$$\overrightarrow{J_n} = nq\mu_n E + qD_n \nabla n = -nq\mu_n \nabla \Phi_n \tag{13}$$

$$\overrightarrow{J_p} = pq\mu_p E - qD_p \nabla p = -pq\mu_p \nabla \Phi_p \tag{14}$$

where Φ_n and Φ_p are electron and hole quasi-Fermi potentials, respectively.

In the presence of strong electric field, electrons gain energy from the field and the temperature of electrons are raised such that electrons may not be in thermal equilibrium with the surrounding semiconductor lattices. Under these circumstances, hydrodynamic (HD) model adopts an additional driving force, namely, the temperature gradient, in the current equation to describe the non-equilibrium electron temperature effect. Current can therefore be written as [27]

$$\overrightarrow{J_n} = nq\mu_n E + qD_n \nabla n + qD_{T,n} \nabla T_n \tag{15}$$

$$\overrightarrow{J_p} = pq\mu_p E - qD_p \nabla p - qD_{T,p} \nabla T_p \tag{16}$$

where $D_{T,n}$ and $D_{T,p}$ are the electron and hole thermal diffusivity, respectively.

In Synopsys™ Sentaurus Device tool, considering Fermi statistics and spatial variation of carrier effective mass, the complete current equation in HD model is expressed as [29]

$$\overrightarrow{J_n} = q\mu_n (n\nabla E_C + kT_n \nabla n + \lambda_n f_n^{td} kn\nabla T_n - nkT_n \nabla \ln \gamma_n - 1.5nkT_n \nabla \ln m_n) \quad (17)$$

$$\overrightarrow{J_p} = q\mu_p (p\nabla E_V - kT_p \nabla p - \lambda_p f_p^{td} kp\nabla T_p + pkT_p \nabla \ln \gamma_p - 1.5pkT_p \nabla \ln m_p) \quad (18)$$

where $\lambda_n = F_{1/2}(\eta_n)/F_{-1/2}(\eta_n)$, $\eta_n = \dfrac{E_{F,n} - E_C}{kT}$ (19)

$$\gamma_n = \frac{n}{N_C}\exp(-\eta_n) \quad (20)$$

$F_{1/2}$ is Fermi integral of order ½. For Boltzmann statistics ($\gamma_n = \gamma_p = \lambda_n = \lambda_p = 1$) and in the absence of spatial variation of effective mass m_n and m_p, Eq. (17) reduces to Eq. (15) and Eq. (18) reduces to Eq. (16). More details about HD model will be discussed in Chapter 2.

In TCAD, macroscopic models, such as DD or HD models, are solved to predict device behaviors rather than directly solving the BTE, as MC method does [29]. As devices size is scaled to decananometer regime, DD and HD models fail to predict device characteristics in such a small dimension. A model calibration is thus needed to yield an accurate and time-efficient TCAD modeling. In this research work, we develop a systematic approach to calibrate HD model against MC simulation for different device dimensions. The details of the HD model and the model calibration methodology will be discussed in Chapter 2.

1.2.2 Parasitics Optimization

Parasitics engineering plays a determining role in the analog/RF performance, especially in an ultrathin body structure. To minimize any resultant performance degradation, the S/D structure designs need to be carefully optimized. Reducing S/D overlap (or increasing underlap) length reduces parasitic capacitance but inevitably increases parasitic resistance, and vice versa. Some research groups have discussed device design for analog/RF optimization in ultrathin body FinFETs or Si/III-V nanowire (NW) FETs. Sohn *et al.* discussed the FinFET design in terms of fin height and fin space through the geometry-dependent capacitive and resistive parasitics optimization [30]. Zhuge *et al.* discussed the impact of the parasitic capacitance and resistance at different Si NW diameters and gate height, and the optimization of NW transistors through different S/D extension doping profiles [31]. Jansson *et al.* discussed the performance evaluation and optimization of III-V NW transistors in terms of spacer thickness, NW array size and array aspect ratio [32]. All of these analyses are based on the symmetric S/D architecture that has limited optimization flexibility. An asymmetric S/D architecture, on the other hand, offers more design versatility and has not been extensively examined before. The parasitics optimization of an asymmetric S/D structure will be discussed in Chapter 3.

1.2.3 Accumulation Mode / Junctionless Device Structure

In recent years, accumulation mode (AM) / junctionless (JL) MOSFETs have been

proposed as an alternative structure to eliminate the difficulty of fabricating an ultrashallow junction in conventional Si MOSFETs [33]-[36]. A conventional ultrashallow junction involves an abrupt doping transition from heavily doped n^+ region (e.g., 10^{19} cm^{-3} source/drain extension) to heavily doped p region (e.g., 10^{18} cm^{-3} halo implant) within couples of nanometers range. A millisecond laser pulse annealing is typically required to minimize dopant diffusion. The degree of dopant activation, precise dopant profile control, and junction abruptness, etc. become more and more difficult as aggressive device scaling continues.

On the other hand, AM/JL devices have the same carrier type in the channel and S/D regions. In JL devices, the channel doping is raised to the same as S/D doping and there exists no junction. Hence, all technological challenges regarding forming an ultrashallow junction formation are completely eliminated. The semiconductor doping is typically high in AM/JL devices in order to achieve high on-current. Also, a thin semiconductor body is required for a full depletion of carriers in the body to turn off the device. By implementing ultrathin body structure, nowadays AM/JL devices yield comparable or even better performance compared with conventional inversion-mode devices [33]-[36].

In brief, due to the simplified fabrication process and promising electrical characteristics, ultrathin body AM/JL devices have aroused widespread attention as one of the potential candidates in the future generations. Therefore, in this work, we explore a III-V accumulation

mode multigate non-planar channel transistor from device modeling, parasitics engineering to fabrication technology.

1.2.4 III-V Transistors Fabrication Technology with Co-Integration Capability

For ultrathin body transistors fabrication, two approaches are commonly used: bottom-up and top-down. In the first method, semiconductor NWs are synthesized elsewhere by, for example, vapor-liquid-solid (VLS) technique, in which a metal nanodroplet (L) preferentially gathers and decomposes the growth precursors (V), allowing them to precipitate in the form of nanowires (S) [37]-[39]. The most commonly used metal catalyst is gold. It functions for the VLS of many materials systems, from group IV and III–V semiconductors to oxides [40]-[42]. The grown NWs are then harvested and transferred to a target substrate. The major limitation is that the transferred NWs are randomly distributed, which greatly limits this technique to be used in large-scaled applications. Alternatively, top-down method utilizes nanolithography-based patterning of semiconductor material and anisotropic etching to create periodic NW arrays [43]. It enables precise control of NW location and orientation and ultra large-scaled integration of nanoelectronic devices.

Further, for III-V transistor fabrication, the co-integration capability with Si on the same substrate is crucial but is still not mature in current technology. The current co-integration

techniques include bonding (wafer-to-wafer and die-to-die bonding [44]-[47]) and monolithic epitaxial growth [48]-[50]. Wafer-to-wafer and die-to-die bonding suffer misalignment and low throughout issues, while growing high-quality epitaxial layers on Si is challenging. In this research work, we develop a VLSI-compatible top-down method to fabricate III-V multigate non-planar channel transistors. NWs are patterned on a source wafer by photolithography and etching and then picked up by a polydimethylsiloxane (PDMS) stamp and transferred to another target substrate. A VLSI cleanroom tool is used in the transfer process to accurately position NWs. This technique facilitates device-level co-integration of III-V multigate non-planar channel transistors on the same substrate with close proximity and overlay accuracy. The details of the experiment will be discussed in Chapter 4.

1.3 Thesis Outline

The thesis is composed of five chapters. Chapter 2 discusses the calibration of hydrodynamic model in TCAD against Monte Carlo simulation in the quasi-ballistic regime. A systematic approach is proposed and the methodology has been applied to two material systems: a GaAs accumulation mode MOSFET and a Ge inversion mode MOSFET. Other physical effects,

such as surface roughness scattering, quantization model, etc., are discussed and can be further included in our methodology.

Chapter 3 addresses the analog/RF performance optimization of a vertical III-V double gate transistor. First of all, we assume vertical replacement gate (VRG) process for a vertical transistor fabrication. Parasitics engineering of a vertical transistor is then discussed. Through separate control of source/drain spacer and underlap, optimization of different analog/RF metrics is analyzed in an asymmetric source/drain vertical device.

In chapter 4, we introduce the process development of both lateral and vertical III-V multigate non-planar channel transistors. For lateral devices, experimental design, such as processing flow design, GaAs source epitaxial layer design, E-beam lithography pattern design, and nanowire stamping transfer and positioning technique is presented. In addition, device fabrication and electrical characteristics of the transistor are discussed. For vertical devices, we discuss the incorporation of graphene as the gate electrode in the transistor. Two critical components, graphene-high-κ interface and graphene-metal contact, are explored. The graphene-high-κ interface is characterized by a graphene capacitor. Further, a novel contact scheme based on the VLSI-compatible contact configuration is proposed to reduce graphene gate/metal contact resistance.

Chapter 5 concludes the thesis and summarizes the contribution of this work. Future

research investigation in some areas is recommended.

Chapter 2
Hydrodynamic Model Calibration in the Quasi-Ballistic Regime

2.1 Introduction

With the relentless, aggressive advancement of semiconductor technology in the past decades, device dimensions have been scaled down to the decananometer regime. At such a short gate length, many physical effects, such as velocity overshoot and quasi-ballistic transport [1]-[4], play a dominant role in device characteristics. As a result, it is more challenging to predict device performance through computer simulations since these physical models for velocity overshoot and quasi-ballistic transport behaviors have to be incorporated and described precisely in a simulator.

An ensemble Monte Carlo (MC) simulation has been used to study device behavior for decades [5]-[9]. In this method, particles are repeatedly injected into the simulated device structure and their trajectories are traced statistically, yielding a good approximation to the average behavior of carriers in a real device [10]-[11]. A typical output of MC simulation is

illustrated in Fig. 2.1. The device is a GaAs accumulation mode MOSFET with 50 nm channel length and 30 nm body thickness. The band diagram is depicted and particles are visible inside the simulated structure with different colors representing different particle energy. MC simulation is capable of capturing velocity overshoot and quasi-ballistic transport by solving the Poisson and Boltzmann transport equations (BTE) self-consistently.

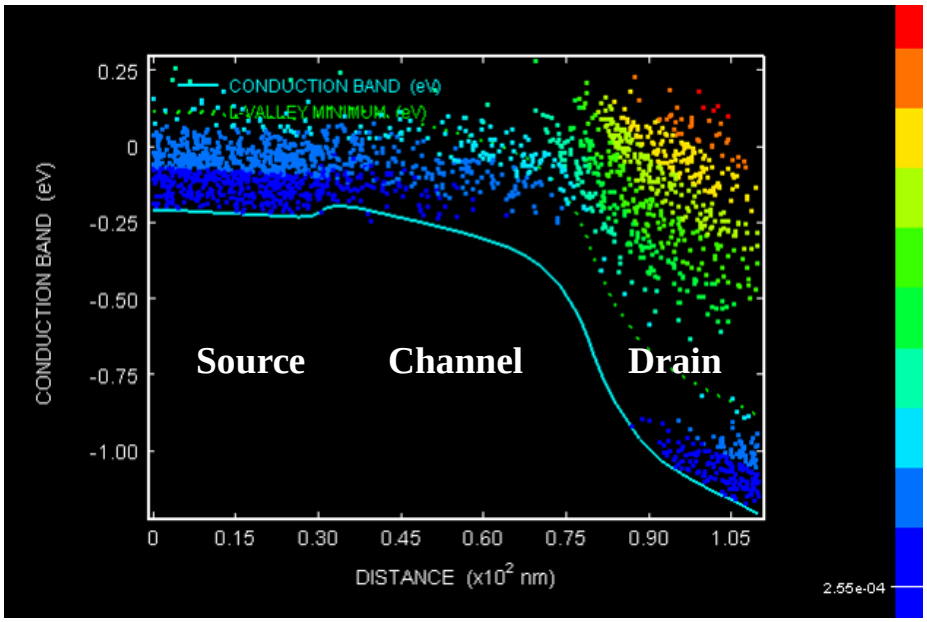


Figure 2.1 Typical MC output of with the band diagram depicted and particles visible inside the simulated structure. The device is a GaAs accumulation mode MOSFET with 50 nm channel length and 30 nm body thickness. Different colors represent different particle energy.

In the semi-classical domain, MC method is considered the most accurate simulation approach. The major limitation of this approach, however, is the enormous computational cost due to its repeated sampling nature. Consequently, MC simulation is not very practical for device

design application.

Alternatively, macroscopic transport models, like the drift-diffusion (DD) and hydrodynamic (HD) models, greatly reduce execution time by applying several simplifying assumptions to the BTE. DD model has been considered the simplest, “local” transport model by solving the linearized BTE under the relaxation time approximation and assuming small field and temperature gradients. (That is, the current at a particular point depends only on the instantaneous electric field and carrier concentration gradient at that point). It yields a good prediction of device performance in large dimensions (on the order of microns). As the dimension is scaled down, the electric field becomes stronger and varies dramatically in a device so carriers no longer remain in equilibrium with the lattice. Thus, DD model fails to correctly simulate the current because of its local transport assumption. To describe these non-stationary effects, HD model incorporates an additional driving force, carrier temperature gradient, in the current equation, and to some extent, captures the velocity overshoot behavior. It, however, cannot capture the “right” carrier distribution in quasi-ballistic regime, either. In other words, the physical accuracy of the macroscopic transport approaches (both DD and HD models) is not satisfactory in small dimensions [12].

A well-calibrated DD or HD model serves as a compromise between computational complexity and accuracy. So far, there has been lacking a clear, promising calibration approach.

Normally, only carrier profiles or a few $I_{D,sat}$ values were matched in prior works [12]-[16]. For example, Granzner *et al.* show the calibrated on-current values at different generations using HD simulations (Fig. 2.2) without showing *I*-*V* characteristics. Although a calibrated I_{DS}-V_{GS} curve has been published using DD or HD model by some groups, no successful I_{DS}-V_{DS} characteristics are reported [17]-[18]. For example, Nayfeh *et al.* demonstrate the calibrated I_{DS}-V_{GS} curve but fail to show the corresponding I_{DS}-V_{DS} curve (Fig. 2.3). Further, it is unknown whether the demonstrated calibrated parameters are extendable to other device dimensions, rendering predictive simulation highly questionable.

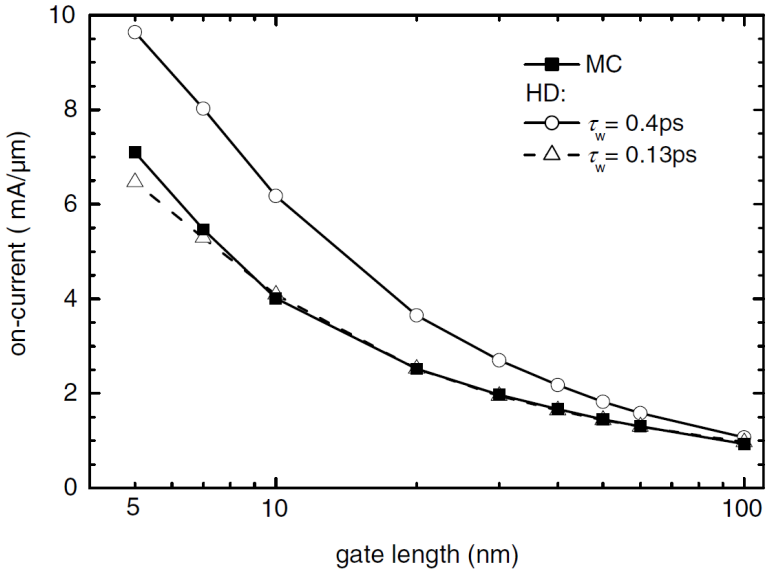


Figure 2.2 Simulated on-current of double-gate MOSFETs as a function of gate length. Open symbols – HD simulations (ATLAS) with modified energy relaxation time τ_w; full square: MC simulation [14].

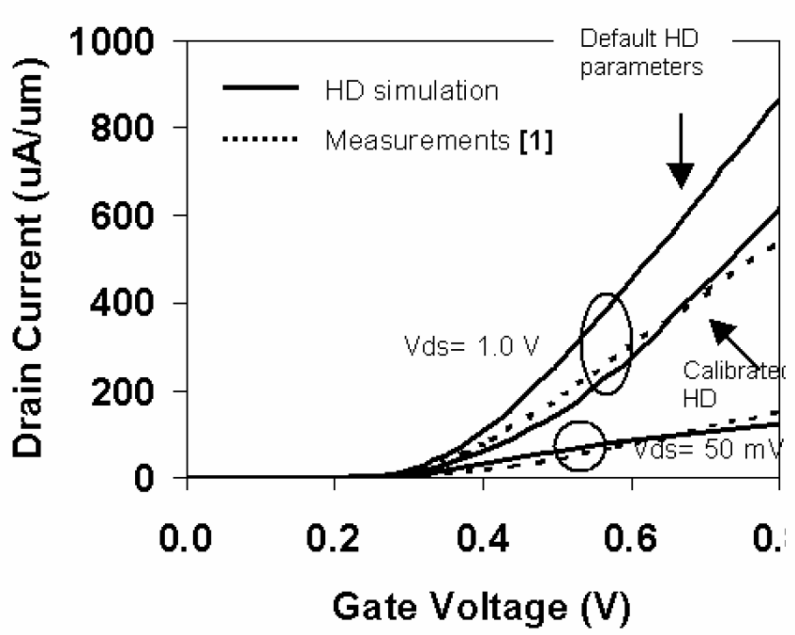


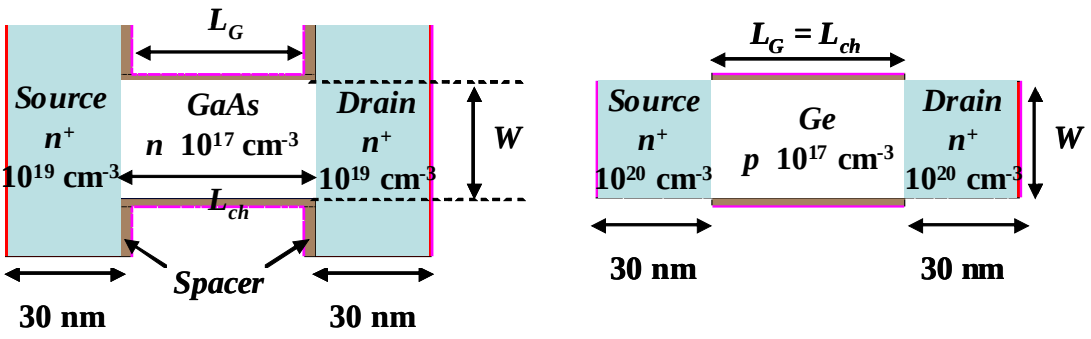
Figure 2.3 Drain current vs. gate voltage of a nanowire wire FET. Shown is the measured data, uncalibrated HD, and calibrated HD. A fit is achieved using energy relaxation time τ_n = 0.1 ps, and energy flux coefficient r_n = 0.3 [17].

This work provides a systematic methodology to calibrate HD model for accurate and time-efficient simulations. The calibration procedure is demonstrated on two different material systems as well as device structures (GaAs accumulation mode and Ge inversion mode MOSFET). Excellent I_{DS}-V_{GS} and I_{DS}-V_{DS} curves fittings are obtained. More importantly, our approach is extendable to other device dimensions (both channel length and body thickness), and its predictive capability is highly desirable in quasi-ballistic device design and optimization.

2.2 Hydrodynamic Model Calibration Procedure

2.2.1 Device Structure and Simulation Models

First of all, a double-gate accumulation mode GaAs MOSFET with flared-out source/drain is used as a vehicle to illustrate the calibration procedure as shown in Fig. 2.4(a). This structure represents a generic III-V *n*-type nanowire transistor, a highly promising potential contender in the post-Si era. The doping is *n*-type 1×10^{17} cm^{-3} and 1×10^{19} cm^{-3} in the channel and source/drain regions, respectively. The gate dielectric is 2 nm HfO_2; the sidewall spacer is 3 nm HfO_2. The channel length (L_{ch}, from n^+ source to n^+ drain) varies from 15 nm to 100 nm. The body thickness (W) varies from 18 nm to 30 nm. The second structure examined is a double-gate



(a) (b)

Figure 2.4 (a) Simulated double-gate GaAs accumulation-mode MOSFET, and (b) double-gate Ge inversion-mode MOSFET.

inversion mode Ge MOSFET, shown in Fig. 2.4(b). The doping is *p*-type 1×10^{17} cm^{-3} in the channel and *n*-type 1×10^{20} cm^{-3} in the source/drain regions. The gate dielectric is 2 nm HfO_2. The channel length (L_{ch}, from n^+ source to n^+ drain) varies from 15 nm to 50 nm. The body thickness (W) is 30 nm. The source/drain doping profile is abrupt in both devices.

Full-band DAMOCLES [19] and commercial Sentaurus^{TM} Device [20] were used for MC and HD simulations, respectively. For consistency, the Monte Carlo and hydrodynamic models used in this work are based on the same set of physics as follows. The device gate workfunction was 4.118 eV and 4.0 eV in the GaAs and Ge device, respectively. No generation or recombination was activated. No interface states were considered in this work. Phonon and ionized impurity scattering were included. Some effects, such as surface roughness, interface states, high-κ related scattering (remote phonon scattering (RPS), remote coulomb scattering (RCS), etc.), are not present in this work as they are experimentally-dependent and hence, there exist no universal quantitative parameters in MC modeling. For computational efficiency, quantum effects were not included as their impact should still be relatively small at the simulated body thicknesses (thicker than 10 nm) in this work. For an ultra-thin device with body film thinner than 10 nm, quantum effects may need to be considered [21]-[22]. The shift of *I-V* characteristics introduced by the quantum correction, however, should be marginal, especially at high drain biases [22]-[24].

In brief, we would like to emphasize that not including those effects does not essentially alter or nullify the theme of this work. The fitting strategy, in fact, can be extended in the presence of those effects if appropriate experimental data are available. That part will be discussed in Section 2.4.

2.2.2 Hydrodynamic Model

The GaAs device is addressed first for a detailed calibration flow demonstration, while the Ge device is demonstrated afterwards. First of all, the transfer characteristics (I_{DS} versus V_{GS}) of

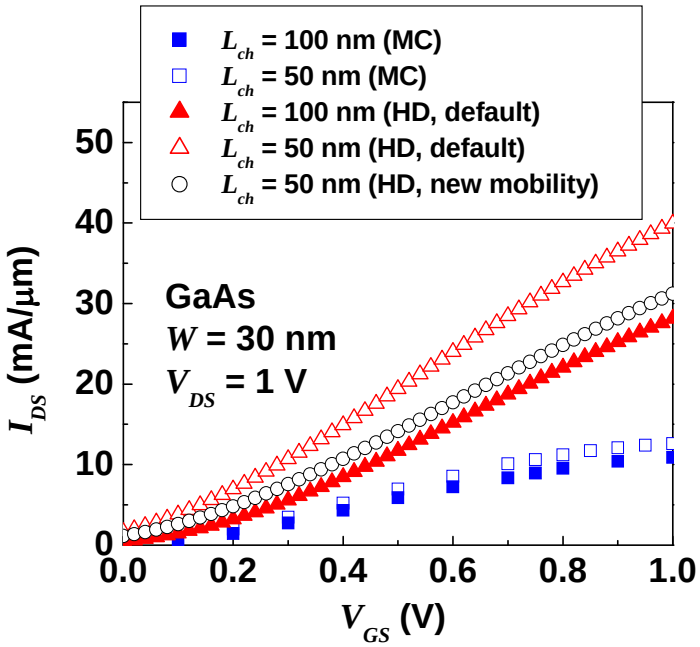


Figure 2.5 I_{DS}-V_{GS} of GaAs MC and standard HD models with 30 nm body thickness, 100 nm and 50 nm channel length. Also shown is HD model with new mobility values (μ_{ch} = 1380 cm^2/V-s, $\mu_{S/D}$ = 1500 cm^2/V-s) of 50 nm channel length.

GaAs MC and standard HD simulations are shown in Fig. 2.5 with 50 nm and 100 nm channel length (L_{ch}) at V_{DS} = 1 V. The body thickness is 30 nm. As is observed, HD greatly overestimates the current compared with MC results. Also, the discrepancy becomes larger as the device is scaled down. The non-calibrated HD model cannot correctly simulate the device behavior as it fails to capture the effect of a near-ballistic carrier distribution. A model calibration is thus needed.

The hydrodynamic model used in Sentaurus^{TM} Device is shown in Equation (1-3),

$$\frac{\partial W_n}{\partial t} + \nabla \cdot \vec{S}_n = \vec{J}_n \cdot \nabla E_C - \frac{W_n - W_{n,0}}{\tau_n} \tag{1}$$

$$\vec{S}_n = \frac{-5 r_n \lambda_n}{2} \left(\frac{kT_n}{q} \vec{J}_n + f_n^{hf} \frac{k^2}{q} n \mu_n T_n \nabla T_n \right)$$

$$= \frac{-5 r_n \lambda_n}{2} \frac{kT_n}{q} \vec{J}_n + Q_{heat} \tag{2}$$

$$Q_{heat} = \frac{-5 r_n \lambda_n}{2} f_n^{hf} \frac{k^2}{q} n \mu_n T_n \nabla T_n \tag{3}$$

where W_n is kinetic energy density; S_n is energy flux; Q_{heat} is heat flux; τ_n is energy relaxation time; r_n is energy flux coefficient; f_n^{hf} is heat flux coefficient; and E_C is conduction band energy. Here, heat flux Q_{heat} (Eq. (3)) is approximate form and it originates from the concept by the Fraz-Wiedermann law,

$$Q_{heat} = -\kappa_T \nabla T_n \tag{4}$$

where κ_T is thermal conductivity. This description of Q_{heat} truncates the infinite hierarchy issue, as mentioned in Chapter 1, and results in a closed set of equation.

Default values of τ_n, r_n, and f_n^{hf} are 1 ps, 0.6 and 1, respectively, for GaAs. The available parameters involved in our calibration methodology include low field mobility (μ_n), energy relaxation time (τ_n), energy flux coefficient (r_n), and heat flux coefficient (f_n^{hf}).

2.2.3 Methodology

Our procedure features a systematic approach to simplify the problem with τ_n as the only fitting parameter for GaAs. The flow chart of the entire procedure is shown in Fig. 2.6 and the detailed calibration procedure is explained as follows. The GaAs device is used as an example.

(i) Low field mobility selection

Nowadays, aggressively-scaled decananometer devices operate in the quasi-ballistic regime. Experimentally, however, the extracted mobility becomes smaller as the gate length is reduced. It seems counter-intuitive as carriers are expected to experience less scattering during the transport in the channel.

This result was explained by Shur [25] with an “artificial” ballistic mobility, which is dependent on the ballistic path distance (source to drain distance). Eqs. (5)-(7) show the apparent mobility (μ_n) incorporating doping-dependent mobility and ballistic mobility based on the

"Matthiessen rule", where μ_0 is doping-dependent mobility, L is ballistic length, v_{th} is thermal velocity, and m is carrier effective mass ($m = 0.067m_0$ for GaAs).

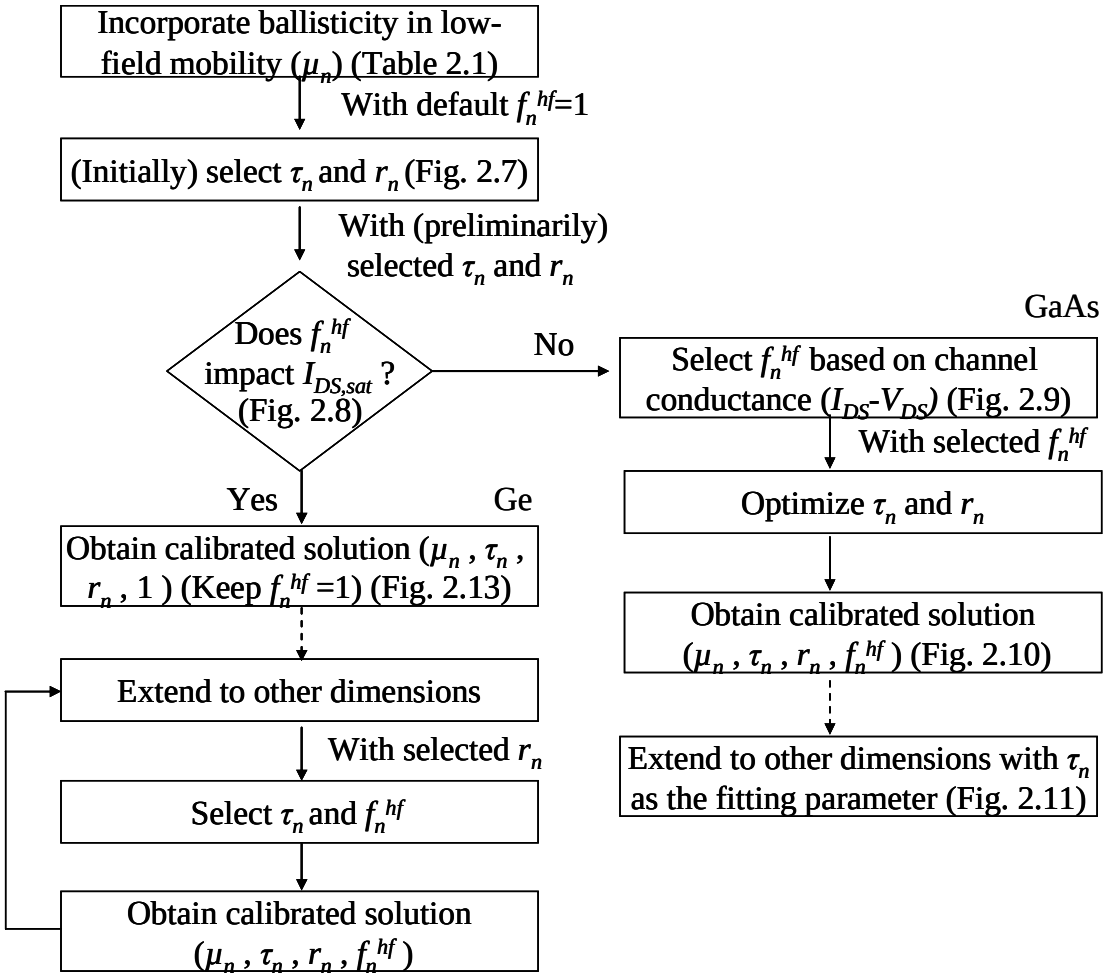


Figure 2.6 Flow chart of the calibration procedure. It features a systematic selection of μ_n, τ_n, r_n, and f_n^{hf}. In addition, the method is extendable to other device dimensions with τ_n (GaAs case), and τ_n and f_n^{hf} (Ge case) as the fitting parameter(s).

$$\mu_n = \left(\frac{1}{\mu_0} + \frac{1}{\mu_{ballistic}}\right)^{-1} \tag{5}$$

$$\mu_{ballistic} = \frac{2qL_{ch}}{\pi m_n v_{th}} \tag{6}$$

$$v_{th} = \left(\frac{8kT}{\pi m}\right)^{1/2} \tag{7}$$

We propose to adopt this concept to calculate the mobility in the channel. Alternatively, in the source/drain, carriers stay in near-equilibrium so impurity scattering dominates the mobility [26]-[27]. The mobility values in the channel and source/drain are tabulated in Table 2.1 using L_{ch} = 50 nm device as an example. We employ a doping-dependent and velocity saturation model without negative differential mobility effects, as the latter has been found to increase computational complexity without qualitatively altering simulation results [28]. Using these new inputted mobility values, the accuracy of the I_{DS}-V_{GS} curve improves yet still not satisfactory (Fig. 2.5). A ballistic-adjusted mobility, however, is the first step towards a successful fitting.

Table 2.1 THE CALCULATED GaAs MOBILITY VALUES IN THE CHANNEL AND SOURCE/DRAIN REGION, RESPECTIVELY, BASED ON SHUR'S MODEL

Channel mobility (μ_{ch})	**GaAs**
μ_0 (cm^2/V-s) [26] ($N_D = 10^{17}$ cm^{-3})	4500
$\mu_{ballistic}$ (cm^2/V-s) (L = 50 nm)	2000
μ_{ch} (cm^2/V-s) $=(1/\mu_0 + 1/\mu_{ballistic})^{-1}$	1380
Source/drain mobility ($\mu_{S/D}$)	**GaAs**
$\mu_{S/D} = \mu_0$ (cm^2/V-s) [26] (GaAs: $N_D = 10^{19}$ cm^{-3})	1500

(ii) Energy relaxation time and energy flux coefficient selection

The remaining non-calibrated parameters are energy relaxation time (τ_n), energy flux coefficient (r_n), and heat flux coefficient (f_n^{hf}). First of all, we use the default f_n^{hf} value (f_n^{hf} = 1) and explore the relationship of τ_n and r_n since these two parameters both have significant effect on the on-current. As a larger τ_n can be balanced by a smaller r_n, and vice versa, in practice we narrow down the best fits by calibrating against multiple bias points. Two points in the I_{DS}-V_{GS} curve (I_{DS} equals to 1.26×10^{-2} A/μm at V_{GS} = 1 V and 7.21×10^{-3} A/μm at V_{GS} = 0.5 V, as shown in Fig. 2.7 inset) are chosen as an initial fitting target. The combinations of τ_n and r_n matching the above currents are shown in Fig. 2.7. The intersection of the two curves indicates $\tau_n \sim 0.49$ ps and

r_n ~ 0.29, which are preliminarily selected. Note that although the current values at these two points (I_{DS} at V_{GS} = 1 V and 0.5 V) have been fitted, the entire I_{DS}-V_{GS} and I_{DS}-V_{DS} curves have not yet been examined.

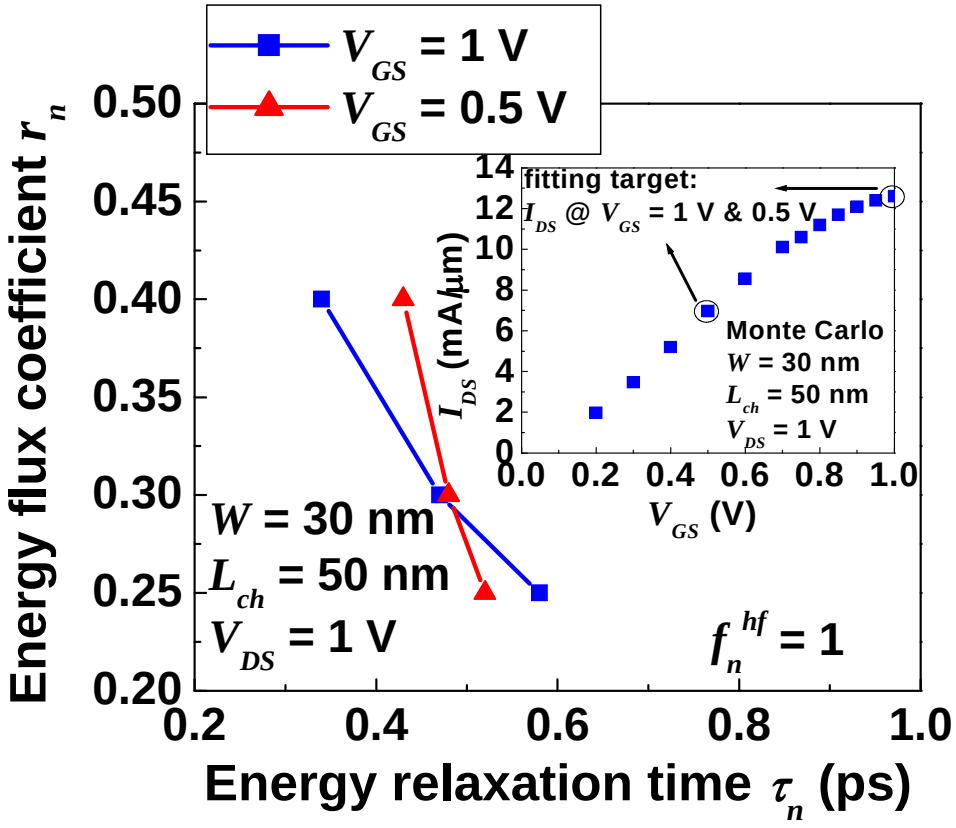


Figure 2.7 Relationship of r_n vs. τ_n to match the GaAs drain current at V_{GS} = 0.5 V and 1 V at default f_n^{hf} = 1. Larger r_n can be balanced by a smaller τ_n for a particular on-current and vice versa. The intersection of the two curves yields a preliminary τ_n = 0.49 ps and r_n = 0.29. The inset shows MC I_{DS}-V_{GS} data.

(iii) Heat flux coefficient selection

The next step is to explore the impact of f_n^{hf} based on the preliminary τ_n = 0.49 ps and r_n = 0.29. The on-state current at V_{GS} = 1 V and 0.5 V is plotted as a function of f_n^{hf}, shown in Fig. 2.8. At V_{GS} = 0.5 V, the on-current remains almost invariant, and at V_{GS} = 1 V, the change of the current is small as well. We conclude that the on-current is not sensitive to f_n^{hf} from 1 to 0.2. The impact of f_n^{hf} is then examined in the I_{DS}-V_{DS} plot with f_n^{hf} equal to 1, 0.6 and 0.2. f_n^{hf} is found to influence the current significantly at lower V_{DS} biases. Lower f_n^{hf} yields a higher current and larger drain conductance in the linear regime, as shown in Fig. 2.9.

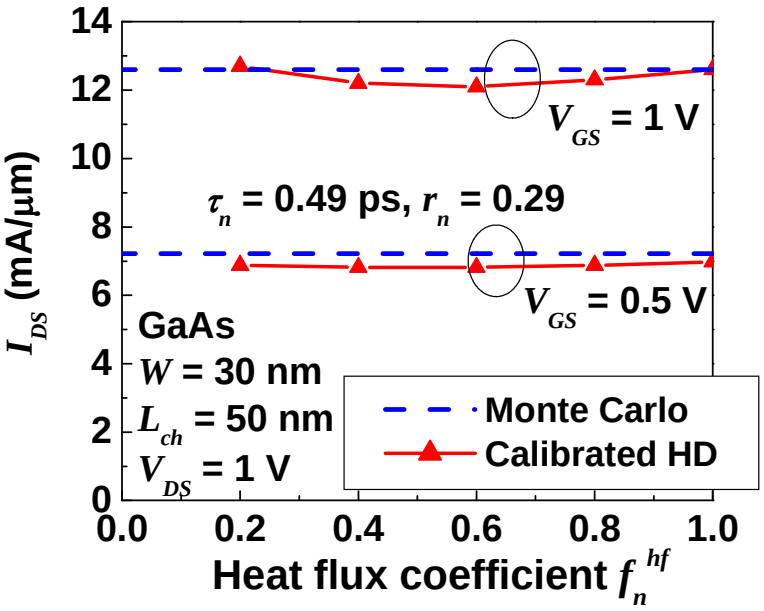


Figure 2.8 On-state current vs. f_n^{hf} of GaAs MC and calibrated HD model with the preliminary τ_n = 0.49 ps and r_n = 0.29 at V_{GS} = 0.5 V and 1 V. f_n^{hf} is found to have little impact on the on-state current.

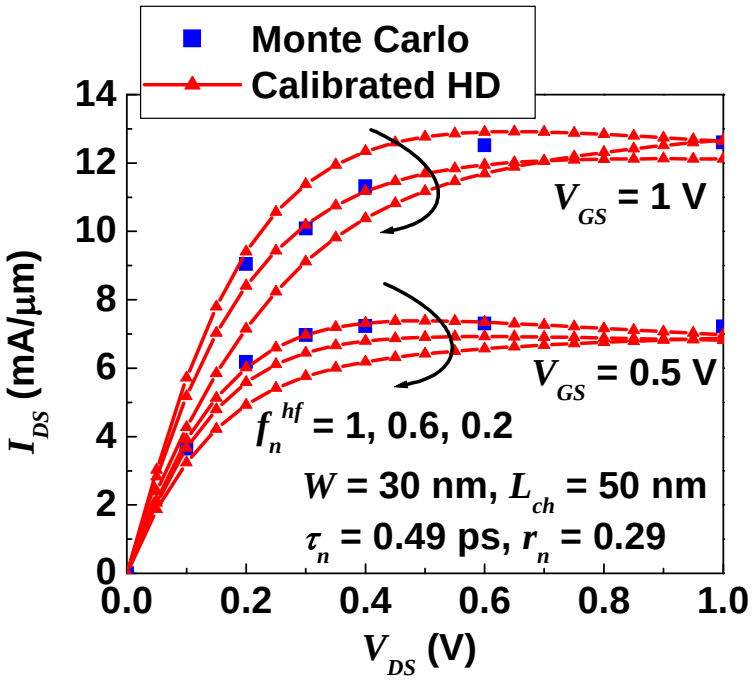


Figure 2.9 I_{DS}-V_{DS} curve of GaAs MC and calibrated HD model with f_n^{hf} value of 1, 0.6 and 0.2 at V_{GS} = 0.5 V and 1 V with the preliminary τ_n = 0.49 ps and r_n = 0.29. f_n^{hf} influences the current significantly in lower V_{DS} biases. The selection of f_n^{hf} lies in matching the conductance of the I_{DS}-V_{DS} curve.

A too large f_n^{hf} tends to overestimates the current in the linear regime (low V_{DS} biases) and hence, results in a negative channel conductance in the saturation region. The impact of f_n^{hf} can be explained by the change of carrier velocity (v), which consists of a drift (v_d) and thermal (v_c) contribution (Eq. 8). Note that the heat flux (Q_{heat}) is taken to be proportional to the temperature gradient through a heat flux coefficient (f_n^{hf}) in the hydrodynamic model (Eq. 3) but essentially originates from the thermal motion of carriers (Eq. 9).

$$\vec{v} = \vec{v}_d + \vec{v}_c \tag{8}$$

$$Q_{heat} = \frac{-5r_n\lambda_n}{2} f_n^{hf} \frac{k^2}{q} n\mu_n T_n \nabla T_n = \frac{1}{2} nm \left\langle v_c^2 \vec{v}_c \right\rangle \tag{9}$$

Under a high field (high V_{DS}), the drift component of carriers dominates the overall current so different f_n^{hf} values do not significantly alter the on-state current. At lower V_{DS}, however, the drift component becomes weaker and the thermal contribution becomes more important. Hence, f_n^{hf} has a greater impact on the drain current in this regime. In brief, the key to the f_n^{hf} selection lies in matching the conductance of the I_{DS}-V_{DS} curve, rather than matching only the on-state current. The on-state current fitting requires a fine-tuning of τ_n and r_n. An appropriate f_n^{hf} is found to be 0.6, which leads to the best fit of the channel conductance.

(iv) Optimization of τ_n and r_n

With f_n^{hf} = 0.6, τ_n and r_n need to be optimized (based on the preliminary τ_n = 0.49 ps and r_n = 0.29) by fitting the entire I_{DS}-V_{GS} and I_{DS}-V_{DS} curves. The finalized τ_n and r_n are 0.52 ps and 0.3, respectively. Excellent fits of I_{DS}-V_{GS} and I_{DS}-V_{DS} curves are obtained (Figs. 2.10(a)-(c)). Note that the number of MC data points in the subthreshold region of the I_{DS}-V_{GS} curve is limited because we focus on the calibration of the on-state current. Since subthreshold behavior is determined primarily by electrostatic integrity, rather than carrier mobility and transport

parameters, it is not a major concern in this work. In fact, even a non-calibrated DD simulation should yield a good fitting in the subthreshold regime [29].

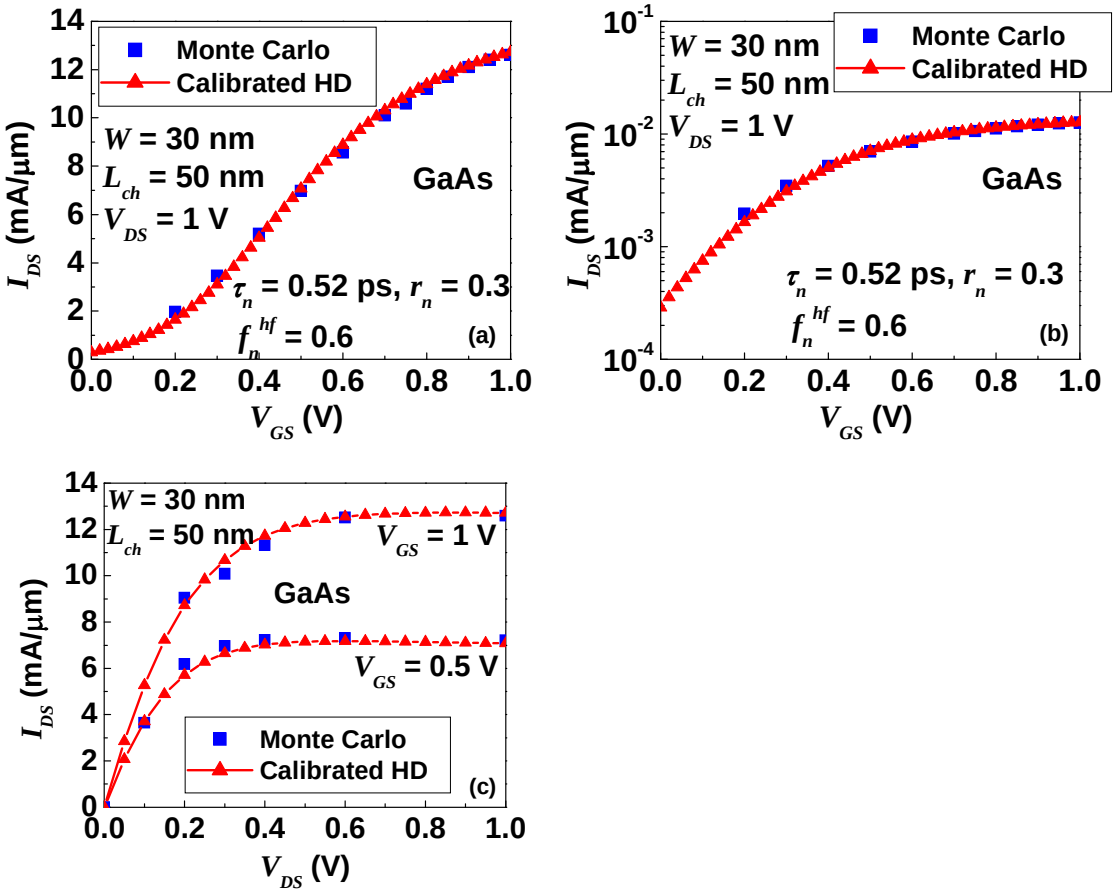


Figure 2.10 GaAs (a) I_{DS}-V_{GS} in linear scale (b) I_{DS}-V_{GS} in log scale (c) I_{DS}-V_{DS} curve of MC and calibrated HD model of 50 nm channel length with the finalized parameters: τ_n = 0.52 ps, r_n = 0.3, and f_n^{hf} = 0.6. An excellent fit is obtained for the entire curve.

2.2.4 Extension to Other Device Dimensions

Our calibration is extendable to different device dimensions using identical r_n (or 0.3), f_n^{hf} (or 0.6), an appropriate mobility (dimension-dependent) based on step (i), and τ_n as the only

fitting variable. As shown in Fig. 2.11, a linear fit provides an appropriate τ_n selection for different channel length from 100 nm to 15 nm as well as different body thickness (30 nm, 24 nm, and 18 nm). The trend of decreasing τ_n with shorter dimensions illustrates the quasi-ballistic transport nature in small device dimensions. The transit time should be shorter in smaller dimensions as the electrons travel a shorter distance from source to drain with few collision events during the course of transport.

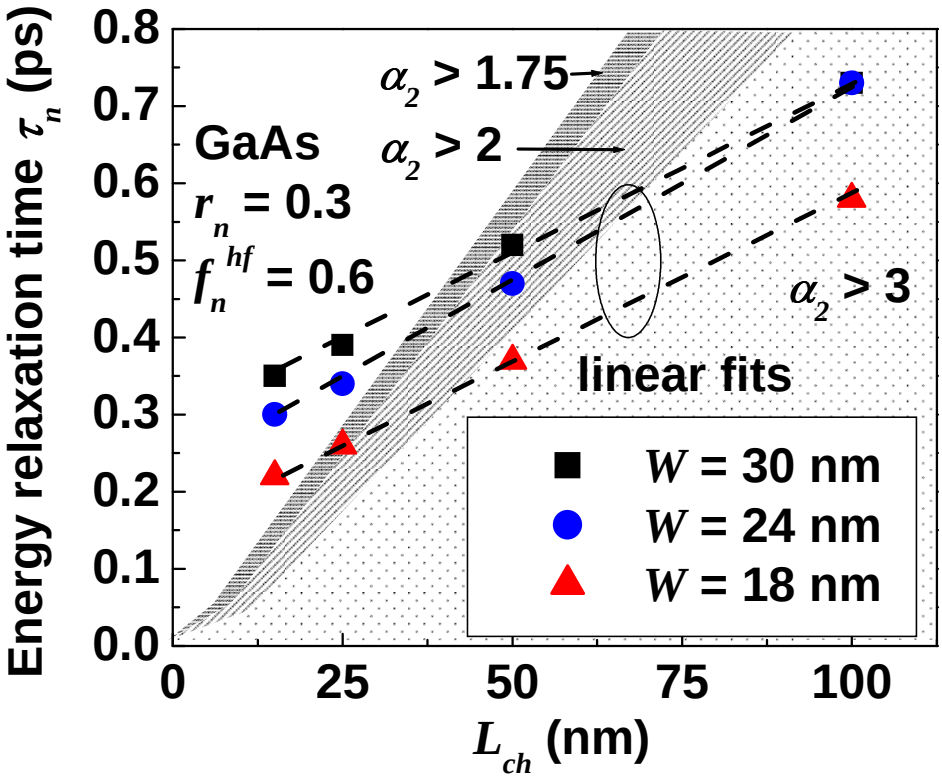


Figure 2.11 τ_n vs. channel length (L_{ch}) of a calibrated GaAs HD model. The linear fit provides an appropriate τ_n selection for different dimensions with the fixed r_n = 0.3, and f_n^{hf} = 0.6. The different shaded areas correspond to different α_2 value [30].

In a double gate device design, the body thickness should be small relative to the gate length to suppress short channel effects. Based on the scaling rule of a double gate device in [30], α_2 is equal to $L_G / 2\lambda_2$ where λ_2 is the neutral length relevant to the permittivity / thickness of the semiconductor and gate oxide, as described in Eqs. 10 and 11. If α_2 is equal to or greater than 3, nearly ideal 60 mV/dec swing can be achieved.

$$\alpha_2 = \frac{L_G}{2\lambda_2} \tag{10}$$

$$\lambda_2 = \sqrt{\frac{\varepsilon_{semi}}{2\varepsilon_{ox}}(1+\frac{\varepsilon_{ox}}{4\varepsilon_{semi}}\frac{t_{semi}}{t_{ox}})t_{Semi}t_{ox}} \tag{11}$$

The gate control decreases with smaller α_2. The different shaded areas in Fig. 2.11 correspond to different α_2 values. For those data points without shade, α_2 is smaller than 1.75.

The fitting of I_{DS}-V_{GS} plots with L_{ch} ranging from 100 nm to 15 nm and W = 30 nm and W = 18 nm are shown in Figs. 2.12(a) and (b), respectively. For those shaded dimensions in Fig. 2.11, the fitting is very good over the whole bias range. For the other dimensions with worse gate control (e.g., not in the shaded area), the fitting at low V_{GS} biases (closer to subthreshold regime) is not as satisfactory. It may be caused by Sentaurus' inability to properly handle the transition between the subthreshold and accumulation regimes if the gate control over the body is inadequate, as pointed out in [31]. We, however, want to emphasize again that this work focuses

on the on-state current calibration and a slight fitting deviation close to the subthreshold regime does not essentially negate the effectiveness of our systematic framework. More importantly, the fitting works satisfactorily in “well-behaved” devices with reasonable gate control.

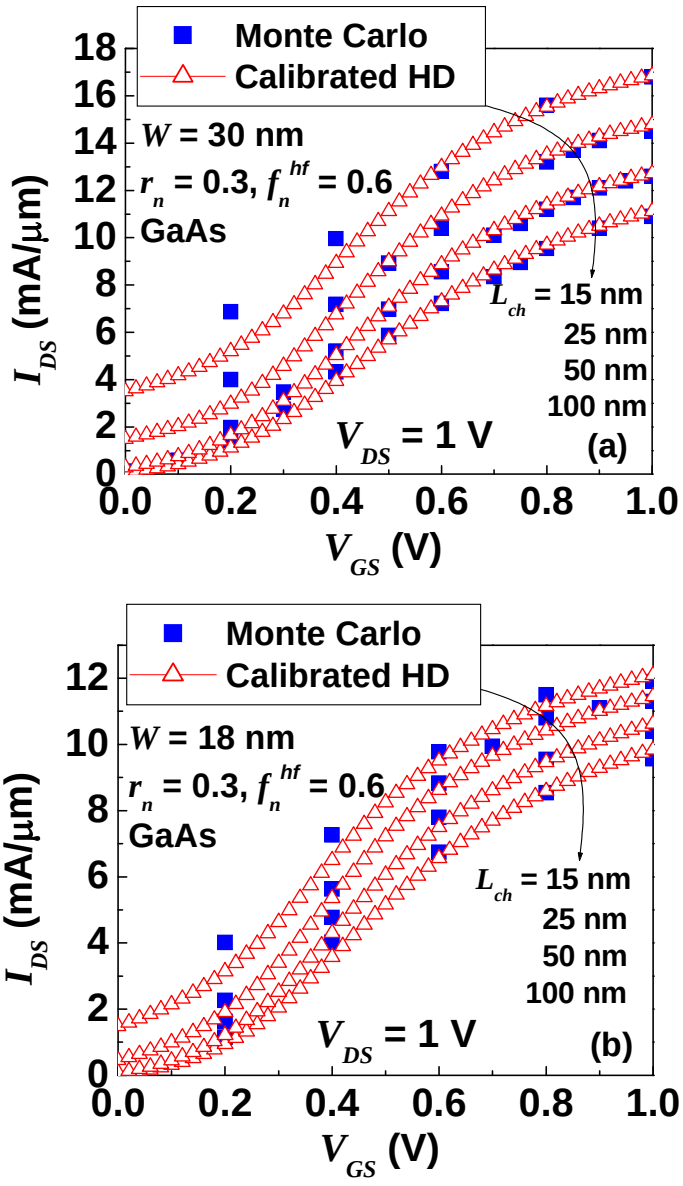


Figure 2.12 I_{DS}-V_{GS} curve of GaAs MC and calibrated HD model of (a) 30 nm body thickness (b) 18 nm body thickness. The channel length ranges from 100 nm to 15 nm. The fixed $r_n = 0.3$, and $f_n^{hf} = 0.6$ and the corresponding τ_n as shown in Fig. 2.11 are used.

2.3 Different Material System

The same methodology is applied to a Ge inversion mode MOSFET (Fig. 2.4(b)). We start with the dimension W = 30 nm, L_{ch} = 50 nm and the inputted mobility is shown in Table 2.2.

Table 2.2 THE CALCULATED Ge MOBILITY VALUES IN THE CHANNEL AND SOURCE/DRAIN REGION, RESPECTIVELY, BASED ON SHUR'S MODEL

Channel mobility (μ_{ch})	**Ge**
μ_0 (cm^2/V-s) [27] ($N_D = 10^{17}$ cm^{-3})	2100
$\mu_{ballistic}$ (cm^2/V-s) (L = 50 nm)	1350
μ_{ch} (cm^2/V-s) $=(1/\mu_0 + 1/\mu_{ballistic})^{-1}$	820
Source/drain mobility ($\mu_{S/D}$)	**Ge**
$\mu_{S/D} = \mu_0$ (cm^2/V-s) [27] (Ge: $N_D = 10^{20}$ cm^{-3})	180

We perform r_n vs. τ_n matrix (fitting target: $I_{D,sat}$ at V_{GS} = 0.4 V and 1 V) with f_n^{hf} = 1 (similar to Fig. 2.7). The preliminarily selected r_n and τ_n are 0.4 and 0.6, respectively. The on-current value, however, is found to decrease with decreasing f_n^{hf} (Fig. 2.13(a)). Note that the I_{DS}-V_{GS} and I_{DS}-V_{DS} curves (Figs. 2.13(b) and (c)) actually fit well with the default f_n^{hf} = 1, except the low V_{GS} biases in the I_{DS}-V_{GS} plot. The fitting in this dimension is thus accomplished. To proceed to the calibration of L_{ch} = 25 and 15 nm, r_n is fixed as 0.4, and τ_n and f_n^{hf} are served as two fitting parameters (as shown in Fig. 2.6 flow chart). The finalized I_{DS}-V_{GS} plots with L_{ch}

ranging from 50 nm to 15 nm and W = 30 nm are shown in Fig. 2.13(d). The fitted τ_n and f_n^{hf} for different L_{ch} is shown in Fig. 2.14. Since f_n^{hf} influences on-current, f_n^{hf} needs to be individually tuned for each dimension to obtain a good fitting.

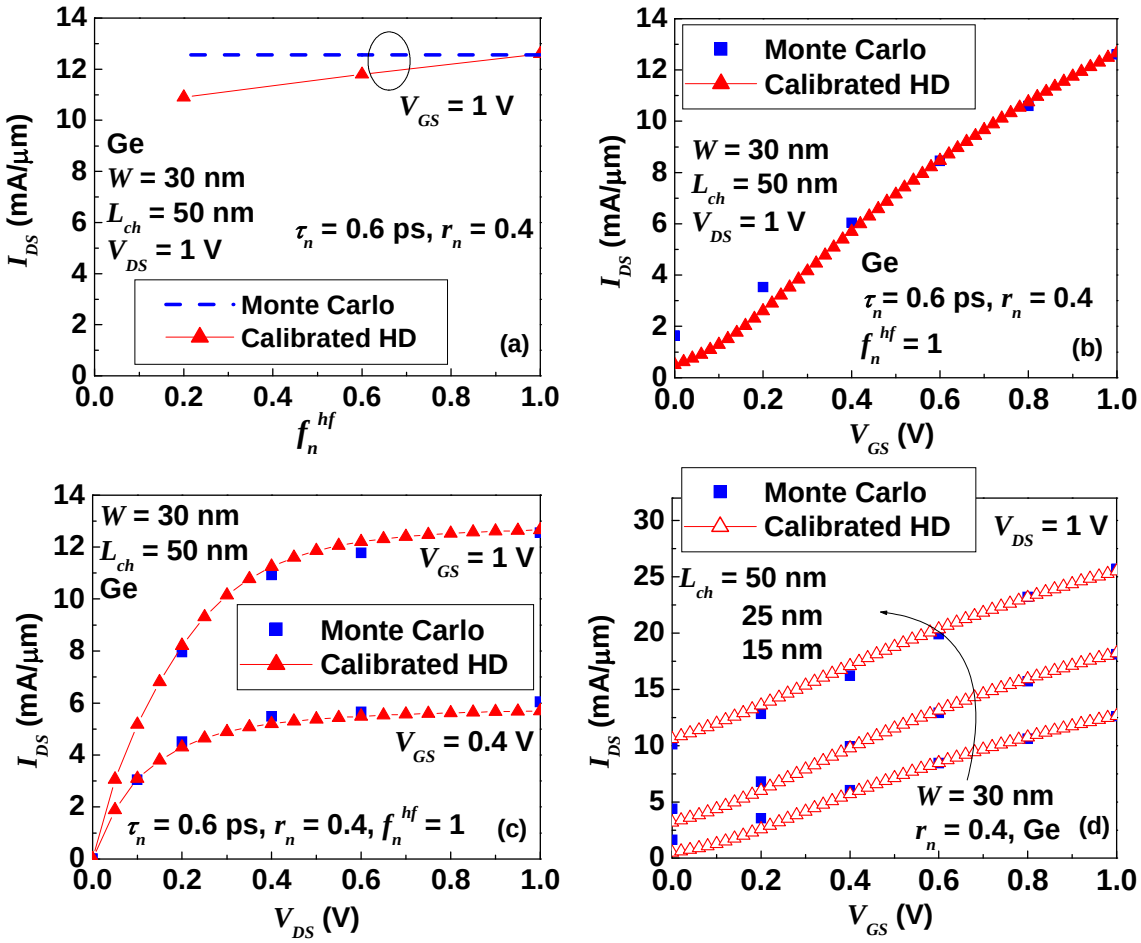


Figure 2.13 (a) On-state current vs. f_n^{hf} of Ge MC and calibrated HD model with τ_n = 0.6 ps and r_n = 0.4 at V_{GS} = 1 V. f_n^{hf} influences the on-state current. (b) I_{DS}-V_{GS} (c) I_{DS}-V_{DS} curve of MC and calibrated HD model of 50 nm L_{ch} with τ_n = 0.6 ps, r_n = 0.4, and f_n^{hf} = 1. (d) I_{DS}-V_{GS} curve of MC and calibrated HD model with the channel length ranging from 50 nm to 15 nm. The r_n is fixed as 0.4, and corresponding f_n^{hf} and τ_n as shown in Fig. 2.14 are used.

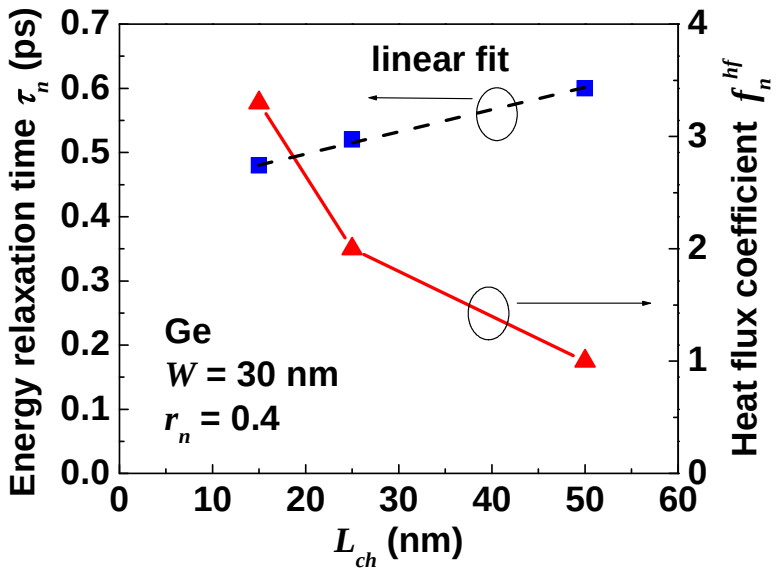


Figure 2.14 τ_n and f_n^{hf} vs. channel length (L_{ch}) of a calibrated Ge HD model. The fit of τ_n and f_n^{hf} provides an appropriate parameter selection for different dimensions with the fixed $r_n = 0.4$.

The possible explanation to the fact that f_n^{hf} impacts $I_{D,sat}$ in Ge but not in GaAs may be due to the greater effective mass in Ge. The drift component of carriers may be reduced while the thermal component is enhanced due to the greater effective mass. Therefore, f_n^{hf} becomes influential on the total current in Ge. Nonetheless, we presently cannot completely rule out other possibilities, such as different device structures (accumulation mode versus inversion mode) or density of states, etc.

2.4 Incorporation of Other Physical Effects

The theme of this work is about a systematic calibration framework. To facilitate the development of this work, MC simulations are used as our reference and hence, some effects that may need appropriate experimental data to “calibrate” MC are not currently considered. Further, due to the relatively thick body thickness, quantum effects are not included. Our calibration strategy, however, is extendable to incorporate these effects. We briefly outline the strategy to include these effects.

(a) Surface roughness: To include surface roughness effect in our methodology, we would calibrate a mobility degradation model (such as Lombardi model) in Sentaurus. An experimental mobility universal curve (mobility versus vertical electric field) is needed as a reference. We fit against the experimental mobility data and extract the corresponding fitting parameters in Lombardi model, similar to what has been done in Si. Once the mobility degradation factors have been set, the rest of the calibration would proceed similarly for our work, with the surface degraded mobility substituted for the bulk mobility.

The same procedure can be applied on MC to calibrate against experimental mobility data. In MC, the ratio of diffusive / reflective scattering at interface can be adjusted to describe surface roughness [32]. By fitting the experimental mobility data, MC can be “calibrated” as well.

(b) High-κ related scattering mechanisms: In this work, high-κ related scattering mechanisms, such as RPS, RCS, are not included in MC. If those scatterings need to be considered, the procedure is similar to what has been mentioned above. In Sentaurus, for example, an enhanced high-κ Lombardi model is available which parameterizes the effects of RPS, RCS, etc. Experimental data are needed for calibration. In practice the fitting in Sentaurus of the appropriate experimental inversion layer mobility will automatically include these mechanisms.

(c) Interface states: To unveil a device's "intrinsic" behavior, routinely interface states are omitted in the device simulation. The key in this work is the systematic calibration procedure of Sentaurus macroscopic models versus MC simulation. The inclusion of interface states does not change the calibration flow at all. Just ensure the same amount of interface states are applied in both Sentaurus and MC. Interface state scattering may be parameterized in a similar fashion to the RPS/RCS effects above if solid data are available.

(d) Quantization effects: To model quantum effects in an ultra-thin body device, the most rigorous approach is to include Schrödinger equation self-consistently into the computation. Due to its heavy computational burden and convergence problems, however, its direct application to simulation is limited. Various macroscopic models, such as density gradient model [33]-[34], van Dort model [35], modified local-density approximation model [36], etc., have been proposed to

incorporate quantum effects with a better computational efficiency, but Schrödinger equation is consistently used for the validation and calibration of these models [20].

Density-Gradient method is a common quantization model [33]-[34]. In this model, a fitting parameter γ is introduced to model quantum carrier confinement within a potential well. To calibrate Density-Gradient model against Schrödinger equation, a MOS structure is used. By tuning γ, the electron concentration computed by using Density-Gradient model is matched to the electron concentration computed by using Schrödinger equation.

We want to emphasize again that incorporation of these effects is feasible and it does not essentially alter our calibration framework. The modified calibration flow chart is shown in Fig. 2.15 should these effects are considered.

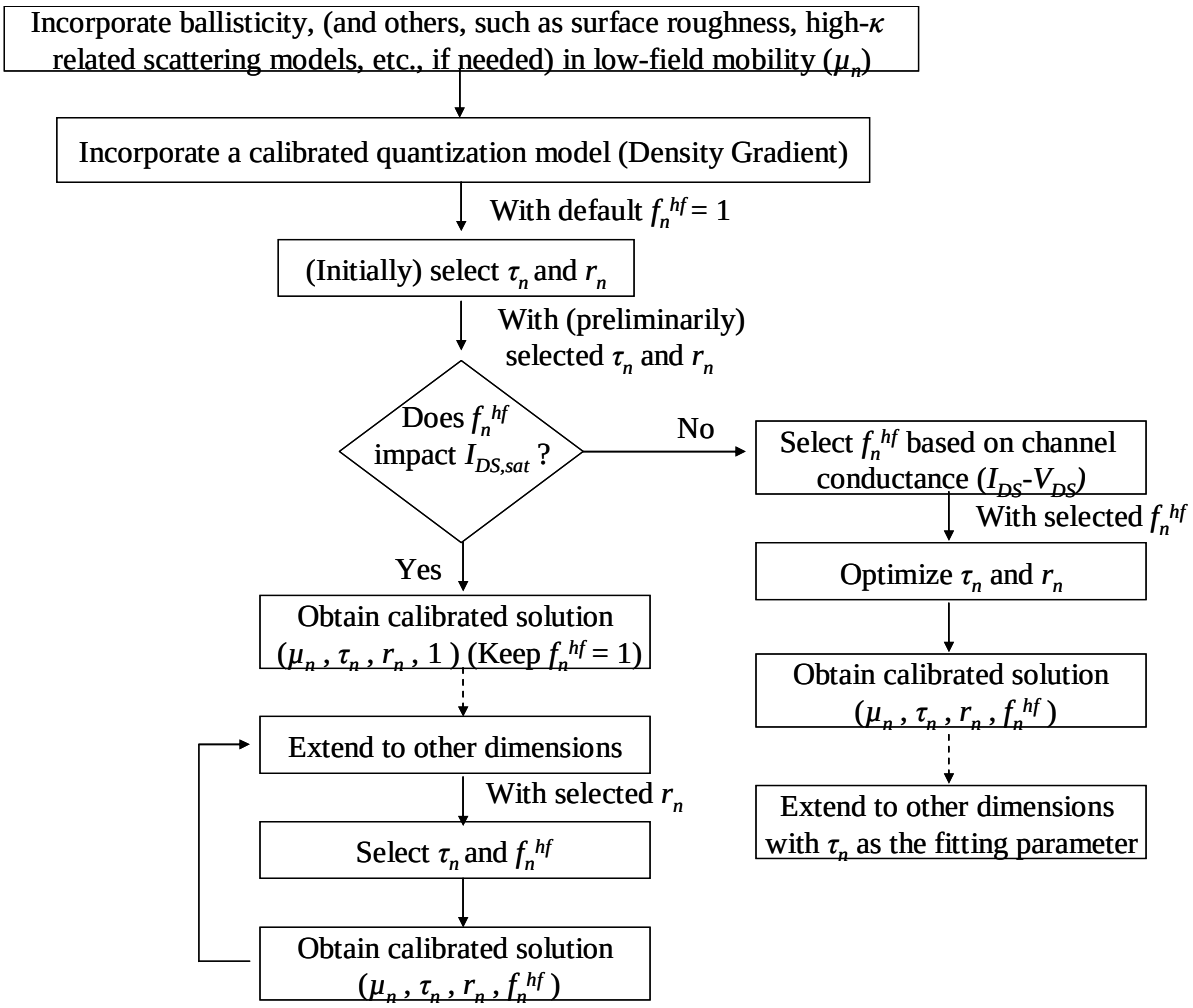


Figure 2.15 Modified flow chart of the calibration procedure for incorporating additional scattering mechanisms or quantum effects.

Here, we would like to demonstrate our calibration method with surface roughness effect included. A Ge inversion mode device is used a vehicle. First of all, we include surface roughness scattering in MC simulation and extract the low-field mobility from a long-channel Ge device. We then calibrate Lombardi model to fit the MC mobility versus surface field data by adjusting the parameters in Lombardi model. Afterwards, we include the calibrated Lombardi model in Sentaurus and perform calibration method to fit *I*-*V* data of a short-channel Ge device generated by MC (with surface roughness effect turned on as well).

In DAMOCLES, surface roughness scattering is modeled as follows. Carriers colliding with the channel/dielectric interface are treated as specular scattering events with probability *s* and diffuse scattering events with probability $1 - s$ [19],[37]. It is shown that experimental data on Si nFETs are reconciled with $s \sim 0.85$–0.90 [37]. In GaAs, however, there has been lacking an experimental mobility data with respect to surface roughness due to the process-sensitive interface properies of III-V semiconductors. Therefore, in our MC simulation, *s* is set to be 0.85, the same as Si value, to account for surface roughness scattering effect. A long channel Ge device ($L_G = 1$ μm) is used as a vehicle for mobility extraction at $V_{DS} = 0.1$ V.

In Lombardi model, surface scattering effect consists of two components [38]. The surface contribution due to acoustic phonon is given by,

$$\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C((N_{A,0} + N_{D,0})/N_0)^{\lambda}}{F_{\perp}^{1/3}(T/300\,\mathrm{K})^{k}} \tag{12}$$

and the contribution due to surface roughness scattering, has the form as

$$\mu_{sr} = \left(\frac{(F_{\perp}/F_{ref})^{A^*}}{\delta} + \frac{F_{\perp}^{3}}{\eta} \right)^{-1} \tag{13}$$

According to Matthiessen's rule, the surface contribution to the mobility (μ_{ac} and μ_{sr}) are then combined with the bulk mobility (μ_0)

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \tag{14}$$

D=exp(-x/l_{crit}) is a damping factor, where x is the distance from the interface and l_{crit} a fit parameter, that damps the impact of surface roughness at locations far away from the interface.

Default values and calibrated values of all parameters in Lombardi model are shown in Table 2.3. The calibrated parameters of Lombardi model corresponds to the fitted mobility-surface field curve in Fig. 2.16.

Table 2.3 THE DEFAULT AND CALIBRATED VALUES OF LOMBARDI MODEL

Parameters	Default value	Calibrated value	Unit
B	4.75×10^{7}	5.75×10^{7}	cm/s
C	5.8×10^{2}	1×10^{3}	$cm^{5/3}V^{-2/3}s^{-1}$
N_0	1	1	cm^{-3}
λ	0.125	0.15	1
k	1	1	1
F_{ref}	1	1	v/cm
A^*	2	2	1
δ	5.82×10^{14}	2.82×10^{15}	cm^2/Vs
η	5.82×10^{30}	5.82×10^{30}	$V^2cm^{-1}s^{-1}$
l_{crit}	1×10^{-6}	1×10^{-6}	cm

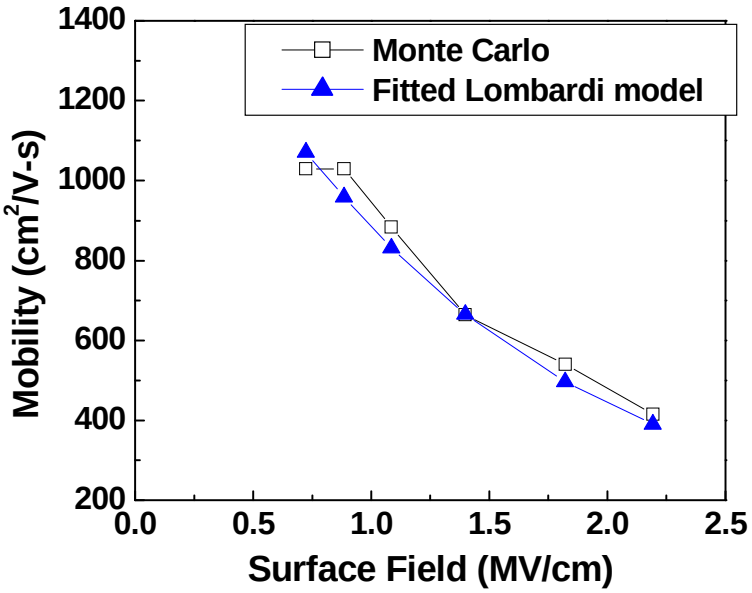


Figure 2.16 The calibrated mobility curve based on Lombardi model. The new set of parameters of Lombardi model is shown in Table 2.3.

With the new calibrated Lombardi model, the fitting I_{DS}-V_{GS} curve is shown in Fig. 2.17 of a 50 nm L_{ch} , 15 nm width Ge inversion mode MOSFET. The parameter set is found to be τ_n = 0.7 ps, r_n = 0.4, and f_n^{hf} = 1. The energy flux coefficient and heat flux coefficient are the same as the case without surface roughness with a new energy relaxation time fitted. The good curve fitting demonstrates that additional relevant physical effects can be successfully incorporated into our calibration methodology.

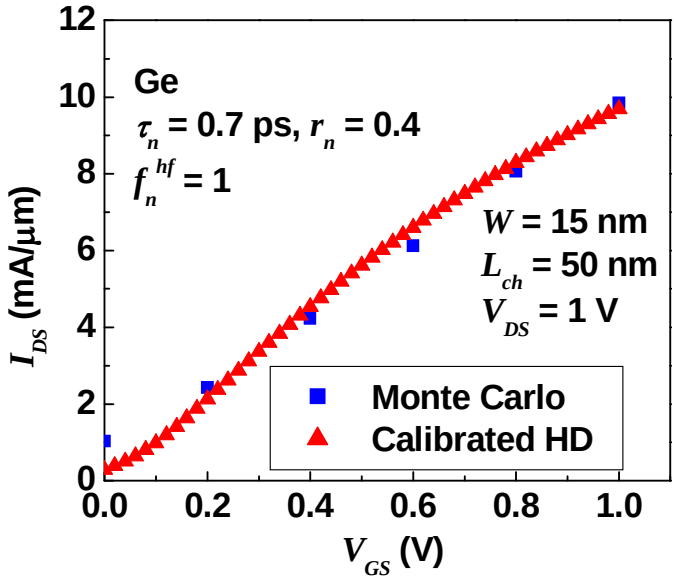


Figure 2.17 I_{DS}-V_{GS} of MC and calibrated HD model of 50 nm L_{ch} , 15 nm width Ge inversion mode MOSFET with τ_n = 0.7 ps, r_n = 0.4, and f_n^{hf} = 1. Surface roughness effect is included in both MC and HD.

2.5 Summary

For the first time, a systematic approach of HD model calibration against MC simulation is presented. Through a step-by-step selection of model parameters (μ_n, τ_n, r_n, f_n^{hf}), the methodology leads to an excellent fitting of entire I_{DS}-V_{GS} and I_{DS}-V_{DS} curves. Further, it is extendable to different device dimensions (both channel length and body thickness). Two different material systems and device structures are demonstrated in this work and the methodology should be applicable to any other material systems. Here, MC simulations are matched but the procedure should be applicable to experimental data as well. This work facilitates the extension of HD simulations to the quasi-ballistic regime with satisfactory accuracy and time-efficiency.

Chapter 3
Analog/RF Performance Optimization of a Vertical III-V Double Gate Transistor

3.1 Introduction

Parasitics engineering in field-effect-transistor (FET) plays a determining role in the analog/RF performance. To minimize any resultant performance degradation, the source (S) and drain (D) structure designs need to be carefully optimized. Reducing S/D overlap (or increasing underlap) length reduces parasitic capacitance but inevitably increases parasitic resistance, and vice versa. Conventional FETs, such as metal-oxide-semiconductor field effect transistors (MOSFETs) or high electron mobility transistors (HEMTs), have inherently symmetric S/D design that has limited optimization flexibility. An asymmetric S/D architecture, on the other hand, offers more design versatility and has not been extensively examined before.

As mentioned before, non-planar structures, such as multigate thin body or gate-all-around nanowire (NW) transistors, emerge as promising devices to improve short channel effect (SCE) [1]-[5]. Although the SCE reduction can improve FET analog/RF performance [6], the parasitic

components pertinent to the ultrathin body architecture compromise the overall benefit. While analog/RF characteristics of either Si or III-V multigate or NW transistors with symmetric S/D design have been previously reported [7]-[12], similar analyses on asymmetric structure are lacking.

In this chapter, we introduce the vertical replacement gate (VRG) [13] process flow and discuss its advantages compared with the lateral counterparts. Secondly, we explore a GaAs accumulation mode vertical DG transistor assuming a VRG or equivalent fabrication process flow for asymmetric S/D design and optimization. Separate control of S/D spacer thickness and underlap length can be implemented and their individual impact on analog performance is discussed. Device design guidelines for different analog/RF metrics improvement are presented.

3.2 Vertical Replacement Gate Process

A vertical transistor possesses several advantages compared with its lateral counterparts. First of all, the critical dimension (e.g., gate length) control is through film deposition rather than through conventional photolithography and etching. The precise film control by deposition is not as challenging as that by photolithography and etching. For examples, the thickness of film deposited using Atomic Layer Deposition (ALD) technique solely depends on the number of

reaction cycles, which enables straightforward and precise thickness control. Secondly, the vertical process facilitates the formation of an asymmetric structure, including asymmetric channel doping, asymmetric S/D overlap/underlap or spacer thickness, etc. These asymmetric structures can be implemented by epitaxial growth, ion implantation, film deposition and so forth.

In this work, assuming a VRG fabrication process, we investigate a GaAs accumulation mode vertical double gate (DG) transistor for asymmetric S/D design and optimization. The VRG process flow is shown as follows.

(a) Start with a n^+ GaAs substrate (Fig. 3.1(a)).

(b) Deposit HfO_2 / SiN / HfO_2 sequentially. HfO_2 and SiN deposition is by ALD and low pressure chemical vapor deposition (LPCVD) process, respectively (Fig. 3.1(b)).

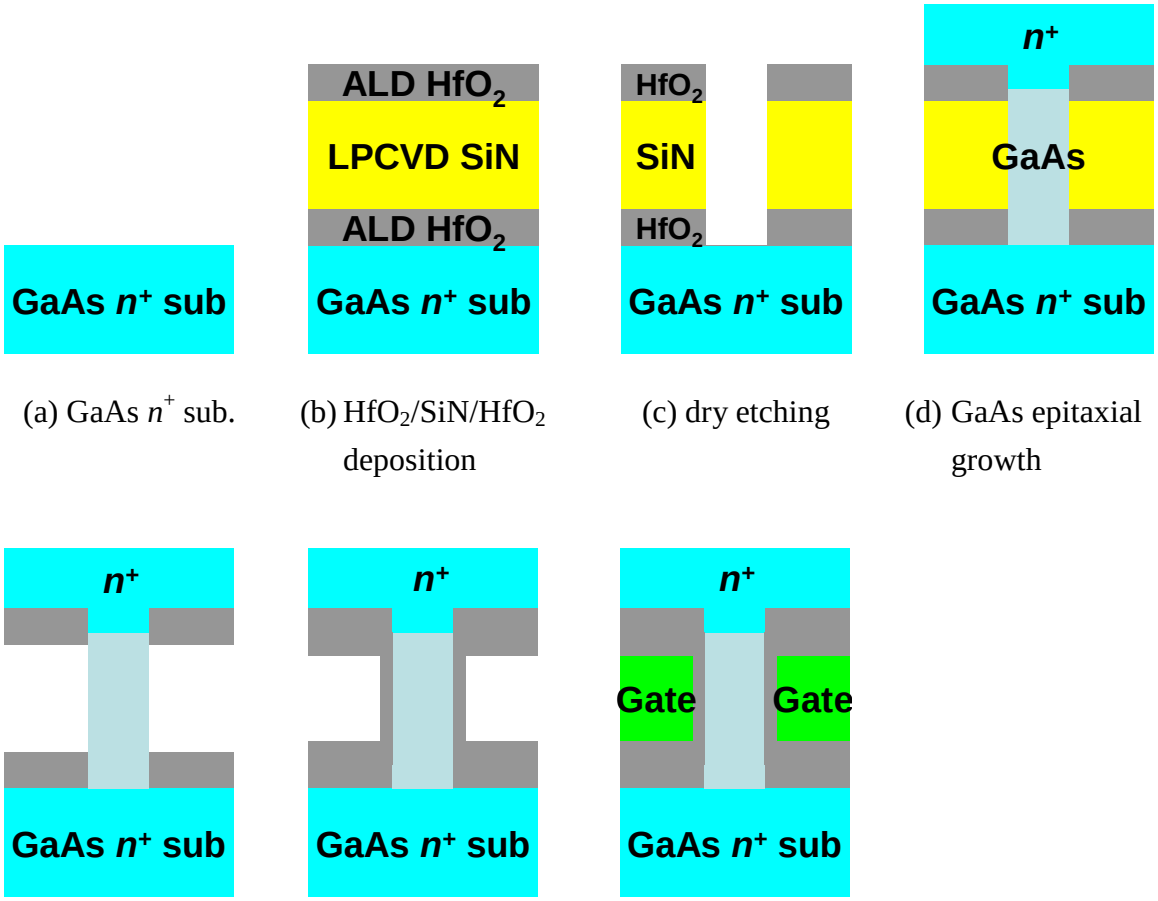
(c) Perform anisotropic etching to open a trench in the HfO_2 / SiN / HfO_2 film stack (Fig. 3.1(c)).

(d) Perform GaAs epitaxial growth to form channel and source region of the device. The doping concentration in the channel and source can be tuned individually during the epitaxial process (Fig. 3.1(d)).

(e) Remove SiN by wet etching (Fig. 3.1(e)).

(f) Deposit HfO_2 gate dielectric using ALD process (Fig. 3.1(f)).

(g) Deposit gate metal (Fig. 3.1(g)).



(a) GaAs n^+ sub. (b) HfO_2/SiN/HfO_2 deposition (c) dry etching (d) GaAs epitaxial growth

(e) SiN wet etching (f) ALD gate dielectric HfO_2 (g) Gate metal deposition

Figure 3.1 Vertical replacement gate process. It features the control of gate length through the deposited SiN thickness rather than the photolithography capability. Further, S/D underlap/spacer can be individually tuned by ALD dielectric thickness and epitaxial process.

In the above VRG process, the device gate length is completely controlled by the deposited LPCVD SiN thickness rather than by photolithography capability. Further, the S/D underlap and

spacer are individually tuned by ALD HfO_2 thickness and epitaxial process. Therefore, asymmetric S/D design can be readily implemented by the VRG process.

3.3 Analog/RF Performance and Optimization

Based on the VRG process, the simulated device structures are shown in Fig. 3.2. Fig. 3.2(a) represents the baseline GaAs accumulation mode DG transistor. The gate dielectric is 2 nm HfO_2; the sidewall spacer is 3 nm HfO_2. The gate length (L_G) is 29 nm, and the body thickness (t_{semi}) is 18 nm. Structures with varying source side and drain side spacer and underlap length are shown in Fig. 3.2(b) and Fig. 3.2(c), respectively. Four different structures based on Fig. 3.2(b) and (c) are discussed in this work (Table 3.1). Structure SS ("Source-side Spacer") has a fixed 3 nm source underlap and different source spacer thickness; drain side is the same as the baseline device. Structure DS ("Drain-side Spacer") is identical to Structure SS with the source and drain switched. Further, Structure SU ("Source-side Underlap") has a fixed 15 nm HfO_2 source spacer and different source underlap; the drain side is the same as the baseline device. Structure DU ("Drain-side Underlap") is identical to Structure SU with source and drain switched.

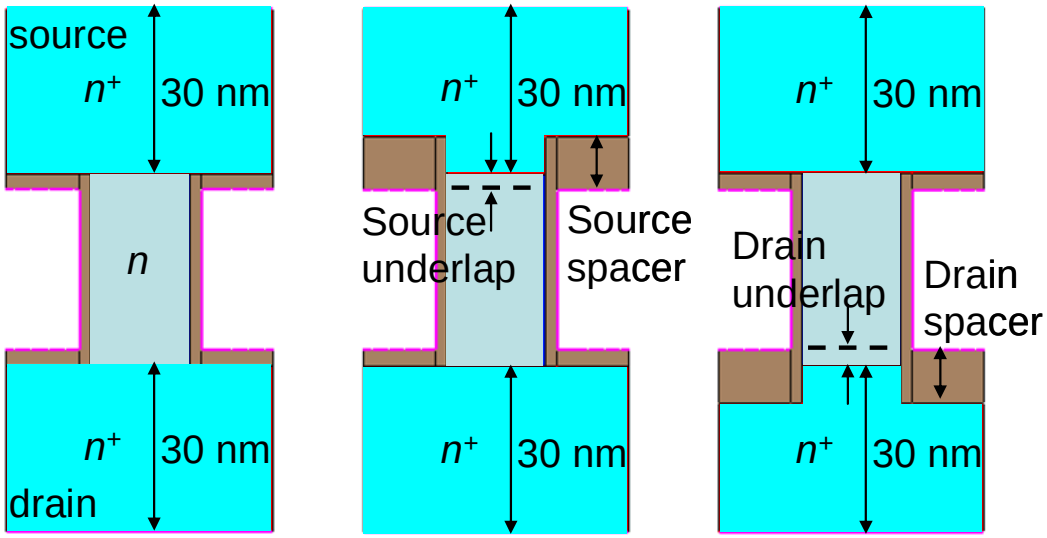


Figure 3.2 (a) Simulated baseline GaAs accumulation-mode DG MOSFET, (b) structure with varying source side spacer and underlap length, and (c) structure with varying drain side spacer and underlap length.

TABLE 3.1

SPACER AND UNDERLAP DIMENSIONS OF SOURCE/DRAIN IN BASELINE DEVICE AND STRUCTURE SS, DS, SU, DU

	Source		Drain	
Structure	Spacer (nm)	Underlap (nm)	Spacer (nm)	Underlap (nm)
Baseline	3	3	3	3
SS	variable	3	3	3
DS	3	3	variable	3
SU	15	variable	3	3
DU	3	3	15	variable

Two different dopings in the channel are used, *n*-type 1×10^{17} cm^{-3} and 5×10^{18} cm^{-3}, while the doping in source/drain regions is *n*-type 1×10^{19} cm^{-3}. The S/D doping profile is abrupt. The distance of channel edge to n^+ S/D metal contact is kept at 30 nm for all devices.

Commercial Synopsys™ Sentaurus Device was used for hydrodynamic simulations in this work. The HD models have been calibrated to full-band DAMOCLES Monte Carlo (MC) simulation [14], as discussed in Chapter 2. Phonon and ionized impurity scattering were included and the gate workfunction was 4.3 eV. No interface state, generation or recombination was activated in either device. Surface roughness is not present in this work as it is experimentally-dependent and there exist no universal quantitative parameters in MC modeling. More importantly, at low gate overdrive and surface field (< 0.35 V and < 5×10^5 V/cm, respectively, in this work), the impact of surface roughness is mitigated [15].

The metrics used in this work include maximum transconductance $g_{m,\max}$, g_m/I_{DS}, cutoff frequency (f_T), maximum oscillation frequency ($f_{\max}$), output resistance (R_{out}) and intrinsic gain ($g_m \times R_{out}$) as these are all important analog device metrics. The extraction was performed at two different bias points. One is the $g_{m,\max}$ point (corresponding to an almost constant gate overdrive for all different structures as shown below) and the other is at a constant bias current, I_{DS} = 2 mA/μm, as constant current is a common biasing method for analog circuit applications. In most devices, it corresponds to ~0.1 V gate overdrive. A constant drain voltage (V_{DS}) equal to 0.5 V is

applied for maximum output swing (half of V_{DD} = 1 V) [20].

3.3.1 Transconductance

With thicker spacers (Structures SS and DS), the parasitic resistances of n^+ source and drain ($R_S(n^+)$ and $R_D(n^+)$, respectively) increase as the n^+ source and drain volume is reduced. Similarly, with larger underlap (Structures SU and DU), the associated parasitic resistances (R_S(underlap) and R_D(underlap), respectively) increase as the distance between n^+ source to gate edge is increased. These sources of increased parasitic resistance in turn lower the $g_{m,\max}$ values of all four structures, as shown in Fig. 3.3(a), where the dashed line indicates the baseline device value (Fig. 3.2(a)). Further, the $g_{m,\max}$ values of Structures SS and DS are comparable to the baseline as the dominant contributor to parasitic resistance is the underlap length, but not the available source/drain volume, for $g_{m,\max}$ degradation. $g_{m,\max}$ reduces more in Structure SU than in DU as the source side parasitic resistance impacts $g_{m,\max}$ more significantly than the drain side parasitic resistance as g_m is given by

$$g_m = \frac{g_{m,\text{int}}}{1 + g_{m,\text{int}} R_S + g_{d,\text{int}} (R_S + R_D)} \approx \frac{g_{m,\text{int}}}{1 + g_{m,\text{int}} R_S} \tag{1}$$

where $g_{m,\text{int}}$ and $g_{d,\text{int}}$ represent the intrinsic g_m and g_d (drain conductance), respectively. R_S and R_D are source and drain total parasitic resistance, respectively (e.g., $R_S = R_S(n^+) + R_S$(underlap), $R_D = R_D(n^+) + R_D$(underlap)). In a "well-tempered" device with good gate control, $g_{d,\text{int}}$ is much

smaller than $g_{m,\text{int}}$ so $g_{d,\text{int}}(R_S+R_D)$ can be neglected in Eq. (1). Also, comparing Fig. 3.3(a) to (b), the $g_{m,\text{max}}$ degradation is more pronounced with lower channel doping, especially for Structure SU, since the associated R_S increase due to a longer source underlap is larger.

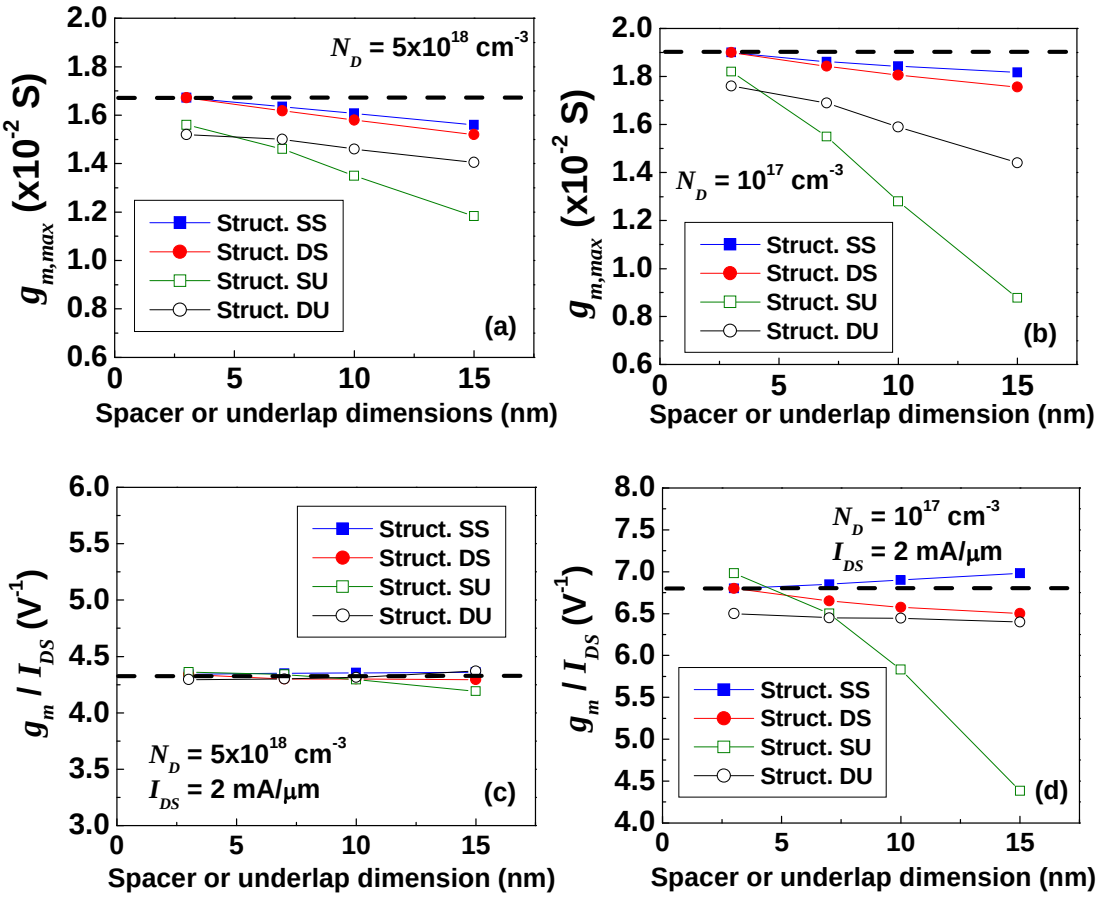


Figure 3.3 The trend of $g_{m,\text{max}}$ with spacer or underlap dimension (a) at N_D = 5×10^{18} cm^{-3} and (b) at N_D = 10^{17} cm^{-3}, and the trend of g_m/I_{DS} (under constant drain current) at (c) at N_D = 5×10^{18} cm^{-3} and (d) at N_D = 10^{17} cm^{-3}. The dashed line indicates the baseline device value.

g_m/I_{DS} is an important analog metric indicating the balance between power and efficiency. In Fig. 3.3(c), g_m/I_{DS} is similar for different structures under a constant current bias. The explanation is as follows. For a short channel, velocity-saturated device with R_S, the drain current equation can be formulated as:

$$I_{DS}/Z = C_{ox}(V_{GS} - I_{DS}R_S - V_t)v_{sat} \tag{2}$$

where v_{sat} is saturated velocity; Z is device width and $I_{DS}R_S$ represents the additional voltage drop at the source due to the source parasitic resistance. I_{DS} can be organized as:

$$I_{DS} = \frac{C_{ox}(V_{GS} - V_t)v_{sat}}{1/Z + C_{ox}v_{sat}R_S} \tag{3}$$

g_m is the derivative of drain current with respect to gate voltage (Eq. (4)). g_m/I_{DS} is thus expressed as Eq. (5).

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{C_{ox}v_{sat}}{1/Z + C_{ox}v_{sat}R_S} - \frac{C_{ox}^2(V_{GS} - V_t)v_{sat}^2(\partial R_S/\partial V_{GS})}{(1/Z + C_{ox}v_{sat}R_S)^2} \tag{4}$$

$$\frac{g_m}{I_{DS}} = \frac{1}{V_{GS} - V_t} - \frac{C_{ox}v_{sat}(\partial R_S/\partial V_{GS})}{1/Z + C_{ox}v_{sat}R_S} \tag{5}$$

To the first order, R_S can be assumed to be independent of gate voltage ($\partial R_S/\partial V_{GS} = 0$) so g_m/I_{DS} is inversely proportional to the gate overdrive ($V_{GT} = V_{GS} - V_t$) according to Eq. (5). At the $g_{m,\max}$ bias points, V_{GT} is found to be relatively constant for various spacer thicknesses and underlap lengths in different structures (Figs. 3.4(a)-(b)). At the constant current bias, however, V_{GT} varies in different structures due to the constraint of delivering the same drain current. As shown in Figs.

3.4(c)-(d), a larger V_{GT} is indeed required for larger parasitic resistance and the magnitude of V_{GT} increase is even larger with a lower channel doping. This explains the almost constant or slight g_m/I_{DS} decrease for all structures in Fig. 3.3(c) and a larger g_m/I_{DS} decrease in Structures SU, DS and DU in Fig. 3.3(d). The g_m/I_{DS} decrease is especially pronounced in Structure SU with lower channel doping (Fig. 3.3(d)) primarily due to the significant increase in V_{GT} (Fig. 3.4(d)).

Although gate overdrive qualitatively explains the decreasing g_m/I_{DS} trends above, it does not, however, clarifies the slight g_m/I_{DS} increase of Structure SS with low channel doping (Fig. 3.3(d)). When the second-order effect is considered, R_S is no longer independent of V_{GS} due to gate modulation of the underlap region and source n^+ region across the spacer. Since $\partial R_S/\partial V_{GS} < 0$ at the bias points and its change in magnitude increases with the spacer thickness, the resultant g_m/I_{DS} is thus slightly increased in Structure SS with lower channel doping.

To summarize, $g_{m,\max}$ and g_m/I_{DS} in general decrease below the baseline due to the increase of parasitic resistance from thicker spacer or longer underlap.

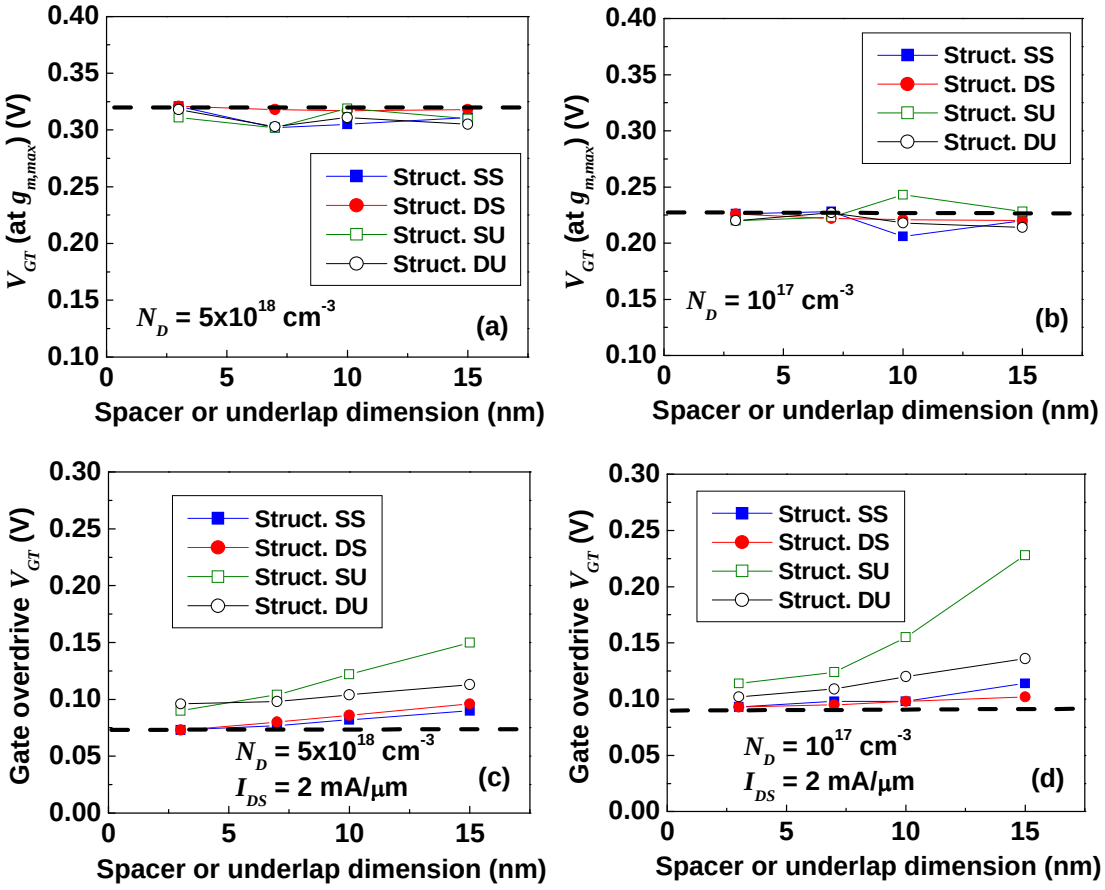


Figure 3.4 The trend of V_{GT} (at $g_{m,max}$ point) with spacer or underlap dimension (a) at N_D = 5×10^{18} cm^{-3} and (b) at N_D = 10^{17} cm^{-3}, and the trend of V_{GT} (under constant drain current) at (c) at N_D = 5×10^{18} cm^{-3} and (d) at N_D = 10^{17} cm^{-3}. The dashed line indicates the baseline device value.

3.3.2 Cutoff Frequency

Cutoff frequency (f_T) depends on transconductance and total gate capacitance (C_{GG}), as expressed in Eq. (6).

$$f_T = \frac{g_m}{2\pi C_{GG}} = \frac{g_m}{2\pi (C_{GG,\text{int}} + C_{GG,para})} \tag{6}$$

where C_{GG} consists of intrinsic ($C_{GG,\text{int}}$) and parasitic ($C_{GG,para}$) components. (Note that the parasitic fringing gate capacitance of an underlap structure has been modeled before [21].) f_T can

be improved in general through parasitic resistance and/or capacitance reduction. In Fig. 3.5(a), for Structures SS and DS with thicker spacers, $f_{T,peak}$ initially increases above the baseline device value due to the reduction of parasitic capacitance and then decreases due to the increase of $R_S(n^+)$ and $R_D(n^+)$. For a device biased at the saturation region, gate-to-source capacitance (C_{GS}) dominates C_{GG}. So the initial parasitic capacitance reduction is more pronounced in Structure SS and thus the higher $f_{T,peak}$.

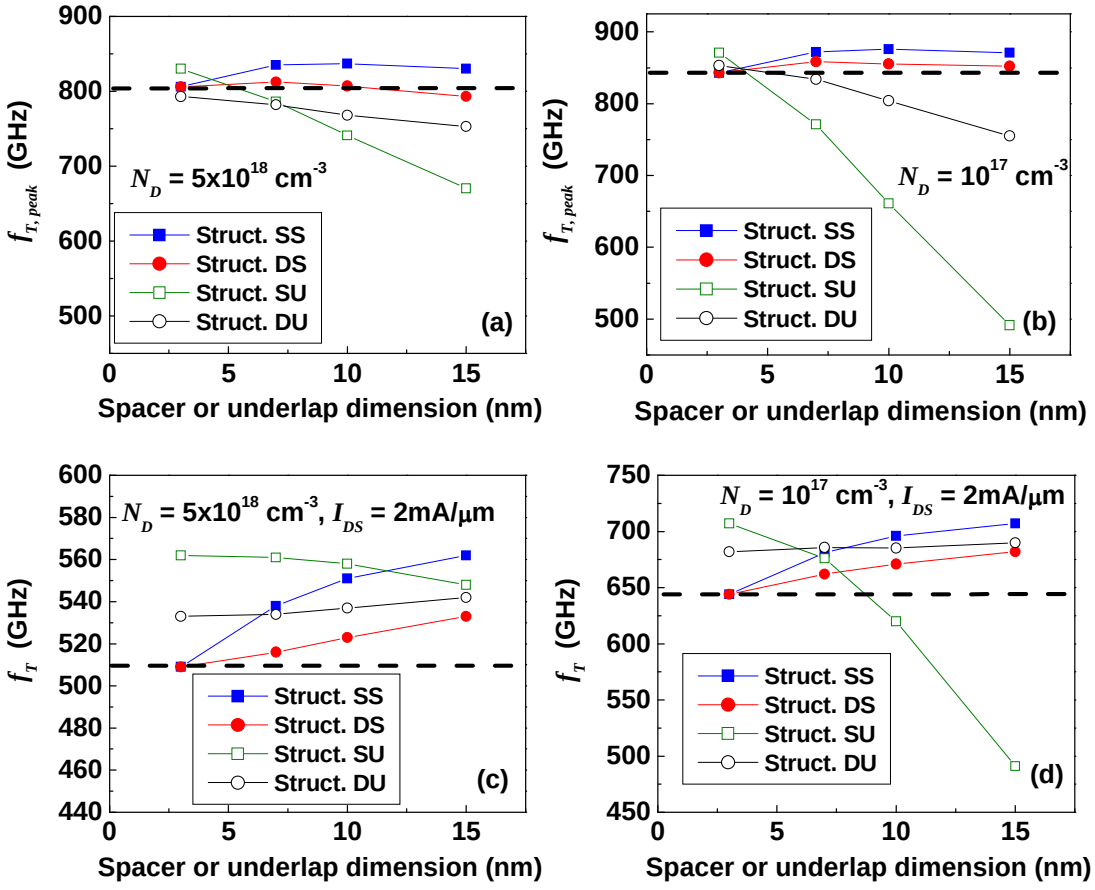


Figure 3.5 The trend of $f_{T,peak}$ with spacer or underlap dimension (a) at $N_D = 5\times10^{18}$ cm^{-3} and (b) at $N_D = 10^{17}$ cm^{-3}, and the trend of f_T (under constant drain current) at (c) at $N_D = 5\times10^{18}$ cm^{-3} and (d) at $N_D = 10^{17}$ cm^{-3}. The dashed line indicates the baseline device value.

For Structures SU and DU, $f_{T,peak}$ monotonically decreases due to the increase of R_S(underlap) and R_D(underlap), respectively. The $f_{T,peak}$ trend follows the $g_{m,\max}$ trend and the impact of R_S(underlap) is observed to be greater than that of R_D(underlap). Further, lower channel doping leads to a higher underlap resistance and therefore, a more significant $f_{T,peak}$ degradation, as shown in Fig. 3.5(b) compared to Fig. 3.5(a). When the source underlap is ≤ 5 nm, Structure SU has its $f_{T,peak}$ even higher than the baseline in both Figs. 3.5(a)-(b) mostly due to a big C_{GS} reduction (with a 15 nm source side spacer).

Alternatively, for the constant current biasing, f_T shows a different trend. In Fig. 3.5(c), Structures SS and DS have increased f_T due to the reduction of parasitic capacitance since g_m/I_{DS} (the same trend as g_m since I_{DS} is constant) remains almost constant, as shown in Fig. 3.3(c). Structure SU shows a slight f_T decrease as its g_m/I_{DS} reduces slightly with larger underlap. Structure DU has a slight f_T increase due to the slight reduction of parasitic gate-to-drain capacitance ($C_{GD,para}$) as the distance between n^+ extensions to the gate edge is increased. All structures show an f_T improvement compared with the baseline device. In the lower channel doping case (Fig. 3.5(d)), the trend is similar but Structure SU has a significant f_T drop below the baseline at larger underlap length due to the pronounced g_m/I_{DS} drop.

In brief, f_T, can be improved with thickened source/drain spacer under both bias schemes mainly due to the reduction of parasitic capacitance.

3.3.3 Maximum Oscillation Frequency

Maximum oscillation frequency ($f_{\max}$) depends on f_T, gate resistance (R_G) and drain side capacitance (C_{GD}), as shown in Eq. 7. In this work, R_G is assumed constant so $f_{\max}$ is dependent on f_T and C_{GD} and given by

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_G C_{GD}}} \tag{7}$$

In Fig. 3.6(a), $f_{\max,peak}$ follows its $f_{T,peak}$ trend in Structure SS. Structure DS has improved $f_{\max,peak}$ due to reduced parasitic drain side capacitance ($C_{GD,para}$). $f_{\max,peak}$ degrades in Structure SU due to increased series resistance (the same trend as $f_{T,peak}$). $f_{\max,peak}$ in Structure DU is high and increases slightly also due to the reduction of $C_{GD,para}$ with increased underlap although its $f_{T,peak}$ degrades due to increased R_S(underlap). As channel doping is reduced (Fig. 3.6(b)), the intrinsic C_{GD} ($C_{GD,\text{int}}$) is also reduced. Since the S/D doping is unchanged, the fraction of $C_{GD,para}$ over the total C_{GD} gets higher in Structures DS and DU with lower channel doping. As a result, the $f_{\max,peak}$ improvement in Structures DS and DU over the baseline device becomes significant (~ 33% in Fig. 3.6(b)).

For $f_{\max}$ biased at constant current, Structures SS, DS and DU follow the $f_{\max,peak}$ trend (Figs. 3.6(c)-(d)). In Structure SU, there is less $f_{\max}$ degradation compared with its $f_{\max,peak}$ trend owing to the less degraded f_T (by constant current) than $f_{T,peak}$.

To summarize, increasing drain side spacer/underlap effectively improves f_{max} over the baseline device value.

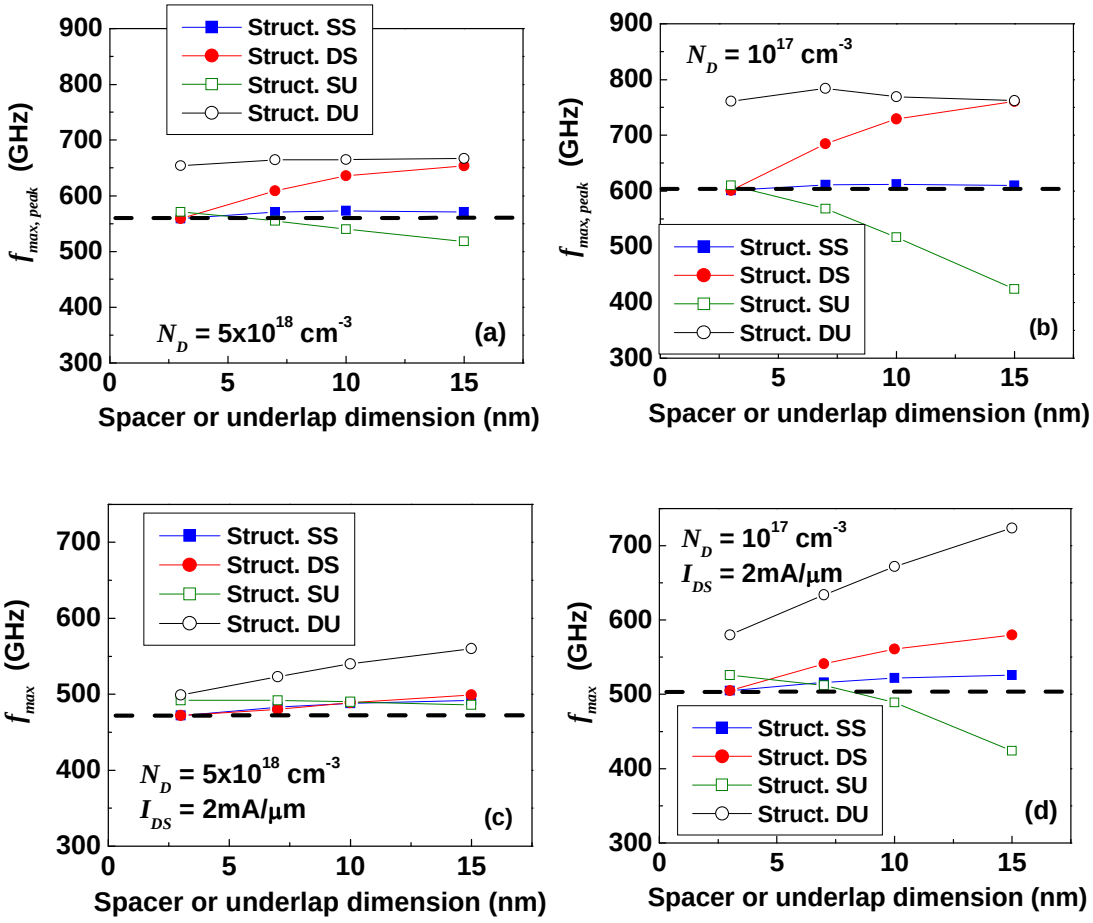


Figure 3.6 The trend of $f_{max,peak}$ with spacer or underlap dimension (a) at N_D = 5×10^{18} cm^{-3} and (b) at N_D = 10^{17} cm^{-3}, and the trend of f_{max} (under constant drain current) (c) at N_D = 5×10^{18} cm^{-3} and (d) at N_D = 10^{17} cm^{-3}. The dashed line indicates the baseline device value.

3.3.4 Output Resistance

Output resistance depends on the biasing current (gate overdrive), SCE, and parasitic resistance. As the gate overdrive increases, channel length modulation of a device would degrade its R_{out}. Also, parasitic resistance increases the overall R_{out} through:

$$\frac{1}{R_{out}} = g_d = \frac{g_{d,\text{int}}}{1 + g_{m,\text{int}} R_S + g_{d,\text{int}} (R_S + R_D)} \tag{8}$$

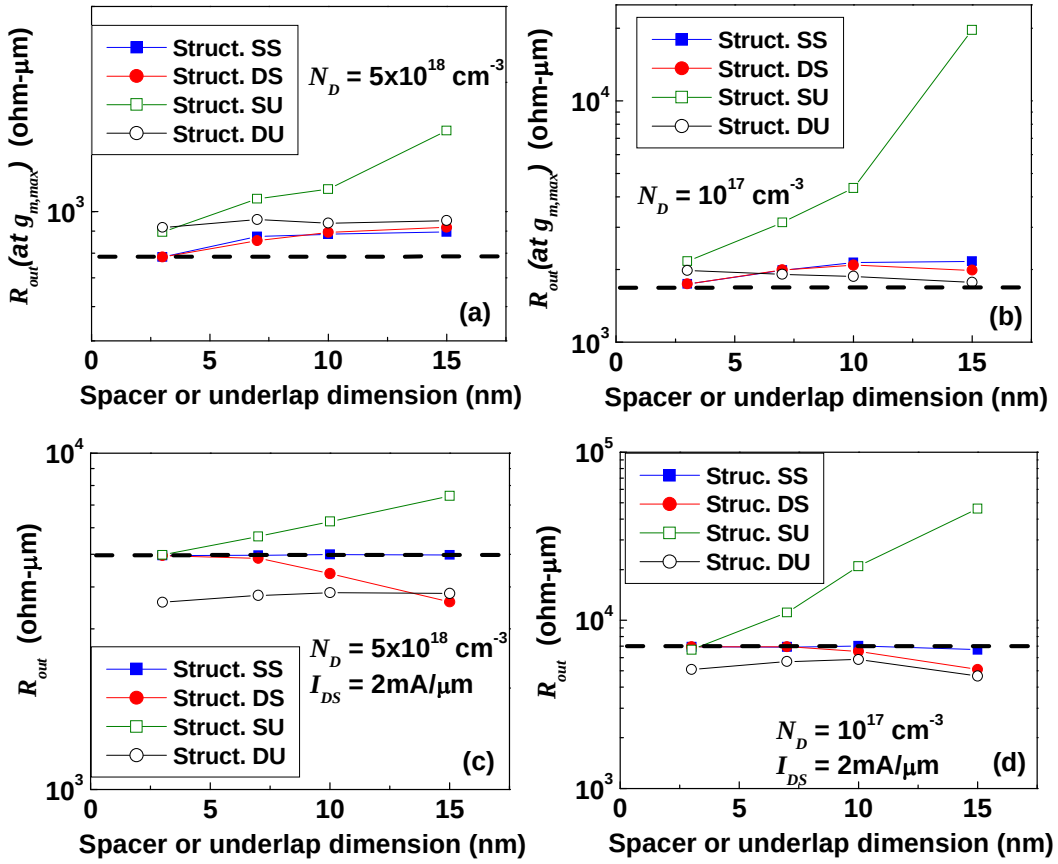


Figure 3.7 The trend of R_{out} (biased at $g_{m,\max}$ point) with spacer or underlap dimension (a) at N_D = 5×10^{18} cm^{-3} and (b) at N_D = 10^{17} cm^{-3}, and the trend of R_{out} (under constant drain current) (c) at N_D = 5×10^{18} cm^{-3} and (d) at N_D = 10^{17} cm^{-3}. The dashed line indicates the baseline device value.

In Fig. 3.7(a), Structures SS and DS show slight R_{out} increase due to the increase of parasitic resistance $R_S(n^+)$ and $R_D(n^+)$. For Structures SU and DU, the increase of source side underlap improves R_{out} while the increase of drain side underlap does not change R_{out}. The same trend is observed in the lower channel doping case (Fig. 3.7(b)) as explained below. Based on the charge sheet approximation, on-state current is proportional to the charge density at the "virtual source" (i.e., at the location of the top of the energy barrier between the source and channel), given by [22]:

$$I_{DS} / Z = Q_0 v_0 \tag{9}$$

where Q_0 and v_0 are the charge density and carrier velocity, respectively, at the virtual source point; Z is the device width. The output resistance can be obtained as the derivative of drain current with respect to drain voltage:

$$\frac{1}{R_{out}} = g_d = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{\partial Q_0}{\partial V_{DS}} v_0 + Q_0 \frac{\partial v_0}{\partial V_{DS}} \tag{10}$$

At the top of the barrier, the charge density Q_0 is almost independent of drain voltage when the device is biased in the saturation region [22]-[23] so the first term on the right hand side of Eq. (10) can be neglected.

At the $g_{m,\max}$ bias point, the band diagrams extracted along the surface and middle of the channel in Structure SU are shown in Fig. 3.8(a)-(d) for source underlap equal to 3, 7, 10, 15 nm, respectively. As observed, at 3 nm source underlap, although there is no barrier for the channel

surface, the barrier position of the channel middle corresponds to the gate edge, which is considered as the virtual source point. The barrier of the channel surface starts to become more pronounced (but somewhat compromised by resistive drop in the source) with the increase of the source underlap and the peak position shifts away from the gate edge. Further, the barrier peak position of the channel surface also coincides with that of the channel middle. As the barrier peak shifts away, the resultant Q_0 is found decreased due to the weaker gate coupling (Q_0 is extracted by integrating electron concentration along the direction perpendicular to the semiconductor/dielectric interface. The extracted Q_0 is equal to 6.5×10^{12}, 5.9×10^{12}, 4.5×10^{12}, 2.7×10^{12} C/cm^2 for 3, 7, 10, 15 nm source underlap, respectively). On the other hand, the band diagram of 3 nm and 15 nm drain underlap in Structure DU are shown in Fig. 3.9(a)-(b), respectively. The band diagram near the source/channel interface in Fig. 3.9(a)-(b) are similar to that in Fig. 3.8(a) as these three cases all have 3 nm source underlap. In other words, the virtual source position is at the gate edge regardless of the drain underlap increase. The extracted Q_0 does not change significantly with the drain underlap increase (Q_0 equal to 4×10^{12} and 3.7×10^{12} C/cm^2 for 3 nm and 15 nm drain underlap, respectively). Moreover, any change in $\partial v_0/\partial V_{DS}$ due to larger source/drain underlap is found to be minimal. Therefore, to the first order, the output resistance is determined by the charge density at the virtual source. Intuitively, the increase of drain underlap is expected to reduce SCE (e.g., Drain-Induced Barrier Lowering (DIBL)) and

hence, improve R_{out}. DIBL effect is confirmed by the I_{DS}-V_{GS} curve with V_{DS} = 0.05 V and 0.5 V at 3 nm and 15 nm drain underlap (Fig. 3.10(a)-(b)). The extracted DIBL values are 47 and 35 mV/V for 3 nm and 15 nm drain underlap, respectively. The impact of DIBL is not significant given the good gate control of the DG structure and thin high-κ dielectric. (The impact of DIBL is not significant with source underlap increase, either, as shown by the I_{DS}-V_{GS} curves of 3 nm and 15 nm source underlap in Structure SU in Fig. 3.10(c)-(d). The extracted DIBL values are 44 and 31 mV/V for 3 nm and 15 nm source underlap, respectively).

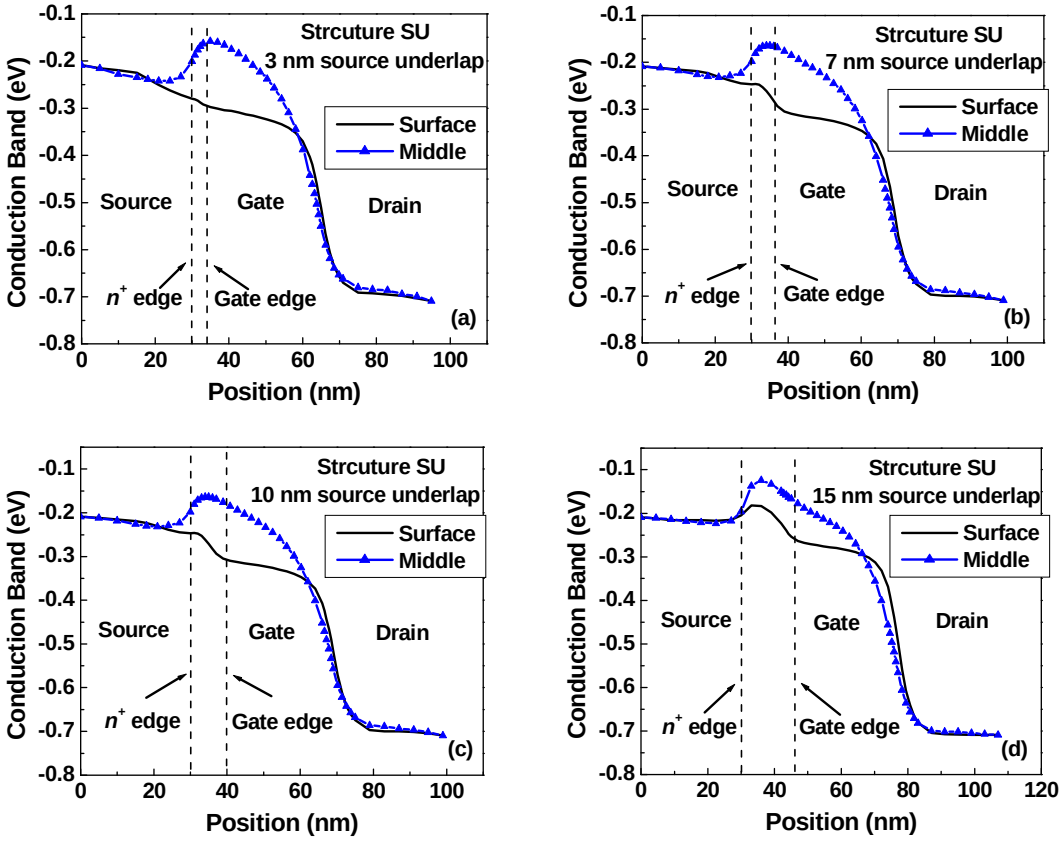


Figure 3.8 Conduction band diagram at the $g_{m,\max}$ bias point of Structure SU with source underlap (a) 3nm (b) 7 nm (c) 10 nm and (d) 15 nm. N_D = 10^{17} cm^{-3}. The bands extracted along the surface and middle of the channel are shown. The dashed lines indicate source n^+ edge and gate edge.

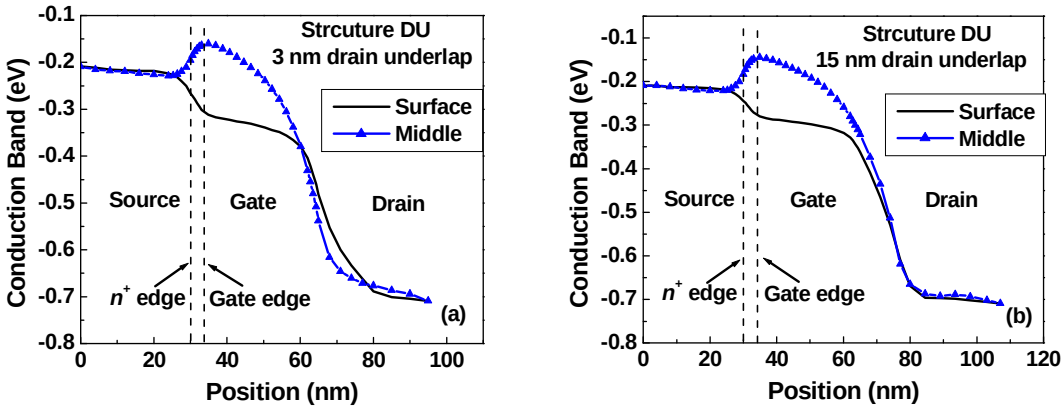


Figure 3.9 Conduction band diagram at the $g_{m,\max}$ bias point of Structure DU with drain underlap (a) 3nm (b) 15 nm. $N_D = 10^{17}$ cm^{-3}. The bands extracted along the surface and middle of the channel are shown. The dashed lines indicate source n^+ edge and gate edge.

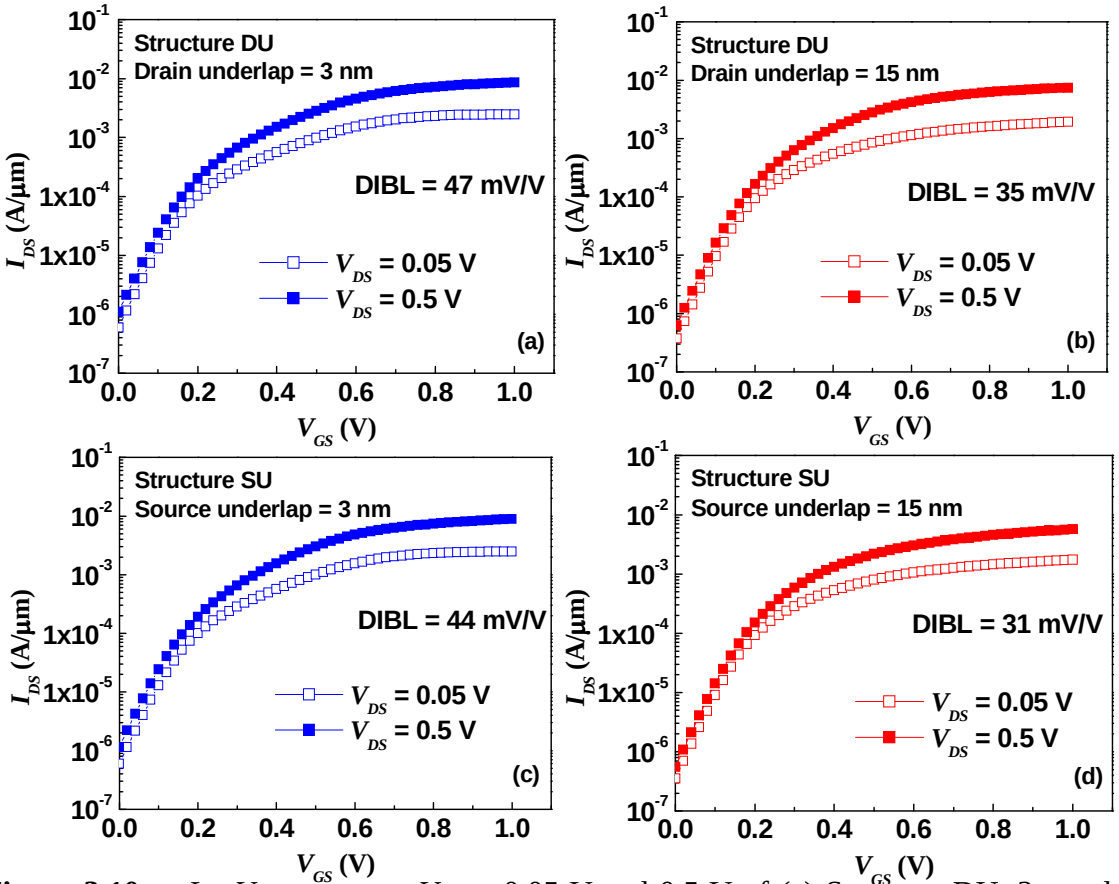


Figure 3.10 I_{DS}-V_{GS} curves at V_{DS} = 0.05 V and 0.5 V of (a) Structure DU, 3 nm drain underlap, (b) Structure DU, 15 nm drain underlap, (c) Structure SU, 3 nm source underlap, (d) Structure SU, 15 nm source underlap. $N_D = 10^{17}$ cm^{-3}. DIBL is found not significant with both drain and source underlap increase.

For R_{out} (by constant current), the trend is similar to R_{out} (at $g_{m,\max}$) except for Structures SS and DS (Figs. 3.7(c)-(d)), which show an invariant or reduced R_{out} trend as V_{GT} is increased for a thicker spacer such that R_{out} is reduced.

To summarize, R_{out} can be effectively increased by increasing the source underlap primarily attributed to the shift of the virtual source position away from the gate edge.

3.3.5 Intrinsic Gain

Intrinsic gain is obtained through $g_m \times R_{out}$. Notably, Structure SU has an improved gain over the baseline device for both channel doping concentrations and biasing points (Figs. 3.11(a)-(d)) due to its large R_{out}. Structures DS and DU alternatively show a reduced intrinsic gain (under constant drain current) in Figs. 3.11(c)-(d) owing to their smaller R_{out}.

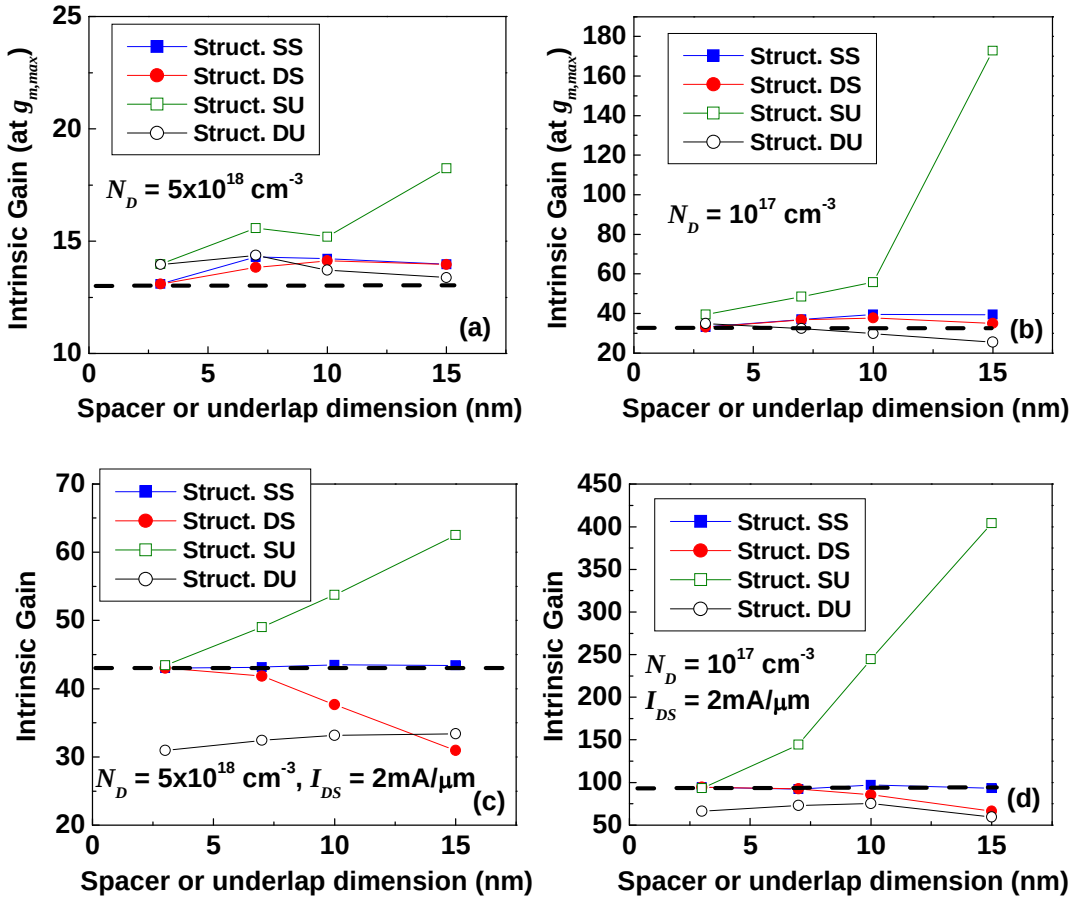


Figure 3.11 The trend of intrinsic gain (biased at $g_{m,\max}$ point) with spacer or underlap dimension (a) at $N_D = 5\times10^{18}$ cm^{-3} and (b) at $N_D = 10^{17}$ cm^{-3}, and the trend of intrinsic gain (under constant drain current) (c) at $N_D = 5\times10^{18}$ cm^{-3} and (d) at $N_D = 10^{17}$ cm^{-3}. The dashed line indicates the baseline device value.

3.3.6 Design and Optimization Guidelines

Compared with the baseline device, different structures offer improvement in different metrics. Note that the improvement is bias-dependent as biasing at the $g_{m,\max}$ point or at a constant current may show different behaviors. Here, we summarize the improved metrics *in*

common for two biasing schemes that each structure may offer, as shown in Table 3.2. Both high and low channel doping devices show similar behaviors. Structures SS and DS have improved f_T and/or f_{max} performance, primarily through the parasitic capacitance reduction with thicker spacer thickness. Structure SU shows increased R_{out} and gain as the top of the barrier is shifted away from the gate edge with larger source underlap. Structure DU has improved f_{max} due to the reduced parasitic capacitance C_{GD} with larger drain underlap. In brief, by asymmetric S/D spacer/underlap design, optimization of different analog/RF metrics can be achieved.

In addition, the analog/RF metrics that are more sensitive to process variation in either the source/drain spacer thickness or underlap length control can also be identified. g_m, R_{out}, intrinsic gain, and f_T are found to be more sensitive to the source side underlap variation. f_{max} is also more sensitive to both the drain side spacer and underlap variation. These process variations should thus be minimized if the respective analog/RF metrics are the key design goals.

TABLE 3.2

IMPROVED METRICS IN COMMON FOR TWO BIASING SCHEMES OF STRUCTURES SS, DS, SU, AND DU COMPARED WITH THE BASELINE DEVICE

Structure	**Mechanism**	**Channel Doping**	
		5×10^{18} (cm^{-3})	10^{17} (cm^{-3})
SS	Thicker source spacer Reduced C_{GS}	f_T, f_{max}	f_T
DS	Thicker drain spacer Reduced C_{GD}	f_{max}	f_T, f_{max}
SU	Larger source underlap Shifted virtual source	R_{out}, gain	R_{out}, gain
DU	Larger drain underlap Reduced C_{GD}	f_{max}	f_{max}

3.4 Summary

In this chapter, we introduce the VRG process for a vertical DG transistor fabrication. S/D underlap and spacer can be individually tuned by ALD HfO_2 thickness and epitaxial process to facilitate an asymmetric S/D design. Also, we present source/drain parasitics engineering of a GaAs vertical transistor for analog/RF performance optimization. Four different structures, based on various source side and drain side spacer thickness and underlap length, have been analyzed and optimized against different analog/RF metrics. The improved metrics in common for two biasing schemes of different structures have been revealed. Thicker source/drain spacer is

effective for f_T and f_{max} improvement due to the reduction of parasitic capacitance. Increased source side underlap improves output resistance and gain through relocating the virtual source point. Increased drain side underlap improves f_{max} through a parasitic capacitance reduction. These optimizations can be readily implemented through asymmetric source/drain spacer/underlap design in a vertical transistor structure. Finally, the sensitivities of relevant analog/RF metrics to the spacer/underlap process variation have been discussed.

Chapter 4
III-V Multigate Non-Planar Channel Transistor Technology

4.1 Introduction

III-V multigate non-planar channel transistors can be divided into two categories, lateral devices and vertical devices, and these two structures have been reported by some research groups. For lateral devices, Radosavljevic *et al.* demonstrate a tri-gate InGaAs quantum well field effect transistor with high-κ gate dielectric [1]. Due to the narrow fin width (30 nm) and high quality high-κ gate dielectric interface on the InGaAs fin, the device shows superior electrostatic control (steep subthreshold swing and low DIBL) compared with other ultra-thin body planar counterparts. The results show that the III-V multigate architecture is a promising candidate for future low power applications. For vertical devices, Thelander *et al.* report the development of a vertical wrap-gated field-effect transistor based on epitaxially grown InAs nanowires [2]-[3]. The vertical nanowire structure inherently facilitates wrap-gate processing for improved electrostatics. Further, a short gate length can be readily implemented in a vertical

device as the gate length controlled is by the deposited metal thickness rather than the photolithography capability.

In this work, we develop a process technique to fabricate large arrays of lateral III-V multigate non-planar transistors. In our process, GaAs nanowires (NWs) are lithographically patterned and etched on a source epitaxial wafer, and then transferred to another receiving substrate. Although other research groups have reported similar stamping transfer methods before [4]-[9], their methods offer no control of the precise NWs locations and orientation on the substrate surface. On the contrary, we develop a stamping transfer and positioning technique that enables to transfer NWs onto a specific position using a standard VLSI cleanroom tool, contact aligner. This technique facilitates a device-level co-integration of III-V NW transistors with close proximity and overlay accuracy. The experimental details will be discussed in Section 4.2.

On the other hand, for a vertical III-V multigate transistor, we propose to incorporate graphene as a gate electrode to implement an ultrashort gate length and a low gate series resistance. We explore the process flow for the device fabrication and discuss two critical components in the structure, graphene-high-κ interface and metal-graphene gate contact resistance. The details will be shown in Section 4.3.

4.2 Lateral III-V Multigate Non-Planar Transistor Fabrication

Fig. 4.1 shows the structure of a lateral III-V multigate non-planar channel transistor. Aligned GaAs NWs are transferred to a SiO_2-coated substrate (mimicked as an inter-layer dielectric) and wrapped by the gate electrode on three sides. In this work, stamping transfer technique is the key technology for the lateral III-V multigate non-planar channel transistor fabrication. This section discusses the NW stamping transfer method, NW layout design and the NW positioning technique, etc.

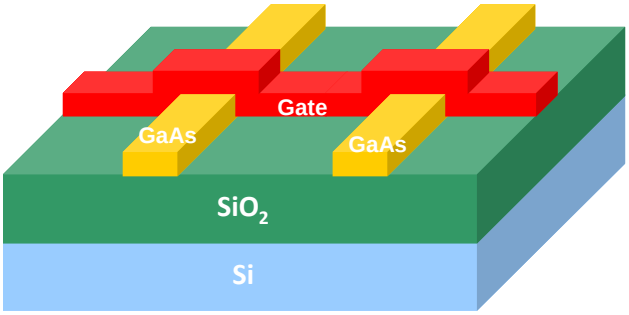


Figure 4.1 The illustration showing the aligned NWs on the SiO_2 (mimicked as an inter-layer dielectric) with the wrapped gate electrode on three sides of the NWs.

4.2.1 Motivation of developing stamping transfer technique

As mentioned in chapter 1, current chemical synthesis technology yields no control over the precise assembly position of the epitaxially grown NWs (bottom up methods). Alternatively, our NW stamping transfer technique possesses several advantages. First of all, by nanolithographic patterning, NW arrays are picked up by a PDMS stamp and transferred onto a

receiving substrate. Large arrays of aligned NWs can thus be obtained. Secondly, stamping transfer technique facilitates device-level co-integration with other materials. And more importantly, the position of the transferred NWs can be precisely controlled on the substrate surface using a VLSI standard cleanroom tool.

4.2.2 Source Wafer Epitaxial Layer Design

Based on the stamping transfer technique, we briefly discuss the epitaxial layer design in the source wafer. The source material is GaAs (active layer). Several issues need to be considered regarding the choice of the sacrificial layer (underneath the active layer) in the epitaxial layer design. First, wet etching of the sacrificial layer is demanded in order to form undercuts for the subsequent NW pickup. Also, the sacrificial layer wet etching needs to be selective to GaAs. Further, lattice constant matching between GaAs and the sacrificial layer is also a concern.

In this work, 80% aluminum composition $Al_{0.8}Ga_{0.2}As$ layer is used as the sacrificial layer due to it wet etching feasibility and the etching selectivity against GaAs. Note that wet etching of AlGaAs layer is aluminum-concentration-dependent. For aluminum composition less than 50%, AlGaAs can be etched by a mixture of citric acid and hydrogen peroxide, which therefore has no selectivity over GaAs layer. Alternatively, for aluminum composition higher

than 70%, the etching by citric acid and hydrogen peroxide stops but the film starts to be etched by diluted BOE. BOE does not etch GaAs so the AlGaAs etching is selective. Therefore, in this work, we use $Al_{0.8}Ga_{0.2}As$ as the sacrificial layer for the etching selectivity. Also, AlGaAs is lattice matched to GaAs regardless of aluminum composition.

To summarize, the choice of the sacrificial layer $Al_{0.8}Ga_{0.2}As$ in this work is based on the high wet etching selectivity over GaAs. The mixture of citric acid and hydrogen peroxide etches GaAs but not AlGaAs for aluminum > 70%. On the other hand, diluted BOE etches high aluminum AlGaAs but not GaAs.

4.2.3 Process Flow of Stamping Transfer

Our starting material is a GaAs wafer with GaAs / $Al_{0.8}Ga_{0.2}As$ alternating epitaxial layers on the substrate. GaAs layers are 10^{18} cm^{-3} *n*-type doped and 50 nm thick; $Al_{0.8}Ga_{0.2}As$ layers are undoped and 60 nm thick. The purpose of having multiple GaAs / $Al_{0.8}Ga_{0.2}As$ epitaxial layers is to facilitate the re-use of the wafer. The process flow is shown as follows.

(a) Start with a GaAs source wafer (Fig. 4.2(a)).

(b) Perform E-beam lithography followed by PMMA development in MIBK : IPA = 1 : 4 for 45 sec. Rinse the sample with IPA (Fig. 4.2 (b)).

(c) Dip the sample in diluted HCl solution (HCl : H_2O = 1 : 5) for 30 sec to remove GaAs

native oxide before GaAs etching,. The removal of GaAs native oxide ensures a subsequent uniform GaAs etching. Then etch GaAs by citric acid mixed with hydrogen peroxide (citric acid : H_2O_2 = 20 : 1) for 22 sec. The etching is selective to the underlying $Al_{0.8}Ga_{0.2}As$ layer (Fig. 4.2 (c)).

(d) Remove PMMA by acetone (Fig. 4.2 (d)).

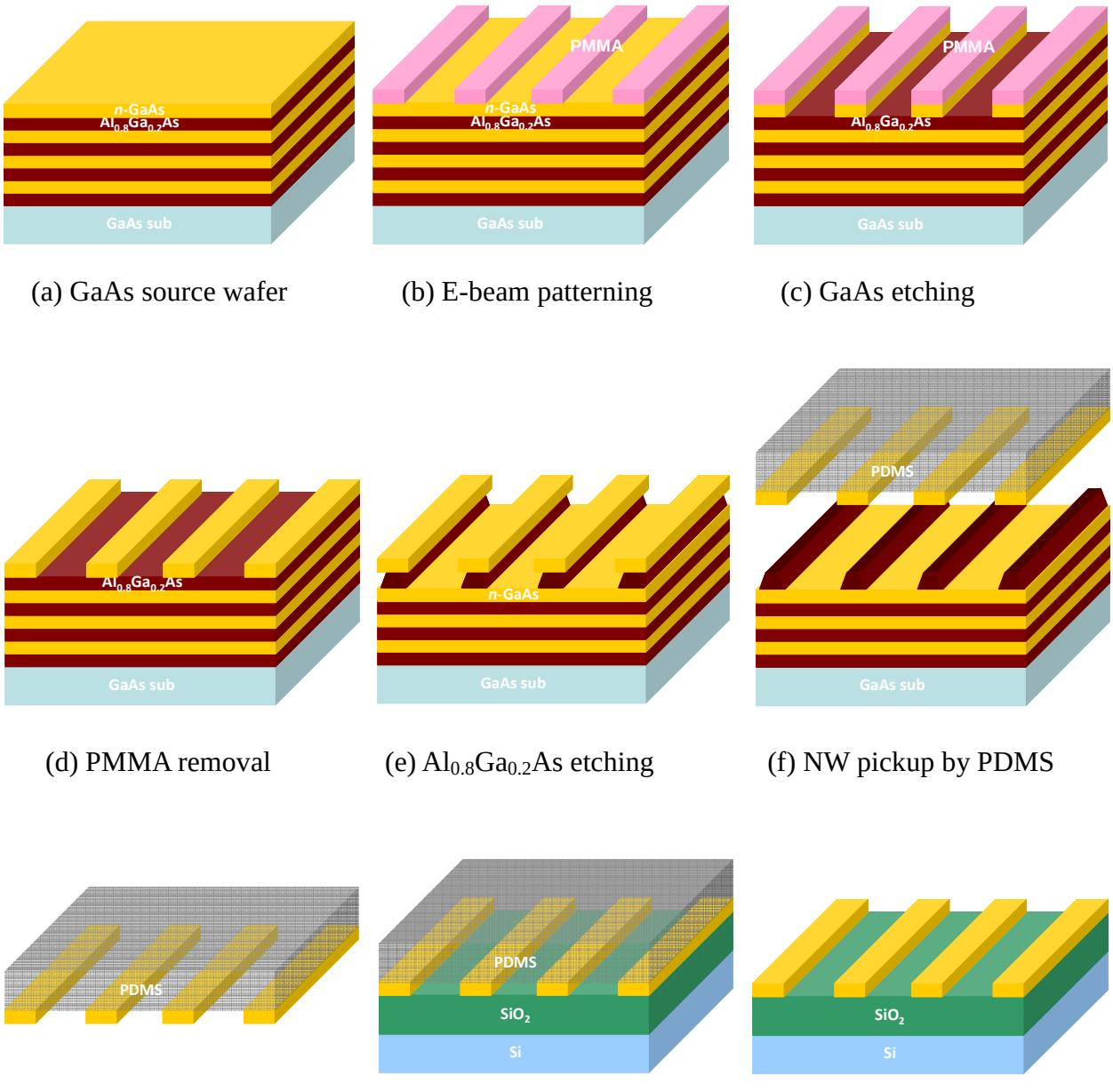
(e) Etch the $Al_{0.8}Ga_{0.2}As$ layer by diluted BOE (BOE : H_2O = 1 : 5) solution to create a undercut. This wet etching step is critical for a successful GaAs NW pickup as an excessive undercut leads to NW bending while an insufficient undercut lowers the yield of the pickup process. The wet etching time needs to be optimized for different GaAs dimensions (Fig. 4.2 (e)).

(f) Pick up GaAs NWs by a PDMS stamp (Fig. 4.2 (f)).

(g) Dip the PDMS stamp into diluted BOE (BOE : H_2O = 1 : 5) solution to remove $Al_{0.8}Ga_{0.2}As$ residues on the backside of NWs. Then dip the PDMS stamp into diluted hydrogen peroxide (H_2O_2 : H_2O= 1 : 5) to form a thin GaAs native oxide layer on the GaAs NWs surfaces. This native oxide formation step is found crucial to improve the transfer yield as the hydrophilicity favors GaAs NWs to be transferred onto a SiO_2 receiving substrate (Fig. 4.2 (g)).

(h) Transfer NWs to the receiving wafer (Fig. 4.2 (h)).

(i) Release the PDMS stamp (Fig. 4.2 (i)).



(a) GaAs source wafer (b) E-beam patterning (c) GaAs etching

(d) PMMA removal (e) $Al_{0.8}Ga_{0.2}As$ etching (f) NW pickup by PDMS

(g) Diluted BOE and H_2O_2 dip (h) Transfer stamping (i) PDMS stamp release

Figure 4.2 The process flow of the stamping transfer technique

4.2.4 III-V Multigate Channel Layout Pattern Design

E-beam lithography was used to pattern NWs on the source wafer for the transfer purposes. E-beam lithography pattern design may be tricky under some circumstances as PMMA is a "negative tone" resist. Our layout pattern design is shown in Fig. 4.3. The filled part is where electron beam writes so the resultant NWs after development and etching will be the empty part. In our design, NW length is 40 µm with different width ranging from 200 nm to 400 nm. There are around 11-14 NWs in each pattern bank. The wider bars on both NW ends are anchors which provide better mechanical support for NWs and reduce the possibility of NW bending during the pickup and transfer process. Since the E-beam writing area is small in our design (only the filled part), it helps save GaAs real estate that needs to be removed each time for NW pickup. Therefore, the same GaAs source wafer can be re-used multiple times.

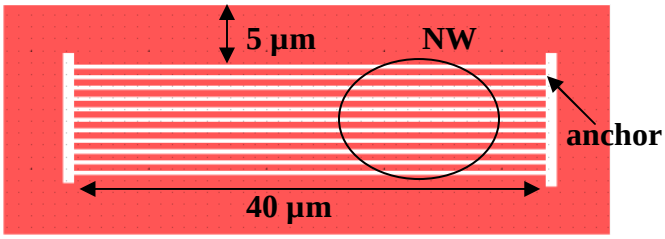


Figure 4.3 E-beam lithography NW pattern design. The white part is where the resultant NWs are after PMMA development and GaAs etching.

4.2.5 E-Beam Lithography Dose Test

We perform E-beam writing dose split to optimize the E-beam dose. Fig. 4.4 (a)-(b) show the E-bean pattern after PMMA development at two different E-beam dose, 700 μC/cm^2 and 800 μC/cm^2, respectively. 700 μC/cm^2 appears to be the optimized dose while 800 μC/cm^2 is over-dosed as the central part of the pattern is blurred.

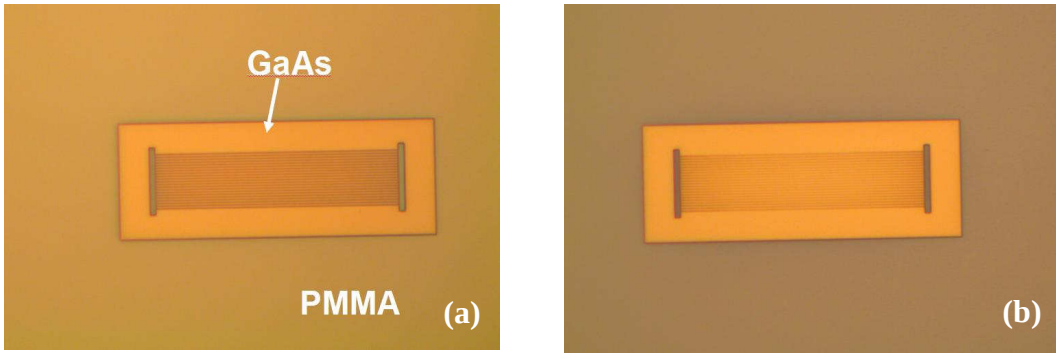


Figure 4.4 Images of E-beam lithography dose test after PMMA development (a) 700 μC/cm^2 is the optimized dose (b) 800 μC/cm^2 is over-dosed, yielding the central part of PMMA strips blurred.

4.2.6 Transfer and Positioning Technique

Our transfer technique enables transfer and alignment of NWs onto a specific position using a commercial contact aligner (Karl Suss). The process is explained as follows. As mentioned before, the patterned NWs are picked up from the source substrate by a PDMS stamp. The PDMS stamp (with to-be-transferred NWs on the surface) is then attached on a glass plate,

which was then loaded onto the mask holder of a contact aligner. The mask holder and the glass plate were then loaded into a contact aligned with the to-be-transferred NWs facing downward. The receiving substrate is subsequently loaded into the contact aligner on the aligner chuck. The whole setup is shown in Fig. 4.5.

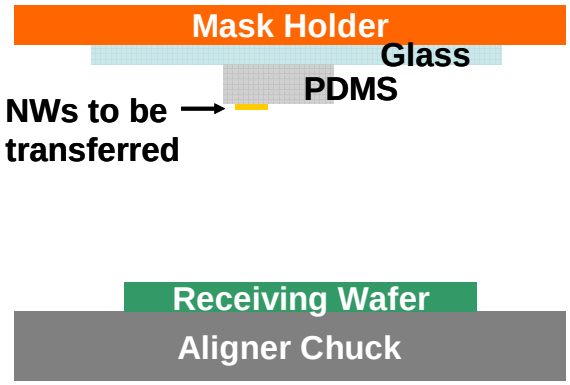


Figure 4.5 The setup of the PDMS stamp, glass plate and the receiving substrate on a contact aligner in our transfer process.

Fig. 4.6 (a) shows the image of attached PDMS stamp underneath the glass plate in the contact aligner. Fig. 4.6 (b) shows the image of the receiving wafer loaded underneath the PDMS stamp.

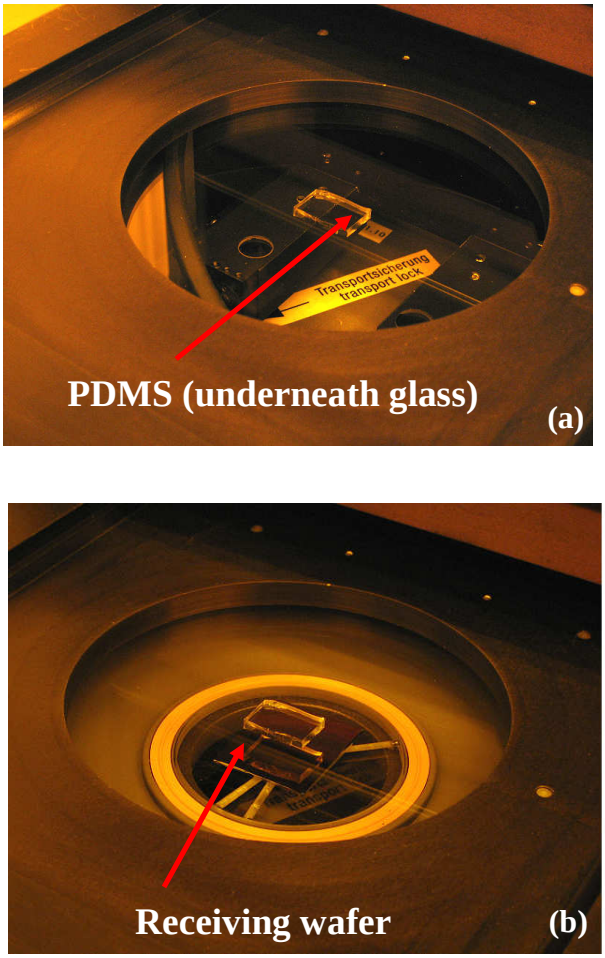


Figure 4.6 Image of (a) PDMS stamp attached underneath the glass (b) the receiving wafer loaded underneath the PDMS stamp in the aligner.

The alignment proceeds in a fashion that we align NW arrays to the target position on the receiving wafer by moving the receiving wafer. Once the alignment is complete, the wafer chuck is raised and the receiving wafer will contact the PDMS to complete the NW transfer process. Through this transfer and positioning technique, the NW transfer is no longer random; instead, the NW position can be well controlled.

The images of transferred GaAs NWs are shown in Fig. 4.7 (a)-(b). In Fig 4.7(a), a 3 × 4 GaAs array is concurrently transferred onto a blanket SiO_2 substrate, which mimics the back end of line (BEOL) dielectric surface, using the contact aligner. This technique demonstrates a high yield, over large area stamping transfer capability that enables III-V NWs co-integration into the BEOL process.

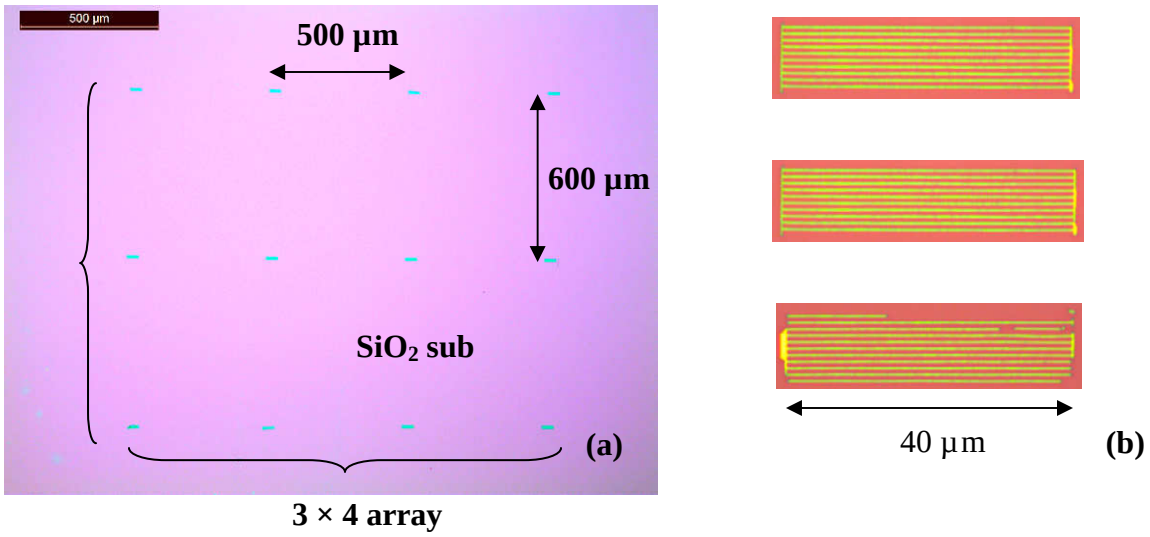


Figure 4.7 (a) 3 × 4 GaAs NW array is successfully transferred onto a SiO_2 substrate concurrently using the aligner (b) Zoomed-in images of some NW in the 3 × 4 array.

Further, device-level co-integration of GaAs and Si on the same substrate can be implemented using our technique. First of all, Si NWs are pre-patterned on a silicon-on-insulator (SOI) substrate by photolithography and anisotropic etching. GaAs NWs are then picked up from the source wafer and transferred to the receiving SOI substrate using our positioning technique.

A large array of GaAs NWs is transferred in proximity to patterned Si NWs arrays, as shown in Fig. 4.8(a). Zoom-in images of aligned GaAs NW to Si NW array are shown in Fig. 4.8(b)-(d). The spacing between Si NW and GaAs NW is found to be around 20 µm and 80 µm in Fig. 4.8(c) and (d), respectively.

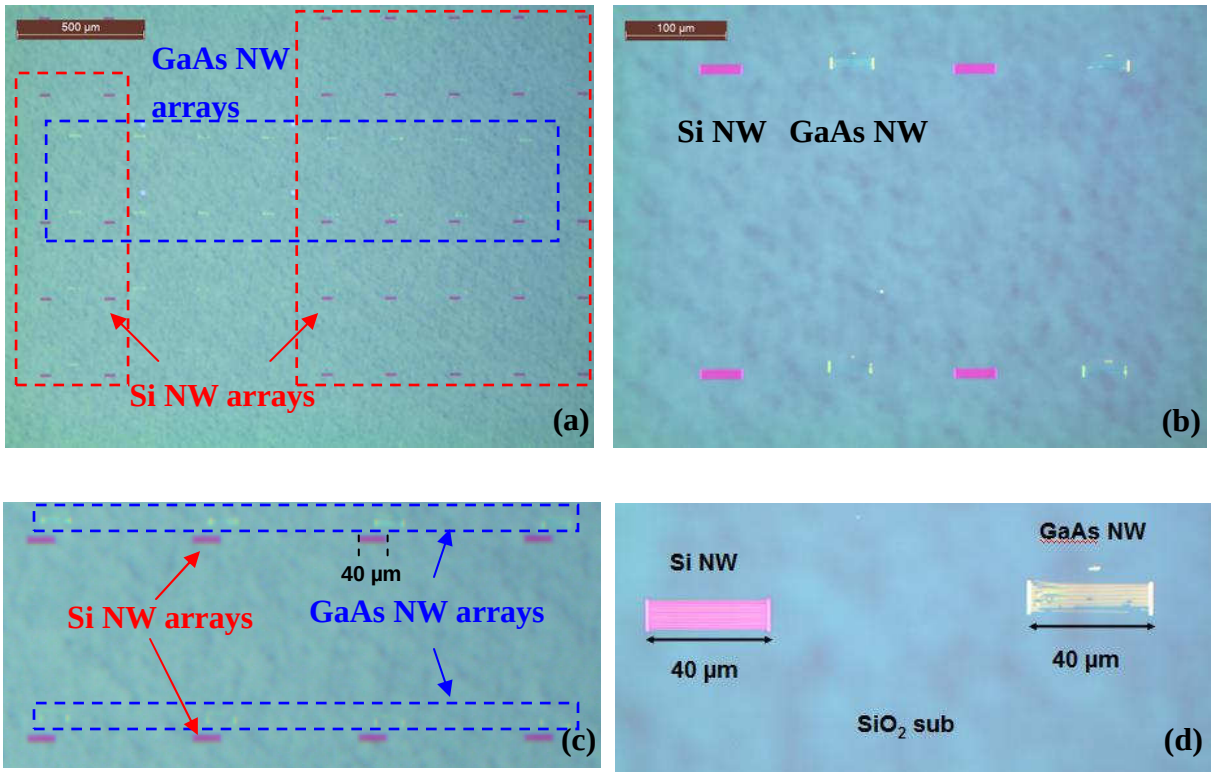


Figure 4.8 (a) A large array of GaAs NWs is successfully transferred in close proximity to Si NW arrays (b) zoomed-in image of the aligned GaAs NWs to Si NWs (c) Si NWs and GaAs NWs are in close proximity. The spacing between Si NWs and GaAs NWs is around 20 µm (d) The spacing between Si NWs and GaAs NWs is around 80 µm.

4.2.7 Device Process Development

A back-gate GaAs NW transistor has been fabricated. The fabrication flow is shown as follows.

(a) Start with a SiO_2-coated Si substrate (Fig. 4.9(a)).

(b) Transfer GaAs NWs onto the SiO_2 substrate using the transfer technique mentioned in Section 4.2 (Fig. 4.9(b)).

(c) Remove GaAs native oxide by diluted HCl (HCl : H_2O = 1 : 5) for 30 sec. Subsequently, 8 nm Al_2O_3 is deposited using ALD process (Fig. 4.9 (c)).

(d) Perform source(S) / drain(D) lithography and remove Al_2O_3 by BOE dip (Fig. 4.9 (d)).

(e) Remove GaAs native oxide by diluted HCl (HCl : H_2O = 1 : 5) for 30 sec. S/D metal is deposited by evaporation (Ni/Ge/Au = 20/20/80 nm), followed by metal liftoff (Fig. 4.9 (e)).

(f) Perform rapid thermal anneal (RTA) 400 ºC 30 sec, followed by additional 425 ºC 30 sec.

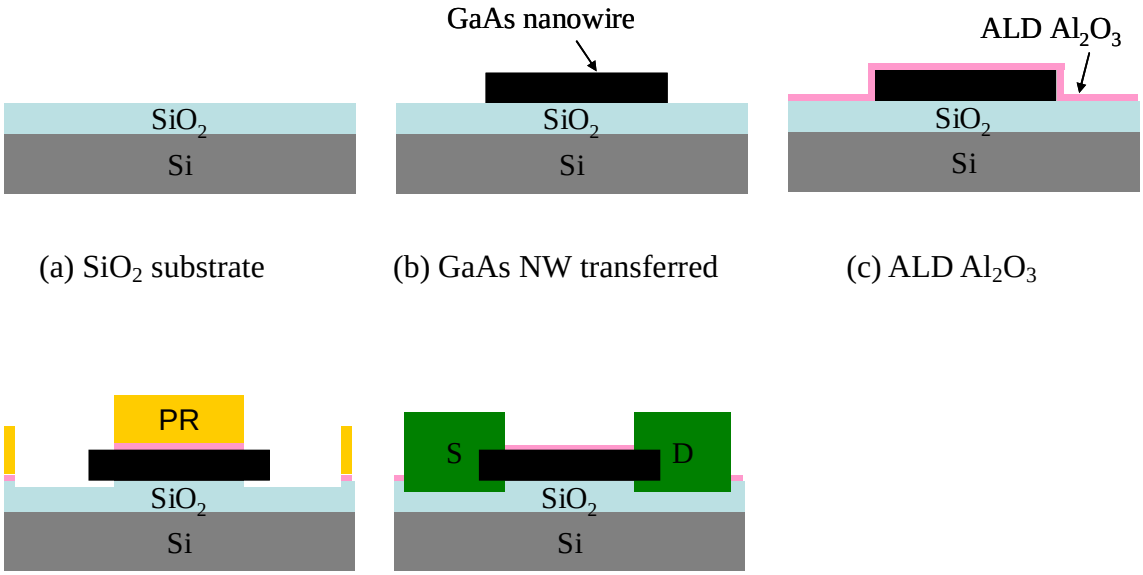


Figure 4.9 Process steps of a GaAs NW transistor fabrication.

The image of the complete device is shown in Fig. 4.10

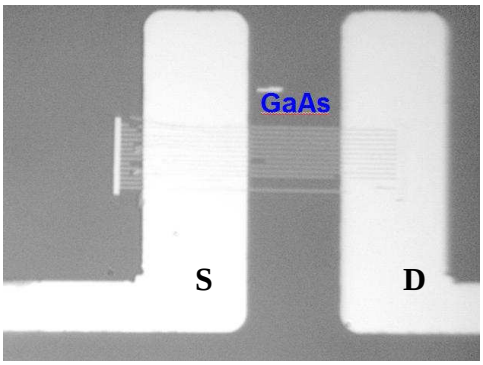


Figure 4.10 Image of the back-gate GaAs NW transistor.

4.2.8 Device Characterization

The back-gate (BG) device has S/D metal spacing 15 μm and total NW width 4 μm (10 NWs with 0.4 μm width of each NW). The bottom SiO_2 is 150 nm thick. The I_{DS}-V_{BG} curve is shown in Fig. 4.11. The back gate does modulate the current around two orders of magnitude but the current level is low. The non-optimized S/D contact may be the performance bottleneck. Also, the interface states extracted from the subthreshold swing is 2.7×10^{13} $cm^{-2}eV^{-1}$, which indicates the back interface between the NW and SiO_2 substrate can be further improved. More experiments are needed to clarify the issues and improve the device performance.

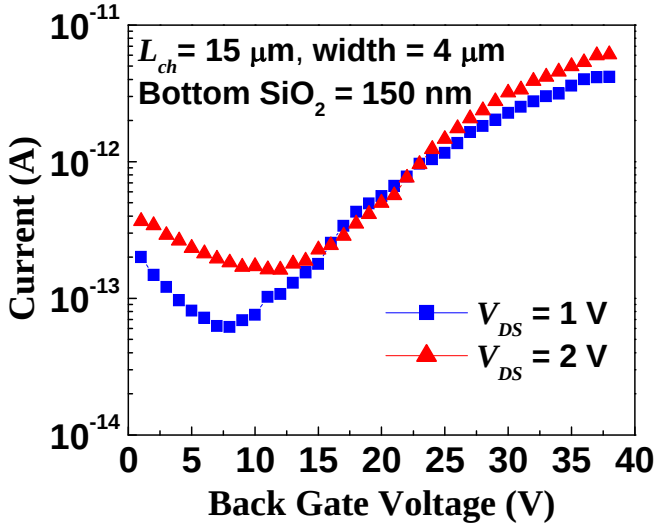


Figure 4.11 I_{DS}-V_{BG} curve of the back-gate GaAs NW transistor.

4.3 Vertical III-V Multigate Transistor Fabrication

4.3.1 Vertical III-V Multigate Transistor Process Flow

As mentioned before, a vertical transistor facilitates a short gate length implementation through the deposition thickness control of gate film. In addition, the source parasitic resistance can be lowered associated with the larger current conduction area. To implement an ultrashort gate length and low gate resistance, we propose to use graphene as the gate electrode in the vertical III-V multigate transistor due to graphene's atomic thickness, superior thermal dissipation, high current conduction capability and free of electromigration problems.

The process flow of a graphene gate electrode vertical transistor is shown as follows.

(h) Start with a GaAs n^+ substrate (Fig. 4.12(a)).

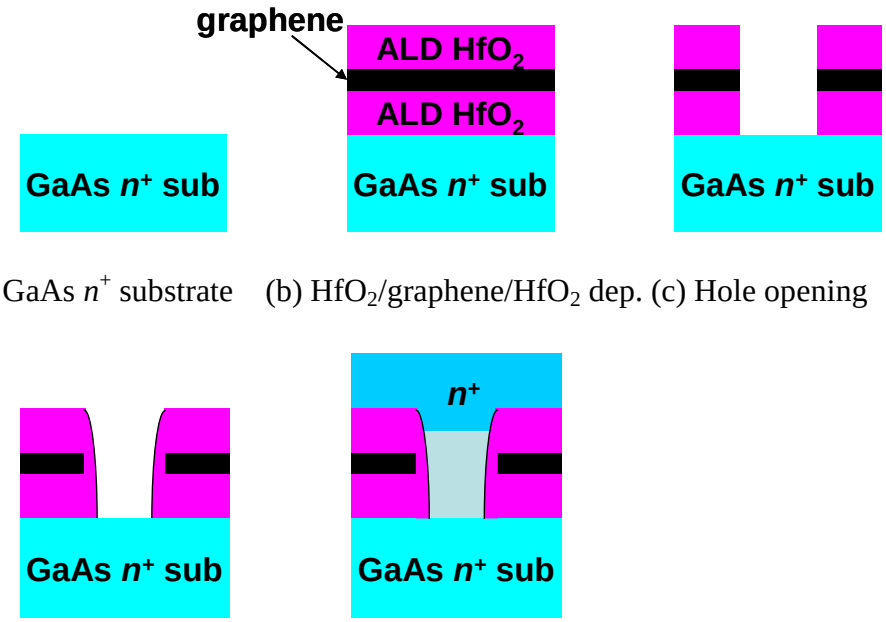
(i) Deposit HfO_2 / graphene / HfO_2 sequentially. HfO_2 deposition is by Atomic Layer Deposition (ALD) process, and graphene deposition can be performed by exfoliation or other chemical synthesis methods (Fig. 4.12(b)).

(j) Perform anisotropic etching to open a trench in the HfO_2 / graphene / HfO_2 film stack (Fig. 4.12(c)).

(k) Deposit HfO_2 and perform anisotropic etching to form a HfO_2 spacer (Fig. 4.12(d)).

(l) Perform GaAs epitaxial growth to form channel and source region of the device. The

doping concentration in the channel and source can be tuned individually during the epitaxial process (Fig. 4.12(e)).



(a) GaAs n^+ substrate (b) HfO_2/graphene/HfO_2 dep. (c) Hole opening

(d) HfO_2 spacer formation (e) GaAs epitaxy

Figure 4.12 Process flow of a graphene gate electrode vertical III-V multigate transistor.

To incorporate graphene as a gate electrode in the vertical III-V multigate transistor, the following two components are crucial. First, the dielectric-graphene interface is paramount so a metal-oxide-graphene (MOG) capacitor is used to probe the oxide-graphene interface properties and the carrier concentration. The details of the graphene-high-κ interface will be discussed in Section 4.3.2. Secondly, a low gate contact resistance is important for device RF characteristics so we analyze contact resistance of metal/graphene interface as it normally becomes a

performance bottleneck. The study of metal/graphene interface will be discussed in Section 4.3.3.

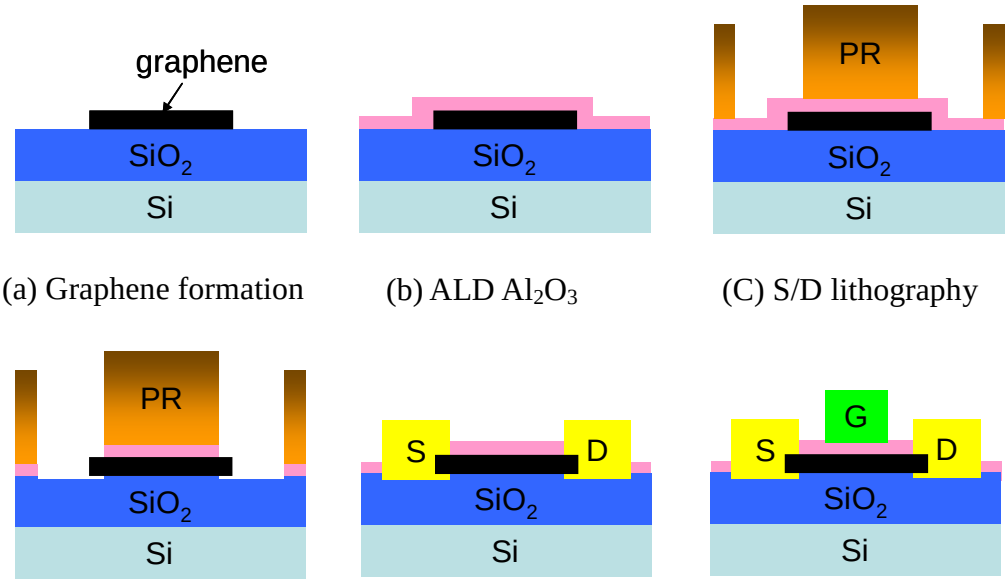
4.3.2 Graphene-High-κ Interface

ALD is commonly used for thin dielectric depositions due to its excellent uniformity and precise thickness control. ALD process on graphene film is, however, challenging as a clean graphene surface is hydrophobic and chemically inert to ALD precursor molecules. In other words, no nucleation site exists on the graphene's honeycomb sp^2 surface on which ALD dielectric can be deposited [11]-[12].

NO_2 functionalization prior to ALD process has yielded successful dielectric depositions on carbon nanotube (CNT) surfaces [13]-[14]. The experimental process flow of NO_2 functionalization is briefly explained as follows. First, Al_2O_3 precursor, trimethylaluminium (TMA, $Al[CH_3]_3$), and NO_2 were alternately pulsed into the ALD chamber (total 50 cycles) at room temperature to form a self-limiting single layer of TMA-NO_2 complex on CNTs surfaces [13]. This TMA-NO_2 complex physically adsorbs on CNTs surfaces and serves as a nucleation site for the subsequent ALD Al_2O_3 depositions. Afterwards, a thin Al_2O_3 layer was deposited with 5-cycle TMA and H_2O alternating pulses (still at room temperature) to cover the TMA-NO_2 complex, preventing it from desorbing [13]. Then the ALD chamber is raised to the process

temperature to start the deposition cycles.

We adopt this NO_2 functionalization technique to deposit dielectric on graphene as well since the unwrapping of CNTs surface is exactly a graphene basal plane without any nucleation sites. The MOG process flow is shown in Fig. 4.13. First of all, graphene films, chemically derived from graphene oxide reduction in hydrazine [15], were spun on a 300 nm thermal SiO_2 substrate followed by NO_2 functionalization steps described above. TMA and NO_2 were alternately pulsed into the ALD chamber (0.1 sec pulse duration, followed by 5 sec pumping time, total 50 cycles) with N_2 flow rate 20 sccm at room temperature to form a TMA-NO_2 complex at the graphene surface. A thin Al_2O_3 layer was deposited with 5-cycle TMA and H_2O alternating pulses (still at room temperature) to cover the TMA-NO_2 complex. Afterwards, ALD chamber was raised to 150 ºC to start around 10 nm-thick Al_2O_3 depositions with TMA and H_2O alternating pulses (100 cycles). S/D lithography was then performed, followed by wet etching of Al_2O_3. Au (100 nm) / Ti (5 nm) S/D metal was evaporated and then lifted off. The same lithography and lift-off process was performed again to define the 100 nm-thick Al gate electrode.



(a) Graphene formation (b) ALD Al_2O_3 (C) S/D lithography

(d) Al_2O_3 wet etching (e) S/D deposition and liftoff (g) Gate formation

Figure 4.13 MOG capacitor process flow.

The MOG was characterized by an Agilent 4284 LCR meter. The total capacitance (C_{tot}) versus gate voltage (V_G) of the graphene capacitor and control Si sample is shown in Fig. 4.14(a) and 4.14(b), respectively.

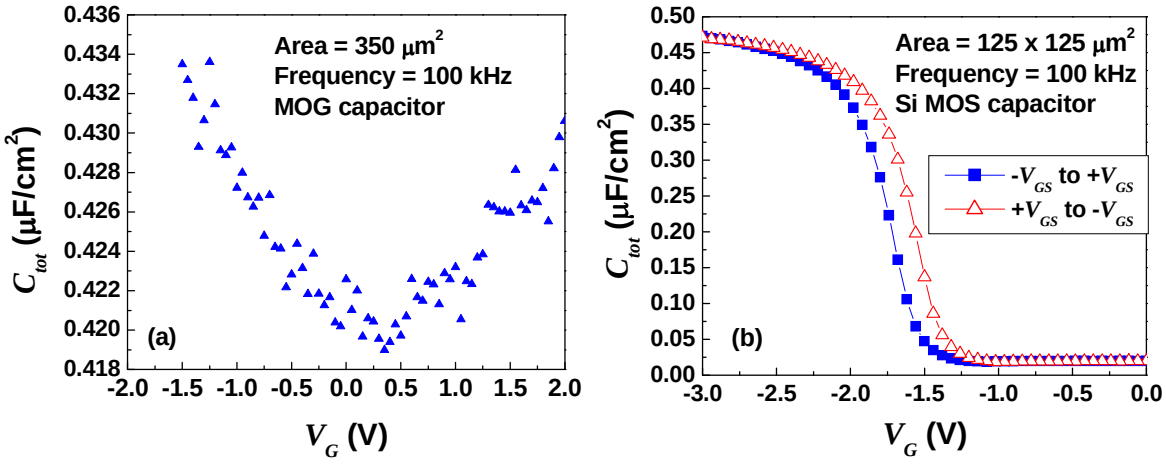


Figure 4.14 The measured capacitance of (a) the MOG capacitor and (b) control Si MOS capacitor.

For the MOG capacitor, we would like to extract the concentration of charged impurities, which reflects the quality of graphene film itself and the graphene-high-κ interface. The approach is as follows. Based on the capacitor network (Fig. 4.15), C_{tot} consists oxide capacitance (C_{ox}), intrinsic graphene quantum capacitance (C_Q) and trap (between graphene and dielectric) charges capacitance (C_{tr}). Effective graphene capacitance (C_Q') is defined as the sum of C_Q and $C_{tr.}$ In an ideal graphene, C_{tr} is equal to zero so C_Q' is equal to $C_{Q.}$

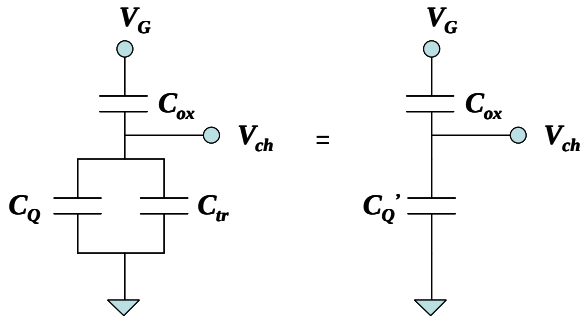


Figure 4.15 The capacitor network with C_{ox} in series with effective graphene capacitance C_Q'. Effective graphene capacitance C_Q' is defined as the sum of C_Q and $C_{tr.}$

Based on the theory of quantum capacitance in an ideal graphene (when C_{tr} = 0) [16], C_Q is defined as the change rate of the total charges (Q) in graphene with respect to the change rate of graphene surface potential (V_{ch}) and can be derived as

$$C_Q = \frac{\partial Q}{\partial V_{ch}} = \frac{2q^2 kT}{\pi(\hbar v_F)^2} \ln[2(1+\cosh(\frac{qV_{ch}}{kT}))] \quad (1)$$

where v_F is graphene Fermi velocity (~10^8 cm/s), which is relevant to the slope of the linear E - k

relation of graphene.

$$E(k) = \pm \hbar v_F \mid k \mid \tag{2}$$

where $\hbar$ is reduced Planck's constant. If V_{ch} is larger than kT/q (0.026 V at room temperature), Eq. (1) can be further simplified as

$$C_Q \approx q^2 \frac{2}{\pi} \frac{qV_{ch}}{(\hbar v_F)^2} = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{n} \tag{3}$$

where n is the carrier concentration in graphene. In practice, however, trapped impurities exist in graphene so the total carrier concentration can be modeled as

$$n = \mid n_G \mid + \mid n^* \mid \tag{4}$$

where n_G and n^* are the carrier concentration caused by the gate potential and trapped charge impurity concentration, respectively. Therefore, the effective quantum capacitance ($C_Q{}'$) becomes

$$C_Q{}' = \frac{2q^2}{\hbar v_F \sqrt{\pi}} (\mid n_G \mid + \mid n^* \mid)^{1/2} = C_Q + C_{tr} \tag{5}$$

$$n_G = \left(\frac{qV_{ch}}{\hbar v_F \sqrt{\pi}}\right)^2 \tag{6}$$

$$C_{tr} = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \mid n^* \mid^{1/2} \tag{7}$$

Based on Eq. (5)-(6), the trapped charge impurities n^* can be obtained if $C_Q{}'$ data is available [16].

We extract $C_Q{}'$ from C_{tot} (Fig. 4.14(a)) using the C_{ox} value (~0.46 μF/cm^2) obtained from

the control Si sample (Fig. 4.14(b)). The extracted C_Q' versus V_{ch} is shown in Fig. 4.16, together with other calculated C_Q' curves with different n^* values, based on Eq. (5). n^* equal to zero corresponds to an ideal quantum capacitance (C_Q) with its minimum value close to zero and the linear capacitance increase with V_{ch}. Experimentally, the presence of C_{tr} increases the minimum value of C_Q' and degrades the slope of the linear C_Q' increase. A larger n^* results in a larger minimum value of C_Q' and a smaller slope, as observed in Fig. 4.16. A fitted n^* equal to 3.4 × 10^{12} cm^{-2} is found to match our C_Q' curve well.

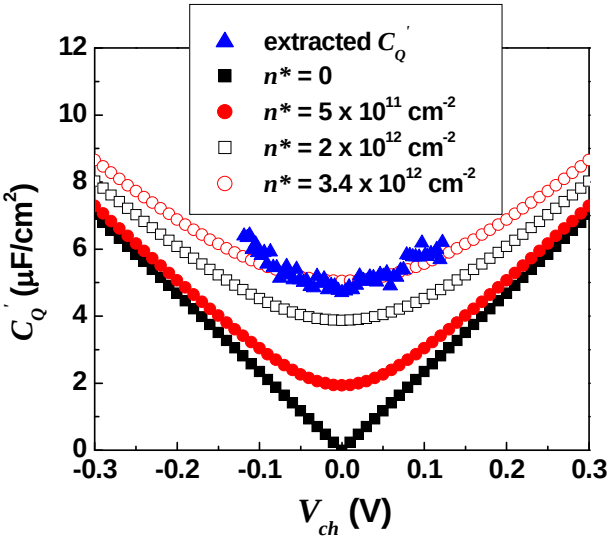


Figure 4.16 The extracted C_Q' curve, together with calculated curves with various n^* values, based on Eq. (3). n^* equal to 3.4 × 10^{12} cm^{-2} fits our C_Q' data.

The obtained n^* is higher than the value reported by Xia *et al.* ($n^* \sim 8 \times 10^{11}$ cm^{-2}) [16]. The possible reasons are as follows. First, in Xia *et al*. experiment, graphene is submerged in ionic liquid electrolyte using a three-electrode electrochemical measurement configuration, so

there is no dielectric deposited on top of graphene. On the contrary, in our structure, ALD dielectric and functionalization process may introduce impurity charges at the graphene/dielectric interface. Secondly, graphene used by Xia *et al.* is through direct exfoliation from graphite. Instead, our graphene is through chemical derivation from graphene oxide which may introduce additional trap impurities between graphene and the underlying substrate or on graphene edges [15].

To summarize, ALD Al_2O_3 dielectric is successfully deposited on graphene surface using NO_2 functionalization technique. A MOG structure has been demonstrated and reasonable capacitance characteristics are obtained, from which quantum capacitance, total carrier concentration and impurity concentration can be extracted. To reduce charged impurities in our process, both ALD functionalization process and graphene synthesis method can be further optimized.

4.3.3 Metal-Graphene Contact

For graphene's both active device and interconnect applications, the metal-to-graphene (M/G) contact is arguably the most important component that often becomes the overall performance bottleneck. The reported M/G contact specific contact resistance (ρ_c) has a huge distribution, ranging from 10^{-5} to 10^{-7} ohm-cm^2 [17]-[19] with different metal material and metal

workfunction, etc. Recently, Moon *et al.* [20] presents a contact resistance below 100 ohm-μm. Huang *et al.* [10] report contact resistance from 750-7500 ohm-μm from different metal stack, such as Ti/Au, Ti/Pd/Au and Ni/Au, etc. Obviously, there exists neither a systematic nor in-depth study of M/G contact resistance so far in terms of different metal material, metal workfunction, number of graphene layer, etc.

Furthermore, it is well known that the electrical conductivity of graphite (i.e. many graphene layers) (Fig. 4.17) is highly anisotropic with its in-plane conductivity much higher than the out-of-plane conductivity (by 4 orders of magnitude) [21]-[22]. This conductivity anisotropy is indeed originated from graphene's sp^2 hybridization of C atoms and thus the presence of numerous delocalized π electrons. Analogously, the specific contact resistivity of an edge contact the graphene sheet ($\rho_{c\text{-edge}}$) is expected to be much lower than that of an out-of-plane contact ($\rho_{c\text{-plane}}$) even though the difference involved might not be the same.

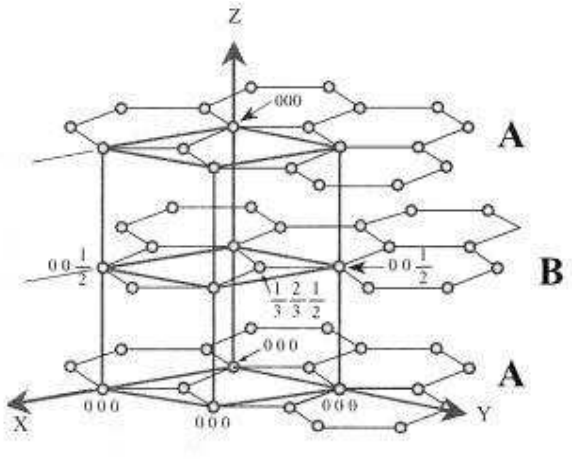


Figure 4.17 Multiple layer graphene structure with $\sigma_{in\text{-}plane} >> \sigma_{out\text{-}of\text{-}plane}$ [21].

Due to the 2D geometry of a graphene sheet, the most prevalent way in research to form metal contacts is by overlaying a bigger metal pad above part of a graphene sheet [23]-[24]. In this contact scheme, the current predominantly flows out-of-plane and minimally conducts out-of-edge (Fig. 4.18). Although the negligibly small area nullifies the edge contribution, this contact scheme does not totally resemble the VLSI practice, in which top-only contact holes through dielectric layers are used for metal contacting with active layers.

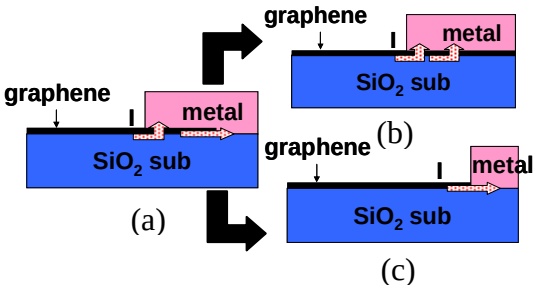


Figure 4.18 Three contact scenarios: (a) both out-of-plane and edge (b) out-of-plane only, and (c) edge only between graphene/metal interface.

In order to ensure a compatibility with the state-of-the-art VLSI metal contact scheme, we focus our M/G contact engineering study on the same structure in which the metal could only contact the semiconductor (or zero bandgap graphene semi-metal in our case) from the top surface. Here, we propose a transformative idea to lower the M/G contact resistance ($R_{c\text{-}tot}$) with the novel introduction of graphene edges inside the contact holes for current conduction in addition to the out-of-plane contribution.

It might seem counter-intuitive at first glance to utilize the graphene edge conduction to

lower the $R_{c\text{-tot}}$ because the associated cross sectional area is anyway very small (as the monolayer graphene thickness is 0.4 nm). While this is generally true for a larger contact hole size, the situation is different for a miniature contact hole. As the ratio of the contact hole area to its perimeter decreases in future technology nodes (Fig. 4.19) [25], there exists a unique opportunity to harness the benefit of low $\rho_{c\text{-edge}}$ by introducing graphene edges within the contact hole. In this work, we have evaluated several novel M/G contact schemes to lower the overall R_C and suggested their fabrication steps for graphitic transistor and interconnect deployments. It should be stressed that our goal is not to reduce R_C by reducing $\rho_{c\text{-edge}}$ and/or $\rho_{c\text{-plane}}$ through any edge and interface passivation control [26]-[27] even though they could provide additional benefits. We alternatively concentrate on the inter-contact-hole graphene geometry engineering to increase the ratio of edge conduction to the out-of-plane conduction for current flowing into the contact metal.

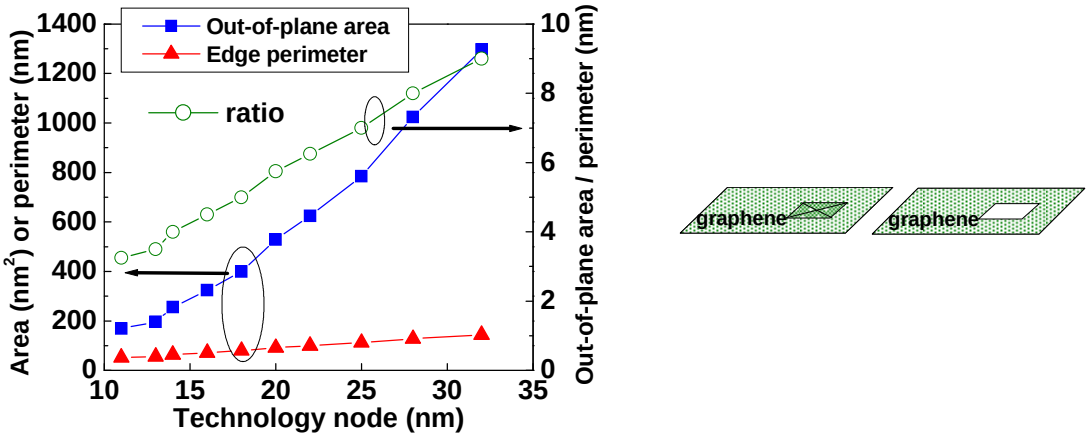


Figure 4.19 Ratio of out-of-plane to edge area of a graphene contact hole reduces with respect to future technology nodes

In the M/G contacts, both the out-of-plane and edge conductions are described by the transmission line model (TLM) (Fig. 4.20) in which ρ_c and sheet resistance (R_s) are the two key parameters (Eqs. 8-10).

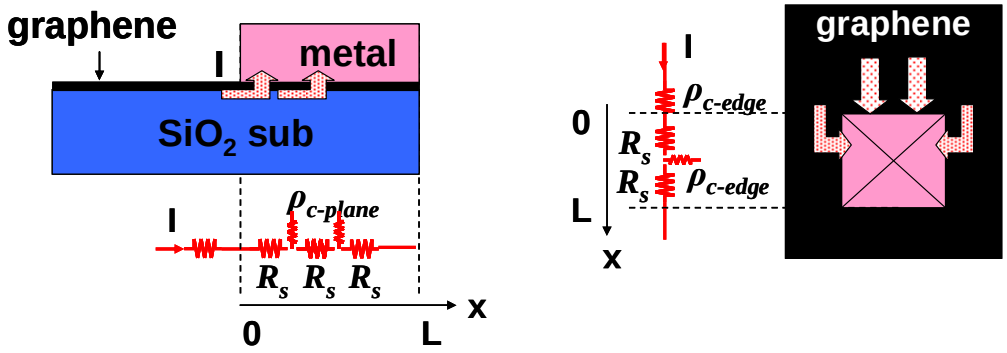


Figure 4.20 Transmission line model (TLM) for standardized R_c estimation including R_s (sheet resistance), ρ_c (specific contact resistivity), and L_T (transfer length).

$$V(x) = \frac{I\sqrt{R_s \rho_c}\,\cosh[(L-x)/L_T]}{Z\sinh(L/L_T)} \tag{8}$$

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \tag{9}$$

$$R_C \equiv \frac{V(x=0)}{I} = \frac{\sqrt{R_s \rho_c}}{Z}\coth\left(\frac{L}{L_T}\right) \tag{10}$$

Along the truly 2D graphene sheet, any spreading resistance near the M/G interface can be neglected that would indeed increase the accuracy of TLM as compared to its application to the conventional 3D materials. Currents through the M/G contacts have been simulated with

Synopsys™ Sentaurus Device. Graphene was treated as a semi-metal (zero bandgap) with separate $\rho_{c\text{-edge}}$, $\rho_{c\text{-plane}}$, and R_s. Since the dimension of graphene regions of interest is > 20 nm, any bandgap increase like in a nanoribbon would be < 10-20 meV [28]. We have verified that such small changes in bandgap do not meaningfully impact our simulation results.

(i) Contact to Graphene Device Monolayer

Two novel M/G device contact schemes have been considered. Starting with the baseline out-of-plane contact (Fig. 4.21), the conduction edges inside the contact hole locations are etched during the graphene active area definition step in scheme (I) (Fig. 4.22).

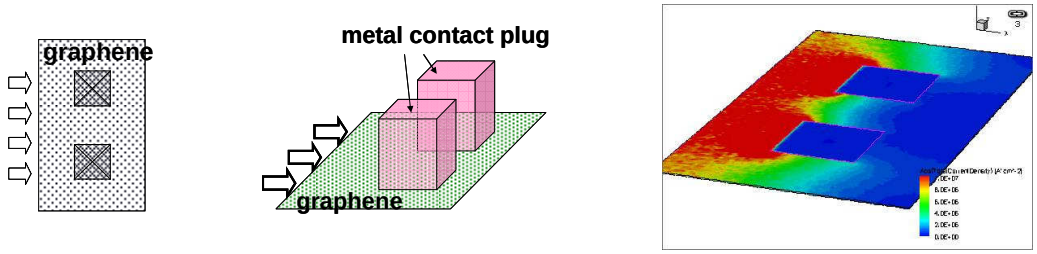


Figure 4.21 Current density profile of the baseline out-of-plane contact.

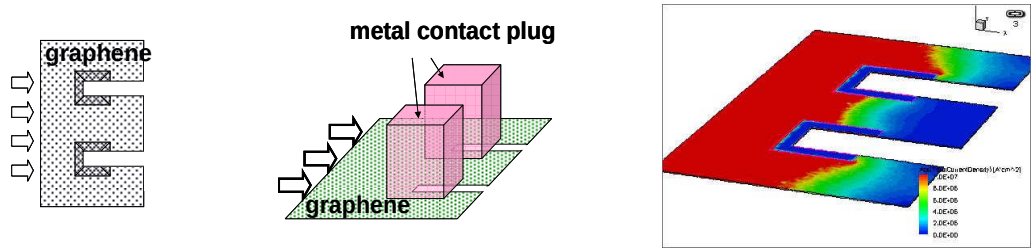


Figure 4.22 Current density profile of a novel contact scheme (I) with both the edge and out-of-plane conduction ($\rho_{c\text{-edge}} < \rho_{c\text{-plane}}$).

Based on the ITRS contact size and overlay values, novel contact holes have been designed (Fig. 4.23) and analyzed assuming different $\rho_{c\text{-plane}}/\rho_{c\text{-edge}}$ ratios. The computed R_c has revealed an advantage over the baseline when the ρ_c ratio is as small as 20-40 (Fig. 4.24). With a ρ_c ratio of 100, the low resistant edge indeed conducts the majority of the current (Fig. 4.25). Comparing the in-plane current profiles, the current crowding is mitigated in the novel scheme (Fig. 4.26) compared with the baseline (Fig. 4.21). Besides, the effects of lithographic misalignment with the overlay in the *x*-direction have been evaluated showing ~10-20% current fluctuation (Figs. 4.27-4.28). There is no major impact from the *y*-direction misalignment.

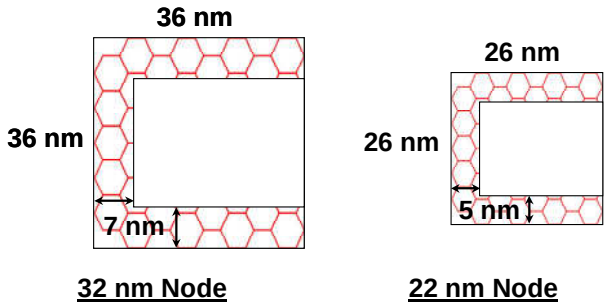


Figure 4.23 Novel metal-to-graphene contact hole design and parameters (the 32 nm and 22 nm node examples are shown).

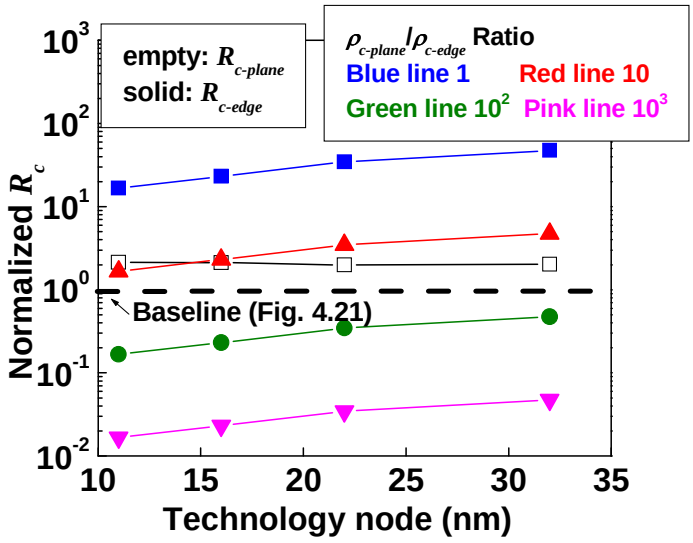
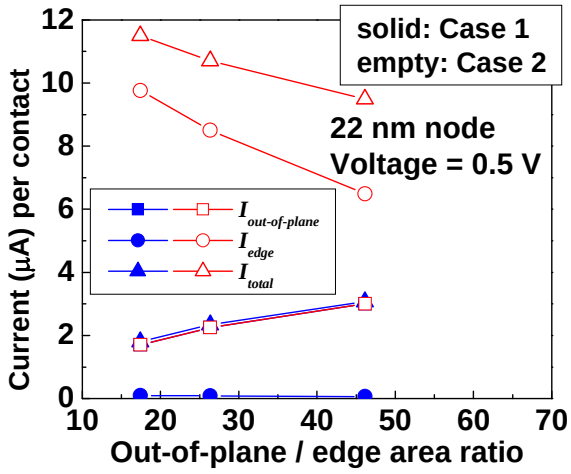


Figure 4.24 The computed $R_{c\text{-}edge}$ and $R_{c\text{-}plane}$ of the novel contact scheme (I) to a monolayer graphene for different ρ_c ratios. All the numbers are normalized to the dashed line baseline scheme.



	$\rho_{c\text{-}edge}$ (ohm-cm²)	$\rho_{c\text{-}plane}$ (ohm-cm²)
Case 1	10^{-6}	10^{-6}
Case 2	10^{-8}	10^{-6}

Figure 4.25 The simulated current components through the novel contacts to a monolayer graphene. The "Case 1" & "Case 2" conditions are tabulated and also for subsequent uses.

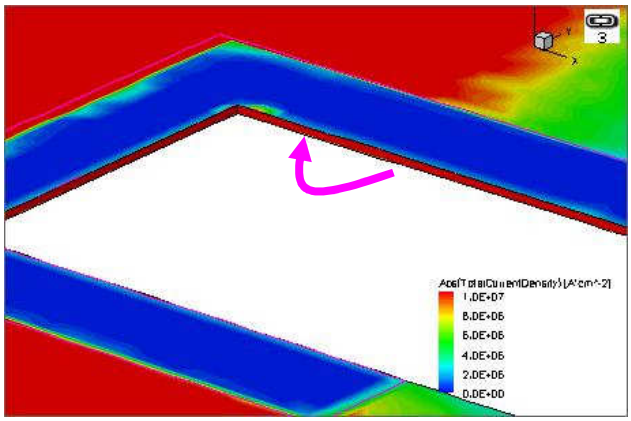


Figure 4.26 Current conduction is preferentially through the edges (more red). The contact transfer length (L_T) is larger than the contact size so current crowding is mitigated compared with the baseline.

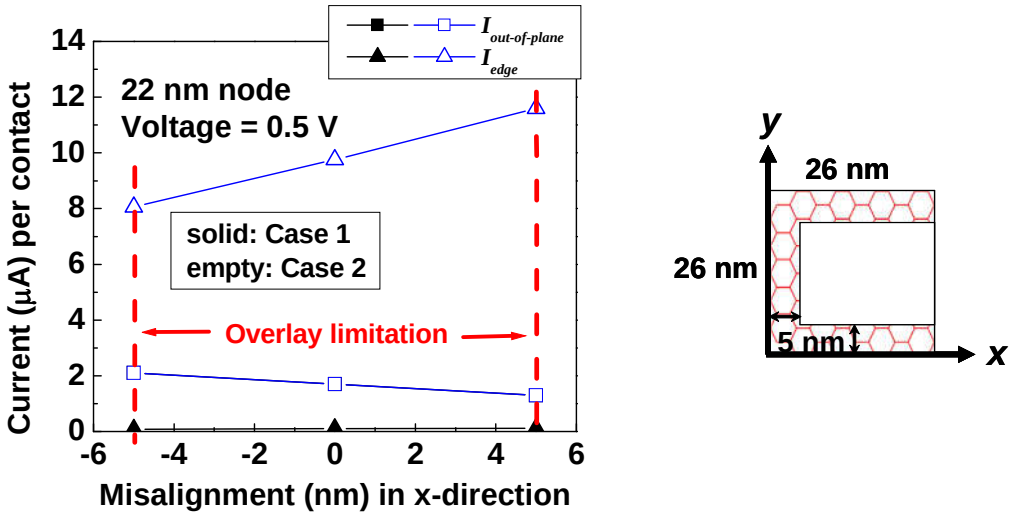


Figure 4.27 The simulated current components against the *x*-direction misalignment. The variation of the out-of-plane conduction is less sensitive than the edge counterpart.

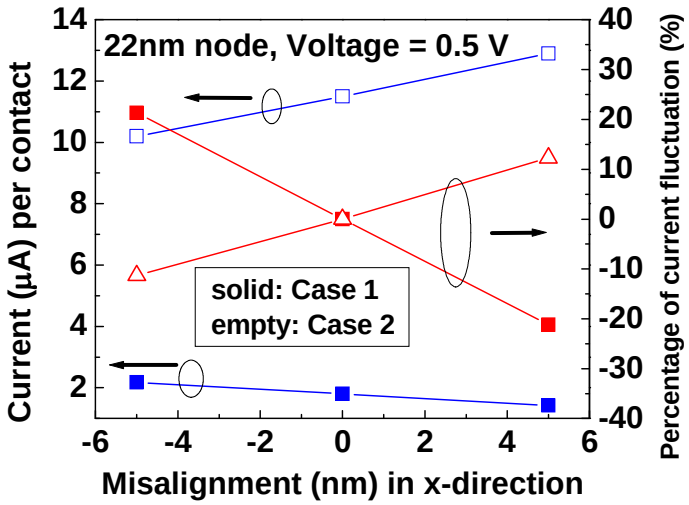


Figure 4.28 The impact of misalignment in *x*-direction on the total current and the percentage of current fluctuation.

Scheme (II) is a self-aligned contact structure (Figs. 4.29-4.30), which can be fabricated using the barrier metal to form the inward spacers inside the pre-metal dielectric (PMD) contact hole (Fig. 4.31). This misalignment-free scheme permits the overlay to scale below the ITRS value and greatly improves the allowable current (Fig. 4.32). It is interesting to note that scheme (II) becomes inferior to (I) when the area difference offsets the ρ_c ratio (e.g. at ~7 nm with a ρ_c ratio of 100). Since the resultant contact hole size would be smaller than the ITRS value, one can consider expanding the initial PMD contact hole size to ease the manufacturing challenge and regain some performance (Fig. 4.33).

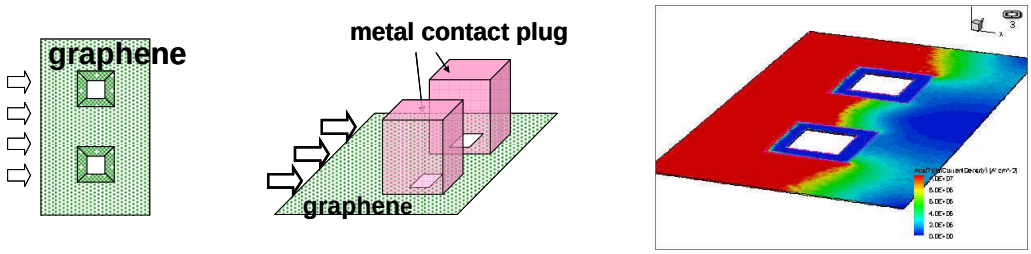


Figure 4.29 Current density profile of the novel contact scheme (II) with both the edge and out-of-plane.

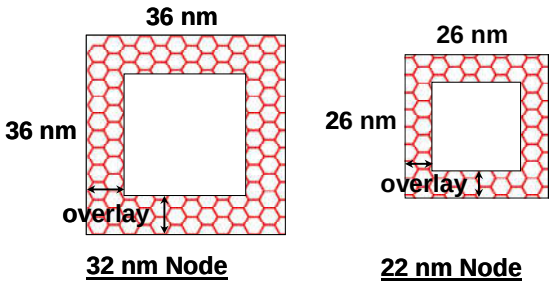
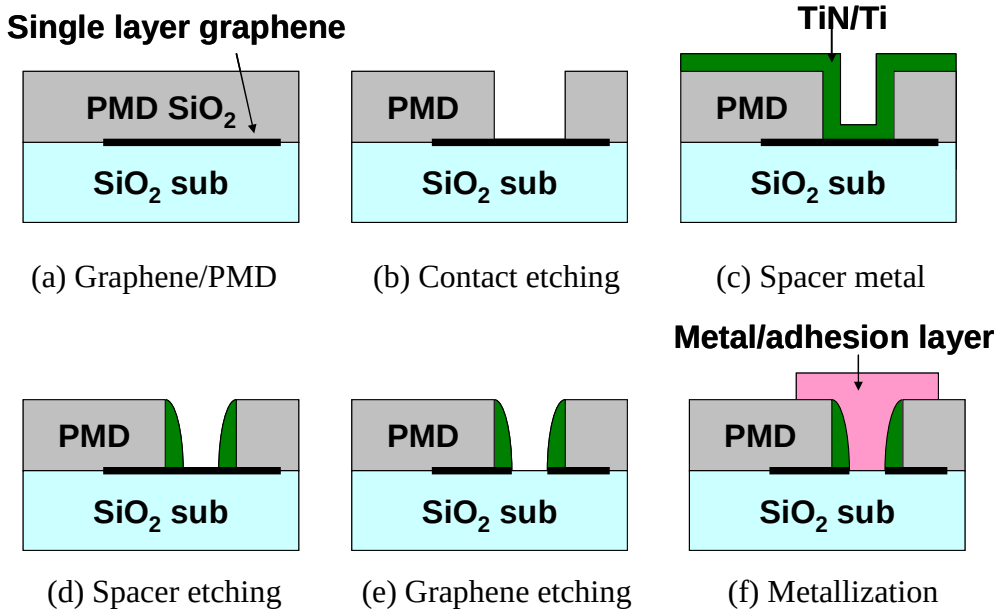


Figure 4.30 Novel self-aligned contact hole design scheme (II).



(a) Graphene/PMD (b) Contact etching (c) Spacer metal

(d) Spacer etching (e) Graphene etching (f) Metallization

Figure 4.31 The process flow to fabricate the novel self-aligned contact scheme (II).

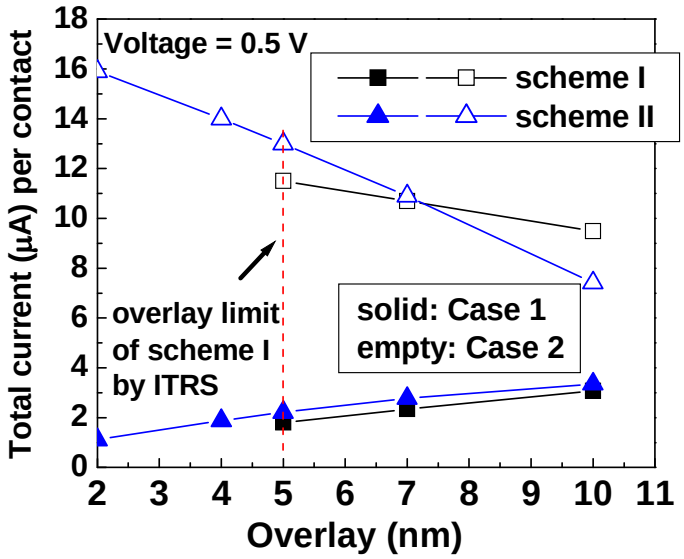


Figure 4.32 Scheme (II) has no overlay limitation and outperforms scheme (I).

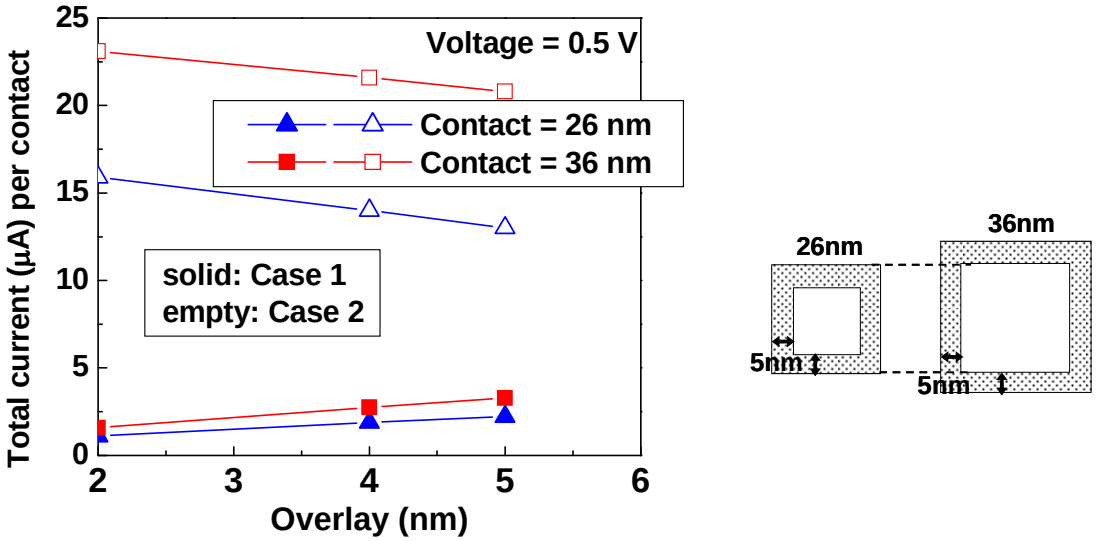


Figure 4.33 The simulated total current evaluating an expanded contact size to regain performance with perhaps a slight density penalty.

(ii) Contacts to Graphene Interconnect Multilayer

The merit of the novel M/G contact scheme is further substantiated with multilayer graphene (MLG) interconnects as only the topmost layer can make an out-of-plane contact while each monolayer can only make an edge contact (Fig. 4.34). The same self-aligned contact scheme to the metal1 (M1) MLG could in fact be seamlessly integrated with that of the M/G device underneath with no extra steps (Fig. 4.35(a)-(f) for the contact (CT) metal plug formation). The M1 MLG would thus only make edge conductions to the CT metal plug (Fig. 4.36) with the same contact hole size (i.e. zero overlay) as the M/G device contact.

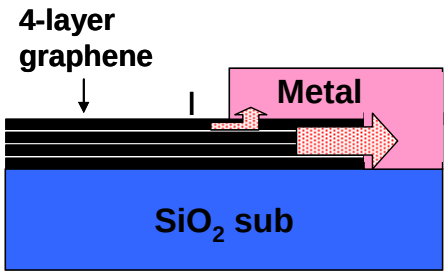


Figure 4.34 A general metal contact scheme to a 4-layer graphene (4LG) interconnect with a larger edge conduction area.

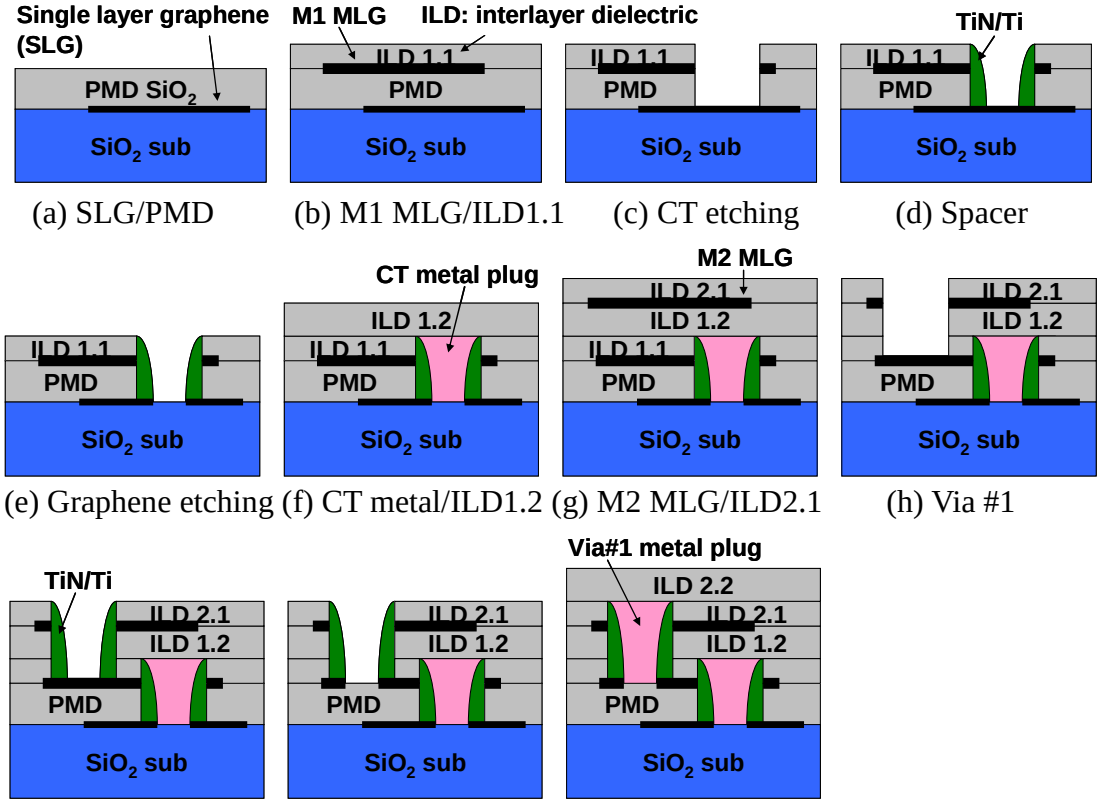


Figure 4.35 A novel process flow to fabricate and integrate SLG device channel with MLG interconnects.

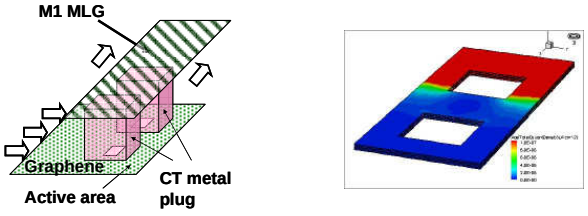


Figure 4.36 Connection between the device SLG to M1 MLG through the CT metal plug.

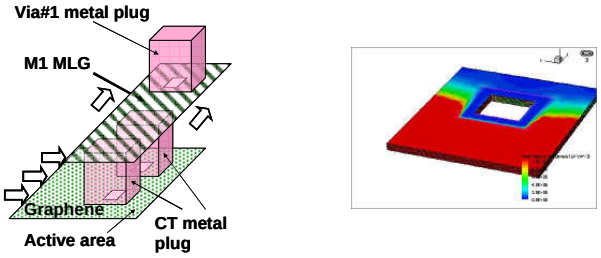


Figure 4.37 Connection between the M1 MLG to M2 MLG through the Via #1 metal plug.

Between the M2 MLG and M1 MLG connection, the same self-aligned contact scheme could be repeated again (Fig. 4.35(g)-(k) for the via #1 metal plug formation). The M1 MLG contact to via #1 will have a finite overlay (Fig. 4.37) while the M2 MLG to via #1 will not (i.e. the same as the M1 MLG to CT contact). With an arbitrarily chosen 4 layers of graphene (4LG), only a very low ρ_c ratio of 2~10 is needed for the novel scheme to outperform the out-of-plane only baseline in R_c (Fig. 4.38). The simulated current as a function of overlay also suggests a similar yet more pronounced phenomenon (Fig. 4.39). The increase in current with a smaller overlay is owing to a longer edge.

To summarize, we have proposed several novel VLSI-compatible metal-graphene contact schemes by harnessing the edge conduction to lower contact resistance versus the out-of-plane only conduction baseline. We have also suggested their fabrication processes and examined the performances and tradeoffs of these novel contacts for graphitic device channel and interconnect

applications. The lower edge contact resistivity and progressively larger edge area collectively endorse an increasing usefulness of these novel schemes.

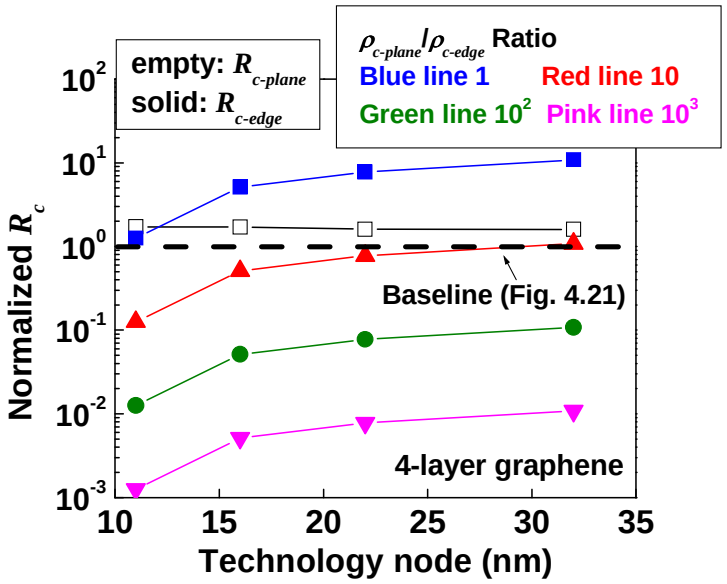


Figure 4.38 The computed $R_{c\text{-}edge}$ and $R_{c\text{-}plane}$ of the novel contact scheme (II) from a 4LG (Fig. 4.36) for a different ρ_c ratios normalized to the baseline (Fig. 4.21).

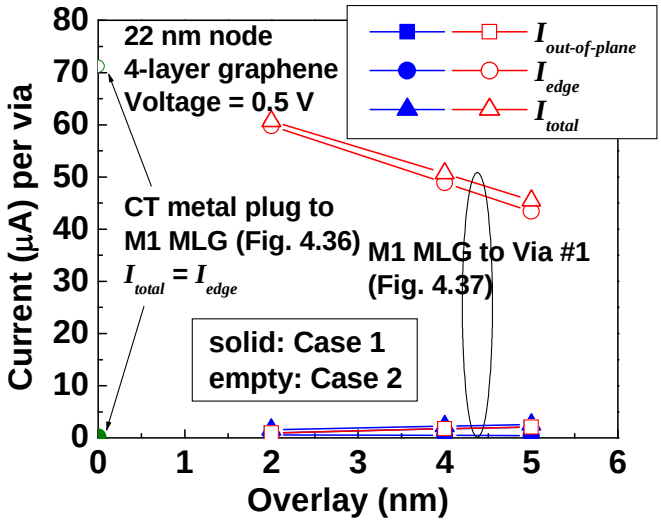


Figure 4.39 The simulated current components for a 4-layer graphene. The zero and finite overlay respectively corresponds to the CT-to-M1 (Fig. 4.36) and M1-to-Via #1 (Fig. 4.37).

4.4 Summary

In this chapter, we discuss the fabrication of both lateral and vertical III-V multigate non-planar transistors. For lateral devices, we develop a stamping transfer technique to fabrication a lateral GaAs multigate non-planar transistor. The design of the source epitaxial wafer, process flow of the stamping transfer technique, multigate channel layout pattern design, etc., are presented. Based on our technology, large arrays of aligned GaAs NWs can be transferred to a specific location on another receiving substrate using a VLSI cleanroom tool. The position of transferred NWs can be well controlled. The co-integration of GaAs and Si NWs is demonstrated with close proximity and overlay accuracy. The fabrication of the GaAs NW transistor and the device characteristics are discussed. The non-optimized S/D contact is presumably to be the reason of the low drain current in our NW transistor. Further experimental evidence is needed to clarify the issue.

For vertical devices, graphene is proposed to be used as a gate electrode in a vertical multigate structure due to its atomic thickness, good electrical conductivity and thermal conductivity, etc. Graphene-high-κ interface has been studied as it is a critical component in a transistor. NO_2 functionalization technique results in a successful ALD dielectric coating on graphene surface and typical graphene capacitance characteristics are obtained, indicating a

healthy graphene-dielectric interface. The concentration of charged impurities in graphene has been extracted. To further reduce the impurities, functionalization process, ALD process and graphene synthesis need to be further improved. Moreover, a low contact resistance of a gate metal contact is desirable so contact resistance of graphene-metal interface is studied. We propose a novel contact scheme to utilize the high conductive graphene edge based on the VLSI-compatible contact configuration. The overall contact resistance can be reduced at small contact hole size due to the contribution of low resistive graphene edge.

Chapter 5
Conclusion

5.1 Summary

As the relentless scaling of conventional Si CMOS transistors continues, it becomes more and more challenging to further increase device drive current and reduce leakage current and power consumption. In order to overcome these scaling limitations and performance tradeoffs, alternative materials and novel transistor structures need to be employed. Advanced high mobility channel materials, such as strained Si, SiGe, Ge and III-V have been explored to improve device drive current and overall performance. Also, ultrathin body or multigate non-planar structures are proposed to suppress SCE and improve leakage current and power consumption.

III-V multigate non-planar channel transistors have emerged as a promising contender in the post-Si era due to its high carrier mobility and superior electrostatic control of the non-planar structure. Some of the main challenges of the III-V multigate non-planar channel transistor lie in the lack of an accurate and time-efficient TCAD modeling of the device, parasitics engineering

and optimization, and fabrication technology with device-level co-integration capability.

First of all, a systematic methodology is developed to calibrate TCAD hydrodynamic model against Monte Carlo (MC) simulation in the quasi-ballistic regime. Through a step-by-step selection of model parameters (μ_n, τ_n, r_n, f_n^{hf}), good fits of both I_{DS}-V_{GS} and I_{DS}-V_{DS} curves have been demonstrated. Further, it is extendable to different device dimensions (both channel length and body thickness). This methodology facilitates the extension of hydrodynamic model simulations to the quasi-ballistic regime with satisfactory accuracy and time-efficiency.

Secondly, a GaAs accumulation mode vertical transistor for asymmetric S/D design and optimization is presented. Various source side and drain side spacer thickness and underlap length have been analyzed and optimized against different analog/RF metrics. Thicker source/drain spacer is effective for f_T and $f_{\max}$ improvement due to the reduction of parasitic capacitance. Increased source side underlap improves output resistance and gain through relocating the virtual source point. Increased drain side underlap improves $f_{\max}$ through a parasitic capacitance reduction. These optimizations can be readily implemented through asymmetric source/drain spacer/underlap design in a vertical transistor structure.

In addition, both lateral and vertical III-V multigate non-planar channel transistor fabrication are explored. For the lateral devices, we develop a VLSI compatible technique to transfer large arrays of aligned GaAs NWs to a specific location on a receiving substrate using a

VLSI cleanroom tool. The position of transferred NWs can be well controlled. The co-integration of GaAs and Si NWs is demonstrated with close proximity and overlay accuracy. Alternatively, for the vertical device, the possibility of incorporating graphene as a gate electrode is explored. Graphene-high-κ interface has been studied as it is a critical component in a transistor. NO_2 functionalization technique results in a successful ALD dielectric coating on graphene surface. The obtained graphene capacitance characteristics suggest a healthy graphene-dielectric interface. Functionalization process, ALD process and graphene synthesis need to be further optimized to further reduce the charged impurities in graphene. Besides, to lower the gate contact resistance in graphene-metal interface, a novel contact scheme is proposed to utilize the high conductive graphene edge based on the VLSI-compatible contact configuration. At small contact hole size, the overall contact resistance can be reduced due to the contribution of low resistive graphene edge.

5.2 Contributions of This Work

The following summarizes the contributions of this work.

(1) Development of a systematic approach of hydrodynamic model calibration on different materials and at different device dimensions.

(2) Study the parasitics optimization of an asymmetric S/D unerlap/spacer structure for analog/RF applications.

(3) Demonstration of large arrays transfer of aligned GaAs nanowires on a SiO_2-coated receiving substrate.

(4) Demonstration of co-integration capability of GaAs nanowires with Si nanowires through transfer and positioning technique using a VLSI cleanroom tool.

(5) Demonstration of NO_2 functionalization technique on graphene surface.

(6) Study of new graphene contact scheme using graphene edge conduction.

5.3 Recommendations for Future Work

Besides the results presented in this work, we would like to recommend future research in the following areas.

(1) Hydrodynamic model calibration against experimental data. Our systematic approach should be applicable for experimental *I-V* fitting. However, experimental mobility curve, source/drain parasitic series resistance, interface states, etc., should be available in order to calibrate the corresponding mobility models or include the parasitic resistance in TCAD before applying our methodology for curve fitting.

(2) GaAs nanowire / metal contact issue. GaAs/metal interface is expected to cause the low drain current in our GaAs nanowire transistors. We have verified from two-terminal measurements that non-transferred GaAs NWs (e.g., on the source epitaxial wafer) yield ~μA current level while our transferred NWs only deliver ~pA current. We believe the passivation of GaAs surface during the transfer process should be crucial. Therefore, we recommend transfer the $Al_{0.8}Ga_{0.2}As$ layers on top and bottom of GaAs nanowire concurrently with GaAs nanowire to fully protect GaAs surface. Re-design of the source epitaxial layers is needed.

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Chapter 1

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