UNIVERSITY OF CALIFORNIA
RIVERSIDE

Radio Frequency Switch Design for 5G Communication and ESD Design on Advanced Technology

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

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March 2019

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Acknowledgements

Foremost, I would like to express my utmost gratitude to my PhD advisor, Prof. Albert Wang for his guidance throughout my research at UCR. With his encouragement, support and supervision, I was motivated to learn about circuit design knowledge, critical thinking and time arrangement skills. Prof. Wang's motivation, integrity and immense knowledge inspired me. I hope to take what I learned from Prof. Wang with me and continue to thrive in my future career.

I would also like to extend my appreciation to Prof. Sheldon Tan and Prof. Ming Liu for serving as a member of my dissertation committee. I am grateful for their time and effort in reviewing my dissertation and their insightful comments.

It's my great pleasure to work with my fellow labmates, Dr. Fei Lu, Dr. Chenkun Wang, Dr. Qi Chen, Mr. Cheng Li, Mr. Mengfu Di and Ms. Zijin Pan, for the discussions and guidance. Their support and talent filled my PhD life with happiness and encouragement.

I appreciate Skyworks for providing me an opportunity to join as an internship. I want to thank my manager Dr. Weiheng Chang, my mentor Dr. Xingyi Hua, and my colleges Dr. Paul Wu and Dr. Yuting Chang. Their knowledge and unselfish share is invaluable throughout my life.

Last but not the least, I would like to express my sincerest gratitude to my parents for their support and love. Without your encouragement, I could not be able to finish my education path. Thank you.

ABSTRACT OF THE DISSERTATION

Radio Frequency Switch Design for 5G Communication and ESD Design on Advanced Technology

by

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Doctor of Philosophy, Graduate Program in Electrical Engineering
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Dr. Albert Wang, Chairperson

The evolving 5G requires high data rate, low latency and broad coverage. Many new technologies are developed to fulfill these requirements, including multi RAT, carrier aggregation, advanced slot-based framework, mm-wave bands, beamforming and MIMO. These technologies require high isolation and harmonic filtering, low insertion loss, high linearity and fast switching RF front-end switches. In this dissertation, a design example of 3.5GHz switch is depicted in chapter 2 and an ESD protected 28GHz travelling wave switch is shown in chapter 3, which achieves comparable performance with state-of-art design and is the first ESD protected travelling wave switch on SOI.

On the other hand, as IC process evolving, traditional CMOS technology cannot fulfill the high speed and low power requirements. Therefore, advanced processes, FinFET and FDSOI technology start to be widely used, following with rising of cost and increase design complexity. Therefore, ESD reliability becomes a major concern. In chapter 4, we proposed a high area efficiency Cell-by-Cell SCR, which can save die area and provide less degradation on RF, mm-wave and high-speed circuit performance due to its low parasitic associated with smaller area. To lower the trigger voltage, Cell-by-Cell DTSCR is proposed. Temperature effect of diode, SCR and DTSCR is illustrated, where the large performance variation across temperature of DTSCR rise a question mark for ESD designer.

Successful simulation before silicon is essential for first-silicon success and time-to-market, especially for high cost advanced technologies. So does for ESD protection. In chapter 5, 3D mixed-mode TCAD ESD simulation flow for FinFET devices is depicted. This flow covers mainstream ESD device type, including diode, ggMOS and SCR. Besides device level ESD simulation, chip level fast dynamic ESD protection simulation methodology using Verilog-A is developed. This methodology is verified with silicon and shows its capability to cover novel ESD devices and various ESD protection circuitry in chapter 6.

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Chapter 1. Introduction of 5G front-end

1.1. 5G background

As demand grows for ubiquitous wireless connectivity and the promise of new and previously unimagined applications, such as autonomous vehicles, artificial intelligence, telemedicine and virtual reality. These applications requires advanced algorithm, hardware processing speed and advance wireless communication techniques.

5G (5th Generation) is the latest generation of cellular mobile communications. 5G performance targets high data rate, reduced latency, energy saving, cost reduction, higher system capacity, and massive device connectivity. 3rd Generation Partnership Project (3GPP) submitted 5G NR (New Radio) as its 5G communication standard proposal. 5G NR include bands below 6 GHz (FR1), and higher frequencies above 24 GHz and into the millimeter waves range (FR2). As shown in Figure 1-1, the first phase of 5G specifications in Release-15 will be completed by April 2019 to accommodate the early commercial deployment, which focus on FR1 bands below 6GHz (n77, n78, n79).

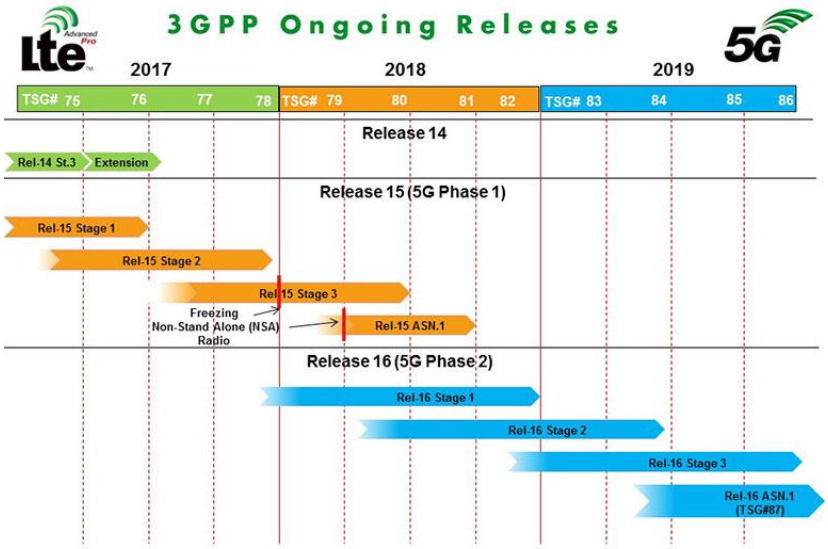


Figure 1-1 3GPP 5G time-line

The second phase in Release-16 is due to be completed by April 2020 for submission to the International Telecommunication Union (ITU) as a candidate of IMT-2020 technology [1]. The ITU IMT-2020 specification demands speeds up to 20 Gbps. To achieve this, several technologies are under developing, including multi-RAT (radio-access-technology), advanced modulation (i.e. CP-OFDM, DFT-OFDM), advanced framework (higher frequency subcarrier and shorter slot), wide channel bandwidths (up to 100MHz for one channel), massive MIMO, beamforming tracking and advanced small cell techniques. The details will be discussed in Chapter 2.

Figure 1-2 shows the key spectrum Federal Communications Commission (FCC) is driving toward 5G. The 3.5GHz and 28GHz frequency bands will be the first commercial 5G bands with highest potential for global harmonization over time.

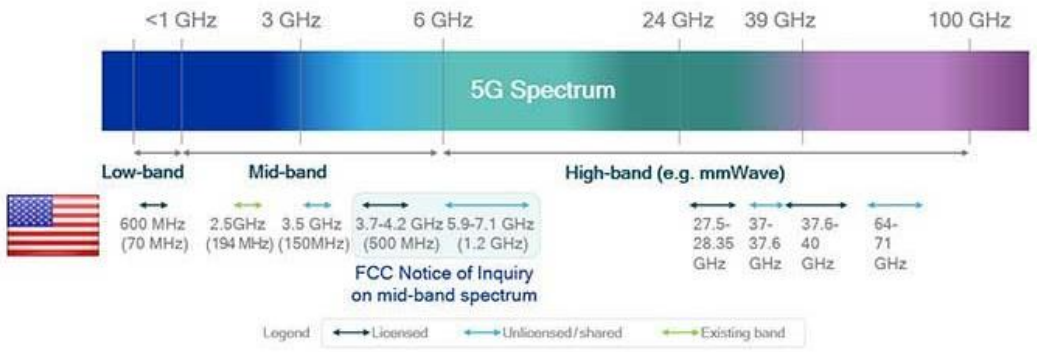


Figure 1-2 The FCC is driving key spectrum initiatives to enable 5G. [1]

1.2. 5G RF front-end

In a radio receiver circuit, the radio frequency front end (RFFE) is a generic term for all the circuitry between a receiver's antenna inputs up to the mixer stage. It consists of all the components in the receiver that process the RF signal from antenna before converting to intermediate frequency (IF), and in the transmitter that amplify the RF signal before signal been sent out to antenna. The main blocks include Antenna switch module (ASM), Band switch (BSW), diplexer, duplexer, filter,

low-noise amplifier (LNA), power amplifier (PA), matching networks and Mobile Industry Processor Interface (MIPI).

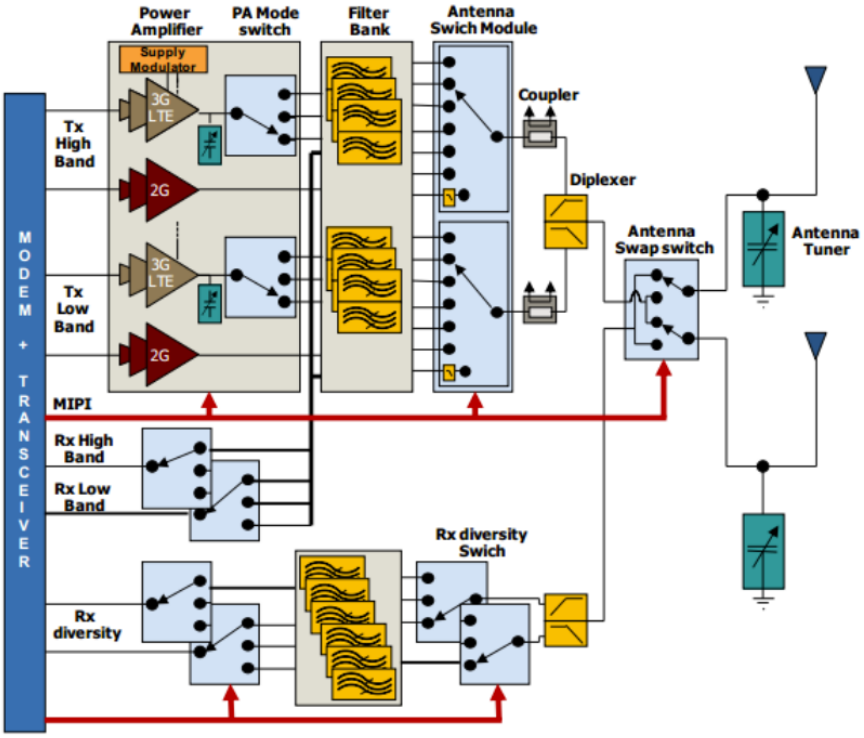


Figure 1-3 Front-end-module block diagram [2]

As wireless communication technology evolves, an increasing number of RFFE components are integrated in the front-end module with smaller chip size. Back to 1990s, cell phone only support GSM bands, however, nowadays a typical 4G cell phone can support more than 10 bands. The rising band number increases complexity of RF front-end design complexity. For example, LNA needs different input matching inductors for different bands, and the source degeneration inductor have to be designed with trade off with noise performance to balance it across different bands. PA needs to cover wider bandwidth with flat frequency response but not sacrifice power efficiency. More duplexers are added to front-end module with shrank size. Antenna switch is required to support more bands, which increase the difficulty of maintaining a good isolation.

When it comes to 5G FR1, more sub-6GHz bands will be included and the new assigned n77, n78 and n79 bands across 3500MHz – 5000MHz uses time division duplexing (TDD), which require T/Rx switches to switch between transmitting and receiving.

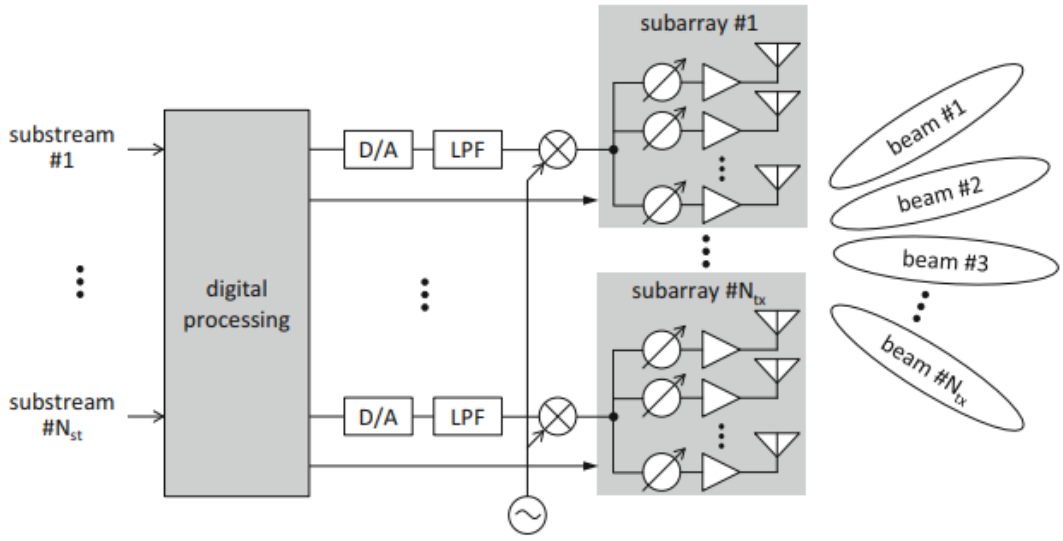


Figure 1-4 illustration of MIMO and Beamforming [3]

For 5G FR2, RF front end will show higher complexity. Due to lower power amplifier output powers, higher path losses, and higher shadowing losses from the decreased diffraction and dispersion effects, transmissions in the mm-wave bands have significantly less favorable link budgets. However, the shorter wavelength in the mm-wave bands means more antennas can be packed into the same physical area. Therefore, multiple antenna techniques such as Multiple-Input Multiple-Output (MIMO) and beamforming are anticipated to perform an important role in 5G system. In addition, massive MIMO benefits for reducing latency and simplifying the MAC layer. Beamforming techniques require accurate phase control of the RF signal. Thus, high accuracy, small size phase shifter is needed, as well as small size antenna array. Moreover, With RF beamforming being deployed with a large scale antenna array, Time Division Duplexing (TDD) is a good alternative to Frequency Division Duplexing due to the ability to leverage uplink/downlink

reciprocity in controlling the beamforming operation. Therefore, in 5G RFFE, there will be massive T/Rx switches and antenna switches, which can be designed as a switch array on the same chip.

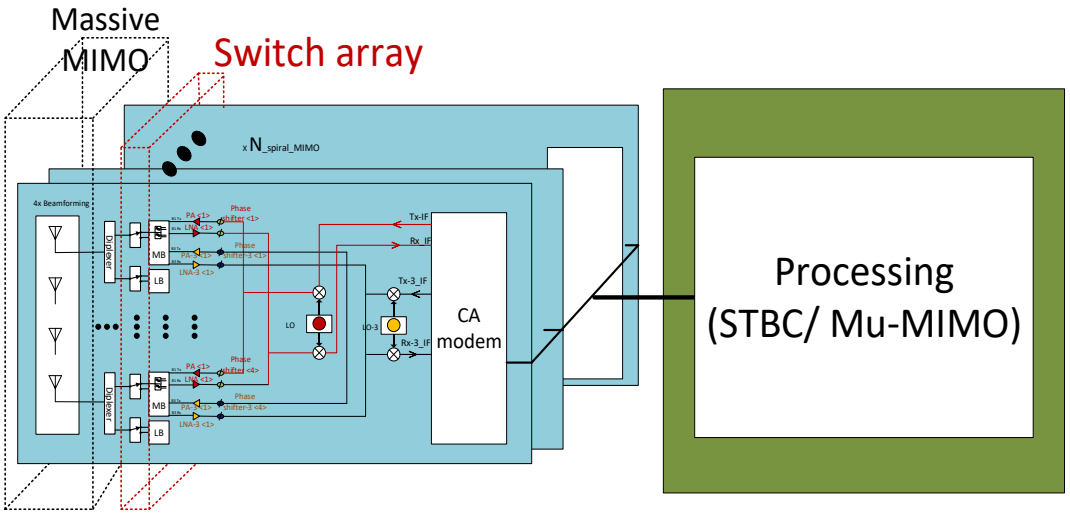


Figure 1-5 Proposed 5G architecture

1.3. 5G RF switch design challenges

As mentioned before, the number of antenna switches and T/Rx switches will increase in 5G RFFE. Coming with the increase number and complicated 5G techniques are various design challenges.

The first problem comes with the increase of supported bands. More bands supported means more branches of the antenna switch. During the operation of antenna switch, only one branch is connected to the input signal, while all other branches are off. The parasitic capacitance of these off branches will cause leakage of the RF power, which results in degradation of the insertion loss. The existence of the parasitic capacitance also degrades matching. The increasing number of switch also rise a problem of interference. Cross-talk between different switch can distort the desired RF signal, which was usually eliminated with proper layout and increasing the distance between switch

blocks. However, for 5G RF front end, with limited area, this is hardly applicable. Metal cage concept is proposed to solve this problem, which uses FIB to each a trench around the switch blocks and fill in silver powder. In this way, the emitted EM signal is shielded from each other.

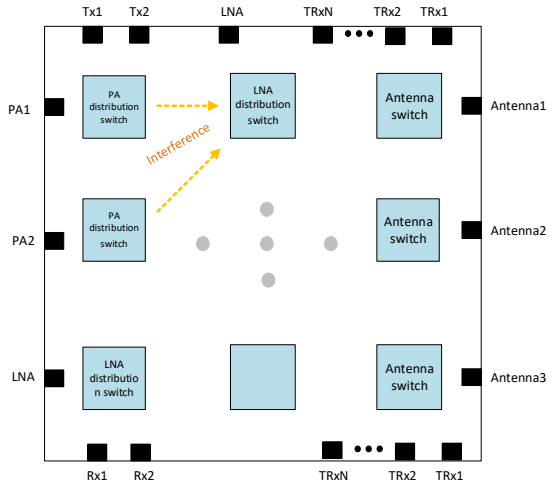


Figure 1-6 Cross-talk between switch blocks in switch array

More severe challenge occurs in high frequency. For 5G FR2, mm-wave switch is required. Under high frequency as 28GHz, the performance of conventional series-shunt type switch is hard to fulfill the requirements due to the high leakage from off branch capacitance. Various switch topology has been reported, including distributed switch, series-shunt with matching inductors and travelling wave switch. The details will be discussed in Chapter 3.

Chapter 2. Introduction of ESD protection

Electrostatic (ESD) failure is a major reliability concern to integrated circuits (ICs) and electronic systems (i.e., smart phones). As IC technology node continue shrinking into nanometer domain, ESD protection is emerging as a key IC design challenge, especially for high-frequency operating at multi-GHz and high-speed ICs with data rates beyond tens gigabits per second. The ESD phenomenon originates from transfer of electrostatic charges between two objects of different electrical potential and the resulting fast and large ESD transients can damage ICs.

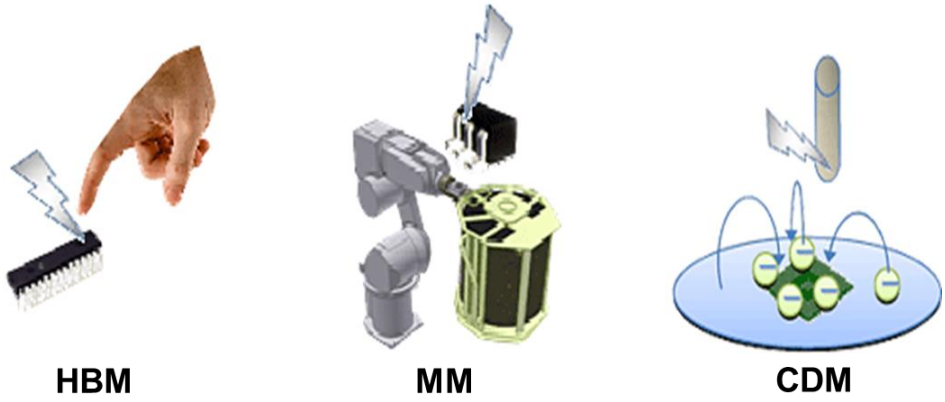


Figure 2-1 ESD test models

2.1. Chip level ESD models

According to the discharging scenario, there are four primary ESD models considered in the microelectronics industry: Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) for on-chip ESD and IEC standard for system level ESD. One emerging ESD protection design challenges along with IC technology scaling-down is the ESD Design Window Shrinking Effect. The human body model represents a human body discharging through the IC module to ground. The equivalent circuit for HBM is a 1.5kΩ resistor in series with a 100pF capacitor. The capacitor is charged to the specified ESD voltage, and then the switch is closed and the current flows through the Device. Machine model represents fabrication or packaging machine

discharge to device. The waveform of machine model is bidirectional damped oscillation. Both MM and HBM ESD events occur between any two pins, therefore, an ESD discharging path is required between every two pins. Charged device model depicts the scenario of changed chip discharge to outside conductor. The charge is induced by friction and the discharge is from one pin to outside. Comparing with HBM, CDM is a very high current event, but occurs in a very short time interval. Due to the fast ESD surge, slow response ESD is not suitable for CDM protection because of the overshoot phenomena. The IC failure under CDM is often caused by gate-oxide (Gox) breakdown, while for HBM and MM, the failure is often caused by thermal breakdown.

To characterize ESD device performance under these ESD events. Transmission-Line-Pulse (TLP) is developed to characterize ESD device performance under HBM. Different from HBM tester which is a one-time transient test, TLP is a quasi-static ESD test. It strikes ESD device with increasing steps of voltage. The measured voltage and current on device is integrated in a time slot (20%-70%) to generate a series of points under a set of pulse voltage. TLP usually has a duration time of 100ns to simulate the same power as HBM pulse. HBM tester can only give a result of pass or fall, however, TLP can provide more insightful results for the ESD device performance. CDM has faster rise time and duration, correspondingly, vf-TLP was developed. Vf-TLP usually has a duration time in range of 2ns to 10ns. Under this high frequency, simple dc cable is not suitable. For vf-TLP measurement, GS probe and coaxial cable for RF measurement are utilized.

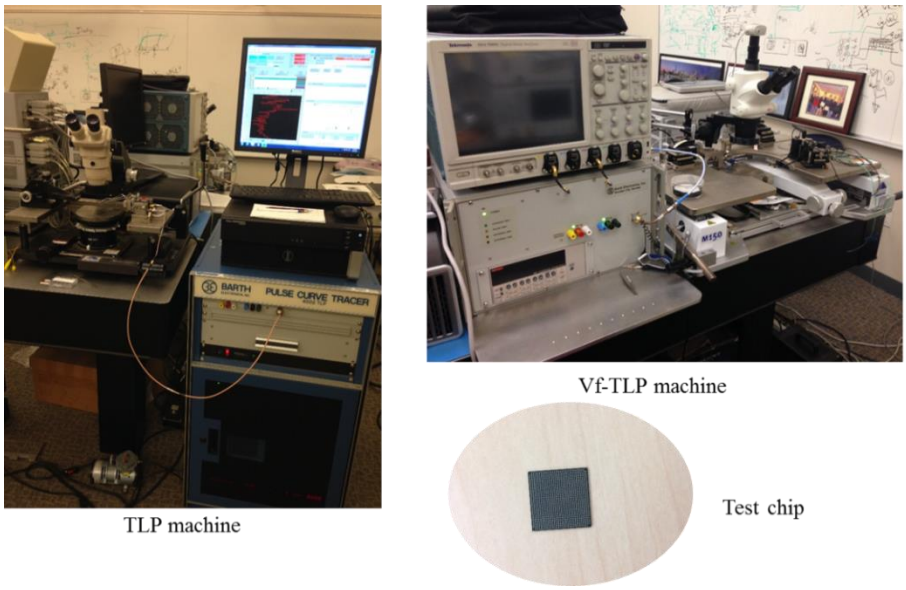


Figure 2-2 ESD protection device characterization instruments

2.2. ESD design window

ESD device design has to fit in ESD design window as shown in Figure 2-3, an ESD Design Window is defined by the breakdown voltage (BV) and power supply voltage (VDD) of the core circuit under protection with a proper safe margin for practical IC designs. An ESD protection solution requires accurate design of ESD-critical parameters including the ESD triggering voltage, current (V_{t1}, I_{t1}), the ESD holding voltage and current (V_h, I_h), the ESD discharging resistance (R_{ON}). The trigger voltage (or turn-on voltage) of the ESD device is required to be lower than the breakdown voltage to discharge ESD current and clamp ESD voltage down before the core circuit is damaged. On the other hand, to prevent the ESD device trigger on under normal operation, trigger voltage is required to be higher than the supply voltage. Moreover, the holding point also has restricted requirements. To prevent the ESD protection device fall into latch-up state after one ESD strike, the holding voltage is usually required to be higher than the supply voltage. Therefore, after the ESD surge pass, the supply voltage cannot sustain the ESD device in snapback states. Another

solution is also widely used, where the holding current is designed to be much higher than the supply current. In this case, supply current can't keep the ESD device in snapback state. For snapback devise, such as GGMOS and SCR, one important rule is that the breakdown voltage (V_{t2}) should be higher than the trigger voltage (V_{t1}) to ensure the ESD device can be uniformly triggered on. As IC technology node mitigating to below 40nm nodes, ESD design window shrinking effect becomes an emerging challenge for ESD protection designer.

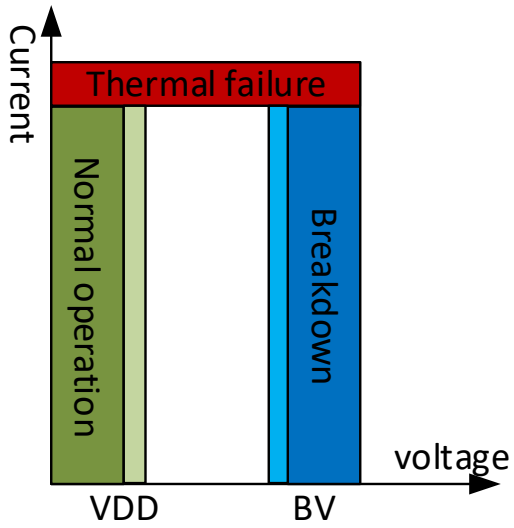


Figure 2-3 ESD design window

2.3. ESD protection strategy

One of the most widely used ESD protection strategies for HBM is to use double diodes on the I/O pin, one to the supply bus and the other to the ground bus. Figure 2-4 shows the protection schematic. The power clamp turns off during normal operation and turn on during an ESD event to provide a very low resistance discharge path between power rail. The discharge path of all passible HBM zapping is illustrate below. For a positive pulse with respect to power supply, the current passes through the upper diode to the supply pin. For a negative pulse with respect to ground, the

current passes through the lower diode and out the signal pin. For a negative pulse with respect to the supply pin, the current flows into the supply pin, flow through the power clamp, and then passes through the diode connected from the pin to ground. For a positive pulse with respect to ground, the current passes through the upper diode, along the supply rail to the power clamp, through the clamp, and out the ground pin.

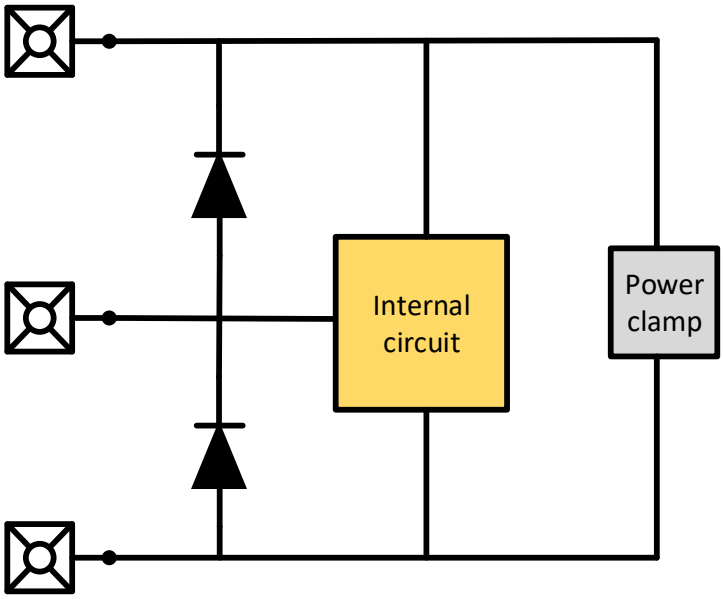


Figure 2-4 ESD protection diagram for HBM

For mixed-voltage circuits where the input power can be higher than the supply voltage, this strategy is not applicable as the up diode will conduct current to supply pins. In this case, a simple solution is to replace the up diode to diode string to prevent ESD protection turning on. GGMOS is usually used to provide bidirectional ESD protection to the input pins. Since GGMOS has high trigger voltage than input signal amplitude, it will not cause signal leakage. Under positive ESD zapping from input pin to ground pin, the GGMOS will trigger on and fall into snapback region to provide a low resistance discharging path. For the negative pulse, the GGMOS will work as a diode connect MOS and conduct ESD current to grounded pins.

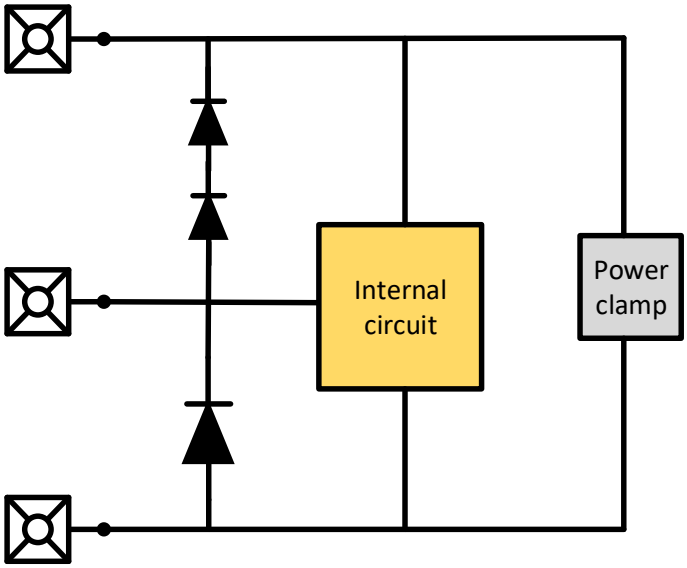


Figure 2-5 Diode-string for ESD protection of mixed voltage application

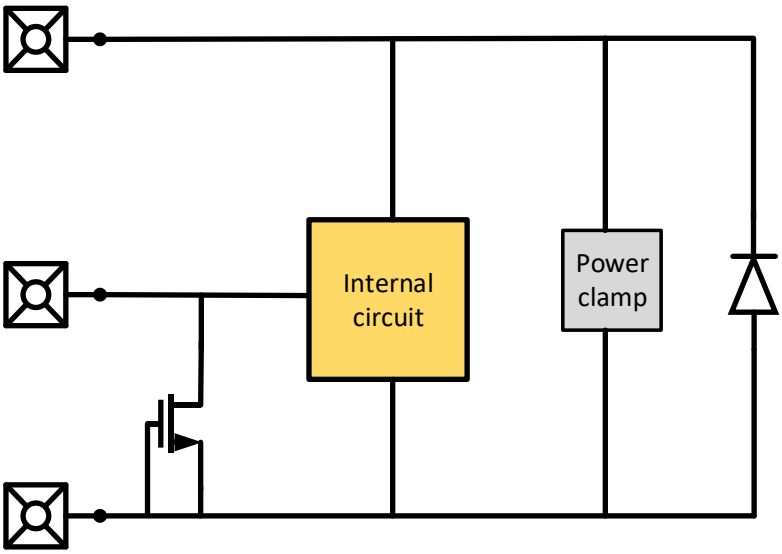


Figure 2-6 GGMOS for ESD protection of mixed voltage application

CDM usually high current and rapid discharge. The main ESD failure mechanism is gate oxide break down. Therefore, the input pins need to be paid extra notice. Due to the high ESD peak current (~10A), even if the diode turn on resistance is very small (~1Ω) , a high voltage (10V) will stress the input buffer gate oxide can cause ESD failure. Thus, 2-statge ESD protection scheme is

commonly used for CDM protection. The first stage discharges the most portion of the ESD current and the second stage is used to clamp the ESD voltage down to safe level.

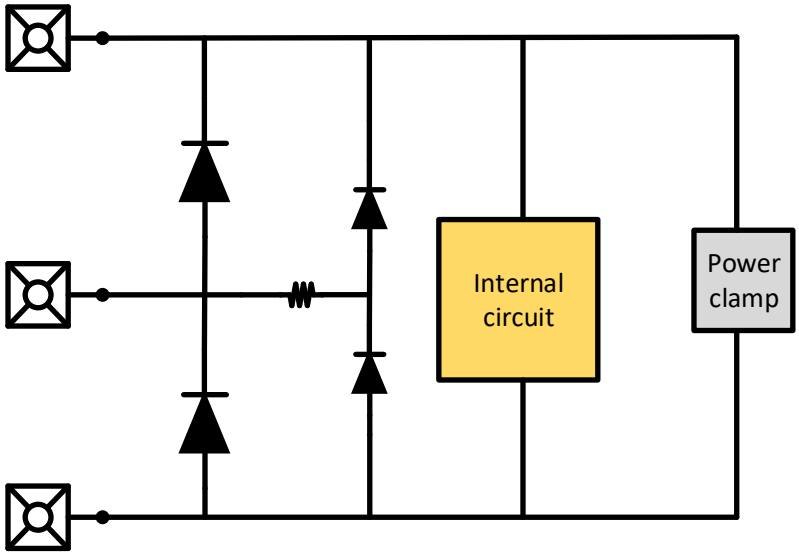


Figure 2-7 CDM ESD protection scheme

Chapter 3. 3.5GHz series-shunt RF switch design in SOI

3.1. SOI technology

Figure 3-1 shows the historical market share of different RF switch process [4]. Benefiting from high mobility and high power handling ability, PHEMT and GaAs had been used for RF switch for a long time. Recently, silicon-on-insulator (SOI) technique featuring low parasitic capacitance, good isolation and high integration ability starts to dominant RF switch market after 2012.

Figure 3-1 SOI penetrating RF switch market [4]

Figure 3-2 shows a cross-section of SOI FET. Where a buried oxide (BOX) layer isolates the substrate and transistor. Combined with shallow-trench-isolation (STI), transistor is isolated from each other. The utilization of BOX can minimize parasitic capacitances associated with junction-to-well diode, and to reduce substrate coupling, which enables high isolation between each circuit block. It is also worth notice that MEMS is penetrating to market and its market share is growing. This chapter will focus on RF switch design on SOI process.

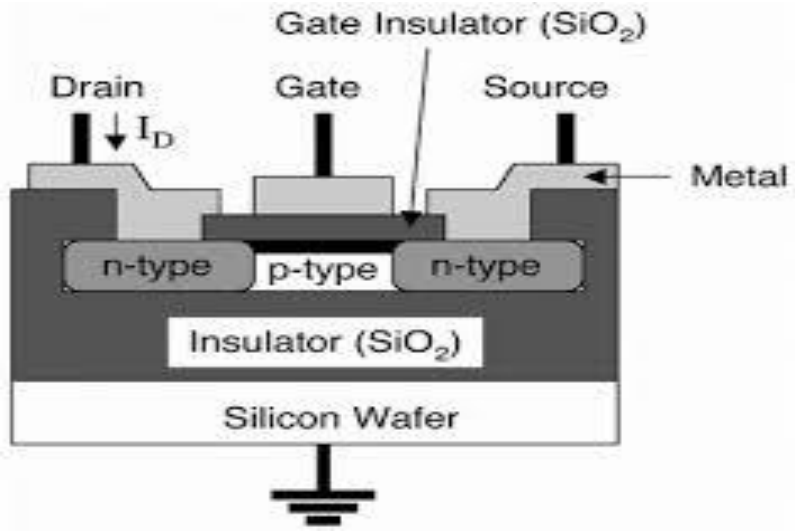


Figure 3-2 SOI cross section [5]

3.1.1. FDSOI and PDSOI

Depending on the depletion region, SOI can be divided into partial depletion (PDSOI) and fully depletion (FDSOI). Partially depleted SOI has been successfully leveraged for high-performance microprocessors and most other SOI applications for almost a decade. Although FD-SOI has been commercially used for a long time, its focus has always been on ultra-low power applications. Recently, the high-performance world is looking at advanced devices such as ultra-thin body FDSOI MOSFETs and multiple-gate MOSFETs (i.e. FinFET) as potential ways to drastically cut power consumption and leakage while preserving high performance and minimizing short channel effects.

FDSOI has several advantages over PDSOI. Since FDSOI uses un-doped or slightly doped channel, the random fluctuations in threshold voltage are minimized. When transistor body is floating in PDSOI, body charge will be introduced by ion-implant when source-drain voltage is very high. These body charge can rise body potential V_{BS} and therefore reduce threshold voltage. This is called “floating bod effect” or “kink effect” for analog design. One method widely used to minimize floating-body effects is to use fully depleted (FD) SOI devices. In FD devices, the SOI

film thickness is (much) smaller than the channel depletion width, and therefore the body charge is fixed. Moreover, FDSOI can achieve better leakage control and power consumption are drastically reduced. From 22nm, FDSOI is designed with ultra-thin channel, which enables body bias technique. However, the ultra-thin channel around 6nm is challenging in fabrication and eliminates its application in high power area.

3.2. RF switch design matrix

RF switch is a key block in FEM. The main specifications of RF switch are Insertion loss (IL) in signal paths, isolation between ports, power handling capability, switching time and linearity. In general, small signal performance of RF devices are characterized by their S-Parameters. For RF switches, there are three S-parameters of significant importance to this project: S11, S21, and S31. These are also known as the reflection coefficient, insertion loss, and isolation, respectively. For large signal behavior, power handling ability and linearity is main concern. Switching time represents the time consumes for a switch turns on form off states, which characterizes its transient behavior.

3.2.1. Insertion loss

Insertion loss is defined as the ratio between output and input RF power or a ratio of the signal level in a test configuration without switch to that with switch. The insertion loss of antenna switch is mainly determined by the on-state resistance (Ron) in series branch as explained in equation 2-1, which is irrelevant to frequency and also known as resistive insertion loss. The frequency dependent part of the insertion loss comes from off-state capacitance.

$$IL = -20log\frac{2R_0}{2R_0+R_{on}} \quad 2\text{-}1$$

The insertion loss of switch can degrade the overall front end performance in both transmitter and receiver side, especially for antenna switch. In RF receiver, a LNA is used to minimize the noise figure (NF) induced of the following stage according to Friis-equation. However, RF signal will go through antenna switch and duplexer before reaching LNA. This loss will directly add to the system NF. Every amount of insertion loss in antenna switch needs much extra effort spent on improving LNA design. More importantly, the system NF directly contributes to RF system sensitivity with equation 2-2.

$$Rx_{Sensitivity} = -174 + 10 \times \log(BW_{[Hz]} + NF_{[dB]} + SNR_{[dB]}) \quad 2\text{-}2$$

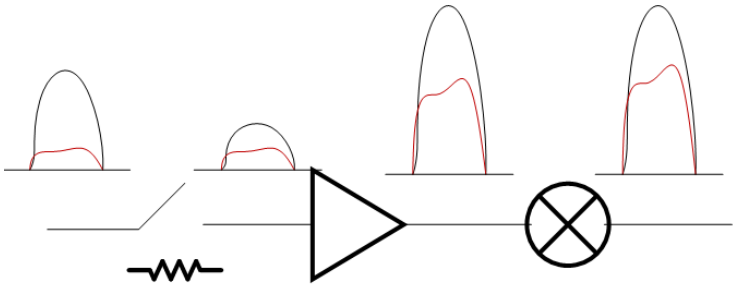


Figure 3-3 Simplified SNR in receiver

The degradation of Rx sensitivity reduces signal coverage as Coverage area reduces approximately 1% per 0.1 dB of IL. High IL also directly degrades the passive efficiency, which results in lower PA efficiency (PAE). PAE degrades approximately 1% per 0.1 dB of IL, which is large enough to determine the market of a FEM.

3.2.2. Isolation

Isolation is defined as the ratio of RF power leaked to the off-state branch to input signal power. Isolation of RF switches depends on the off-state capacitance as expressed in equation 2-3. On SOI process, the body of a FET has two configuration. For floating body connection, the parasitic

capacitance is smaller comparing with body connected FET. However, floating body can cause linearity problem due to kink effect.

$$Iso = -20log\frac{2R_0}{2R_0+{}^{1}/_{\omega C_{off}}} \quad 2\text{-}3$$

To improve the isolation of switch, layout works is one of the main concern. To reduce the parasitic capacitance between metal lines, M1 is better to keep away from each other. To keep low resistance of signal path, M1 connected to source and drain needs to be wider. To lower the capacitance between Vias, via is better to be placed in cheese pattern as shown in Figure 3-4.

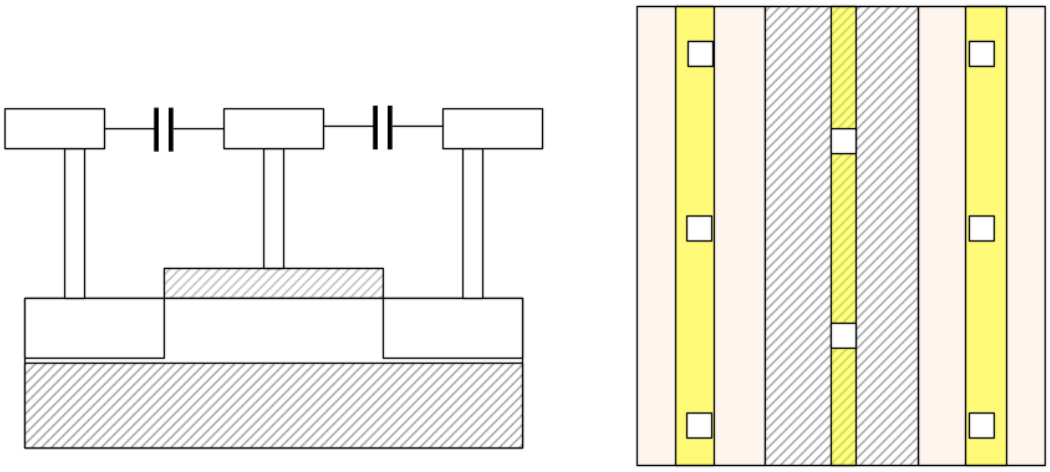


Figure 3-4 Layout concern in switch design

Poor isolation of switch can degrade RF system performance in some cases. For example, the uplink of Band28 spans from 703MHz to 748MHz while the down link of Band 29 is 717-728MHz. Due to the fact that B29 only has downlink and its frequency overlaps with Band 28 Tx, B29 Rx and B28 Tx is usually covered with one off-chip acoustic filter and a switch is used to considering cost and size. Under B29 and other band (i.e. B12) carrier-aggregation case, where B29 Rx and

B12 Tx turns on at the same time. The RxBn of B12 Tx power shown as noise to B29 Rx, which can cause severe degradation to receiver sensitivity as shown in Figure 3-5.

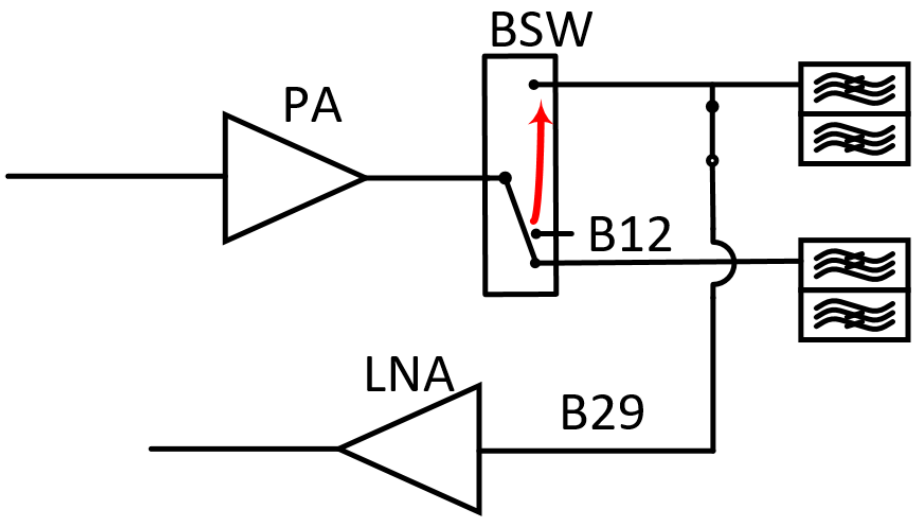


Figure 3-5 RxBn caused by BSW isolation.

3.2.3. Linearity

The linearity of RF switch is characterized by its gain compression point (P1dB) and Third Order Input Intercept Point (IIP3). As shown in Figure 3-6, kink effect for floating body SOI FET will degrades the linearity of switch. Therefore, for switches requiring high linearity, body is better to be connected.

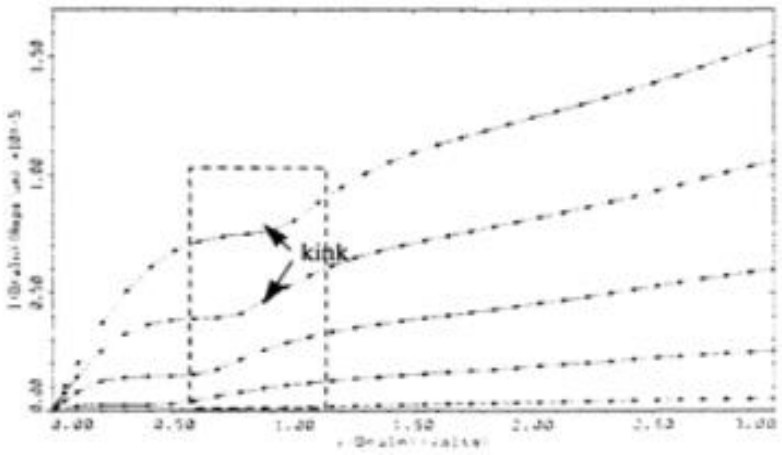


Figure 3-6 Kink effect

Moreover, there are some typical causes of linearity degradation. To improve linearity, the body is usually connected as shown in Figure 3-7, where the PMOS acts as a diode connection. When the FET is switched off, the gate is biased with negative DC voltage (V_g<0V). PMOS turns on and draw the body voltage to negative. This configuration ensures the P-well/N-plus junction keeping off, which is harmful to the linearity of switch as it causes power drop out.

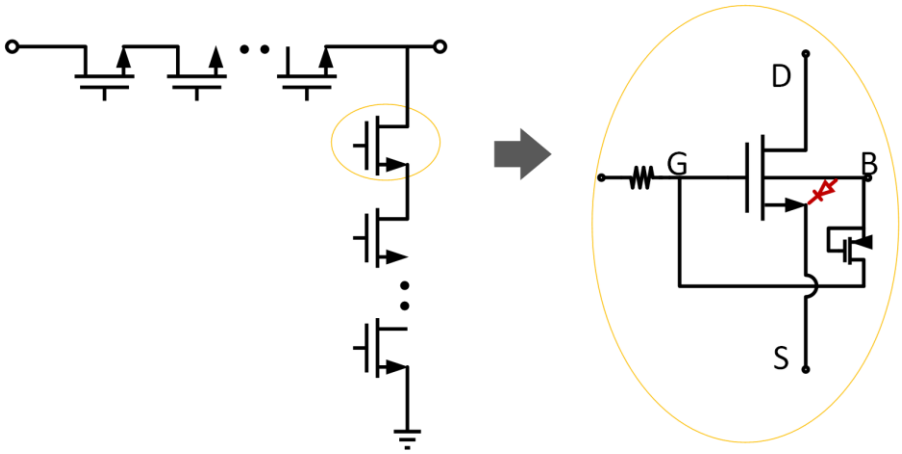


Figure 3-7 Body connection of SOI NFET

- ESD drop out

When RF signal power is large enough that the peak voltage is higher than the turn-on voltage of ESD device, RF signal is clamped. Thus, linearity degrades severely.

- RF-Control coupling

When high power RF signal path (PA, switch) is placed around the control signal line, or the bonding wires are placed closed to each other, the RF signal can couple into control line and change control states. For example, turn on the off-state branch. Therefore, degrades linearity

- Body biasing – NVG loading

As mentioned before, diode connection PMOS is usually used to connect the body of FETs. When the switch turns off from on-state, the voltage on gate node drops to negative with a negative voltage generator (NVG). As the PMOS turns on to draw the body voltage down, it sinks current. When the switch have a lot of branches, this can be a problem when the loading capability of the NVG is not enough. The result is the output negative voltage rise up and linearity degrades.

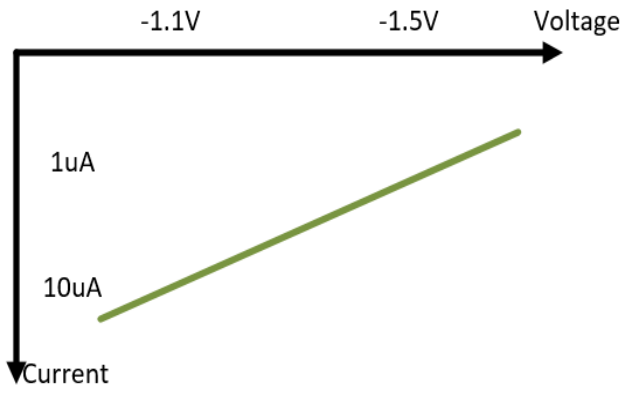


Figure 3-8 A sample of negative voltage generator output load-line

3.2.4. Power handling ability

When we say "power handling (P_{max})" for switches, what we mean is the power level that will correspond to the onset of gain compression. The on-state power handling ability is highly related to the current handling ability of transistors while the off-state power handling ability is related to breakdown voltage. To improve on-state power handling ability, wider transistor size is desired. However, for the off-state power handling, the breakdown voltage is limited by process parameters, i.e. doping level, thickness of gate oxide, etc. To improve the power handling ability, FETs are stacked to distribute the large RF power. The process of determining stack number is expressed in equation 2-4 to equation 2-7. Due to substrate and gate leakage, V_{ds} distribution is imbalance across the FETs. End devices will see a larger V_{ds} swing, which limit the power handling ability. To improve voltage imbalance, forward coupling capacitor can be used, which however can cause RF simulation convergence problem sometimes. Width modulation is another method. By making end FET wider, the voltage can show better balance. Reminder the fact that source-drain breakdown voltage is related to the channel length of FETs. Thus, by increasing gate length of end FETs, the power handling ability can be improved. This method is called length modulation.

$$Maximum\ output\ power = P_{max} \tag{2-4}$$

$$V_{pk} = \sqrt{2 \times P_{watt} \times Z_0} \tag{2-5}$$

$$V_{max} = V_{pk}\left(1 + \frac{VSWR-1}{VSWR+1}\right) \tag{2-6}$$

$$Stack\ height = \frac{V_{max}}{BV_{dss}} \tag{2-7}$$

3.2.5. Figure of merits

There are two types of figure of merit for switch process. The first one is the product of on-state resistance and off-state capacitance (R_{on}*C_{off}). This figure of merit is used to identify the small signal capability of the switch process. The lower the figure of merit, the better performance it can achieve on insertion loss and isolation. As technology developing, the figure of merit is getting smaller. For the state-of-art, The FOM can reach as low as around 100 [6]. Another type of figure of merit is proposed to identify the power handing and isolation capability of switch process. It takes breakdown voltage into consideration and expressed as (R_{on}*C_{off}/BV).

3.3. 3.5GHz T/Rx Switch design consideration

Spectrum availability for IMT in the 3300-4200 and 4400-5000 MHz ranges is increasing globally. The 3400-3600 MHz frequency band is allocated to Mobile Service on a co-primary basis in almost all countries throughout the world. Administrations will make available different portions of the 3300-4200 and 4400-5000 MHz ranges at different times, incrementally building large contiguous blocks.

The 3GPP 5G NR specification will support 3300-3800 MHz from the start (n78), using a TDD access scheme (Figure 3-9). In line with the release plans from many countries, the 3300-3800 MHz band will be the primary 5G band with greatest potential for global harmonization over time.

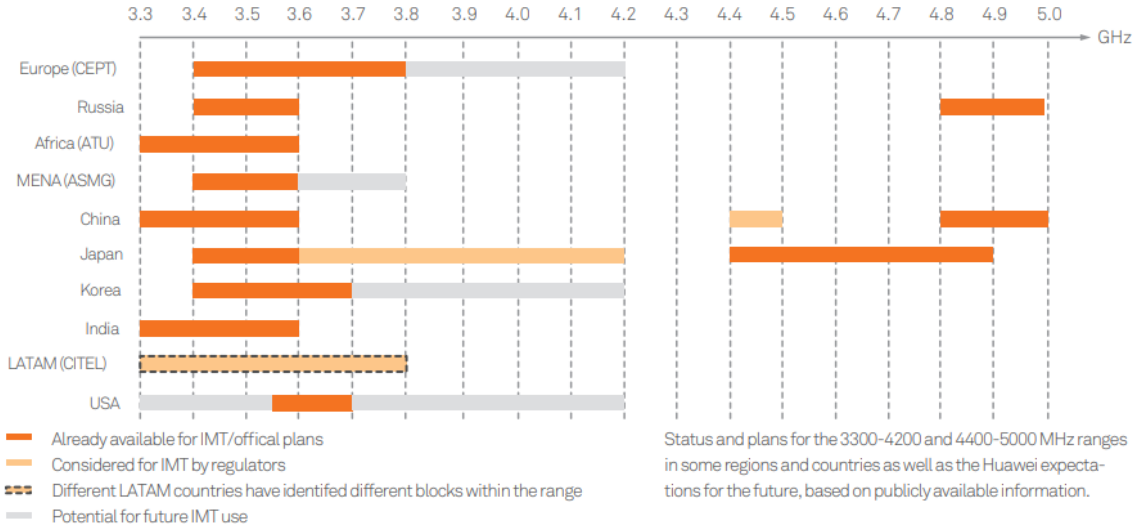


Figure 3-9 Global availability and planning of the 3300-4200 MHz and 4400-5000 MHz frequency ranges [source. Huawei – 5G Spectrum public policy position]

As mentioned in Chapter 1, many new technologies are invented for 5G FR1 under 6GHz. Utilization of large system bandwidth is considered as an effective method to significantly increase per-user throughput and overall system capacity. Carrier aggregation (CA) technology is developed to combine two or more carriers, in the same or different frequency bands, into one data channel to enhance the data capacity. 5G NR supports carrier aggregation with 16 component carriers. Moreover, Carrier aggregation of LTE and 5G NR carriers is also possible which is known as Dual Connectivity (DC). Multiband RF radio signals can interfere with each other because of insufficient filter attenuation. This means there is a higher probability of desense in CA applications if isolation or cross-isolation between transmit and receive paths is insufficient. Therefore, High switch isolation and harmonic filtering are required to mitigate this situation [7][8].

For 3GPP Release 15 it was agreed that an OFDM-based waveform with Cyclic Prefix (CP-OFDM) will be supported for both 5G NR download and upload. DFT-S-OFDM based waveform will be also supported, complementary to CP-OFDM waveform and used for an enhanced mobile broadband (eMBB) uplink up to at least 40GHz. CP-OFDM waveform features higher peak-

average power ratio (PAPR), which rise higher requirements on switch linearity. On the other hand, under high PAPR, power amplifier (PA) faces more restricted trade-off between linearity and efficiency. Thus, low insertion loss switch is required to relief PA design challenges [9].

To reduce latency, evolution in the slot-based framework used in LTE has been developed for 5G. LTE has 15 kilohertz subcarrier spacing, with 1 millisecond slots (or subframe) each supporting 14 symbols. Similarly, 5G allows for a 15 kHz subcarrier with a 1 millisecond slot for 14 symbols, in a deliberate attempt to align 4G with 5G. But 5G has other options, including 30 kHz subcarrier with a 500 microsecond slot, 60 kHz with a 250 microsecond slot, and 120 kHz with a 125 microsecond slot. The shorter slot requires faster TDD switching. Therefore, switching time also meets more restrict specifications.

In conclusion, these new technologies introduced to realizing 5G FR1 requires high switch isolation, high harmonic filtering, low insertion loss, high linearity and fast switching 3.5GHz RF switch.

3.4. 3.5GHz T/Rx Switch design in SOI

The MIPI Interface standard defines industry specifications to interface chipsets and peripherals in mobile-connected devices. In the mobile industry the solutions are used in smartphones, tablets, laptops and hybrid devices. The basic configuration of the RFFE MIPI interface and control diagram of antenna switch (ASW) and band switch (BSW) are shown in Figure 3-10. Two control signal line coveys the serial bidirectional data signal (SDATA) and the clock signal (SCLK) into MIPI interface, then the data is processed and send to internal SWIPI. SWIPI process the input data with MISR (multi-inpuit-shift-register) and assign the data to slave interface according to register enclosed in MIPI word [10]. Figure 3-11 shows the bias diagram of designed SPDT switch. Where a negative voltage generator (NVG) is utilized to generate a negative

bias voltage to off branch. Quadrature connected transistors are used to swap the control voltage. The control voltage VDD is supposed to be supplied from a LDO regulator to eliminate the interference from control signal to RF signal.

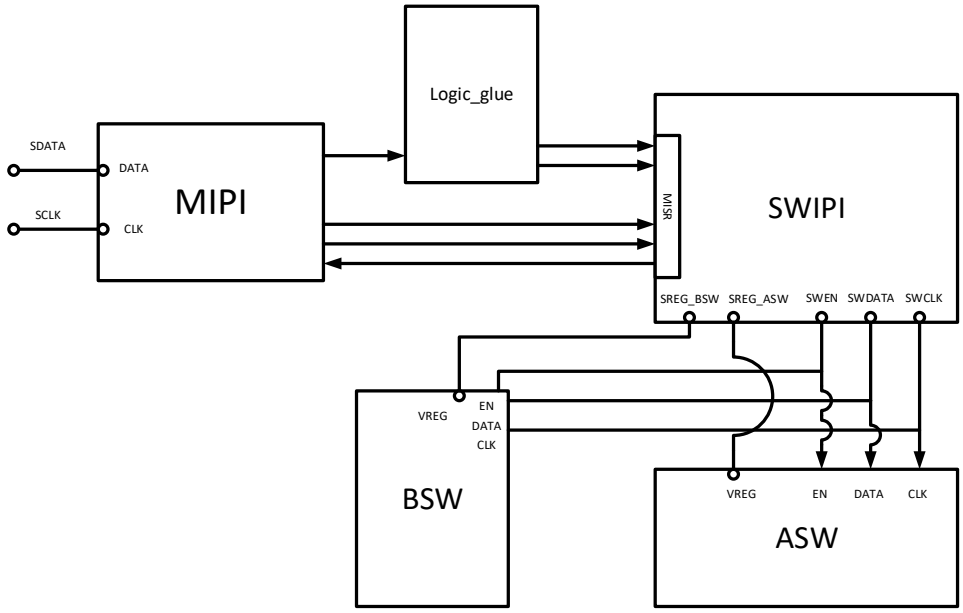


Figure 3-10 Control diagram of antenna switch and band switch

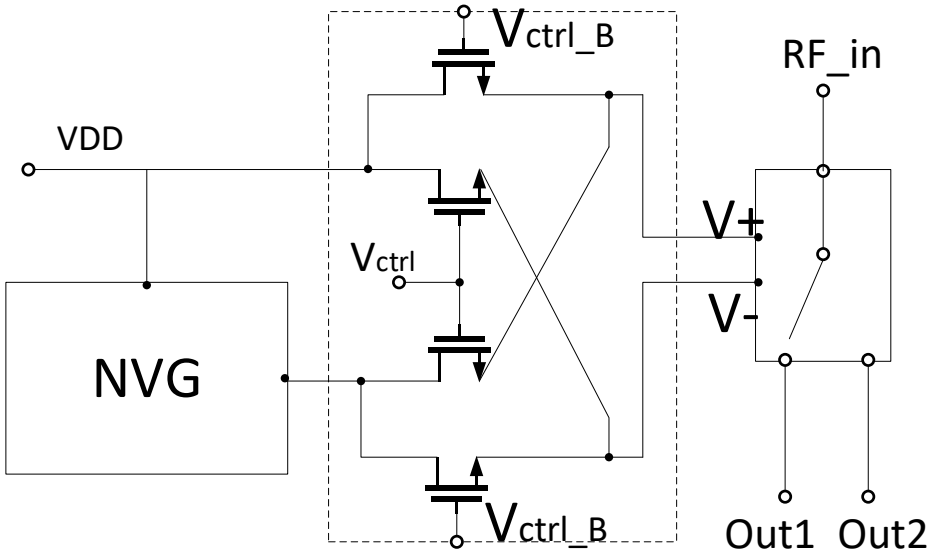


Figure 3-11 Block diagram of SPDT switch core and bias

3.4.1. Negative voltage generator design

Charger pump is wide used in analog and RF circuit design, such as PLL, DC-DC converter and negative voltage generator. To generate a negative bias voltage, a circuit using charge pump concept is used as a negative voltage generator. Figure 3-12 shows the block diagram. A two phase clock generator creates two clock signal with same frequency and 180 degree phase shift. These two clock signal input to charge pump and drive the charge pump draw charge from capacitor to generate a negative voltage. The output of the charger pump is noisy due to clock punch through. Thus, a low-pass RC filter is used to remove the ripple, with a cost of delayed response time. The schematic of the charge pump is shown in figure. M1 and M2 are PMOS while M3 and M4 are NMOS. Two capacitors Cp are used to connect M1 drain and M2 drain. When CLK changes from zero (0V) to high voltage (V_{DD}). Due to the fact that charge in capacitor can't discharge immediately, voltage across capacitor stays the same. Therefore, voltage at node A rises the same amount as CLK. CLKB is out of phase with CLK. Thus, in the same time, node B drops a voltage equals to $-V_{DD}$. Therefore, M3 is open and M2 is also open. During this clock cycle, M3 draws current from output capacitor C1, and M2 conducts current to ground (Figure 3-13). Therefore, voltage of node A decrease to 0V and forms a voltage equals to V_{DD} across Cp. In the meantime, a negative voltage forms at node C. for the next clock phase, voltage of node A drops to $-V_{DD}$, which opens M4 and drain current from C1 to lower node C voltage. In the same while voltage of B rises to V_{DD} to conduct current to ground through M1 (Figure 3-14). As analyzed here, during each clock cycle, M1 and M4 or M2 and M3 pair work together to draw charge from capacitor C1 to generate a negative voltage. Finally a negative voltage $-V_{DD}$ appears at output.

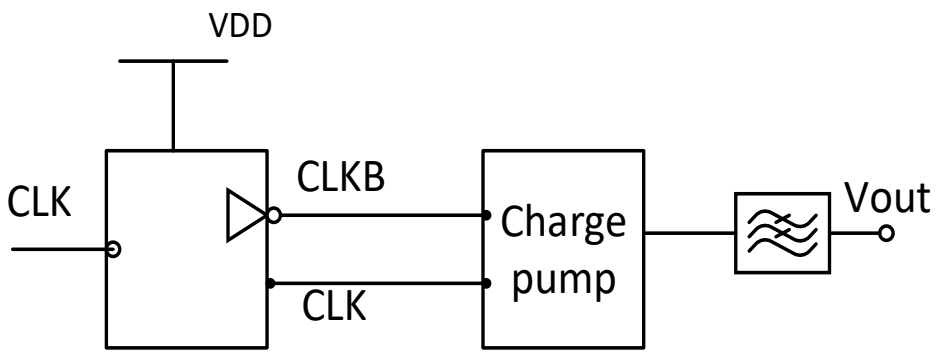


Figure 3-12 Block diagram of negative voltage generator

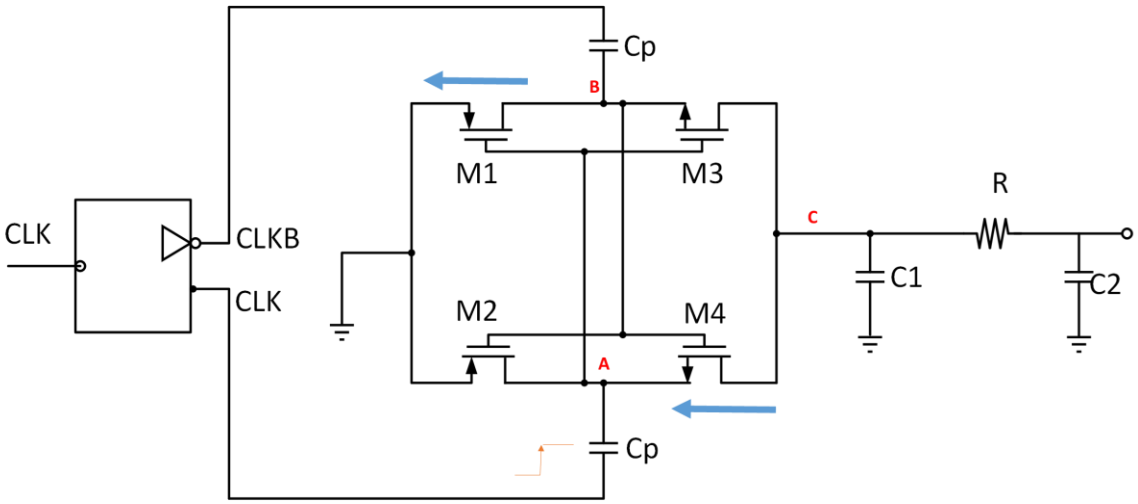


*Figure 3-13 Current flow during CLK rising to VDD *

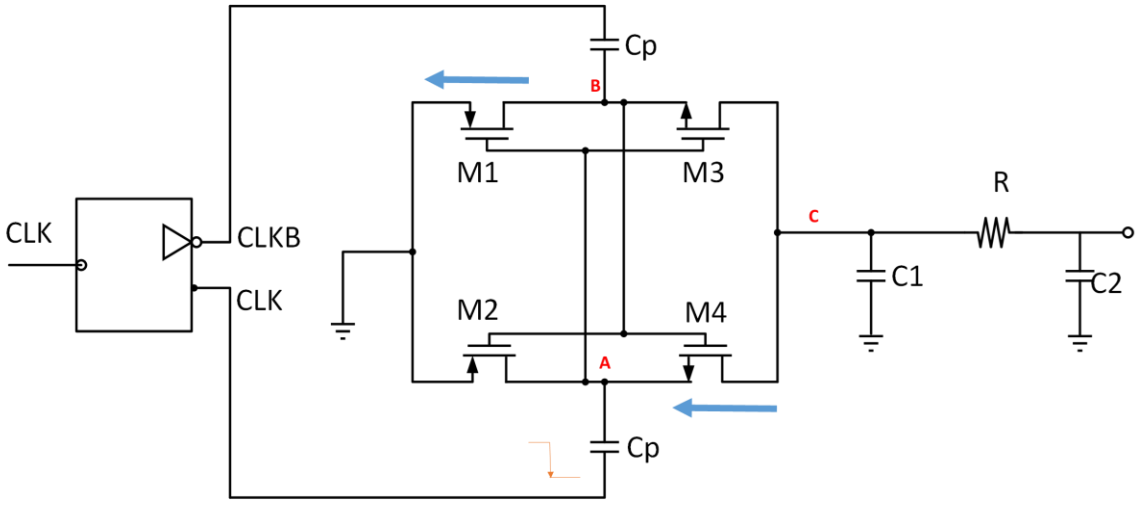


Figure 3-14 Current flow during CLK falling to GND

By setting the resistor R and capacitor C2 response time, the ripple on output negative voltage is filter out to generate a purified voltage to bias switch. The simulation result is shown in Figure 2 16. The output can reach -790mV.

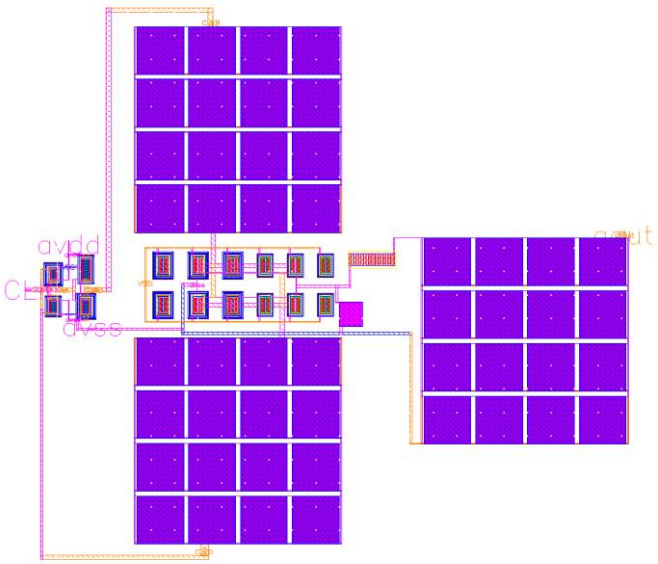


Figure 3-15 Layout of designed negative voltage generator

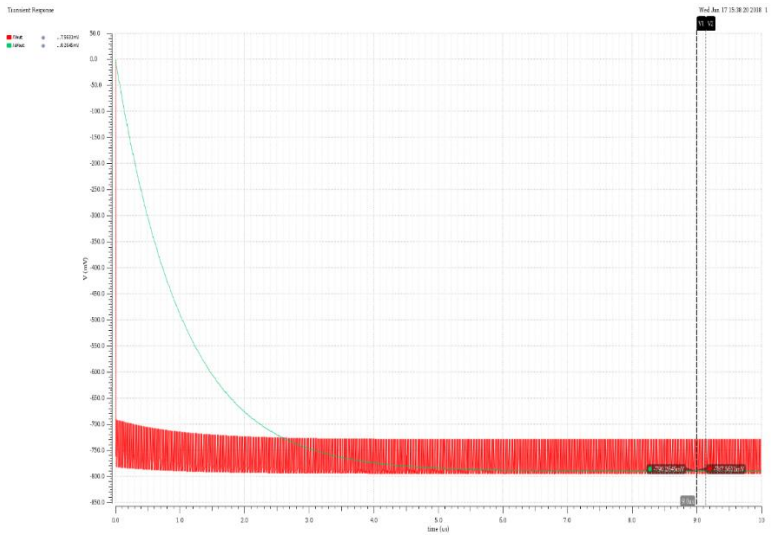


Figure 3-16 Simulation result of designed charger pump.

3.4.2. Switch Topology and design

To cover the wide bandwidth at sub-6GHz frequency range, series-shunt topology is a good candidate. The process used for this design is 22nm FDSOI (fully-depleted SOI) process. The advantage of FDSOI is that the threshold voltage features very low variation due to the fully-depleted channel does not have doping, therefore, the threshold voltage variation caused by channel doping process variation is eliminated. Another advantage is the body-bias technique. By applying voltage at the back node, the transistor performance can be tuned as shown in Figure 3-17.

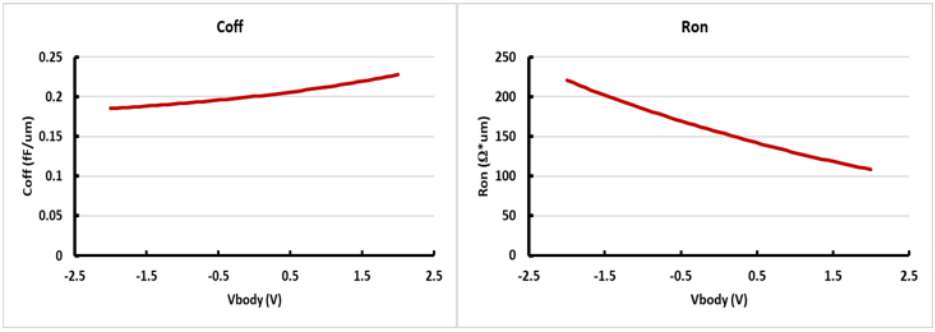


Figure 3-17 Ron and Coff change with body-biasing voltage

Figure 3-19 shows the schematic of the SPDT switch. 8 MOSs are stacked to handle a RF power up to 37 dBm. A 50KΩ resistor is connected to the gate to AC-float the gate node. The purpose is to prevent RF signal leakage and reduce RF voltage stress on gate oxide. So does for the body connection. To balance the voltage swing across each MOS, a 10K resistor is connected between source and drain for each MOS. For shunt branch, the stack number is the same as series branch considering power handling ability. The width and length of the series and shunt branch is listed in Table 3-1.

	Stack Number	Width (um)	Length (nm)	Rg (Ω)	Rds (Ω)
Series	8	2000	20	50	10K
Shunt	8	300	20	50	12K

Table 3-1 design parameters of SPDT switch

As shown in Figure 3-17 before. Decreasing bias voltage of NMOS with decrease its off-state capacitance and increase it's off-state resistance. This will benefit to the overall isolation performance of the SPDT switch.

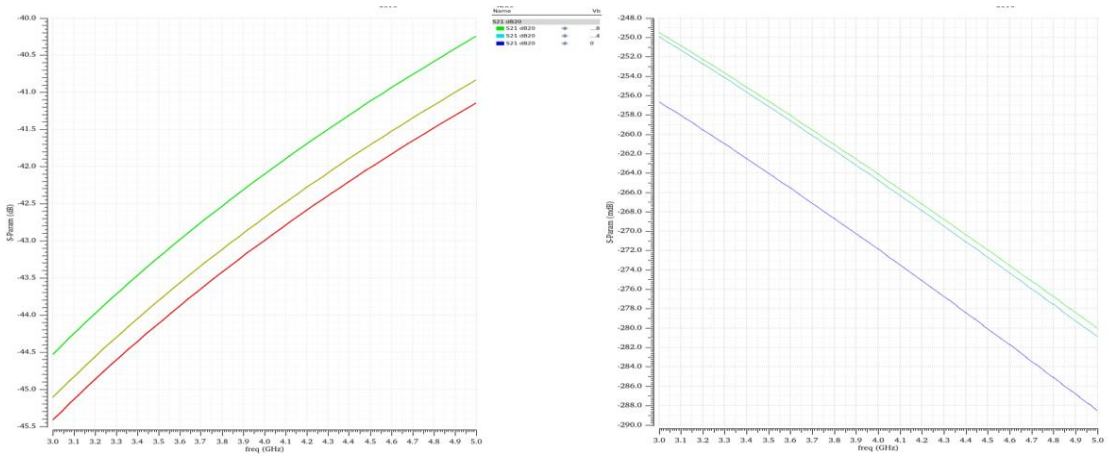


Figure 3-18 Simulated I.L. and Isolation with body bias voltage change

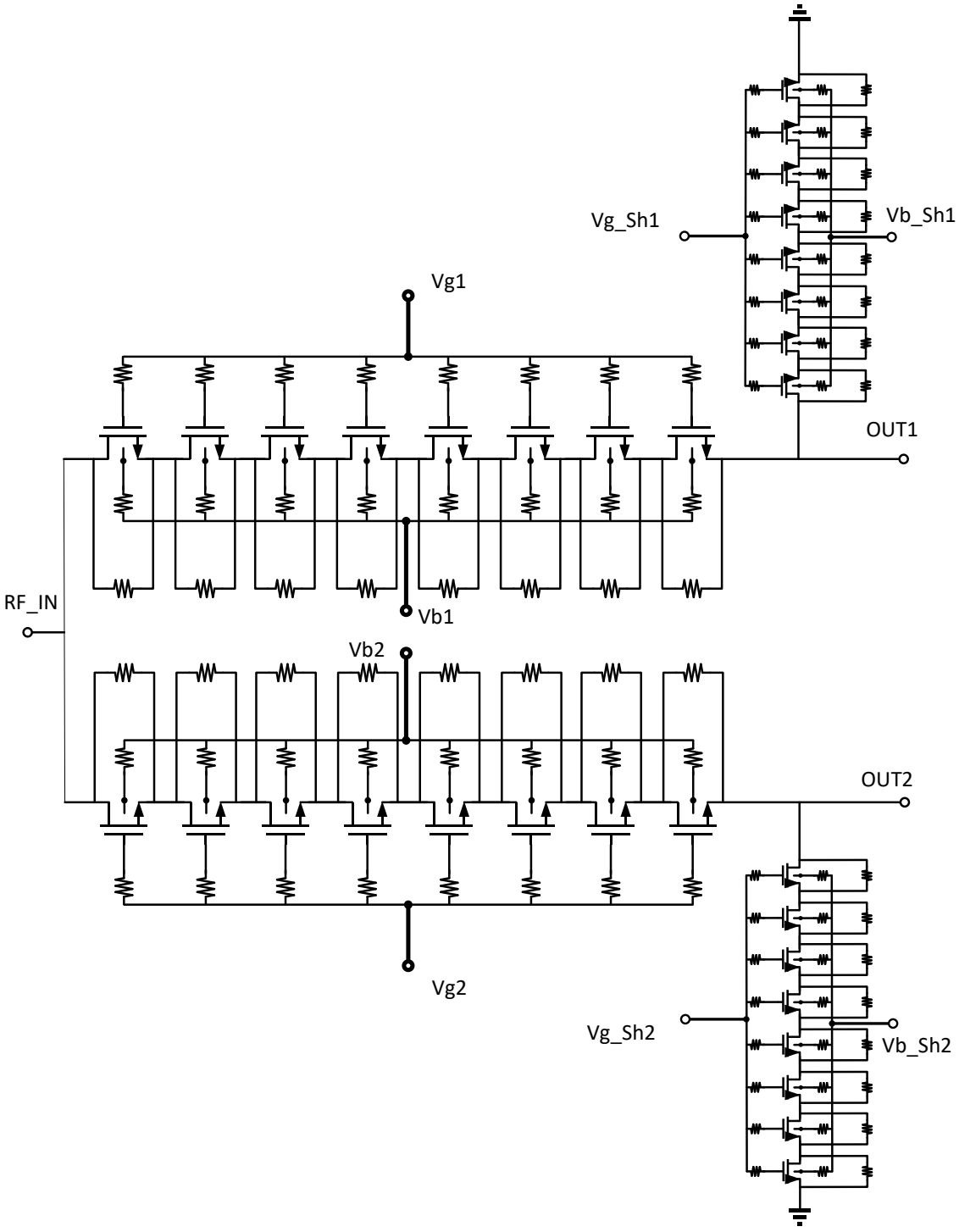


Figure 3-19 Schematic of SPDT switch core

Figure 3-18 confirms this assumption. When bias voltage changes from 0V to -0.8V, the isolation improves around 1dB from 3000-5000MHz. The insertion loss also improves slightly with a number of 0.006dB. The large signal performance of the designed SPDT switch is also simulated. Figure shows the high linearity of designed switch which achieved a 1dB gain compression point at 37dBm. The switching time is also simulated in time domain. The simulation result shows the turn on switching time is 0.3us.

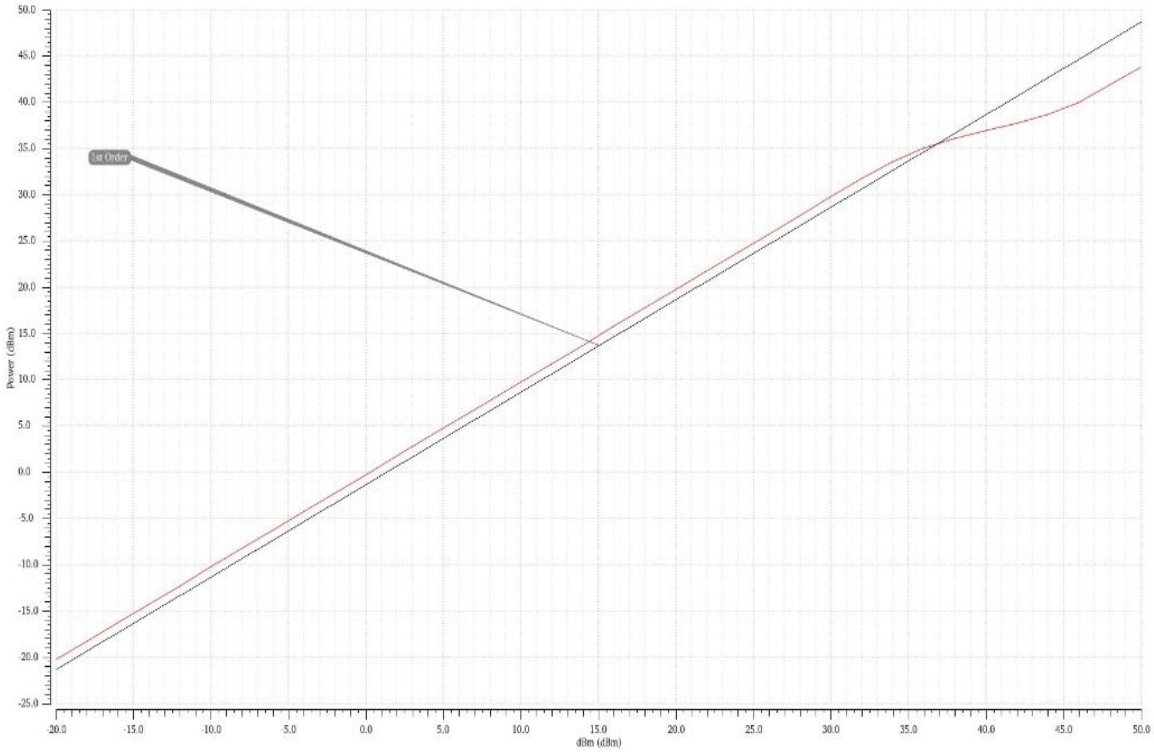


Figure 3-20 Simulated input P1dB of the SPDT switch

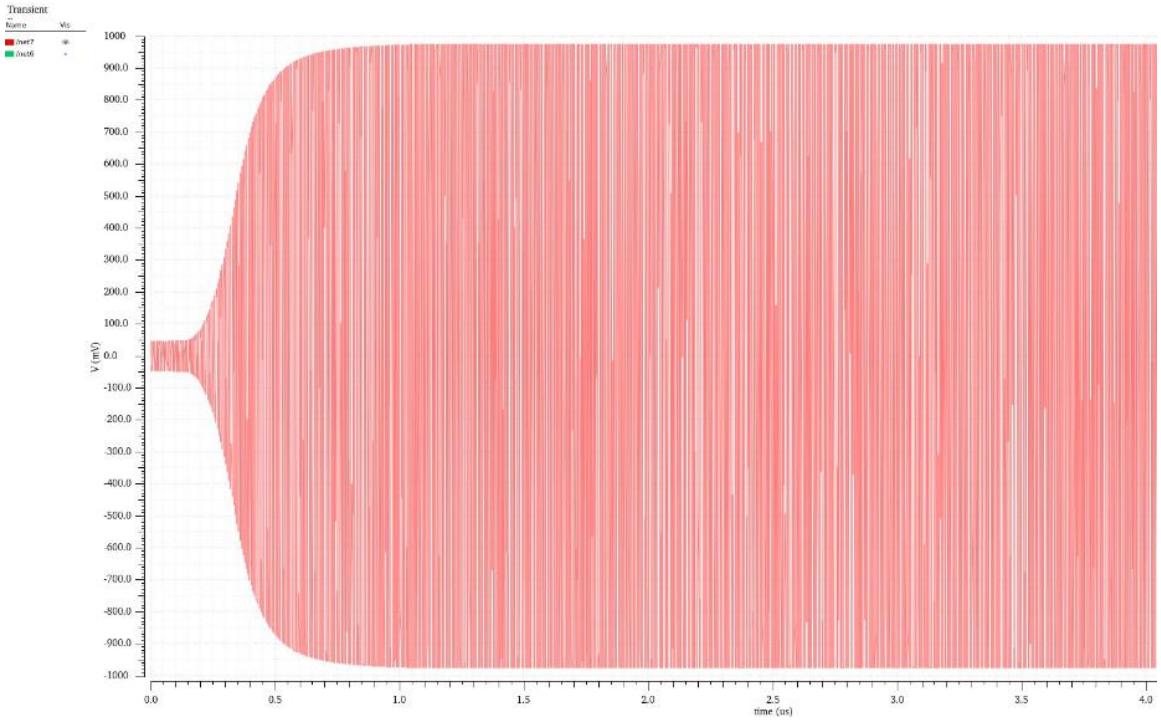


Figure 3-21Simulated switching time of designed SPDT switch

As a comparison, the simulation results are put in Table 3-2 in comparison with a industrial SPDT switch. The simulation result shows comparable performance with the industrial product.

Specs.	**Performance (simulation)**	**SKYA21038 (data sheet)**
Frequency range	3GHz-5GHz	0.6GHz-6GHz
Insertion loss	<0.3dB	0.5dB@2.4GHz
Isolation	>40dB	38dB@2.4GHz
P1dB	36.5dBm@3.5GHz	31dBm@2.4GHz
Switching speed	0.5us	2~5us*

* From SKYA21052 Antenna switch SP12T

Table 3-2 Simulation result of design SPDT switch in comparison with SKYA21038

Chapter 4. Millimeter Wave Switch design in SOI for 5G applications

RF switches are essential components for the RF front-ends of smartphone systems, especially for 5th generation (5G) mobile systems featuring rich frequency channels and utilizing time division duplexing transceiver architecture in millimetre-wave bands. To improve the power efficiency and sensitivity of transceivers, RF switches are required to have low insertion loss and high isolation. On the other hand, high integration has been a pursuit of IC designs for cellular chipsets for long. These are key design challenges in RF IC designs for 5G systems, especially for above-6GHz designs. From 3GPP 5G proposal, the high frequency bands around 28GHz and 38GHz will be used in FR2. In this chapter, I will present a travelling wave based 28GHz SPDT RF switch with robust on-chip ESD protection designed and fabricated in a foundry 22nm fully depleted SOI technology. This fully ESD-protected mm-wave SPDT switch covers the n257 and n258 bands of 5G systems, and demonstrates good insertion loss and isolation compatible to the state-of-the-art utilizing other process technologies. This design also shows the feasibility of high level integration with sub-6GHz RF front-ends in SOI CMOS.

4.1. Introduction of mm-wave switch design

Historically, high-performance RF switch design mostly uses III–V semiconductor-based processes or silicon-on-sapphire (SOS) technologies due to its high mobility and high power handling ability [11]. In these process a metal layer is often applied to the back side of die, which is very convenient to form a ground plane for microstrip line and mm-wave circuit design [12][13][14]. However, III–V semiconductor-based (for example, GaAs, and InP) and SOS technologies uses expensive substrate and features poor integration capability with digital circuits most of which use commercial silicon-based technologies. Bulk silicon process offers good capability of system integration and low cost, but suffers from poor linearity and high loss as high

power RF signal coupling to the low-resistivity silicon substrate [15][16][17]. Triple-well technique was reported, which shows improvement of the performance. In recent years, by using high-resistivity (HR) substrate, HR SOI technology has been penetrating into the switch market. With buried oxide isolate transistor and substrate, SOI reduced parasitic capacitance and substrate loss [18]-[19]. Trap-rich (TR) layer was late introduced to capture the free carriers at the interface of buried oxide (BOX) layer and HR Si substrate and eliminate parasitic surface conduction at the interface. SOI process achieves a balance between performance and cost, while maintains a capability of integration.

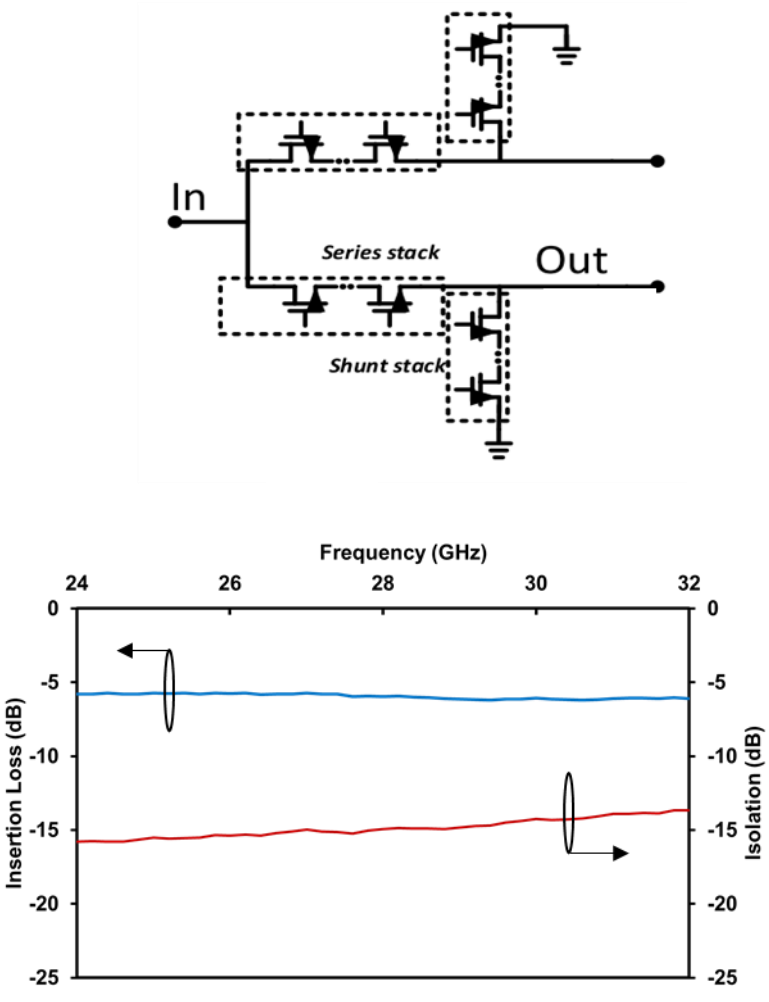


Figure 4-1 measurement result of SPDT switch on 28GHz using series-shunt topology [23]

Various topology is also reported for millimeter-wave switch design. The key fact that affects the design of mm-wave circuit is that as the frequency increase, the wavelength decrease to the scale of a circuit. Therefore, some electrical component can't be seen as a lumped device as in several gigahertz range. For example, transmission lines are used as conductor to replace simple one layer metal line. In several gigahertz frequency range, i.e. LTE, GSM bands, series-shunt type switch is widely used. In this topology, a shunt branch is added after the series branch to improve the isolation. However, mm-wave circuit is more sensitive to parasitic capacitance. The parasitic capacitance of the off branches in series-shunt switch degrades insertion loss and return loss to a large degree. Figure 4-1 shows the measurement result of our previous design on 28GHz using series-shunt topology [23]. The switch can only reach an insertion loss around 6dB and isolation worse than 16dB.

Therefore, various effort was done to improve the performance of conventional series-shunt switch. Lumped inductors are added to rematch the input and output impedance [20][21]. Later on, high quality factor inductive short stub transmission line is used to act as an inductor for impedance matching. However, since the impedance matching network is narrow band, the frequency response of these switch is also narrow band. On the other hand, the distributed switch concept has also been adopted to guide the design, where switch is used as a component to control the transmission line impedance. Depending on how the inductance is formed, distributed switch can be sort into artificial-transmission-line switch and travelling-wave switch.

4.2. Travelling wave switch basics

In RF world, typical transmission lines consist of two long conductors separated by some insulating material. Since the voltage and current of a transmission line vary with position and time, we have to characterize it by a distributed circuit model. Figure 4-2 shows the equivalent circuit model of a transmission line, where series inductor and shunt capacitor are placed periodically. In

the presence of imperfect conducting and imperfect insulating materials, voltage drop along the conducting line and leakage current between them exist, which can be modelled by a series resistor and a shunt conductor, respectively.

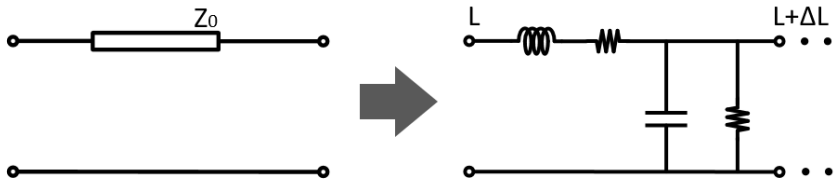


Figure 4-2 Equivalent circuit of transmission line

Characteristic impedance (Z0) of a transmission line is the ratio of the amplitudes of voltage and current of a single wave propagating along the line. The characteristic impedance can be calculated form the equivalent circuit model as $Z_0 = \sqrt{R + j\omega L/G + j\omega C}$. According to microwave theory, when the impedance of source and load conjugate match to each other, maximum power can be delivered to load. For RF switch used in a RF system, the output impedance of previous stage (i.e. antenna) and the input impedance of the next stage (i.e. duplexer) are both usually designed to 50ohm. Therefore, an ideal transmission line with 50ohm characteristic impedance can connect the source and load with no insertion loss. Figure 4-3 shows a schematic of an artificial transmission line formed by lumped elements. Lumped series inductors and shunt capacitors are placed periodically to simulate a transmission line whose characteristic impedance is controlled by carefully choose the L and C values to reach 50ohm.

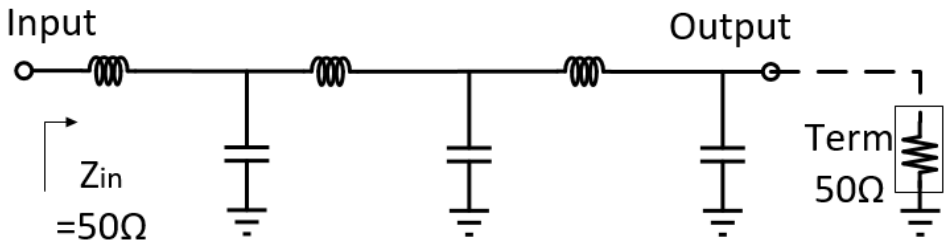


Figure 4-3 schematic of artificial transmission line

As shown in Figure 4-4, in a traveling wave switch, the inductive line is periodically loaded by shunt transistors. In the ON state, the inductive line with loaded off-state capacitances functions as a transmission line to pass the millimeter-wave signals, while in the OFF state, the shunt on-resistance shorts the millimeter-wave signal to ground. There exists an optimum number of shunt transistors for which the switch performance is a compromise between insertion loss and isolation. Figure 4-5 and Figure 4-6shows the simulated impedance looking into the SPST switch which uses coplanar waveguide line (CPL) and MOSFETs. From the smith chart, it's clear that when MOSFET turns off, the inductive CPL and capacitance of MOSFETs forms a 50ohm transmission line. However, when the switch turns on, the impedance is significantly away from 50ohm. Therefore, most input RF signal are reflected back, in other word, almost no power can be received on the load.

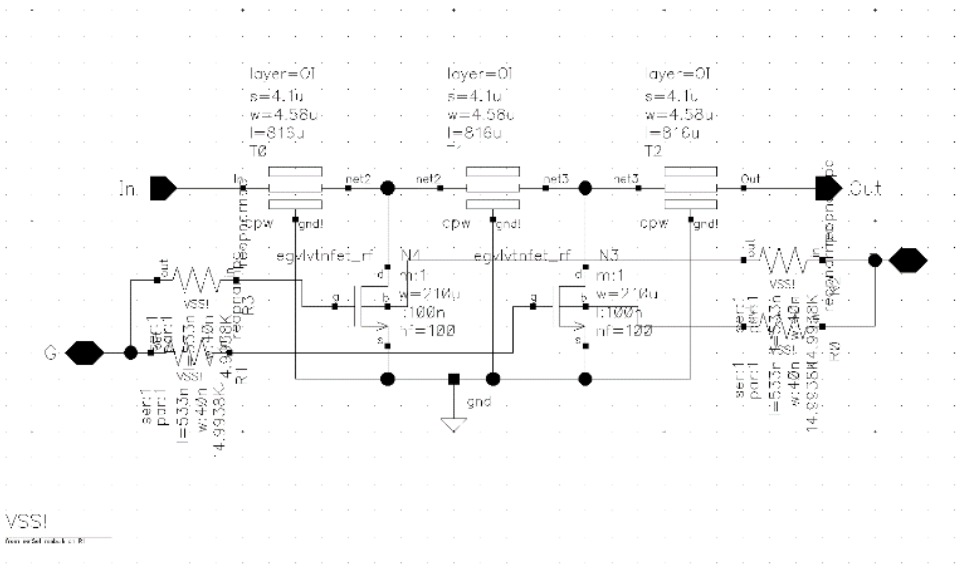


Figure 4-4 Schematic of a SPST travelling wave switch

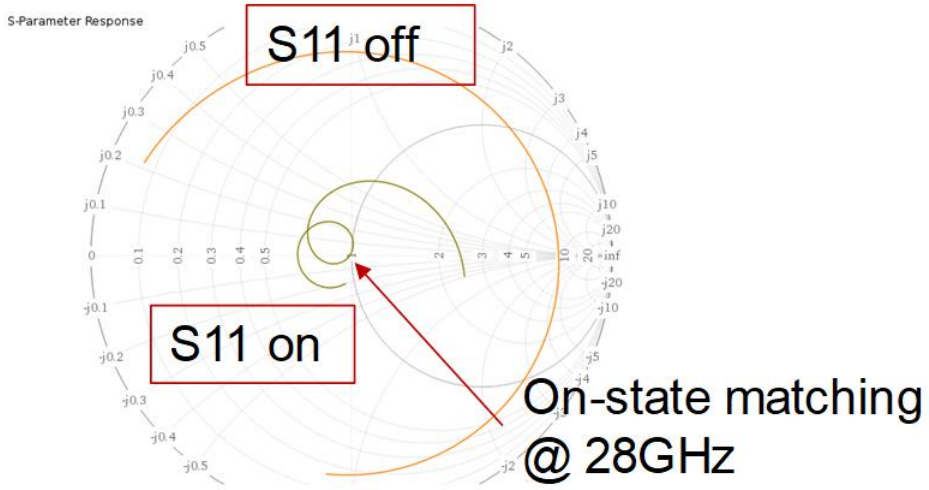


Figure 4-5 Input impedance of on and off state of SPST switch

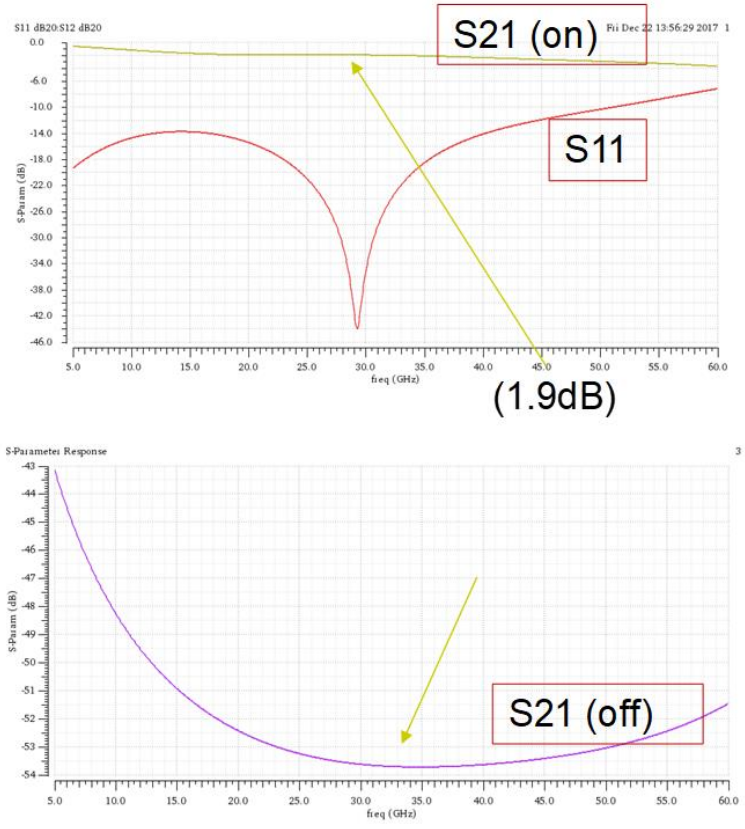


Figure 4-6 Simulated S21 of on and off state

To apply this concept on SPDT or SPnT switch, the off-state branch can't load the on-state branch. Thus, an impedance transformer is needed to transform the small impedance to almost open. There are mainly two ways to achieve this: the first is use 50ohm quarter wave transmission line to rotate the phase of off branch impedance to high side. Due to the high Q factor of transmission line, this method introduce less insertion loss. However, quarter wavelength transmission line has very narrow bandwidth, which is a drawback. Another solution is to add another series transistor to control on signal path. As transistor adds additional resistance to the signal path, this solution will expect more loss.

4.3. Travelling wave switch design in SOI

4.3.1. Circuit design

Conventional series-shunt transistor topology shows excellent switch performance under 6 GHz [22]. However, for higher frequency such as 28GHz, the performance of series-shunt transistor switches degrades severely [23]. Recently, various techniques were reported to design millimeter wave RF switches. For example, [24] and [25] utilized channel mobility and body floating enhancement techniques to improve insertion loss and isolation of conventional series-shunt FET based switches, respectively. [26][27] report improvement of switches using on-chip inductance-capacitance (LC) matching techniques. Alternatively, travelling wave based switch topology becomes attractive for broadband mm-wave switches [28][29] in GaAs HEMT and bulk CMOS. This design adopts the travelling wave topology for 28GHz SPDT switches in 22nm FD-SOI for 5G systems.

Figure 4-7 depicts the schematic of the SPDT switch designed in a foundry 22nm FD-SOI technology. The three-stage travelling wave structure comprises inductive transmission lines and transistors. Due to the relatively low frequency for this switch, the travelling wave structure does

not use quarter-wave transmission lines because they would consume too large die area and the long trace would increase insertion loss typically for non-ideal lossy transmission lines. The series transistors (M1, M2) provide extra control of the switch status and improve the isolation. To improve the power handling ability, thick oxide long channel NMOSFETs are used for the series and shunt transistors (M1-M8). The FET sizes are optimized by simulation to be L = 100nm for M1-M8, W = 115μm for M1 and M2, and W = 20.3μm for M3-M8. Under 1.8V operation voltage the on-state resistance is 3.6Ω and the off-state capacitance is 21.5fF for M1 and M2. The on-state resistance is 17Ω and off-state capacitance is 6.3fF for the shunt FETs M3-M8. A 10KΩ resistor is added to the gate to prevent leakage. The inductive transmission lines with characteristic impedance of 70Ω form the distributed switch.

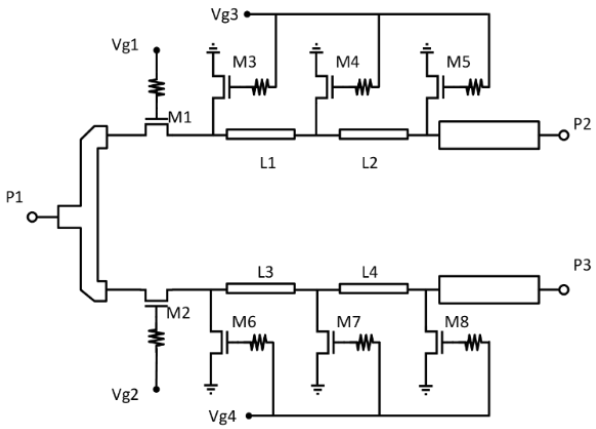


Figure 4-7 Schematic of the SPDT traveling wave switch design in this work.

The design is optimized in ADS to determine the parameters of inductive transmission line and transistors. Then, width was determined for transistors. According to the optimized characteristic impedance and electrical length, microstrip line is carefully design and simulated in HFSS. After layout works, the parasitic effects of active devices are extracted from pex r+c+cc for both on-state and off-state. Then the performance of the whole circuit is verified in cadence with S-parameter extracted from HFSS. Whole Back-end-of-Line (BEOL), including testing pad, of the

travelling wave switch is simulated using full EM tools (HFSS). Ports are set at each connection toward active device (MOS). Figure 4-9 and Figure 4-10shows the 3D model of the structure and the simulation procedure.

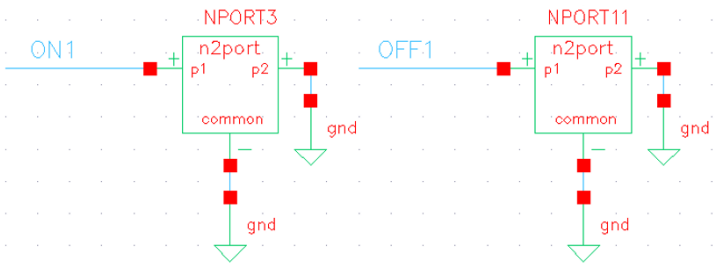


Figure 4-8 Extracted S parameter file with on/off state

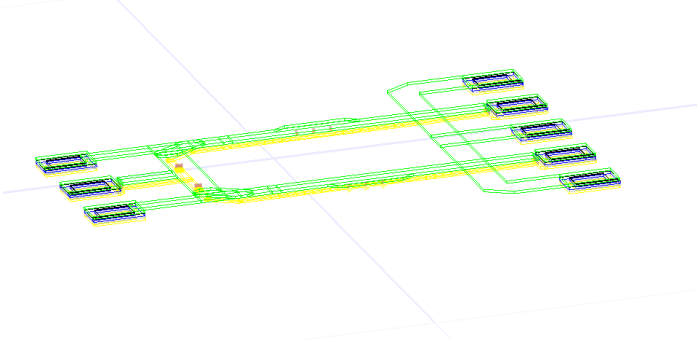


Figure 4-9 HFSS EM model of microstrip line switch BEOL

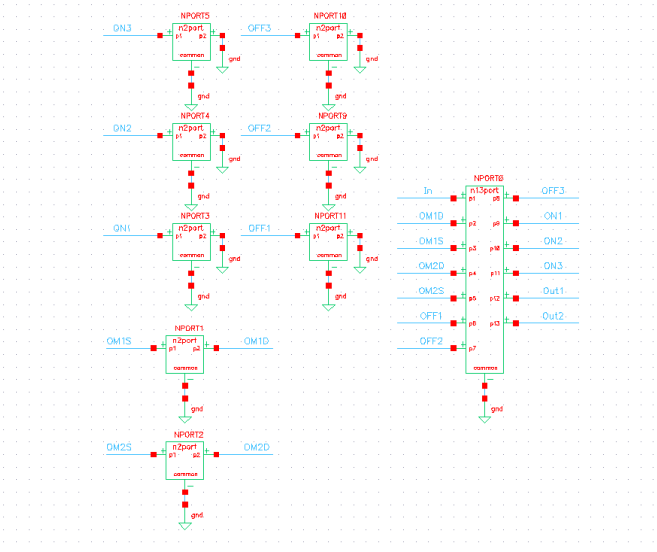


Figure 4-10 Cadence co-simulation test bench with extracted EM model

4.3.2. Microstrip Line design

Comparing with a co-planar waveguide, a microstrip line takes less area and is easier to realize. In HEMT technology, a metal layer is often applied to the back side of die to form a ground plane. In CMOS and SOI technologies, conventional microstrip line often uses the top metal as the signal line and the bottom metal (ML1) close to Si as the ground plane, which is typically three time wider than the signal line. However, in advanced CMOS technologies, the maximum width of ML1 is strictly limited by the design rules. To solve this layout problem, the wide ML1 ground plane is often slotted as depicted in Figure 4-12. Unfortunately, a slotted ML1 ground plane introduces many problems: the sheet resistance (R) increases substantially compared with a continuous ML1 ground plane and the impedance discontinuity due to the openings leads to higher loss, which will seriously affect switch performance. Figure 4-12c shows the simulation result of two microstrip lines of same layout dimension, but with and without slots. It clearly observed that the slotted ground microstrip line induces about 1.5 times of loss over the non-slotted ML1 line.

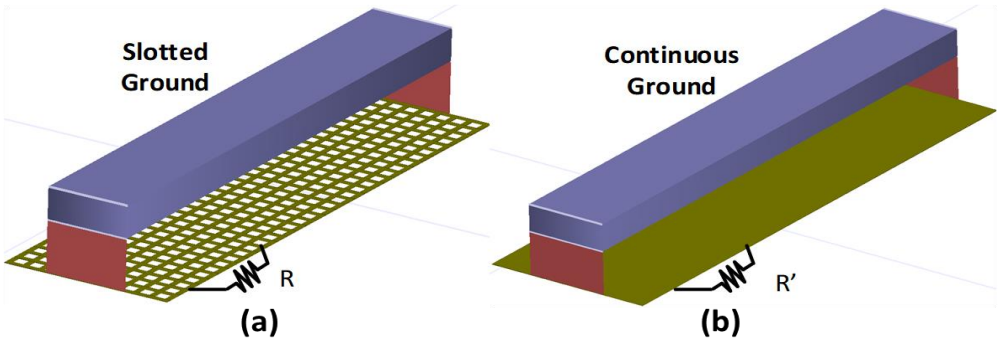


Figure 4-11 Comparison of microstrip lines: (a) Case-1 uses ML9-ML1 with slots in the ML1 ground plane, (b) Case-2 uses ML9-ML1 without slots in the ML1 ground plane

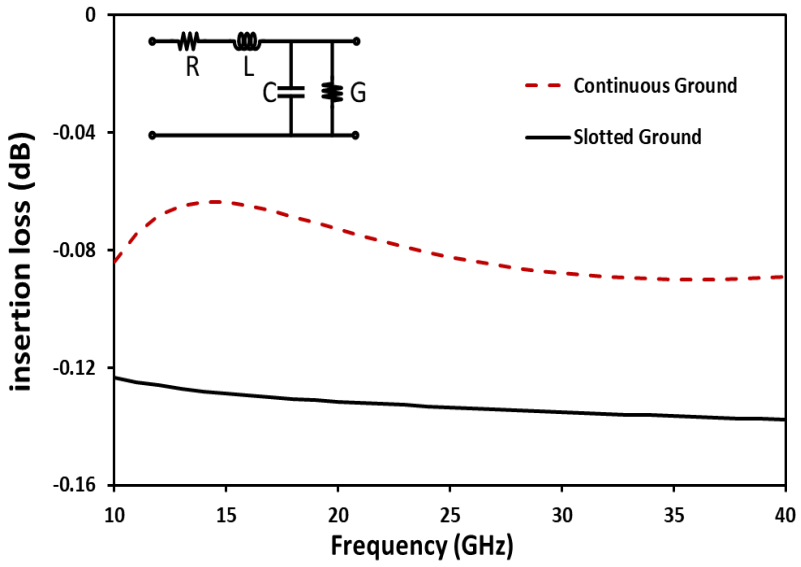


Figure 4-12 Insertion loss (normalized to the same βL) for the two 50Ω microstrip lines by HFSS simulation.

The 22nm SOI technology used in this design has 11 metal layers as shown in Figure 4-13. We studied three layout cases of forming the 50-ohm transmission line by EM simulation, all using ML9 metal as the signal line: Case-1 and Case-2 using slotted and non-slotted ML1 as the ground plane, respectively, and Case-3 having the top ML11 (LB) as the ground plane. Case-3 has the layout advantage that LB is very thick and its width is not limited by the design rules, i.e., no slots are needed. The comparison of insertion loss for the three cases were studied by HFSS simulation with the results shown in Figure 4-12 and Figure 4-14. For meaningful comparison, the simulation results are normalized to the same electrical length. Clearly, Case-3 (ML9-LB microstrip line) induces much lower insertion loss than Cases-1, about three times less. From full-chip layout point of view, using the ML9-LB microstrip line (Case-3) also makes interconnection with active devices much easier since the LB metal trace will not be blocked by the lower layer metals.

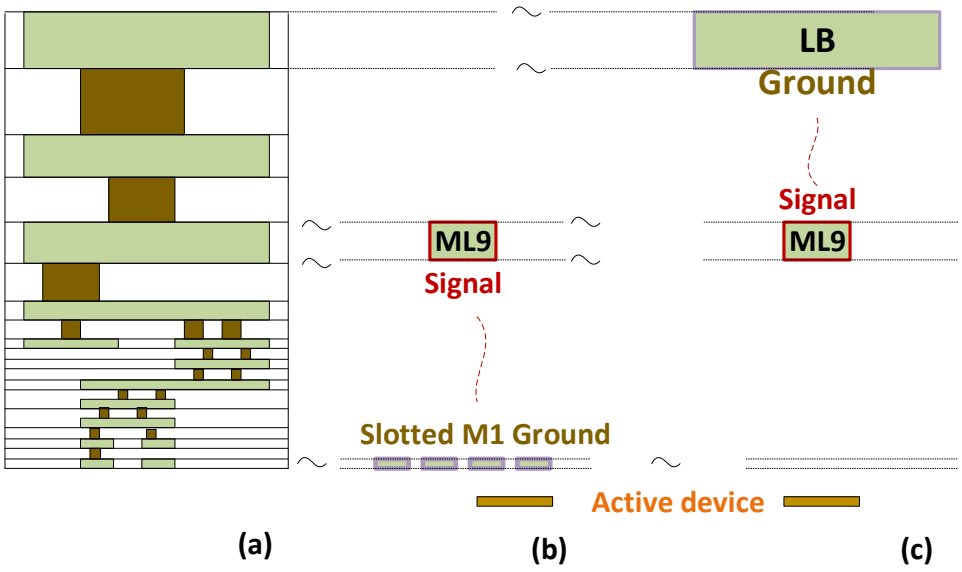


Figure 4-13 Illustration of the two microstrip line cases: (a) 11-metal stack in 22nm SOI, (b) Case-1 of ML9-ML1 with slots, (c) Case-3 of ML9-LB microstrip lines. The distances of ML9-ML1 and ML9-LB are almost same.

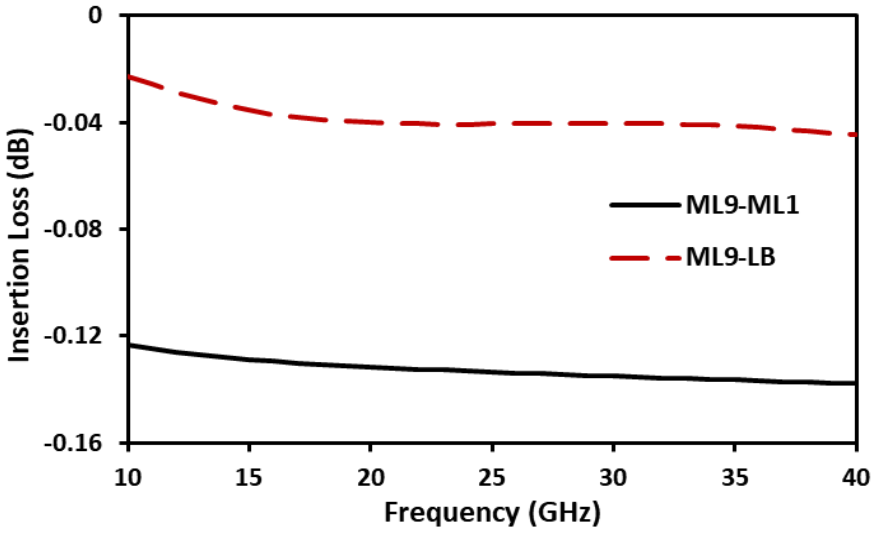


Figure 4-14 Comparison of insertion loss (normalized to the same βL) between Case-1 of ML9-ML1 with slots and Case-3 of ML9-LB microstrip lines by HFSS simulation.

4.3.3. Measurement result

The 28GHz switches were fabricated in a foundry 22nm FD-SOI CMOS technology. Figure 4-17 shows the die photo for the SPDT switch that has a chip size of 0.66×0.64 mm2 (including test pad). S-parameter measurement was conducted at die level using RF probe station and Agilent-E8363B from 5GHz to 40GHz. Two-port S-parameters were calibrated to the GSG probe tips using an SOLT calibration kit. Figure 4-19 shows the measured S-parameters for the SPDT switches. This design has two design splits: SPDT without ESD protection and SPDT with ESD protection. From 5GHz to 20GHz, the SPDT switch without ESD protection achieves insertion loss range from 1.0dB to 3.1dB and isolation better than 30dB. Across n257 and n258 band (24.25-29.5GHz) for 5G, the insertion loss is better than 3.9dB and the isolation is better than 23dB. It shows that this 28GHz SPDT switch design in 22nm FD-SOI has good performance comparable to reported mm-wave switches designed in HEMT and bulk CMOS technologies

4.4. Travelling wave switch ESD protection and co-design

4.4.1. ESD PROTECTION

Electrostatic discharge (ESD) failure is a huge threat to any consumer electronics, particularly smartphones because the ESD risk exists all the time and becomes more dangerous as more advanced IC technologies are used for mobile chips. ESD protection design is very challenging for RF and high-speed ICs [30][31]. While ESD protection for antenna switches were well studied, ESD protection design for mm-wave switches is an emerging challenge [22][23].

Robust ESD protection is designed for the 28GHz switches in this work targeting for 9KV HBM ESD protection. To eliminate the switch power dropout caused by ESD leakage, a diode-string ESD protection structure with 4 diodes in series is designed to protect the 28GHz switch at the output ports as shown inFigure 4-15. The 4-diode-string ESD structure has an ESD triggering

voltage of ~2V and is designed to ensure 19dBm output power. The ESD-induced parasitic capacitance of this 4-diode-string ESD device is estimated to be CESD ~ 40fF from the PDK. While CESD ~ 40fF seems to be small, it does have significant adverse impacts on the 28GHz mm-wave switches, which will be discussed in the Measurement Section.

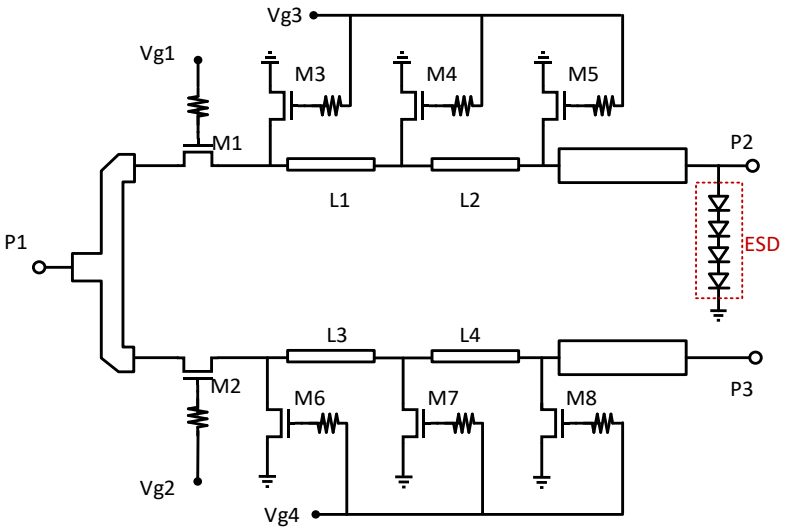


Figure 4-15 4-diode-string ESD protection is used to protect the 28GHz switches.

4.4.2. Co-design

For broadband application, an inductor is usually put in series with the ESD device as shown in Figure 4-16(a), where the LC resonate frequency is set far away from application bands [24]. However, it's risky under charged device model (CDM), as the inductor will create a delay for ESD device discharge the CDM ESD surge, whose frequency can reach several Giga Hz. As chip size increasing and the thriving progress of system-on-chip (SOC), high volume charge is easier to accumulate during manufacturing, which exacerbates the CDM threats. To elevate this problem, in this work, a series inductor is put before ESD device to draw the impedance closer to 50 ohm. Under CDM event, this inductor will cause a delay for ESD discharging into circuit, thus, gives ESD device more time to discharge CDM current. By adding a series inductor, the matching is also

improved because the impedance is draw to lower VSWR circuit as shown in the smith chart in Figure 4-16(b).

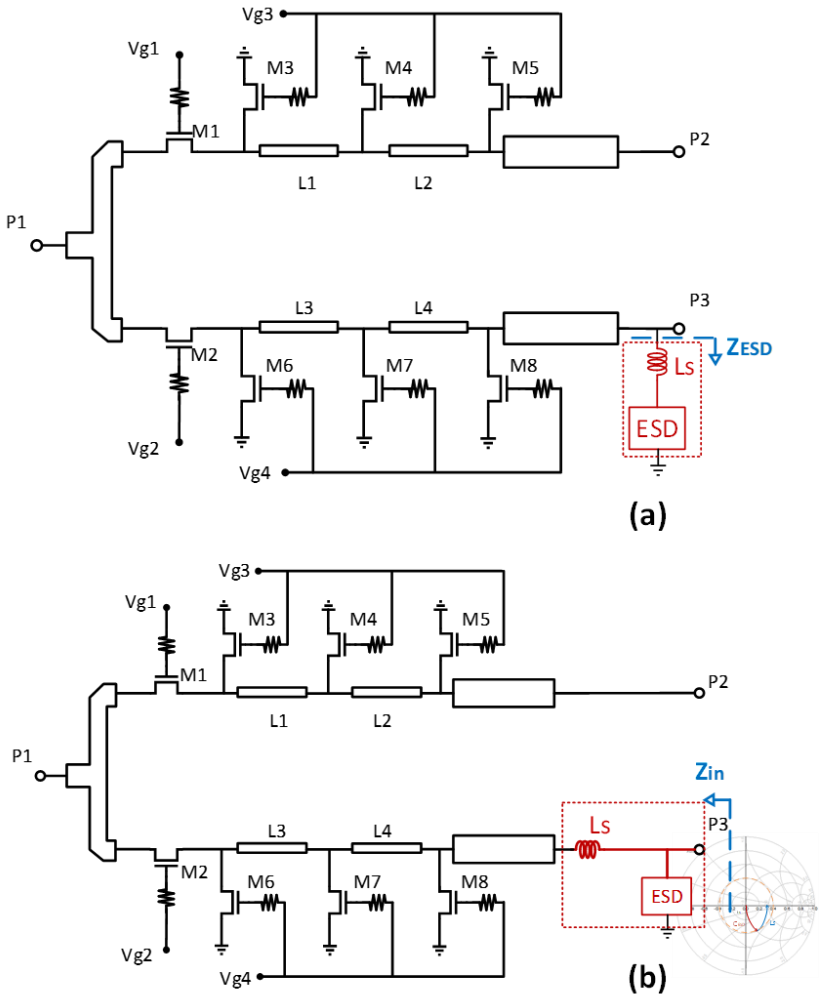


Figure 4-16 (a) Conventional broadband ESD protection co-design method (b) ESD co-design used in this work.

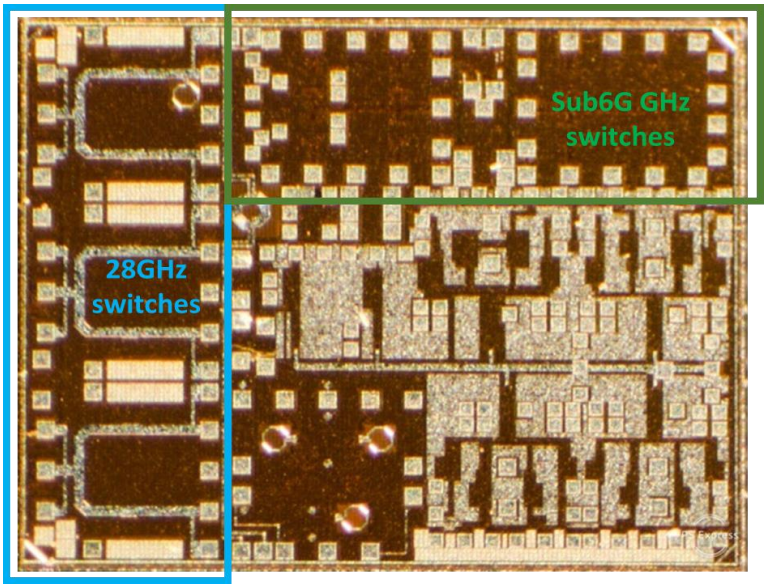


Figure 4-17 Die photo for designed 28GHz switches and sub6GHz switches.

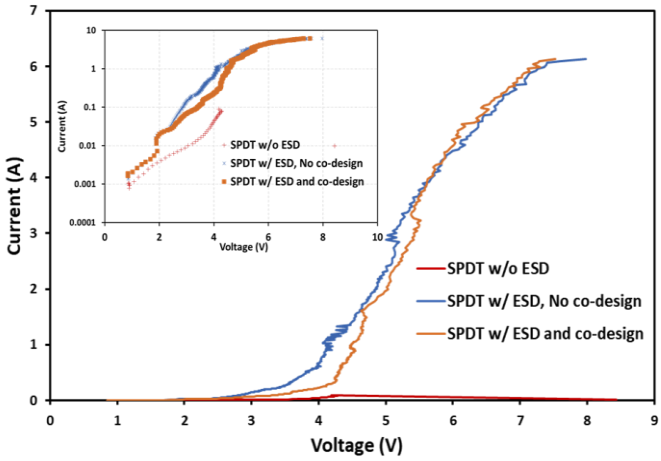


Figure 4-18 Measured 100ns TLP I-V curve for SPDT switch of three splits featuring (1) without ESD protection, (2) with ESD protection, but no co-design optimization, (3) with ESD protection and co-design optimized.

4.5. Measurement and discussion

The 28GHz switches were fabricated in a foundry 22nm FD-SOI CMOS technology. Fig. 6 shows the die photo for the SPDT switch that has a chip size of 0.66×0.64 mm2 (including test pad). S-parameter measurement was conducted at die level using RF probe station and Agilent-E8363B from 5GHz to 40GHz. Two-port S-parameters were calibrated to the GSG probe tips using

an SOLT calibration kit. Figure 4-19 shows the measured S-parameters for the SPDT switches. This design has two design splits: SPDT without ESD protection and SPDT with ESD protection. From 5GHz to 20GHz, the SPDT switch without ESD protection achieves insertion loss range from 1.0dB to 3.1dB and isolation better than 30dB. Across n257 and n258 band (24.25-29.5GHz) for 5G, the insertion loss is better than 3.9dB and the isolation is better than 23dB. It shows that this 28GHz SPDT switch design in 22nm FD-SOI has good performance comparable to reported mm-wave switches designed in HEMT and bulk CMOS technologies, as summarized in Table 4-1.

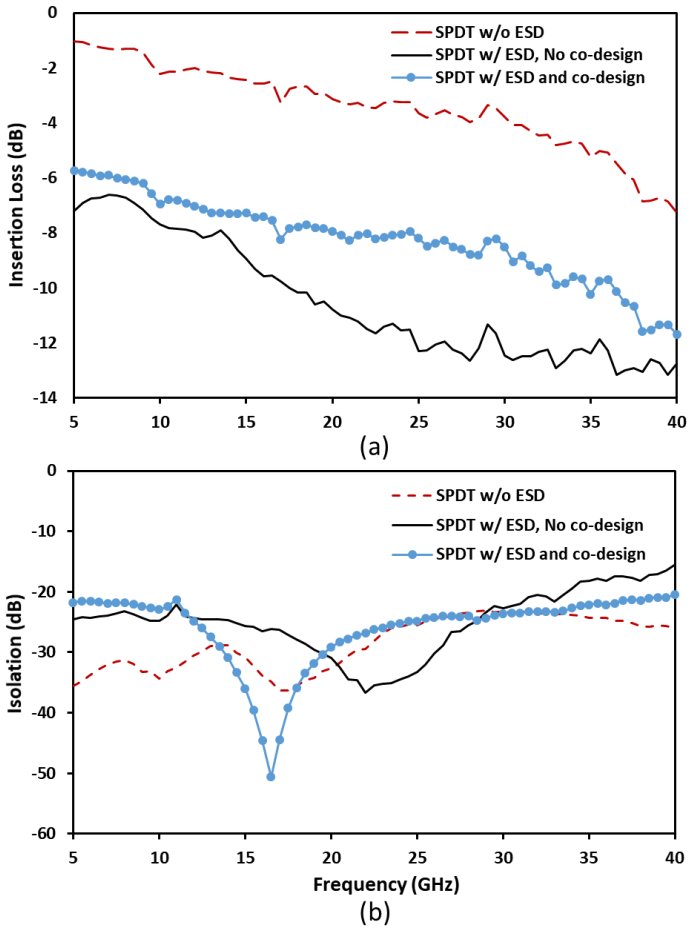


Figure 4-19 Measured insertion loss and isolation for SPDT switch of three splits featuring (1) without ESD protection, (2) with ESD protection, but no co-design optimization, (3) with ESD protection and co-design optimized.

It is worth noting that, to our best knowledge, this may be the first travelling wave SPDT designed in FD-SOI with a center frequency of 28GHz for 5G n257 and n258 bands, while the other mm-wave switches may have limited comparison meaning. HBM ESD performance was measured using transmission line pulsing (TLP) ESD tester (Barth 4002) featuring a rising time of 10ns and duration time of 100ns for the ESD pulses. Figure 4-18 shows that, without on-chip ESD protection, the SPDT switch can only handle a low ESD current of 0.1A due to self-protection, equivalent to ~150V. With the 4-diode-string ESD protection in place, the SPDT switches can readily handle very large ESD transients of at least 6A, equivalent to HBM ESD protection level of ~9KV. To our best knowledge, this is the first reported mm-wave TRx switch for 5G with robust full-chip ESD protection. On the other hand, Figure 4-19 also shows significant impacts of ESD protection on switch performance, leading to substantial degradation of insertion loss, ~6dB at low frequency and ~8.7dB at 28GHz. After careful co-design, the insertion loss improve ~4db and remains the same isolation comparing with simple ESD add-on.

Table 4-1 Meaningful mm-wave switch performance comparison.

Ref.	Process	Frequency (GHz)	Topology	Insertion Loss (dB)	Isolation (dB)	ESD	Die size (mm^2)
[24]	130nm SOI	DC-50	Series-shunt with mobility enhancement by SMT	<2.1* 0.93@28GHz	>27 33@28GHz*	No	0.041
[25]	130nm CMOS	DC-28	Series-shunt with enhanced body floating	<2.5* 2.1@28GHz	>15* 16@28GHz	No	0.015
[26]	65nm CMOS	25-39.5	Series-shunt with matching inductor	<1.9 1.06@28GHz	>25 -39@28GHz	No	0.01
[27]	180nm SOI	DC-40	Series-shunt with matching inductor	<5* 2.3@28GHz	>17* 17@28GHz	No	0.025
[28]	90nm CMOS	DC-60	Travelling wave	<3* 2.2@28GHz	>48 60@28GHz*	No	0.59**
[29]	180nm CMOS	DC-50	Travelling wave	<6* 5@28GHz	>26* 27@28GHz	No	0.25**
This work	22nm FD-SOI	DC-30	Travelling wave without ESD protection	<3.9 3.9@28GHz	>23 24@28GHz	No	0.16
This work	22nm FD-SOI	DC-30	Travelling wave with ESD protection	<12.6 12.6@28GHz	>22 25@28GHz	9KV	0.42**
This work	22nm FD-SOI	DC-30	Travelling wave with ESD protection	<8.8 8.8@28GHz	>22 24@28GHz	9KV	0.42**

* Estimated value from the reported graph ** Chip size includes testing pads

Chapter 5. High area efficiency ESD device and temperature concern

Form result shown in previous chapter, ESD parasitic shows severe degradation to SCR performance. In this chapter, we will discuss novel low parasitic high area efficiency ESD device and design concern on these devices.

5.1. Cell-By-Cell SCR

As semiconductor technologies scale down to nanoscale, fabrication process is becoming more and more complex, leading to rapid increase in Si die costs. One the other hand, as IC function continues getting more complicated, chip size becomes a major concern in new designs. Unfortunately, ESD protection never scaled down per the Moore's Law [32][33]. In fact, as IC technology scaling continues and IC complexity increases, ESD protection design emerges as a major IC design challenge due to several key disadvantageous factors: ESD-induced parasitic effects, ESD layout style and size, and ESD discharging uniformity [30][31]. Silicon-Controlled Rectifier (SCR) and its derivatives are considered efficient ESD protection structures due to many advantages: high current handling ability, high ESD robustness, small size and low parasitic effects [32]. Hence, SCR-type ESD protection structures are becoming popular in the IC industry [34][35]. For example, low-triggering multi-directional SCR ESD structures in CMOS, SCR ESD structure in LDMOS [36], and waffle structured SCR ESD structures [37] were reported. However, designing robust area-efficient SRC ESD structure is still an active topic. This paper reports a new cell-by-cell SCR ESD protection structure for better layout efficiency and ESD discharging performance.

5.1.1. Cell-By-Cell SCR ESD structure

Figure 5-1.a depicts a common multi-finger parallel layout for conventional SCR ESD protection structures. Large body pick-up fingers are normally used to achieve even current conduction. Further analysis of SCR ESD working mechanism suggests that a body pick-up mainly serves to trigger an ESD structure. After ESD triggering, a body pick-up plays little role in discharging large ESD current. Hence, a body pick-up can be shared by adjacent SCR ESD cores (P-doping/N-well/P-well/N-doping) for better layout efficiency. Further, the body pick-ups in the edge SCR cores (Fig. 1b) can also be redesigned to improve layout efficiency.

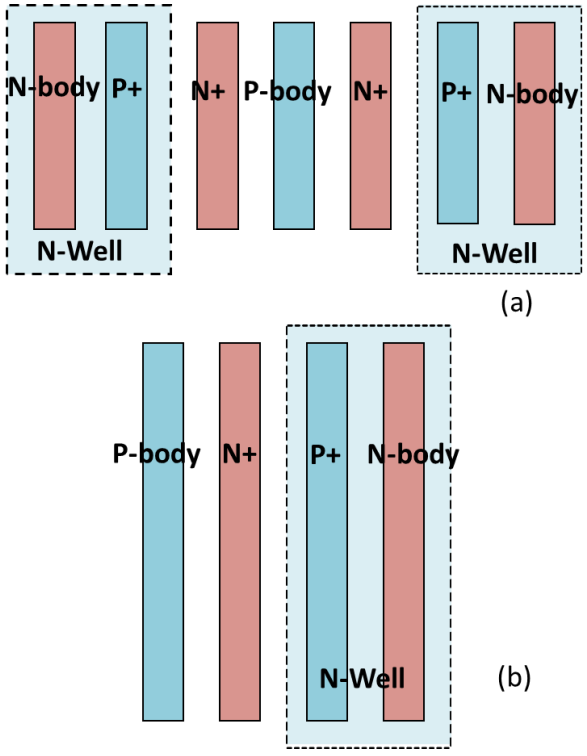


Figure 5-1 Top view of conventional SCR ESD layout: (a) multi-finger layout and (b) classic parallel finger layout.

In this section, we proposed and demonstrated a novel cell-by-cell across-boundary SCR ESD structure for better area efficiency and ESD discharging uniformity. Fig.2 depicts the new cell-by-

cell SCR ESD protection structure including its cross-section showing the SCR ESD discharging mechanism. The new ESD structure has two types of cells: Anode cell (A-cell) and Cathode cell (K-cell). The A-cell features an N+ body pick-up of Nwell surrounded by a P+ ring with STI isolation in between. Fig. 3 shows that the current flowing into the N+ pick-up in A-cell serves to trigger the SRC ESD structure. The K-cell consists of a P+ body pick-up of Pwell enclosed by an N+ ring separated by STI isolation.

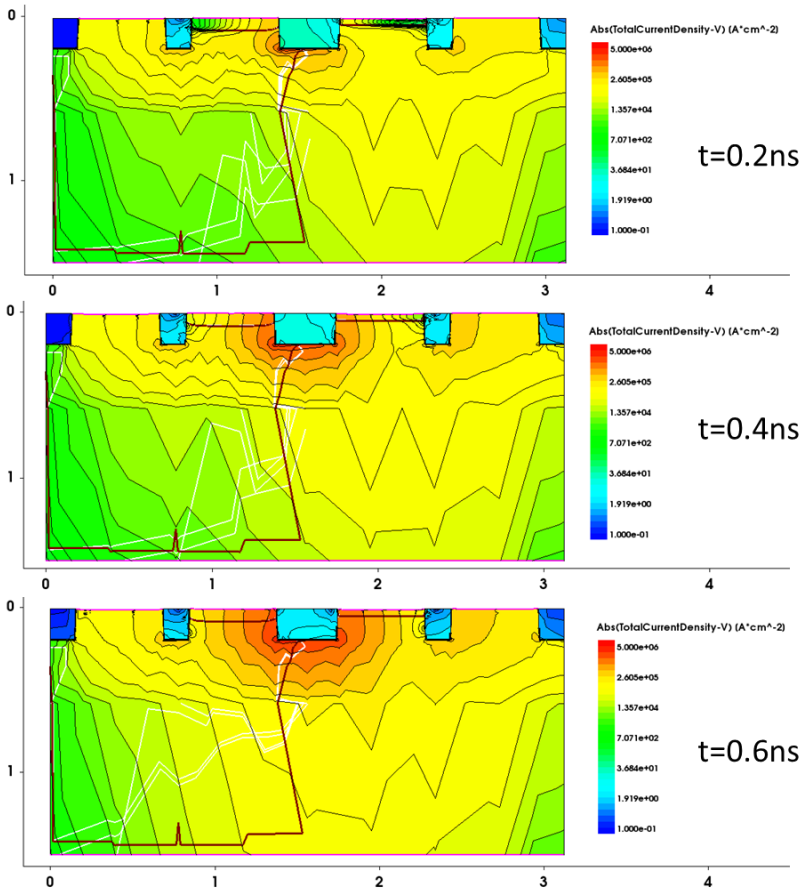


Figure 5-2 TCAD simulation result of planar SCR shows that body pickup conducts very small current during the whole ESD event.

The new SCR ESD structure is formed by an array of A-cells and K-cells placed alternatively against each other as shown in Figure 5-4. All same-kind cells are connected together by metal

lines. Figure 5-3 gives a cross-section of a K-cell surrounded by A-cells. It shows that from the A-cell to the K-cell, a basic SCR core of PNPN structure (i.e., P+/Nwell/Pwell/N+) is formed across the A-cell and K-cell boundary. Different diffusion regions are isolated by STI. For each cell, four cross-boundary SCR cores will be formed to discharge ESD surges. There are several key advantages for this new cell-by-cell SCR ESD structure: First, the cell structure is more area efficient than traditional parallel finger type SCR ESD structure. Second, using small cells improves ESD discharging uniformity (Figure 5-5), which is critical for high ESD protection level. Evenly distributed ESD discharging current around the boundary of a small cell will alleviate possible ESD current crowding, typically in large ESD protection structures, and eliminates ESD discharging hot spots. Third, the cell structure is scalable in layout according to specific ESD protection design target. Fourth, compared to finger-type SRC ESD structure, the cell-by-cell SCR structure is more layout-friendly, making full chip floor planning easier. Fifth, area efficiency will result in minimized ESD-induced parasitic effects. Overall, it is expected that the new cell-by-cell SCR ESD protection structure is more area efficient, layout friendly and ESD robust.

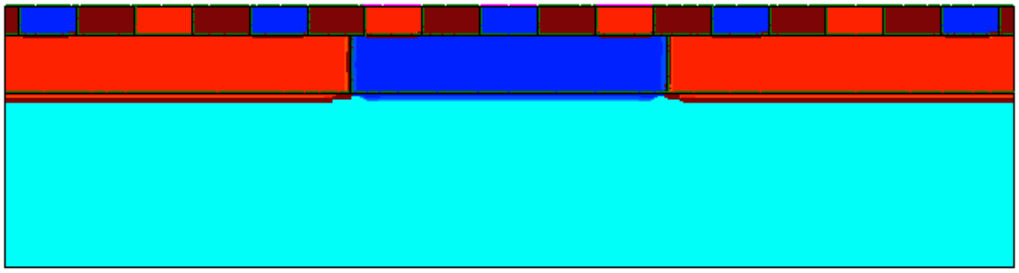


Figure 5-3 Cross section of designed Cell-by-Cell SCR from TCAD

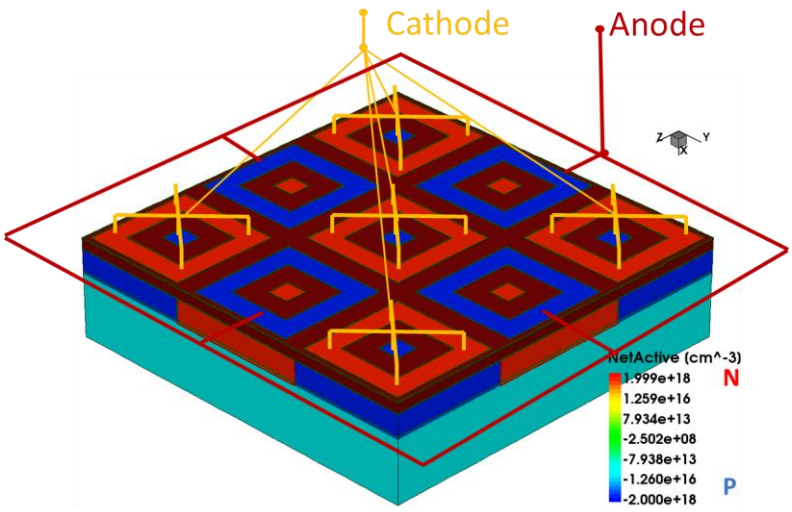


Figure 5-4 3D view of designed Cell-by-Cell SCR structure

5.1.2. TLP measurement results

In this work, a set of new cell-by-cell SCR ESD structures and its conventional counterpart, i.e., parallel multi-finger SCR ESD structures, were designed for a comparison study. The cell-by-cell SCR ESD structure is a 3X3 cell array. These SRC ESD structures were fabricated in a foundry 28nm CMOS technology. Transient transmission line pulse (TLP) measurement was conducted for HBM ESD evaluation. The TLP (Barth Model 4002) pulse width and rise time were set to 100ns and 5ns, respectively.

For both SCR structures, the length between N+ and P+ (LSTI1) is 1μm, and the N+ and P+ doping region length (LN+/P+) is 1μm. The STI between N+ doping area and P-type body pick-up (STI2) is the same as the distance between P+ doping area and N-body pick-up, which is designed to be LSTI2=1μm. The body pick-up is a rectangular with a length of L_{BP}=1μm (Fig. 2 and Fig. 3). The cell dimension is therefore 5μm × 5μm. As illustrated in Figure 5-4, the total ESD conduction width of the 3X3 cell array is sum of twelve conducting sides, i.e., W_{eff} = 60μm. The reference multi-finger SCR ESD structure is designed to have 2 fingers. Its dimension is the same as 3×3 cell

array SCR. Each finger is 15μm long, hence, the multi-finger SCR ESD reference has a total ESD conduction width of W_{total} = 30μm. The total layout area for the cell-by-cell SCR ESD array is 279.9μm^2 and that for the multi-finger SCR ESD structure is 195.4μm^2. By normalizing failure current to the layout area, Sudoku-SCR features about 1.5 times higher area efficiency (I_{t2}/Area) when comparing with multi-finger SCR, while keeps similar ESD current handling ability (I_{t2}/Width).

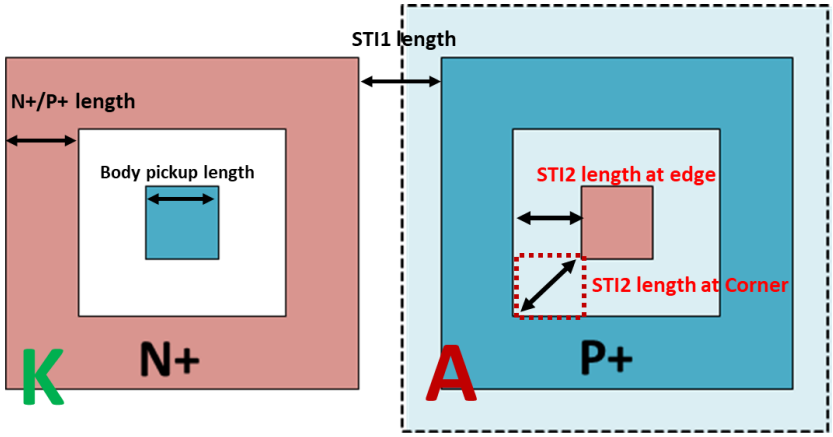


Figure 5-5 Detailed view of A-cell and K-cell. STI is isolation.

Figure 5-6 gives sample measured I-V curves by TLP testing for both SCR ESD structures, showing good snapback ESD discharging behavior for both. The key ESD specs measured are summarized in Table I. No meaningful change was observed for ESD triggering voltage (V_{t1}) and holding voltage (V_h) for the SCR ESD cell array and multi-finger SCR ESD structures. However, the ESD discharging resistance (R_{ON}) for the cell-by-cell SCR is obviously lower than that for the multi-finger SCR. The measured ESD thermal failure current for the SCR ESD cell array, I_{t2}~1.02A, is substantially higher than that for the multi-finger SCR ESD structure of I_{t2}~0.53A, which is attributed to both larger W_{eff} and improved ESD discharging uniformity. The normalized I_{t2}/width values are similar for both ESD structures as per the design, however, the overall ESD discharging

capability, i.e., I_{t2}/area of the cell-by-cell SCR ESD structure (3.64) is significantly higher than that for the multi-finger SCR ESD device (2.7). This clearly shows that the new cell-by-cell SCR ESD structure is more area efficient and much more ESD robust, validated the new layout design concept.

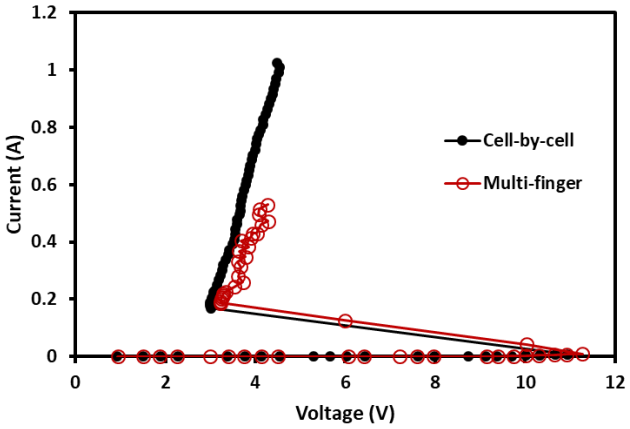


Figure 5-6 Measured ESD discharging I-V curves for the SCR ESD cell array and multi-finger SCR ESD structures by TLP.

SCR Structures	V_{t1} (V)	V_h (V)	I_{t2} (A)	Width (μm)	Layout Area		Normalized It2/Width (mA/ μm)	Normalized It2/Area (mA/μm²)
					Dimension (μm×μm)	Area (μm²)		
Sudoku-SCR	11.3	3.2	1.02	60	16.73*16.73	279.9	17	**3.64**
Multi-finger SCR	10.9	3.0	0.53	30	12.83*15.23	195.4	18	**2.7**

Table 5-1 Summary for the measured ESD critical parameters for the SCR ESD cell array and multi-finger SCR ESD structures by TLP measuring

5.1.3. Scalability and layout perspective

- STI dimension change splits

The improvement on area efficiency of Cell-by-Cell layout is also verified with different layout parameters and in different process technology. Cell-by-Cell SCR is also designed on 22nm SOI process. Comparison splits are also designed. Conventional single directional SCR is design with same dimension as Cell-by-Cell SCR. A split with STI1 length change is also designed and

measured to verify the improvement is constant under different dimension. Considering the conduction depth and layout restrictions. These SCR structures are designed on “hybrid” layers in FDSOI process, which means buried oxide is removed under these device. Therefore, the Cell-by-Cell structure is the same as shown in Figure 5-4 and Figure 5-5 in previous section. TLP measurement was conducted and the result is shown in Figure 5-7 and Figure 5-8. The area consumed by Cell-by-Cell SCR (STI1=1um) is 17um×17um with an effective width of 60um, while the area consumed by conventional SCR is 60um×6.5um with total width of 60um. Therefore, by normalizing It2 to area. The Cell-by-Cell SCR in 22nm FDSOI also shows much higher area efficiency (almost 2 times).

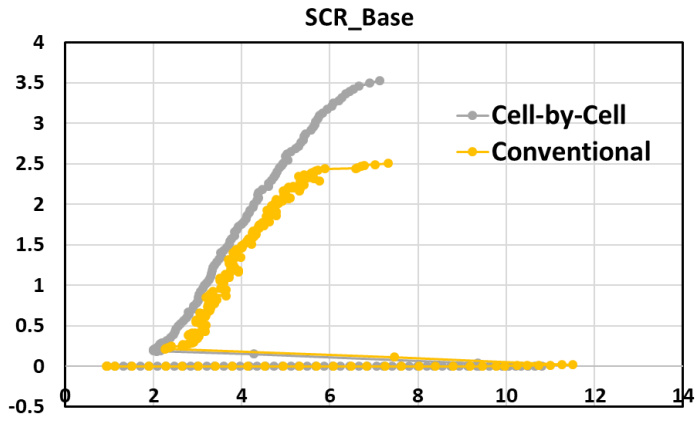


Figure 5-7 Measurement result of Cell-by-Cell and Conventional SCR on 22nm FDSOI

For the SCRs with STI1 length decreased to 0.5um, the base length of the two parasitic bipolar transistors are decreased. As a consequence, the turn on resistance is lower. On the other hand, the area efficiency of Cell-by-Cell SCR is also much higher than conventional SCR. The area of Cell-by-Cell SCR is 16um×16um, which is 1.45 times smaller than conventional SCR. However, when comparing the It2, Cell-by-Cell SCR can handle 1.4 times higher ESD current. Therefore, the area

efficiency is almost twice higher than conventional SCR, which confirms with previous design on 28nm.

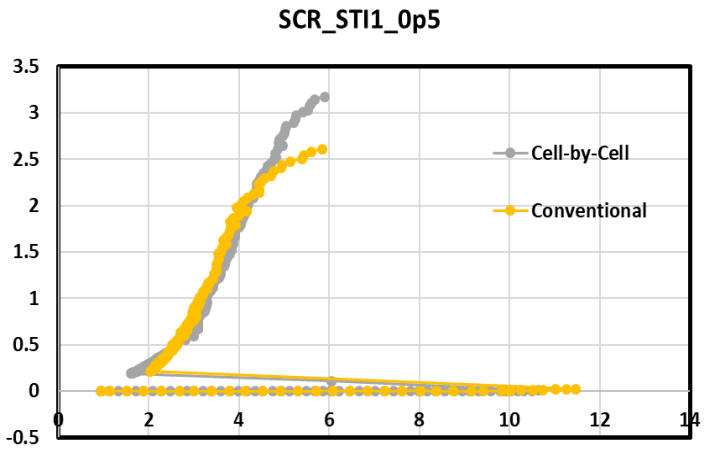


Figure 5-8 Measurement result of Cell-by-Cell and Conventional SCR with 0.5um STI1 length

- Scalability

SCR ESD structure is known for its ESD discharging robustness. We report an improved cell-by-cell cross-boundary SCR ESD array structure to enhance area efficiency and ESD discharging uniformity. The new 3×3 SCR ESD array structure, fabricated in a foundry 28nm CMOS, shows much higher area efficiency over conventional multi-finger SCR ESD structures, i.e., an improvement in I_{t2}/area of about 35%. The cell-by-cell SCR ESD structure is scalable and the area efficiency can be further improved for a larger array layout. One problem for large array Cell-by-Cell SCR design is the metal connection. Since for the design discussed before, metal routes around the Cell-by-Cell structure to connect all the cathodes and anodes. When the array grows larger, i.e. 4×4 array, this layout will not be applicable. To improve the scalability, Figure 5-9 shows a proposed layout, where 45 degree metal bus is used to pick up ESD current. In this layout, the metal-metal overlap area is much smaller, which can also reduce ESD device parasitic capacitance

contributed by metal connection. The only disadvantage is that 45 degree metal bus may not be available in advanced node like FinFET technique.

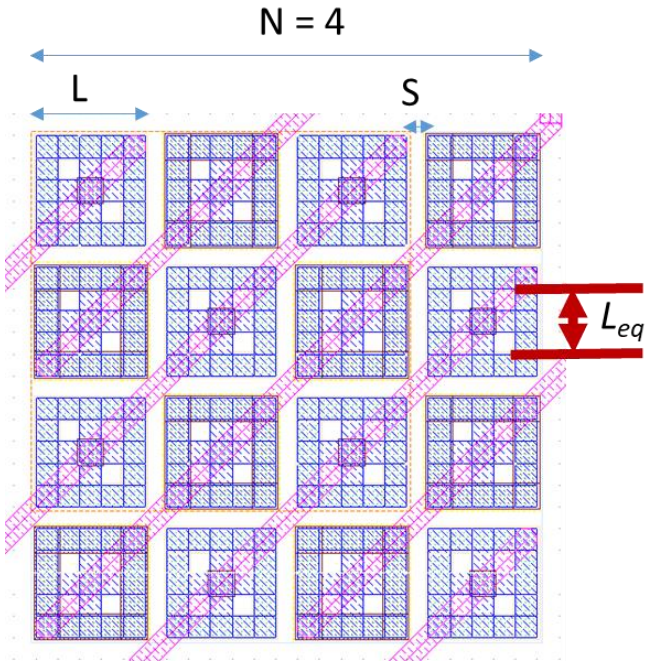


Figure 5-9 Layout for 4×4 Cell-by-Cell SCR array

5.1.4. Theoretical analysis of cell-by-cell SCR

For the designed cell-by-cell SCR, the sides of SCR cells on the edge and corner are not fully used. Therefore, the directly calculation underestimates the real potential of the cell-by-cell topology. To theoretical analyze the area efficiency, we can expended Cell-by-Cell SCR array to make the portion of edge and corner sides lower. The length of the side of each cell is L and the space between cells is S. We assume the effective width of each edge in the cell is L_{eq}. The cells number of each lateral is N. Then the total equivalent width of the cell-by-cell structure can be expressed as Equation 4-1. We assume that in the cell-by-cell SCR, current handling ability for every equivalent conducting width is the same as I_0. Then the ESD current handling ability of the cell-by-cell structure will be calculated as in Equation 4-2. Therefore, the area efficiency can be

expressed as shown in Equation 4-3. When the number of repetition number (*N*) increase to infinity, the limit of area efficiency can be represented as Equation 4-4. Therefore, from the measurement result ($I_{t2(N=3)}$) of the designed cell-by-cell SCR (*N=3*), We can calculate the theoretical area efficiency when the cell array expends to infinity repetition. Although expanding array size can bring us higher area efficiency, the ESD handling ability maybe over-designed due to too large area. Thus, to trade off area efficiency and occupied area, the area efficiency and array size relationship is plotted. Figure 5-10 shows as the array get bigger, the overall area efficiency rises while the rising rate decreases (Figure 5-11). When N is higher than 10, the area efficiency almost reaches upper limit.

$$Equivalent\ width(W_{eq}) = \frac{(4\times L_{eq}\times N^2 - 4\times L_{eq}\times N)}{2} = 2N(N-1)L_{eq} \quad 4\text{-}1$$

$$I_{t2} = W_{eq} \times I_0 \quad 4\text{-}2$$

Where I_0 is the normalized I_{t2}*/width.*

$$Area\ efficiency = \frac{2N(N-1)L_{eq}}{(NL+NS-S)^2} I_0 \quad 4\text{-}3$$

$$Area\ efficiency = \frac{2L_{eq}}{(L+S)^2} I_0 = \frac{2L_{eq}}{(L+S)^2} \times \frac{I_{t2}}{2N(N-1)L_{eq}} = \frac{I_{t2(N)}}{N(N-1)(L+S)^2} \quad 4\text{-}4$$

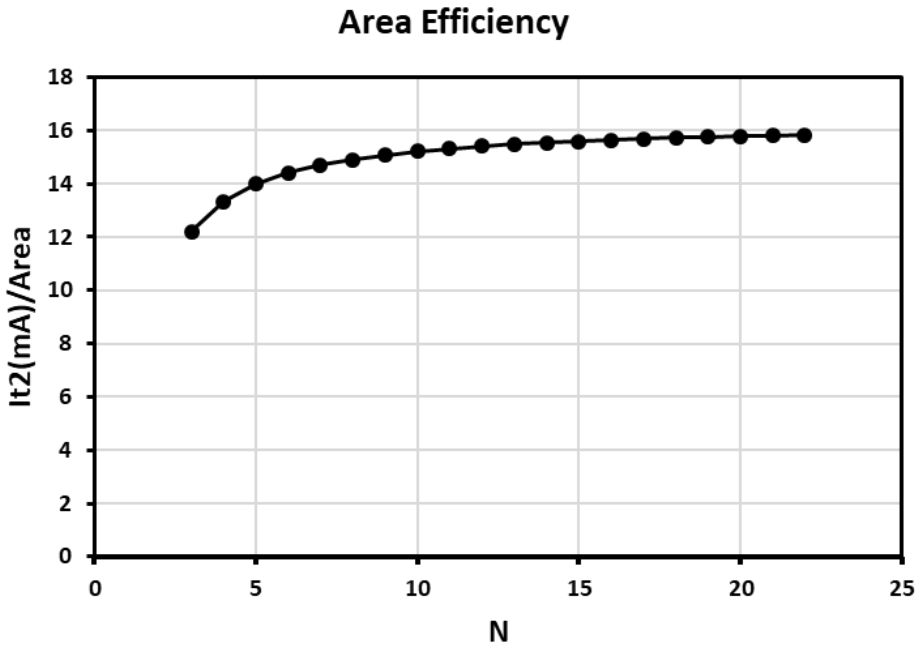


Figure 5-10 Area efficiency relationship to array size

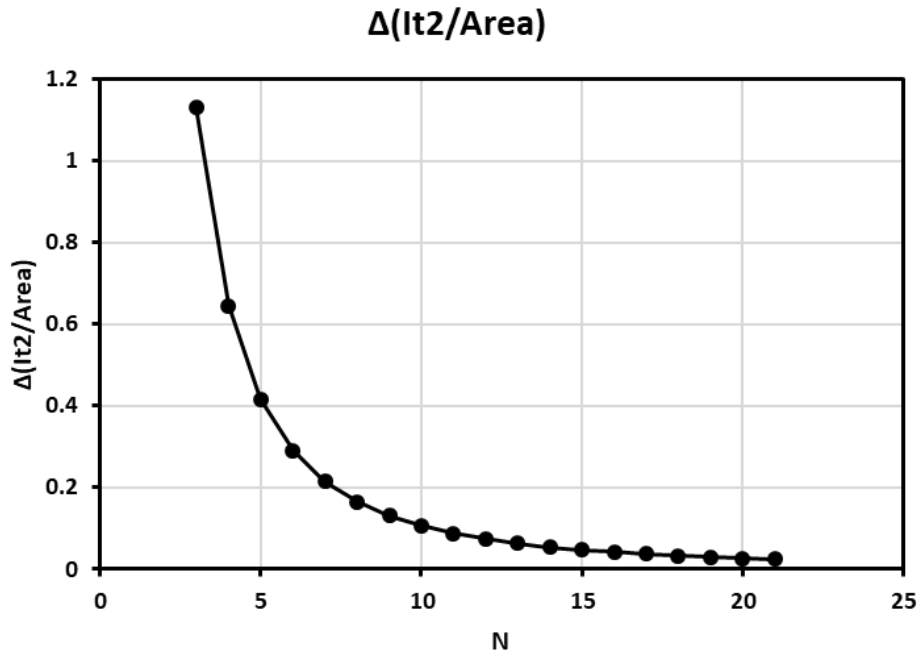


Figure 5-11 Increasing rate related to array size

5.2. Cell-by-Cell DTSCR structure

SCR usually features high triggering voltage, which limits its application on low power circuits. Nowadays, to reduce power consumption, the supply voltage can be as low as 1.2V. Therefore, to make use of SCR's high area efficiency and robust features, lowering SCR triggering voltage is a need. There are several ways to lower the voltage. Among them, diode-triggered SCR (DTSCR) is most widely used for its simple structure. Figure 5-12 shows a schematic of DTSCR. A diode string is connected to G2 of SCR structure. When voltage at node A is high enough to turn on the diode chain formed by intrinsic diode inside SCR and the external diode string, "seed" current will flow through the base of PNP transistor and contributes to triggering the SCR core structure.

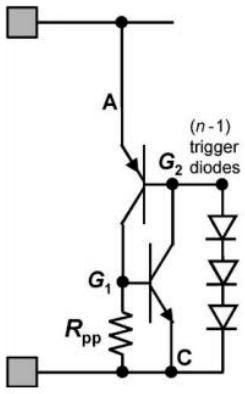


Figure 5-12 Schematic of DTSCR structure.

Following the concept of Cell-by-Cell SCR structure, Cell-by-Cell DTSCR (CCDTSCR) structure is developed. Figure 5-13 shows the proposed structure of CCDTSCR. The core SCR structure is similar to the Cell-by-Cell SCR except that the body pickup (G2) is designed with larger area. The reason is that before SCR core structure is triggered on, almost all ESD current flows through the intrinsic diode to G2 then flow into external diode string. Considering device robustness, G2 pickup area is designed with larger area. Diode is placed to surround the core SCR structure.

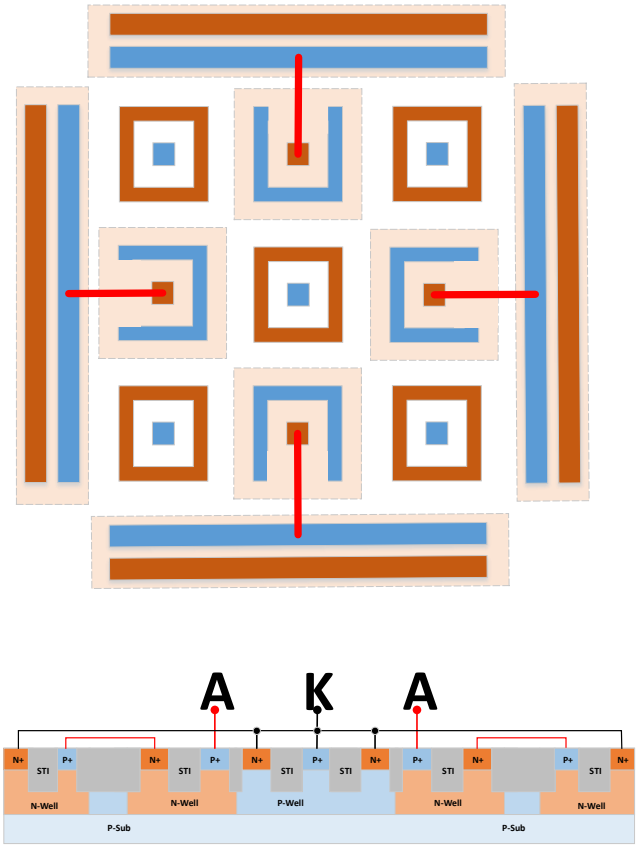


Figure 5-13 Structure of Cell-by-Cell DTSCR

Figure 5-14 shows the measurement result of proposed Cell-by-Cell DTSCR and conventional DTSCR with same width and dimension. The designed Cell-by-Cell shows lower current handling ability and higher turn on resistance, which draws back the layout area it saves. The reason is assumed to be the limited G2 connection area.

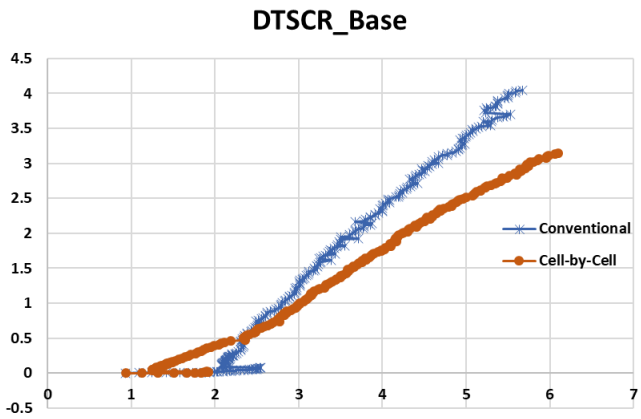


Figure 5-14 Measured TLP I-V curve of Cell-by-Cell and conventional DTSCR

5.3. Temperature awareness in DTSCR structure design

As technology shrinks to nanometer node, the two existing challenges, Electrostatic discharge (ESD) and shifting of operating temperature, hinder us from achieving high performance reliable IC, which is the never-ending goal that IC designers pursuing. To produce endurable IC for tremendous applications corresponding to great temperature variability, operating temperature range and testing method have been standardized [32]. In the meanwhile, EDA tools are developed to conduct simulations that sweep across the operating temperature to ensure IC functionality. However, due to the complex electro-thermal-process-device-circuit-layout, ESD behavior is very hard to predict, especially include operating temperature into consideration [38]. Massive research efforts have been made to develop ESD modeling techniques, which, however, are either developed for fast chip-level ESD protection circuit [39][40][41], or require process technology information. Therefore, ESD protection design stays dominated by trial-and-error approach. Under this situation, it becomes very important to evaluate the influence of temperature on ESD device performance.

Lin et al. [42][43] discussed the temperature-dependence I-V characteristics of some SCR based ESD protection circuit. Liang et al [44] introduced the characteristics of ESD protection devices operating under high temperature. In this paper, the temperature-dependence characteristics

of various ESD protection devices is presented, including diode, Grounded-gate MOS (GGMOS), SCR and DTSCR. Within which, DTSCR shows high sensitivity to operating temperature. TCAD simulation is also used to illustrate the underlying physical process.

5.3.1. Experimental Result and device physics

The ESD structures in this work is designed and fabricated in a 28nm CMOS. These structures are characterized under TLP with temperature ranging from -40 ºC to 110 ºC. TLP pulse is configured with 100ns pulse duration and 10ns pulse rise time.

- Stand-alone Diode and SCR

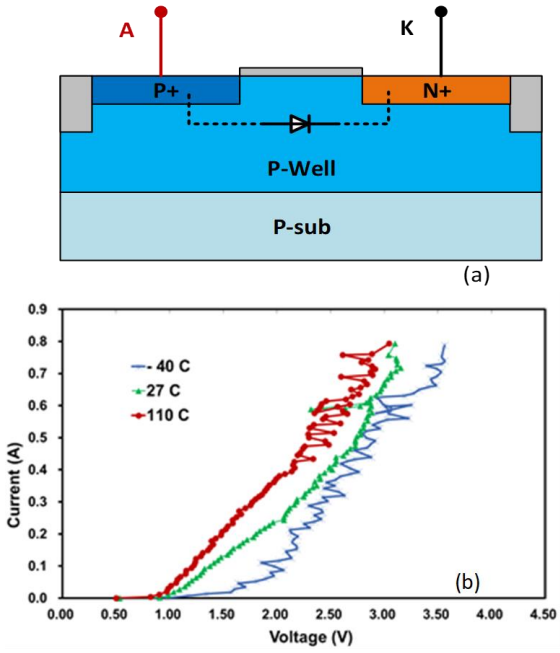


Figure 5-15 (a) Cross-section of Gated-diode (b) TLP measurement result of Gated-diode under different temperature. (Width = 30um)

Figure 5-15(a) shows the cross-section of designed Gated-diode, where gate is put between P+ and N+ doping area instead of STI to form a low resistance conducting path. With temperature increase from -40 ºC to 110 ºC, it's clear that turn-on voltage decrease as temperature increase,

while current flow through diode under the same voltage increase noticeably (Figure 5-15(b)). According to theory, ideal diode current is given by:

$$I = I_s e^{((\frac{V}{n \times V_t} - 1))} \qquad 4\text{-}2$$

Where, $V_T = \frac{KT}{q}$

As temperature increase VT increase, which decrease the exponential item. However, reverse saturation current (IS) increase quicker as the temperature increase. Thus, in total, the current increase with temperature increase. The TLP measurement result shows I-V characteristics under ESD surging matches theoretical prediction.

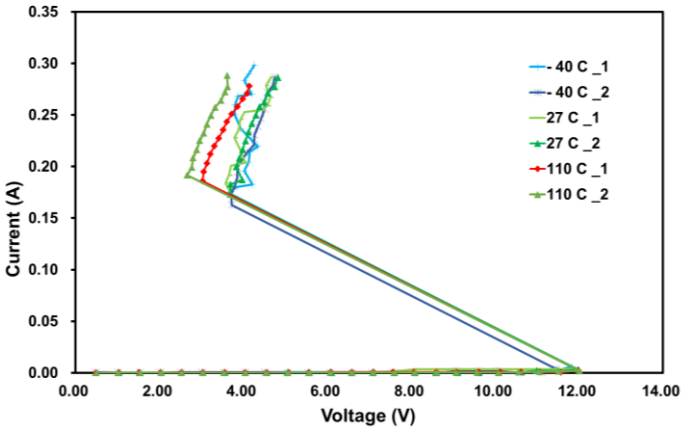


Figure 5-16 (a) Cross-section of designed SCR structure; (b) TLP measurement result of SCR under different temperature. (Width = 30um)

Silicon-Controlled Rectifier (SCR), featuring high current handling ability, area efficiency and high robustness, has been widely used as an electrostatic discharge (ESD) protection device. Figure 5-16(a) shows the cross-section of designed Silicon-Controlled-Rectifier (SCR). In this structure, the core P+/N-well/P-well/N+ structure forms two parasitic bipolar transistors (Q1 and Q2), and parasitic substance resistors (Rsub1 and Rsub2) lies on the path between body pickup and N/P-well.

The trigger of the SCR structure start with the p-well/n-well avalanche breakdown, the avalanche current accumulates voltage across the parasitic substance resistance, which turns on the parasitic BJTs. Thus, SCR goes to snapback region. The ESD critical parameters didn't change much along with temperature increasing. As temperature increase from -40 ºC to 110 ºC, the trigger voltage stays around 12V, while the holding voltage decrease with increasing temperature (Fig. 2(b)).

- DTSCR Structure and Performance

As supply voltage decreasing with technology node shrinking, the high trigger voltage of SCR cannot meet the design window of normal low voltage applications. Therefore, diode-triggered SCR (DTSCR) was invented to lower the trigger voltage by introducing a set of diode into SCR structure as shown in Figure 5-17(a). Figure 5-17(b) shows the equivalent circuit of a DTSCR structure. The added diode combined with the intrinsically embedded diode forms a forward current conducting path. Part of the current flows into the base of Q1 and helps triggering the core SCR structure.

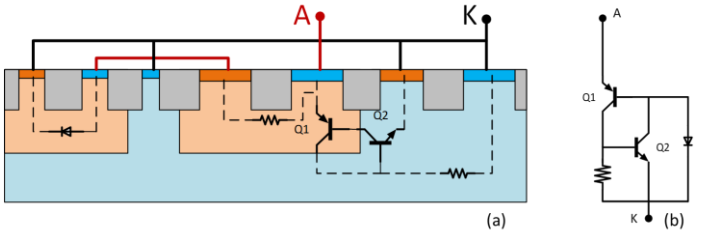


Figure 5-17 (a) Cross-section of designed DTSCR; (b) equivalent circuit of DTSCR structure

Figure 5-18 depicts the I-V characteristics tested under different temperature. It's worth notice that the trigger voltage shifted in a very large scale. Under -40 ºC, trigger voltage Vt1=8.64V, which is almost two times the trigger voltage under 110 ºC. And comparing with 2-diode-trigger DTSCR, the trigger voltage Vt1 are almost the same. The holding point also shows clearly temperature

dependence. Under -40 °C, the holding voltage (V_h) is 3.37V, holding current (I_h) is 0.2A. As temperature rise to room temperature (27 °C), the holding point shifts with holding voltage decreases to 3.16V, holding current decrease to 0.16A. The I-V characteristics under higher temperature confirms this trend, which features a holding voltage equals to 2.59V and holding current of 0.12A. These results depicts a clear trend that as temperature increase, V_{t1}, V_h, I_h decrease.

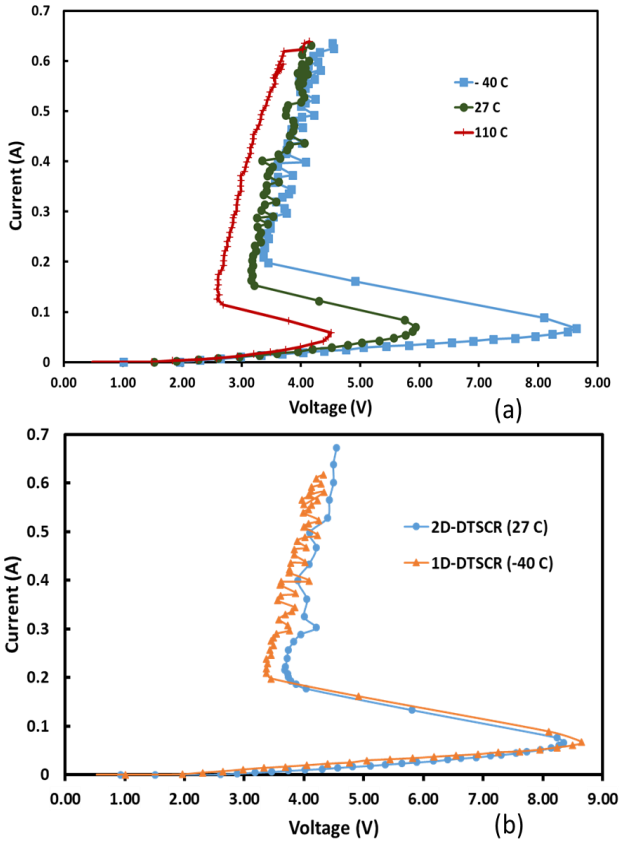


Figure 5-18 (a) TLP measurement result of 1-diode DTSCR under different temperature; (b) TLP measurement result of 1-diode DTSCR and 2-diodes DTSCR

The notable sensitivity of DTSCR to temperature can be a big harassment to ESD protection if it's not carefully considered in design and testing. Fig. 4(b) shows a comparison between I-V curves of 1-diode DTSCR under -40 °C and a 2-diodes DTSCR under 27 °C. It is remarkable that the two DTSCR with different number of triggering diode performs similar ESD critical parameter

under two different temperature. Therefore, the influence of temperature variation is as significant as changing ESD protection devices.

- ESD failure cases

In this section, we will talk about the ESD failure cases caused by the temperature awareness of DTSCR. Figure 5-19 shows a full ESD protected input buffer, where double diode structure provides protection from Input pad to V_{DD} pad and from VSS pad to Input pad. Here, M1 and M2 forms an inverter. The breakdown voltage of M1 and M2 are BV_{DS}~7V and BV_{GS}~7V. The normal operation supply voltage is 5V. The DTSCR is used to provide dual direction protection to V_{DD} and VSS. Considering the ESD design window, the 1-diode DTSCR with triggering voltage Vt1 = 6V under room temperature can be used. Therefore, this ESD protection network provides an ESD discharge path between every two pads. However, this design is very risky that under huge temperature variation. For example, for the automotive chips nearby the engine, its operating temperature often rises to higher than 100 ^{o}C. As a temperature sensitive ESD device, the 1-diode DTSCR ESD performance shifts with temperature. According to Figure.4, when temperature increases to 110 ^{o}C, the triggering voltage rises to Vt1 = 8.6V, which exceeds the break down voltage of gate oxide. In this case, when an ESD strikes V_{DD} pad and input pad, the gate oxide of transistor M1 will breakdown before DTSCR triggering on, which causes circuit ESD failure.

This ESD protection circuit is also risky under very low temperature. For example, for the sensor circuit used in airplane whose operating temperature often drops below zero. When the temperature drops to -40 ^{o}C, what will happen is that the triggering voltage drops to 4.4V according to measurement result shown in Figure.4. As mentioned before, under normal operation, the supply voltage is 5V. Therefore, the 1-diode DTSCR structure turns on and start to discharge, which will cause a huge leakage from power supply. What's more, if the leakage exceeds the current loading

ability of power supply, the supply voltage will be drag below 5V. As a consequence, the circuit may not be able to work normally.

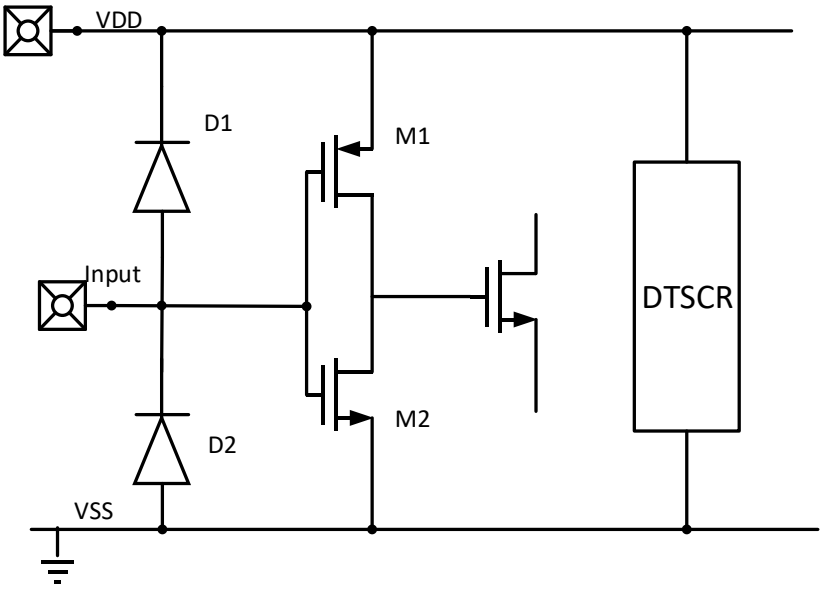


Figure 5-19 Schematic of a full protected input buffer with DTSCR serves as power clamp

5.3.2. TCAD simulation on DTSCR structure

TCAD simulation reveals the underlying physics process of this DTSCR-temperature phenomena. The structure used in TCAD simulation has the same dimension as fabricated DTSCR devices. Figure 5-20 shows the built structure corresponding to the designed DTSCR structure (Figure 5-17(a)), where the left part is the triggering diode and right part is the core SCR structure.

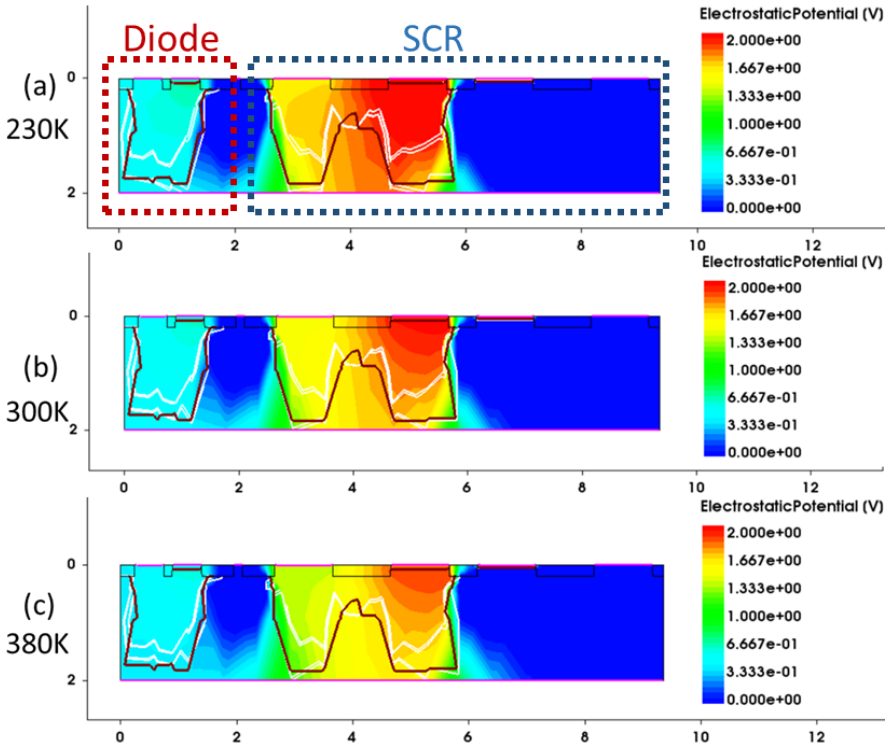


Figure 5-20 Electrostatic potential distribution on DTSCR at 0.4ns under different temperature: (a) 230K; (b) 300K; (c) 380K.

Figure 5-20 depicts the simulated electrostatic potential distribution on DTSCR under different temperature at 0.4ns, when the DTSCR structure is not yet turned on. The simulation confirms TLP testing result where under lower temperature, the voltage is accumulated higher (refer to the red area). Fig. 6 shows Current density distribution on DTSCR under different temperature also at 0.4ns. As temperature rise, the current flows more into core SCR structure, which contributes to turning on SCR. As a consequence, the DTSCR structure triggers with lower voltage under higher temperature. (Boxed area)

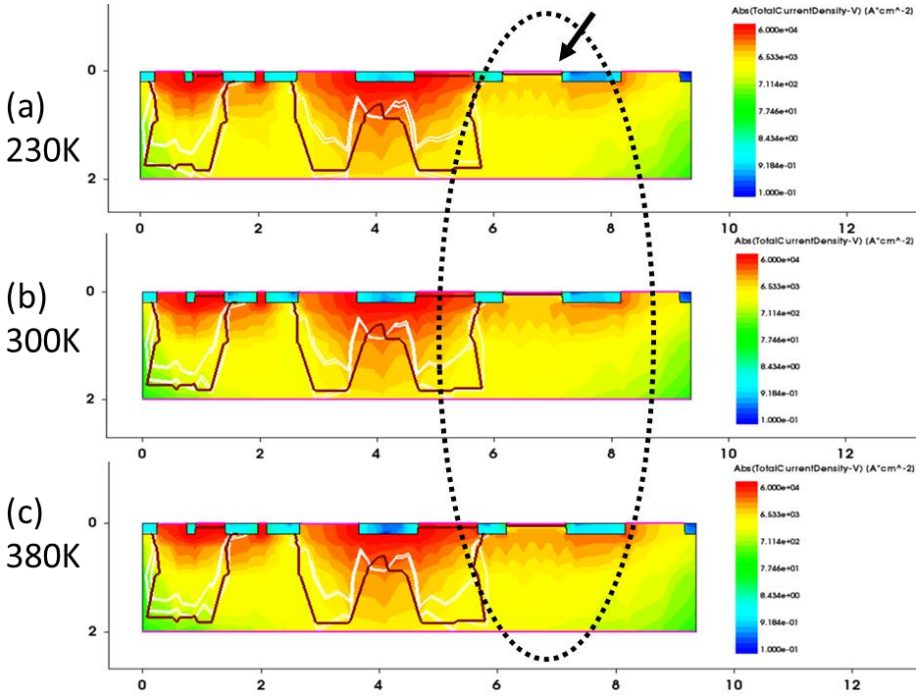


Figure 5-21 Current density distribution on DTSCR at 0.4ns under different temperature: (a) 230K; (b) 300K; (c) 380K

Figure 5-21 shows three different states of DTSCR at 4ns under HBM surge. In Figure 5-21(a), most current flow through triggering diode. DTSCR is not triggered yet. While under room temperature, the current distributes half and half between triggering diode and core SCR structure. DTSCR is in the process of triggering. (Figure 5-21 (b)). Figure 5-21(c) depicts a fully triggered DTSCR structure, where core SCR becomes the main discharging path. The simulation shows that under higher temperature, triggering diode is easier to conduct current with lower voltage across anode and cathode of DTSCR, which results in lower triggering voltage.

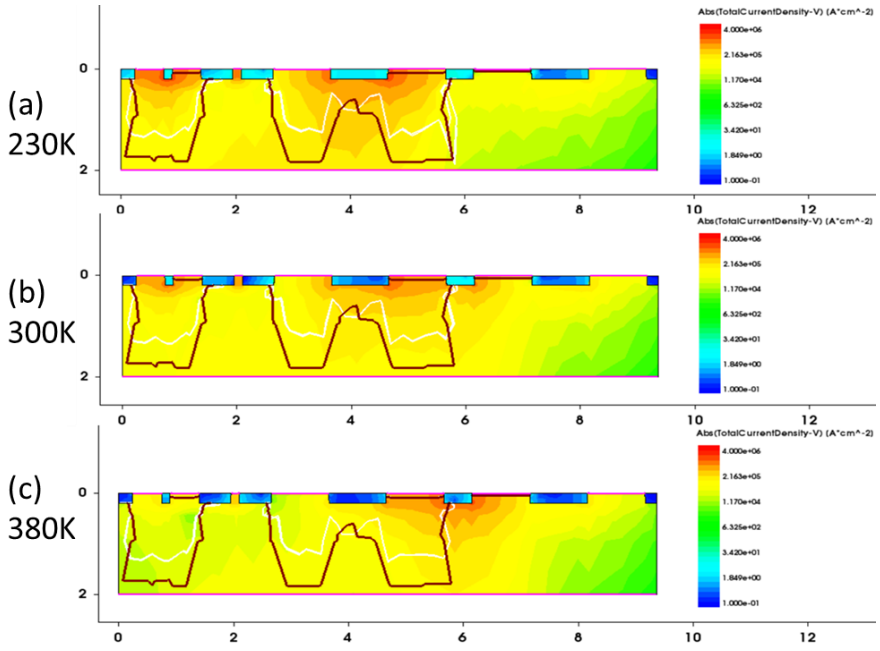


Figure 5-22 Current density distribution on DTSCR at 4ns under different temperature: (a) 230K; (b) 300K; (c) 380K

In this section we investigated the ESD performance of DTSCR under various temperature. The testing and simulation result reveals that DTSCR features high temperature sensitivity. Huge shift of triggering voltage V_{t1} and holding voltage V_h can cause disaster to ESD protection. Thus, influence of temperature on DTSCR's ESD performance must be carefully considered in ESD circuit design and verification process.

Chapter 6. FinFET ESD design with 3D TCAD

In 1965, Gordon Moore sketched out his prediction of the pace of silicon technology that "the number of transistors on integrated circuits doubles every two years". In the past 30 years, the physical dimension of transistors scaling down of 10^3 times, and the transistor on a wafer increased 10^6 times, which is realized by thinning gate dielectrics, forming shallower extensions, increasing channel doping, and lowering power supply voltages. However, many of these key scaling methods are reaching fundamental limitations. In CMOS technology, channel area underneath the gate is too deep and too much of the channel is too far away from the gate to be well-controlled. The consequences are higher leakage power and threshold voltage variance, which results in power consumption and huge design mismatch correspondingly. These limitations of CMOS technology caused more severe problem under the current trend of increasing computing power and adding of functionality in mobile devices, which obviously increased the minimum power budget required for system operation. Green computing and ultra-low power (ULP) operation bring the need for higher energy efficiency, increased versatility and better computing power adaptability. The major energy savings are located at low power supply voltages (i.e. near sub-threshold operation) where process, voltage, and temperature (PVT) variations have the most adverse effects and where computing power is drastically reduced. This operation region brings more and more design challenges; process sensitivity to PVT variations increasing as power supply voltage is going down, static multi-V_t implementation depending on the predicted activity ratio of the circuit.

To meet the requirement of lower power consumption and better PVT variation control, the key point is to make the channel thinner so that it is well controlled by the gate. Two alternative technology have been invented: FDSOI (Fully-Depleted Silicon-On-Insulator) and FinFET was introduced on 28nm and 22nm node respectively (Figure 6-1). These thin channel technologies offer scaling and power saving advantages over conventional devices.

6.1. FinFET Technology

Different from planar CMOS process, FinFET Fin Field-effect transistor is a 3D structure. Figure 6-2 shows a cross section of FinFET structure, the gate wraps around the fin shaped silicon channel to achieve better control of the channel. Thus, achieve lower turn-off leakage current and lower threshold voltage. The 3D structure also benefits for the higher transistor density. Due to the significantly faster switching times and higher current density than the mainstream CMOS technology, FinFET can provide higher performance in digital processing. Consequently, FinFET is widely used in mainstream applications, including servers, networking, graphics and high-end mobile baseband. i.e. Qualcomm snapdragon series. The 3D structure increases the difficulty to simulate the already very complex layout-physics-electrical-thermal ESD behavior.

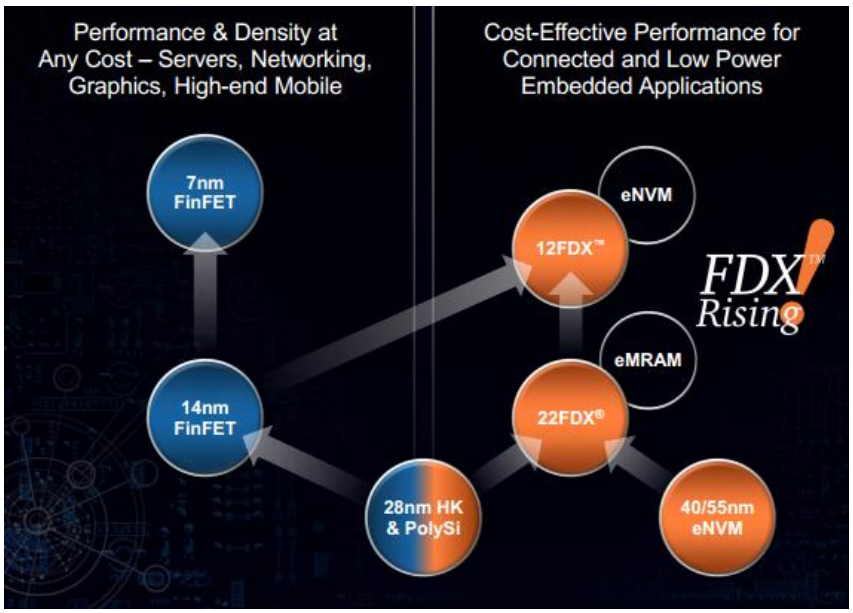


Figure 6-1 CMOS development road map [45]

6.1.1. Comparison with FDSOI technology

Over Bulk CMOS and FinFET technology, FDSOI technology offers several enhancements which may promote it as a good candidate for low to ultra-low power computing: higher energy efficiency, better gate electrostatic control, reduced gate delay and lower process variability.

Major difference from BULK technology is the possibility to control the back-plane potential of both transistor types to modulate the threshold voltage, which improves the opportunity for an advanced dynamic threshold voltage tuning. Moreover, as FDSOI is built on top of BULK CMOS technology, design flow for a node essentially remains the same. However, comparing with FinFET, the gain FDSOI device can provide is lower. Due to the high cut-off frequency, FinFET is dominating high speed circuit market, while FDSOI may more suitable for low power application.

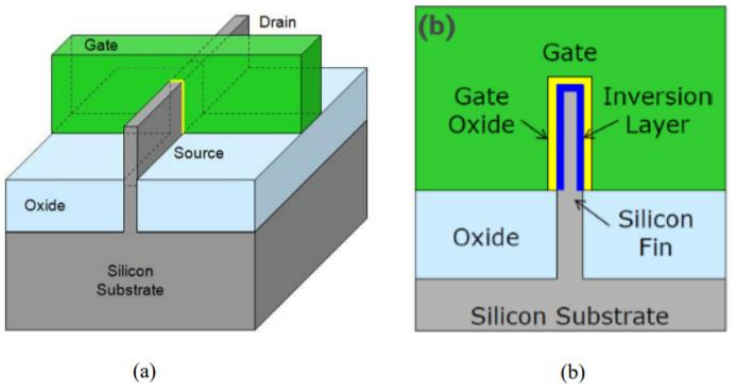


Figure 6-2 (a) 3D FinFET structure; (b) cross-section across the fin

6.2. FinFET ESD design

6.2.1. Systematic ESD protection design method

ESD protection design in FinFET technology is more challenging than planar CMOS technology. The primary reason is that FinFET technology features thinner gate oxide and the source-drain distance is smaller, therefore, IC designed in FinFET technology is more vulnerable

to ESD damage. On the other hand, most of the ESD protection devices are expected to have weaker ESD power handling ability than planar CMOS. If we look into the cross-section of the FinFET devices, FinFET ESD device discharges with smaller cross-section area than CMOS technology. Therefore, ESD discharging current will crowd in fin area and generates hot-spots. To provide effective ESD protection to IC in FinFET technology, systematic ESD characterization using ESD test-chip will be a good solution.

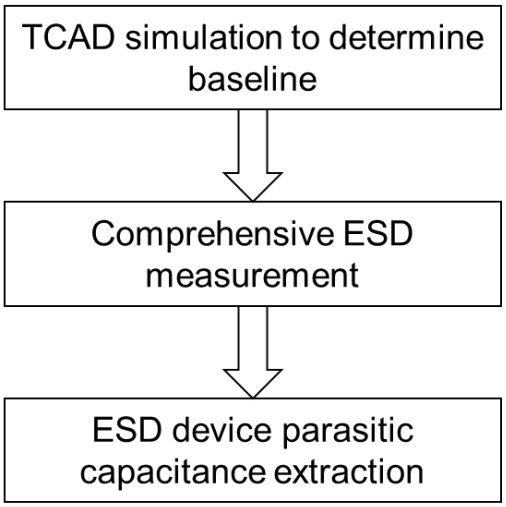


Figure 6-3 ESD test-chip design flow

- Stand-alone ESD device characterization

The ESD testchip is designed in the following process. Firstly, because ESD device features huge difference with planar CMOS technology. Thus, it's not appropriate to take the previous ESD protection device design parameters as a reference. To find the proper value of ESD protection device dimension, TCAD simulation is desired. From TCAD simulation, ESD designer can find out the weak point of designed ESD protection device and find out a reasonable value as a start point. To successfully design the ESD device to meet ESD protection specification and optimize the ESD protection device dimension, comprehensive ESD protection device design and characterization is desired. The detailed solution is that based on the baseline, a set of ESD device

splits is designed. For example, if we design several ESD protection device with different width while keep all other dimension the same. By carefully characterization with TLP or vf-TLP, we can find the correct value to provide a certain ESD protection level without over-design.

- Parasitic capacitance extraction

As discussed before, ESD protection is necessary for all pads. However, the parasitic capacitance of ESD devices can severely degrade circuit performance, especially for high-speed circuit and RF circuit working on high frequency. Moreover, Accurate ESD parasitic parameter extraction is a key to realize full-chip ESD-IC co-design. So, beside the ESD protection ability, parasitic capacitance is also an important feature that has to be carefully measured. However, the test connections will introduce extra capacitance such as the capacitance between metal interconnects (C_{metal}) and capacitance of the probing pad itself (C_{pad}). Thus, these capacitances introduced by test pattern should be calibrate out. To achieve this, de-embedded method is developed, where beside the test-key with ESD device and measurement patterns, another split with only the measurement pattern is also designed as shown in Figure 6-4. Utilizing network analyzer, we can extract the Y parameter for both test pattern A and pattern B. By simple calculation, we can extract out the capacitance of ESD device (C_{esd}).

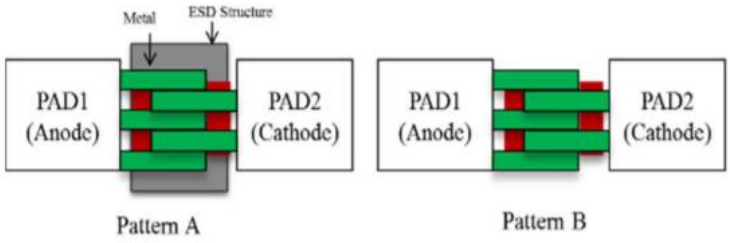


Figure 6-4 De-embedding ESD testing patterns A (full ESD structure) and B (Si structure removed)

6.2.2. ESD protection device layout in FinFET

In FinFET technology, fin is built in one direction, so the layout is directional, which means the horizontal direction is different with vertical direction. Due to the complicated fabrication process, FinFET ESD device layout has more restricted design rules.

First, in FinFET technology, fin pitch and fin width are usually fixed. Therefore, to change the equivalent width, the usual method is to change the fin numbers of the ESD device. One active area (AA) block in FinFET technology usually can contain limited number of fins. Therefore, to increase the fin numbers, rather than directly increase the width of active area, we usually use repeated active area blocks. This limitation of FinFET technology rises difficulty on designing ESD device guard ring (GR), because the guard ring cannot fully surround the ESD device core. Furthermore, the gate length of FinFET device usually can not change continuously when it is shorter than 72nm. Therefore, we may not be able to fine tune the ESD device performance by change the gate length in some cases. Metal width, especially for the connection of source and drain (M0) usually is also fixed. So to prevent the ESD failure on M0 connection, adding several M0 lines is a more common solution rather than conventionally increasing M0 width.

6.3. FinFET ESD protection devices

Due to the 3D feature of FinFET structure. FinFET ESD device has a lot of difference comparing with conventional planar CMOS ESD device. We will talk about these devices one by one.

6.3.1. Gated diode:

Figure 6-5 shows the Gated Diode cross-section (left: N+/PW Gated-diode; right: P+/NW Gated-diode). In Gated diode, a gate is placed between P+ doping area and N+ doping area. A

shorter channel is formed beneath the gate. Compared with STI diode, gated diode usually has lower turn on resistance.

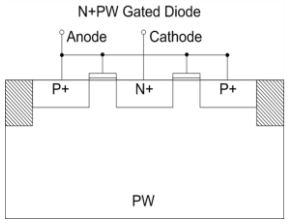


Figure 6-5 Cross-section of planar Gated-diode (N+/PW Gated-diode)

With the same concept, gated diode is widely used in FinFET technology as ESD protection device, due to its low turn-on voltage and low turn-on resistance. In a FinFET Gated diode, the anode is connected to P+ doping area, and cathode connects to N+ area. As in FinFET MOS, the gate wraps around the fin structure, though no control nodes are applied on the gate. The current flowing direction is along the fin direction.

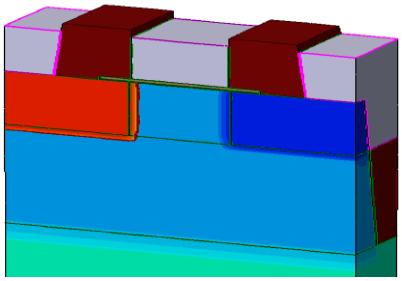


Figure 6-6 Structure of gated diode in FinFET

6.3.2. STI diode

Figure 6-7 shows the STI Diode cross-section (left: N+/PW diode; right: P+/NW diode). Due to the STI between P+ doping area and N+ doping area, the current discharging path is longer, but in the same while, ESD discharging current is less concentrate,. As a consequence, STI diode usually features higher failure current.

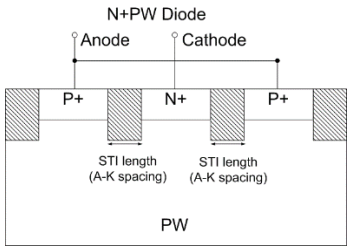


Figure 6-7 planar STI diode x-section (N+/PW diode)

For 3D FinFET STI diode, because fin has a direction. Thus, the STI diode can be sorted to 2 sub-categories: horizontal STI diode and vertical STI diode. For horizontal STI diode, the P+ anode and N+ cathode are placed along the fin direction. Therefore, the current flows along the fin direction. On the other hand, in the vertical STI diode, P+ anode and N+ cathode are placed in perpendicular with fin. As a consequence, the current needs to flow through the bulk area before discharged. Figure 6-8 shows a TCAD built vertical STI diode structure.

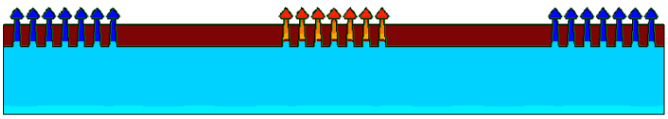


Figure 6-8 Vertical STI diode in FinFET.

6.3.3. Grounded-Gate MOS (GGMOS)

Figure 6-9 shows a planar GGNMOS cross section. In GGNMOS structure, gate is connect to ground to prevent NMOS turn on. The parasitic bipolar transistors (BJT) discharges most ESD current. Due to its snapback feature, it is widely used in high voltage ESD protection, i.e. mixed voltage interface. In advanced technology, low-doping drain (LDD) threats the robustness of GGMOS, as a solution, drain ballast resistance is introduced. A popular way to realize it is to use silicide block technique (DCP) and sometimes decrease doping level in certain area (ESD implant).

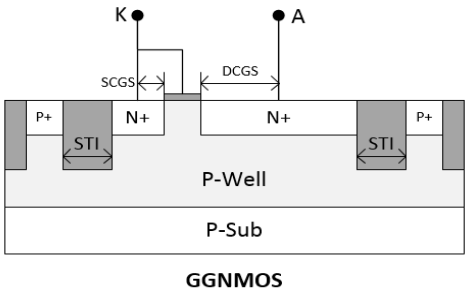


Figure 6-9 Planar GGNMOS cross-section

The 3D structure of the FinFET GGNMOS is shown in Figure 6-10, the structure is almost the same as normal FET, with the drain-gate distance larger and gate node connected to ground outside. The current flows along the fin direction.

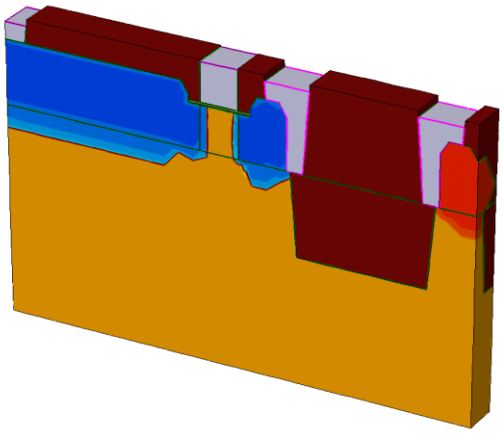


Figure 6-10 3D structure of GGNMOS in FinFET

6.3.4. SCR

In SCR structure, P+ and N+ area forms two parasitic bipolar transistors which latches up with each other. As mentioned before, SCR has capability of handling large ESD current within small area, which makes it a good candidate for high power ESD protection.

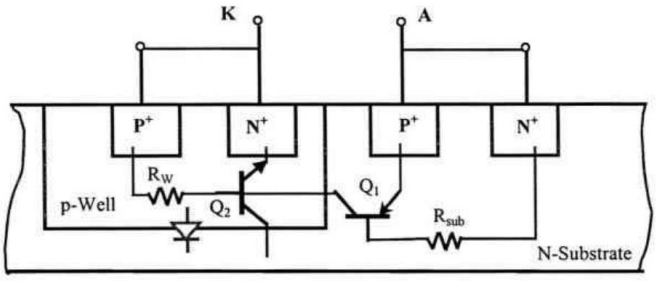


Figure 6-11 Cross-section of planar SCR

Figure 6-12 shows a 3D structure of SCR built in TCAD, one fin is shown. Here P+ and N+ are placed along fin direction. The current flows along fin direction. Due to complicate structure and

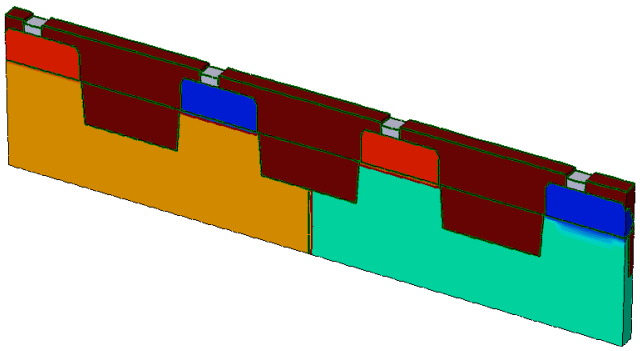


Figure 6-12 3D structure of SCR in FinFET.

6.4. 3D TCAD simulation for FinFET ESD protection devices

Common ESD failures are catastrophic, leading to immediate malfunction of IC chips caused by either thermal breakdown in silicon and/or metal interconnects due to high current transients or dielectric breakdown in gate oxide due to high voltage overstress. Therefore, dedicated on-chip ESD protection circuits are required to protect IC chips against ESD damages. With continuous scaling down in IC technologies, on-chip ESD protection design becomes a major challenge in IC design. Unfortunately, trial-and-error approaches still dominate in current ESD protection design

practices that are extremely time consuming and costly. A rational simulation-based ESD design methodology is, therefore, highly desirable.

Due to the complicated 3D character of FinFET. Conventional 2D simulation cannot offer precise electro-thermal analysis, since none of cross sections can represent the structure of FinFET as in planar CMOS [46]. Figure 6-13 depicts the mixed mode TCAD simulation flow. In Sprocess, FinFET device structure is created and meshed. Then contact is added. In Sdevice, models and ESD stimulus are applied to the built structure. Then electric-thermal simulation is conducted. Svisual and Inspect is used to view the simulation result.

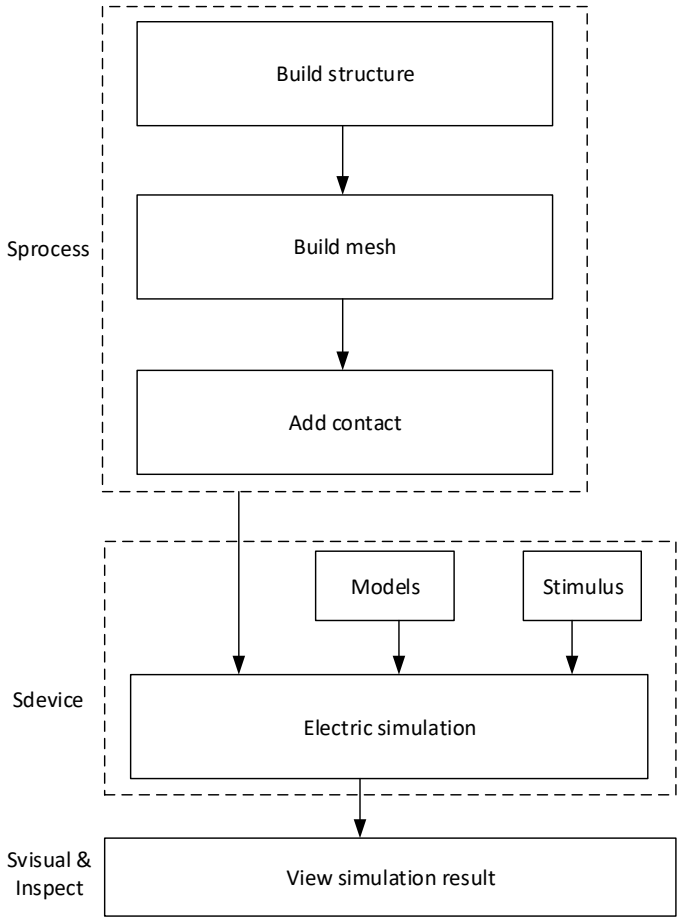


Figure 6-13 Mixed-mode TCAD simulation flow

6.4.1. TCAD process of creating 3D FinFET device

The first step to conduct TCAD simulation is building up device structure. Figure.1 shows the sprocess step in Synopsys TCAD to build up a FinFET structure. The process includes the following steps:

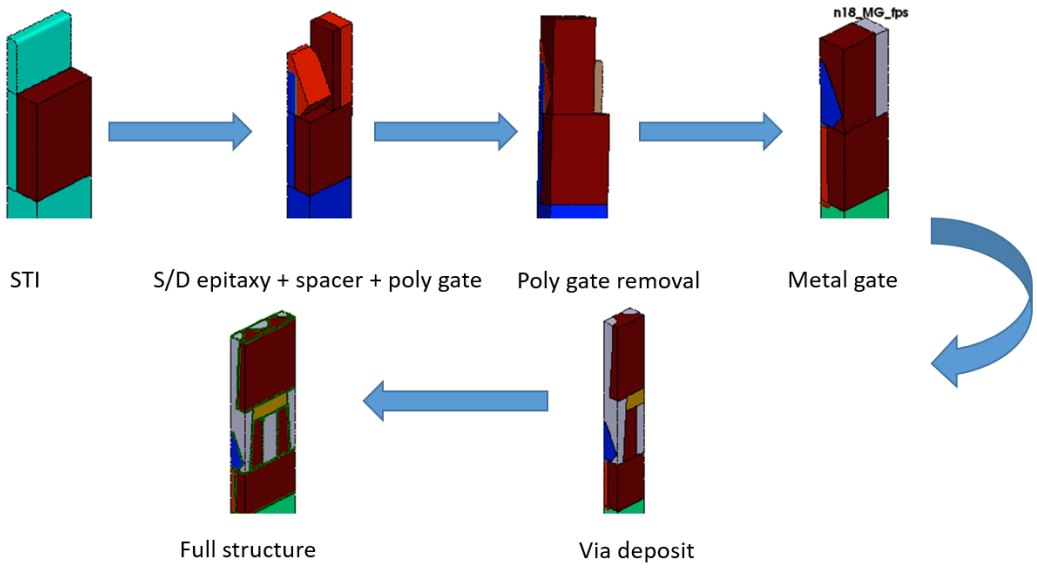


Figure 6-14 TCAD process to build a FinFET

- STI and high-K

Fin is defined in a certain area by code. Then etch is performed to each out the fin shape, which is the core structure of the built FinFET structure. After the fin forms. Oxide is deposited to a height slightly lower than fin height. The STI covered region is the called channel region. High-K material is then deposited to cover the open area around fin, which is part of the process to make the gate structure.

- Poly Gate

In the FinFET process, gate contact is formed later after source-drain structure built up. Therefore, the gate of FinFET is a gate-last process. The poly gate is deposited to hold the place of metal gate and give spacer a surface to grow. After the source and drain formed, the poly gate will be removed.

- Spacer

Spacer is a low-k material. Spacer works as insulator between gate contact and source, as well as between gate and drain. The existence of spacer prevent these three contact from being shorted to each other.

- S/D Epitaxy

The reason why source and drain are epitaxial grown is that the resistance of source/drain to channel needs to be very small to prevent degradation of FinFET performance, i.e. power consumption. In FinFET technique, the fin in source/drain region is cut out in the first step, then, the SiGe/SiC epitaxy is grow for P-type FETs and NFETs accordingly. The process is shown in Figure 6-15.

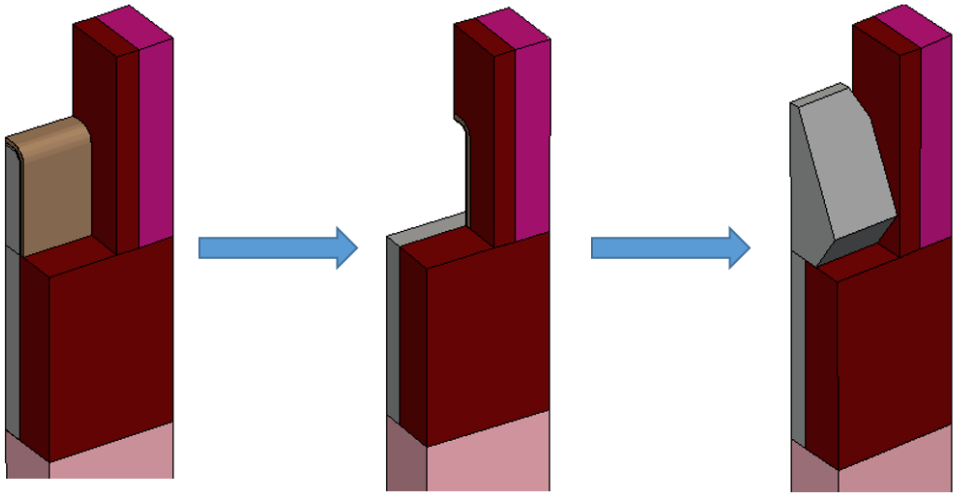


Figure 6-15 Process of Source/Drain epitaxy

- Gated removal and HKMG

The poly gate is then removed by etching. Then metal is deposited to gate region to form the High-K Metal-Gate (HKMG). Till now, the active structure is built up. Then, the connection to back end of line (BEOL) is constructed (Via) by etch and deposit. The final built structure is shown in Figure 6-16.

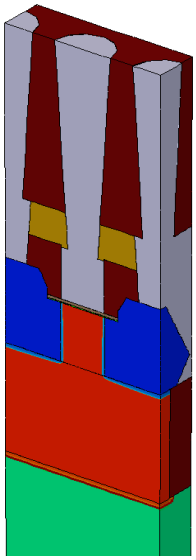


Figure 6-16 Final structure of FinFET built in TCAD

After we build the ESD protection device, to conduct ESD simulation, the device has to be re-meshed to be more suitable for electronic and thermal simulation. Since FinFET technology contains more complicated physics effects, such as quantum effects, therefore the device models are more complicated, which rises the difficulty for simulation convergence. To achieve better convergence under ESD strikes, a mesh strategy is developed for ESD device in FinFET technology as shown in Figure 6-17: first, adaptive mesh is applied to the whole structure. The adaptive mesh determines mesh density according to the doping gradient. Therefore, in area that doping concentration changes flat, the mesh is also looser, which can ensure simulation speed. Secondly, the junction area is specially refined as the doping concentration changes rapidly in this area. Since

some physical equations are doping dependent, the mesh density is desired to be higher for smaller simulation error. Last but not least, the mesh is refined at the silicon and dielectric interface. Although dielectric does not conduct ESD current, refined mesh is needed to reduce the simulation error introduced by thermal conduction and thermal dynamics.

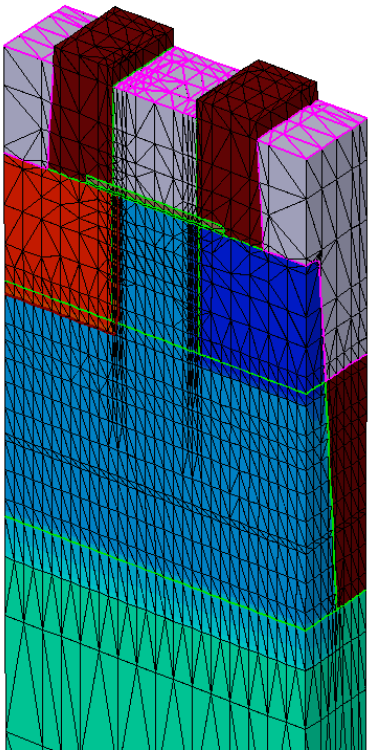


Figure 6-17 Mesh of a TCAD built Gated-diode in FinFET process

6.4.2. ESD simulation setup

The second step of TCAD ESD simulation is using Sdevice to conduct the electric simulation on the built ESD device. Figure shows the simulation flow in Sdevice. First the ESD simulation bench is built, and ESD waveform is applied to the ESD device as excitation. Then the electronic and thermal models are assigned to ESD device to simulate the real world physical process. After assigning models, simulation algorithms are chosen and ESD failure criteria is set. Since for ESD device, thermal failure is most commonly met cases, therefore, lattice temperature reaching silicon

melting temperature is set as stop mark. Lastly, the output is set in Sdevice to choose what to output. Usually, beside the I-V curve, the lattice temperature, current density distribution and doping concertation will be plotted to inspect the hot spot and the current crowding effects.

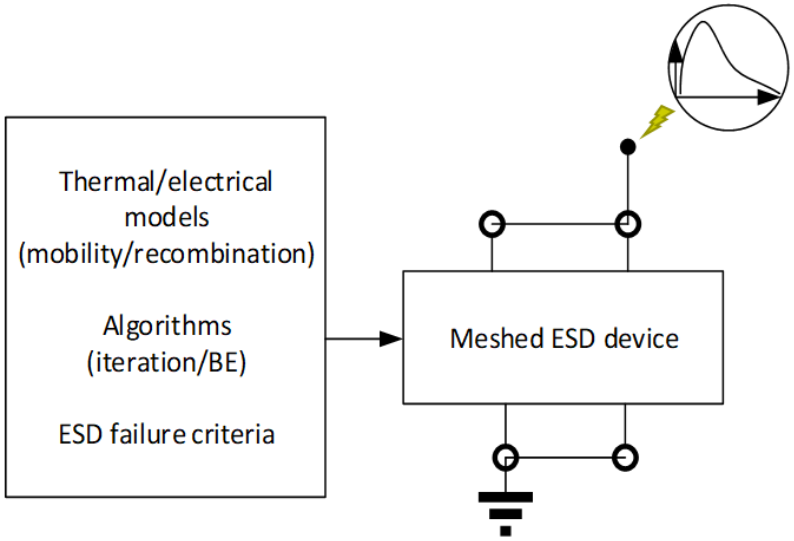


Figure 6-18 Sdevice simulation bench

For the electrons and holes mobility, it is doping dependent. As higher doping level will contributes to higher mobility. ESD events features high voltage and rapid discharge, as a result, the high field saturation effect must be considered. Another physical effect associated with high field is the carrier-carrier scattering. The overall mobility degradation caused by carrier scattering is captured using Brooks-Herring screening theory. Electrons and holes recombination is another important physical mechanism in semiconductors. Recombination through deep defect levels in the gap is usually labeled Shockley–Read–Hall. This effect is temperature and doping dependent. Auger effects also contributes to the recombination process. Thus, Auger recombination needs to be included. Avalanche is an important effects for junction reverse conducting, which generates the "seed" current to trigger BJT and SCR structure. Electron–hole pair production due to avalanche generation (impact ionization) requires a certain threshold field strength and the possibility of acceleration. For the driving force, "GradQuasiFermi" is recommended for ESD simulation. ESD

event often comes with large current surge in company with sudden thermal change. Therefore, thermal effects need to be take in to consideration. Thermal energy and thermal-dynamic models are used in simulation.

```
Physics { EffectiveIntrinsicDensity ( OldSlotboom )
        AreaFactor=1200
     Mobility ( DopingDep ( UniBo )
         HighFieldSaturation ( GradQuasiFermi )
         CarrierCarrier ( ConwellWeisskopf )
       )
     Recombination ( SRH ( DopingDependence  TempDependence )
          Avalanche ( UniBo2 GradQuasiFermi )
          Auger
       )
      Thermodynamic
      AnalyticTEP
```

Figure 6-19 ESD simulation related models

To solve differential equations associated with the physics models, Synopsys TCAD uses finite element analysis, which requires a mesh to identify calculation points. Suitable mesh is important for convergence and time efficiency. Specify for ESD event, mesh has to be designed according to physics process. For example, as mentioned before, mobility and recombination are doping dependent, therefore, for better convergence, the mesh can be sparser at low doping area and show higher density in high doping area. Avalanche occurs when junction is reverse biased. Therefore, mesh should be dense enough across junction area to fully capture this effects. The same concept also applicable to thermal-dynamics. Heating effect often caused by current crowed effects, which indicates a rapid rise in current density due to device geometry. Around the predicted hot spot, mesh should be more condensed. For better convergence in the TCAD ESD simulation, doping adaptive meshing method are utilized with refinement around junction and hotspot area. Then the meshed device is put into the Mixed-Mode simulation bench to conduct ESD simulation. Connections of electronic nodes are defined by script. For example, gate of NMOS are set to be connected with ground in the Mixed-Mode script. HBM or CDM waveform is injected with a

current source. Poisson equations and Kirchhoff Circuit Laws are applied to the system level simulation. The outcome will be the simulation result.

6.4.3. Simulation guide ESD design

The last step of TCAD simulation flow is to inspect the simulation result. The TCAD simulation can provide the lattice temperature, current density and direction, voltage potential and the contribution of each physics effect on every nodes. Here a simulation result of a GGNMOS is depicted as an example. Figure 6-20 depicts the doping concentration of a GGNMOS. The color code for n-type doping is red and for p-type is blue. Darker color means higher doping level. Figure 6-22 shows the current density distribution on FinFET under ESD peak current. The red color code depicts the current density. The current line indicates current flow, which also shows the current density with sparse line means lower current density.

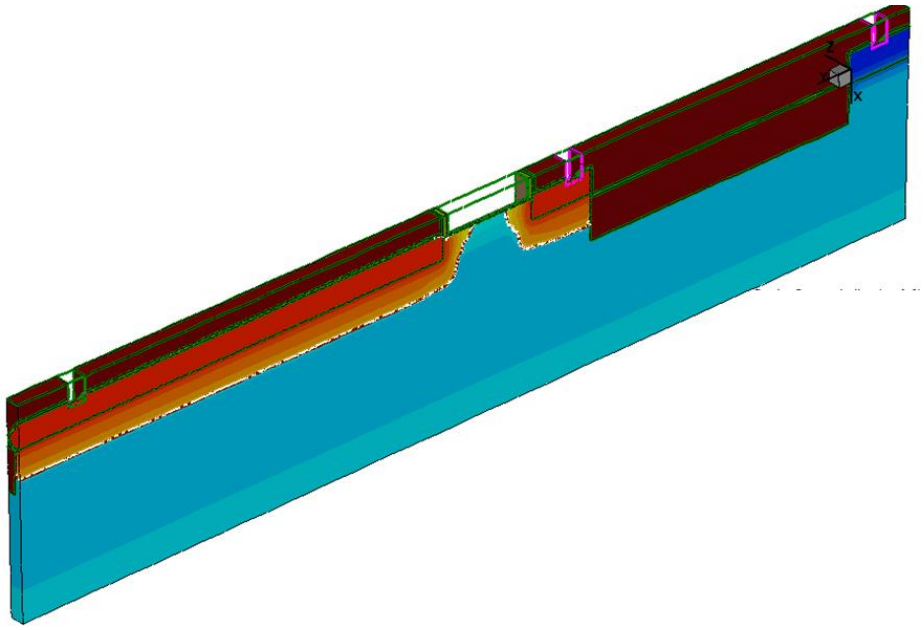


Figure 6-20 Doping concentration

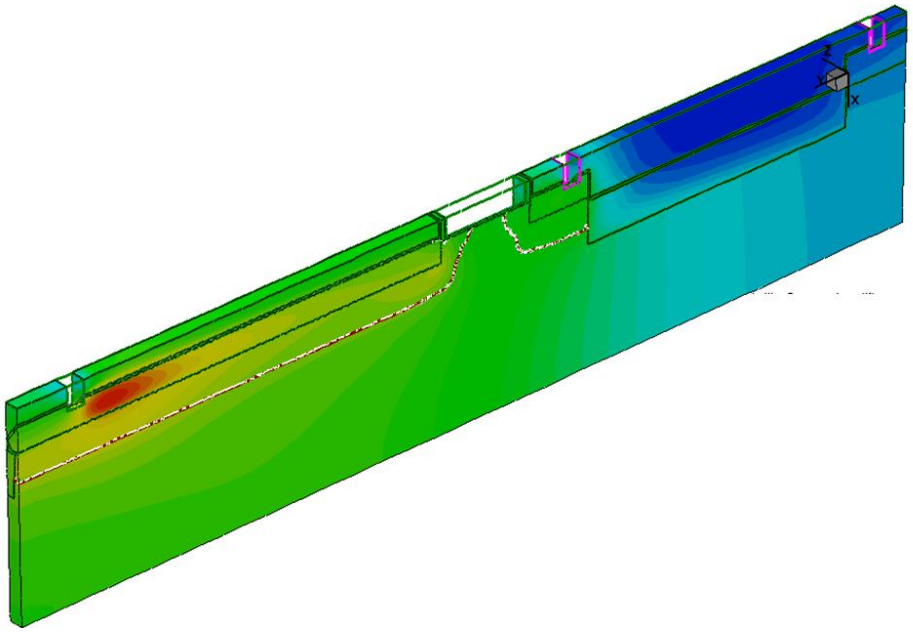


Figure 6-21 Lattice temperature

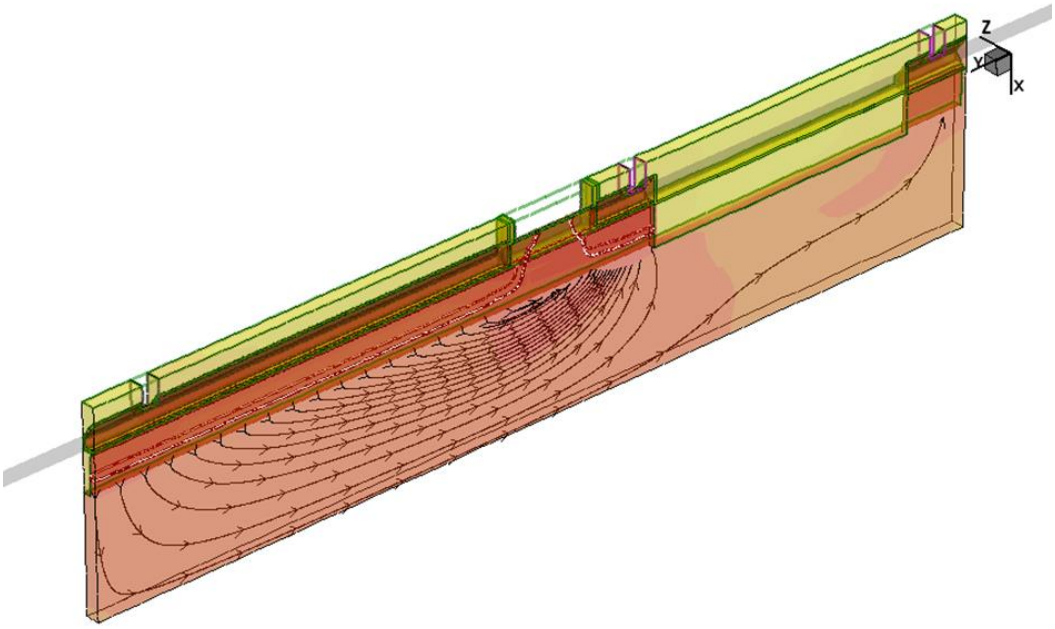


Figure 6-22 Current density

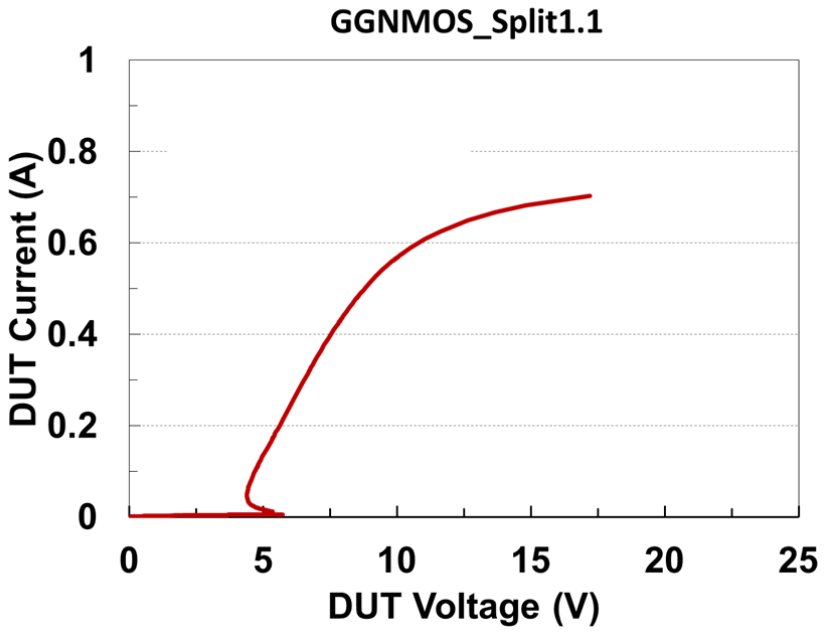


Figure 6-23 Simulated I-V curve of GGNMOS with snapback

From the simulation result, many features of GGNMOS in FinFET are revealed. First, from the lattice temperature distribution, it's obvious that the hot spot locates near drain contact and in fin region. This is due to the current are sparser in bulk area than fin area, which causes higher current density in fin region. From the current density distribution plot, the density of current line indicates current density at that point. It is clear that the increased length between drain contact and gate helps conducting current evenly. Also, body pickup takes small portion of ESD current, most ESD current were discharged through parasitic bipolar. Figure 6-23 shows the simulated I-V curve of GGNMOS, which shows a beautiful snapback behavior. By conducting a series simulation experiment, the simulation result can instruct the design works both in values and trends. For example, by increasing the width of GGNMOS (in FinFET process, it's equal to increase fin number), the turn on resistance will decrease. What's more, as fin number increase, the power handling ability of designed GGNMOS will increase. From the 3D TCAD simulation result shown

in Figure 6-24. When fin number larger than 4000, the GGNMOS device can survive HBM 2KV, which can give designer a guidance.

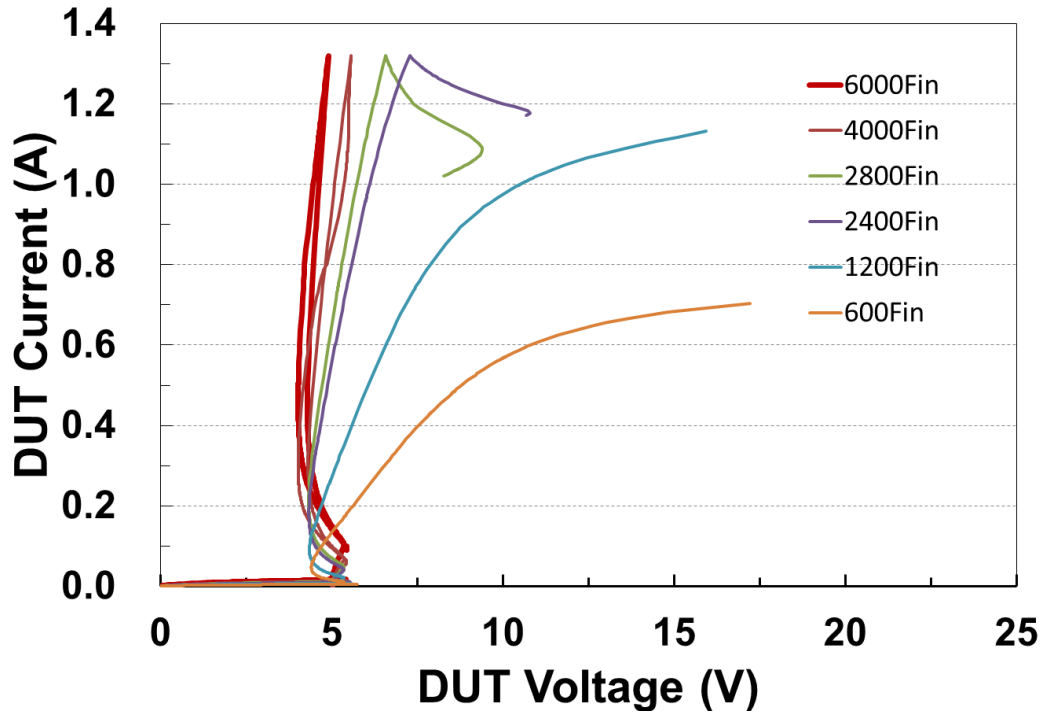


Figure 6-24 Mixed-mode TCAD simulated result of GGNMOS with different fin number (width)

The TCAD simulation is also capable to help designer find the optimized device design parameters: by set a split of design parameter and observe the simulated current density, hot spot distribution, and transient response, ESD device designer will be able to find the weak point of design and optimize the design.

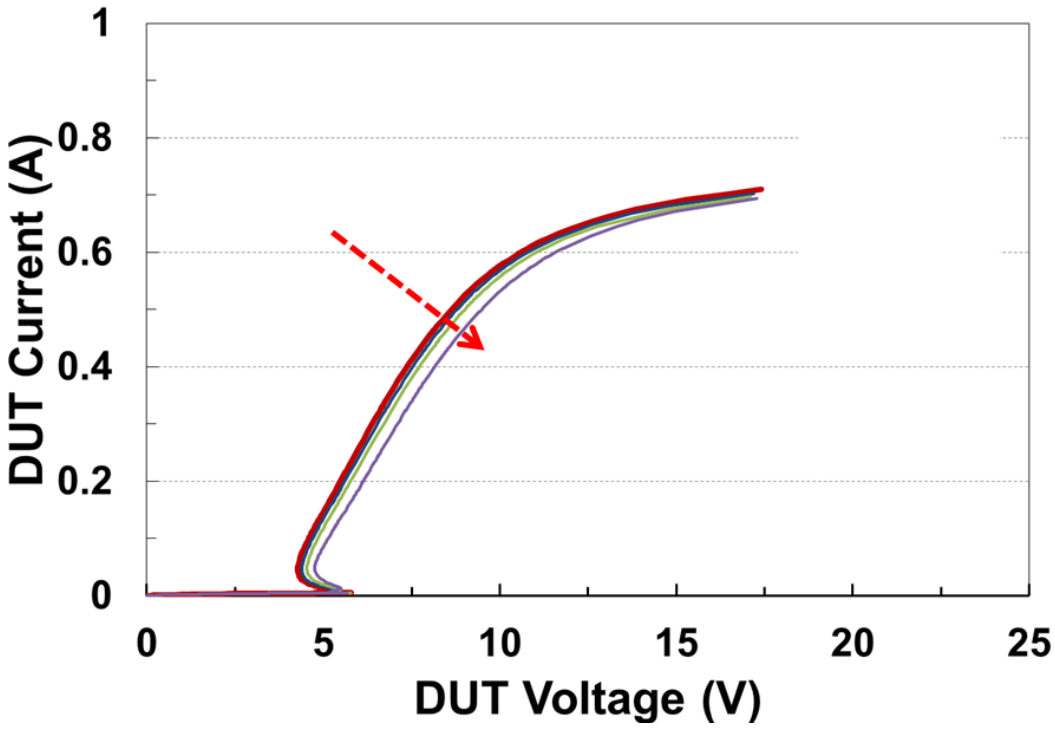


Figure 6-25 Mixed-mode simulation result of GGNMOS with different gate length

Figure 6-25 shows the TCAD simulation result of GGNMOS with a set of different gate length. Form the simulation result, it clearly shows with change in gate length, only minor influence to the electronic performance was shown: triggering voltage and current handling ability does not show much improvement. What's more, the temperature distribution also not change much as shown in Figure 6-26. Hot spots moves a little bit to the gate region as gate length decrease. But the overall ESD performance doesn't improve much. Therefore, from layout area consideration, designer can use minimized gate length to save are and put in more fingers.

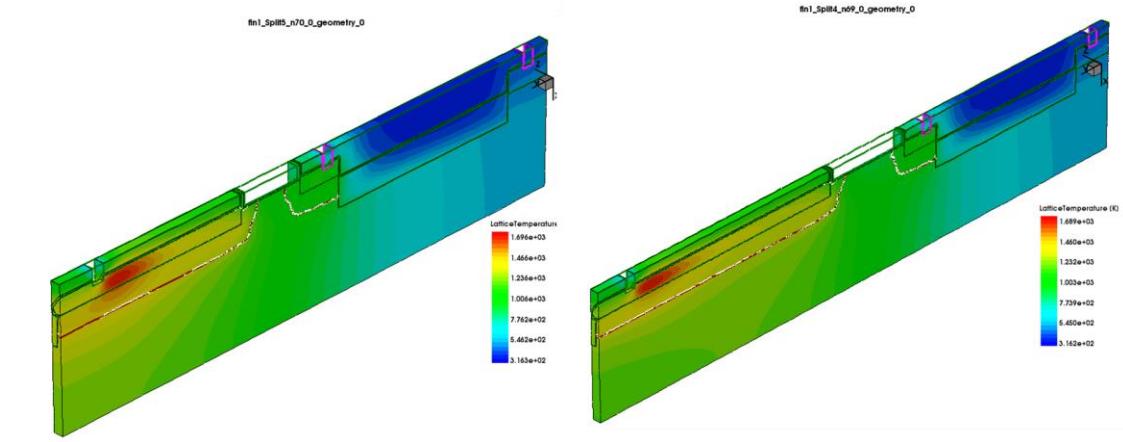


Figure 6-26 Lattice temperature simulation show minor change between GGNMOS with different gate length

The same methodology also apply to other parameters. For example, the DCGS which identify the value of drain ballast resistance and ESD current density across drain area. As discussed before, a successful DCP design will improve the power handling ability. Here, DCGS is designed up to 2um (green line in Figure 6-27), which is absolutely too large for GGNMOS. The simulated It2 shows ignorable improvement while the Ron increases significantly.

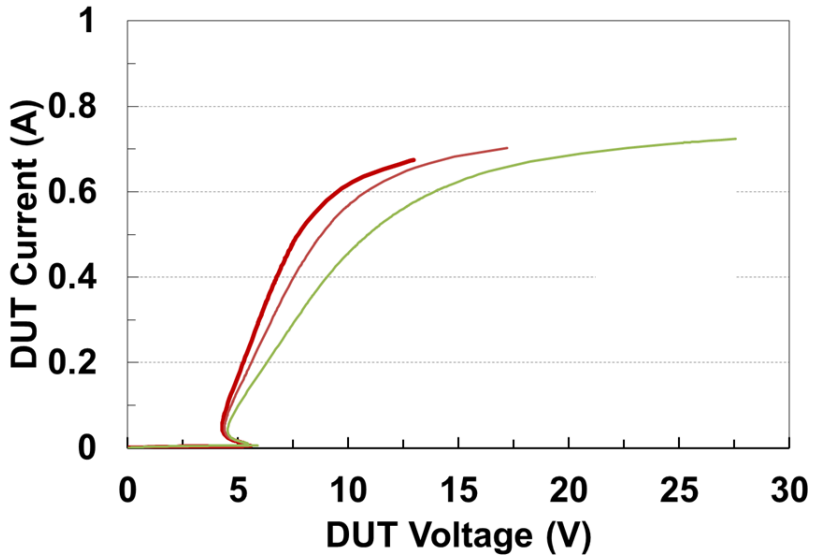


Figure 6-27 Mixed-mode simulation result of GGNMOS with different DCGS length

Further simulation on the parasitic capacitance shows the increase in DCGS length can cause huge increase in parasitic capacitance. Therefore, the lower DCGS value is appropriate to GGNMOS design (Figure 6-28).

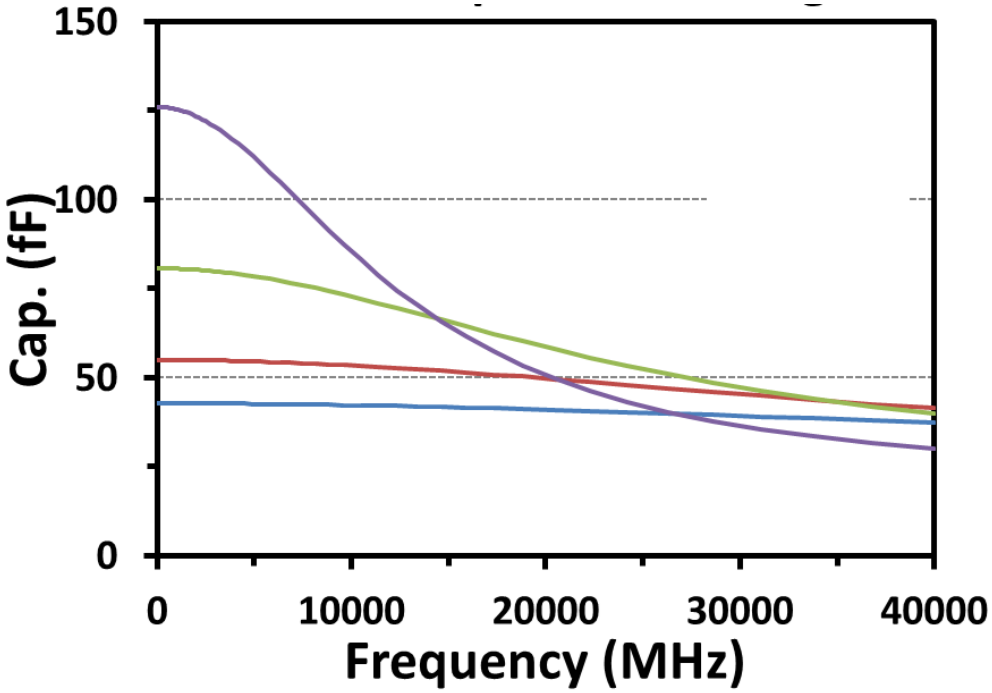


Figure 6-28 TCAD simulation result of parasitic capacitance

In this chapter, FinFET ESD design is introduced and a 3D mixed-mode TCAD simulation flow is presented, which can provide designer pre-silicon data and help designer optimized ESD device design. Adaptive mesh is applied for better simulation convergence. Sdevice models are selected to characterize the complicated thermal-electrical ESD events. Then, a simulation case of GGNMOS is presented as an example. The simulation result can be used to guide the ESD layout and design works.

Chapter 7. Full-Chip ESD Protection Simulation Methodology

7.1. Introduction of Circuit level ESD Protection Simulation

As semiconductor technologies rapidly advance into Nano nodes and FinFET technology domains, meanwhile IC chip complexity continuously increases, on-chip ESD protection design becomes extremely challenging. Circuit simulation can be conducted for simple timing analysis, which however cannot simulate ESD protection functions for most ICs that typically uses ESD protection structures featuring complex snapback I-V behaviors. Due to lack of accurate ESD device models and suitable full-chip ESD simulation CAD tools that can fully address the complex electro-thermal-process-device-circuit-layout coupling effects associated with ESD discharging behaviors, chip-scale ESD protection circuit design verification is still impractical for real world designs [33]. Tremendous research efforts have been given to develop various ESD modeling and simulation techniques. TCAD-based mixed-mode ESD simulation-design method was reported to simulate small I/O blocks with ESD protection structures that do not require compact ESD device models, which is however impractical to handle large circuits. Physics-equation-based models were reported for ESD simulation, which is still inaccurate and hindered by convergence problems in practical ESD circuit simulation [47][48][49]. A new technology-independent ESD CAD tool was reported for whole-chip ESD protection circuit design verification, which uses a novel CAD algorithm to extract arbitrary ESD structures and generate an ESD netlist directly from an IC layout data file, hence perform ESD-function-based design verification [50][51]. Recently, [52] reports a chip-level dynamic ESD simulation technique, which however relies on a numerical method for substrate analysis, as well as technology and layout data, all are impractical for ordinary circuit designers. G.Langguth [53] describes using ESD sub-circuit models for SPICE ESD simulation, which is limited by accuracy and availability of ESD device models for different ESD structures

due to the complexity of ESD discharging behaviors, such as high current and over-heating phenomena, layout irregularity and transient dV/dt effect. N.Trivedi [54] depicts an integrated ESD checking flow combining DRC, topology and interconnect checking, which is a static checking technique. S.Poon [55] presents a full-chip ESD simulation method, however, it can only check node voltage failures, ignored ESD current failures, and can only handle non-snapback ESD devices. In real-world IC designs, an practical circuit-level ESD simulation and quick dynamic ESD checking technique is highly desirable that should allow ordinary IC designers to conduct comprehensive, quantitative and efficient full-chip ESD protection circuit simulation and design verification that is entirely based on ESD discharging functions.

This chapter discusses a simple and fast schematic-level ESD simulation and dynamic checking method using SPICE and ESD device behavior models that allows IC designers to quickly verify ESD protection circuit designs at full chip level. Circuit designers rely on CAD tools, e.g., SPICE, to design ICs following a common flow: schematic, pre-simulation, layout, post-simulation, verification, extraction, post-simulation and tape-out. The goal of this new circuit-level ESD protection circuit design method is to provide a SPICE-based circuit design flow allowing ordinary IC designers to conduct ESD-function-based full-chip ESD protection design simulation and analysis to verify ESD protection performance at full chip level before tape-out.

Figure 7-1 depicts the design flow of the new ESD circuit simulation method. The design flow starts from defining the specs for both core circuit and ESD protection of an IC chip.

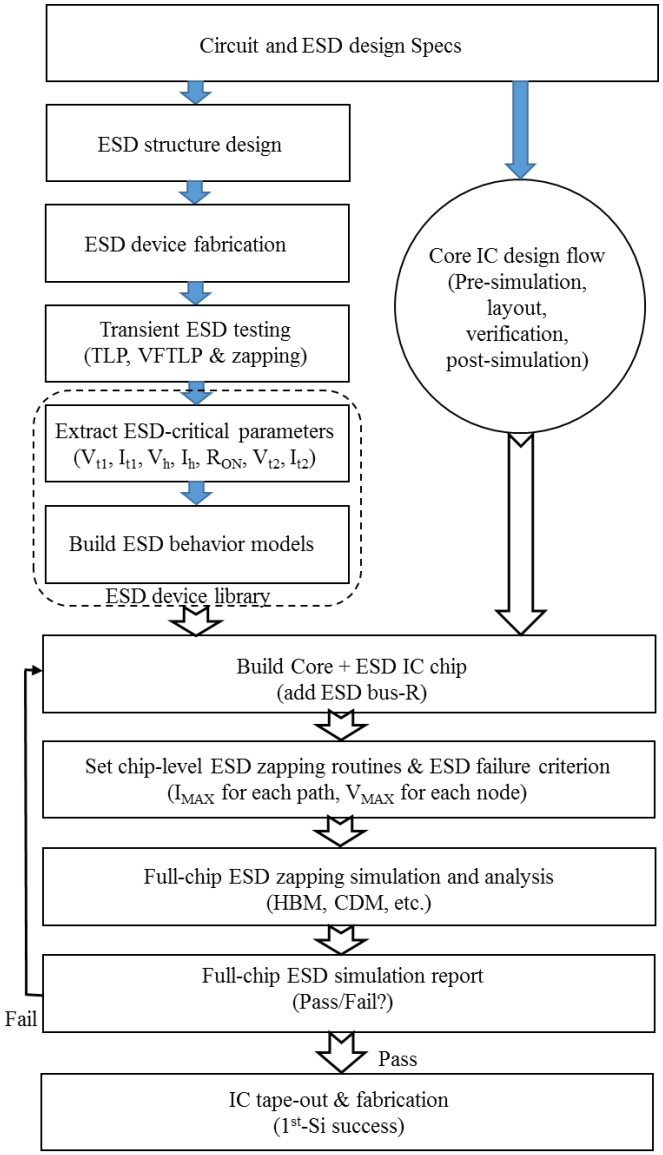


Figure 7-1 A flow chart for the new full-chip circuit-level ESD protection circuit simulation and analysis method.

Typically, for a given IC technology, ESD structures will be designed and optimized, which will be fabricated and tested [31][33]. Comprehensive transient ESD characterization include transmission line pulse (TLP) for human body model (HBM), very-fast TLP (VFTLP) for charged device model (CDM) and ESD zapping test. TLP/VFTLP testing reveals all ESD-critical parameters, e.g., ESD triggering voltage (V_{t1}) and current (I_{t1}), holding voltage (V_h) and current

(I_h), discharging resistance (R_{ON}), and failure voltage (V_{t2}) and current (I_{t2}), which define the ESD Design Window on a chip. Numerical characterization of an ESD protection structure or sub-circuit at chip level is required to accommodate the ESD Design Window Shrinking Effect for advanced IC technologies [56]. The transient discharging I-V characteristics for the ESD structures will be studied to extract the corresponding ESD device behavior models [57]. The advantage of ESD behavior modeling is that it circumvents the technical barrier of no good compact ESD device models for ESD circuit simulation. An ESD library will be built up consisting of the verified ESD protection structures and their behavior models for a given IC technology. This task is handled by either the IC foundries or the design service team in a fabless design house. Since the ESD behavior models are extracted from the measured ESD I-V curves, they are very accurate. An IC designer can go through the normal IC design flow to complete design of the IC core circuit. In the next step, the IC designer will select suitable ESD devices from the ESD library and integrated the selected ESD devices into the IC core to complete the whole IC chip (ESD + core circuit). It follows that the full chip (ESD + core) can be simulated using SPICE to study the ESD protection functions at circuit level. Since ESD current is typical very large, the metal bus resistance in an ESD discharging path may play a significant role in full-chip ESD protection design. Hence, the ESD interconnect resistance (bus-R) should be extracted and included in the chip-level ESD circuit simulation. At this point, circuit level ESD protection simulation can be conducted using SPICE similar to normal IC simulation except for: 1) using an ESD pulse as the stimulus, 2) following chip-level ESD zapping routines, and 3) analyzing ESD protection performance per ESD failure criteria. First, it is obvious that, for ESD circuit simulation, the input signals must be transient ESD pulses, i.e., the ESD pulse waveforms defined in ESD testing standards for HBM, CDM, MM, IEC or any other ESD testing models. The ESD stimuli can also be TLP or VFTLP waveforms. Second, unlike typical IC simulation using a small sinusoidal signal, chip-level ESD simulation routines are

very complicated and time-consuming according to the industrial standard ESD zapping test procedures. Briefly, each pad (I/O, control and supply) must be zapped by a set of ESD pulses with respect to a reference pad, while all other pads on a chip have to be handled per an ESD testing standard selected, e.g., all open or all grounded. Meanwhile, each pad must be zapped against a positive supply pad (V_{DD}) and a negative supply pad (V_{SS}) positively (PD and PS modes) and negatively (ND and NS modes). Each supply pad (V_{DD}) must also be zapped against another supply pad (V_{SS}) positively (DS mode) and negatively (SD mode). Further, each pad must be zapped several times for each zapping mode, typically three times. Therefore, full-chip ESD zapping test is extremely tedious, time-consuming and costly, which makes the new chip-level ESD circuit simulation method even more desirable and valuable. Accordingly, a proper full-chip ESD zapping routine must be defined and programmed for ESD circuit simulation. Third, full-chip ESD simulation analysis is much more complicated than typical SPICE circuit simulation. According to the ESD-critical parameters and the ESD Design Window, chip-level ESD simulation must be analyzed for at least two ESD failure criteria:

- Criterion-1

The maximum allowed voltage (V_{MAX}) at the protected nodes, typically defined by the breakdown voltage (BV) the nodes, against the simulated ESD clamping voltage (VESD) at the same nodes. If VESD<VMAX holds for all pads, then the chip passes the ESD testing; otherwise, ESD failure will occur.

- Criterion-2

The maximum sustainable current (IMAX) for each ESD discharging path against the simulated maximum ESD charging current (IESD) in the same path. Typically, IESD is same as the It2 of the ESD protection structure. If IESD>IMAX holds for all ESD discharging paths, then the chip passes the ESD testing; otherwise, it fails the ESD testing. In practice, a safety margin

(10%~20%) needs to be defined for an IC.

The results for the whole-chip ESD circuit simulation should be analyzed carefully. If an ESD failure occurs, the IC designer will go back to check and revise the ESD protection designs, for example, using an ESD device featuring suitable Vt1, RON or It2. If the chip passes the comprehensive circuit-level ESD simulation, one can proceed to tape-out the design for fabrication and expect first-Si ESD design success. This new chip-level ESD protection circuit simulation and analysis method were validated by several ICs fabricated in foundry IC technologies as discussed below.

7.2. Design Validation and Discussions

The new circuit-level ESD simulation method was verified using several ICs designed and fabricated in foundry 28nm CMOS and 45nm SOI technologies.

7.2.1. Input Buffer with Full ESD Protection

The first example is an input buffer circuit with full ESD protection designed in a foundry 28nm CMOS. Figure 7-2 shows the block diagram for the IC featuring ESD protection at the input and between the power supply buses with its layout shown in Figure 7-3. The targeted ESD protection is 2KV per HBM model. The 28nm CMOS features V_{DD}=0.9V and typical breakdown of BV_{GS}=8.52V and BV_{DS}=7.01V, which defines the ESD Design Window. The input ESD protection utilizes an N+/P-well diode for power-down ESD protection (PD-ESD) against GND and a P+/N-well diode for power-up ESD protection (PU-ESD) against V_{DD}.

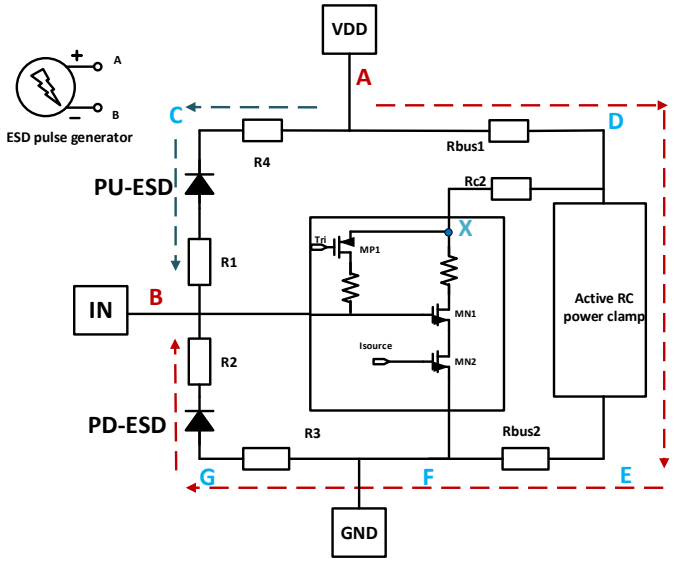


Figure 7-2 Simplified functional diagram for the input buffer IC with full ESD protection for chip-level ESD protection circuit simulation. The key ESD metal resistances were extracted from its layout below.

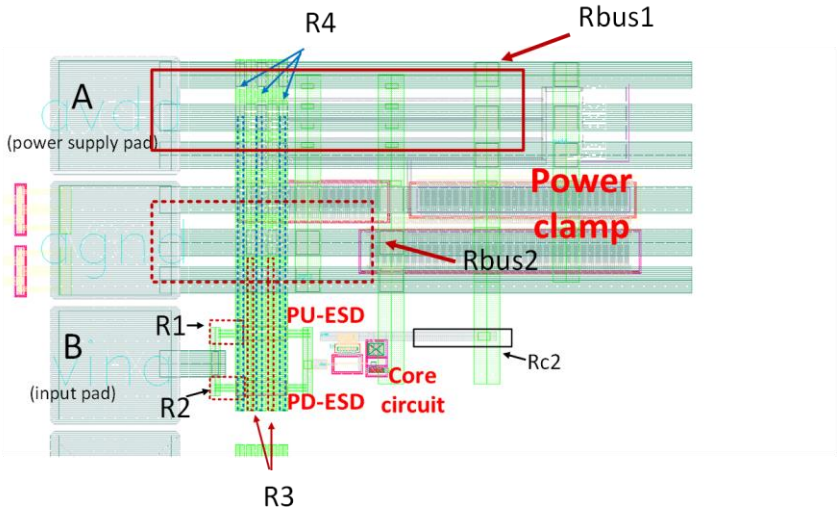


Figure 7-3 Layout of the ESD-protected input buffer IC where key ESD metal resistances are extracted for full-chip ESD circuit simulation.

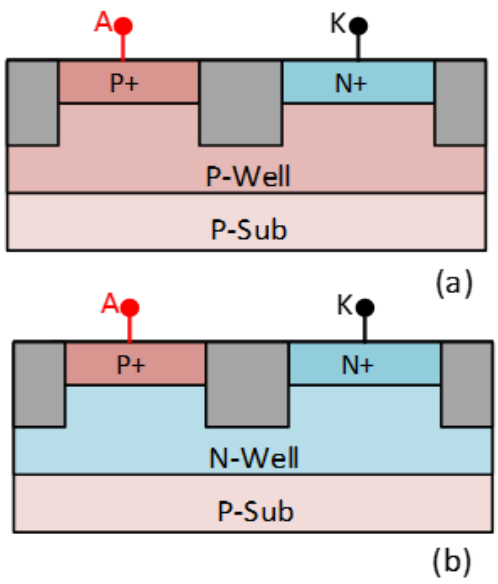
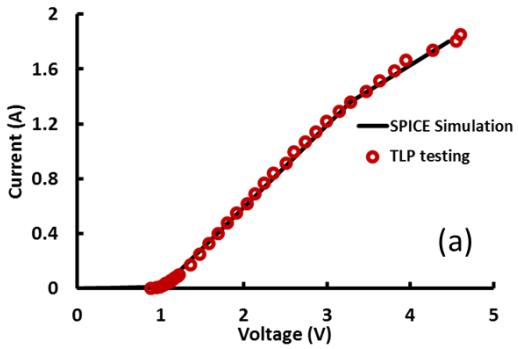


Figure 7-4 Simplified cross-sections for the STI ESD diodes in this work: (a) N+/P-well PD-ESD diode and (b) P+/N-well PU-ESD diode.

Both ESD didoes, shown in Figure 7-4, feature shallow trench isolation (STI) to minimize the parasitic capacitance for high-speed ICs. An active RC power clamp is used to protect the power rail. As part of the whole project, these ESD protection structures were first designed and fabricated, which were then characterized by TLP testing that delivers the transient ESD discharging I-V curves and their ESD-critical parameters, including the critical V_{t1}, V_h, R_{ON} and I_{t2}.

Figure 7-5 presents the measured ESD discharging I-V curves for the ESD diodes that were used to extract the ESD device behavior models, which are saved in the ESD library for circuit-level ESD simulation. The TLP measurement shows that the ESD thermal failure currents are about I_{t2}=1.8A (i.e., HBM 2.7KV) for the PD-ESD diode and I_{t2}=2.3A (i.e., HBM 3.5KV) for the PU-ESD diode, respectively. The reverse ESD triggering voltage for the PU-ESD diode is about V_{t1}=-8V per TLP testing. Accuracy of the extracted ESD behavior models is critical for circuit simulation, which was confirmed by SPICE simulation for the ESD diodes using the corresponding ESD behavior models as depicted in Figure 7-5. Due to large ESD currents, full-chip ESD circuit

simulation must include key ESD metal interconnect resistances, which depends entirely on the IC layout. For this purpose, the metal interconnects for ESD connections are characterized first by TLP for the metal interconnects in the back-end-of-line (BEOL) of the 28nm CMOS. Figure 7-6depicts the transient I-V characteristics for one sample metal stack, the M_X (M2-M5), by TLP testing. The TLP-measured sheet-resistance is around $R_{\square}$=1Ω/☐ for M_X stack and $R_{\square}$=0.3Ω/☐ for the M-y stack (M8-M10), both used for ESD interconnects in this design. According to the layout (Figure 7-3), the extracted ESD metal resistances are: R_{bus1}=1.5Ω between V_{DD} and power clamp anode (using M10, L=183μm and W=36μm), R_{bus2}=0.3Ω from the power clamp cathode to GND, R_1=1Ω between Input pad and cathode of PU-ESD, R_2=1Ω between Input and PD-ESD anode, R_3=1.15Ω from PD-ESD cathode to GND and R_4=0.6Ω from V_{DD} to PU-ESD anode. These key ESD metal bus resistors are included in schematic test bench as shown in Figure 7-2.



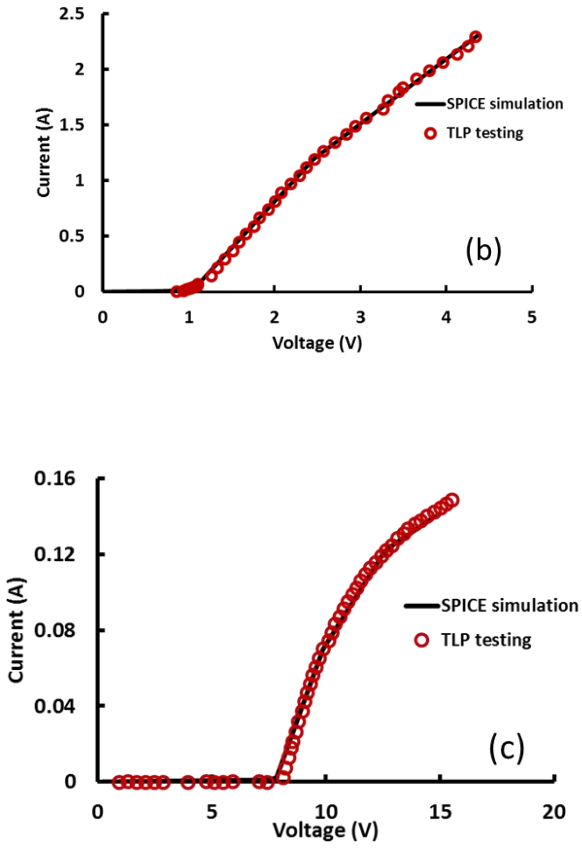


Figure 7-5 Transient ESD I-V curves measured by TLP for, (a) N+/P-well diode (forward ESD mode), (b) P+/N-well diode (forward ESD mode) and (c) P+/N-well diode (reverse ESD mode), match well with SPICE simulation using the extracted ESD behavior models accordingly.

Comprehensive full-chip ESD circuit simulation using the new method was conducted for the ESD-protected input buffer IC to study its compliance against the ESD Design Window. The input stimuli for ESD simulation are 2KV HBM ESD pulses with the required ESD zapping routines and polarities as discussed previously. The simulated node voltages and branch currents under ESD stressing are carefully examined for the IC. Take one ESD zapping case as an example, which applies a negative HBM ESD pulse to the Input pad with respect to V_{DD} (i.e., ND ESD mode where the ESD pulse occurs to node B, while node A is grounded).

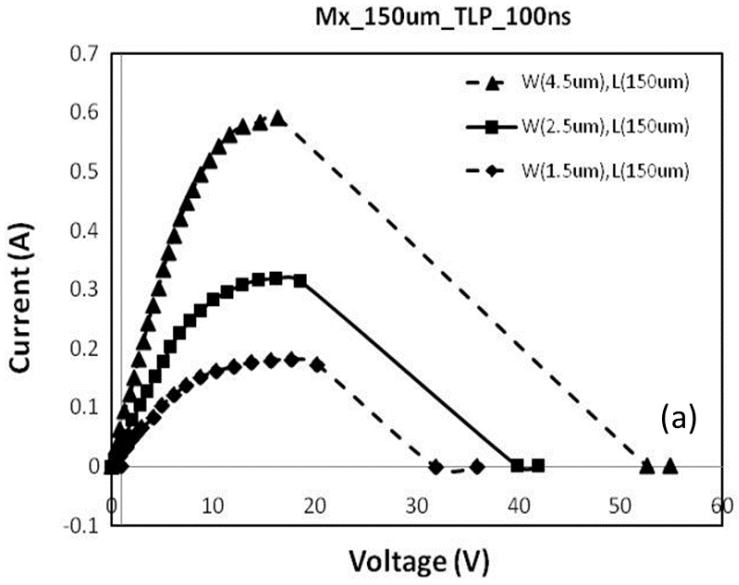


Figure 7-6 Transient ESD I-V curves by TLP testing for an example M_X metal stack (M3-M7) used for ESD interconnects in this work.

Figure 7-7 depicts the circuit node transient voltages under ESD zapping. Figure 7-8 presents the ESD discharging currents and transient voltage for the core circuit transistors by ESD simulation. Per design, the intended main ESD discharging path would be the route-ADEFGB (Red line, conduction through the active ESD power clamp and PD-ESD diode in forward mode) that is confirmed by ESD circuit simulation (Figure 7-2 & Figure 7-8). Figure 7-7 clearly shows that VDE<2.5V for the power clamp, the voltage across the PD-ESD diode remains smaller than 2.7V, and the voltage from VDD to GND across the core circuit (VDF) is less than breakdown of BVDS = 7.01V of the core circuit transistor, which confirms a successful design of the PD-ESD diode and the ESD power clamp.

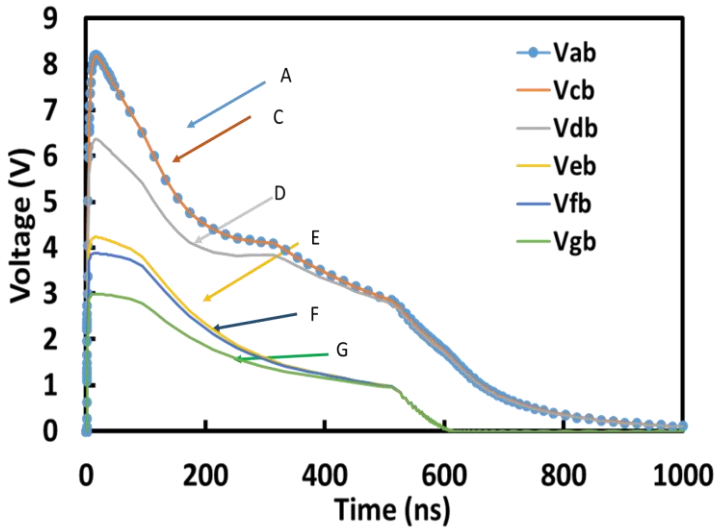


Figure 7-7 Simulated transient node voltages for the ESD-protected input buffer IC using the new ESD simulation method under an ND mode 2KV HBM ESD zapping to the input pad (B) against V_{DD} (A). Note that all voltages are referred to node-B.

However, ESD simulation also found a transient current of around 40mA in the route-ACB (Marked in Blue, conduction via PU-ESD diode in reverse mode, Figure 7-2 & Figure 7-8), which is because the voltage at Node-C exceeds the reverse BV (7.98V) of the PU-ESD diode (Fig. 7, i.e., the reverse ESD triggering voltage Vt1) during the ESD stressing period. Fig. 8 also confirms that VDS<BVDS~7.01V for MP1 and VGS<BVGS~8.52V for MN1 of the core circuit during the ESD stressing. This analysis suggests that the ESD design works for 2KV HBM zapping, though the PU-ESD diode (reverse mode) seems to be a weak point. This analysis was confirmed by the Emission microscopy (EMMI) image shown in Figure 7-9, where a hot spot was observed at the PU-ESD diode location under HBM zapping. More analysis indicates that this issue may be associated with the higher-than-expected ESD metal resistance that led to a total voltage drop reaching to 4V, which may be revised by re-designing the ESD metal to reduce the total ESD discharging R_{ON}. In summary, this example validated the new chip-level ESD circuit simulation

and analysis method and reveals its value of helping IC designers to analyze full-chip ESD design, to pin-down ESD design weak points and to optimize ESD protection design for a whole chip.

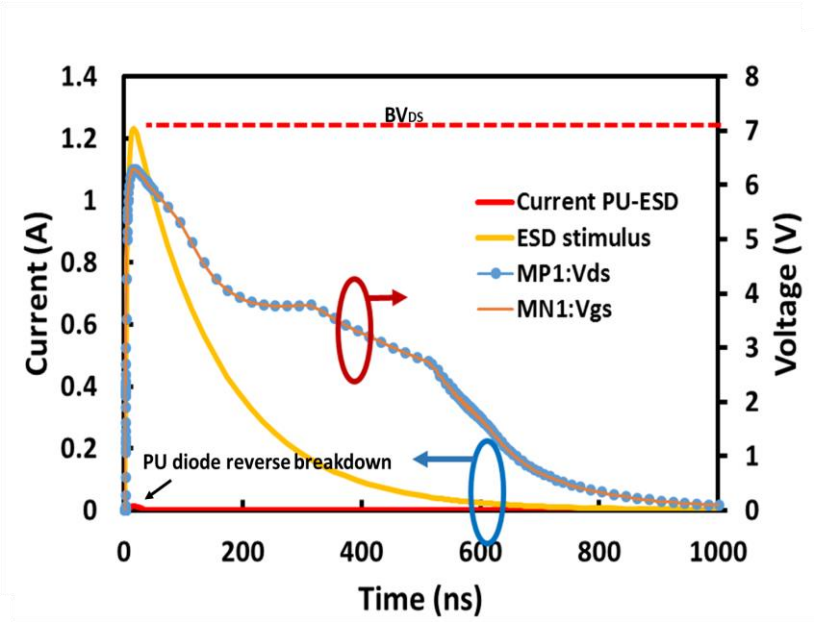


Figure 7-8 Simulated branch currents (Left axis) and core circuit transistor voltages (Right axis) under the ND mode ESD zapping from Input pad (B) to V_{DD} (A).

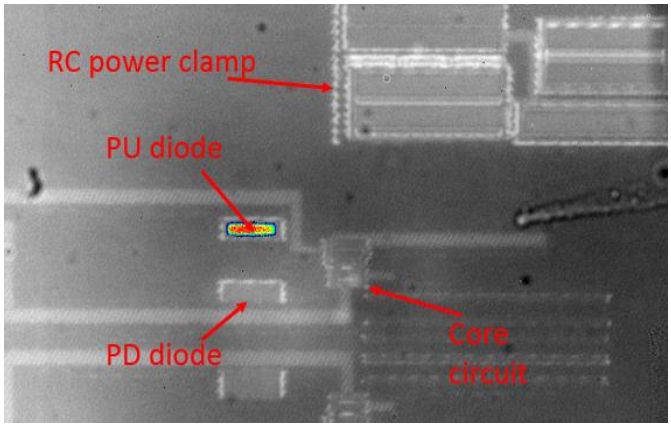


Figure 7-9 An EMMI image under HBM zapping reveals a hot spot at the PU-ESD diode, indicating an ESD weak point in the design.

7.2.2. Large IC with Snapback DTSCR ESD Protection

The second example is a ESD-protected 7-bit pseudorandom binary sequence (PRBS) generator circuit, including D flip-flop and XOR gate, designed and fabricated in another foundry 28nm CMOS with BV_{DS}~5.6V and BV_{GS}~5.2V. The purpose is to validate the new ESD circuit simulation method using a large-scale IC with ESD protection featuring snapback I-V behavior that cannot normally be handled by SPICE simulation. Figure 7-10 shows the IC schematic where I/O ESD protection devices are diodes and the power clamp is a diode-triggered silicon-controlled rectifier (DTSCR) ESD structure. An SCR ESD protection structure is normally very ESD robust because of its snapback I-V behavior, low V_h, very high I_{t12} and very low R_{ON}. Unfortunately, the V_{t1} of SCR is too high for advanced CMOS. DTSCR utilizes diodes to trigger the SCR, hence achieves very low V_{t1}. Following the new ESD circuit simulation method, the diode and DTSCR ESD structures were designed, fabricated and characterized by TLP with the ESD I-V curves shown in Figure 7-11. TLP testing found a very low V_{t1} ~ 3.19V for DTSCR, good for 28nm CMOS ICs, and V_{t1} ~ 1.03V at 10mA for the gated diodes, also suitable for I/O ESD protection in forward mode since V_{DD} = 0.9V in this 28nm CMOS. ESD behavior models were then extracted for the diode and DTSCR ESD devices, which were verified by SPICE simulation (Figure 7-11).

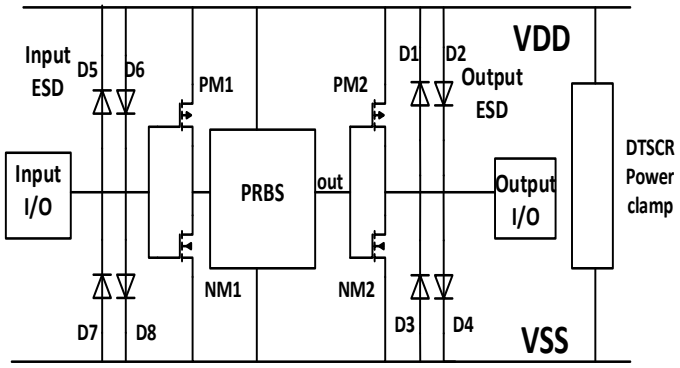


Figure 7-10 A functional schematic for the ESD-protected PRBS IC where gated ESD diodes (D1-D8) protect I/O pins and the power clamp is a DTSCR.

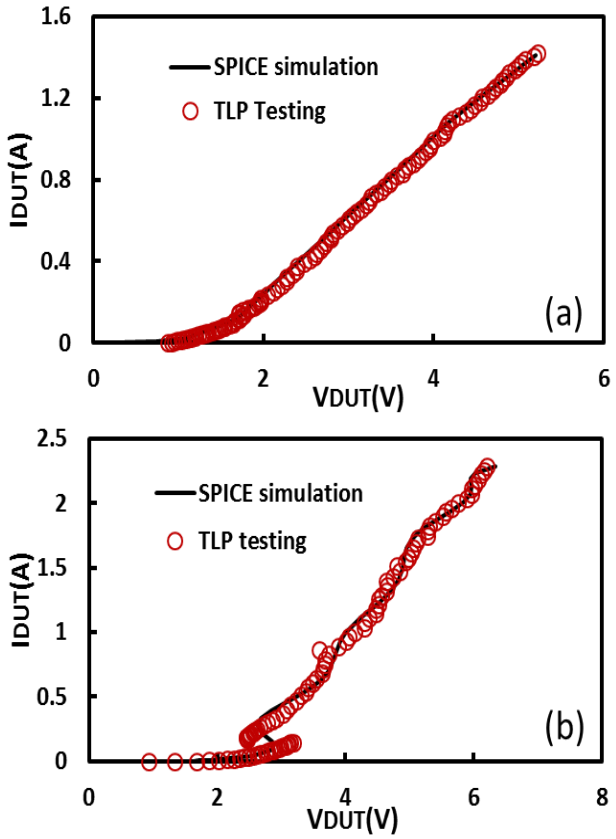


Figure 7-11 ESD I-V curves by TLP testing (Blue) agree well with SPICE simulation (Orange) using the extracted ESD behavior models for: (a) gated diode and (b) DTSCR.

Comprehensive circuit-level ESD simulation was then conducted for the full chip by the new method using HBM ESD pulses as stimuli. Figure 7-12 shows two exemplary ESD circuit simulation cases. First, Figure 7-12a presents a positive Input-to-V_{SS} zapping case (PS mode) where D_8 is the intended ESD discharging path. In addition, two possible unintentional ESD discharging paths, D_5+DTSCR and D_5+D_2+D_4, may exist during HBM zapping. Figure 7-13a depicts the simulated ESD discharging currents for each path, which readily shows that almost all ESD surge is discharged through input ESD diode (D_8) in forward mode as designed, while negligible current seen in any unwanted path.

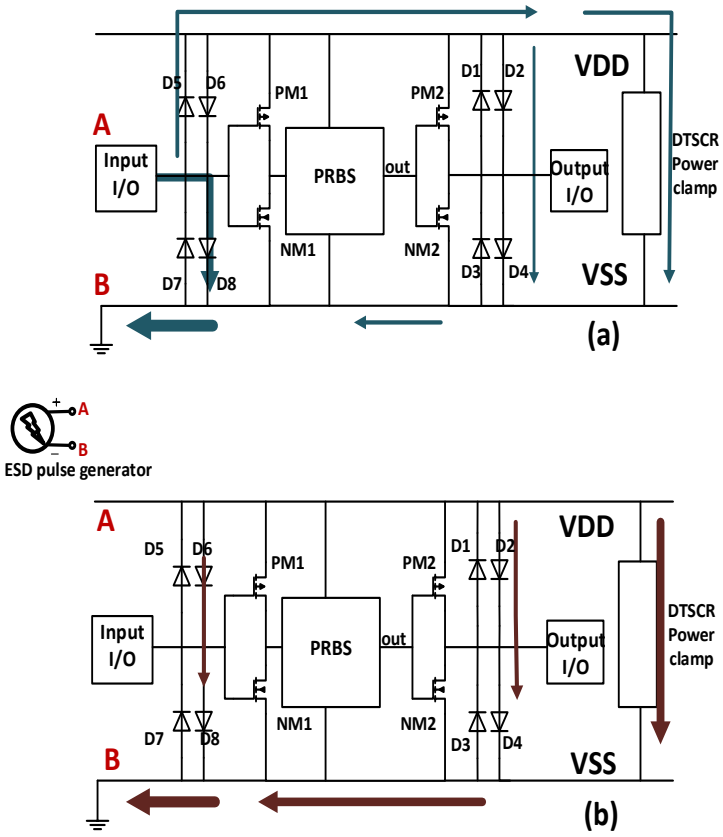


Figure 7-12 Two exemplary full-chip ESD simulation cases: (a) positive Input-to-V_{SS} HBM zapping, and (b) positive V_{DD}-to-V_{SS} zapping. The arrowed lines indicate the possible ESD discharging paths with the thickness suggesting the amount of ESD discharging current.

Figure 7-12b depicts a positive V_{DD}-to-V_{SS} zapping case where the DTSCR power clamp is the intended ESD charging path, which is confirmed by ESD simulation given in Fig. 13b showing conducting >70% of the ESD stimulus due to very low R_{ON} in DTSCR. Meanwhile, there are two other unintentional paths, D_2+D_4 and D_6+D_8, which conduct a small amount of the ESD current as shown in Figure 7-13b. The peak V_{DD}-to-V_{SS} voltage corresponds to the V_{t1} of DTSCR during HBM zapping. In summary, this design example confirms that the new ESD circuit simulation method can handle SCR-type ESD structures with snapback I-V behavior and works for large ICs for full-chip ESD circuit simulation and analysis.

7.2.3. RF Switch Circuit with Graphene NEMS ESD Structure

A good CAD tool should be technology-independent and be able to handle various emerging and non-traditional devices [40]. In fact, traditional in-Si PN-based ESD protection structures have many inherent disadvantages, such as parasitic capacitance, leakage and noise, which are becoming intolerable to parasitic-sensitive analog and RF ICs at nano nodes. Several novel non-traditional ESD protection structures were reported for future ICs at nano nodes. For example, [58] reports an above-IC graphene-based NEMS (gNEMS) switch ESD structure, heterogeneously integrated into a CMOS back-end using a post-CMOS process. The third example is a single-pole-double-throw (SPDT) RF switch circuit designed and fabricated in a foundry 45nm SOI CMOS that is protected by the above-Si gNEMS ESD switch made by a post-CMOS process. Figure 7-14(a) depicts the gNEMS ESD structure. The gNEMS ESD switch was fabricated in a post-CMOS process and characterized by TLP testing, as shown in Figure 7-14(b). The gNEMS ESD device remains OFF in normal IC operations. During an ESD event, the strong transient electrostatic force will pull down the suspended graphene membrane to touch the bottom electrode, hence quickly turns ON to discharge the ESD surge. The device behavior model was extracted for the gNEMS ESD device, which was verified by SPICE simulation using the extracted model as shown in Figure 7-14.

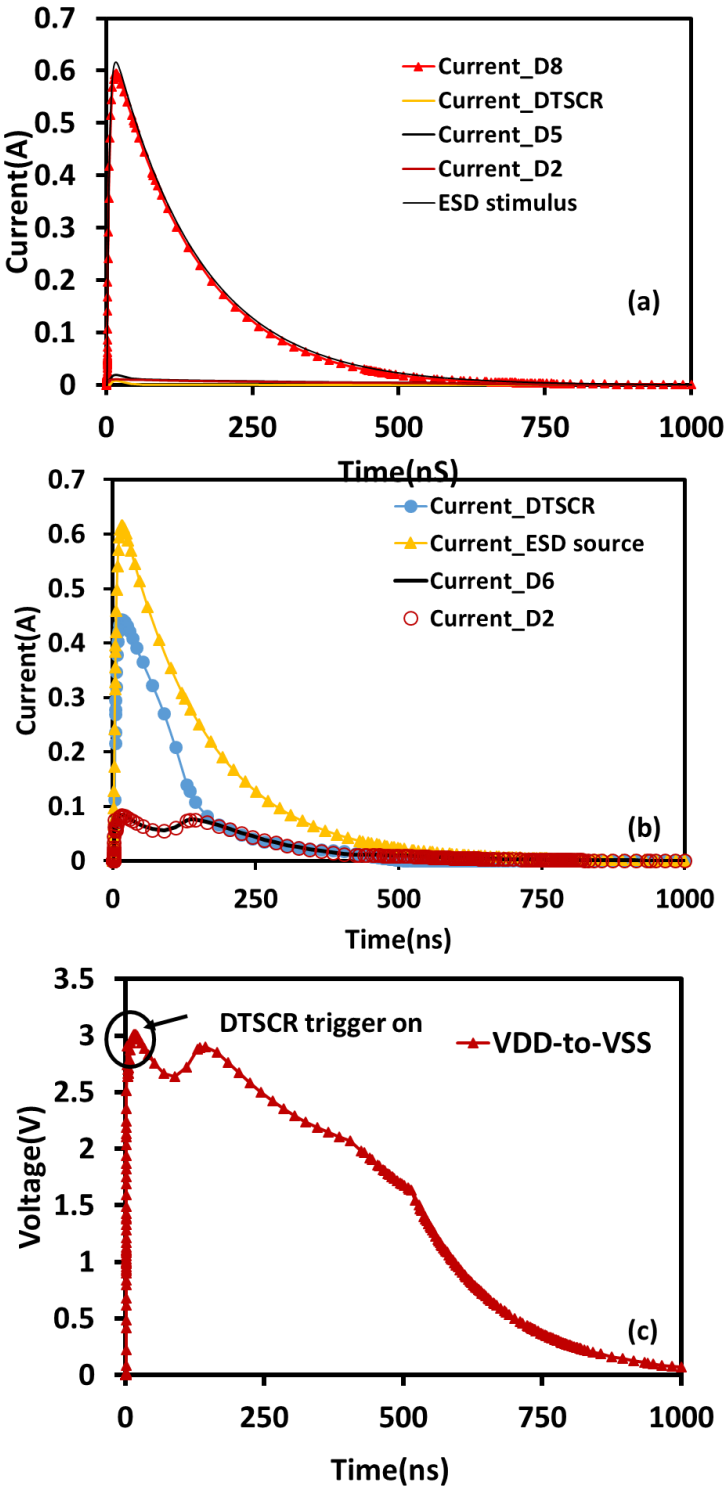


Figure 7-13 Simulated transient ESD discharging behaviors for two ESD zapping cases: (a) Input-to-V_{SS}, and (b) V_{DD}-to-V_{SS}.

Figure 7-15 shows a functional schematic for the SPDT circuit, designed as a LTE band switch between band4 and band25 with a maximum output power of +23dBm (V_{peak}=3.2V) and its output pin is protected by a gNEMS ESD device (V_{t1}~10V). SPDT uses a CMOS transistor stack to handle the output power that requires a total output-to-ground breakdown of BV~15V. Comprehensive circuit-level ESD simulation was conducted using the new ESD circuit method.

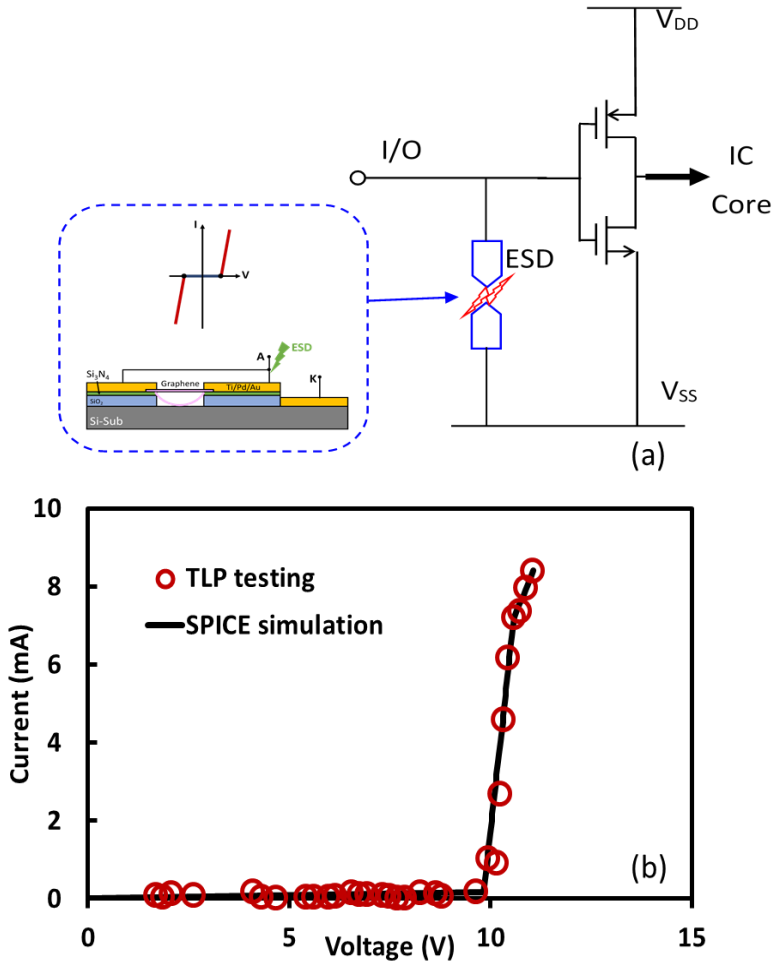


Figure 7-14 A non-traditional above-Si gNEMS ESD protection structure: (a) gNEMS cross-section and ESD circuit scenario, and (b) ESD discharging I-V curves by TLP testing and SPICE simulation using its behavior device model match each other well. TLP testing shows V_{t1}~10V and I_{t2}~8.4mA for the gNEMS ESD device.

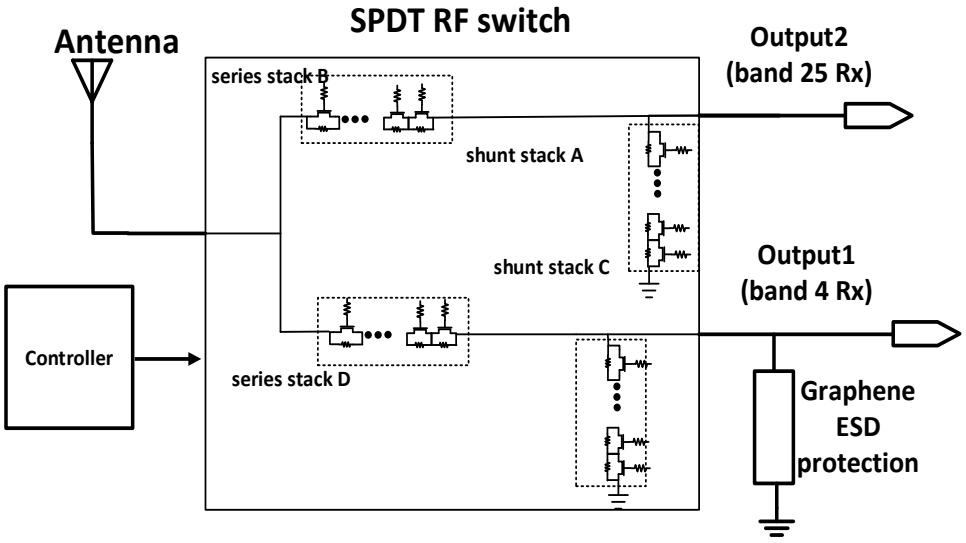


Figure 7-15 A functional schematic of SPDT RF antenna switch circuit made in 45nm SOI CMOS with a gNEMS ESD protection fabricated by post-CMOS processing.

Figure 7-16(a) depicts the simulated ESD discharging current distribution among different circuit components, showing that most ESD current is discharged through the shunt transistor stack, because they are large and have self ESD protection capability. Figure 7-16(b) shows that the transient node voltage peaks at above 30V, suggesting a potential ESD failure due to source-drain breakdown. While Figure 7-14 shows that the individual gNEMS ESD device works nicely under TLP testing, Figure 7-16 depicts that the gNEMS ESD device can only conduct small amount of the ESD surge at the chip level, which is attributed to its relatively large R_{ON} due to poor graphene contact. In summary, example-three shows that the new ESD circuit simulation method can handle non-traditional ESD protection structures as well, hence having a great potential for future ICs at nano nodes and featuring 3D heterogeneous integration.

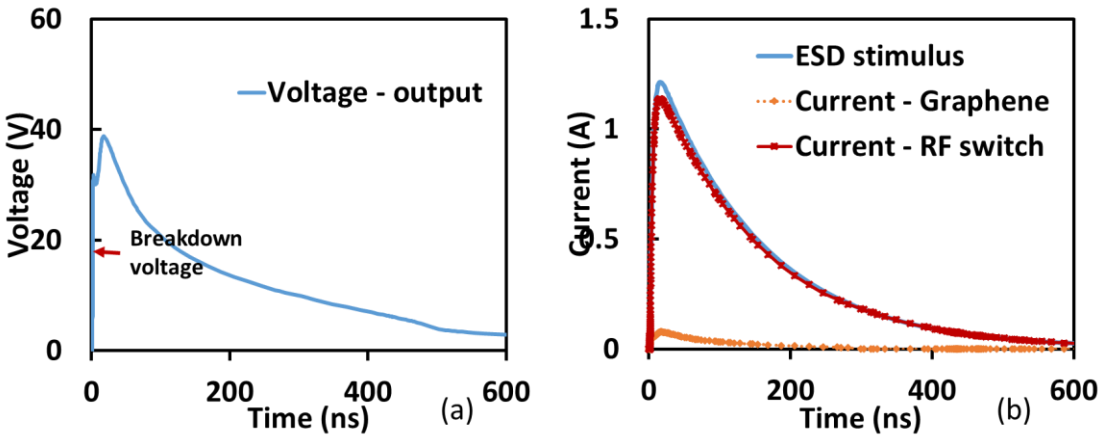


Figure 7-16 (a) Simulated ESD current distribution for the SPDT circuit with gNMES ESD protection at the output pin. (b) Simulated output voltage for the ESD-protected SPDT circuit peaks at above 30V due to poor R_{ON} of gNMES ESD device.

7.2.4. Multiple power domain ESD failure

For complex mixed-signal ICs having multiple power domains, ESD protection design is very challenging. Our new ESD circuit simulation method can be used to address this design problem easily. Figure 7-17 depicts an exemplary IC with multiple power domains, i.e., V_{DD1}, V_{SS1}, V_{DD2} and V_{SS2}. ESD zapping simulation was conducted by applying the ESD pulse to V_{DD2} pad. Due to noise coupling consideration, the two power domains are typically separated by a parasitic p-substrate resistance (Rsub). When a 1KV ESD pulse is applied to V_{DD2} with V_{SS1} grounded, Figure 7-17(b) shows that the transient voltage at the V_{DD2} pad is too high compared to the node breakdown voltage, hence, ESD failure occurs. As a solution, we added a bus-to-bus bidirectional diode between V_{SS1} and V_{SS2}. ESD circuit simulation shows that the transient voltage at the V_{DD2} pad was successfully clamped to a safe level lower than node breakdown voltage, ensures 1KV ESD protection.

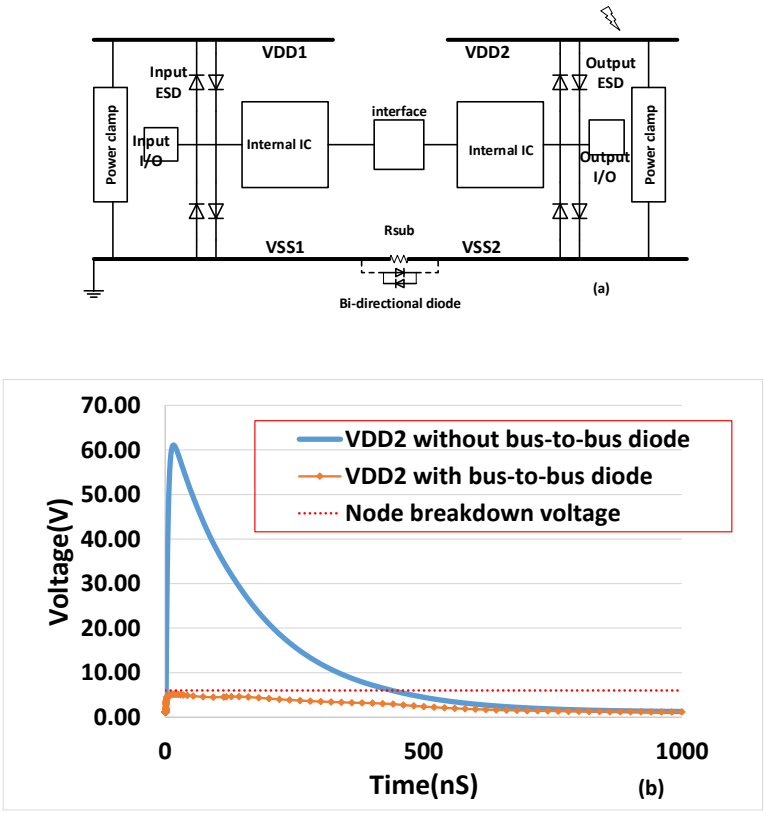


Figure 7-17 A multiple power domain IC with ESD protection: (a) ESD protection schematics, (b) simulated transient voltage at the V_{DD2} pad in comparison with the node breakdown voltage.

In this chapter, a new circuit-level ESD protection design simulation and analysis method using SPICE and ESD device behavior models is discussed. The developed methodology allows IC designers to conduct fast and accurate circuit-level ESD protection simulation. The unique capability of circuit-level ESD protection function simulation makes it possible to verify whole-chip ESD circuit designs, therefore ensures first-silicon design success. The new ESD circuit simulation method was fully validated using three ESD-protected ICs designed and fabricated in foundry 28nm CMOS and 45nm SOI CMOS technologies.

Chapter 8. Conclusion

Among 5G FR1 new radio bands, n77, n78 and n79 can provide the highest data throughput due to their wide bandwidth. For 5G FR2, 3GPP is driving mm-wave bands n257, n258 and n260. All these 6 bands are in TDD mode. Therefore, a T/Rx switch is required. In this work, a 3.5 GHz switch utilizing series-shunt topology is designed to cover 3-5GHz, the simulated performance is comparable with industrial product. However, simple series-shunt topology can hardly provide good performance on 28GHz range due to the off-branch leakage. In this work, SPDT travelling wave switch is designed and measured in 22nm FDSOI. The performance is comparable with state-of-art designs. ESD protection is added to protect the output port. However, due to the parasitic capacitance of ESD device, the RF performance degrades. ESD co-design is applied to improve the RF performance while maintaining an HBM 9KV ESD protection.

As technology evolving, short channel effect causes huge leakage. Therefore, FinFET and FDSOI are developed. These advanced technology nodes require high area efficiency ESD devices and robust ESD protection. Cell-by-cell SCR structure is designed and measured. The measurement result shows 1.5 times higher area efficiency than multi-finger SCR. Cell-by-cell DTSCR is further developed to lower the trigger voltage. To provide robust ESD protection across temperature, DTSCR is measured across a large temperature range. Its performance shows huge shift. Thus, we suggest careful characterize DTSCR temperature effect before utilizing in ESD protection design.

Beside ESD design, ESD simulation is also important. In this work, FinFET ESD design with 3D TCAD simulation flow is depicted. The TCAD simulation can provide guidance to device design. Full-chip ESD simulation methodology is developed and verified on a fabricated 28nm design. This simulation methodology can help ESD designer find ESD failure risks and optimize ESD protection circuit design.

For the future work and further improvement. First, distributed ESD protection for travelling wave switch should be considered to provide better co-design performance. FinFET ESD simulation flow can be further developed to include DTSCR and LVTSCR structures. Currently, the full-chip ESD protection simulation methodology can only support HBM ESD events. CDM events should be researched and a corresponding simulation methodology is desired.

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