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Demonstration of a Heterogeneously Integrated System-on-Wafer (SoW) Assembly

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***Abstract*—This paper describes the integration of a System-on-Wafer (SoW) assembly using test dielets mounted on a Silicon Interconnect Fabric (Si-IF) with an inter-dielet spacing of 100 µm and using 10 µm interconnect pitch. The continuity within and across the dielet assembly is shown using daisy chains of Au-capped Cu-Cu thermal compression bonds. The daisy chains run not only through every dielet but also across all the adjacently mounted dielets on the Si-IF. The interconnections exhibited an effective contact resistivity of 0.8-0.9 Ω-µm^2 and an average shear strength of 125 MPa. Our investigations showed that Argon plasma pre-treatment improves the shear strength of the metal bonds by a factor of 5X. Thermal simulation of the SoW assembly showed superior heat spreading across the assembly in a checkerboard configuration of alternate hot (0.5 W/mm^2) and cold (0.1 W/mm^2) dielets with an average temperature of 82 °C & 78 °C respectively.**

Keywords-component; System-on-Wafer, Thermal Compression Bonding, Silicon Interconnect Fabric, Heat dissipation

I. INTRODUCTION

The electronic system integration today relies on conventional assembly techniques, where packaged dies are mounted on a printed circuit board (PCB) using ball grid array (BGA) or pin grid array (PGA) type of interconnects, with pitches in the range of 400-1000 µm. Similarly, the die-to-laminate (or package) interconnects (C4 bumps) are realized in a flip chip fashion, where pitches are in the range of 150-250 µm [1]. The high package area – to – die area ratio results in large inter-dielet spacing (few mm) and consequently, the communication link lengths are larger than 10 mm. Furthermore, the data bandwidth is limited by the limited number of BGA connections on the board. Interposers can provide moderate interconnect densities (Pitch: ~45 µm), in the form of solder capped copper pillars. But this adds on an additional packaging level in the hierarchy and the cost of packaging inflates. In ECTC 2017, we have proposed a package-less dielet-to-Silicon Interconnect Fabric (Si-IF) assembly [2]. This scheme comprises of a single hierarchical packaging level, where interconnects are realized using a solderless metal-metal thermal compression bonding (TCB) process at 10 µm pitch and with an inter-dielets distance of 100 µm. We use a Simple Universal Parallel interface for Chips (SuperCHIPS) to achieve high data-bandwidth (> 8Tbps/mm), for communication between the dielets that uses simple inverter-based transceivers. [3]

II. TEST VEHICLES FOR SOW ASSEMBLY

The test dielets and Si-IF were fabricated using conventional back end-of-line (BEOL) processing. Si-IF samples were terminated with Cu pillars, planarized using a chemical mechanical planarization (CMP) process and further capped with an evaporated Au-layer. The details of the fabrication process are described in [2]. The SoW assembly was designed to accommodate integration of multiple test dielets of sizes i.e. 4, 9, 16, & 25 all in mm^2 on a 100 mm wafer with two damascene process metal layers. The integrated 371 chips on Si-IF covered an effective area of > 3100 mm^2 as shown in figure 1. The assembly is further passivated with a conformal Parylene-C coating, which can creep through micron scale crevices.

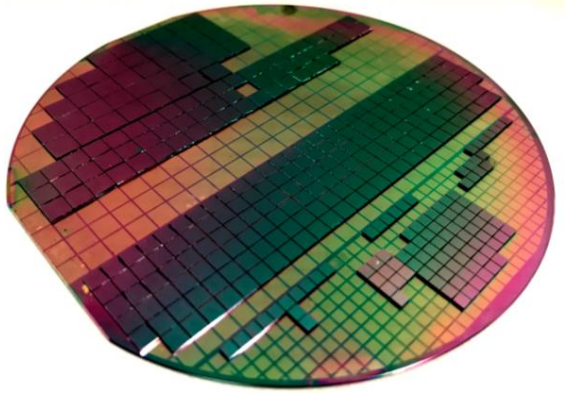

Figure1: Demonstration of a heterogeneously integrated assembly.

III. SILICON INTERCONNECT FABRIC

The Si-IF was designed in a way, where daisy chains in the assembly not only run through the dielet and Si-IF under the dielet area but also connect to the adjacent dielets through the links in the Si-IF as shown in figure 2 and 3. The micrograph in figure 4 shows the Si-IF with Au-capped pillars and adjacent links. The detailed fabrication process is described in [2].

The aim was to demonstrate the electrical continuity within the area of the dielet as well as across the adjacent dielets. The schematic of the test assembly is shown in the figure 3. The dielets were mounted on the Si-IF using a solderless direct metal-metal thermal compression bonding process using a K&S chip-to-wafer bonding machine (APAMA) [4]. The process parameters for

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TCB process are given in table 1. No post bonding annealing process was used after the TCB process.

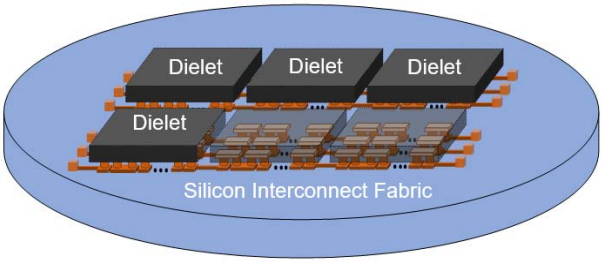

Figure 2: Schematic of the assembly with dielets mounted on the Si-IF to test the continuity within and across the adjacent dielets

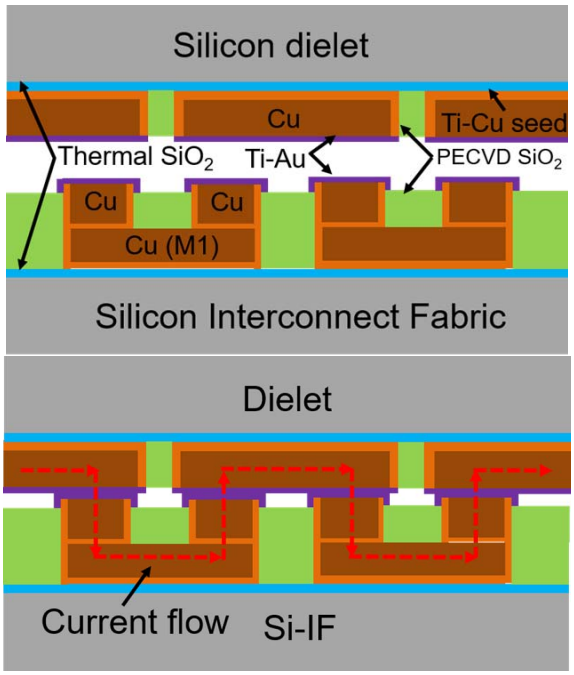

Figure 3: Schematic cross section of the TC bonded dielet on Si-IF shows the daisy chins

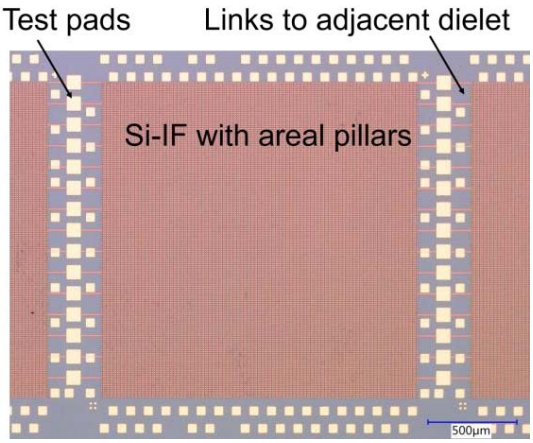

Figure 4: Si-IF shows areal pillars with the adjacent links to the neighboring dielets in the passivation layer.

TABLE I. PROCESS PARAMETES FOR THERMAL COMPRESSION BONDIGN

Process parameters	Values
Bondhead temperature	350 °C
Chuck temperature	150 °C
Bonding time	3 sec
Bonding pressure	100 MPa
Bonding environment	Air
Pre-bond treatment	Ar-plasma, 800 Watts, 3 min, 80 °C chuck.

IV. ELECTRICAL CHARACERIZATION

For electrical tests, an assembly consisting of 10 dielets with an area of 4 mm^2, a diameter of 5 µm Au-capped copper pillars, and an interconnect pitch of 10 µm were thermal compression bonded to Si-IF, as shown in figure 4, using the process parameters given in table 1.

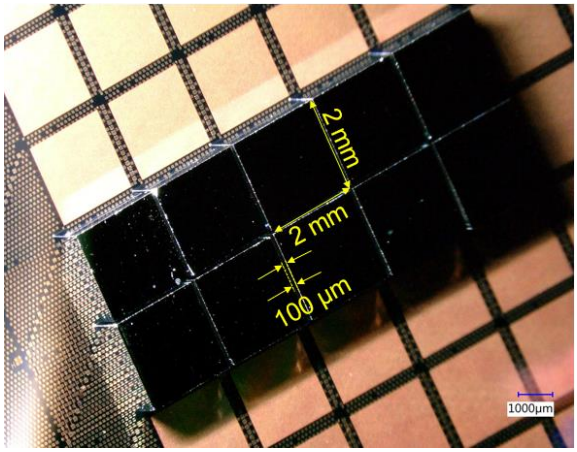

Figure 5: Micrograph of the assembly

Each row of serpentine, running through the dielet, consisted of 1960 TC bonded connections as depicted in figure 4.

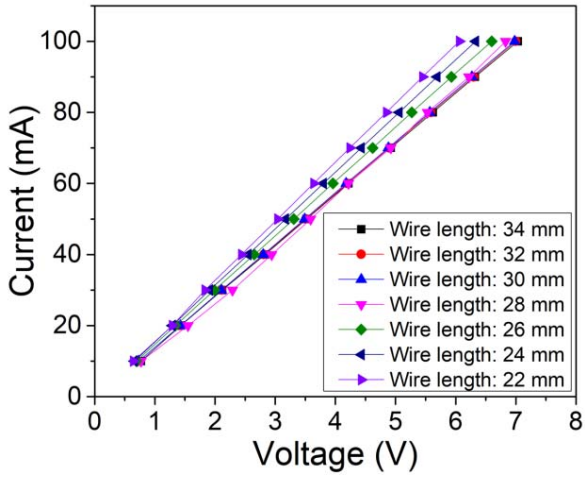

Figure 6: IV-characteristics of the daisy chains (both links & contacts.

With all 10 dielets connected in series, there were 19600 TC bonded connections in a single row. There were total of 180 such rows. Test pads were fabricated on the Si-IF to identify the faulty contacts within the entire edge of the dielets. The assembly exhibited 100 percent contact continuity yield across the dielets. Figure 5 shows the IV-characteristic of the serpentine including all the wires and contact resistance, while, figure 6 shows the resistance of serpentine across the connected assembly of 10 dielets.

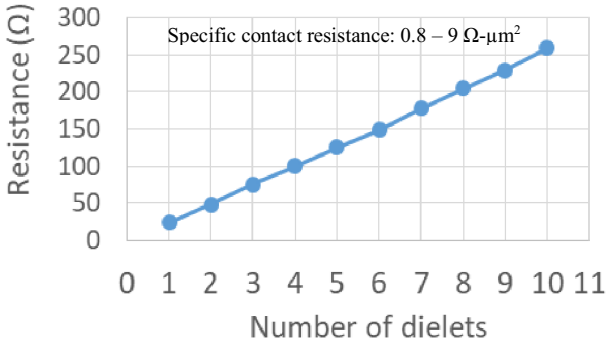

Figure 7: Resistance of a single serpentine across 10 dielets connected in series

The effective contact resistance of the contacts was found to be in the rage of 0.8 – 0.9 Ω-μm².

V. Mechanical Characterization

Without any pre-treatment of the Au-capped surface, the average shear strength of the contact was found to be around 25 MPa for a sample set of 20. Various surface treatments were used to clean the gold surface including oxygen and argon plasma pre-treatment. The plasma treatments were applied prior to the bonding process and the time gap between the treatment and the actual thermal compression bonding was around 10-15 min.

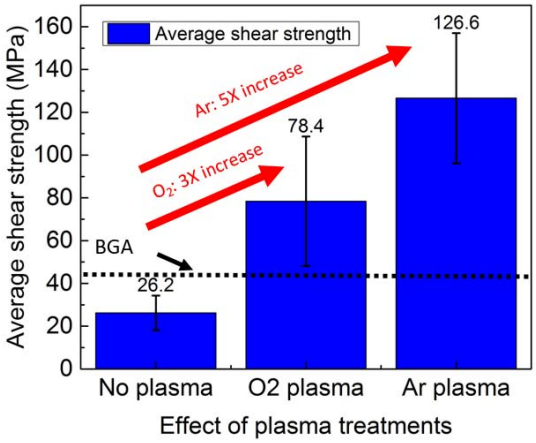

Figure 8: Effect of plasma treatments on the shear strength of the contacts.

It was found that both oxygen and argon plasma treatments improve the adhesion strength of the bonds. The average shear strength of the oxygen plasma treated gold surfaces i.e. both Au-capped pillar and Au-capped pad, improved by 3X, while, it improved by 5X with argon plasma treatment. The argon plasma not only cleans the gold surface but also creates surface activation in the form of dangling bonds [5]. Figure 7 shows the effect of plasma treatments on the shear strength of the contact. The cross-section of Au-capped Cu pillar and Au-capped Cu pad is shown in figure 9. Au is a relatively compliant metal and free of any native oxide. This allows intimate contact at the interface of the mating surfaces during thermal compression bonding [6].

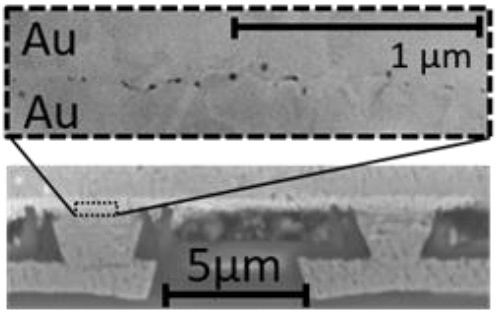

Figure 9: Cross section of Au-capped copper pillar to Au-capped copper pad contact

VI. Thermal Modeling Of Dielet Integration on Si-IF

Increasing packaging density makes thermal issues quite challenging, as the heat density increases, and the area to spread this heat out and sink it reduces. It has been a significant barrier to the proliferation of 3-D integration beyond low-power memory stacks. In conventional packages, heat is extracted from the top of the die through a heat-spreader and a heat sink that may be air or water cooled. Very little heat (~10%) is extracted from the bottom of the die, due to the poor thermal conductivity of the organic laminate. In contrast, the Si-IF presents a richer thermal scenario where heat may be extracted from either side.

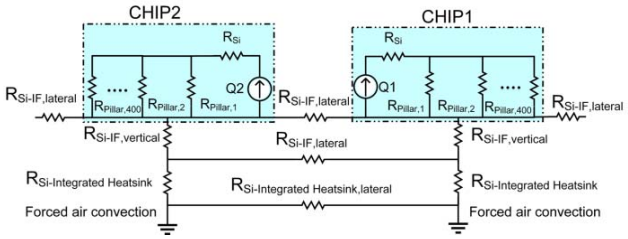

Figure 10 : Equivalent thermal resistance model of the dielets assembled on the Si-IF with 100 μm inter-dielet spacing with integrated Si micro-machined heatsink

We consider a high-power die (0.5 W/mm²) and a low-power die (0.1 W/mm²) assembled in three configurations: all high-power dies, all low-power dies, and a checkerboard configuration. Fig. 10 shows the equivalent thermal circuit used in this analysis. The Si-IF behaves as an integrated heat spreader because of high thermal conductivity of Si and a

fin structure is micro-machined on the backside of the Si-IF. Note that heat can be transferred laterally from a hot die to a cold die through the Si-IF. No heat sink is used on the top of the dies. A convective coefficient of 1000 W/m^{2}K, typical of forced air cooling was used. The heat is assumed to enter the Si-IF only through the interconnects. There is no thermal interface material used.

The superior thermal properties of the Si-IF are apparent from Fig. 11. The worst case is when all the dies are operating at high power at all times. In steady state, all the dies are around 120 ºC and a few degrees cooler near the edge. In the checker board case, the temperature is significantly lower but once again all the dies (including the low-power dies) reach the same temperature of about 80 ºC. This is because of the isothermal nature of the Si-IF heat sink. Fig. 12 shows the temperatures of the hot and cold die as a function of the convective heat transfer coefficient showing that forced air cooling is an adequate approach to heat sink even a large SoW.

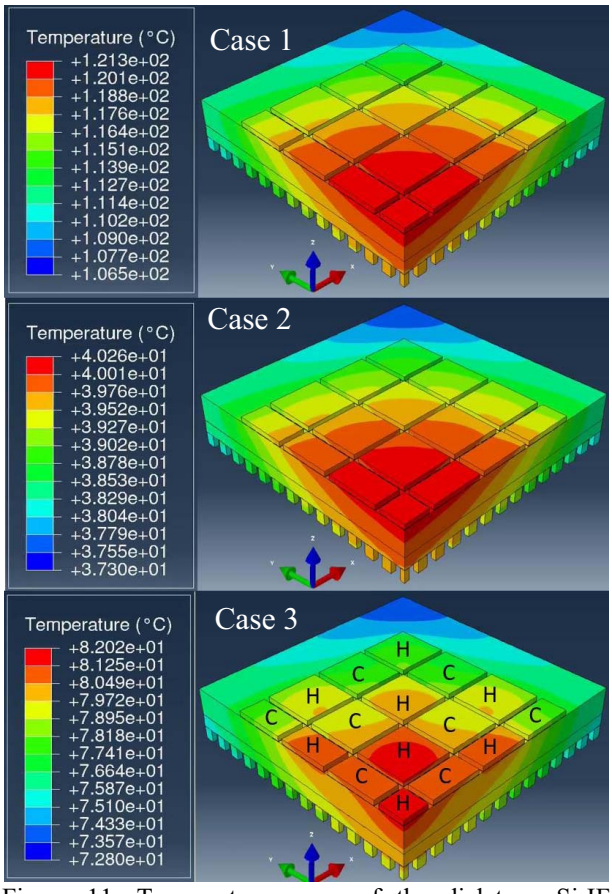

Figure 11: Temperature maps of the dielets-on-Si-IF assembles.

(a) Case 1: All dielets assembled on Si-IF are operating at 0.5 W/mm^2 power density (Hot dies).

(a) Case 2: All dielets assembled on Si-IF are operating at 0.1 W/mm^2 power density (Cold dies).

(c) Case 3: The dielets are assembled on Si-IF in a checkerboard configuration with alternative hot (H: 0.5 W/mm^2) and cold (C: 0.1 W/mm^2) dielets.

This preliminary study shows that the use of an all silicon package has significant thermal advantages –leverage the Si-IF as an efficient heat spreader, integrated micro-machined heat sinks, elimination of thermal interface material as the heat is transferred through the Cu interconnects from the die to the Si-IF (and not through solder intermetallics and organic under fill). Die side heat sinks and the use of more elaborate cooling systems such as micro-machined fluidic channels and heat pipes will greatly expand the heat dissipation capabilities.

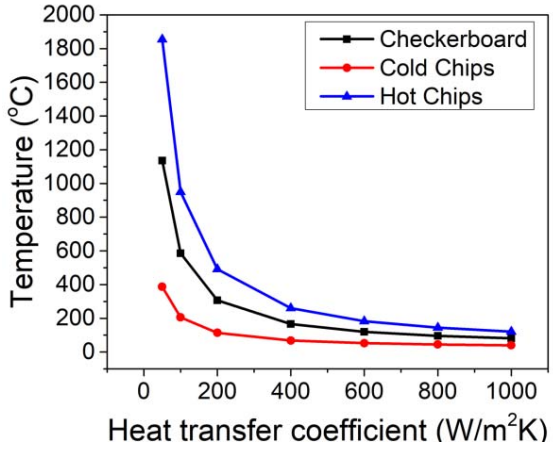

Figure 12: : Maximum temperatures profiles of the dies assembled on Si-IF for three operational cases: all hot (blue), all cold (red) and checkerboard configuration

VII. Conclusions

An SoW assembly is demonstrated using test dielets and a silicon interconnect fabric. The chip-to-wafer interconnects are realized using a solderless metal-metal thermal compression bonding process. The TC bonded contacts (Ø = 5 µm & P = 10 µm) exhibited 100% contact yield across the assembly of ten dielets, within the individual dielets as well as across the adjacently connected dies. Based on the current results, we can confidently state that the reliable contacts can be extended over the entire wafer. Note, that a real system will always contain redundancy to accommodate an unforeseen failure. Plasma treatment significantly improves the adhesion of the metal bonds. Therefore, the shear strength of the joints increases by 5X in comparison with untreated samples. The shear strength of the metal bonds (150 MPa) is 3X larger than the strength of the BGA and C4 type connections. The SoW assembly mainly consists of "Silicon" material, which has very high thermal conductivity (150 W/mK). FEM simulations reveal that superior heat spreading properties of silicon allows integration of hot (0.5 W/mm^2) and cold (0.1 W/mm^2) on a Si-IF at 100 µm inter-dielet spacing with uniform heat spreading, and without increasing the maximum temperature

beyond 85 °C. We can confidently state that SoW assembly will allow heterogeneous reliable integration of dielets (semiconductor base, sizes, etc.) with high interconnect density ($4 \text{ X } 10^6 \text{ cm}^2$), low interconnect resistivity ($0.8 - 9\ \Omega\text{-}\mu\text{m}^2$, close inter-dielet spacing ($\leq 100\ \mu\text{m}$), high adhesion strength (150 MPa), and with more uniform heat spreading.

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