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Title
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Permalink
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Journal
IEEE Electron Device Letters, 25(4)

ISSN
0741-3106

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Publication Date
2004-04-01

Peer reviewed

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High Breakdown Voltage AlGaN–GaN HEMTs Achieved by Multiple Field Plates

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***Abstract*—High-voltage $Al_{0.22}Ga_{0.78}N$–GaN high-electron mobility transistors have been fabricated using multiple field plates over dielectric passivation layers. The device breakdown voltage was found to increase with the addition of the field plates. With two field plates, the device showed a breakdown voltage as high as 900 V. This technique is easy to apply, based on the standard planar transistor fabrication, and especially attractive for the power switching applications.**

***Index Terms*—Breakdown voltage, field-effect transistors (FETs), field plates, high-electron mobility transistors (HEMTs), passivation, power electronics.**

I. Introduction

SOLID-STATE devices have played an important role in power applications. Following the success of GaAs-based field-effect transistors (FETs) for millimeter-wave power applications, GaN-based FETs have successfully demonstrated unprecedented potential in radio frequency (RF) power and power electronics applications, featuring both high saturation current, and high breakdown voltage [1]–[3]. To improve device performance, efficiency, and stability one needs to increase the gate–drain reverse breakdown voltage and, simultaneously, eliminate RF dispersion [4].

Various technologies have been developed in the more mature GaAs material system to increase the breakdown voltage, including insulated gate [5], recessed gate [6], [7], overlapping gate [8], field plate (FP) over a stepped insulator [9], and field-modulating plate over an insulator [10]. Similar techniques are under development in GaN-based transistors, demonstrating good results. For AlGaN–GaN high-electron mobility transistors (HEMTs), Zhang *et al.* employed double-layer gate dielectrics [11] to minimize both dispersion and gate leakage, and they obtained a breakdown voltage higher than 1 kV. They also used an overlapping gate [12] and demonstrated HEMTs with a breakdown voltage higher than 570 V. Karmalkar *et al.*[13] showed by simulations that a FP over a stepped insulator is superior to an overlapping gate scheme, and a breakdown voltage as high as 1900 V was predicted. Takada *et al.* [14] demonstrated 600-V HEMTs by fabricating a FP electrically connected to the source electrode. Recently, Chini *et al.* [15], [19], fabricated AlGaN–GaN HEMTs with very high power density at 4 GHz (12 W/mm on sapphire and 18.8 W/mm on SiC) by employing a field-modulating plate over a passivation dielectric layer.

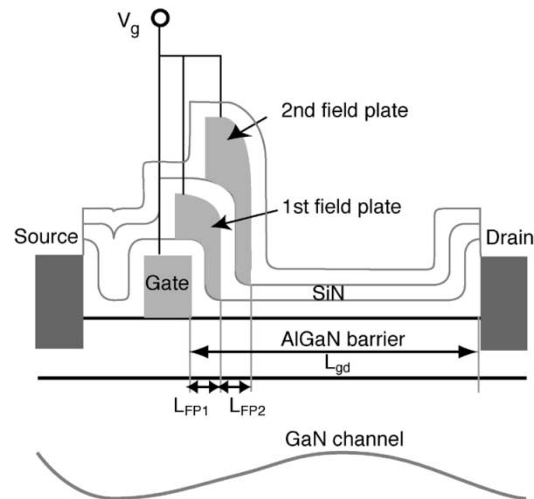

Fig. 1. Schematic of AlGaN–GaN HEMTs with surface passivation and two field plates connected to the gate at the gate pads (not shown), exhibiting a high breakdown voltage with no dispersion.

In this letter, we report a simple technique of multiple FPs over insulators to be very effective in increasing the device breakdown voltage with no dispersion. With this technique, we demonstrate AlGaN–GaN HEMTs with a breakdown voltage of up to 900 V.

II. Device Fabrication and Measurement

The AlGaN–GaN HEMTs were grown by metal–organic chemical vapor deposition (MOCVD) on c-plane sapphire substrates. The semi-insulating buffer consists of a 0.7-μm-thick GaN:Fe and 50-nm AlN followed by 1.8-μm unintentionally doped GaN. The top $Al_{0.22}Ga_{0.78}N$ barrier is 29-nm-thick and doped with Si. It is also capped with 4-nm SiN to reduce gate leakage [16]. Hall effect measurements at room temperature show a channel carrier concentration of 8.59×10^{12} cm^{-2} with a mobility of 1310 cm^{2}V^{-1}s^{-1}.

Our AlGaN–GaN HEMTs employ the T-shape gate layout with a gate width of 2 × 25 μm. The gate length is 1.5 μm and the gate–drain spacing L_{gd} varies from 4 to 28 μm. The schematic cross section of the completed device is shown in Fig. 1. First, Ti–Al–Ni–Au ohmic metals were deposited and annealed at 870 °C, followed by the mesa formation using Cl_2 reactive ion etch. Ni–Au was deposited for the gate Schottky electrode. Devices were then tested using a curve tracer. They were found to have RF dispersion, and the three terminal breakdown voltage increases with the increasing gate–drain

Manuscript received October 22, 2003; revised December 27, 2003. This work was supported by Office of Naval Research (ONR) under a grant monitored by H. Dietrich. The review of this letter was arranged by T. Mizutani.

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Digital Object Identifier 10.1109/LED.2004.824845

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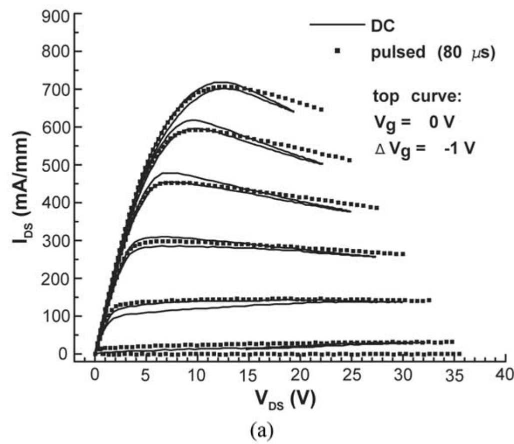
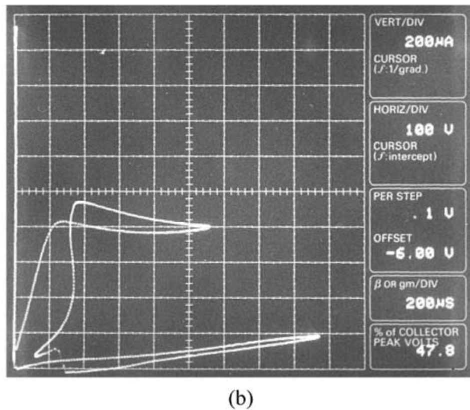


(a)



(b)

Fig. 2. (a) *I–V* characteristics of $Al_{0.22}Ga_{0.78}N$–GaN HEMTs with our standard SiN passivation at dc and pulsed condition, showing a current density of 700 mA/mm with no dispersion. (b) $Al_{0.22}Ga_{0.78}N$ –GaN HEMTs with two FPs exhibiting a breakdown voltage of ~900 V.

spacing. For $L_{\rm gd} = 24$ μm, the device breakdown voltage was between 350–400 V. This breakdown voltage decreased to about 250 V after our standard surface passivation, performed by depositing approximately 180-nm SiN by plasma-enhanced chemical vapor deposition (PECVD). The current–voltage (*I–V*) characteristics at dc and 80 μs pulsed measurements are plotted in Fig. 2(a). The devices showed high current densities (>700 mA/mm) with no dispersion at the measured frequency. After patterning openings over the electrode pad areas, the first FP was formed by depositing a 1.5 μm Ni–Au gate line on top of the passivation layer using the same gate layer mask. The FP is connected to the gate at the gate pad. The overlap of these two metal lines is about 0.8–1 μm, i.e., $L_{\rm FP1} = 0.5 - 0.7$ μm. $L_{\rm FP1}$ is the length of the first FP, as shown in Fig. 1. Another roughly 180-nm-thick SiN layer was then deposited by PECVD. A substantial increase in breakdown voltage was observed. For $L_{\rm gd} = 24$ μm, devices exhibited a breakdown voltage of 600–700 V. Repeating the same process, the second FP was formed by depositing another 1.5-μm Ni–Au gate line on top of the SiN layer. It was shifted toward the drain side by another 0.5–0.7 μm, i.e., $L_{\rm FP2} =$ 0.5–0.7 μm. After another 180-nm SiN was deposited by PECVD, we found the device breakdown voltage increased further. For $L_{\rm gd} = 24$ μm, the device hard breakdown voltage increased up to 900 V, as shown in Fig. 2(b). There is no change observed in device dc *I–V* characteristics. The measured three-terminal breakdown

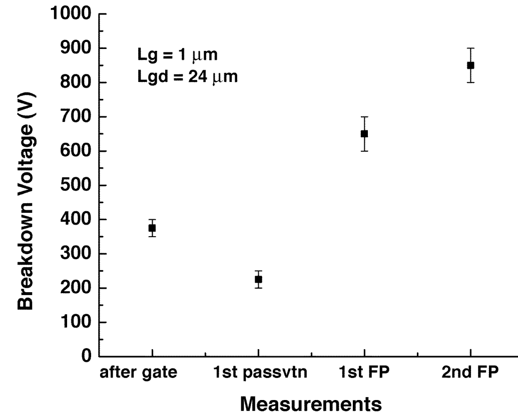


Fig. 3. Trend of the $Al_{0.22}Ga_{0.78}N$/GaN HEMT breakdown voltage with respect to the processing stages.

voltages at various processing stages are shown in Fig. 3. The continuous improvement in the breakdown voltage can be ascribed to the reduction of electrical field strength around the gate area on the drain side due to the addition of FPs. Examination of devices with more than two-stage FPs and their effects on high-frequency performance is underway.

III. Discussion

It is believed that gate breakdown occurs at the drain-side edge of the gate electrode due to the huge electric field spike under normal operating conditions [4], via avalanche breakdown and thermally assisted tunneling [17]. The RF dispersion originates from surface states [11], [18]. In the presence of dispersion, the surface traps are negatively charged at pinchoff, therefore, the effective gate length increases and the electrical field under the gate on the drain side is much reduced. Due to the mitigation of electrical field crowding, devices generally show very high breakdown voltage (>350 V). But they also show large dispersion owing to the slow response of the surface traps. When the dispersion is removed by surface passivation, the electrical field under the gate on the drain side drastically increases. This extremely large electrical field spike can cause local Schottky-barrier breakdown at a much lower applied drain voltage. For a functioning device employed either in solid-state amplifiers or power switching applications, dispersion has to be eliminated. Thus, electric field engineering in proximity of the gate is necessary to improve the device performance.

In terms of electric field shaping, the FP technique offers additional advantages compared with insulated-gate technique. Inserting an insulating layer, which is carefully chosen to keep the interfacial state densities low, under the gate electrode is effective in reducing the gate leakage. However, it does not alleviate electrical field crowding at the drain-side of the gate edge. As both the simulations and experiments have demonstrated, the FP technique is effective in extending the drain depletion region and replacing a single-peak electric field with $n+1$ peaks with much reduced electric field strength (n is the number of FPs) [13]. The technique, multiple FPs over passivation dielectric layers, presented in this paper uses simple and typically well-controlled processing steps. Since there is no need to pattern dielectrics over the active device region, the active device

is protected from possible damages induced in the subsequent processing steps. This technique should be readily applied to other planar FETs as well. Since the multiple FPs are expected to cause some high-frequency performance degradation owing to the increase in gate capacitance, it is especially attractive for power electronics applications below 1-GHz range.

IV. Conclusion

We report a simple technique using multiple FPs to increase the device breakdown voltage of planar transistors. $Al_{0.22}Ga_{0.78}N$–GaN high breakdown voltage HEMTs were fabricated using this technique. An increase of the breakdown voltage was observed with the addition of a FP. With two FPs over the passivation dielectric layers, a breakdown voltage as high as 900 V was observed, compared with a breakdown voltage of 250 V of the standard passivated devices with no FPs. This technique offers an efficient and easy solution to improve device breakdown voltage based on the standard planar transistor fabrication.

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