Title

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***Abstract*—The Flying Capacitor Multi-Level (FCML) converter is heralded as enabling the utilization of low-voltage switches within a high-voltage converter by evenly distributing the voltage stress on a series string of switches through the use of "flying" capacitors. However, this advantage of the converter requires that the flying capacitors do not deviate too far from their ideal voltage distribution regardless of transients, load disturbances, or other parasitics to ensure the switches are not overvolted among other concerns. Previous works have identified certain theoretic combinations of duty cycle and level count where the flying capacitor voltages do not naturally balance and instead diverge. Although seemingly problematic, in practice this behavior is not observed in practical implementations. To resolve this discrepancy between FCML theory and experiment, we analyze the impact of switch output capacitance on the flying capacitor voltage balancing dynamics, and illustrate this capacitance has a naturally balancing effect.**

I. Flying Capacitor Multilevel Converter Balancing Mechanisms and Unbalanced Conversion Ratios

Power converters in applications such as traction and propulsion drives, and data center power delivery require high power density and efficiency. In pursuit of maximizing these objectives, the Flying Capacitor Multi-Level (FCML) converter has emerged as a promising topology for these cutting edge applications [1], [2]. Although the topology was initially developed to remedy the lack of high voltage switches rated for the input voltage in high voltage power conversion applications [3], it is able to outperform conventional topologies in lower voltage applications where even though a monolithic switch may be available, the series combination of multiple lower voltage switches is found to be higher performance [4]. A simplified schematic of a 5-level FCML converter is presented in Fig. 1.

The promise of the topology to enable a series stacking of switches with an even voltage stress distribution requires the flying capacitors within the converter to not deviate too far from the ideal voltage distribution. If this constraint is violated, the system efficiency will decrease and in the worst case, the switches will be exposed to a voltage higher than their ratings, yielding converter failure. Previous works [5]–[8] have analyzed the mechanisms by which the flying capacitors within an FCML converter converge to their steady state voltage

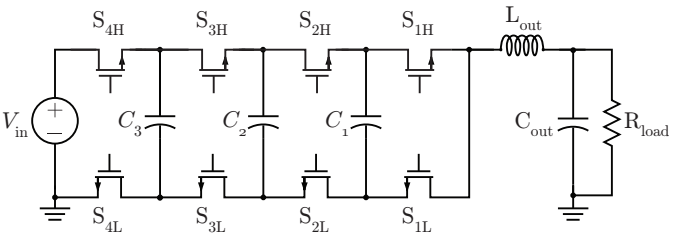

Fig. 1: Simplified 5-Level FCML converter schematic.

distribution $v_{C_i} = i \cdot \frac{V_{\text{in}}}{N-1}$ where N is the number of discrete levels in the switch node waveform, and i ranges from 1 to $N-2$, as shown in Fig. 1. Work in [3] demonstrated that with symmetric Phase-Shifted PWM (PS-PWM) modulation, the flying capacitor voltages will dynamically balance to the aforementioned voltage distribution and if the high-side switches $S_{x\text{H}}$ are operated with a duty cycle D, and the low-side $S_{x\text{L}}$ switches in a complementary fashion, the output voltage will be $V_{\text{out}} = D\,V_{\text{in}}$.

Several works [5]–[7], [9] have discovered "unbalanced" conversion ratios, at which the flying capacitors theoretically do not passively balance to their desired steady-state values and instead diverge[1]. Of note, however, is that these theoretically unbalanced operating points and divergent flying capacitor voltages are not typically observed in experimental hardware [5], pointing to a gap in our understanding of all pertinent balancing mechanisms within the converter. This work analyzes the natural balancing of the capacitor voltages in a FCML converter, and extends past work to also include the impact of switch output capacitance. Crucially, it is discovered that the transient charge flow between flying capacitors and parasitic switch capacitance during switch transitions has a naturally balancing effect, which has previously not been documented. A detailed state-space model is developed to include this balancing mechanism, and through hardware validation, it is shown that the proposed model accurately captures the experimental behavior, which was not achieved

[1]These "unbalanced" conversion ratios are defined by conversion ratios where $D \cdot (N-1)$ and $(N-1)$ are not co-prime, where D is the duty cycle of the FCML operated with symmetric PS-PWM and $D \cdot (N-1)$ is an integer.

in previous models. Of particular interest in this work is the combination of a $N = 5$ level FCML converter and a duty cycle of $D = 50\%$ as it is the simplest FCML converter which exhibits this theoretical behavior. This work has two key contributions: 1) Identification of the role of the switch output capacitance in the natural balancing of the flying capacitor voltages, along with an analytical expression of the strength of the balancing mechanism. 2) Development of an analytical model incorporating said balancing mechanism, which shows excellent agreement with experimental results. Together, these two contributions yield - for the first time - a model of FCML converter natural balancing that matches experimental observations during practical operating conditions (e.g., high current, transients).

II. Switch Output Capacitance (C_{oss}) Impact on Flying Capacitor Natural Balancing

To resolve the discrepancy between previous literature and experimental evidence, there must exist some mechanism not included in the aforementioned works' simplified model of the FCML converter which acts to drive the flying capacitors to their balanced state, even at "unbalanced" conversion ratios. One such mechanism not previously modeled is charge redistribution induced by the switch parasitic output capacitance which drives the flying capacitors to a balanced state. During each switching event, the output capacitance C_{oss} of a switch which was previously on is charged from $v_{DS} \approx 0$ V to a linear combination of the flying capacitor voltages and input voltage. For example, in Fig. 2, $C_{oss,\mathrm{H}}$ is charged from $v_{\mathrm{H}} = 0$ to $v_{\mathrm{H}} = v_{C_2} - v_{C_1}$ when $S_{2\mathrm{H}}$ switches from ON to OFF and $S_{2\mathrm{L}}$ switches from OFF to ON. Similarly, $S_{1\mathrm{H}}$ in Fig. 1 will have its C_{oss} charged from 0 to v_{C_1} when it switches from ON to OFF. As will be shown in subsequent analysis, these previously unmodeled charge flows due to C_{oss} are functions of the flying capacitor voltages, and provide an inherent balancing mechanism.

A. Charge Flow Analysis

To provide a tractable analytical result of this charge flow mechanism, we make the following simplifying assumptions: 1) all switches are commuted with zero dead-time and in perfect complementary fashion, and 2) the flying capacitors and C_{oss} parasitic capacitances are linear. Examining the switching event illustrated in Fig. 2, at $t = 0$, $S_{2\mathrm{H}}$ opens and $S_{2\mathrm{L}}$ closes. Denoting t_{final} the time at which the system voltages have approximately settled:

$$\begin{aligned} Q_{\text{flow}} = C_{oss,\mathrm{H}} \Delta v_{\mathrm{H}} &= C_{oss,\mathrm{H}} \cdot \big(v_{\mathrm{H}}(t_{\text{final}}) - v_{\mathrm{H}}(0)\big) \\ &\approx C_{oss,\mathrm{H}} \cdot \big(v_{C2}(t_{\text{final}}) - v_{C1}(t_{\text{final}})\big) \end{aligned} \quad (1)$$

In this process, Q_{flow} leaves C_2 and is deposited on C_1. Given the charge flowing within the circuit (as a function of the flying capacitor voltages at the end of a commutation event), we can solve for the flying capacitor voltages after a commutation event has occurred as a function of the flying capacitor voltages before a commutation event.

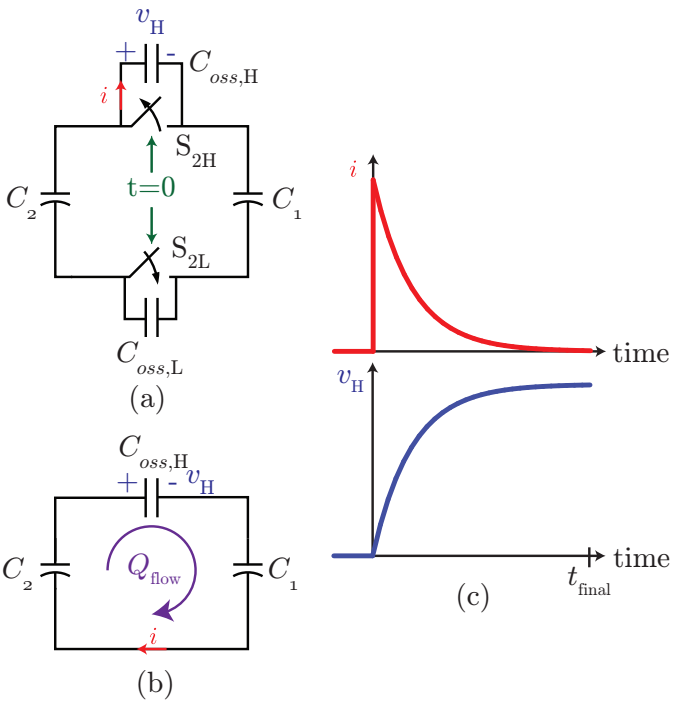

Fig. 2: (a) Switching cell 2 from Fig. 1 with switch output capacitances C_{oss} explicitly drawn. At $t = 0$ a commutation of the S_2 switching cell occurs, with S_{2H} turning OFF and S_{2L} turning ON. (b) Equivalent circuit after $t = 0$ for analyzing commutation charge flow. Q_{flow} circulates around the commutation loop, discharging C_2 and charging C_1 and $C_{oss,\mathrm{H}}$. (c) Current and voltage waveforms through $C_{oss,\mathrm{H}}$ after the commutation event at $t = 0$. Parasitic resistances are omitted for clarity.

$$\begin{aligned} v_{C2}(t_{\text{final}}) &= v_{C2}(0) - \frac{Q_{\text{flow}}}{C_2} \\ &= v_{C2}(0) - \frac{C_{oss,\mathrm{H}}}{C_2} \cdot \big(v_{C2}(t_{\text{final}}) - v_{C1}(t_{\text{final}})\big) \end{aligned} \quad (2)$$

$$\begin{aligned} v_{C1}(t_{\text{final}}) &= v_{C1}(0) + \frac{C_{oss,\mathrm{H}}}{C_1} \cdot \big(v_{C2}(t_{\text{final}}) - v_{C1}(t_{\text{final}})\big) \\ &= \frac{v_{C1}(0) \cdot (C_1 C_2 + C_1 C_{oss,\mathrm{H}}) + C_2 C_{oss,\mathrm{H}} v_{C2}(0)}{C_1 C_2 + C_{oss,\mathrm{H}} (C_1 + C_2)} \end{aligned} \quad (3)$$

Under the assumption of zero dead-time, both high-to-low switch transitions and low-to-high switch transitions experience the same charge flow. Table I summarizes each flying capacitor voltage after a commutation event occurs. These approximations assume that the commutation events are "local", that is only the flying capacitors connected to a commutating switching cell participate in C_{oss} charge redistribution. Additionally, if two cells commutate at the same time, the voltage at the end of the event can be approximated by a cascade of two separate switching events.

B. Analytical FCML Model Incorporating C_{oss} Induced Charge Flow

Given that the C_{oss} induced voltage changes per commutation event are very small compared to the average values

TABLE I
TABULATED ANALYTICAL SOLUTIONS TO THE FLYING CAPACITOR VOLTAGES AFTER A COMMUTATION EVENT OCCURS FOR N=5. DUE TO THE RELATIVELY SHORT DURATION OF COMMUTATION, THE VOLTAGE ON THE FLYING CAPACITORS APPEAR TO IMPULSIVELY CHANGE AS THE C_{OSS} ARE HARD CHARGED.

Switching Cell Event (on or off)	Flying capacitor voltage after commutation
S_1	$v_{C1}[i+1] = v_{C1}[i] - \frac{C_{oss}}{C_1+C_{oss}} v_{C1}[i]$
S_2	$v_{C1}[i+1] = v_{C1}[i] + \frac{C_2 C_{oss}}{C_1C_2+C_{oss}\,(C_1+C_2)}(v_{C2}[i] - v_{C1}[i])$ $v_{C2}[i+1] = v_{C2}[i] + \frac{C_1 C_{oss}}{C_1C_2+C_{oss}\,(C_1+C_2)}(v_{C1}[i] - v_{C2}[i])$
S_3	$v_{C2}[i+1] = v_{C2}[i] + \frac{C_3 C_{oss}}{C_2C_3+C_{oss}\,(C_2+C_3)}(v_{C3}[i] - v_{C2}[i])$ $v_{C3}[i+1] = v_{C3}[i] + \frac{C_2 C_{oss}}{C_2C_3+C_{oss}\,(C_2+C_3)}(v_{C2}[i] - v_{C3}[i])$
S_4	$v_{C3}[i+1] = v_{C3}[i]\left(1 - \frac{C_{oss}}{C_3+C_{oss}}\right) + \frac{C_{oss}}{C_3+C_{oss}} V_{\text{in}}$

of the flying capacitor voltages, it is difficult to ascertain a priori whether the flying capacitors will settle to a balanced state and if they do, how quickly it takes transients to settle. To investigate, a MATLAB script was developed to solve the state variables within the circuit as a function of time. To analytically simulate the circuit, each switching configuration is associated with a set of state space matrices. As an example, consider the symmetric PS-PWM switch configuration to generate an approximate switch node voltage of $\frac{V_{\text{in}}}{2}$ with switches $S_{1\text{H}}$, $S_{2\text{L}}$, $S_{3\text{L}}$, and $S_{4\text{H}}$ ON while complementary switches are OFF. This sub-circuit configuration is illustrated in Fig. 3. By inspection, the state space description of this sub-circuit is:

$$\begin{bmatrix} C_1 & 0 & 0 & 0 & 0 \\ 0 & C_2 & 0 & 0 & 0 \\ 0 & 0 & C_3 & 0 & 0 \\ 0 & 0 & 0 & L_o & 0 \\ 0 & 0 & 0 & 0 & C_{\text{out}} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ i_L \\ v_{\text{out}} \end{bmatrix} = \mathbf{A} \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ i_L \\ v_{\text{out}} \end{bmatrix} + \mathbf{B} V_{\text{in}} \tag{4}$$

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & -1 & -R_L & -1 \\ 0 & 0 & 0 & 1 & -\frac{1}{R_{\text{load}}} \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \\ 0 \end{bmatrix} \tag{5}$$

Where R_L is the sum of series resistances within the sub-circuit comprising e.g., inductor resistance, switch on-state resistance, flying capacitor ESR, etc.

The state variables at the end of a switching state are then found by solving the state evolution equation $\dot{x}(t) = \mathbf{A}\,x(t) + \mathbf{B}\,u(t)$ as a function of the state variables at the beginning of a switching state[2]. To save memory and computational load, the state variables are only solved at each switching instance, thus the time steps of the solver are the same as those of the switching instances of the converter. By "stitching" together these final and initial states and continually solving the state evolution equation we can obtain time-series data of the converter's state variables.

[2] $x(t) = e^{A(t-t_0)}x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)}Bu(\tau)d\tau$ where $x(t_0)$ is the initial condition for the state variable and $x(t)$ the final state value

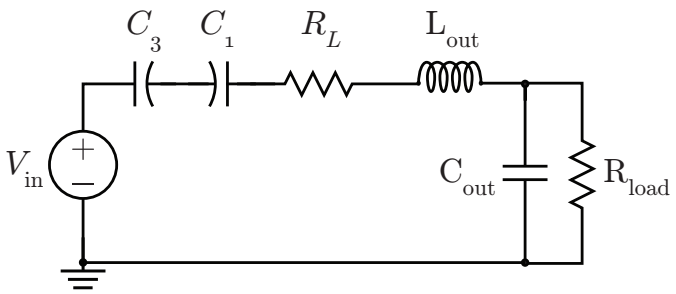

Fig. 3: Sub-circuit of FCML converter with switches $S_{1\text{H}}$, $S_{2\text{L}}$, $S_{3\text{L}}$, and $S_{4\text{H}}$ ON while complementary switches are OFF. Analysis of this circuit yields the state space description of Eq. 5. R_L models the sum of series resistances in the power path (e.g. inductor and FET resistance, etc.).

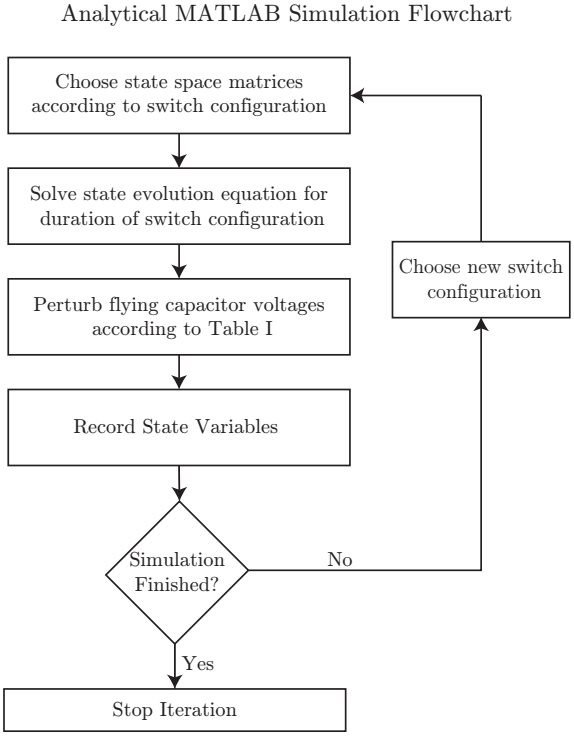

Fig. 4: Flowchart illustrating the MATLAB algorithm developed to obtain the FCML state variables as a function of time.

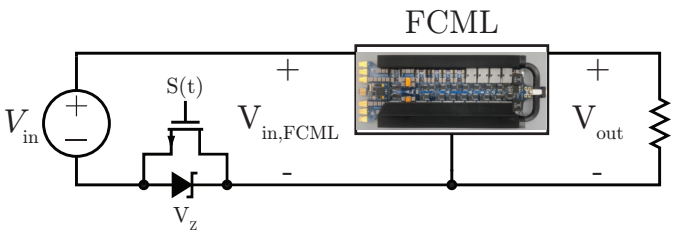

Fig. 5: Simplified schematic of circuit used to obtain fast input voltage transients. The FCML hardware [1] used in Section III is shown as well. By adjusting the switching signal S(t) from OFF to ON, the input voltage to the FCML is raised from $V_{\text{in}} - V_Z$ to V_{in} where V_Z is the Zener voltage of the external Zener diode in series with the input port of the FCML. The hardware employs EPC2034 GaNFETs, 4.4 μF of flying capacitance using C5750X6S2W225K250KA, two parallel XAL1510-153 output inductors and 0.6 μF of C5750C0G2J104J280KC for the output capacitor.

In order to incorporate the charge flows and voltage changes induced by the switch output capacitance, the flying capacitor voltages at the end of a switching state are impulse changed according to Table I and used as the initial value for the next state evolution equation solver. The developed algorithm is shown schematically in Fig. 4.

III. Experimental Validation

To validate the theory of C_{oss} induced natural balancing of flying capacitors, we imposed an input voltage transient on a 5-level FCML converter hardware prototype, and observed the oscillatory response of the flying capacitor voltages and the time-domain response of the circuit. To experimentally observe all pertinent frequencies, the step input voltage excitation must have a rise time sufficiently fast to excite higher frequency oscillations. To accomplish this, the circuit shown in Fig. 5 was devised. Before the step occurs, the gate of the MOSFET is held low (where $S(t)$ is the switching signal applied to the FET) and $V_{\text{in,FCML}} = V_{\text{in}} - V_Z$, where V_Z is the Zener voltage, is applied to the FCML converter's input port. To activate the step, the FET's gate is pulled high, increasing the input voltage to the converter to V_{in} at a high slew rate. This input voltage excitation was applied to the five-level converter hardware demonstration. The output of the converter was connected to a constant 9.8 Ω load and the converter was operated with symmetric PS-PWM at a constant switching frequency of 115 kHz, for an effective switch-node frequency of 460 kHz.

Presented in Fig. 6 are the results from this input voltage step study. As can be seen, both simulation and measured results agree very well when including the impact of C_{oss} on the FCML converter as derived in Section II. If the impact of C_{oss} is not included and the FCML converter is modeled in the traditional way, the flying capacitor voltages will not converge to a balanced state as experiment does. These results are significant as they indicate that previous models of the FCML converter were inadequate as they neglected a key parasitic element in the circuit rather than a flaw in the analysis of the simplified circuit.

Fig. 7 shows the transient response of the FCML converter at a "balanced" conversion ratio of 25%. Since the RLC circuit dynamics investigated in previous works [10], [11] are now able to participate in driving the flying capacitors to their balanced voltages at this conversion ratio, the flying capacitor voltages converge much faster to their balanced values compared to the case of a conversion ratio of 50 %. The FCML converter used to generate these plots, shown in Fig. 9, was a degenerated twelve level converter and used EPC2302 devices, 8.8 μF of flying capacitance, 10 μH and 44 μF for the output filter inductor (IHLP5050CEER100M01) and capacitor[3] respectively and operated at a switching frequency of 75 kHz. The six highest voltage switch pairs were held constantly ON to generate the five level converter.

[3]Both flying capacitors and output capacitors are implemented with C5750X6S2W225K250KA. The capacitance reported is the nominal, non-derated capacitance.

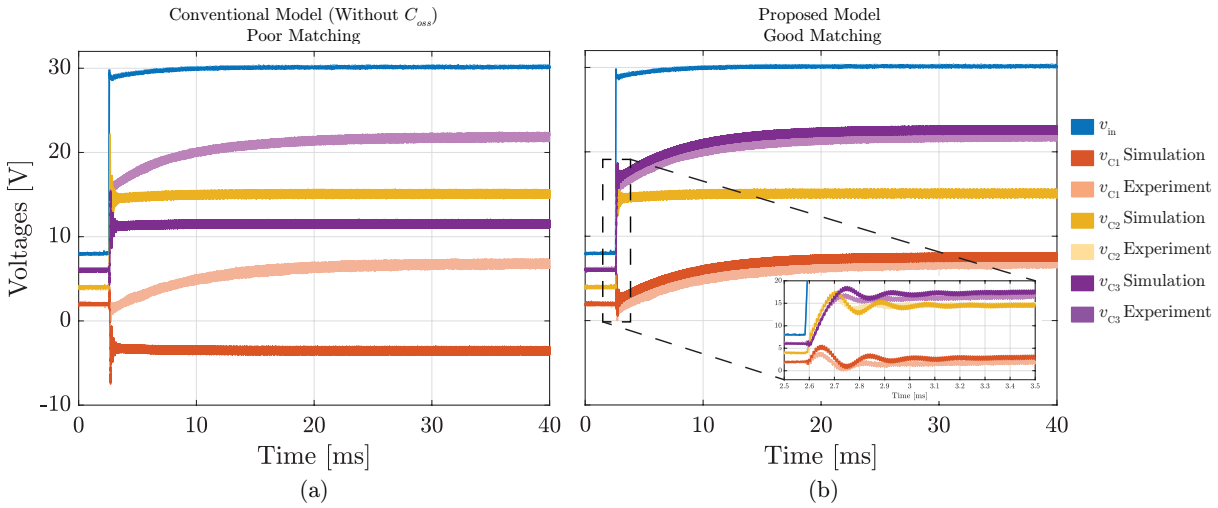

Fig. 6: Measured data from a 5-Level FCML [1] excited with an $\approx$ 22.5 V input voltage step by the circuit of Fig. 5 operating at a duty cycle of 50 %. Figure (a) compares a traditional model (i.e. one that does not include the impact of C_{oss}) with experiment, clearly showing previous models were deficient in modeling the flying capacitors' transient response. Figure (b) elucidates how including the impact of C_{oss} predicts the flying capacitors natural convergence to their balanced values as experiment does. The inset in Figure (b) shows a zoomed in view of the initial flying capacitors' transient response, which exhibits an oscillatory behavior. Both simulations employed the algorithm shown in Fig. 4.

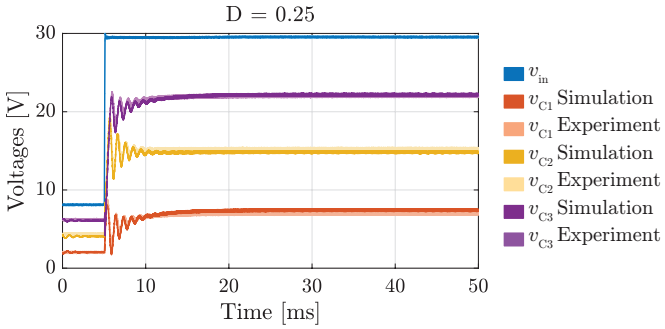

Fig. 7: Measured data from the 5-Level FCML shown in Fig. 9 at a duty cycle of 25 %. Operation at this "balanced" conversion ratio still yields good matching between simulation and experiment. The FCML was excited with the same input voltage excitation as the experiment presented in Fig. 6

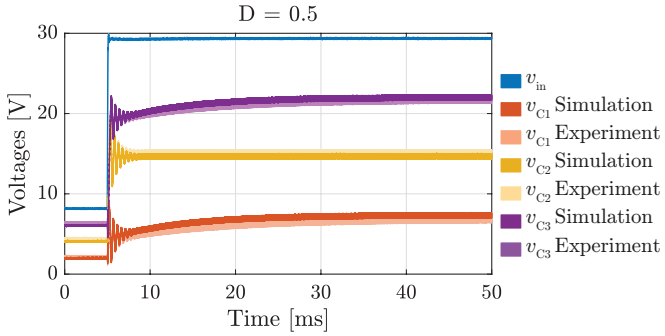

Fig. 8: Measured data from 5-Level FCML shown in Fig. 9 at a duty cycle of 50 % using the same hardware as was used in Fig. 7. The FCML was excited with the same input voltage excitation as the experiment presented in Fig. 6. Compared to the experiment presented in Fig. 6, this hardware switches slower (65 %) and utilizes a larger output capacitor (73x). Despite these differences the presented model and experiment agree quite well.

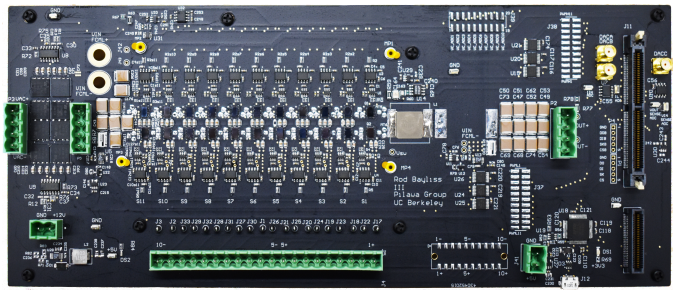

Fig. 9: Hardware photograph of 12 level FCML converter configured for 5 level operation for the experiments performed in Fig. 7 and Fig. 8. This prototype uses EPC2302 devices, C5750X6S2W225K250KA for flying and output capacitors and IHLP5050CEER100M01 for the output filter inductor.

IV. Conclusion

This work has analyzed a key parasitic element, the switch output capacitance C_{oss}, and its impact on the ability for the capacitors within a FCML converter to balance to their desired voltages. Without the inclusion of this previously neglected balancing mechanism, simulation and analytical models of the FCML converter are unable to track experimental data. Ensuring model fidelity of the FCML converter is critical for both flying capacitor voltage estimation (e.g. for converter health monitoring) and active balancing control of the flying capacitor voltages.

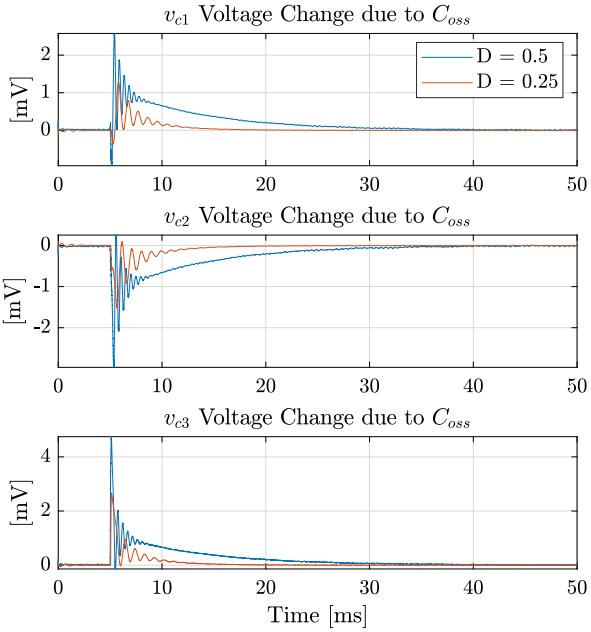

Fig. 10: Simulated period-by-period voltage changes on the flying capacitors denoted in Fig. 1 due to C_{oss} charge redistribution. Charge flows are dictated by the equations from Table I. For visualization the raw voltages are filtered by a moving average filter to capture the average change induced by C_{oss} over a switching period. Note, the integral of these curves would be the cumulative voltage change induced by C_{oss} natural balancing for the transient presented in Fig. 7 and Fig. 8.

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