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***Abstract*—This paper presents a novel circuit topology and control strategy for use in single-phase buck-type power factor correction (PFC) ac-dc rectifiers. We propose a topological change to the flying capacitor multilevel (FCML) converter to place inductors at the input rather than the conventional output along with a novel control strategy for ac-dc operation. The proposed topology retains the high efficiency and power density advantages of the FCML topology while enabling improved control of the input current for PFC operation, and better EMI performance for the same magnetic energy storage. An active flying capacitor voltage balancing control technique is presented, which enables high bandwidth (e.g., 120 Hz) control of the flying capacitor voltages. The new circuit topology and enabling control technique are demonstrated in a six-level, 240 $\mathrm{V_{rms}}$/48 $\mathrm{V_{dc}}$, 817 W hardware prototype.**

I. Introduction

Data center power delivery and other grid-connected applications require a target output dc voltage that is significantly lower than the incoming mains voltage. Additionally, high power factor current must be drawn from the mains interface, requiring a power factor correction (PFC) rectifier. Often, a two-stage approach is employed where the incoming mains voltage is rectified to an intermediate dc voltage higher than the peak of the mains. This intermediate dc voltage is then processed by a second step-down converter to a lower voltage (e.g., 48 V). This two-stage power conversion approach suffers from a cascade of efficiency penalties and lower power density due to the increased effective conversion ratio associated with step-up and step-down operation.

Single-stage rectification directly generates the target voltage from the mains voltage. Given that the target voltage is lower than the peak of the mains, a buck-type PFC rectifier [1], [2] is typically employed. Despite having to turn the converter OFF during the portions of the line cycle where the input voltage magnitude is lower than the output voltage, sufficiently high power factor and current THD can be obtained with the input and output voltages typical of data center power delivery (e.g., $v_{\mathrm{ac}} = 240\,\mathrm{V_{rms}}, V_{\mathrm{out}} = 48\,\mathrm{V_{dc}}$) [3]. Hold-up capacitors and/or twice-line-frequency power pulsation filter capacitors that are typically required in this application provide sufficient energy storage to maintain the dc voltage to the load when the ac-dc stage is turned OFF.

This work employs the flying capacitor multilevel (FCML) converter [4] as the power stage. The FCML converter has the high performance characteristics of small magnetics volume due to reduced inductor volt-seconds and utilization of high-performance low voltage switches [5]. In the buck-type PFC application, however, there are two challenges in utilizing this topology addressed by this work: 1) the input current of the converter must be controlled to achieve both high power factor and low distortion, a challenge for the traditional FCML converter variant where the inductor is placed at the output; and 2) the flying capacitor voltages must track a large signal, twice-line-frequency reference to realize the benefits of the FCML converter. The first challenge is addressed through a topological variant of the traditional FCML converter, termed the input inductor FCML converter, discussed in Section II, while the second challenge is addressed through active flying capacitor voltage balancing and is discussed in Section III. Experimental verification of the proposed topology and control scheme is provided in Section IV.

II. Input Inductor Flying Capacitor Multilevel Converter

The input inductor FCML converter [6]–[9] is a topological variation of the standard output inductor FCML converter. This converter topology belongs to a class of converters with "nonpulsating" port currents [6], enabling a reduction in required input current filtering. This topology was shown to be a promising candidate in buck-type PFC applications in [7].

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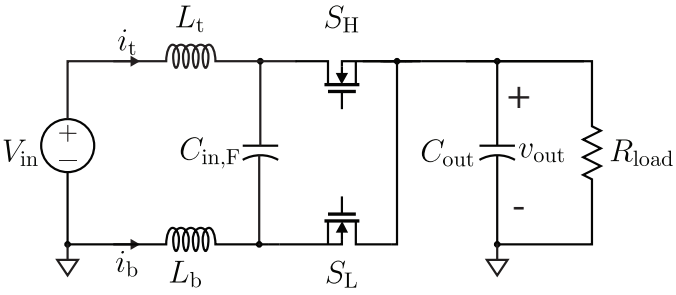


Fig. 1: Circuit diagram of an input inductor buck dc-dc converter.

A schematic drawing an input inductor buck dc-dc converter is shown in Fig. 1 and a drawing of a six-level input inductor FCML rectifier is shown in Fig. 2. The converter maintains the same input-output voltage characteristic as an output inductor FCML converter with $V_\mathrm{out} = DV_\mathrm{in}$ where D is the duty cycle applied to all high-side switches S_H and $S_{\mathrm{H},k}$.

Compared to the output inductor FCML converter, the input inductor variant requires significantly less input current filtering for the same peak magnetic energy storage, a useful proxy for inductor size [10]. This is a consequence of the topology's "nonpulsating" port currents property. First, we derive the total stored magnetic energy in both an output inductor buck converter and an input inductor buck converter. We assume the inductance of all inductors are chosen such that the inductor current ripple ratio $\alpha = \Delta i_L / I_L$ is the same, where Δi_L is the peak-to-peak current ripple and I_L is the average current in inductor L.

The peak energy E_{L_o} stored in the inductor L_o, which carries an average current I_out, for the output inductor buck converter can be derived as

$$\begin{aligned} E_{L_\mathrm{o}} &= \frac{1}{2} L_\mathrm{o} I_\mathrm{pk}^2 = \frac{1}{2} L_\mathrm{o} \left(I_\mathrm{out} + \frac{\Delta i_{L_\mathrm{o}}}{2} \right)^2 \\ &= \frac{1}{2} L_\mathrm{o} I_\mathrm{out}^2 \left(1 + \frac{\alpha}{2} \right)^2 . \end{aligned} \tag{1}$$

The inductance L_o is then defined by the desired current ripple ratio α,

$$L_\mathrm{o} = \frac{D(V_\mathrm{in} - V_\mathrm{out})}{\alpha f_\mathrm{sw} I_\mathrm{out}} \tag{2}$$

yielding a peak inductor energy of

$$E_{L_\mathrm{o}} = \frac{D(V_\mathrm{in} - V_\mathrm{out}) I_\mathrm{out} (1 + \alpha/2)^2}{2\alpha f_\mathrm{sw}} . \tag{3}$$

The input inductor buck converter, shown schematically in Fig. 1, contains two inductors L_t and L_b. We derive the average inductor currents relative to the output current $I_\mathrm{out} = v_\mathrm{out} / R_\mathrm{load}$ by performing a charge balance on $C_{\mathrm{in,F}}$ in order to establish a comparison against the output inductor buck converter:

$$I_{C_{\mathrm{in,F}}} = -DI_\mathrm{b} + (1 - D) I_\mathrm{t} = 0 \tag{4}$$

$$I_\mathrm{b} = \frac{1 - D}{D} I_\mathrm{t} \tag{5}$$

$$I_\mathrm{b} + I_\mathrm{t} = I_\mathrm{out} \tag{6}$$

$$I_\mathrm{t} = DI_\mathrm{out}, \; I_\mathrm{b} = (1 - D) I_\mathrm{out} . \tag{7}$$

The peak energy E_{L_t} stored in L_t is

$$\begin{aligned} E_{L_\mathrm{t}} &= \frac{1}{2} L_\mathrm{t} \left(I_\mathrm{t} + \frac{\Delta i_{L_\mathrm{t}}}{2} \right)^2 \\ &= \frac{1}{2} L_\mathrm{t} \left(DI_\mathrm{out} + \frac{\alpha D I_\mathrm{out}}{2} \right)^2 \\ &= \frac{1}{2} L_\mathrm{t} D^2 I_\mathrm{out}^2 \left(1 + \frac{\alpha}{2} \right)^2 \end{aligned} \tag{8}$$

As in the output inductor buck converter, the inductances are defined by the desired current ripple ratios α:

$$L_\mathrm{t} = \frac{D(V_\mathrm{in} - V_\mathrm{out})}{\alpha f_\mathrm{sw} I_\mathrm{t}} = \frac{(V_\mathrm{in} - V_\mathrm{out})}{\alpha f_\mathrm{sw} I_\mathrm{out}} \tag{9}$$

$$E_{L_\mathrm{t}} = \frac{(V_\mathrm{in} - V_\mathrm{out}) D^2 I_\mathrm{out} (1 + \alpha/2)^2}{2\alpha f_\mathrm{sw}} . \tag{10}$$

While the peak energy E_{L_b} stored in L_b is

$$\begin{aligned} E_{L_\mathrm{b}} &= \frac{1}{2} L_\mathrm{b} \left(I_\mathrm{b} + \frac{\Delta i_{L_\mathrm{b}}}{2} \right)^2 \\ E_{L_\mathrm{b}} &= \frac{1}{2} L_\mathrm{b} \left((1 - D) I_\mathrm{out} + \frac{\alpha (1 - D) I_\mathrm{out}}{2} \right)^2 \\ &= \frac{1}{2} L_\mathrm{b} (1 - D)^2 I_\mathrm{out}^2 (1 + \alpha/2)^2 \end{aligned} \tag{11}$$

$$L_\mathrm{b} = \frac{D(V_\mathrm{in} - V_\mathrm{out})}{\alpha f_\mathrm{sw} (1 - D) I_\mathrm{out}} \tag{12}$$

$$E_{L_\mathrm{b}} = \frac{D(V_\mathrm{in} - V_\mathrm{out})(1 - D) I_\mathrm{out} (1 + \alpha/2)^2}{2\alpha f_\mathrm{sw}} . \tag{13}$$

Finally, the total peak magnetic energy is derived as

$$E_{L_\mathrm{t}} + E_{L_\mathrm{b}} = \frac{D(V_\mathrm{in} - V_\mathrm{out}) I_\mathrm{out} (1 + \alpha/2)^2}{2\alpha f_\mathrm{sw}} , \tag{14}$$

which is identical to (3). Thus the total peak magnetic energy in an input inductor buck converter is the same as that of an output inductor buck converter under the constraint of equal current ripple ratio in all inductors. For an FCML converter, given a level count N, all of the inductors within both an input and output N-level FCML converter are subjected to the same voltages. Additionally, the inductors carry the same average currents as the corresponding inductors in the buck converters. Thus the preceding analysis is directly applicable and the property of constant total peak magnetic energy across both the input and output inductor variants holds.

Typically, the input current of PFC converters must adhere to conducted emissions standards (e.g., CISPR 32) and the input inductor variant offers a distinct advantage over the

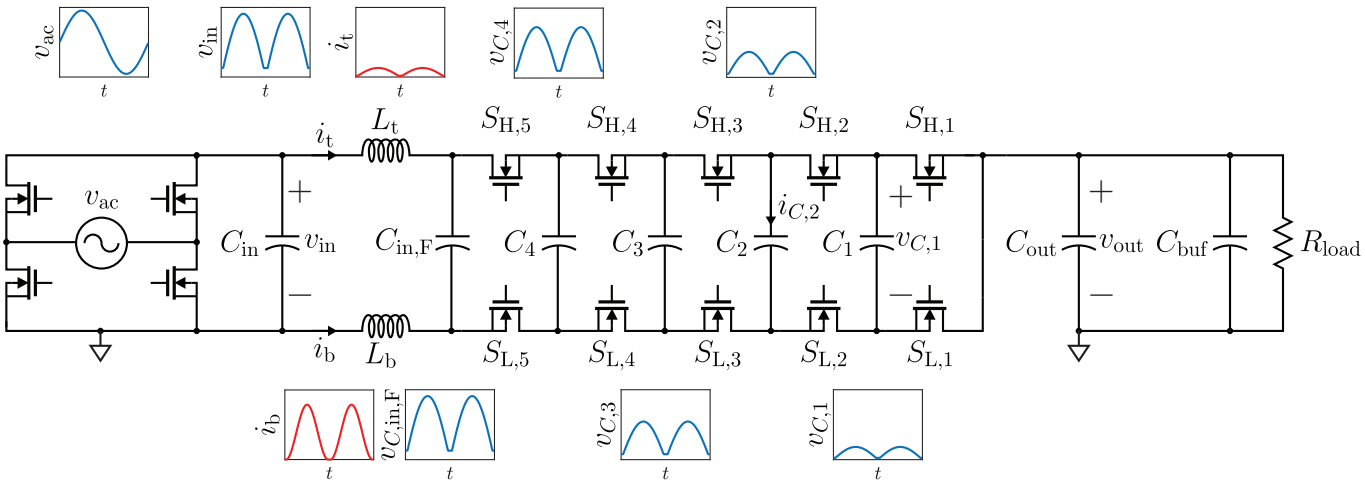


Fig. 2: Circuit diagram of an ac-dc PFC rectifier utilizing a six-level input inductor FCML converter with an input synchronous rectifier. C_{out} serves to buffer switching frequency ripple while C_{buf} performs twice-line frequency power buffering.

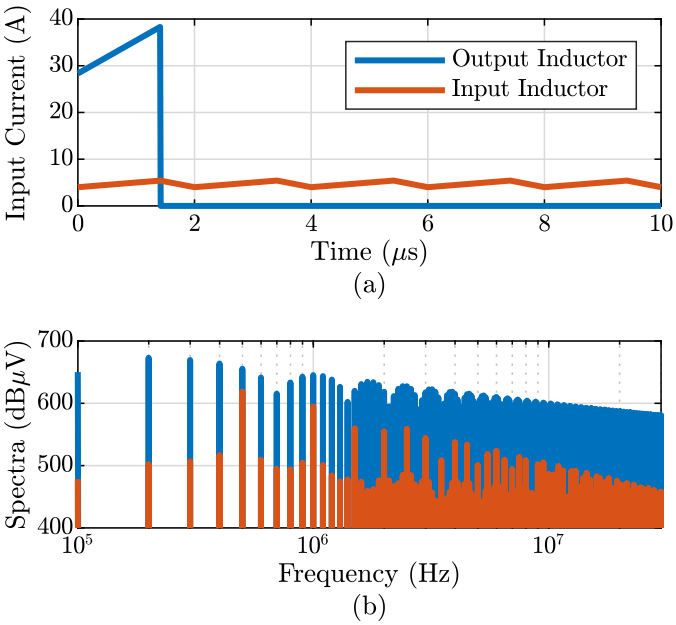


Fig. 3: Simulation comparison of the input current waveform in (a) the time-domain and (b) spectra in the frequency-domain between an output inductor and input inductor FCML converter. Both converters employ a six-level FCML converter operating at the same dc-dc operating point of: $V_{\text{in}} = 339\,\text{V}$, $V_{\text{out}} = 48\,\text{V}$, $P_{\text{out}} = 1.6\,\text{kW}$, $f_{\text{sw}} = 100\,\text{kHz}$. The inductances of the three inductors were chosen such that the inductor current ripple ratio was 30%. The spectra voltage is the voltage that would be measured across a $50\,\Omega$ resistor conducting the input current (as would occur in a line impedance stabilization network). As noted in Section II, the peak magnetic energy stored in the two converters is the same.

output inductor variant in this regards. To assess the filtering effort required, we define the input current as the current supplied by the grid assuming the grid behaves as a perfect voltage source (i.e., the current that flows through $S_{\text{H},N-1}$ for the output inductor FCML converter and i_{t} for the input inductor FCML converter). Fig. 3 shows a comparison in the input current spectra between an input inductor and output inductor FCML converter. Both converters in this simulation study operate at the same input/output voltages, output power, and switching frequency. Since both inductors operate at the same ripple ratio, the total magnetic energy is the same. However, due to the "nonpulsating" continuous input current property of the input inductor FCML converter, the input current spectra are significantly reduced: up to 175 dBμV over the frequency range of 150 kHz–3 MHz. This reduction in input current disturbance will result in a reduced input filter volume and/or loss to meet the same input current emissions specification.

Finally, in comparison with the output inductor variant, the input inductor FCML converter reduces the effort required for power factor correction control. Since L_{t} is directly in series with the rectified input voltage source, control of i_{t} directly controls the input current. In comparison, for the output inductor FCML converter, controlling the output inductor current does not directly dictate the input current as $\langle i_{\text{in}} \rangle = D\langle i_L \rangle$ where $\langle x \rangle$ denotes the average value of x over a switching period and D is the duty cycle applied to the high-side switches. Additionally, the input and flying capacitors within the output inductor FCML converter present a reactive power draw to the grid [2]. To compensate this reactive power draw and maintain high power factor, the inductor current reference must be modified to be bipolar rather than strictly positive. This presents control challenges for the active balancing controller as the inductor current crosses zero.

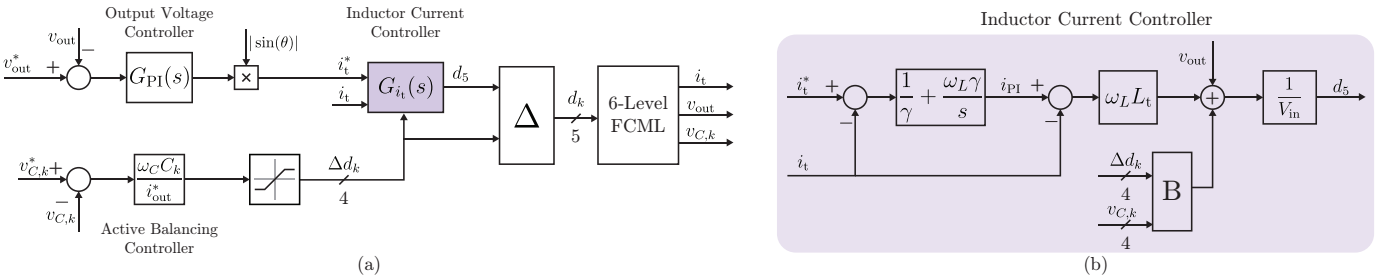


Fig. 4: Block diagram for the implemented combined active flying capacitor voltage balancer and inductor controller for a six-level input inductor FCML converter. (a) Overall control structure. (b) Inductor current controller which includes both feedback decoupling and a PI controller. Block **B** represents the feedback decoupling between the active flying capacitor voltage balancer and the inductor current controller, shown explicitly in (20). Block Δ generates individual duty cycles from the collection of d_{N-1} and Δd_k as in (21).

III. Controller Development

A significant challenge associated with using an FCML converter in a buck-type PFC application is the large-signal, time-varying input voltage. That is, the voltages on C_{in} and $C_{\text{in,F}}$ follow a rectified sinusoid value with a frequency of twice the mains frequency (e.g., 120 Hz). In order to utilize low voltage switches, the voltages on the flying capacitors within the converter must maintain a "balanced" distribution where $v_{C,k} = (kv_{\text{in}})/(N-1)$ where k ranges from 1 to $N-2$. If this flying capacitor voltage distribution is not maintained, excessive voltage stress will be applied to the switches, potentially resulting in converter failure. Typically, the FCML converter is operated with symmetric phase shifted-PWM (PS-PWM); in this scheme each high-side switch is modulated with the same duty cycle and switch gating signals are evenly phase shifted [4], yielding *passive balancing* of the flying capacitor voltages [11], [12]. The bandwidths of passive balancing are often insufficient to allow the flying capacitors to track a twice-line-frequency reference as would be required in a buck-type PFC application [2].

A. Plant Model

Active flying capacitor voltage balancing changes the modulation scheme of the converter to achieve the desired flying capacitor voltage distribution. The derivation of this control law is similar to the derivations of [13], [14] and was shown to be effective in an output inductor FCML converter for buck-type PFC applications in [15]. We use state space averaging [16] to analyze the plant and make the simplifying approximation that $v_{C_{\text{in,F}}} \approx v_{C_{\text{in}}}$. First, we develop a model for the flying capacitor voltages assuming that the high-side switches $S_{\text{H},k}$ are driven by switching signals q_k which have duty cycles d_k:

$$\begin{aligned}\langle i_{C,k}\rangle &= C_k\frac{\text{d}}{\text{d}t}\langle v_{C,k}\rangle = \langle (q_{k+1}-q_k)(i_{\text{t}}+i_{\text{b}})\rangle \\ &\approx \langle q_{k+1}-q_k\rangle\langle i_{\text{t}}+i_{\text{b}}\rangle \\ &= (d_{k+1}-d_k)(I_{\text{t}}+I_{\text{b}}) \qquad (15)\\ &= \Delta d_k(I_{\text{t}}+I_{\text{b}}), \qquad (16)\end{aligned}$$

where $I_{\text{t}} = \langle i_{\text{t}}\rangle$. Thus the flying capacitor voltages respond primarily to Δd_k, the differences in duty cycles of adjacent switch pairs. To develop a plant model for the top inductor current i_{t}, we analyze the voltage across L_{t}:

$$\langle v_{L_{\text{t}}}\rangle = \left\langle v_{C,\text{in}}q_{N-1} - v_{\text{out}} - \sum_{k=1}^{N-2}(q_{k+1}-q_k)v_{C,k}\right\rangle \qquad (17)$$

$$L_{\text{t}}\frac{\text{d}}{\text{d}t}\langle i_{\text{t}}\rangle \approx \langle v_{C,\text{in}}\rangle d_{N-1} - \langle v_{\text{out}}\rangle - \sum_{k=1}^{N-2}\Delta d_k\langle v_{C,k}\rangle. \qquad (18)$$

The inductor current thus primarily responds to a weighted sum of all of the duty cycles and the output voltage v_{out}. We can focus exclusively on the flying capacitor voltages $v_{C,k}$ and the top inductor current i_{t} as the control objectives are to regulate the input current and the flying capacitor voltages. The active flying capacitor voltage balancer can thus adjust Δd_k to control the flying capacitor voltages $v_{C,k}$ and the inductor current controller can adjust d_{N-1} to control the inductor current i_{t}. As in [15], feedback decoupling [13], [17] can be employed to remove the dependence of the inductor current on the output of the active flying capacitor voltage balancer Δd_k. Fig. 4 shows a control block diagram of the implemented control strategy.

B. Controller Design

The duty cycle control law is thus given by:

$$\Delta d_k = \frac{\omega_C C_k}{i^*_{\text{out}}} = \frac{\omega_C C_k V_{\text{out}}}{i^*_{\text{t}} V_{\text{in}}} \qquad (19)$$

$$d_{N-1} = \frac{1}{V_{\text{in}}}\left((i_{\text{PI}}-i_{\text{t}})L_{\text{t}}\omega_L + v_{\text{out}} + \sum_{k=1}^{N-2}\Delta d_k v_{C,k}\right) \qquad (20)$$

$$d_k = d_{k+1} - \Delta d_k,\ k \in (1, N-2), \qquad (21)$$

where i_{PI} is the output of the PI controller shown in Fig. 4(b). The following control parameters were chosen empirically: $\omega_L = 2\pi\cdot 2.78\,\text{kHz}$, $\omega_C = 2\pi\cdot 477\,\text{Hz}$, $\gamma = 0.35$.

The output of the active balancer Δd_k is followed by a saturation block with symmetrical limits of $\pm 1\%$. Near the zero-crossing of the grid voltage, the slew rates of the flying capacitor voltages are largest and the inductor currents are

smallest. These two properties result in large control actions from the active flying capacitor voltage balancer. By introducing a saturation block, the destabilizing effect of excessively large Δd_k can be avoided and minimal switch voltage stress maintained. Compared to [13], the inductor current controller uses measured flying capacitor voltages (rather than their quiescent values) when calculating the feedforward component of d_{N-1} (i.e., $\Delta d_k v_{C,k}$ rather than $\Delta d_k \cdot kV_{\text{in}}/(N-1)$ in (21)). This design choice resulted in improved current quality, particularly near the zero-crossings of the grid voltage. As in [15], by introducing scaling constant γ to the PI controller's proportional and integrator terms (cf. [13]), a larger phase margin and high-frequency gain are achieved. However, the system is no longer designed to be first-order, one of the objectives in [13].

IV. Experimental Results

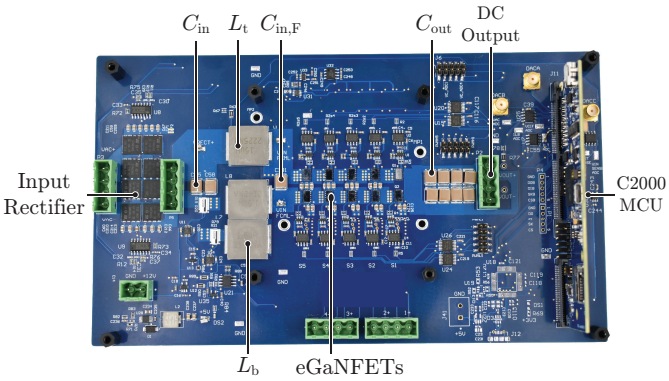


Fig. 5: Photograph of the hardware prototype. A component list of the power stage is provided in Table I. Dimensions: 222 mm × 127.5 mm.

TABLE I: System Specifications and List of Main Components

Parameter	Value
v_{ac}	208-240 V_{rms}
V_{dc}	48 V
P_{out}	820 W
f_{sw}	100 kHz
Power Semicond.	1.8 mΩ 100 V EPC 2302
Rectifier	61 mΩ 650 V STL57N65M5
L_{t}	15 μH (IHLP6767DZER150M11)
L_{b}	3 μH (IHLP6767DZER1R5M11)*
C_{buf}	162 mF (380LX183M063A082)
C_{in}	4.4 μF (C5750X6S2W225K250KA)
$C_{\text{in,F}}$	11 μF (C5750X6S2W225K250KA)
C_{out}	30.8 μF (C5750X6S2W225K250KA)
C_1	8.8 μF (C5750X6S2W225K250KA)
C_2	13.2 μF (C5750X6S2W225K250KA)
C_3	17.6 μF (C5750X6S2W225K250KA)
C_4	22 μF (C5750X6S2W225K250KA)

*L_{b} is composed of two 1.5 μH inductors in series.

A hardware prototype, shown in the annotated photograph of Fig. 5, was developed to validate the proposed topol-

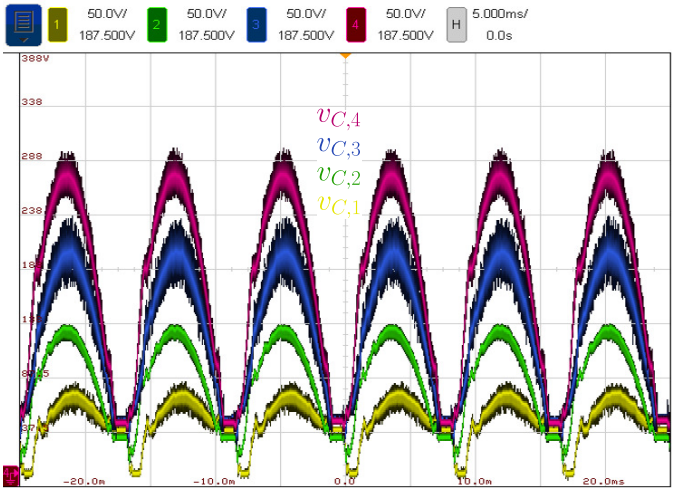
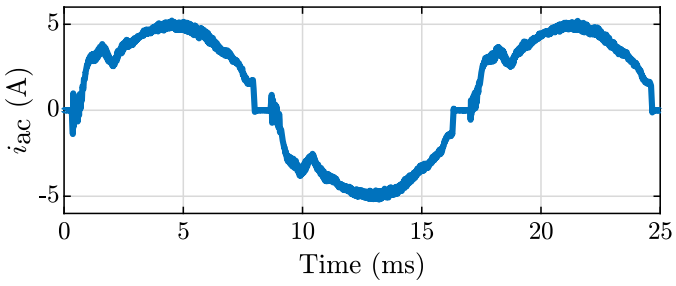
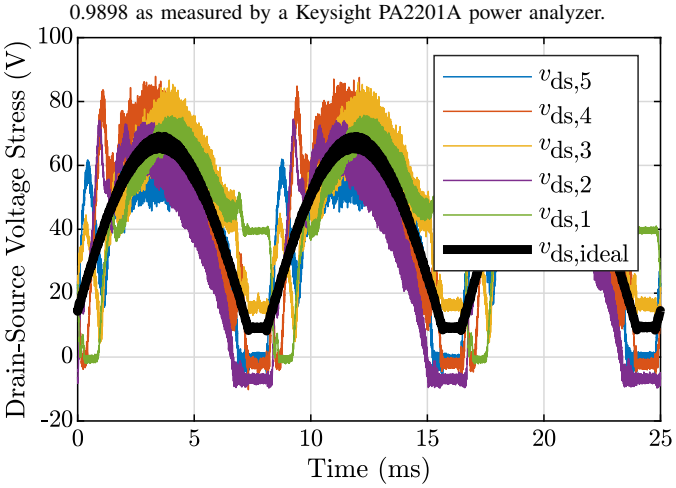


Fig. 6: Measured flying capacitor voltages. The flying capacitor voltages are able to track their reference values sufficiently well to limit the peak switch voltage stress.



(a) Measured line current. The input current achieves a power factor of 0.9898 as measured by a Keysight PA2201A power analyzer.



(b) Measured switch drain-source voltage stress. Ideally, the peak switch drain-source voltage is $v_{\text{in}}/(N-1)$ (plotted in black). This ideal voltage stress is achieved only when all flying capacitor voltages are at the balanced distribution.

Fig. 7: Measured input voltage and current and switch voltage stress when operating at $v_{\text{ac}} = 240\,V_{\text{rms}}$, $V_{\text{out}} = 48\,V$, and $P_{\text{out}} = 817\,W$. High fidelity control of the input current to achieve high power factor and sufficient flying capacitor voltage balancing to limit the peak switch voltage stress are the most pertinent goals of the controller. The peak switch voltage stress is 88.37 V.

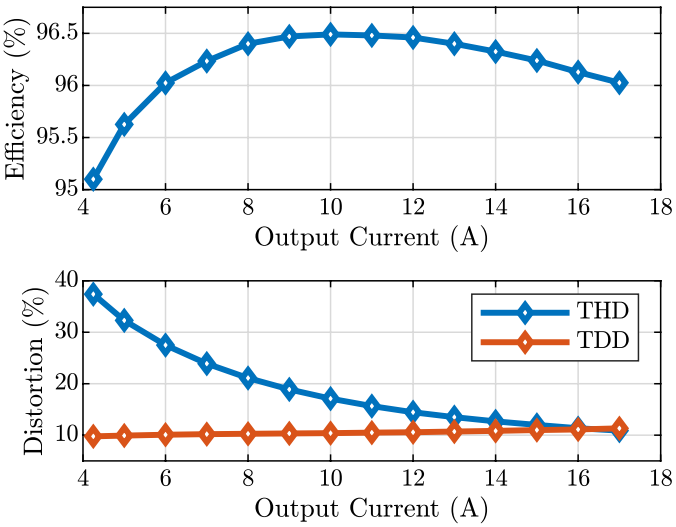


Fig. 8: Measured efficiency and line current THD and TDD for the operating point $v_{\text{ac}} = 208\,\text{V}_{\text{rms}}$, $V_{\text{out}} = 48\,\text{V}$. The measured peak efficiency is 96.49% at $P_{\text{out}} = 480\,\text{W}$. The measured line current passes the IEC61000-3-2 Class A harmonic limits for all measured points.

ogy and control structure. Relevant system specifications and component parameters are given in Table I. A second order generalized integrator (SOGI) [18] was used to generate the reconstructed grid voltages for phase-locking. A discrete $10\,\mu\text{H}$ inductor was inserted in series with the ac power supply to emulate realistic grid inductance.

As can be observed in Fig. 6, the flying capacitor voltages track the rectified sinusoidal reference, indicating low voltage stress on the switches. Fig. 7 shows the measured input current and switch voltage stress. The input inductor current i_{t} tracks its rectified sinusoid reference, yielding high power factor and low THD input current. Additionally, as evidenced by Fig. 7(b), the active flying capacitor voltage balancing controller is able to maintain low switch voltage stress across the full ac cycle. Switch drain-source voltage stress is calculated as the differences in adjacent flying capacitor voltages for $v_{\text{ds},2,3,4}$. $v_{\text{ds},5} = v_{C,\text{in,F}} - v_{C,5}$ and $v_{\text{ds},1} = v_{C,1}$. The peak switch voltage stress is 88.37 V.

At an input voltage of $208\,\text{V}_{\text{rms}}$, the converter achieves a full-power (820 W) efficiency of 95.64% at a power factor of 0.993 and current THD of 9.79% and a peak efficiency of 96.49% at an output power of 480 W. At an input voltage of $240\,\text{V}_{\text{rms}}$, the converter achieves a full-power efficiency of 95.72% at a power factor of 0.990 and current THD of 12.75% as measured by a Keysight PA2201A power analyzer. Fig. 8 shows the efficiency and line current distortion characteristic with respect to output current. Total demand distortion (TDD) is defined as $\text{TDD} = \text{THD} \cdot I_1/I_{\text{D}}$, where THD is the total harmonic distortion, I_1 the fundamental current magnitude and I_{D} the rated fundamental current. From 25% power to full load, the TDD is below 12%. Across this power range, the measured line current harmonics stay well within the IEC61000-3-2 Class A limits.

V. Conclusion

This paper presents an input inductor FCML converter for a buck-type PFC rectifier utilizing active flying capacitor voltage balancing. The input inductor topology reduces both the control and filtering effort required for achieving high quality mains current compared to an output inductor topology. Additionally, the FCML converter enables high power density through a reduction in magnetics volume and high efficiency through the utilization of low voltage switches compared to a two-level converter. To utilize the FCML converter in this application, an active flying capacitor voltage balancing control scheme was developed which operates in tandem with the input current controller. The proposed topology and controller were validated on a hardware prototype resulting in a peak efficiency of 96.49% and a current THD of 9.79% at full load converting $208\,\text{V}_{\text{rms}}$ to 48 V.

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