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## PROGRAM AUGAT

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## ABSTRACT

A program has been written and used for over a year which allows the engineer to more easily design, document and build hardware on the Augat 8136-RG4 logic card. Input is via a card deck of control cards interspersed with data cards. A description of the control and data cards, their function and operation is given, as well as a simple example.

## INTRODUCTION

The AUGAT program is designed to help the engineer develop a good design of a circuit consisting of integrated circuits on an AUGAT 8136-RG4 wire wrap card.

The AUGAT 8136-RG4 card consists of 60 sockets in a 5 x 12 array, and 120 edge connectors. The Augat card is 1/8 inch thick, and is 7-3/8 inches wide by 7 inches long. The back of the card contains an array of wire wrap pins 1/2 inch long. Figure 1 illustrates the card.

Each card contains a ground (GND) and Vcc (+5 V) printed circuit plane on opposite sides of the card.

Each socket consists of an array of 18 wire wrap pins and 16-pin I. C. Sockets, at normal spacing for the standard DIP package. The two additional pins are a local source of +5 V and GND. Any socket may be loaded with any 4,6,8,14 or 16-pin DIP, or discrete components. The program has facilities for processing 8-, 14-, and 16-pin DIP automatically.

The edge connector consists of 60 printed fingers on each side of the board, and a key slot. There is also an array of 120 wire wrap pins, numbered 1 to 122, with pins, numbers 58 and 119 (corresponding to finger location at the key slot) missing.

#### CIRCUIT DESCRIPTION

A circuit is described in terms of signal names and socket/edge locations. The basic description may be modified by additional commands, described below.

A signal is an eight character name, which may contain imbedded blanks. Any character string may be used for a signal name, subject to two conditions: 1) a name consisting of all blanks is ignored; 2) a signal which has the character "\$" as the first character is treated specially. Otherwise identical names with imbedded blanks in different position are treated as different names. Thus, "SIGNAL1" is considered by the program to be different than "SIGNAL 1".

Any signal with a "S" prefix is considered to be the same as the identical signal without the \$, and with an appended blank: "\$" is merely a code for a signal source, and the pin to which it is applied is so flagged. (Various of the output documents will have the "\$" flag shown to aid the engineer) Thus, "\$CLOCK1^" is identical to "CLOCK1^^".

A physical component (I.C., edge pin group) is first invoked by the appropriate command, and then described by the appropriate number of cards containing up to ten names each, in 10A8 format. This is illustrated in Appendix 1.

A component may, if desired, be defined more than once (provided this is done cautiously). In this case, new signals override old signal definitions, but blank signals will leave the previous definition unchanged. Similarly, a blank input may be overridden by a BUSS command to connect +5 V and GND to an I.C.

(NOTE: The program will become confused if a signal is redefined after a LINK command has been issued.)

Successive signal names will be allocated to successive I.C. pins in prevailing I.C. mode (8-PIN, 14-PIN and 16-PIN). Thus in 14-PIN mode, the eight signal name will correspond to pin 8 of a 14-pin I.C., or to pin 10 of that socket.

## WIRE ROUTING

Upon recognizing a LINK command, AUGAT will proceed to connect all pins with the same signal, and perform routing on the interconnections. This is done in four passes, illustrated in Figs. 2 through 5.

Essential to this description is the concept of signal strings. A signal string consists of a list of one or more pins associated with a given signal name, linked together in the order in which they will be wired. The result of a LINK command is one separate signal string for each signal defined.

Routing Pass 1: (Fig. 2) for each of the 18-pin socket pins which is the start of a signal string, the end of that string is found, and linked to the next signal string (identical as to signal). This is iterated until each socket contains only one signal string for each unique signal. At this point GND and +5 V are linked for each socket.

Routing Pass 2: (Fig. 3) for each of the five sockets in a column (e.g., numbers 1,13,25,37 and 49) routing is performed for signal strings, excluding +5 V and GND. The result is the shortest possible routing within a given column.

Routing Pass 3: (Fig. 4) for each defined edge pin, the nearest signal string (either edge or column) is found and linked into a new string starting at the edge.

Routing Pass 4: (Fig. 5) at this point any given signal will have no more than 12 signal strings, each moving predominantly column-wise. The program now proceeds from one side of the card to the other linking

signal strings together. Individual strings may be inverted (turned end-for-end) if this will provide shorter interconnection links.

The result of routing is a near optimum (on the basis of wire length) string of wires connecting pins together. (NOTE that a linked string may be relinked as a single string after future placements.)

#### COMMANDS

Commands are cards designated by an asterisk "\*" in column 1. The next eight characters are the mnemonic command. Successive card fields are numbers (13), I.D. (A8) and comment (5A10). The individual commands are described below.

#### PROGRAM CONTROL

RESTART	reinitialize the program to process another source deck.
END	cause the program to exit.

#### LISTING CONTROL

LIST	list cards input.
NOLIST	do not list input cards.



MODIFIERS

- 8-PIN declare mode of successive I.C.'s to be 8-Pin with Pin 4 = GND, 8 = +5 V.
- 14-PIN declare mode of successive I.C.'s to be 14-Pin with Pin 7 = GND, 14 = +5 V.
- 16-PIN declare mode of successive I.C.'s to be 16-Pin with Pin 8 = GND, 16 = +5 V.
- BUSS declare pin Number to have the default signal assignment of ID. (ID must be "+5 V" or "GND".)
- RESERVE declare socket Number to be reserved.
- SOCKET declare socket Number to be of type ID. This command is followed by one (if mode is 8-Pin) or two (if mode is 14- or 16-Pin) data cards containing signal names. Comments are maintained with each socket.
- EDGE declares that, starting at Edge pin Number, up to ten signals will be defined, from the one card following. Comments are maintained with pin Number.
- LINK causes all signals defined to be linked into input strings. (Note: no signal is defined unless that socket is called out.)
- CARD print a picture of the card showing all signals on edge pins, and the contents of all sockets.
- CLIST print the list of all edge pins used, the signal output, and wires routed to and from that pin, as well as comments assigned to a pin. Then print a list of all non-empty sockets, listing both the socket pin number and the I.C. pin number of each pin, the signal assigned, and all wires routed to and from each pin. Comments input with each socket are listed.
- SLIST print a list of all signals, listed in alphabetic order and the list of pins associated with each signal. (List is in routing order).

WLIST            print a wireman's list of all wires used. Each entry will have a check place "()", a wire number, from-location, to-location, and wire length. (Note that wire length is dependent on wire size, so the program lists only insulation length.)

PUNCH            write a file names "PAPER", appropriate to the LBL semi-automatic wire wrap machine, (in the same sequence as printed via WLIST), and print a table of wire wrap machine bin numbers, wire length, and number of wires required.

Both WLIST and PUNCH will first process all +5 V and GND connections, since these are the most common and shortest multiple wire strings. Successive wires will bury these interconnections.

Successive signals will be wired in the order they appear in our table internal to the program. This table may be in either of two forms. The table is originally filled in the order signals are defined. However the command SLIST reorders this table in alphabetical order. Thus, if the SLIST command is given before either WLIST or PUNCH, the wires will be output alphabetically. If SLIST is not called upon, wire settings will be output in the order of definition.

#### USING THE PROGRAM

The program exists at the computer center as a datacell file, ready to use. The control card sequence required is:

-JOB CARD-  
LIBCOPY (EEBINARY, AUGAT, AUGAT)  
7-8-9 card  
AUGAT command desk  
6-7-8-9 card

The file PAPER is generated if a \*PUNCH command is included in the command deck. This file may either be copied or assigned (via a REQUEST card) to the paper tape punch (PP).

#### INTERNAL DATA STRUCTURE

A brief description of the basic data structure, intended to the program, is included as a reference and guide to others intending to produce a similar program.

There are two basic data structures. The first of these is a NAME structure, in the form of a linear list (vector). Each of the NAME list elements consists of a unique 8-character BCD signal name, and a pointer cell. The pointer cell is used to contain either a negative (Flag) index (for the BUSSED signals, "+5 V" and "GND") or a positive index to an entry in the second data structure, the PIN structure.

The PIN structure element has three major cells; a FLAG cell, a FROM-pointer cell, and a TO-pointer cell. The FLAG cell contains various binary attributes of the pin (such as "Edge Pin", "Signal Source", "Socket Type", etc.).

The PIN-pointer cells are used to link the PIN-elements into a bi-directional signal string, and to link this string to the NAME list element, a pointer value of zero indicates end-of-string list. A

positive, non-zero value is an index for the next pin in the list. A negative value can exist only in a FROM-cell, and designates both the beginning of the list, and the negative index of the corresponding NAME cell.

The NAME structure, being a linear list, has an element count associated with it, and indeed, is treated as a stack when new elements are added to it. It may be reordered for alphabetization, at which time appropriate adjustments are made in any pertinent PIN-FROM-pointer cells.

The PIN structure is partitioned into a linear EDGE-PIN array, and a three-dimensioned SOCKET-PIN array. These partitions permit the simple referencing of a pin by position in a socket, and to a socket by its row and column.

Physical (X-Y) coordinates of each pin are derived from these partitions and indices, rather than being carried along with each pin elements.

In addition to the above major structures, there are minor data structures used to map between external representation of device pin labels, external socket pin labels, and internal representations.

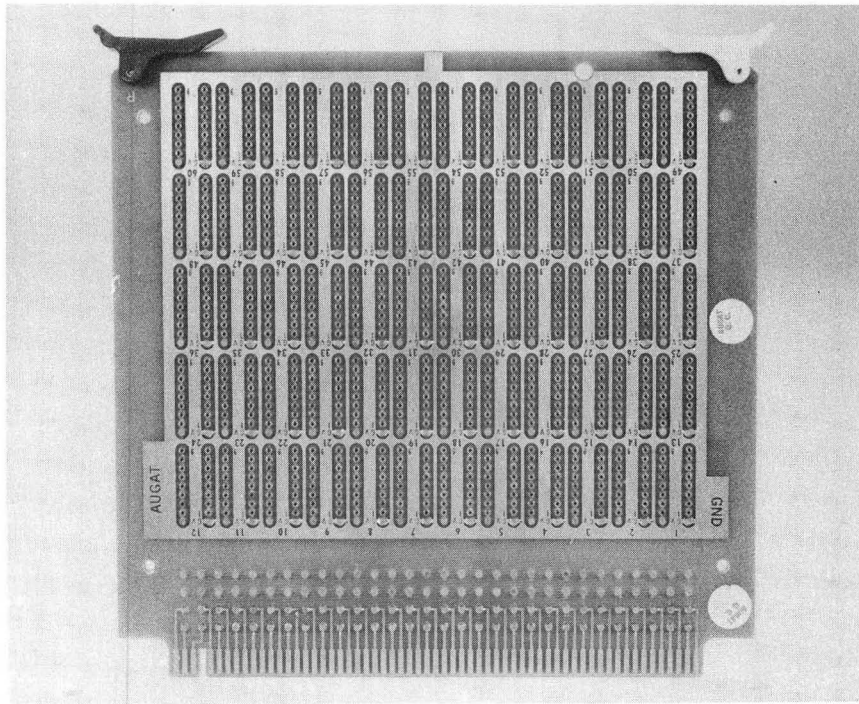


Fig. 1A. Augat Board, Component Side

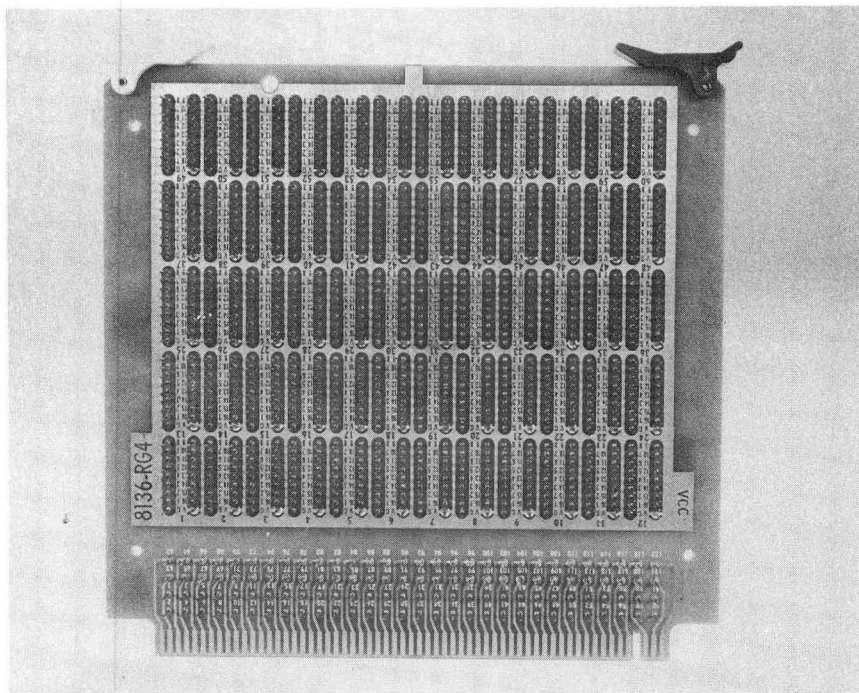


Fig. 1B. Augat Board, Pin Side

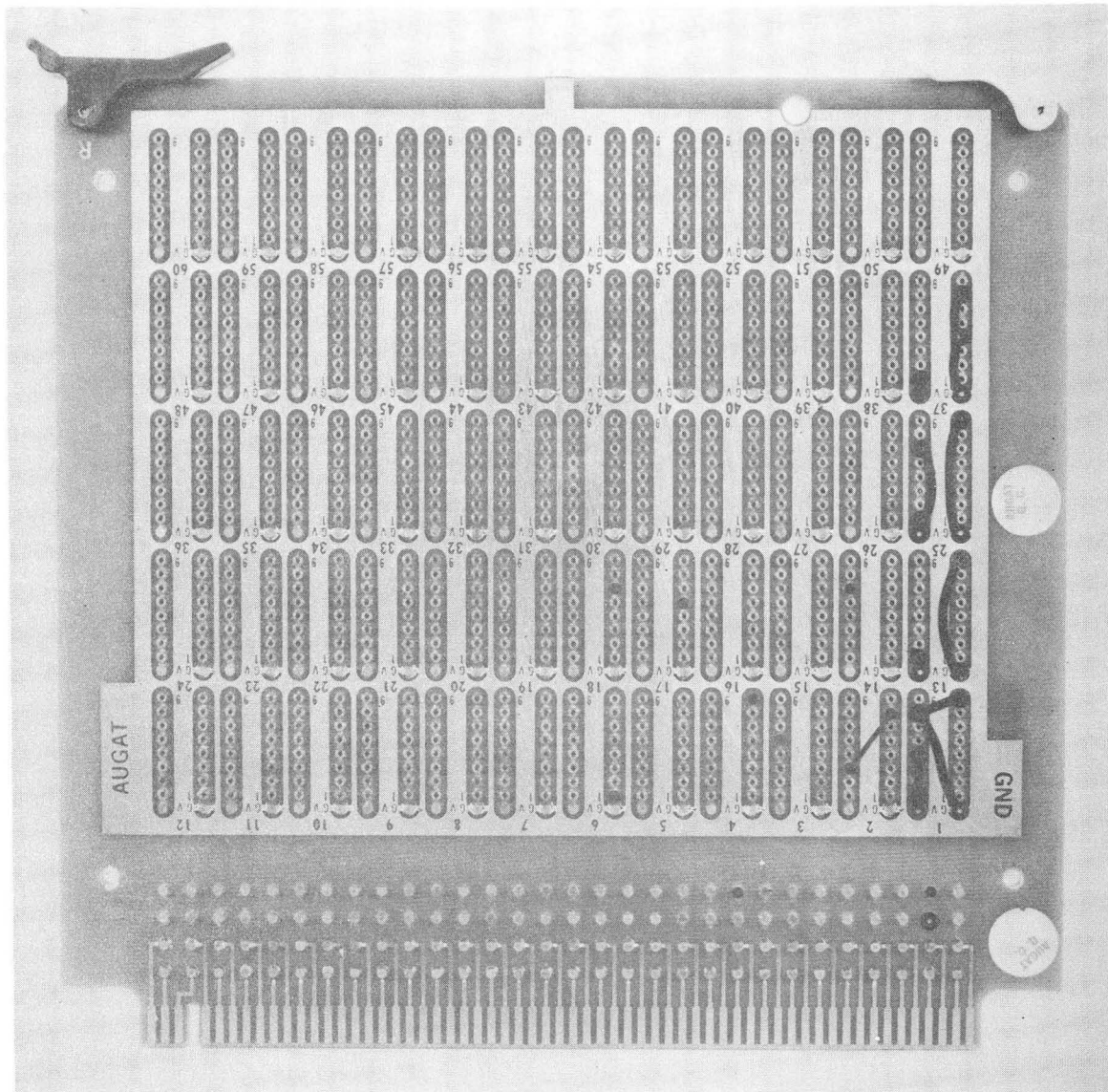


Fig. 2. The interconnection of an arbitrary set of pins after Routing Pass 1. Large circles indicate GND and +5 V; small designate a specific signal. Only interconnections within a socket are generated at this time.

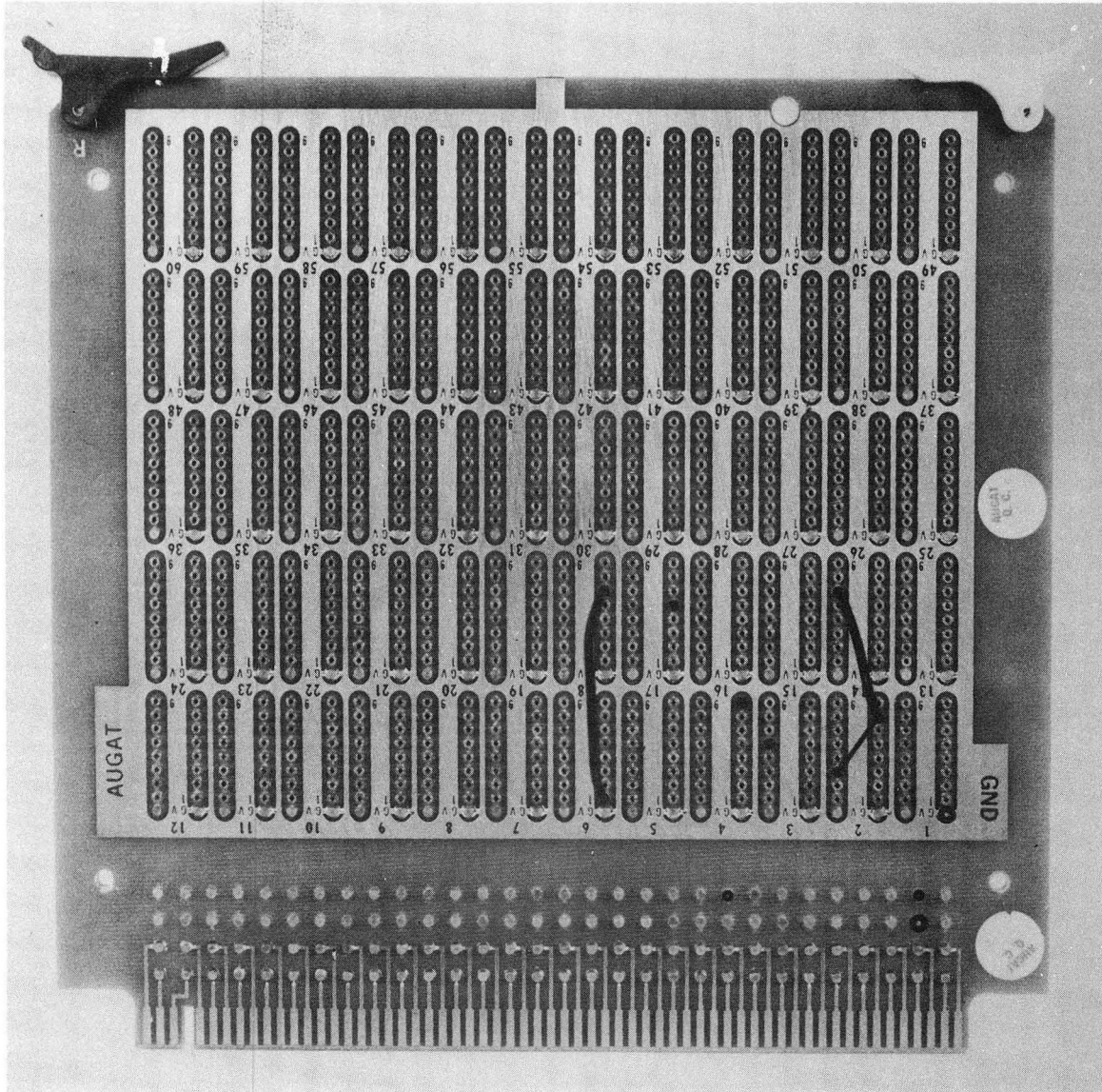


Fig. 3. As in Fig. 2, but now at the completion of Pass 2. Thin Lines indicate previously wired signal strings. GND and +5 V have been eliminated for clarity.

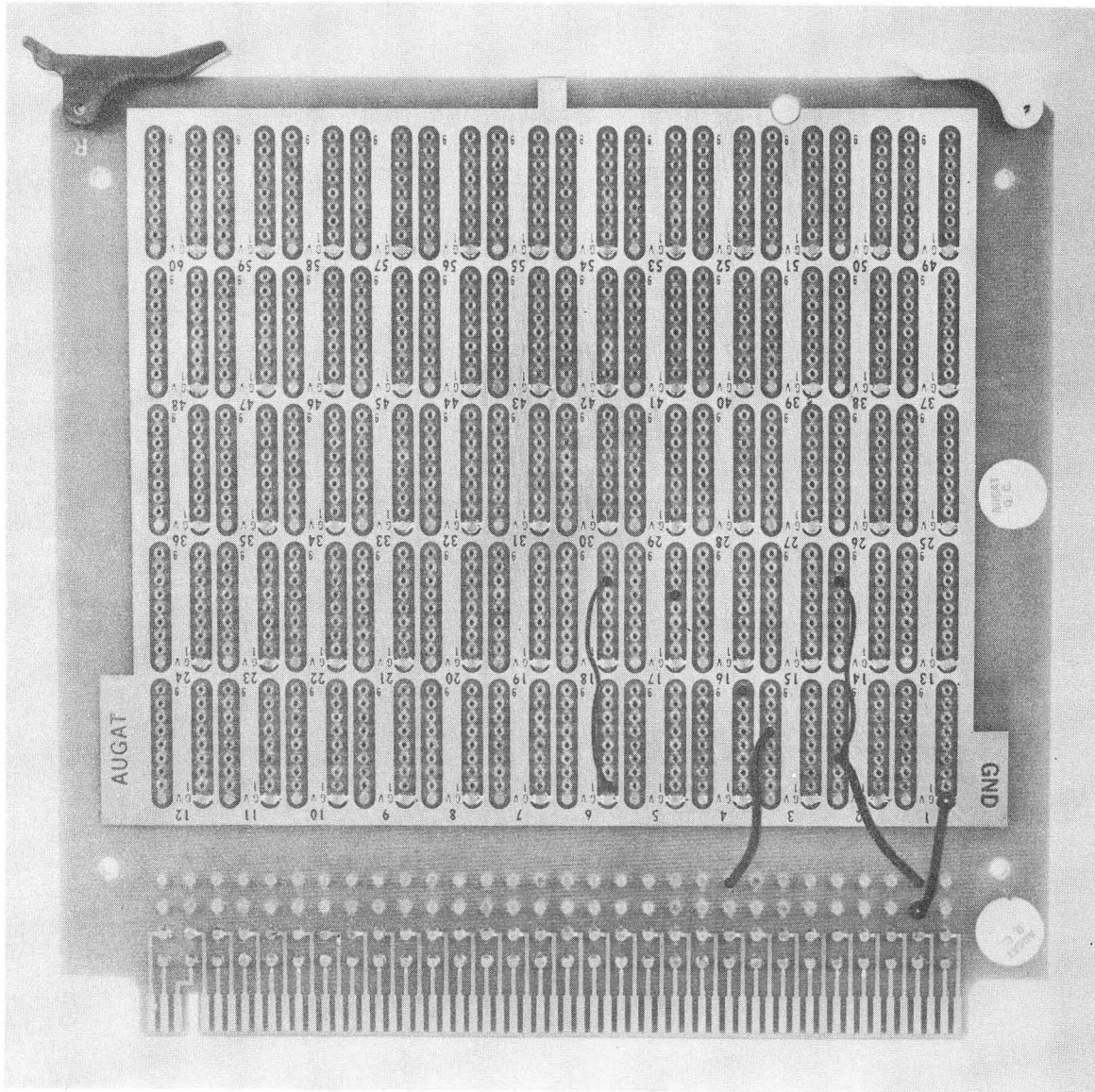
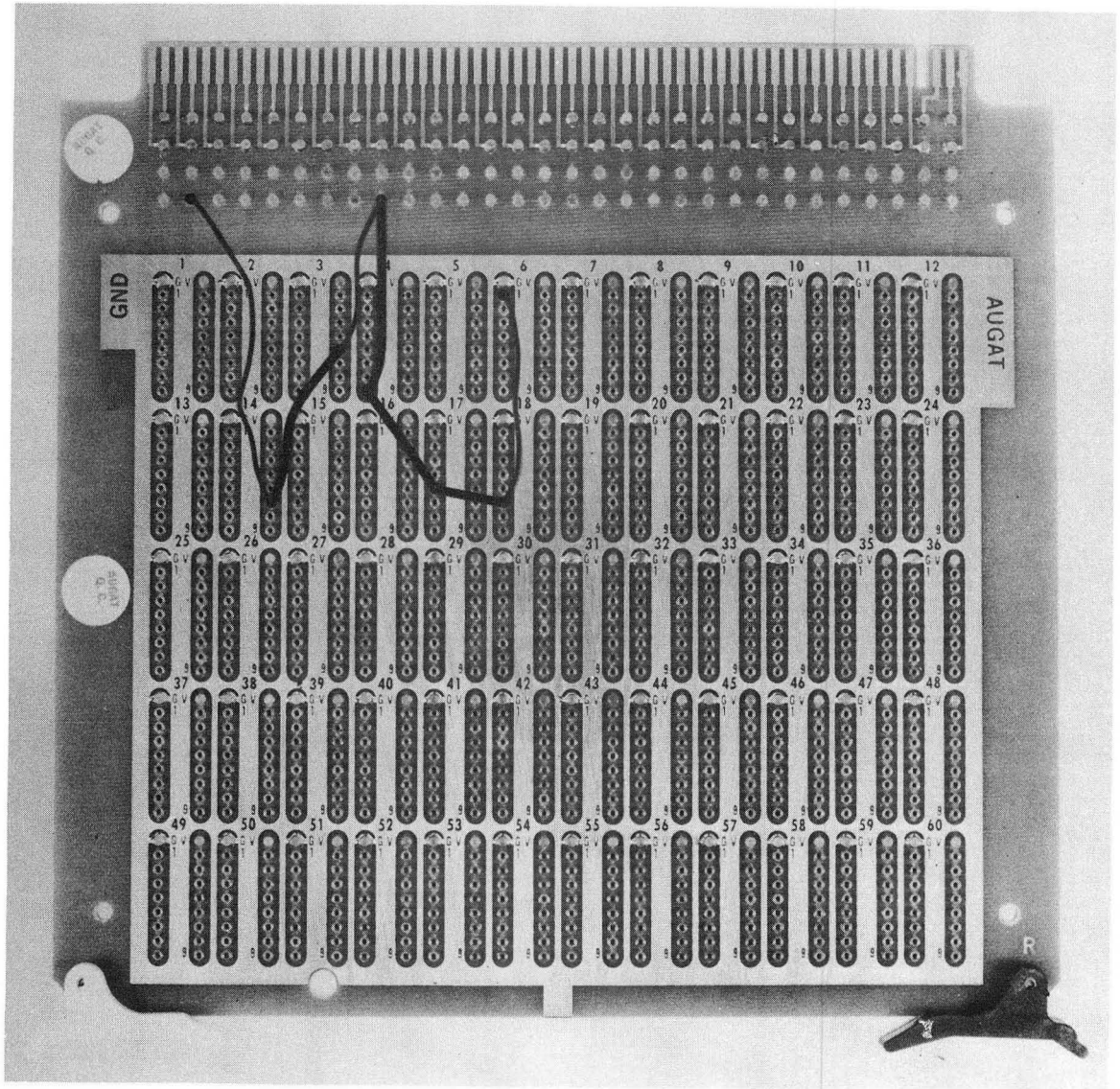


Fig. 4. At the end of Pass 3, edge pins have been connected to nearby columns. Pins interval to previously generated signal strings are not shown.



Fig. 5. The board is completely wired.



0 0 0 0 3 7 0 4 4 1 0

A P P E N D I X 1

```

*16PIN
*SOCKET      19301
IN1          IN2
$OUT2       $OUT1
*14PIN
*SOCKET      24601
GND          STROBE                $*STROBE

*BUSS        5+5V
*BUSS        10GND
*NDLIST
*SOCKET      137491V

*STROBE $CLOCK1 CLOCK1 $ALPHA
*SOCKET  147491V

*STROBE $CLOCK2 CLOCK2 $BETA
*EDGE   1
$+5V    $GND    $IN1    $IN2    OUT1    OUT2    $STROBE *STROBE
*LINK
*CARD
*CLIST
*SLIST
*WLIST
*LENGTH
*PUNCH
*END

```

```

*****
*                                     *
*   PROGRAM DESCRIPTION               *
*                                     *
*****

```

AUGAT IS A PROGRAM INTENDED FOR WIRE ROUTING AND DOCUMENTATION INVOLVING AUGAT CARDS OR EQUIVALENT COMPONENTS. THAT IS, EACH CONNECTOR (SOCKET) HAS ASSOCIATED WITH IT 18 INDEPENDENT PINS, IN TWO COLUMNS OF 9 EACH. THESE ARE NUMBERED (V, 1, 2, ..., 7, 8) AND (G, 16, 15, ..., 9, 8). THESE SOCKETS APPEAR IN 5 ROWS OF 12 SOCKETS EACH.

SOCKETS ARE NUMBERED FROM 1-60.

IT IS NECESSARY TO SPECIFY THE LOCATION OF EACH SOCKET WITHIN A CARD, AND THE SIGNALS PRESENT ON EACH PIN. AT THE COMMAND \*LINK, A CONNECTION IS DESCRIBED BETWEEN IDENTICAL SIGNALS WITHIN A SOCKET, SUCH THAT THE WIRES RUN FROM ONE END OF THE SOCKET TO THE OTHER, FORMING SIGNAL STRINGS. THEN ALL LIKE SIGNAL STRINGS WITHIN A COLUMN ARE JOINED, MINIMIZING WIRE LENGTHS, AND FINALLY ALL COLUMNS ARE WIRED TOGETHER. THE ALGORITHM USED PROVIDES THAT NO PIN SHALL HAVE MORE THAN TWO WIRES ATTACHED. WHILE THIS SCHEME IS NOT NECESSARILY THE MOST EFFICIENT IN TERMS OF WIRE LENGTH, MAINTAINANCE IS ENHANCED.

FOR CONVENIENCE, DEFAULT CONDITIONS ARE BUILT INTO THE PROGRAM. EACH SOCKET USED HAS 'GND' AND '+5V' DEFINED. THESE MAY BE OVERWRITTEN IF DESIRED, AS DESCRIBED BELOW. INITIAL SOCKET INPUT MODE IS 16-PIN. IF PARAMETER 1 OR PARAMETER 2 ARE UNDEFINED OR 0, THE VALUE 1 WILL BE USED.

CONTROL IS PROVIDED BY CONTROL CARDS, IDENTIFIED BY AN ASTERISK (\*) IN COLUMN 1. THESE CONTROLS ARE BY MNEMONIC, WHICH MUST START IN COLUMN 2, CONTAIN NO IMBEDDED BLANKS, AND HAVE TRAILING BLANKS FOR A TOTAL OF 8 CHARACTERS. CONTROLS ARE--

* CONTROL	PARAM 1	PARAM 2	DESCRIPTION
A1 A8	I3	A8	FORMAT
* FND	---	---	TERMINATE PROGRAM
* RESTART	---	---	REINITIALIZE FOR MORE DATA
* NDLIST	---	---	CONTROL CARD PRINTING IS SUPPRESSED
* LIST	---	---	DO NOT SUPPRESS LISTING
* EDGE	N	---	READ UP TO 10 SIGNALS FOR EDGE PINS STARTING AT PIN N
* 8PIN	---	---	SIGNAL SEQUENCE IS FOR 8-PIN DUAL-IN-LINE I. C.
* 14PIN	---	---	SIGNAL SEQUENCE IS FOR 14-PIN DUAL-IN-LINE I. C.
* 16PIN	---	---	SIGNAL SEQUENCE IS FOR 16-PIN DUAL-IN-LINE I. C.
* CARD	---	---	PROVIDE A MAP OF POSITIONS ON CARD
* CLIST	---	---	PROVIDE A LIST BY SOCKETS
* SLIST	---	---	PROVIDE A LIST BY SIGNALS
* WLIST	---	---	PROVIDE A WIRE LIST
* PUNCH	---	---	PUNCH A PAPER TAPE FOR AUTO-WIREWRAP
* LENGTH	---	---	PROVIDE WIRE LENGTH LIST

* BUSS	N	SIGNAL	DECLARE SIGNAL TO BE BUSSED AT PIN N (APPLIES ONLY TO *+5V* AND *GND* )
* LINK	---	---	CAUSES ALL SIGNALS AND SIGNAL STRINGS TO BE LINKED TOGETHER
* RESERVE	SOCKET NO	---	DECLARE SOCKET RESERVED
* SOCKET	SOCKET NO	I. D.	SEE BELOW

\*SOCKET CONTROL CARDS MUST BE FOLLOWED BY 1 OR 2 CARDS CONTAINING SIGNAL NAMES, IN 10A8 FORMAT. INPUT IS IN PREVAILING MODE (8, 14, OR 16-PIN). ANY CHARACTERS ARE LEGAL IN A SIGNAL NAME, AND ALL PINS WITH IDENTICAL NAMES WILL BE WIRED TOGETHER. ONE SPECIAL CASE IS THAT OF A BLANK NAME. IF BLANK, ANY SIGNAL ALREADY ASSIGNED TO A PIN REMAINS ASSIGNED. (THIS FEATURE PERMITS DEFAULT SPECIFICATION OF GND AND +5V.) A SECOND CASE IS A SIGNAL STARTING WITH THE CHARACTER \$. \$ INDICATES A SIGNAL SOURCE, AND THUS \$SIG IS TREATED AS THE SOURCE OF SIG, AND IS OTHERWISE IDENTICAL TO SIG.

16PIN -0

SOCKET 19301

SOCKET 1  
TYPE 9301

PARAMETERS INPUT

SIGNAL	PIN	PIN	SIGNAL
IN1	1 0	0 16	+5V
IN2	2 0	0 15	
	3 0	0 14	
	4 0	0 13	
	5 0	0 12	\$OUT1
	6 0	0 11	\$OUT2
	7 0	0 10	
GND	8 0	0 9	

14PIN -0

SOCKET 24601

SOCKET 2  
TYPE 4601

PARAMETERS INPUT

SIGNAL	PIN	PIN	SIGNAL
GND	1 0	0 14	+5V
STROBE	2 0	0 13	
	3 0	0 12	
	4 0	0 11	
	5 0	0 10	
*\$STROBE	6 0	0 9	
GND	7 0	0 8	

BUSS 5+5V

BUSS 10GND

NOLIST -0

## SIGNAL LIST, 12 SIGNALS

ALPHA	(\$)	13-14			
BETA	(\$)	14-14			
CLOCK1		13-13	(\$)	13-12	
CLOCK2		14-13	(\$)	14-12	
GND		BUSSED			
IN1	(\$)	3(EDGE)		1-1	
IN2	(\$)	4(EDGE)		1-2	
OUT1		5(EDGE)	(\$)	1-12	13-9
OUT2		6(EDGE)	(\$)	1-11	14-9
STRDRF	(\$)	8(EDGE)		2-2	
+5V		BUSSED			
*STROBE		9(EDGE)	(\$)	2-5	14-11 13-11

NOTE...PIN NUMBERS ARE I.C. PINS, NOT SOCKET PINS

	-FROM-	-TO-	LENGTH		-FROM-	-TO-	LENGTH
1( )	1-16	1-V	.3	2( )	1-V	1(EDGE)	1.3
3( )	1-8	1-G	1.0	4( )	1-G	2(EDGE)	1.4
5( )	2-7	2-1	.8	6( )	2-1	2-G	.3
7( )	13-12	13-G	.8	8( )	2-16	2-V	.3
9( )	14-12	14-G	.8	10( )	13-3	13-V	.6
11( )	13-14	13-15	.3	12( )	14-3	14-V	.6
13( )	1-1	3(EDGE)	1.3	14( )	14-14	14-15	.3
15( )	1-12	5(EDGE)	1.6	16( )	1-2	4(EDGE)	1.6
17( )	1-11	6(EDGE)	1.9	18( )	13-11	1-12	1.3
19( )	2-2	8(EDGE)	1.5	20( )	14-11	1-11	1.5
21( )	14-13	2-6	1.1	22( )	2-6	9(EDGE)	1.9
23( )	13-13	14-13	.5				

PIN NUMBERS ARE SOCKET PINS, NOT I.C. PINS

## WIRE LENGTH LIST, 23 WIRES TOTAL

NUMBER LENGTH

5	.4
1	.6
2	.7
3	.9
1	1.0
1	1.1
3	1.3
1	1.4
1	1.5
3	1.6
2	1.9

BIN NUMBER WIRE (INSULATION) LENGTH REQUIRED

2	.4	5
3	.6	1
4	.8	2
5	1.0	4
6	1.2	1
7	1.4	4
8	1.6	4
10	2.2	2

CARD MAP

23	GND	10	+5V	633	620					
43	IN2	33	INI	653	640					
63	OUT2	50	OUT1	673	660	1	9301	13	7491N	25 *EMPTY*
83	STROBE	70		693	680					37 *EMPTY*
103		93	*STROBE	713	700	2	460I	14	7491N	26 *EMPTY*
123		110		733	720					38 *EMPTY*
143		130		753	740					50 *EMPTY*
163		153		773	760	3	*EMPTY*	15	*EMPTY*	27 *EMPTY*
183		170		793	780					39 *EMPTY*
203		193		813	800	4	*EMPTY*	16	*EMPTY*	28 *EMPTY*
223		210		833	820					40 *EMPTY*
243		233		853	840	5	*EMPTY*	17	*EMPTY*	29 *EMPTY*
263		250		873	860					41 *EMPTY*
283		270		893	880					53 *EMPTY*
303		293		913	900	6	*EMPTY*	18	*EMPTY*	30 *EMPTY*
323		310		930	920					42 *EMPTY*
343		330		953	940					54 *EMPTY*
363		350		973	960	7	*EMPTY*	19	*EMPTY*	31 *EMPTY*
383		370		993	980					43 *EMPTY*
403		390		1013	1000	8	*EMPTY*	20	*EMPTY*	32 *EMPTY*
423		410		1033	1020					44 *EMPTY*
443		433		1053	1040					56 *EMPTY*
463		453		1073	1060	9	*EMPTY*	21	*EMPTY*	33 *EMPTY*
483		470		1093	1080					45 *EMPTY*
503		490		1113	1100	10	*EMPTY*	22	*EMPTY*	34 *EMPTY*
523		510		1133	1120					46 *EMPTY*
543		530		1153	1140					58 *EMPTY*
563		550		1173	1160	11	*EMPTY*	23	*EMPTY*	35 *EMPTY*
583		573		1203	1180					47 *EMPTY*
603		610		1213	1220	12	*EMPTY*	24	*EMPTY*	36 *EMPTY*
										48 *EMPTY*
										60 *EMPTY*

EDGE PINS USED

	PIN	SIGNAL	-FROM-	-TO-
(S)	1	+5V		1-V
(S)	2	GND		1-G
(S)	3	INI		1-1
(S)	4	IN2		1-2
	5	OUT1		1-12
	6	OUT2		1-11
(S)	8	STROBE		2-2
	9	*STROBE		2-6

NOTE ... (S) INDICATES SIGNAL SOURCE

PIN NUMBERS ARE SOCKET PINS, NOT I.C. PINS



SOCKET 1, TYPE 9301  
16-PIN I.C.

SOCKET PIN	SIGNAL	-FROM-	-TO-	I.C. PIN	SOCKET PIN	SIGNAL	-FROM-	-TO-	I.C. PIN
G	GND	2 (EDGE)	1-8		V	+5V	1 (EDGE)	1-16	
1	IN1	3 (EDGE)		1	16	+5V	1-V		16
2	IN2	4 (EDGE)		2	15				15
3				3	14				14
4				4	13				13
5				5	(S) 12	OUT1	5 (EDGE)	13-11	12
6				6	(S) 11	OUT2	6 (EDGE)	14-11	11
7				7	10				10
8	GND	1-G		8	9				9

SOCKET 2, TYPE 4501  
14-PIN I.C.

SOCKET PIN	SIGNAL	-FROM-	-TO-	I.C. PIN	SOCKET PIN	SIGNAL	-FROM-	-TO-	I.C. PIN
G	GND		2-1		V	+5V		2-16	
1	GND	2-G	2-7	1	16	+5V	2-V		14
2	STROBE	8 (EDGE)		2	15				13
3				3	14				12
4				4	13				11
5				5	12				10
(S) 6	*STROBE	9 (EDGE)	14-13	6	11				9
7	GND	2-1		7	10				8
8					9				

SOCKET 13, TYPE 7491N  
14-PIN I.C.

SOCKET					SOCKET				
PIN	SIGNAL	-FROM-	-TO-	I.C. PIN	PIN	SIGNAL	-FROM-	-TO-	I.C. PIN
G	GND		13-12	1	V	+5V		13-3	
1				2	(S) 16	ALPHA			14
2				3	15	CLOCK1		13-14	13
3	+5V	13-V		4	(S) 14	CLOCK1	13-15		12
4				5	13	*STROBE	14-13		11
5				6	12	GND	13-G		10
6				7	11	OUT1	1-12		9
7					10				8
8					9				

SOCKET 14, TYPE 7491N  
14-PIN I.C.

SOCKET					SOCKET				
PIN	SIGNAL	-FROM-	-TO-	I.C. PIN	PIN	SIGNAL	-FROM-	-TO-	I.C. PIN
G	GND		14-12	1	V	+5V		14-3	
1				2	(S) 16	BETA			14
2				3	15	CLOCK2		14-14	13
3	+5V	14-V		4	(S) 14	CLOCK2	14-15		12
4				5	13	*STROBE	2-6	13-13	11
5				6	12	GND	14-G		10
6				7	11	OUT2	1-11		9
7					10				8
8					9				

## LEGAL NOTICE

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