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Authors

Mukim, Prashansa
Dalakoti, Aditya
McCarthy, David
et al.

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Distributed Pulse Rotary Traveling Wave VCO: Architecture and Design

Prashansa Mukim, Aditya Dalakoti, David McCarthy, Brandon Pon, Carrie Segal, Merritt Miller,
James F. Buckwalter and Forrest Brewer
Department of Electrical and Computer Engineering
University of California Santa Barbara
Santa Barbara, U.S.A.
E-mail: {prashansa_mukim, adityadalakoti, davidmccarthy, bapon, chsegal, merrittmiller, buckwalter, forrest}@ucsb.edu

***Abstract*—This paper describes the architecture and design of pulse rotary traveling wave voltage controlled oscillators that preserve wave shape, and thus wave harmonics using non-linear amplification. These oscillators can provide multiple low duty-cycle clock phases and allow for the same clock phase to be present at multiple physical locations. A design fabricated in GFUS 130nm (8RF) technology operates at 5.32 GHz with a 10 MHz offset phase noise of -128.15 dBc/Hz at 45.4 mW while generating 12 driven phase outputs with 15.66 ps phase resolution and less than 500 fs cycle-to-cycle jitter. The clock can be coarse or fine tuned within a frequency range of 4.35 GHz to 5.4 GHz with K_{VCO} of 1.7 GHz/V and 470 MHz/V respectively. The positive start-up mechanism of the oscillator minimizes transmission line reflections and allowing maintenance of the traveling wave shape, yielding an average 3 dB figure of merit improvement over existing designs.**

***Index Terms*—Voltage Controlled Oscillator (VCO); Rotary Traveling Wave Oscillator (RTWO); pulse oscillator; transmission line stabilization; low duty-cycle multi-phase oscillator**

I. Introduction

High precision, low phase noise, multi-phase voltage controlled oscillators are needed in many RF applications ranging from radio links to ADCs. In particular, low jitter, low skew timing distribution is required for mixer first receiver architectures and N-Path filters [1] [2]. Key features needed in such designs are full swing, non-overlapping and less than 25% duty cycle clock drivers. Transmission-line stabilized clock distribution offers a viable method to produce such low skew, multi-phase VCOs. Transmission line systems such as salphasic distribution [3] and distributed transmission line amplification [4] provide sinusoidal or semi-sinusoidal clocks. They achieve fast clocking edges using additional buffering, unfortunately adding to the delivered jitter and power requirements. Rotary traveling wave oscillators (RTWO), which have been well analyzed [5] [6] overcome these challenges. However, such designs provide limited signal swings and do not provide non-overlapping clock phases. This limits the utility of these oscillators for designs of mixer-first receivers and similar circuits.

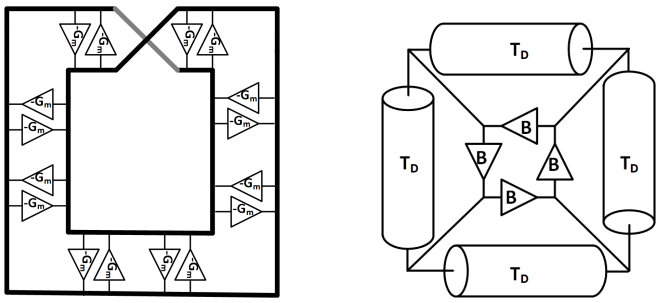
Previous studies on pulsed wave oscillators using linear transmission line elements demonstrated good phase noise properties [7]. These oscillators are implemented using off-chip, low-loss elements. A different implementation [8] demonstrated an on-chip transmission line pulsed wave oscillator. That design used distributed pulse regenerating amplifiers to counter comparatively high loss on-chip transmission line elements to obtain an oscillator that operates at 3.02 GHz but required 68.7 mW of power consumption. In this work, systematic design and architecture of a low-power, full-swing pulsed rotary wave VCO is presented. The presented design operates at about 80% higher frequency while consuming substantially less power than in [8], resulting in a $\approx 3\ dB$ figure of merit improvement. It utilizes non-linear, full-swing, limiting amplifier stages to maintain the wave shape of a unidirectional, low-duty cycle, fast-slope traveling pulse. Since the event sampling accuracy directly relates to the slope of the clock edge, the presented high-slope pulsed rotary wave VCO is an ideal candidate for accurately capturing event timing at low injected jitter. Further, applications requiring timing distribution, or non-overlapping, low duty-cycle multi-phase clocks can effectively utilize these designs. Although the presented oscillator operates at 5.32 GHz, it provides 12-clock phases, and hence can be potentially used for capturing or synchronizing events at a much higher effective rates.

The main contributions of this paper are as following: (1) A pulsed RTWO fabricated in GFUS 130 nm (8RF) technology is presented that preserves the slope of the traveling pulse and provides 12-low-duty cycle clock phases. (2) A method to reliably start-up the oscillator is presented. The start-up methodology aids in both - lowering the power consumption, as well as maintenance of wave shape by minimizing reflections. (3) Design constraints and methods for tuning of parameters such as oscillator frequency, phase-stability and power are discussed. (4) Techniques for stable multi-pulse (overtone) behavior are described that enable a unique architectural feature: the same phase is available at multiple physical locations of the oscillator. This feature can be utilized for timing distribution and synchronization.

II. Oscillator Architecture

Conventional RTWOs have differential amplifiers along a transmission line loop (Fig. 1a). The amplifiers are always connected to diagonally opposite ends of a transmission line. It is not possible to get non-overlapping clock output taps from the propagating wave in the loop. Also, no two locations

along the loop have the same phase. On the other hand, the pulse RTWO (Fig. 1b) allows propagation of a unidirectional pulse around the transmission line loop. Pulse regenerating amplifiers (labeled "B") are used to compensate for losses and create a pulse traveling wave. Multiple low-duty cycle, non-overlapping clock phases can be tapped from the transmission line. By propagating more than one pulse around the loop, it is possible to obtain identical phases at different loop locations. There are easy to satisfy circuit conditions which enforce uniform clock pulse spacing for multi-pulse clocks [9] .



(a) (b)

Fig. 1: (a) Conventional RTWO (b) Pulse RTWO

Consider the segment shown in Fig.2. A pulse V_1 at the input of the segment goes through the transmission line and comes out as V_{1T} after delay T_D. The amplifier also generates an output pulse V_{1B}, after delay T_B. In stable operation, the amplifier output compensates for the loss in the corresponding transmission line segment. An output waveform V_2 is produced, that is the superposition of the two waves V_{1B} and V_{1T}. The shape of the output waveform is dependent on the relative phase difference of the two superposing pulses ($T_D - T_B$).

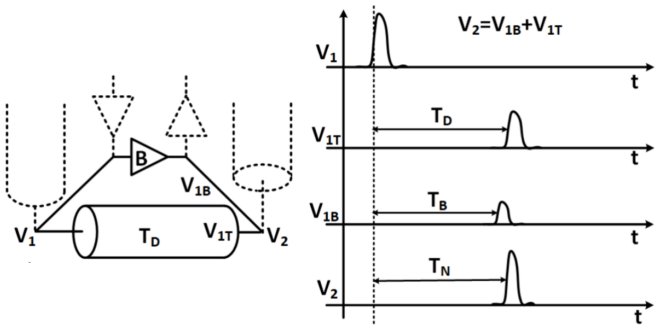
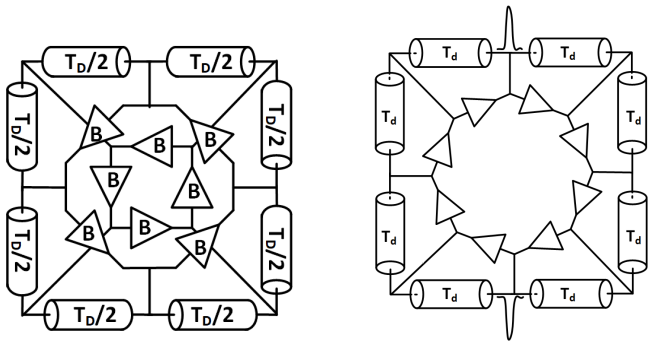


Fig. 2: Pulse wave along a distributed transmission line

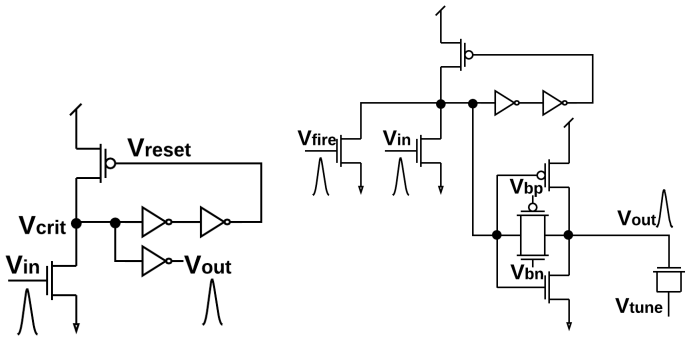
The pulse RTWO consists of one or more copies of the pulse amplifier, connected in parallel to a transmission line segment, with drive that is enough to compensate for loss and time delay that meets the phasing constraints for regeneration (Fig.2). The pulse amplifier stages, by design, have a forward propagation delay that is roughly 1/4 of their reset time. The local transmission line segments are timed so that $T_D \approx T_B$, the condition where most of the amplifier power is in-phase with the transmission line wave. The portion of the output wave traveling in the reverse direction arrives at the input of the previous stage when the pulse amplifier is in its reset phase. It arrives too early to re-trigger the amplifier, thus suppressing the reflected wave. The pulse then propagates in a single direction (either clockwise or counter clockwise), set by the physical connectivity between amplifiers and transmission line segments. Fortunately, the required timing conditions are easy to meet, allowing stable operation over a fairly wide range of voltages and device variations.

The pulse RTWO architecture allows for several design alternatives to meet specific goals. For example, it is possible to interleave the amplifiers (Fig.3a), such that the transmission line is driven more frequently by smaller amplifiers. This results in a more uniform drive and availability of more phase taps from the buffer outputs. Another topology can have multiple pulses stored in the transmission line (Fig. 3b), allowing identical phases to be present at more than one physical location on the ring. This feature can aid in clock distribution networks where identical clock phases can be utilized without the extra jitter and skew associated with timing distribution. Multi-pulse stability and uniform timing distribution is maintained by the interaction between pulses in pulse amplifier circuits [9].



(a) (b)

Fig. 3: (a) Interleaved pulse RTWO (b) 2-Pulse RTWO



(a) (b)

Fig. 4: (a) Pulse amplifier (b) Pulse amplifier with added resistive feedback, fire input and fine tuning input

III. Oscillator Design

A. Pulse Amplifier

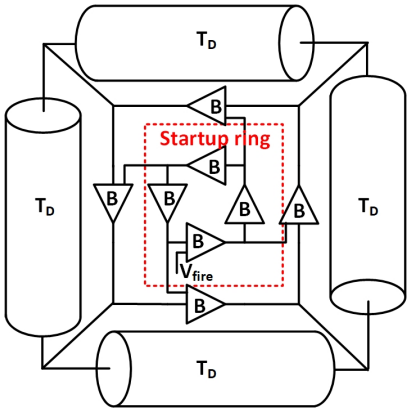
The non-linear pulse amplifiers (Fig. 4a) are self-reseting pulse gates. V_{crit} is pulled down on the rising edge of the signal at V_{in}. This pulls up V_{out} and pulls down V_{reset}, causing the PMOS to pull up V_{crit}, which causes V_{out} to pull down. The output pulse shape is set by the internal reset loop as long as the input pulse does not persist longer than the reset time, and hence is relatively insensitive to the input pulse shape or amplitude. After the pulse output, but before the reset has concluded, the input is insensitive to further pulses and the output is low impedance to ground, suppressing the reverse wave in the transmission line. The pulse RTWO uses the pulse amplifier shown in Fig. 4b, that contains additional inputs V_{fire}, V_{bp} and V_{bn} that aid in oscillator start-up, as explained in the next section. V_{tune} is an analog voltage used for fine control of the oscillator frequency. The supply voltage (V_{dd}) is used as a coarse frequency control knob.

B. Startup Mechanism

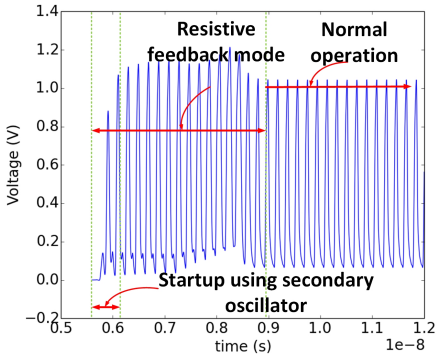
At startup, all the inputs of the pulse amplifiers are low-impedance to ground and there is no energy stored in the transmission line. In order to sustain oscillations in the transmission line, pulses must have sufficient amplitude to trigger the amplifiers. Unfortunately, a single pulse amplifier (Fig. 4a) connected to a transmission line segment cannot create a pulse of sufficiently high amplitude. The output impedance of the amplifier is much higher than the transmission line, in fact it is just sufficient to compensate line loss. The following techniques ensure reliable startup:

1) Resistive Feedback Mode: The pulse amplifier is modified with the addition of a transmission gate as shown in Fig. 4b. Minimum sized PMOS and NMOS are used for the T-gate to ensure that the startup circuitry adds minimum capacitance to the output driver. The feedback resistance thereby achieved is $R_{on-p}||R_{on-n}$ and is relatively high (few KΩ). During startup, V_{bp} is set to *GND* and V_{bn} to V_{dd} externally in the current designs. This connects the input and output of the output inverter through the *T-gate*'s R_{on}, forcing the pulse amplifier into resistive feedback mode and charging the transmission line to $\approx V_{dd}/2$. In this mode, small pulses are amplified so that start-up pulses rapidly grow to the limiting amplitude. After oscillation is established, the amplifier is set to the pulse amplifier mode by removing the feedback.

2) Secondary Start-up Oscillator: A "starter" oscillator with oscillation frequency equal to or slightly faster than RTWO is built via a ring of pulse transmission buffers. This oscillator uses internal delay instead of the stable transmission line. A pulse is then injected into the secondary oscillator at V_{fire} to start it. The outputs of the secondary oscillator drive the V_{fire} inputs of the RTWO amplifiers with correctly matched phases as shown in Fig. 5a. Once the RTWO boots up, the secondary oscillator is disabled. The secondary oscillator has series stacked NMOS at V_{in}. One of the series transistors is switched from V_{dd} to *GND* to disable it. The RTWO output in different startup modes is shown in Fig. 5b.



(a)



(b)

Fig. 5: (a) Start-up circuit (b) Transients at start-up

C. Transmission Line Design

The transmission line structure utilized in the fabricated design is shown in Fig.6. It comprises of $5\mu m$ copper signal lines shielded by $4\mu m$ ground lines spaced $3\mu m$ from the signal lines, with a ground plane underneath at a distance of $4\mu m$. The copper traces are $3\mu m$ thick. For the pulse RTWO fabricated in GFUS 130 nm (8RF) technology, the total transmission line length is $24mm$ built in a serperntine topology as shown in Fig. 7. It occupies a total area of $0.41mm^2$. The transmission line is divided into 12 equal segments of $2mm$ each with a buffer tap (B1-B12) at every $2mm$ segment, connected across a $4mm$ segment. The buffers as well as the secondary start-up oscillator are placed at the centre of the transmission line loop.

D. Simulation Results for a Fully Parasitic-Extracted Design

Post-layout simulation results for the fabricated pulse RTWO are summarized in Table I. The oscillator operates reliably across the different process corners with frequency ranging between 4.65 GHz and 5.4 GHz at the nominal supply voltage. The change in buffer delay as a result of process variations causes the phasing relationship between the buffers and transmission line segments to vary, resulting in change in the shape of the propagating pulse and the oscillation

TABLE I: Simulation results for a fully parasitic extracted design at $V_{dd} = V_{tune}$ = 1.5V

Corner	Frequency (GHz)	Power (mW)	Pulse Width (ps)	Rise Time (ps)	V_{peak} (V)	Phase Noise @ 10 MHz offset (dBc/Hz)
TT	4.98	41.05	57.3	21.2	1.12	-127.5
FF	5.4	42.07	43.8	19.1	1.02	-126.9
SS	4.65	39.6	75.5	24.2	1.12	-125.2
FS	4.94	41.65	57.1	20.4	1.14	-127.7
SF	5	40.03	58.8	22.9	1.09	-127.4

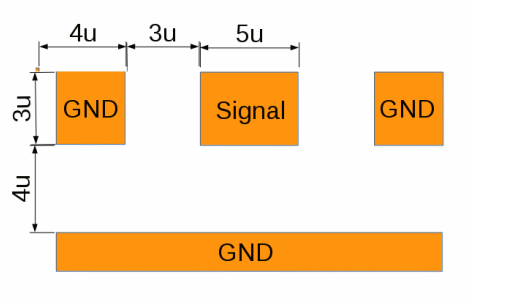


Fig. 6: Transmission line structure

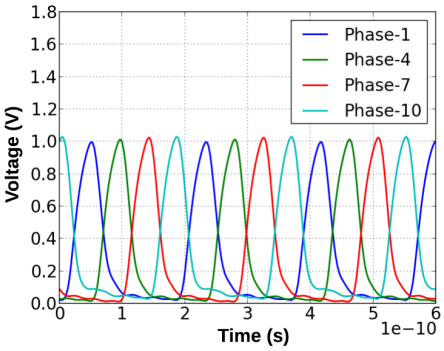


Fig. 8: Waveform showing 4 of 12 clock phases, duty cycle = 27%

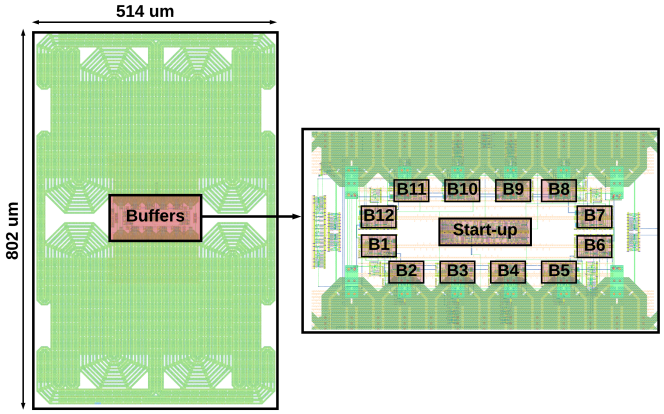


Fig. 7: Oscillator layout: transmission line loop and buffers

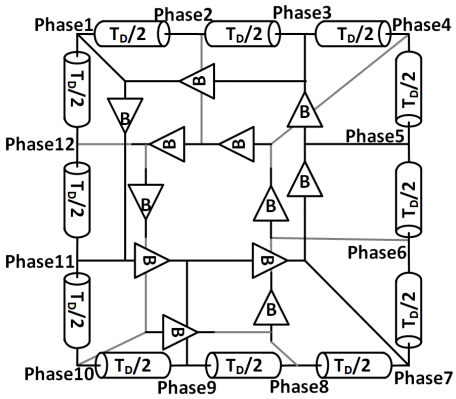


Fig. 9: Interleaved 12 phase pulse RTWO

frequency. Consequently, the phase noise is also affected and can see a worst-case degradation of $\approx 2.5dB$.

Fig. 8 shows the timing of 4 of the 12 total phases of the oscillator under nominal operating conditions. The pulse exhibits a 27% duty cycle. At the typical corner, the simulated oscillator frequency can be tuned in the range of 4.41 GHz to 5.09 GHz for V_{dd} = 1.15V to 1.6V, providing a coarse K_{VCO} = 1.51 GHz/V. Further, at V_{dd} = 1.5V, varying V_{tune} in the range of 0 to 0.6V provides a fine frequency control between 4.61 GHz to 4.93 GHZ, providing a fine K_{VCO} = 543.4 MHz/V.

IV. Design Constraints and Parameters

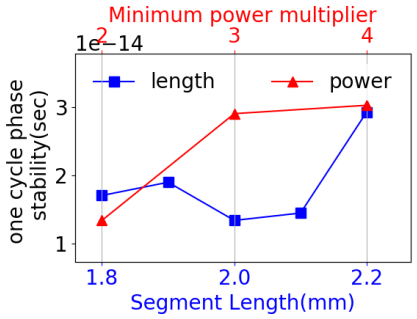
The fabricated RTWO has 12 output phases and a cross-interleaved topology (Fig.9). Design choices were based on performance projections of transient noise simulations on the fully parasitic-extracted design. The two metrics used (based on application specifications) were single-cycle phase stability and integrated 40-cycles phase stability.

Period: Fast rising edges minimize the conversion of voltage noise to time deviations [11]. Setting $T_D \approx T_B$ leads to constructive superposition and maximizes the rising edge slope of the propagating wave. Thus, the period of the oscillator is largely dependent on the total transmission line length, with gain elements added at the appropriate intervals. The phasing of the transmission line and amplifier impacts both power and noise as can be seen from the simulation results.

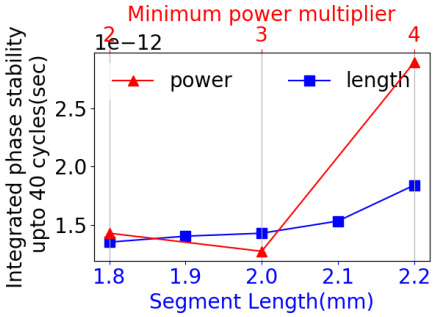
Buffered Segment Lengths: The maximum functioning transmission line length is determined by simulating the performance of minimum sized buffers and analyzing the performance across a number of possible single segment lengths. The single cycle stability, as impacted by the transmission line segment length is shown in Fig. 10a. The length of $2mm$ per segment is ideal for achieving best single cycle phase stability. On the other hand, integrated phase stability in Fig. 10b can

TABLE II: Comparison of pulse RTWO with other free running RTWOs

Ref	Technology	Phase Noise	Frequency	Power	Tuning Range
This Work	CMOS 130nm	-128.15dBc/Hz@10MHz	5.32 GHz	14.7mW-48.8mW	4.35-5.4 GHz
[5]	CMOS 130nm	-134dBc/Hz@3MHz	2 GHz	30.2mW	1.7-2 GHz
[6]	CMOS 110nm	-140.8dBc/Hz@3MHz	3.05 GHz	52.8mW	3.05-3.65 GHz
[8]	CMOS 130nm	-131.75dBc/Hz@10MHz	2.93 GHz	34.75mW-68.7mW	2.53-3.02 GHz
[10]	CMOS 110nm	-134dBc/Hz@3MHz	3.5 GHz	90mW	2.6-4.25 GHz



(a)



(b)

Fig. 10: (Smaller value of phase stability is better)(a) Single-cycle phase stability (b) 40-cycles integrated phase stability

be seen to grow with segment length. For the fabricated pulse RTWO $2mm$ was chosen to be the transmission line segment length in order to achieve low cycle-cycle jitter and relatively small integrated 40-cycle jitter. The forward pulse buffer delay is greater than the propagation delay of a $2mm$ transmission line segment, thus the design needs interleaving to support both correct phasing and the attenuation characteristics of the transmission line.

Power: In simulation, a $24mm$ transmission line required 2 parallel minimum sized buffers to reliably maintain oscillations. This assumes the transmission line is divided into 12 segments with a buffer every $2mm$, connected across a $4mm$ segment. As can be seen from Fig. 10a, single cycle phase stability is best at minimum operational power. Integrated phase stability in Fig. 10b is nearly constant for buffer multipliers of 2 and 3 but is considerably worse for multiplier of 4. This is due to the fact that the high wave slope is maintained as a design constraint and is not improved

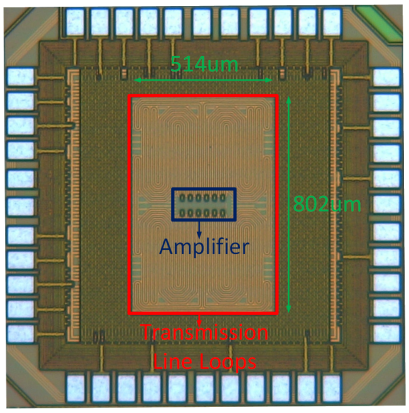


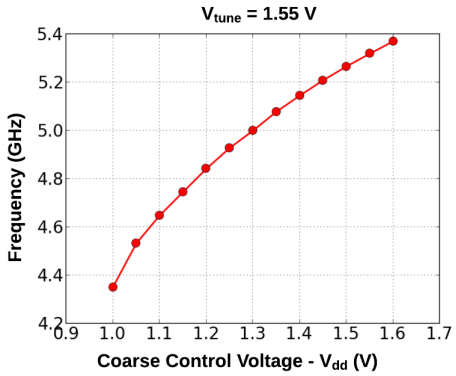
Fig. 11: Die micrograph

by over-sizing buffers. Hence a multiplier of 2 was chosen in the final design, which also causes the power consumption to be lower.

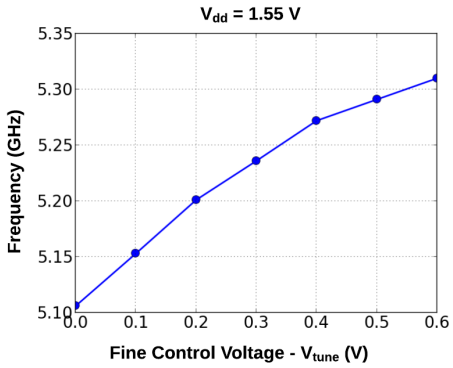
V. Results

The pulse RTWO fabricated in GFUS 130 nm (8RF) operates at 5.32 GHz ($V_{dd} = 1.5V$) with a $24mm$ transmission line length, $0.41mm^2$ area and 12 output phases. Fig. 11 shows the die micrograph of the fabricated oscillator chip ($1.5mm \times 1.5mm$). Voltage controlled frequency responses obtained by tuning V_{dd} and V_{tune} are shown in Fig. 12. The tunable frequency range of the oscillator is 4.35 GHz to 5.4 GHz with coarse and fine K_{VCO} of 1.7 GHz/V and 470 MHZ/V respectively for $V_{dd} =$ 1V to 1.6V and $V_{tune} =$ 0 to 0.6V. The corresponding power consumption lies in the range of 14.7 mW to 48.8 mW.

Phase noise measurements were done using Keysight PXA signal analyzer N9030B, 3 Hz-26.5 GHz. Fig. 13a shows the phase noise of the pulse RTWO operating at $V_{dd} = V_{tune} =$ 1.55V for offset frequencies between 100 Hz and 100 MHz. Fig. 13b shows the 10 MHz offset phase noise across the operational frequency range of the pulse RTWO. The improvement in phase noise for higher frequencies is due to the operation of the oscillator at a higher value of V_{dd}, resulting in stronger compensation of loss by the buffers and a higher amplitude traveling pulse wave. As shown in Table II, although the fabricated RTWO operates at a higher frequency, it consumes substantially less power, provides a wide tuning range and has a comparable phase noise with other free running RTWOs. In addition, it provides 12 output phases with $\approx 26\%$ duty cycle, 15.66 ps phase resolution and cycle jitter of less that 500 fs.

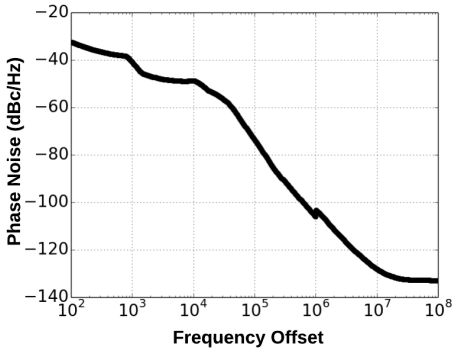


(a)

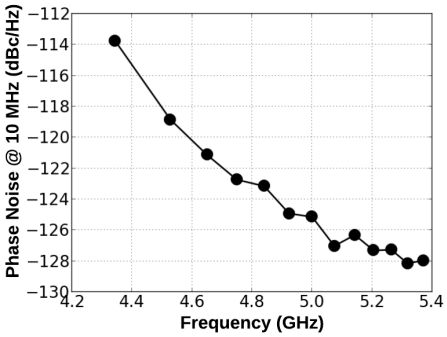


(b)

Fig. 12: Measured voltage controlled frequency (a) Coarse (b) Fine



(a)



(b)

Fig. 13: (a) Measured Phase Noise at $V_{dd} = 1.55V, V_{tune} = 1.55V$ (b) Phase Noise as a function of operating frequency

VI. Conclusion

This paper presents an on-chip low-power pulse RTWO that utilizes distributed non-linear pulse amplifiers for compensating transmission line loss. It involves propagation of a high slope pulse around the transmission line loop. The design achieves low phase noise at low power by ensuring that the superposition of the compensating buffers' output and traveling wave maximizes the wave slope. It provides a technique for low duty-cycle, full-swing, multi-phase clocking, that avoids additional power costs associated with timing distribution and is useful for applications ranging from clock data recovery to ADCs.

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