UNIVERSITY OF CALIFORNIA, SAN DIEGO

Compact Modeling of Quantum Effects in Double Gate MOSFETs

A dissertation submitted in partial satisfaction of the

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Electrical Engineering (Applied Physics)

by

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2007

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in quality and form for publication on microfilm:

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DEDICATION

This dissertation is dedicated to my lovely wife Ying..

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ABSTRACT OF THE DISSERTATION

Compact Modeling of Quantum Effects in Double-gate MOSFETs

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Professor Yuan Taur, Chair

As CMOS scales down to the limits imposed by oxide tunneling and voltage non-scaling, double-gate (DG) MOSFET has become a subject of intense VLSI research. In this dissertation, quantum effects were investigated in both long channel and short channel Double-Gate MOSFETs.

A 1-D numerical Poisson-Schrodinger solver was developed for the quantum solutions in DG MOS structure. The solver can be expanded for the current characteristics of DG MOSFETs because of equivalent influence of the quasi-Fermi potential and the gate voltage on the inversion charge density. Through extension

solutions in symmetric DG MOSFETs, quantum effects induced threshold voltage shift was expressed as a close form function of the silicon thickness based on a physical approximation. The gate capacitance degradation due to quantum effects was modeled by the inversion layer thickness change, which can be extracted from the inversion charge density. Quantum $I - V$ and $C - V$ characteristics were generated by the analytical classical potential model with the threshold voltage and gate capacitance degradation implemented as quantum corrections.

Complicated quantum mechanical behavior of electrons in asymmetric DG MOSFETs was investigated. The threshold voltage shift can be calculated with the electron ground state energy calculated through different methods. An equivalent small-signal capacitance circuit was developed to model the charge coupling between the two gates and inversion channels. The capacitance model was valid for different types of DG MOSFETs and different operation region.

A 2-D analytical potential solution to the Poisson's equation was incorporated into the Schrodinger equation for the quantum solutions in short channel DG MOSFETs. With the eigen energies calculated through the perturbation method, quantum subthreshold current was calculated. The results agreed well with the simulated data by an iteration procedure. The quantum threshold voltage shift and sunthreshold slope in short channel DG MOSFETs were expressed as close functions of device parameters and bias, which can easily be implemented into the classical model.

Chapter 1 Introduction

1.1 Introduction to CMOS Scaling

Since the invention of the metal-oxide-semiconductor field-effect transistor (MOSFET), CMOS has been the driving engine of the semiconductor industry because of its successful incorporation into the integrated circuits (ICs). CMOS technology evolution in the past few decades has followed the path of device scaling to achieve density, speed and power improvement. As indicated by the Moore's law [1], the number of transistors inside chips doubles every two years because of the shrinking size of MOSFETs. It is well known that reducing the source-to-drain spacing, i.e., the channel length of a MOSFET, increases the driving current in the channel. Other than that, it also leads to the short-channel-effects (SCE) [2]. The most undesirable short-channel-effect for digital application is a reduction in the gate threshold voltage (V_t) at which the device turns on, especially at high drain voltage. The reduced gate threshold voltage causes the subthreshold leakage current to increase dramatically, which makes the device difficult to turn off. Full realization of the benefits of the new high-resolution lithographic techniques therefore requires the development of new device designs, technologies, and the structures that can keep the short-channel-effects under control at very small dimensions.

The scaling concept is schematically illustrated in Figure 1.1, in which the device dimension (both horizontal and vertical) and the device voltages are scaled by the same factor to keep the electrical field inside the device constant.

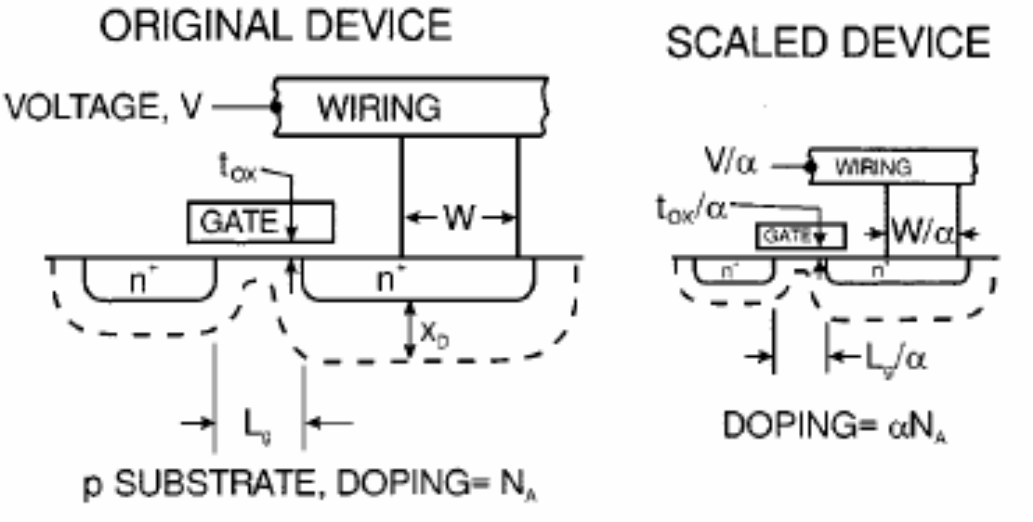


Figure1.1 Schematic illustration of the scaling principle of silicon technology. (Adapted from [3]).

The reduction of the vertical dimension of MOSFETS, i.e., the gate oxide thickness, enhances the gate control over the channel, which improves the short-channel behavior. Thin oxide also improves the driving capability of MOSFETs. However, ultrathin gate oxide will lead to high gate leakage current due to direct tunneling. Alternative gate dielectric materials with higher permittivity (high-K) than SiO2 [4] have been exploited to increase the physical thickness while maintaining the same effective-oxide-thickness (EOT). It is also illustrated that the well doping concentration is also scaled up by the same factor. In deep submicron, non-uniform well doping profiles in both vertical and lateral direction are developed for the suppression [5-6]. Super steep retrograde channel doping [7], which is made possible by the ion implantation, gives the device designer an additional degree of freedom to tailor the profile for meeting both the threshold voltage and off-current requirement. In lateral direction, more highly doped regions near the two

ends of the channel are beneficial to the suppression of short-channel-effects, since they help to compensate charge-sharing effects from the source-drain fields [8]. Such a self-aligned channel doping is often referred to as *halo* or *pocket* doping [9]. With optimally designed 2-D non-uniform doping profile (superhalo), nearly identical Ion and Ioff for devices of different channel lengths within the process tolerances can be achieved [10].

To improve the MOSFET performance, many other technologies have also been developed such as shallow source/drain extension to reduce the amount of channel depletion charges controlled by the drain [6], a lightly doped drain (LDD) structure [7] to relieve hot-electron reliability problems at high voltages, self-aligned silicide [11] to reduce the channel sheet resistance and the contact resistance, stained Si, Ge or SiGe channels to increase the channel carrier mobility [12], etc.

1.2 Quantum Mechanical Effects in Bulk MOSFETs

Even though constant-field scaling introduced in section 1.1 provides a basic guide line to the design of scaled MOSFETs, reducing the voltage by the same factor as the device physical dimension is too restrictive. The CMOS delay degrades rapidly once the threshold voltage V_t exceeds 25% of the power supply voltage V_{dd}. When V_{dd} is reduced toward shorter channel length, it becomes increasing difficult to satisfy both the performance and off-current requirements. Another reason is the reluctance to depart from the standardized voltage levels of the previous generation. The general trend is that V_{dd} has not been scaled down in proportion to the oxide thickness t_{ox}, and V_t has not been scaled down in proportion to V_{dd}, as is evident in Figure 1.2.

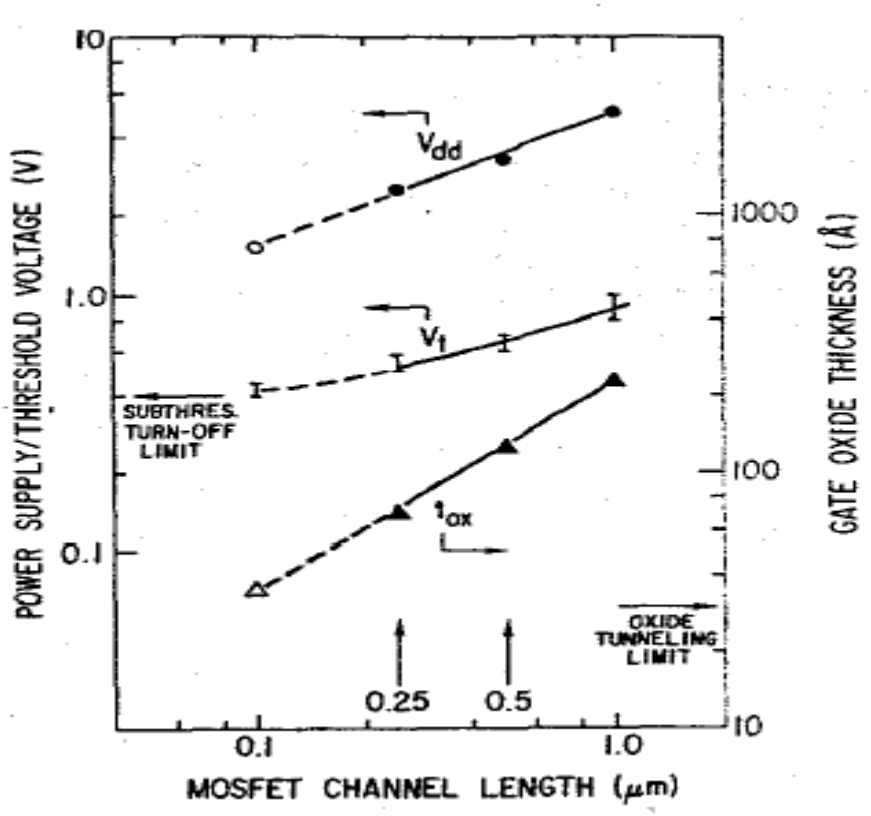


Figure 1.2 Trends of power-supply voltage, threshold voltage, and gate oxide thickness versus channel length for CMOS technologies from 1 μm to 0.1 μm (Adapted from [13]).

As a result, the operating electric field in MOSFETs becomes higher accompanying the device scaling. In the presence of such a high electric field, significant carrier quantization is observable in the MOFETs. Also well known is that in the inversion layer of a MOSFET, carriers are confined in a potential well close to the surface. The well is formed by the silicon conduction band which bends down severely toward the surface due to the gate field and the oxide barrier which is essentially infinity for the inversion carriers. Because of the confinement of motion in the direction perpendicular to the surface, one should treat the inversion electrons quantum mechanically as a 2-D electron gas [14]. The quantum mechanical behavior of inversion electrons differs from their classical behavior significantly. Due to the quantization, the electron energy levels are

grouped in discrete subbands in the normal direction instead of classical 3-D continuous energy states.

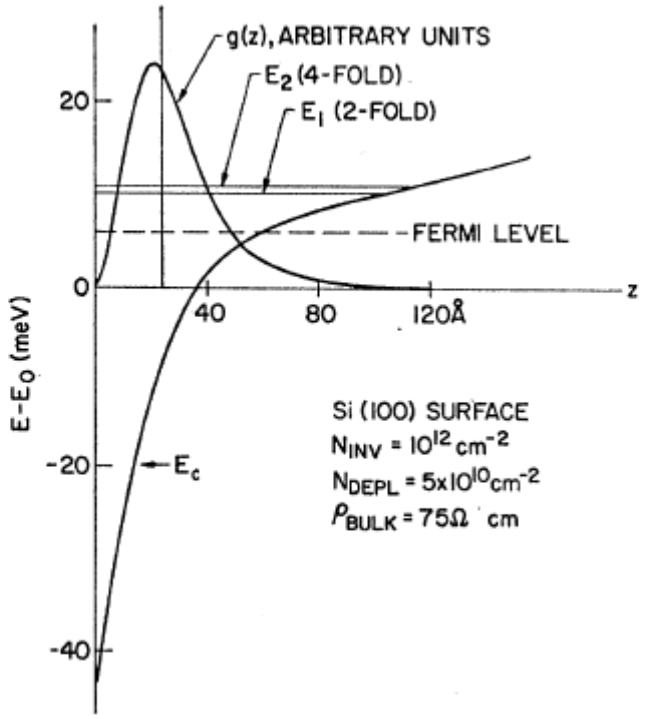


Figure 1.3 Surface potential well and surface charge distribution for a representative Si surface. The ground state is about 40 mev above the bottom of the conduction band. The dashed line indicates the Fermi level in the inversion layer (Adapted from [14]).

As shown in Figure 1.3, even the lowest subband is some energy (40mev in this case) above the bottom of the silicon conduction band. On the other hand, the wave function must be zero at the surface where the potential barrier is infinity. As a consequence, the electron concentration is also zero in the surface and therefore peaks below the surface, which is contrast to the classical model as shown in Figure 1.4.

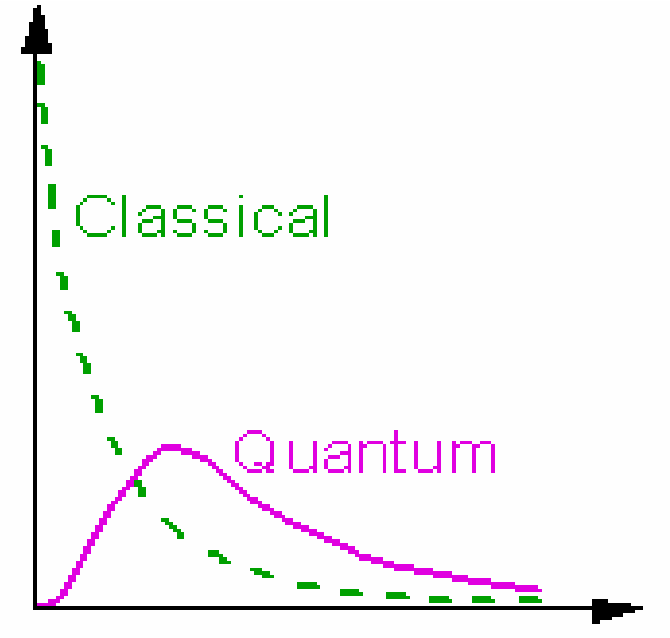


Figure 1.4 Schematic diagram of the classical and quantum inversion charge distribution in the direction perpendicular to the silicon-oxide surface.

Quantum effects of the inversion electrons affect MOSFET operation in two aspects. First of all, since the electrons occupy at subbands above the bottom of the silicon conduction band, more band bending is required to populate even the lowest subband and therefore the threshold voltage becomes higher. Second of all, the inversion layer forming below the surface suggests the finite inversion layer thickness and thus reduces the total gate capacitance. This reduces the transconductance and the current drive of a MOSFET since it needs higher gate voltage to produce a given level of inversion charge density.

Quantum effects in MOSFETs have been studied extensively since 1970's. A full solution of the silicon inversion electron can be obtained by solving coupled Poisson's and Schrodinger equations self-consistently [14-17] during which a numerical method must be used. However, a simplified method is possible under subthreshold conditions. First, it is reasonable to decouple the two equations because of low inversion charge

density. Since band bending is solely determined b the depletion charge, the electric field can then be treated nearly constant (ε_s). Therefore, it is a good approximation to consider the quantum well as composed of an infinite oxide barrier for $x < 0$, and a triangular potential $V(x) = q\varepsilon_s x$ for $x > 0$. The solutions of Schrodinger equation are Airy functions with eigen values E_j given by [14]

$$E_j = \left[\frac{3hq\mathcal{E}_s}{4\sqrt{2m_x}} \left(j + \frac{3}{4} \right) \right]^{2/3}, \quad j = 0,1,2,... \tag{1.1}$$

where h is Planck's constant and m_x is the effective mass of electrons perpendicular to the surface. For silicon in the <100> direction, there are two groups of energy subbands, or valleys. The lower valley has a two-fold degeneracy ($g = 2$) with $m_x = 0.92m_0$, where m_0 is the free-electron mass. The energy level is designated as E_j. The higher valley has a four-fold degeneracy ($g' = 4$) with $m'_x = 0.19m_0$. The energy levels are designated as

$$E_{j'} = \left[\frac{3hq\mathcal{E}_s}{4\sqrt{2m'_x}} \left(j' + \frac{3}{4} \right) \right]^{2/3}, \quad j' = 0,1,2,... \tag{1.2}$$

With the energy levels in two valleys, the total inversion charge per unit area is expressed as [18]

$$Q_i^{QM} = \frac{4\pi qkTn_i^2}{h^2 N_c N_a} \left(gm_d \sum_j e^{-E_j/kT} + g' m'_d \sum_{j'} e^{-E'_j/kT} \right) e^{q\psi_s/kT} \tag{1.3}$$

where k is the Boltzmann's constant, T is the temperature in Kelvin, n_i and N_a are the intrinsic carrier and doping concentration in silicon, $m_d = 0.19m_0$ and $m_d' = 0.42m_0$ are the density-of-states effective masses of the two valleys and ψ_s is the surface potential.

Note the classical inversion chare density per unit area for the subthreshold region is given by [18]

$$Q_i^{CL} = \frac{kTn_i^2}{\varepsilon_s N_a} e^{q\psi_s/kT} \tag{1.4}$$

When the field is small, both the lowest energy level E_0 and the spacings between the subbands are less than kT at room temperature. A large number of subbands are occupied and Q_i^{QM} is the same as Q_i^{CL}. However, the subbands spacings are larger than kT and only a few lowest energy subbands are occupied. Therefore, Q_i^{QM} is significantly less than Q_i^{CL}. This means that additional band bending $\Delta\psi_s^{QM}$ is required to obtain the same inversion charge density as the classical value. When the field beyond 106 V/cm, only the lowest subband is occupied by electrons, and

$$\Delta\psi_s^{QM} \approx \frac{E_0}{q} - \frac{kT}{q}\ln\left(\frac{8\pi q m_d \varepsilon_s}{h^2 N_c}\right) \tag{1.5}$$

Knowing $\Delta\psi_s^{QM}$, one can easily calculate the threshold voltage shift due to quantum effects

$$\Delta V_t^{QM} = m\Delta\psi_s^{QM} \tag{1.6}$$

where m is the body-effect coefficient of MOEFETs.

Triangular well approximation is one of the most widely used methods for carrier quantization in MOSFETs [19-21]. However, in strong inversion region, the inversion charge density is very high and the triangular potential-well approximation is no longer valid. In the case of high field and only the lowest energy subband is populated, an

approximate expression for the average distance of electrons from the surface was derived through a variational approach [15]

$$x_{av}^{QM} = \left(\frac{9\varepsilon_{si} h^2}{16\pi^2 m_x q Q^*} \right)^{1/3} \tag{1.7}$$

where $Q^* = Q_d + \frac{11}{32} Q_i$ is a combination of the depletion and inversion charge in the channel. Such an inversion layer thickness adds the effective gate oxide thickness about 3-4 Å and effectively reduces the current drive and transconductance of MOSFETs.

1.3 Double-Gate MOSFETs – Advantages and Additional QM Confinement

Through years of technology developments, conventional bulk MOSFET technology is currently progressing to the 45nm regime [22, 23]. It is also believed that CMOS will still be the dominant technology in the near future. However, fundamental and practical scaling limits impose tremendous challenges beyond the 45nm technology node [23-25]. Severe short channel effects come from the nonscaling of the silicon energy. Quantum mechanical tunneling current through the thin gate oxide becomes significant. The random dopant fluctuation effects increase with shrinking device size and leads to threshold voltage variation from device to device. These effects constitute the limiting factors of CMOS scaling at present [26].

Multi-gate MOSFETs, such as Surrounding-gate [27], Pi-gate [28], Omega-gate [29], Tri-gate [30] and Double-gate (DG), have been proposed to be the alternatives for bulk

MOSFETs beyond the 45nm node. Numerical simulation and analytical analysis have shown better scalability of multi-gate MOSFETs over bulk MOSFETs. Among multi-gate MOSFETs, the DG MOSFET is the most promising device structure because it is best compatibile with conventional planar technology although other candidates might have better performance than the DG MOSFETs.

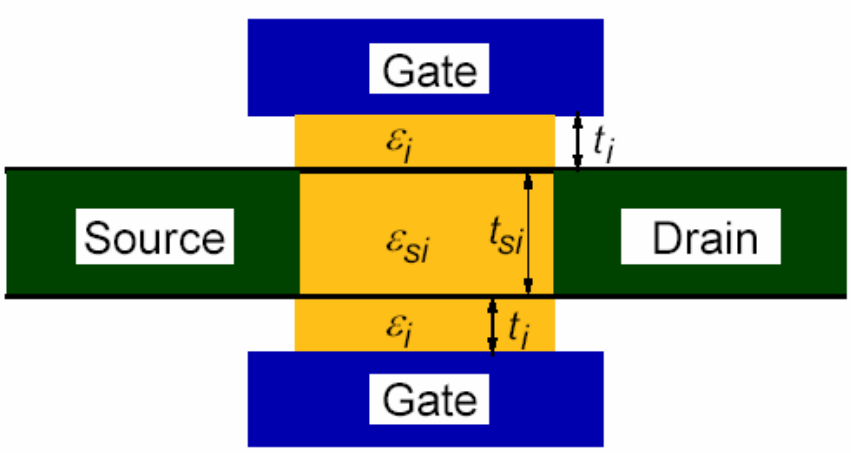


Figure 1.5 Schematic diagram of a double-gate MOSFET

With two gates on the both sides of the channel, DG MOSFET has a better performance than the conventional bulk MOSFET. Figure 1.5 shows the schematic diagram of a double-gate MOSFET. The key benefit of DG MOSFETs is better short channel effects immunity over the bulk MOSFETs. In principle, DG MOSFETs can be scaled to the shortest channel length for a given oxide thickness [31], because the bottom gate can effectively screen the field penetration from the drain, hence suppress the short channel effects. Based on the general scale length theory [32], the threshold voltage roll-off due to short channel effects is proportional to $\exp(-\pi L/2\lambda_1)$, where L is the channel

length and λ_1 is the scale length. Therefore the minimum channel length imposed by short channel effects is ~$2\lambda_1$. The scale length of bulk MOSFETs and DG MOSFETs can be expressed approximately

$$\lambda_1 = W_d + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} \tag{1.8}$$

$$\lambda_1 = t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} 2t_{ox} \tag{1.9}$$

where W_d is the depletion width in bulk MOSFETs, t_{si} is the silicon film thickness and t_{ox} is the gate oxide thickness. Reducing W_d in bulk MOSFETs requires higher doping concentration which results in increased junction capacitance, reduced carrier mobility, degraded subthreshold slope and increased band-to-band tunneling from the drain to the body. By using a t_{si} much smaller than W_d, DG MOSFETs can avoid these dilemmas and achieve tight control of short channel effects.

Since the two gates are connected and switched together, DG MOSFET also has an ideal subthreshold slope. In the subthreshold region, the conduction band of the silicon film moves along with the applied gate voltage (volume inversion). As shown in Figure 1.6, the body effect coefficient m equals

$$m = \frac{\Delta V_g}{\Delta \psi_s} \tag{1.10}$$

and hence, the subthreshold slope is ideal 60mv/dacade.

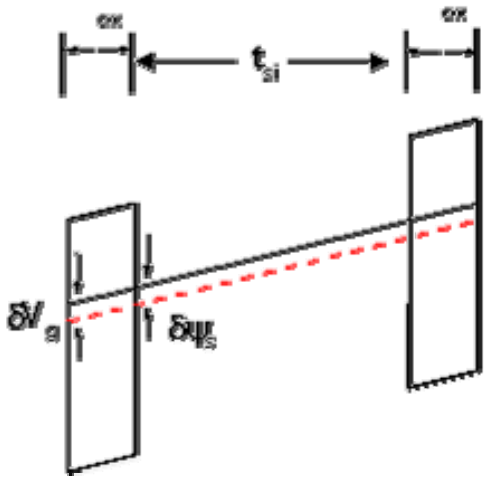


Figure 1.6 Schematic diagram of conduction band shifting with applied gate voltage.

In DG MOSFETs, the silicon body is usually undoped or lightly doped, which leads to oseveral benefits. First of all, the threshold voltage variation due to random dopant fluctuation effects is greatly reduced because the threshold voltage of DG MOSFETs is controlled by the gate work function instead of the dopants. Second of all, the undoped body greatly reduces the source and drain junction capacitances and hence, improves the switching speed of DG MOSFETs. Third of all, the elimination of depletion charges also provides an enhancement of carrier mobility because of reduced coulomb scattering and surface roughness scattering.

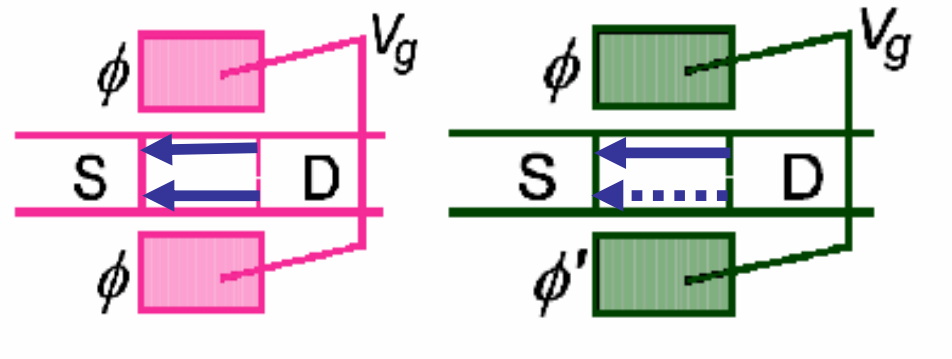
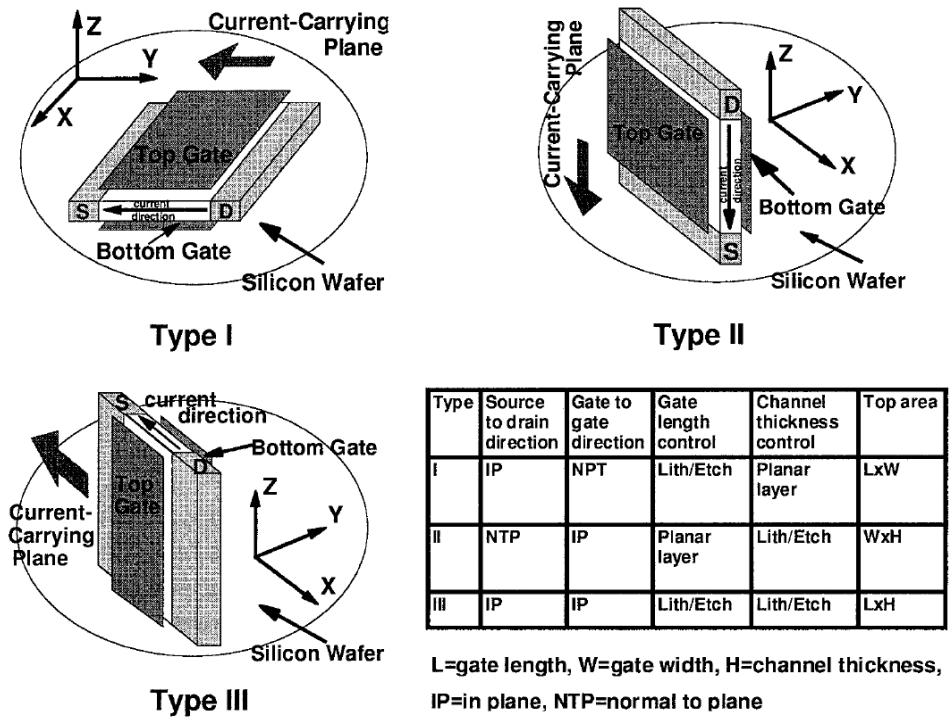


Figure 1.7 Schematic diagram of a symmetric (left) and an asymmetric Double-Gate MOSFET.

Figure 1.7 illustrates two different types of DG MOSFETs: symmetric DG MOSFETs in which the two gates have identical work functions and asymmetric DG MOSFETs in which the two gates have different work functions. There are two operation modes for DG MOSFETs. One is the three-terminal mode in which two gates are tied and switched simultaneously. The other is the four-terminal mode in which only one gate is switching with the other back gate constantly biased. The back gate voltage enables the possibility of dynamic threshold voltage with the cost of losing the ideal 60mv/decade subthreshold slope.



Type	Source to drain direction	Gate to gate direction	Gate length control	Channel thickness control	Top area
I	IP	NPT	Lith/Etch	Planar layer	LxW
II	NTP	IP	Planar layer	Lith/Etch	WxH
III	IP	IP	Lith/Etch	Lith/Etch	LxH

L=gate length, W=gate width, H=channel thickness,
IP=in plane, NTP=normal to plane

Figure 1.8 Different topologies of DG MOSFETs (Adapted from [33]).

In principle, DG MOSFETs can be manufactured by one of the three topologies shown in Figure 1.8. Type I (planar type) DG MOFET [33] has the channel layer in the silicon wafer plane so that it controls the channel thickness by thin film deposition rather than by lithography. The drawback is the difficulty to align the top and bottom gate. Type II (vertical type) DG MOSFET has the channel in the vertical direction and is most compact for DRAM application [34]. However, it is topologically difficult for a CMOS application. Type III (Fin type) DG MOSFET [33], in which current flows horizontally through the fin channel, has the highest packing density for high speed logic applications.

Quantum mechanical behavior of inversion electrons in DG MOSFETs is much more complicated than in bulk MOSFETs. In DG MOSFETs, the potential well is formed by

the front gate oxide barrier, the conduction band and the back gate oxide barrier. Therefore the confinement of motion not only comes from the conduction band of the silicon body, but also comes from the silicon film thickness. This additional confinement modulates the potential well and hence the energy levels and wave functions significantly. It becomes dominant when the silicon film is extremely thin or the field is very small (subthreshold region of symmetric DG MOSFETs). Quantum effects in DG MOSETs are hence more complicated than bulk MOSFETs because of the combined confinement mechanism. Since quantum behavior of electrons generally depend on both the silicon thickness and the shape of the silicon conduction band, modeling of quantum effects is in great interest of researching rather than applying the results from bulk MOSFETs.

1.4 Compact Modeling of MOSFETs

As mentioned in section 1.1, MOSFET has been the main building block of integrated circuits ever since its invention. Accordingly, compact modeling of MOSFETs has also been continuously evolving for complex circuit design. To achieve fast and accurate circuit simulation results, explicit algebraic equations of device terminal parameters such as I-V and C-V characteristics are required. Compact model of MOSFETs usually starts from a precise core model – long channel classical model. All specific physical phenomena including quantum effects, short channel effects, channel length modulation, etc., are then implemented into this core model as modifications. Figure 1.9 illustrates the schematic structure of a compact model for a MOSFET. The evolution of MOSFET

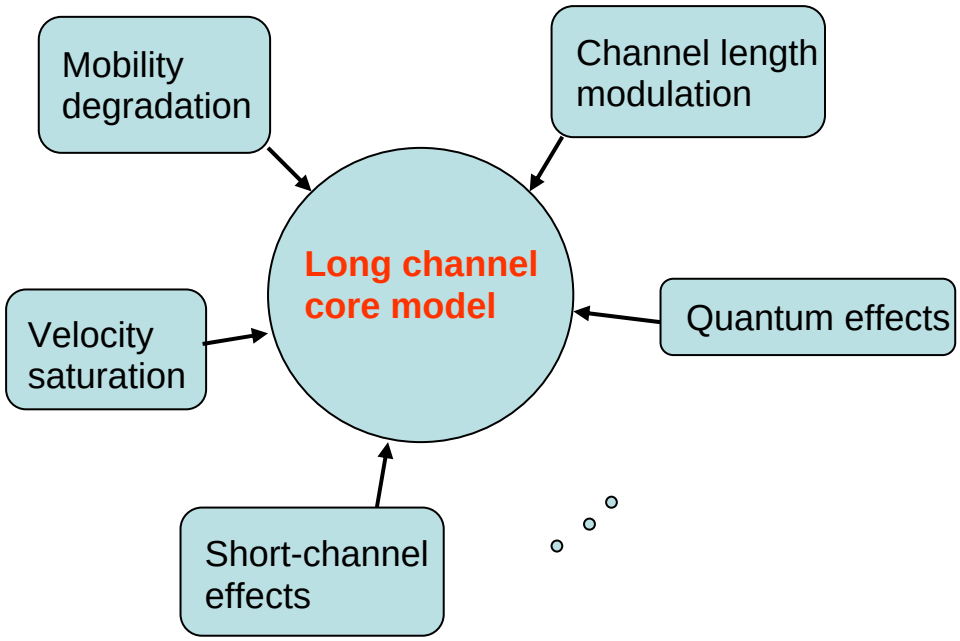


Figure 1.9 Schematic diagram of a compact model for the bulk MOSFETs.

compact model follows the trend from simple, piecewise models to complicated, continuous models to provide more accurate circuit simulations. The piecewise models such as early versions of BSIM model provide separate equations based on the charge sheet approximation for different operation regions. This leads to the discontinuous first order derivates of current and charge and hence severe convergence. Non-physical mathematical smoothing functions are adopted in recent BSIM3/BSIM4 models to overcome the convergence problem. Another prominent issue with the BSIM models is the violation of source and drain symmetry, which means source and drain are not interchangeable with each other in BSIM. Both the current model [35] and the capacitance model [36] are shown to be asymmetric with respect to the source and drain in BSIM models. To avoid the disadvantages of BSIM models, the surface potential models such as PSP [37] and HiSIM [38] models have been developed as the next

generation of compact model for bulk MOSFETs. Without introducing the threshold voltage, one single surface potential equation valid for all the operation regions is solved for the solution in these models. The symmetry property can be preserved by using the symmetric linearization techniques [39].

However, there still lacks a comprehensive compact model for DG MOSFETs, especially when quantum effects dominate. Various approaches have been applied to study quantum effects in DG MOSFETs, including the nonequilibrium Greens function [40], density gradient model [41], [42], and Monte Carlo simulation [43]-[45]. The mathematical complexities of these models make them impractical for compact modeling. In another work, quantum subband energy levels [46] and the quantum threshold shift [47] have been investigated through a variational approach. However, only the potential and charge distribution have been worked out. No drain current equation has been developed for a compact model. A quantum compact model [48] was previously developed based on the approximation of a single sine wave function for different energy subbands. This is only valid for an infinite, flat potential well under subthreshold condition. Once the DG MOSFET is strongly inverted, the field due to electrons themselves causes a bimodal wave function with peaks near the surfaces not well represented by the sine function. In this work, we bridge the gap by implementing quantum effects into an analytic potential model [49, 50] as quantum corrections for DG MOSFETs. We also investigate quantum effects in the short channel DG MOSFETs based on a 2-D analytical potential solution. The dissertation of this work is listed in the next section.

1.5 Outline of The Dissertation

In chapter 1, the concept of CMOS scaling is first introduced. Quantum mechanical effects in bulk MOSFETs and methods of investigating quantum effects are reviewed. The structure and advantages of DG MOSFETs are then summarized. After introducing compact models for bulk MOSFETs, objective and status of compact modeling of quantum effects in DG MOSFETs are presented. The rest of the dissertation is organized as follows.

Chapter 2 introduces the 1-D numerical Poisson's and Schrodinger solver for DG MOS structure, including the numerical methods of solving equations and the iteration procedure of finding self-consistent solutions. Classical and quantum results from the solver are presented. The 1-D solver is then extended to also calculate the DG MOSFET drain current.

From the extensive solution from the solver, threshold voltage shift and inversion layer capacitance for symmetric DG MOSFETs are extracted as closed form functions of silicon thickness and inversion charge density in Chapter 3. With these modifications, the analytic compact potential model is shown to reproduce quantum I-V and C-V curves of symmetric DG MOSFETs consistent with those obtained from the full quantum solutions. CMOS circuit simulations using the full model are also presented.

Chapter 4 focuses on compact modeling of asymmetric DG MOSFETs. Threshold voltage shift is extracted as closed form function of silicon thickness and device built-in field by using the eigen energy levels calculated through the variational approach. Another expression for the energy levels is also obtained based on physical observations. An equivalent small signal capacitance model is developed to model the gate capacitance degradation due to quantum effects in asymmetric DG MOSFETs.

In chapter 5, quantum solutions are obtained by incorporating the 2-D analytical potential solution for DG MOSFETs in the subthreshold region. Quantum subthreshold current is obtained through a iteration procedure as well as a double integral in which the eigenvalues of Schrodinger equation is calculated through the perturbation approach. Approximate expressions of quantum threshold voltage roll-off due to short channel effects and quantum subthreshold slope are derived.

Conclusions of the dissertation and discussion of future directions beyond the scope of this work are drawn in the last chapter.

Chapter 2

A 1-D Poisson-Schrodinger Numerical Solver

2.1 The Coupled Poisson And Schrodinger Equations

The salient feature of a DG MOSFET is the thin silicon layer which is beneficial to device scaling. Quantum effects arise due to the confinement of electron motion in the thin silicon film in contrast to the confinement by the surface potential (or field) in bulk devices. To obtain the quantum electrical characteristics of a DG MOS structure, one needs to solve the coupled Poisson and Schrodinger equations self-consistently [51]:

$$\frac{d^2\psi(x)}{dx^2} = \frac{q}{\varepsilon_{si}} n(x) \tag{2.1}$$

and

$$-\frac{\hbar^2}{2m_i}\frac{d^2\varphi_{i,j}(x)}{dx^2} + \left(-q\psi(x)\right)\varphi_{i,j}(x) = E_{i,j}\varphi_{i,j}(x) \tag{2.2}$$

where x is the coordinate along the normal direction, $\psi(x)$ is the electrostatic potential, q is the electronic charge, ε_{si} is the silicon permittivity, $\hbar$ is the Planck's constant, m_i is the electron effective mass in the i*th* valley, $\varphi_{i,j}(x)$ is the normalized wave function associated with the eigenenergy $E_{i,j}$ of the j*th* subband in the i*th* valley and $-q\psi(x)$ is the potential energy.

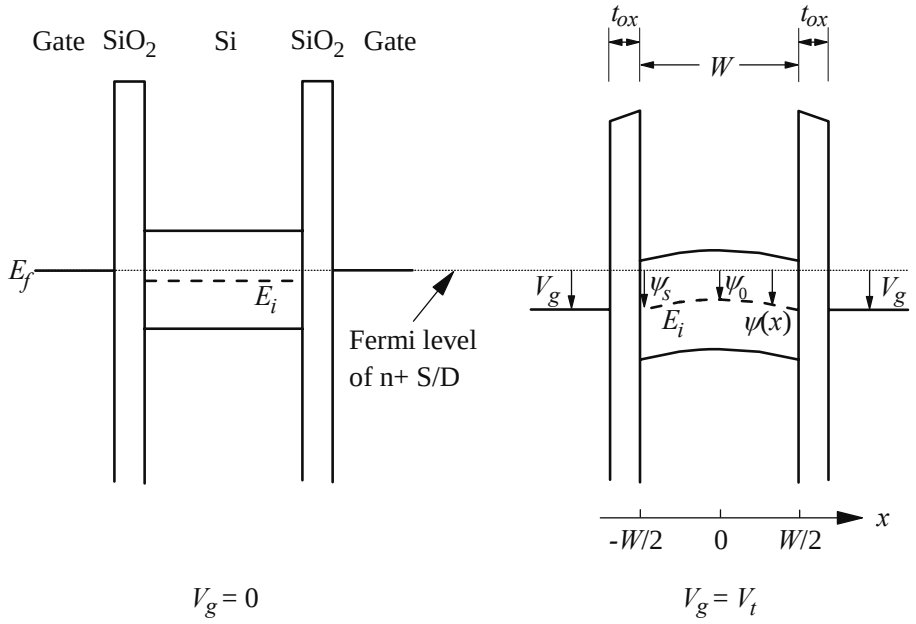


Figure 2.1 The schematic band diagram of a double gate MOSFET. The electrostatic potential is reference to the quasi-Fermi level of the n^+ source/drain.

The two equations couples with each other through the potential energy term in the Schrodinger equation and the electron density $n(x)$ which is given by the eigen energy $E_{i,j}$ and the wave function $\varphi_{i,j}(x)$ as:

$$n(x) = \frac{kT}{\pi\hbar^2}\sum_i g_i m_i^* \sum_j \ln[1+e^{(E_F-E_{ij})/kT}]\left|\varphi_{ij}(x)\right|^2 \tag{2.3}$$

where k is the Boltzmann's constant, T is the temperature in Kelvin, E_F is the Fermi level, g_i and m_i^* are the degeneracy and density-of-state effective mass in the i*th* valley, respectively.

$\psi(x)$ is related to the gate voltage V_g and oxide thickness t_{ox} through the boundary condition at the silicon-oxide interfaces, as shown in the schematic band diagram of a double gate MOSFET (Figure 2.1).

$$\varepsilon_{ox}\frac{V_g-\Delta\phi_1-\psi(x=t_{si}/2)}{t_{ox}}=\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=\frac{t_{si}}{2}} \tag{2.4}$$

$$\varepsilon_{ox}\frac{V_g-\Delta\phi_2-\psi(x=-t_{si}/2)}{t_{ox}}=-\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=-\frac{t_{si}}{2}} \tag{2.5}$$

where ε_{ox} is the oxide permittivity, $\Delta\phi_1$ and $\Delta\phi_2$ are the work function difference between the gate electrode and the intrinsic silicon, and t_{si} is the thickness of the silicon film.

A 1-D Poisson-Schrodinger solver is then developed to solve these two equations iteratively for a 1-D MOS device.

2.2 Numerical Method Of Solving The Equations

2.2.1 Solving Poisson Equation

The subroutine “Poisson1” and “Poisson” in the solver are used to solve the Poisson equation numerical. The difference of these two subroutines will be discussed in section 2.4. Assuming we know the solution in the m^{th} computation loop, which is the electrostatic potential $\psi^m(x)$, the electron density $n^m(x)$ and the hole density $p^m(x)$. And now we need to solve the solution in the next loop. The solutions in the two consecutive loops relate to each other after defining the increment of the potential $\Delta\psi(x)=\psi^{m+1}(x)-\psi^m(x)$, the electron density $\Delta n(x)=n^{m+1}(x)-n^m(x)$ and the hole density $\Delta p(x)=p^{m+1}(x)-p^m(x)$.

$$\frac{d^2\psi^{m+1}(x)}{d^2x} = \frac{d^2\psi^{m}(x)}{d^2x} + \frac{d^2(\Delta\psi(x))}{d^2x}$$
$$= \frac{q}{\varepsilon_{Si}}\left[(n^m(x) - p^m(x) - N_d{}^+ + N_a{}^-)\right] + \frac{q}{\varepsilon_{Si}}\left(\Delta n(x) - \Delta p(x)\right) \tag{2.6}$$

From the Boltzmann's relations (2.7), one can easily express $\Delta n(x) - \Delta p(x)$ in terms of the incremental potential $\Delta\psi(x)$.

$$n(x) = n_i e^{q\psi(x)/kT} \quad p(x) = n_i e^{-q\psi(x)/kT} \tag{2.7}$$

$$\Delta n(x) - \Delta p(x) = \frac{q\left(n^m(x) + p^m(x)\right)}{kT}\Delta\psi \tag{2.8}$$

Then we need to divide the device to a certain mount of mesh. In the discrete computation mesh, the differential becomes finite difference. Substitute (2.8) into (2.6) and we obtain:

$$\frac{\Delta\psi(x+\Delta x) - 2\Delta\psi(x) + \Delta\psi(x-\Delta x)}{(\Delta x)^2}$$
$$= -\frac{\psi^{(m)}(x+\Delta x) + 2\psi^{(m)}(x) - \psi^{(m)}(x-\Delta x)}{(\Delta x)^2}$$
$$+q\frac{n^{(m)}(x) - p^{(m)}(x) + N_a{}^- - N_d{}^+}{\varepsilon_{Si}} + \frac{q}{\varepsilon_{Si}}\left(\Delta n(x) - \Delta p(x)\right) \tag{2.9}$$
$$= -\frac{\psi^{(m)}(x+\Delta x) + 2\psi^{(m)}(x) - \psi^{(m)}(x-\Delta x)}{(\Delta x)^2}$$
$$+q\frac{n^{(m)}(x) - p^{(m)}(x) + N_a{}^- - N_d{}^+}{\varepsilon_{Si}} + \frac{q^2(n^{(m)}(x) + p^{(m)}(x))}{\varepsilon_{si}kT}\Delta\psi(x)$$

where Δx is the length of the mesh.

Rearrange (2.9) in terms of the incremental potential in three consecutive meshes and we have:

$$\Delta\psi(x+\Delta x)-2\Delta\psi(x)+\Delta\psi(x-\Delta x)-(\Delta x)^2\frac{q^2(n^{(m)}(x)+p^{(m)}(x))}{\varepsilon_{si}kT}\Delta\psi(x)$$
$$=-\psi^{(m)}(x+\Delta x)+2\psi^{(m)}(x)-\psi^{(m)}(x-\Delta x)+(\Delta x)^2 q\frac{n^{(m)}(x)-p^{(m)}(x)+N_a^{-}-N_d^{+}}{\varepsilon_{Si}} \quad (2.10)$$

The above equation can be expressed in a tridiagonal matrix form:

$$\begin{pmatrix} \ddots & \ddots & & & \\ \ddots & \ddots & \ddots & & \\ & 1 & c(i) & 1 & \\ & & \ddots & \ddots & \ddots \\ & & & \ddots & \ddots \end{pmatrix}\begin{pmatrix} \vdots \\ \Delta\psi(i-1) \\ \Delta\psi(i) \\ \Delta\psi(i+1) \\ \vdots \end{pmatrix}=\begin{pmatrix} \vdots \\ b(i-1) \\ b(i) \\ b(i+1) \\ \vdots \end{pmatrix} \quad (2.11)$$

where $c(i)$ is the diagonal element of the matrix which stores the coefficients of the $\Delta\psi(i)$ term in (2.10), and the lower-subdiagonal and upper-subdiagonal elements which represents the coefficients of the $\Delta\psi(i+1)$ and $\Delta\psi(i-1)$ term in (2.10) respectively are both the constant 1.

$$c(i)=-2-\Delta x^2\frac{q^2(n(i)+p(i))}{\varepsilon_{si}kT} \quad (2.12)$$

and $b(i)$ is the element of a vector which stores the right hand of (2.10).

$$b(i)=\psi(i+1)-2\psi(i)+\psi(i-1)-(\Delta x)^2\frac{q(n(i)-p(i)+N_a^{-}-N_d^{+})}{\varepsilon_{si}} \quad (2.13)$$

With $c(i)$ and $b(i)$ fully known, an algorithm named "Lu3" can be used to calculate the solution of (2.11), which is the vector that stores the incremental potential $\Delta\psi(i)$ at every mesh. If the maximum value of $\Delta\psi(i)$ is small enough (smaller than an criteria we set up which is 10^{-8} V in the solver), the loop will be terminated and the $\psi(x)$, $n(x)$ and $p(x)$ at that loop are the final solution of the Poisson equation. If the maximum value of $\Delta\psi(i)$ is greater

than the criteria, the potential is revised to $\psi(x) + Max\left(\Delta\psi(i)\right)/10$ and another loop starts. The same procedure is repeated till the maximum incremental potential is smaller than the criteria.

2.2.2 Solving Schrodinger Equation

The subroutine "schrodinger" in the solver is used to solve the Schrodinger equation numerically. Just as solving the Poisson equation, the differential becomes the finite difference and the Schrodinger equation has the following formula:

$$\frac{2\varphi_{i,j}(x) - \varphi_{i,j}(x+\Delta x) - \varphi_{i,j}(x-\Delta x)}{\Delta x^2} \times \left(\frac{\hbar^2}{2m_i}\right) - q\psi(x)\varphi_{i,j}(x) = E_{i,j}\varphi_{i,j}(x) \quad (2.14)$$

Rearrange (2.14) in terms of the electron wave function in three consecutive meshes and we have:

$$\left[\frac{2}{\left(\Delta x\sqrt{2m_i}/\hbar\right)^2} - q\psi(x)\right]\varphi_{i,j}(x) - \frac{\varphi_{i,j}(x+\Delta x) + \varphi_{i,j}(x-\Delta x)}{\left(\Delta x\sqrt{2m_i}/\hbar\right)^2} = E_{i,j}\varphi_{i,j}(x) \quad (2.15)$$

Now, it is straight-forward to see that the solution of Schrodinger equation has been turned into finding the eigenvalues and eigenvectors of a symmetric tridiagonal matrix A whose diagonal elements and sub-diagonal elements are shown in (2.16) and (2.17), respectively.

$$A(i,i) = \frac{2}{\left(\Delta x\sqrt{2m_i}/\hbar\right)^2} - q\psi(x) \quad (2.16)$$

$$A(i,i-1) = A(i-1,i) = \frac{-1}{\left(\Delta x\sqrt{2m_i}/\hbar\right)^2} \quad (2.17)$$

With the matrix “A” fully known, we can use the “bisection” algorithm to calculate the eigen value which is the eigen energy and use the “inverse iteration” algorithm to calculate the eigen vector which is wave function in both valleys.

After obtaining the eigen energy and the wave function of all the subbands in both valleys, the electron density can be calculated by summing the contribution of all the subbands through (2.3).

2.2.3 Solving Poisson and Schrodinger Equation Self-Consistently

As mentioned in the section 2.1, the Poisson equation and the Schrodinger equation couple with each other through the potential energy term. To obtain the correct solution, an iteration procedure is needed to solve the two equations self-consistently. Figure 2.2 shows the process flow of the iteration procedure. First we solve the Poisson and obtain the initial potential in the subroutine “poisson1”. The electron density is also calculated in this subroutine using (2.7). This means that we obtain the classical solution which includes both the classical potential profile and the classical electron distribution after completing this subroutine. Then, we substitute the initial potential into the potential energy term and solve the Schrodinger equation in the subroutine “schrodinger”. The quantum electron density is also calculated in this subroutine. Using this quantum electron distribution, we then solve the Poisson equation again in the subroutine “poisson2”. Note that in the subroutine “poisson2”, only the potential is solved while the electron density is fixed at the quantum one obtained from the subroutine “schrodinger”. This ensures that the final quantum results are the self-consistent solutions of both

Poisson and Schrodinger equations. After completing the subroutine “poisson2”, we have two potentials. One is the potential in the current loop, and the other is the one in the previous loop or the initial potential. Then, the two potentials are compared with each other. If the difference between the two potentials is smaller than the criteria (10-6 V) that we set up in the solver, the final self-consistent quantum solutions are found. If the two potentials do not converge with each other, another iteration loop starts. The same procedure repeats until the correct solutions are obtained. The computation loop number for the quantum solution depends on the device size, the gate bias and the criteria. Usually the bigger the device, the higher the gate voltage, and the smaller the criteria, the more the computation loops are needed.

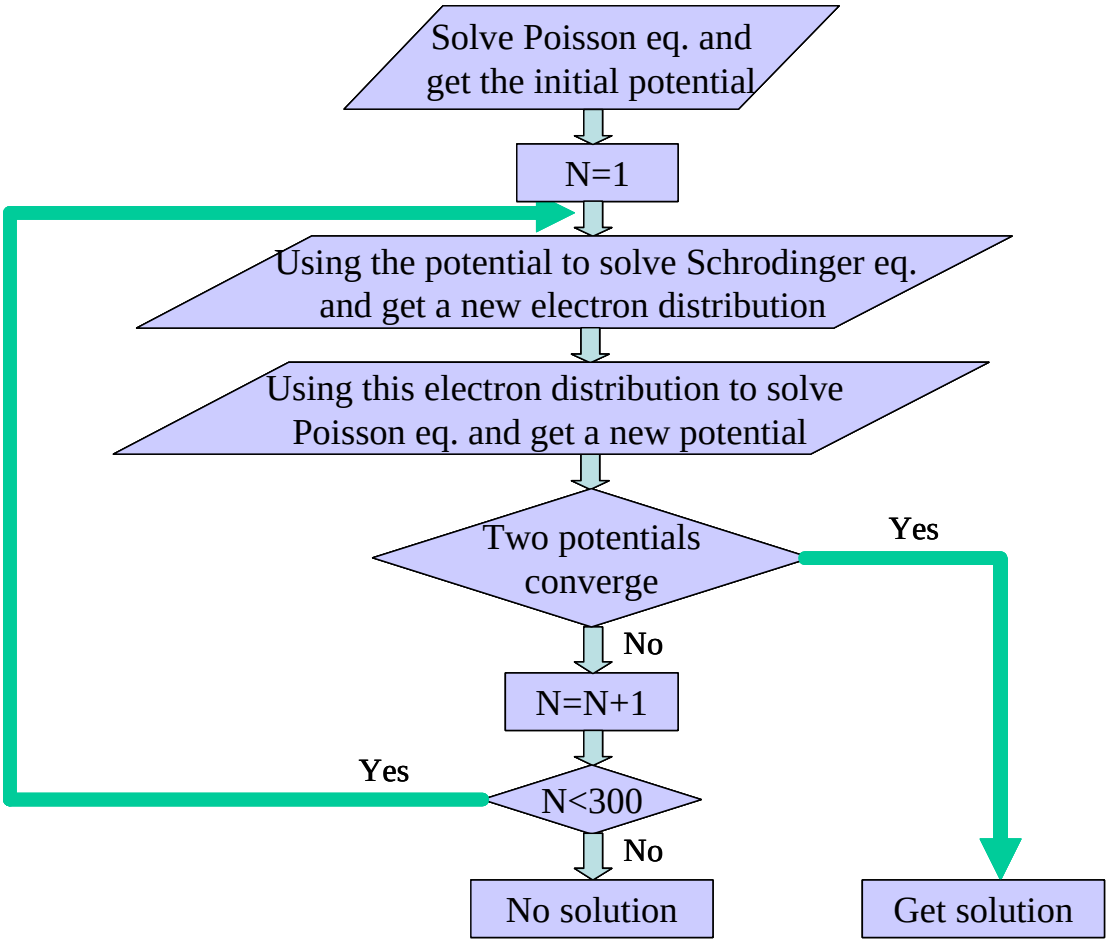
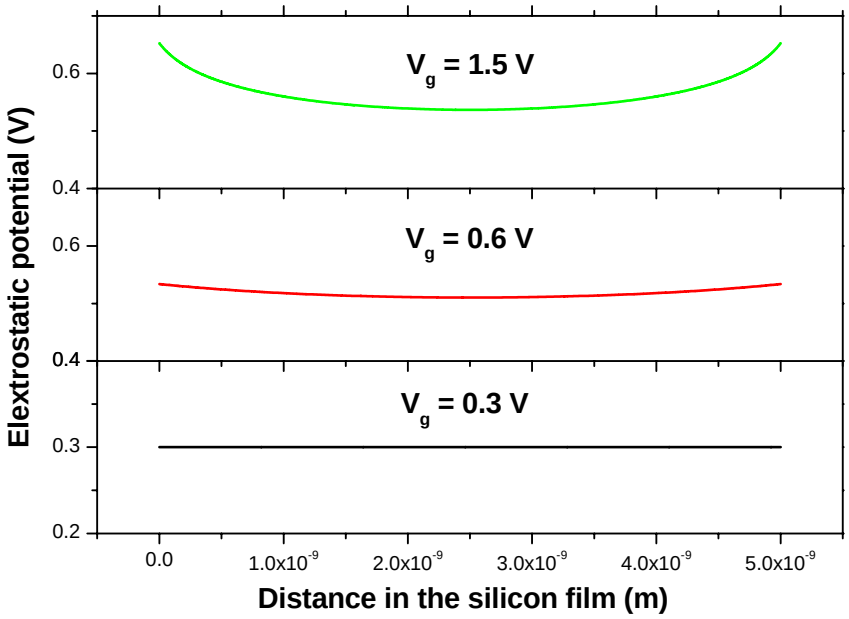


Figure 2.2 The flow chart of the numerical iteration procedure used to solve Poisson and Schrodinger equations self-consistently.

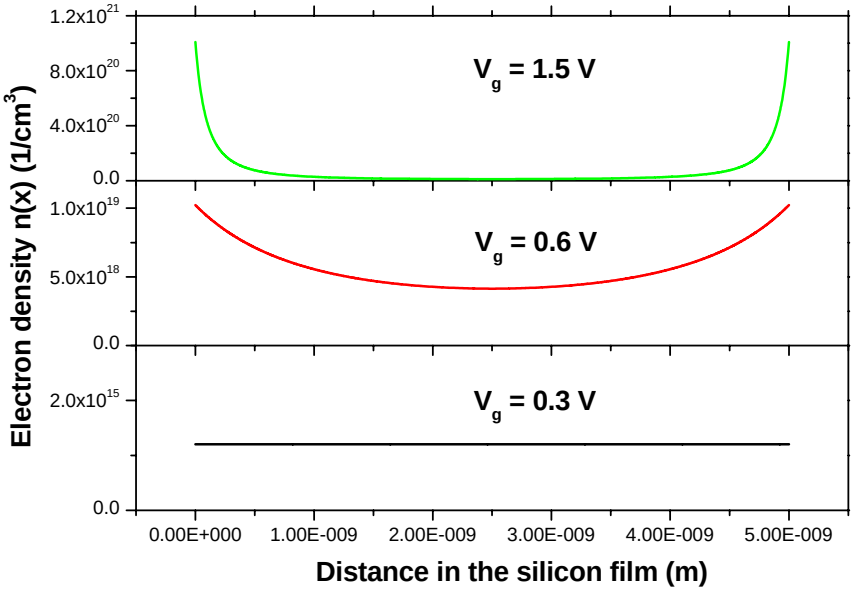
2.3 Classical and Quantum Results from the 1D Solver

From the 1-D numerical solver, we can obtain the classical electrostatic results by solving the Poisson equation only and quantum results by solving the Poisson and Schrodnger equations self-consistently. Figure 2.3 (a) shows the classical electrostatic potential profile in the silicon film at several values of gate voltage V_g and Figure 2.3 (b) shows the corresponding classical inversion electron density. At small gate voltage, the

inversion electron density is very small and its influence on the potential is negligible. The conduction and of the silicon film therefore remains essentially flat and follows up the change of the gate voltage. As a result, the electron density is also essentially flat, which is called “volume inversion”. As V_g increases, the potential profile starts bending the silicon conduction band and does not follow up the gate voltage change due to the voltage drop in the gate oxide. At high V_g, the inversion is very strong and so is the band bending. As a consequence, the electron density has two sharp peaks at the silicon-oxide interface as shown in Figure 2.3 (b).



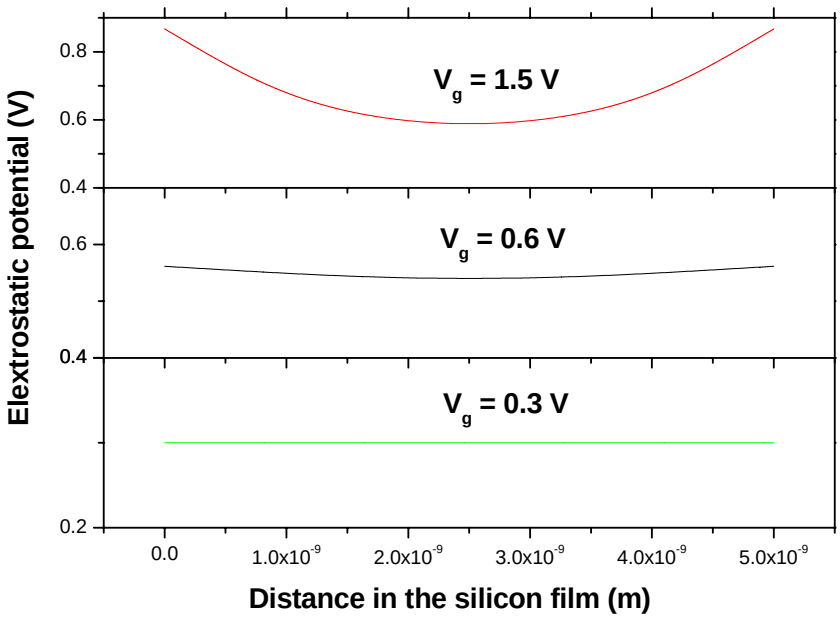
(a)



(b)

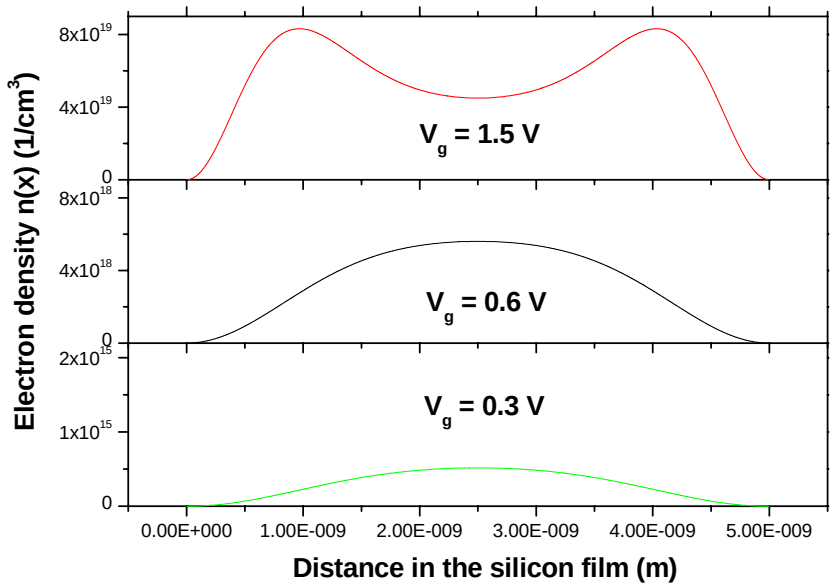
Figure 2.3 The classical (a) electron potential and (b) density obtained from the Poisson-Schrodinger solver as a function of position in the silicon film for a symmetric DG MOSFET with midgap gates. Three gate voltages V_g=0.3, 0.6 and 1.5 V are considered.

However, the pictures are different due to the quantization induced by the confinement of the oxide barrier and silicon conduction band. The quantum potential and electron density at different gate voltages are shown at Figure 2.4 (a) and (b), respectively. At low gate voltage, although the potential profile still remains flat because of the weak inversion, the high enough oxide barrier confinement leads to zero wave function at the two silicon-oxide interface. Therefore, the electron concentration peaks at the center of the silicon film. As Vg increases, this electron concentration peak remains at the middle of the silicon film until the gate voltage V_g is so high that the peak in the center will become two peaks close to the two interfaces.

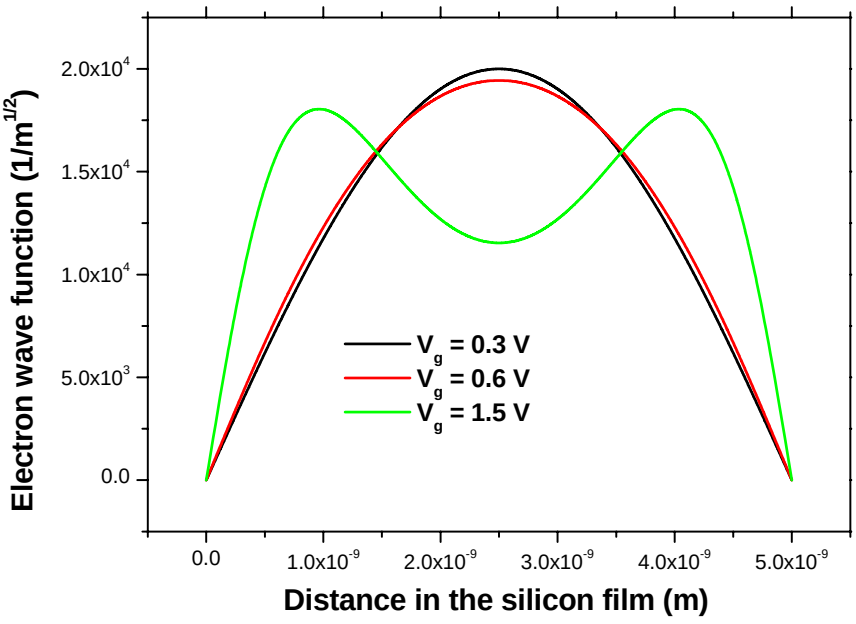


(a)

Figure 2.4 The classical electron (a)potential, (b) density and (c) wave function of the lowest subband obtained from the Poisson-Schrodinger solver as a function of position in the silicon film for a symmetric DG MOSFET with midgap gates. Three gate voltages V_g=0.3, 0.6 and 1.5 V are considered (Figure 2.4 (b) and (c) continued).



(b)



(c)

Figure 2.4 continued

The electron wave function of the lowest subband shown in Figure 2.4 (c) partially explains the reason. At a small V_g, the potential is flat but the probability of electrons appearing at the center is the greatest due to the oxide barriers at the interfaces. With increasing V_g, the potential profile bends up, which means that the potential energy bends down. In other words, the silicon conduction band in the center is the highest in the whole silicon film. Therefore, the probability of electron appearing at the center will decrease because electrons tend to stay at low energy states. Accordingly, the wave function between the center and the interface will increase due to the normalization requirement. However, this effect is weak because the band bending is not strong when the V_g is not too high. At a high Vg, the band bending is very strong and the high potential energy at the center prevents the electrons from populating there, Therefore, the maximum probability of electrons appearing will move to the place between the center and the interface.

2.4 Expanding The Solver To MSOFET – Influence Of Quasi-Fermi Level

The 1-D numerical solver can be used to calculate the current of a DG MOSFET through the integration of the 1-D electrostatic solution of corresponding MOS structure. Figure 2.5 shows the schematic diagram of a long channel DG MOSFET. The same voltage V_g is applied to the two gates, and different voltages V_s and V_d are applied to the source and

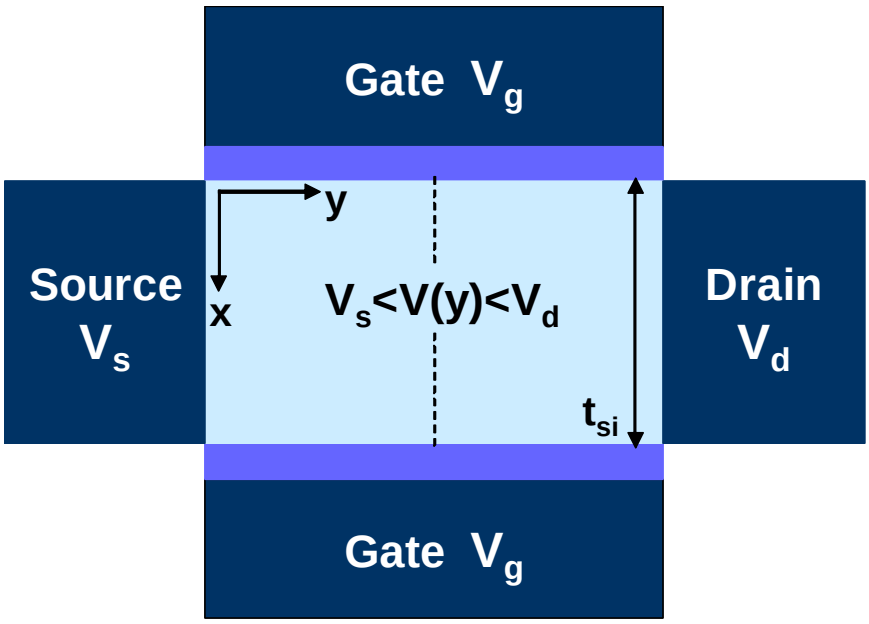


Figure 2.5 Schematic diagram of a long channel DG MOSFET. The quasi-Fermi potential V is constant in the vertical direction.

drain respectively. The quasi-Fermi potential V, which stays constant in the vertical(x) direction according to the gradual channel approximation, equals to V_s at the source and V_d at the drain. The inversion charge sheet density Q_i at y, which is the electron concentration $n(x,y)$ integrated over the silicon film varies with y, or equivalently with V from the source to the drain.

$$Q_i \equiv q\int_0^{t_{si}} n(x,y)dx \tag{2.18}$$

The Pao-Sah's integral indicates that the drain current I_{ds} is proportional to the integral of the inversion charge sheet density Q_i as a function of V from the source to the drain.

$$I_{ds} = \mu\frac{W}{L}\int_{V_s}^{V_d} Q_i\left(V_g, V\right)dV \tag{2.19}$$

where μ is the electron mobility, W is the device width and L is the channel length.

It is clear that one needs the inversion charge sheet density as a function of the quasi-Fermi potential along the channel to do the integral and then calculate the current. The 1-D solver we developed can calculate the classical and quantum inversion charge density for the DG MOS in which $V_s = V_d$. To simplify the problem, the default value of V_s/V_d used in the solver is zero. The classical and quantum Q_i-V_g curves for $V_s = V_d = 0$ shown in Figure 2.6 are both obtained from the solver.

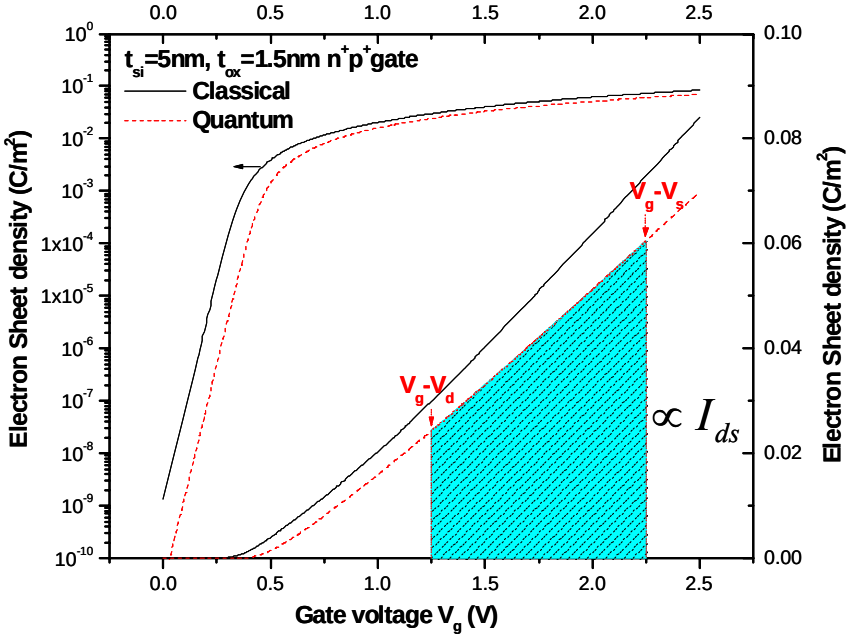


Figure 2.6 Classical (solid line) and quantum (dash line) Q_i–V_g curves obtained from the solver on both linear and logarithmic scale for an n^+p^+ DG MOS. The area under the curve from V_g - V_s to V_g - V_d is proportional to the drain current of corresponding DG MOSFET.

Along the channel, the Poisson's equation at y becomes

$$\frac{d^2\left(\psi(x)-V\right)}{dx^2}=\frac{q}{\varepsilon_{si}}n(x) \tag{2.20}$$

with the boundary condition.

$$\varepsilon_{ox}\frac{V_g - V - \Delta\phi - \psi(x = t_{si}/2)}{t_{ox}} = \varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=\pm\frac{t_{si}}{2}} \tag{2.21}$$

$$\varepsilon_{ox}\frac{V_g - V - \Delta\phi - \psi(x = -t_{si}/2)}{t_{ox}} = -\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=\pm\frac{t_{si}}{2}} \tag{2.22}$$

Comparing (2.20), (2.21) and (2.22) with (2.1), (2.4) and (2.5), one can easily find out that there is no difference between the potential solution of the DG MOSFET channel with a gate bias V_g and quasi-Fermi level V and the solution of a DG MOS with a different gate bias $V_g - V$. Consequently, one has

$$Q_i^{CL}\left(V_g, V\right) = Q_i^{CL}\left(V_g - V, 0)\right). \tag{2.23}$$

In the quantum case, the quasi-Fermi potential does not show up in the Schrodinger equation and hence the eigenenergy levels and wave functions are the same with those of corresponding DG MOS. The influence of the quasi-Fermi potential is pulling down the Fermi level E_F in (2.3) by the amount of V. However, decreasing the gate voltage Vg by the amount of V has the same affect, which leads to

$$Q_i^{QM}\left(V_g, V\right) = Q_i^{QM}\left(V_g - V, 0)\right) \tag{2.24}$$

(2.23) and (2.24) mean $Q_i(V_g,V)$ as a function of quasi-Fermi potential V in the DG MOSFET can be obtained from the $Q_i(V_g,0)$ data of the 1-D DG MOS. Through the transformation in (2.24), the area under the 1-D DG MOS $Q_i(V_g,0)$ curve from V_g - V_s to V_g - V_d, which is shown graphically in Figure 2.5, can be substituted for the $Q_i(V_g,V)$ integral in (2.19). Therefore the Pao-Sah's integral becomes the integration of Q_i as the function of the gate voltage

$$I_{ds} = \mu \frac{W}{L} \int_{V_s}^{V_d} Q_i\left(V_g, V\right) dV = -\mu \frac{W}{L} \int_{V_g - V_s}^{V_g - V_d} Q_i\left(V_g', 0\right) dV_g' \tag{2.25}$$

Conventionally the source voltage is defined as the ground potential, and the drain voltage is $V_{ds} = V_d - V_s$, then we have

$$I_{ds} = -\mu \frac{W}{L} \int_{V_g}^{V_g - V_{ds}} Q_i\left(V_g', 0\right) dV_g' \tag{2.26}$$

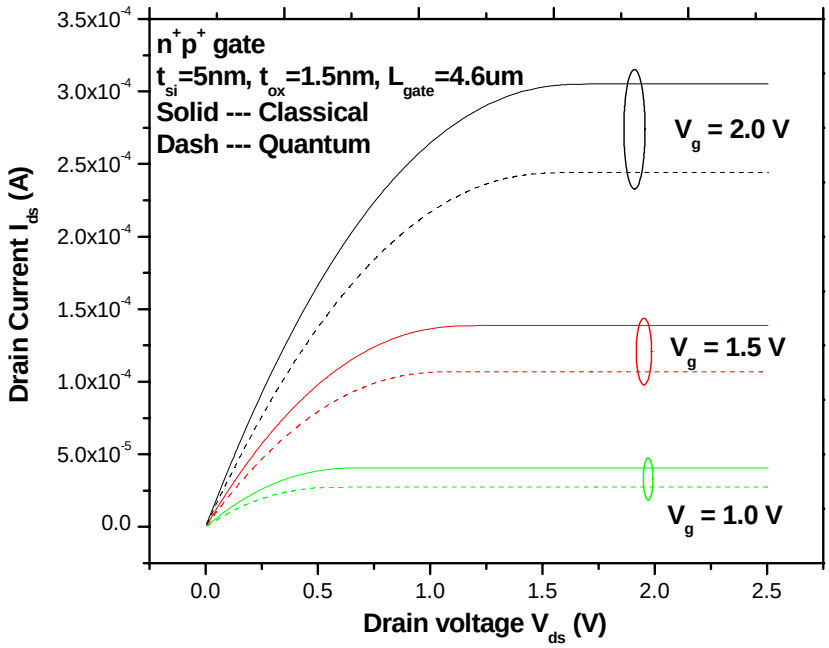


Figure 2.7 Classical (solid line) and quantum (dash line) I_{ds}-V_{ds} characteristics at different gate voltage V_g. All the curves are obtained from the integration of $Q_i(V_g,0)$ data.

The I_{ds}-V_{ds} characteristics at different V_g obtained from the integration of $Q_i(V_g,0)$ curve are shown in Figure 2.7. By this method, one can avoid solving the coupled Poisson, Schrodinger and current continuity equations self consistently to obtain $Q_i(V_g,V)$ in the Pao-Sah's integral. The electrostatic results of a DG MOS obtained from the Poisson/Schrodinger solver are extended directly to the I-V characteristics of a DG MOSFET. As shown in Figure 2.6, the higher threshold voltage and the smaller gate

capacitance due to quantization cause the area under the quantum $Q_i(V_g,0)$ curve to be smaller than the area under the classical curve for the same gate and source-drain voltages. For the same reason, the quantum drain current is smaller than the classical current at the same gate and drain bias in Figure 2.7. In saturation, the quantum current is about 20% lower than the classical current for the DG device studied, due mainly to the gate capacitance degradation.

Chapter 3

Compact Modeling of Quantum Effects in Symmetric DG MOSFETs

3.1 Thickness And Field Dependent Quantum Effects

3.1.1 Infinite Square Well Behavior At Low V_g

As discussed in 1.4, the quantum well in a DG MOSFET consists of the front and back oxide barriers and the conduction band of the silicon film, therefore, both the silicon thickness and the electrical field (slope of the conduction band) play important roles in the quantum effects. However, when V_g is below the threshold voltage, the silicon conduction band remainss essentially flat and follows up the change of the gate voltage due to negligible influence of the small inversion electron density on the potential profile. In other words, the quantum well mostly acts like an infinite square well whose eigen energy levels and wave functions only depend on the silicon thickness as:

$$E_j = \frac{\hbar^2 \pi^2 j^2}{2mt_{si}^2}, \qquad j = 1, 2, 3, \bullet\bullet\bullet \tag{3.1}$$

$$\varphi_j(x) = \begin{cases} \sqrt{\frac{2}{t_{si}}} \sin\left(\frac{j\pi x}{t_{si}}\right), & 0 < x < t_{si} \\ 0, & x < 0, x > t_{si} \end{cases} \tag{3.2}$$

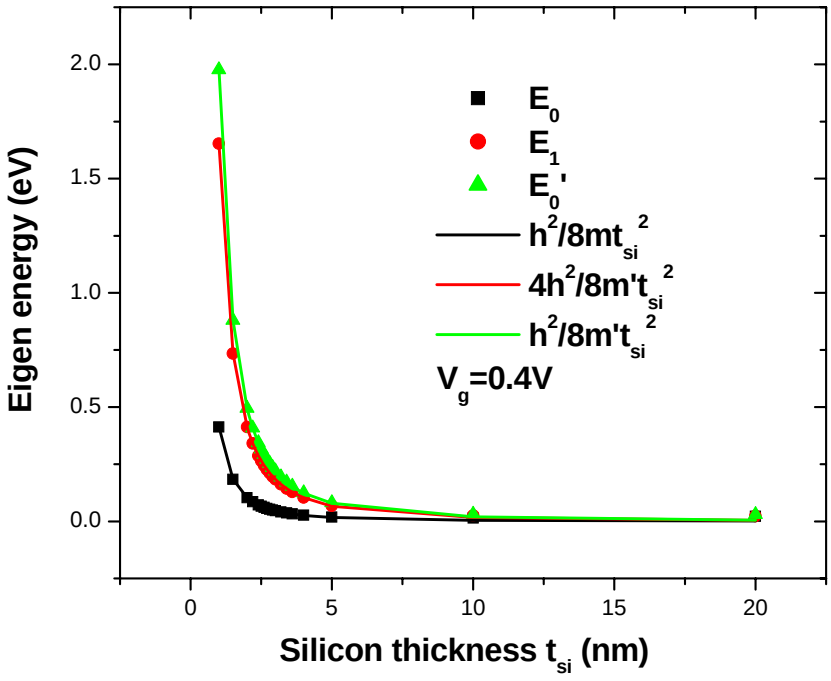


Figure 3.1 The first two lowest eiegn energy levels in the g = 2 valley and the lowest energy level in the g = 4 valley of a symmetric DG MOSFET compared with the corresponding eigen energy levels of an infinite square well.

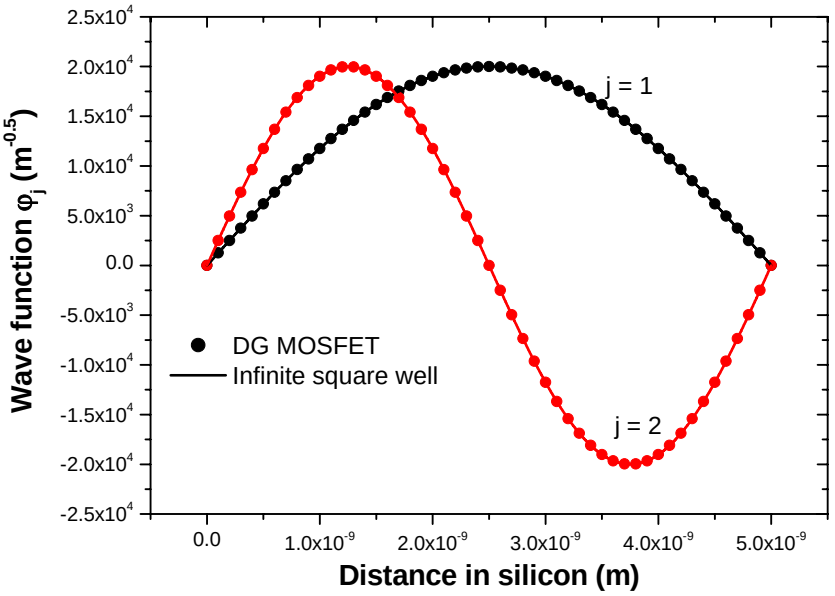


Figure 3.2 Wave functions of the two lowest subbands of a symmetric DG MOSFET (line) compared with corresponding wave functions of an infinite square well (symbol).

Figure 3.1 shows the first three lowest eigen energies of a DG MOSFET with different silicon thickness compared with the eigen energies of an corresponding infinite square well. The wave function comparison is illustrated in Figure 3.2. The excellent agreement of both eigen energy and wave function verifies the validity of treating the DG MOSFETs at low V_g as an infinite square well.

3.1.2 Effect Of Band Bending On Quantum Solutions

When V_g is above the threshold voltage, the conduction band starts to bend and hence, the electrical field becomes significant, which has a strong influence on the eigen energy levels. As illustrated in Figure 3.2, the eigen energies increase rapidly with the surface field after the device is turned on.

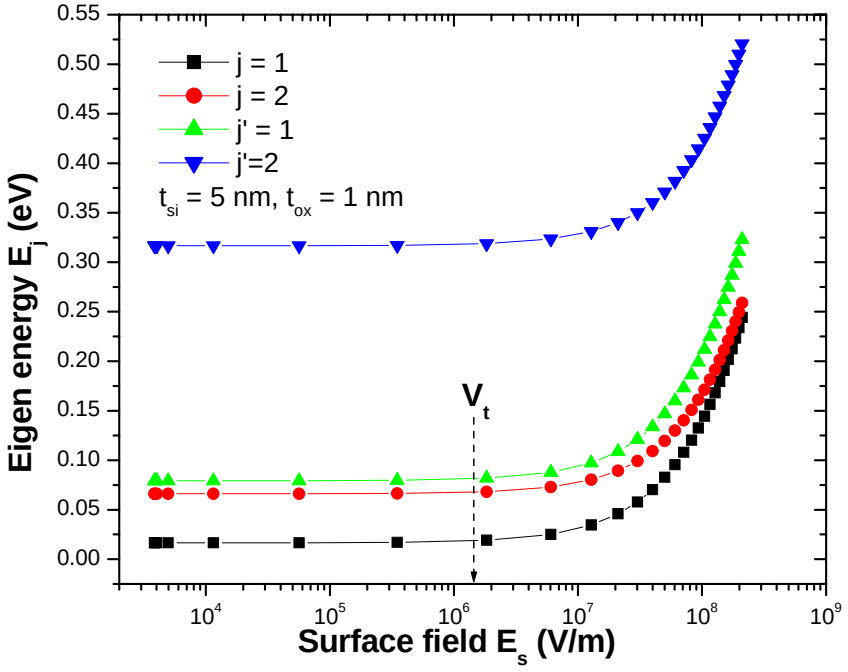


Figure 3.3 The lowest two eigen energy levels in both valleys versus the surface field of a symmetric DG MOSFET.

This means that quantum effects in a symmetric DG MOSFET at high V_g depend on both the silicon thickness and the shape of the conduction band. It is shown in Figure 3.4 that instead of changing monotonously with t_{si} at low V_g case, the eigen energy has an minimum around a certain value of t_{si} when V_g is high.

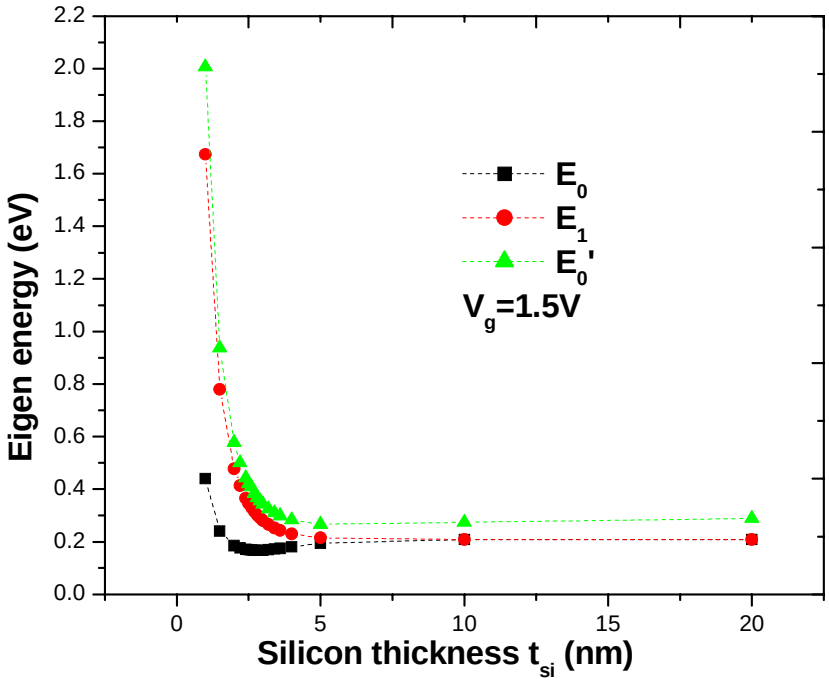


Figure 3.4 The lowest two eiegn energy levels in the $g = 2$ valley and the lowest energy level in the $g = 4$ valley of a symmetric DG MOSFET at $V_g = 1.5$ V.

This phenomenon was observed before but no physical explanation are given. The physics behind this energy minimum is the combined silicon thickness and field influence on the eigen energies. As t_{si} decreases, the eigen energies tend to increase according to the uncertainty principle. On the other hand, the surface field also decreases due to decreasing inversion charge sheet density (V_t increase with decreasing t_{si}) and hence the eigen energies tend to increase. The opposite energy tendencies with varying t_{si} therefore lead to the energy minimum in Figure 3.4.

3.2 Threshold Voltage Shift Due To Quantum Effects

3.2.1 Definition Of V_t Shift

The quantum threshold voltage is higher than the classical one due to the discrete energy levels which is higher than the bottom of the conduction band. Figure 3.5 illustrates the definition of the threshold voltage shift due to quantum effects and the gate capacitance as well. The V_t shift is extracted from the parallel shift of Q_i- V_g curve at subthreshold region with respect to the classical curve at the same inversion charge sheet density Q_i.

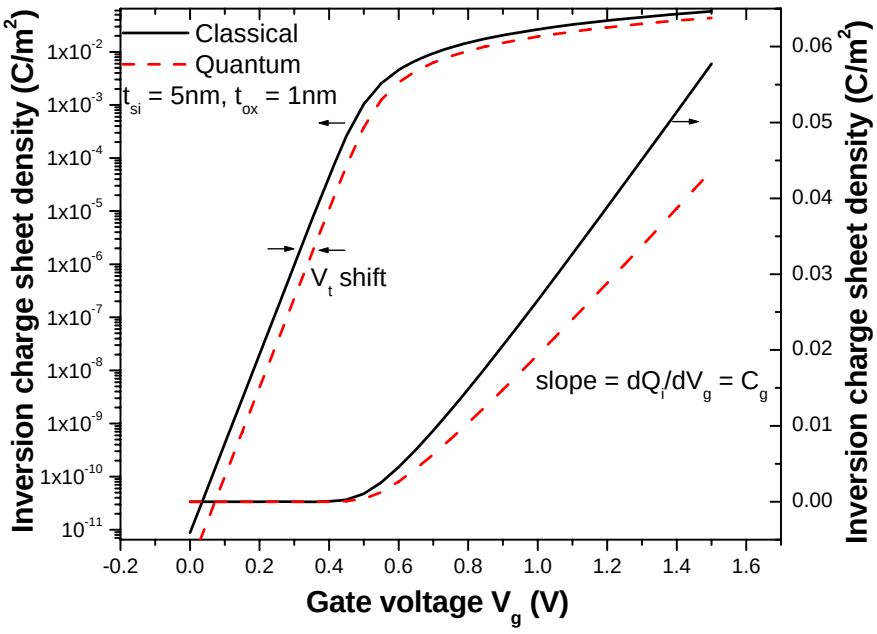


Figure 3.5 Classical (solid line) and quantum (dashed line) mobile charge sheet density Q_i of symmetric DG MOSFETs in both linear (right) and logarithmic (left) scales versus gate voltage.

As discussed in 3.1.1, the potential remains essentially flat in the subthreshold region of a symmetric DG MOSFET, which means the voltage drop across the gate oxide is negligible. Therefore, the oxide thickness does not affect both classical and quantum inversion charge densities and hence, the threshold voltage shift as shown in Figure 3.6.

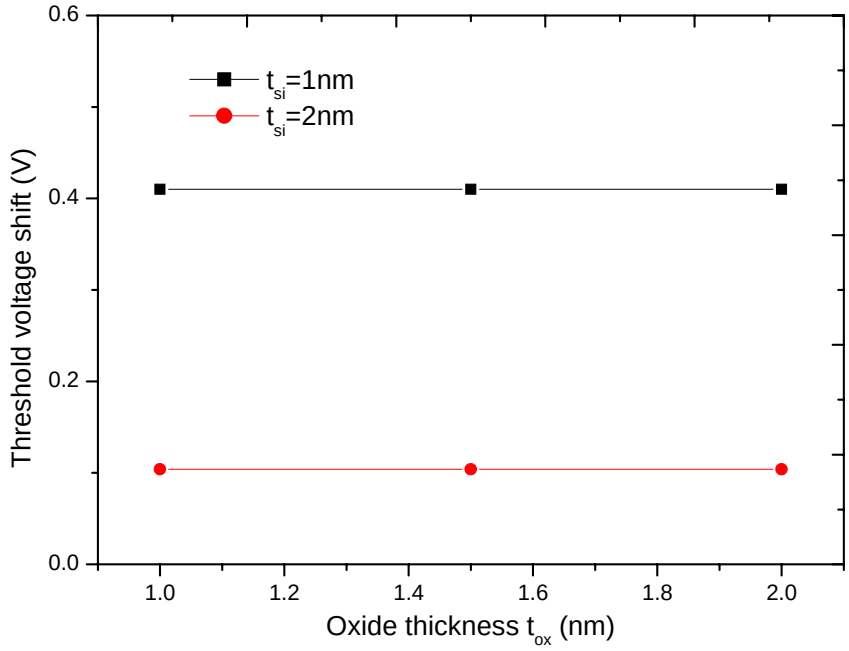


Figure 3.6 Threshold voltage shift of a symmetric DG MOSFET with different silicon and oxide thickness.

3.2.2 Expression Of V_t Shift

Due to volume inversion, the classical inversion charge sheet density is

$$Q_i^{CL} = \int_0^{t_{si}} qn_i e^{q\psi(x)/kT} dx = qn_i t_{si} e^{\frac{qV_g}{kT}} \tag{3.3}$$

And the quantum inversion charge density is

$$\begin{aligned} Q_i^{QM} &= \frac{qkT}{\pi\hbar^2}\left\{ gm_d \sum_j \ln\left(1+e^{(E_f-E_j)/kT}\right) + g'm_d' \sum_{j'} \ln\left(1+e^{(E_f-E_j')/kT}\right)\right\} \\ &= \frac{qkT}{\pi\hbar^2}\left\{ gm_d \sum_j e^{-E_j/kT} + g'm_d' \sum_{j'} e^{-E_j'/kT}\right\} e^{\left(qV_g-\frac{E_g}{2}\right)\Big/kT} \end{aligned} \tag{3.4}$$

where E_j is the eigen energy ((3.1)) of the infinite square well based on the discussion in 3.1.1. In (3.4), we assume that the Fermi level is at least several kT below the lowest eigen energy level.

From the definition of V_t, one has.

$$Q_i^{CL} = Q_i^{QM} e^{q\Delta V_t / kT} \tag{3.5}$$

Substituting (3.3) and (3.4) into (3.5) yields an expression of the V_t shift.

$$\Delta V_t = \frac{kT}{q} \ln \left(\frac{n_i t_{si} \pi \hbar^2}{qkT \left(g m_d \sum_j e^{-E_j / kT} + g' m_d' \sum_{j'} e^{-E_{j'} / kT} \right)} \right) + \frac{E_g}{2q} \tag{3.6}$$

3.2.3 First Energy Level Approximation

From the compact modeling point of view, (3.6) is too tedious. Rewrite (3.6) by subtracting E_1 in every E_j, one has

$$\Delta V_t = \frac{kT}{q} \ln \left(\frac{n_i t_{si} \pi \hbar^2}{qkT \left(g m_d \sum_j e^{-(E_j - E_1)/kT} + g' m_d' \sum_{j'} e^{-(E_{j'} - E_1)/kT} \right)} \right) + \frac{E_g}{2q} + \frac{E_1}{q}. \tag{3.7}$$

The first term in the right side of (3.7) is a weak function of t_{si} and its value largely cancel with $E_g/2q$, which is the second term in the right side of (3.7). Therefore, the V_t shift can be expressed as a closed form function of t_{si}.

$$V_t^{QM} - V_t^{CL} = \Delta V_t = \frac{E_1}{q} = \frac{\hbar^2 \pi^2}{2q m^* t_{si}^{\ 2}} \tag{3.8}$$

where $m^*=0.91m_0$ is the larger effective mass in the two valleys.

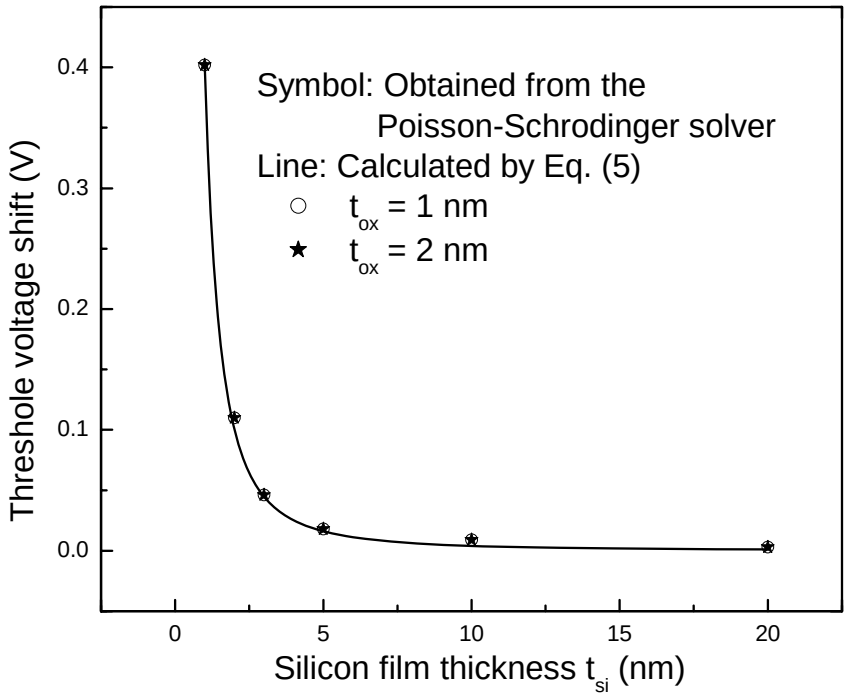


Figure 3.7 Threshold voltage shift due to quantum effects as a function of silicon film thickness. Symbols (t_{ox}=1nm (circle) and t_{ox}=2nm (star)) are obtained from the Poisson-Schrodinger solver. The line is calculated from (3.8).

The first subband approximation in (3.8) is justified in thin Si films where the energy spacing between the subbands is larger than kT so that electrons predominantly occupy the lowest subband. For thick Si films, the subband spacing decreases and several subbands may be populated. But in that case, the quantum V_t shift is small and the error associated with equation (3.8) is much less than kT/q. Figure 3 7 shows that the threshold voltage shift calculated by (3.8) is in good agreement with that obtained directly from the Poisson-Schrodinger solver. As expected, the result is independent of t_{ox}.

3.3 Gate Capacitance Degradation And Effective Inversion Layer Thickness

3.3.1 Definition of Effective Inversion Layer Thickness

The distribution of inversion charges from the surface due to quantum effects suggests the finite thickness of the inversion layer. This means an inversion capacitance in series with the oxide capacitance. In the presence of this inversion capacitance, the total gate capacitance, or the slope dQ_i/dV_g in Figure 3.5, is reduced.

$$\frac{dQ_i}{dV_g} = C_g = \frac{2}{\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{inv}}{\varepsilon_{si}}} \tag{3.9}$$

where t_{inv} is defined as the equivalent inversion layer thickness. The factor of two arises from the two symmetric channels of the device. The fact that electrons are distributed farther away from the surface due to quantum effects increases the inversion layer thickness and causes gate capacitance degradation. It can be modeled in terms of a parameter,

$$\delta t_{inv} = t_{inv}^{QM} - t_{inv}^{CL} \tag{3.10}$$

where t_{inv}^{CL} and t_{inv}^{QM} are extracted from the classical and quantum Q_i-V_g curves via (3.9).

3.3.2 Extracting Effective Inversion Layer Thickness

There are two different methods to extract δt_{inv} in (3.10) through the classical and quantum t_{inv}. Figure 3.8 shows the classical and quantum Q_i–V_g curves. The quantum curve is shifted to the left by the value of ΔV_t to ensure the influence caused by V_t shift is

eliminated. The first method is using the slopes at point A and B which have the same gate voltage to calculate δt_{inv} through (3.9) and (3.10). The other one is using the slopes at point B and C which have the same inversion charge sheet density.

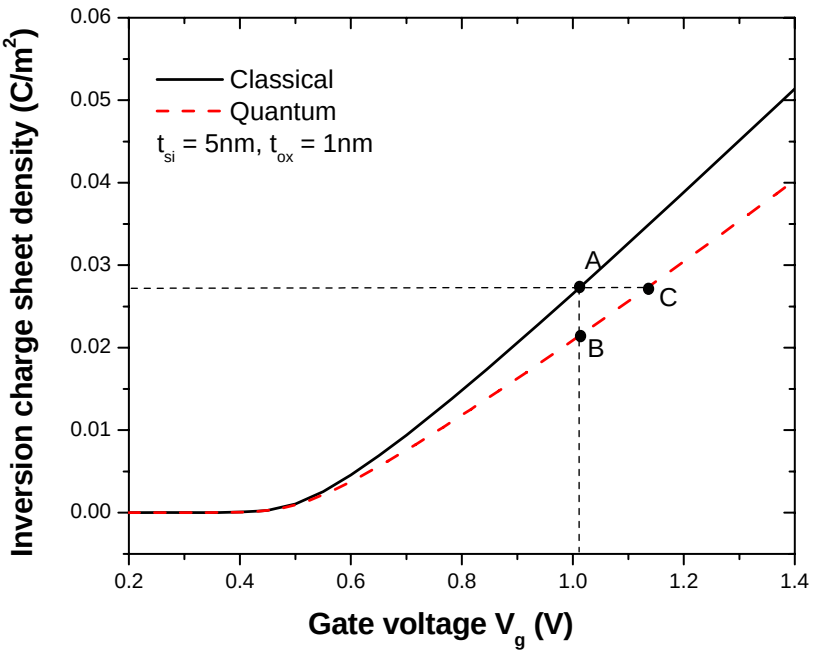
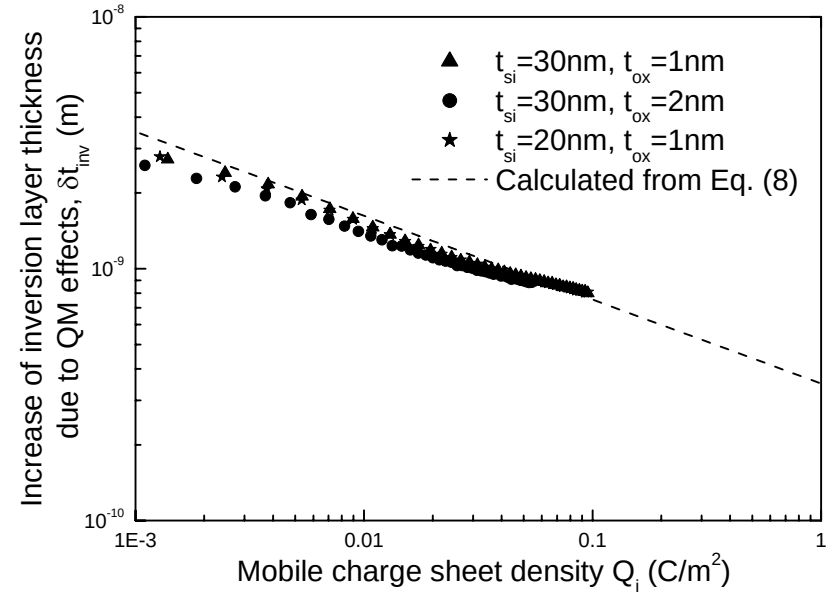


Figure 3.8 Classical and quantum Q_i–V_g curves for a symmetric DG MOSFET. The quantum curve is shifted to the left by the amount of ΔV_t to ensure the same off-state condition.

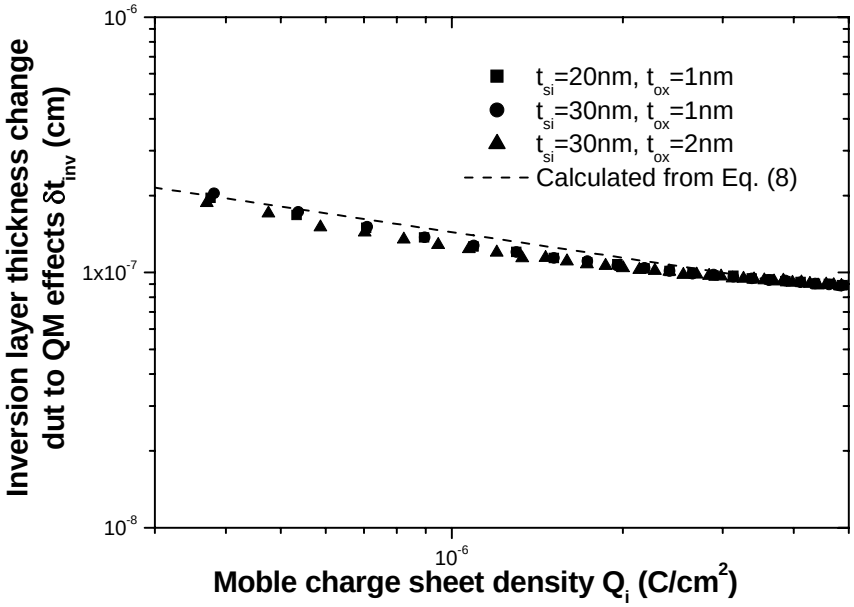
In general, δt_{inv} is a weak function of Q_i. In bulk MOSFETs, an approximate expression for the quantum inversion layer thickness in the electric quantum limit was derived by Stern [18]. A similar approximate expression for δt_{inv} is found to apply to DG MOSFETs,

$$\delta t_{inv} = \left(\frac{\alpha \varepsilon_{si} \hbar^2}{m^* q Q_i} \right)^{1/3} \tag{3.11}$$

where α is a fitting constant to represent the influence of the classical inversion layer thickness. Its value is also different when using different methods to extract δt_{inv}: α = 10.5 at same V_g and α = 7 at same Q_i. Figure 3.9 compares δt_{inv} vs. Q_i calculated from (3.11) and those obtained from the Poisson-Schrodinger solver for symmetric DG MOSFETs with different silicon and oxide thickness. Quantum degradation of gate capacitance can then be modeled as an effective increase of the oxide thickness t_{ox} by $(\varepsilon_{ox}/\varepsilon_{si})\delta t_{inv}$ based on (3.11).



(a)



(b)

Figure 3.9 Increase of inversion layer thickness due to QM effects, δt_{inv}, as a function of Q_i calculated from (3.11) (line) and obtained from the Poisson-Schrodinger solver (symbol) for three sets of silicon and oxide thickness. δt_{inv} is extracted at the same V_g in (a) and at the same Q_i in (b).

3.4 Analytical Classical Potential Model

In the undoped DG MOSFETs, due to absence of the depletion charge, Poisson's equation $\frac{d^2\psi(x)}{dx^2} = \frac{q}{\varepsilon_{si}} n(x)$ with $n(x) = n_i e^{q\psi/kT}$ can be rigorously solved to obtain an analytical expression for the potential in the silicon film [49]

$$\psi(x) = V - \frac{2kT}{q} \ln\left[\frac{t_{si}}{2\beta} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} \cos\left(\frac{2\beta x}{t_{si}} \right) \right] \tag{3.12}$$

where V is the electron quasi-Fermi potential at a point along the channel, and the dimensionless parameter β is a function of V to be determined from the boundary condition

$$\varepsilon_{ox} \frac{V_g - \Delta\phi - \psi(x = \pm t_{si}/2)}{t_{ox}} = \pm \varepsilon_{si} \left. \frac{d\psi}{dx} \right|_{x=\pm\frac{t_{si}}{2}} \tag{3.13}$$

Substituting (3.12) into (3.13) leads to

$$\frac{q\left(V_g - \Delta\phi - V\right)}{2kT} - \ln\left[\frac{2}{t_{si}} \sqrt{\frac{2\varepsilon_{si} kT}{q^2 n_i}} \right] = \ln\beta - \ln\left[\cos\beta\right] + 2\frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}} \beta \tan\beta \tag{3.14}$$

From Gauss's law, the classical charge density is

$$Q_i = 2\varepsilon_{si} \left. \frac{d\psi}{dx} \right|_{x=\pm\frac{t_{si}}{2}} = 8\frac{\varepsilon_{si}}{t_{si}} \frac{kT}{q} \beta \tan\beta \tag{3.15}$$

Differentiating (3.14) yields

$$\frac{dV}{d\beta} = -\frac{2kT}{q}\left(\frac{1}{\beta} + \tan\beta + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\left(\beta\sec^2\beta + \tan\beta\right)\right) \tag{3.16}$$

By substituting (3.15) and (3.14) into the current continuity equation and integrating [16], a continuous, analytical drain current expression is obtained for all regions of MOSFET operation,

$$\begin{aligned} I_{ds} &= \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(V)dV = \mu\frac{W}{L}\int_{\beta_s}^{\beta_d} Q_i(V)\frac{dV}{d\beta}d\beta \\ &= \mu\frac{W}{L}\frac{4\varepsilon_{si}}{t_{si}}\left(\frac{2kT}{q}\right)^2\left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta^2\tan^2\beta\right]\Bigg|_{\beta_d}^{\beta_s} \end{aligned} \tag{3.17}$$

Here, β_s, β_d are solutions to (3.14) corresponding to V being the source voltage V_s and the drain voltage V_d, respectively. Figure 3.10 compares the I_{ds}-V_{ds} characteristics calculated by the analytical model with the 2-D numerical simulation (ISE) results. They are in excellent agreement in different operation regions.

Using the $Q_i(\beta)$ expression, the gate capacitance can be expressed in terms of β.

$$C_g = \frac{dQ_i}{dV_g} = \frac{dQ_i}{d\beta}\frac{d\beta}{dV_g} = 4\frac{\varepsilon_{si}}{t_{si}}\frac{\beta\sec^2\beta + \tan\beta}{\frac{1}{\beta} + \tan\beta + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\left(\beta\sec^2\beta + \tan\beta\right)} \tag{3.18}$$

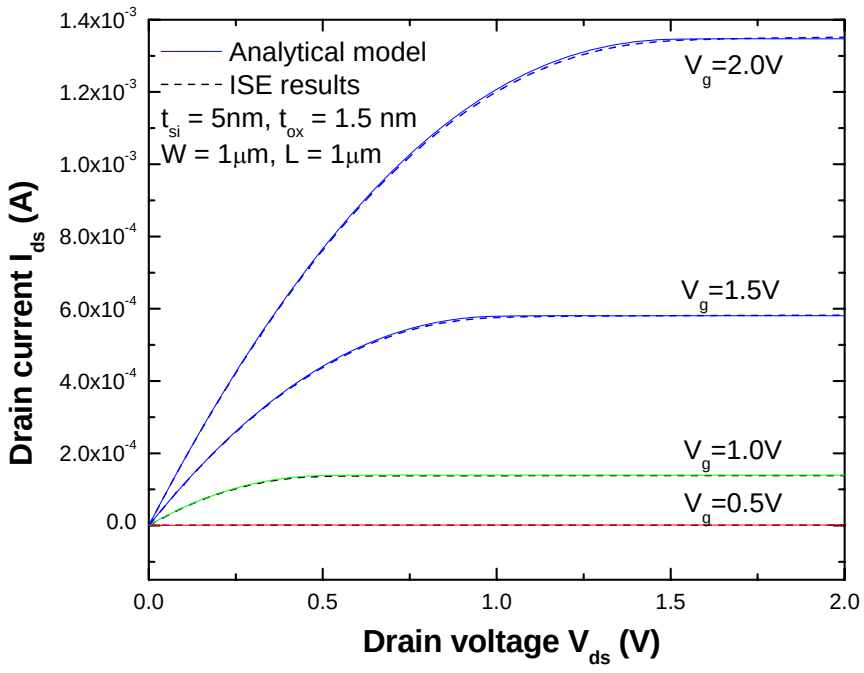


Figure 3.10 I_{ds}-V_{ds} curves of a symmetric DG MOSFET at different gate voltages. The solid line is calculated from (3.17) and the dashed line is from the ISE results.

3.5 Implementation Of Quantum Effects In The Compact Model

3.5.1 Implementation of V_t Shift

Although no specific definition of threshold voltage is invoked in the analytic potential model, the threshold voltage shift due to quantum effect can be implemented by changing the gate work function in (3.14) from $\Delta\phi$ to $\Delta\phi + \Delta V_t$, with ΔV_t given by (3.8). Quantum threshold voltage shift can be also implemented as an effective change in the silicon thickness in a classical compact model for symmetric DG MOSFETs.

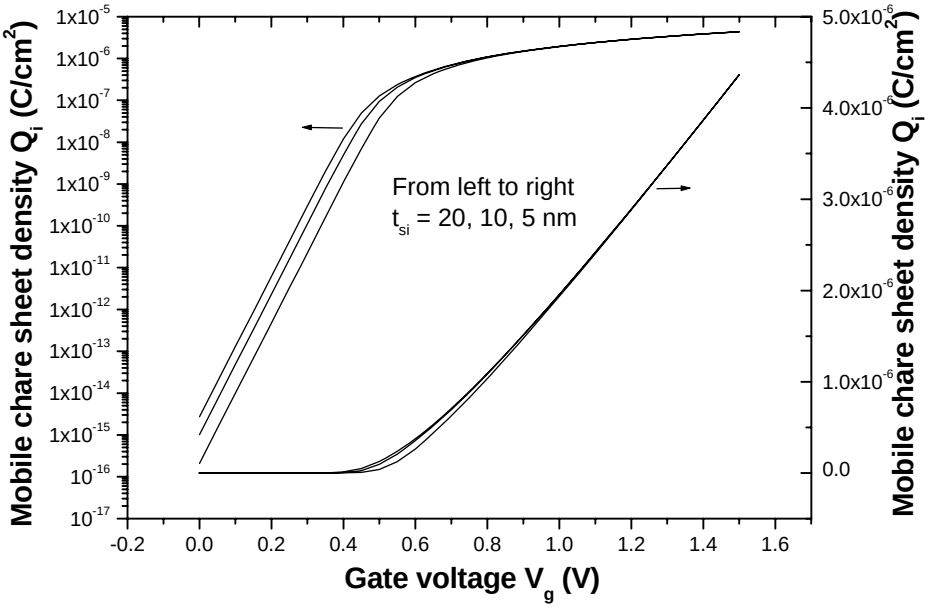


Figure 3.11 Quantum inversion charge sheet density Q_i in both linear (right) and logarithmic (left) scales as a function of the gate voltage V_g. All curves (same t_{ox} = 1 nm but different t_{si}) are obtained from the solver.

Figure 3.11 presents the quantum Q_i-V_g curves obtained from the Poisson-Schrodinger solver for a symmetric DG MOSFET with different silicon thickness. It shows that the t_{si} dependent V_t shift due to quantum effects only occurs in the subthreshold region and does not affect the on-state Q_i for $t_{si} \geq$ 5nm. To implement such effects in a classical model, we make use of the fact that the subthreshold current obtained from (3.14) and (3.17) in the limit of $\beta \langle \langle 1$,

$$I_{ds} = \mu \frac{W}{L} kTn_i t_{si} e^{\frac{q(V_g - \Delta\phi)}{kT}} \left(1 - e^{-\frac{qV_{ds}}{kT}}\right) \tag{3.19}$$

is proportional to t_{si} (volume inversion), whereas and the on-state current (in the limit of $\beta \approx \pi/2$) is insensitive to t_{si}. Then, the quantum induced V_t shift can be implemented as an

effective change in the silicon thickness which shifts the subthreshold current by the ΔV_t of (3.8) without affecting the above-threshold characteristics.

$$t_{si}^{QM} = t_{si} e^{-\frac{q\Delta V_t}{kT}} = t_{si} e^{-\frac{\hbar^2 \pi^2}{2m^* kT t_{si}^2}} \tag{3.20}$$

3.5.2 Effective Gate Work Function and δt_{inv} At Same V_g

There are different combinations of the implementation of quantum effects into the classical compact model since we have different methods of implementing V_t shift and extracting δt_{inv}. Among them, the simplest combination is implementing V_t shift by effective gate work function and extracting δt_{inv} at the same V_g. At a given bias V_g, we first calculate the classical boundary parameter β^{CL} using (3.14) with $\Delta\phi$ changing to $\Delta\phi + \Delta V_t$. Then, we can obtain Q_i^{CL} through (3.15) and δt_{inv} through (3.11). After updating t_{ox} with t_{ox}^{QM},

$$t_{ox}^{QM}(\beta^{CL}) = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \left(21\varepsilon_{si}\hbar^2 \Big/ m^* q * 16 \frac{\varepsilon_{si}}{t_{si}} \frac{kT}{q} \beta^{CL} \tan\beta^{CL} \right)^{1/3} \tag{3.21}$$

we can calculate the quantum boundary parameter β^{QM}.

$$\begin{aligned} \frac{q\left(V_g - \Delta\phi - \Delta V_t - V\right)}{2kT} - \ln\left[\frac{2}{t_{si}} \sqrt{\frac{2\varepsilon_{si} kT}{q^2 n_i}} \right] \\ = \ln\beta^{QM} - \ln\left[\cos\beta^{QM}\right] + 2\frac{\varepsilon_{si} t_{ox}^{QM}(\beta^{CL})}{\varepsilon_{ox} t_{si}} \beta^{QM} \tan\beta^{QM} \end{aligned} \tag{3.22}$$

Note that both β^{CL} and β^{QM} appear in the above equation. It is extremely difficult to obtain an explicit expression of $dV_g/d\beta^{QM}$ since we can not derive an explicit relationship between $\beta^{CL}$and β^{QM}. Consequently, we are unable to obtain expressions for the drain

current and the gate capacitance. To simplify the problem, we can neglect the involvement between $\beta^{CL}$and β^{QM}. Then, following the same procedure in section 3.4, we can obtain an expression of the drain current

$$I_{ds} = \mu \frac{W}{L} \frac{4\varepsilon_{si}}{t_{si}} \left(\frac{2kT}{q} \right)^2 \times \left[\beta^{QM} \tan \beta^{QM} - \frac{\beta^{QM\,2}}{2} + \frac{\varepsilon_{si} t_{ox}^{QM}\left(\beta^{CL}\right)}{\varepsilon_{ox} t_{si}} \left(\beta^{QM}\right)^2 \tan^2 \beta^{QM} \right]_{\beta_d^{QM},\,\beta_d^{CL}}^{\beta_s^{QM},\,\beta_d^{CL}} \tag{3.23}$$

where β_s^{QM} and β_d^{QM} are the solutions to (3.22) corresponding to V being the source voltage V_s and the drain voltage V_d respectively, and $t_{ox}^{QM}(\beta_s^{CL})$, $t_{ox}^{QM}(\beta_d^{CL})$ are calculated from (3.21) using β_s^{CL}, β_d^{CL} accordingly.

And the gate capacitance is

$$C_g = 4\frac{\varepsilon_{si}}{t_{si}} \frac{\beta^{QM} \sec^2 \beta^{QM} + \tan \beta^{QM}}{\dfrac{1}{\beta^{QM}} + \tan \beta^{QM} + \dfrac{2\varepsilon_{si} t_{ox}^{QM}\left(\beta^{CL}\right)}{\varepsilon_{ox} t_{si}} \left(\beta^{QM} \sec^2 \beta^{QM} + \tan \beta^{QM} \right)} \tag{3.24}$$

By incorporating the quantum corrections, it is possible to generate *I-V* and *C-V* curves from the classical model that resemble the quantum *I-V* and *C-V* curves as shown in Figure 3.12 and 3.13.

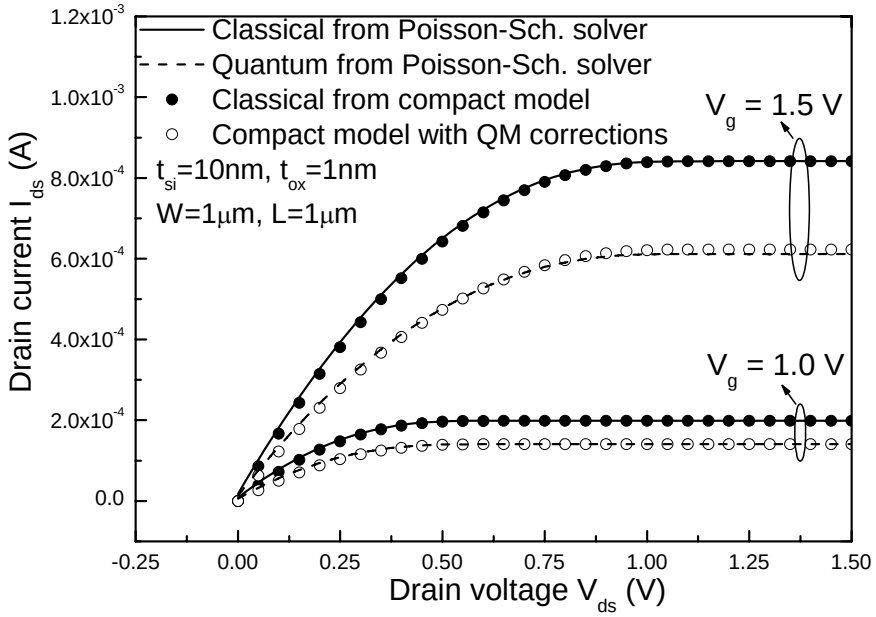


Figure 3.12 I_{ds}-V_{ds} curves obtained from the analytical compact model (symbol) compared with those obtained from the Poisson-Schrodinger solver (line) for a symmetric DG MOSFET at two different gate voltages.

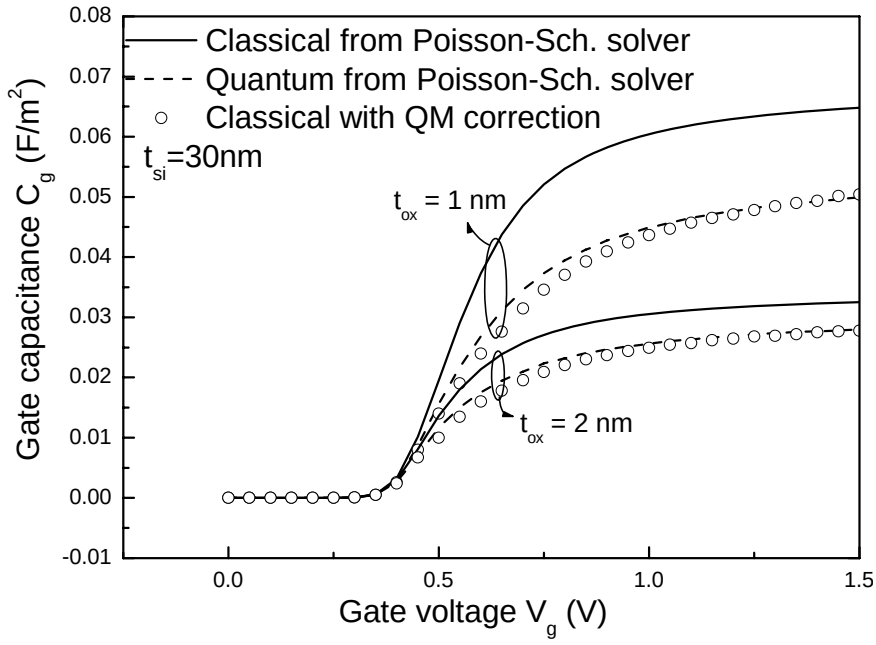


Figure 3.13 Classical (solid line) and quantum *C-V* curves (dotted line) obtained from the Poisson-Schrodinger solver compared with the classical *C-V* curves with quantum corrections (symbol).

3.5.3 Effective Silicon Thickness and δt_{inv} At Same Q_i

We can avoid the differential and integral problem in section 3.5.2 by extracting δt_{inv} at the same Q_i. Quantum effects have been incorporated into the analytic potential model for DG MOSFETs by changing the silicon thickness from t_{si} to t_{si}^{QM} and replacing t_{ox} by $t_{ox}^{QM} = t_{ox}+\delta t_{inv}\varepsilon_{ox}/\varepsilon_{si}$, where t_{si}^{QM} is given by (3.20) and δt_{inv} by (3.11). Since $Q_i = 8(\varepsilon_{si}/t_{si})(kT/q)\beta\tan\beta$, t_{ox}^{QM} depends on the bias voltage through the parameter β^{QM}.

$$\begin{aligned} t_{ox}^{QM}(\beta^{QM}) &= t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\delta t_{inv}\left(\beta^{QM}\right) \\ &= t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{7\varepsilon_{si}\hbar^2 t_{si}^{QM}}{8m^*\varepsilon_{si}kT\beta^{QM}\tan\beta^{QM}}\right)^{1/3} \end{aligned} \tag{3.25}$$

β^{QM} can be solved from the boundary equation (3.14) in its quantum form,

$$\begin{aligned} &\frac{q\left(V_g - \Delta\phi - V\right)}{2kT} - \ln\left[\frac{2}{t_{si}^{QM}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right] \\ &\qquad = \ln\beta^{QM} - \ln\left[\cos\beta^{QM}\right] + 2\frac{\varepsilon_{si}t_{ox}^{QM}}{\varepsilon_{ox}t_{si}^{QM}}\beta^{QM}\tan\beta^{QM} \end{aligned} \tag{3.26}$$

Differentiating (3.26) leads to

$$\frac{dV}{d\beta^{QM}} = -\frac{2kT}{q}\left(\frac{1}{\beta^{QM}} + \tan\beta^{QM} + 2r'\left(\beta^{QM}\sec^2\beta^{QM} + \tan\beta^{QM}\right)\right) \tag{3.27}$$

where

$$r' = \frac{\varepsilon_{si}}{\varepsilon_{ox}t_{si}}\left(t_{ox} + \frac{2}{9}\delta t_{inv}\left(\beta^{QM}\right)\right) \tag{3.28}$$

The quantum drain current is then

$$I_{ds} = \mu \frac{W}{L} \frac{4\varepsilon_{si}}{t_{si}^{QM}} \left(\frac{2kT}{q} \right)^2 \times \left[\beta^{QM} \tan \beta^{QM} - \frac{\left(\beta^{QM}\right)^2}{2} + \frac{\varepsilon_{si}\left(t_{ox} + \frac{12}{45}\delta t_{inv}\left(\beta^{QM}\right)\right)}{\varepsilon_{ox} t_{si}^{QM}} \left(\beta^{QM} \tan \beta^{QM}\right)^2 \right]_{\beta_d^{QM}}^{\beta_s^{QM}} \quad (3.29)$$

where β_s^{QM}, β_d^{QM} are the solutions to (3.26) corresponding to V being the source voltage V_s, and the drain voltage V_d, respectively, $\delta t_{inv}(\beta_s^{QM})$, $\delta t_{inv}(\beta_d^{QM})$ are calculated from (3.25) using β_s^{QM}, β_d^{QM} accordingly.

The effective oxide thickness in which equals $t_{ox} + \frac{12}{45}\delta t_{inv}\left(\beta^{QM}\right)$ is close to $t_{ox}{}^{QM}$ which equals to $t_{ox} + \frac{1}{3}\delta t_{inv}\left(\beta^{QM}\right)$. Changing from one to another only causes small errors (less than 2% even for t_{ox} =1nm). This justified what we did in section 3.5.2. If we do the same simplification here, the current will be

$$I_{ds} = \mu \frac{W}{L} \frac{4\varepsilon_{si}}{t_{si}^{QM}} \left(\frac{2kT}{q} \right)^2 \times \left[\beta^{QM} \tan \beta^{QM} - \frac{\left(\beta^{QM}\right)^2}{2} + \frac{\varepsilon_{si} t_{ox}^{QM}(\beta^{QM})}{\varepsilon_{ox} t_{si}^{QM}} \left(\beta^{QM} \tan \beta^{QM}\right)^2 \right]_{\beta_d^{QM}}^{\beta_s^{QM}} \quad (3.30)$$

The quantum gate capacitance $C_g = dQ_i/dV_g$, is calculated from:

$$C_g = 4\frac{\varepsilon_{si}}{t_{si}} \frac{\beta^{QM} \sec^2 \beta^{QM} + \tan \beta^{QM}}{\frac{1}{\beta^{QM}} + \tan \beta^{QM} + 2r'\left(\beta^{QM} \sec^2 \beta^{QM} + \tan \beta^{QM}\right)} \quad (3.31)$$

SPICE3 simulations have been run to demonstrate the impact of quantum mechanical effects on the gate capacitance and the drain current. Figure 3.14 and Figure 3.15 show the comparison of classical and quantum *C-V* and *I-V* curves obtained from the Poisson-Schrodinger solver and those calculated from the analytic potential compact model with and without the quantum corrections. Both *C-V* and *I-V* curves are in good agreements. Comparing Figure 3.14 and Figure 3.13, we found that by extracting δt_{inv} at same Q_i and calculating C_g using (3.31), a better agreement of the *C-V* curves agreement improve is obtained.

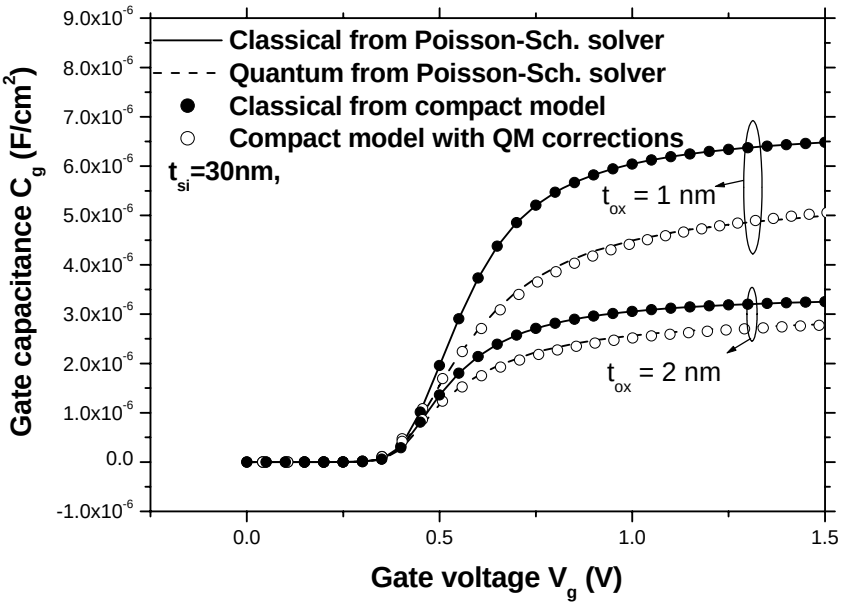


Figure 3.14 Classical (solid line) and quantum *C-V* curves (dotted line) obtained from the Poisson-Schrodinger solver compared with the classical *C-V* curves with quantum corrections (symbol).

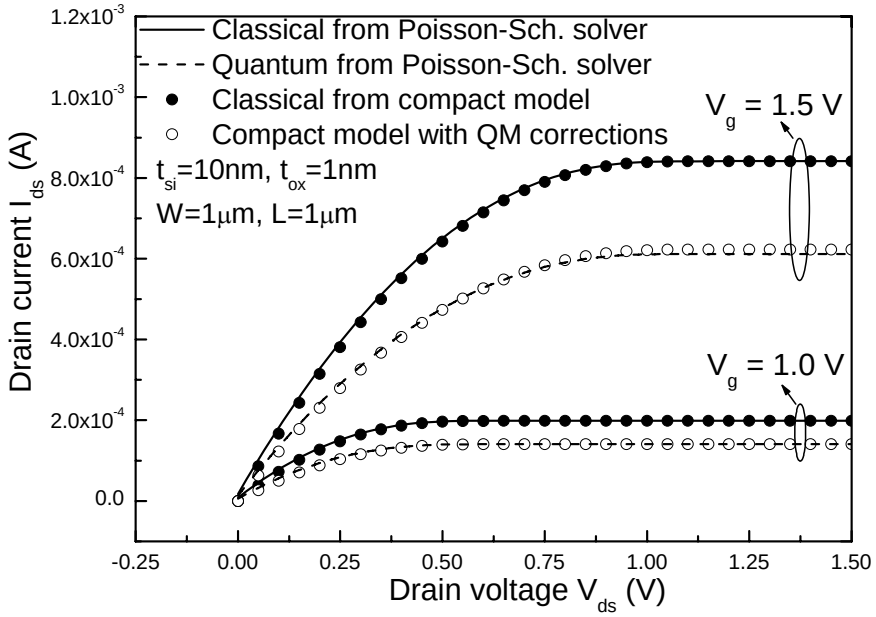


Figure 3.15 I_{ds}-V_{ds} curves obtained from the analytical compact model (symbol) compared with those obtained from the Poisson-Schrodinger solver (line) for a symmetric DG MOSFET at two different gate voltages.

Figure 3.16 shows the waveforms at two successive stages of a CMOS inverter chain in response to a step input signal. The figure plots the pull-up of one stage and the pull-down of the next stage with and without the QM correction. The compact model also includes a parasitic gate to source or drain overlap capacitance of 0.3 fF/μm per gate per edge. It is observed that the propagation delay with QM effects is about 20% longer than that without QM effects for the same V_t. This is because quantum effects degrade the current more than the capacitance, which contains an extrinsic component independent of t_{ox}.

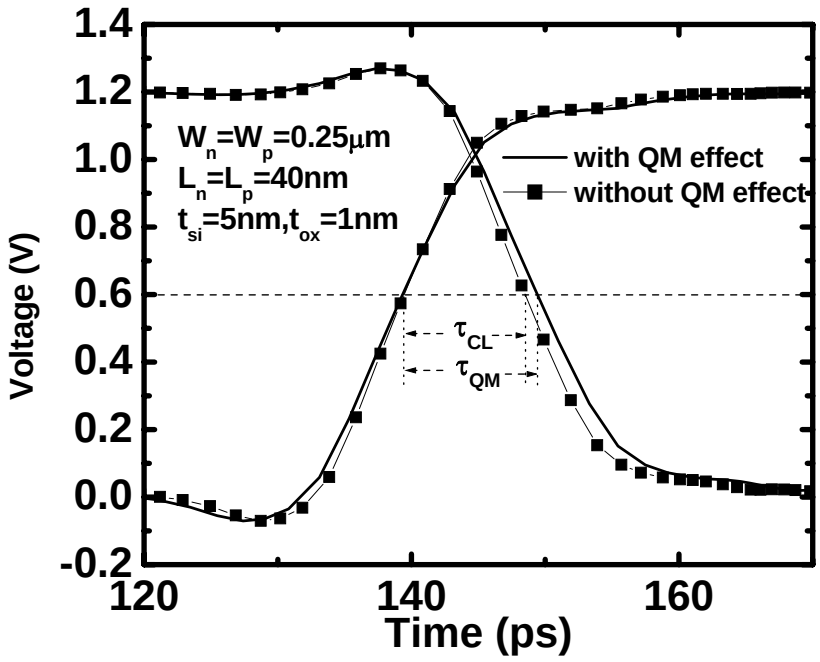


Figure 3.16 Voltage waveforms at successive stages of a DG CMOS inverter chain generated from the analytic potential compact model with quantum effects (solid line) and without quantum effects (line with symbol).

The text of Chapters Three, in part, is a reprint of material that appears as "Compact modeling of quantum effects in symmetric double-gate MOSFETs" by Wei Wang, Huaxin Lu, Shih_Hsien Lo and Yuan Taur, submitted to Solid State Electronics.

Chapter 4

Compact Modeling of Quantum Effects in Asymmetric DG MOSFETs

4.1 Quantum Effects In asymmetric DG MOSFETs

In an asymmetric DG MOSFET, the work functions at the front and back gates are different. As shown in the schematic band diagram (Figure 4.1), the silicon band becomes sloped between the two gates. This leads to a built-in electrical field across the silicon film even at zero gate voltage. In the subthreshold region, this built-in field does not change with the gate voltage. In other words, the silicon bands move as a whole with the applied gate voltage, similar to the symmetric DG MOSFETs where the built-in field is zero. Therefore, the subthreshold slope of asymmetric DG MOSFETs is also 60 mV/decade. Due to the presence of this built-in field, the quantum mechanical behaviors of electrons in asymmetric DG MOSFETs are much different from those in the symmetric devices. The potential well does not behave like an infinite square well because of the slope of the conduction band. Consequently, the electron eigen energy levels are higher with respect to the eigen energy levels in the infinite square well.

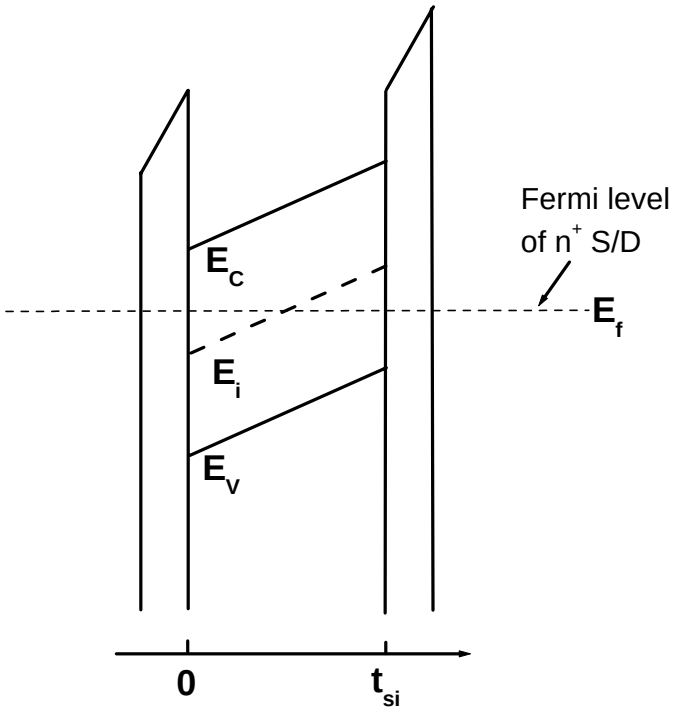


Figure 4.1 Schematic band diagram of an asymmetric DG MOSFET at zero gate voltage. The left gate is assumed to have smaller work function than the right gate

As illustrated in Figure 4.2, the ground state energy of electrons in a n^+p^+ gate MOSFET (the left gate has the same work function as n^+ silicon and the right gate has the same work functions as the p^+ silicon) is much higher than the ground state energy in a symmetric DG MOSFET discussed in Chapter 3. The sloped conduction band causes higher electron population on the left side of the silicon film as shown in Figure 4.2. The centriod of the inversion charge distribution moves closer to the left surface as the built-in field increases, e.g., the two gate work functions become more.

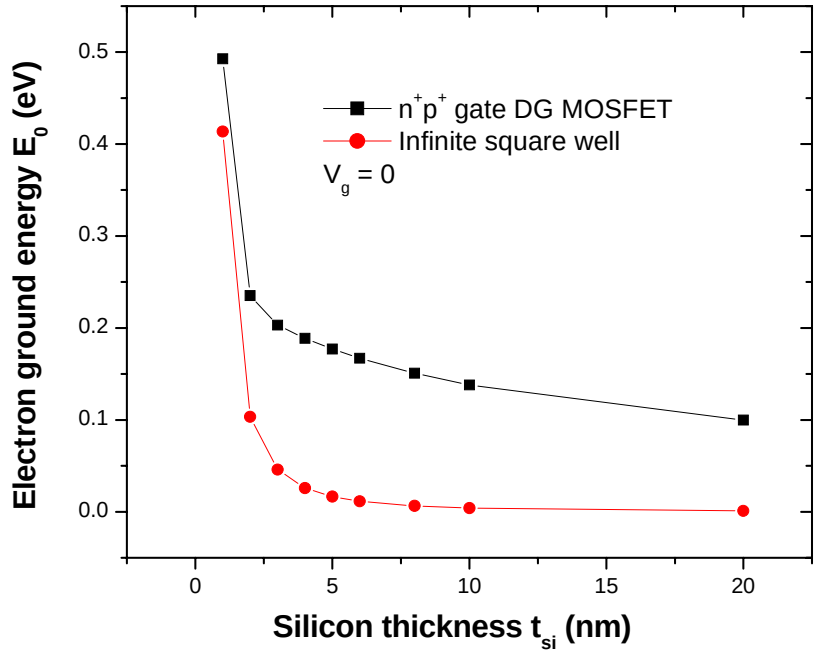


Figure 4.2 The comparison of electron ground state energy between an symmetric DG MOSFET with n^+p^+ gate work functions and an infinite square well.

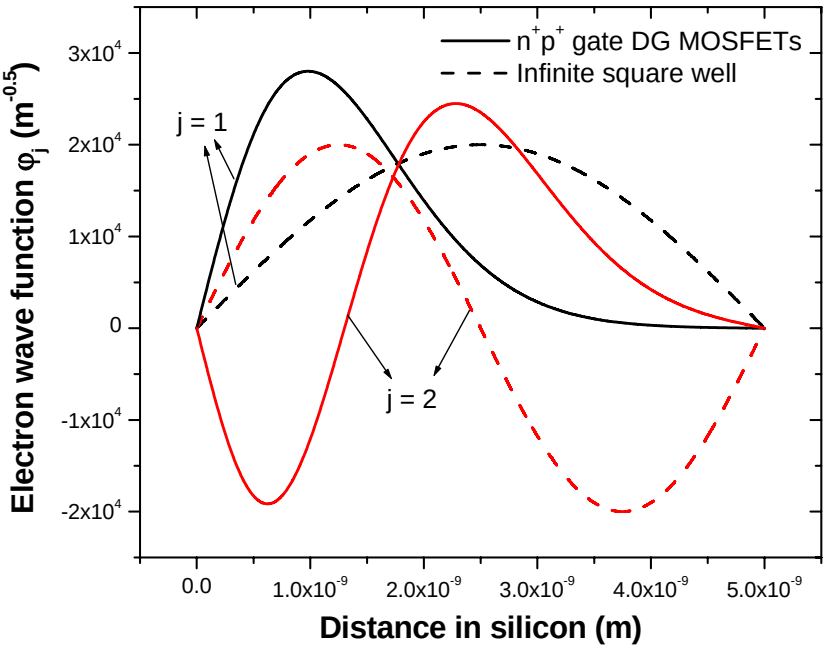


Figure 4.3 Wave function of the first two subband electron in an asymmetric DG MOSFET with n^+p^+ gate work functions compared with that in a corresponding infinite square well.

However, when the silicon film is very thin, the strong confinement in the silicon film causes the centroid to move to the center of the film just like the symmetric device. The electrostatic coupling between the front channel and the back gate is stronger than the classical case since the front channel is closer to the back gate due to quantum effects. Therefore the difference between the Q_i-V_g characteristics of symmetric and asymmetric DG MOSFETs is smaller than the classical case as shown in Figure 4.4.

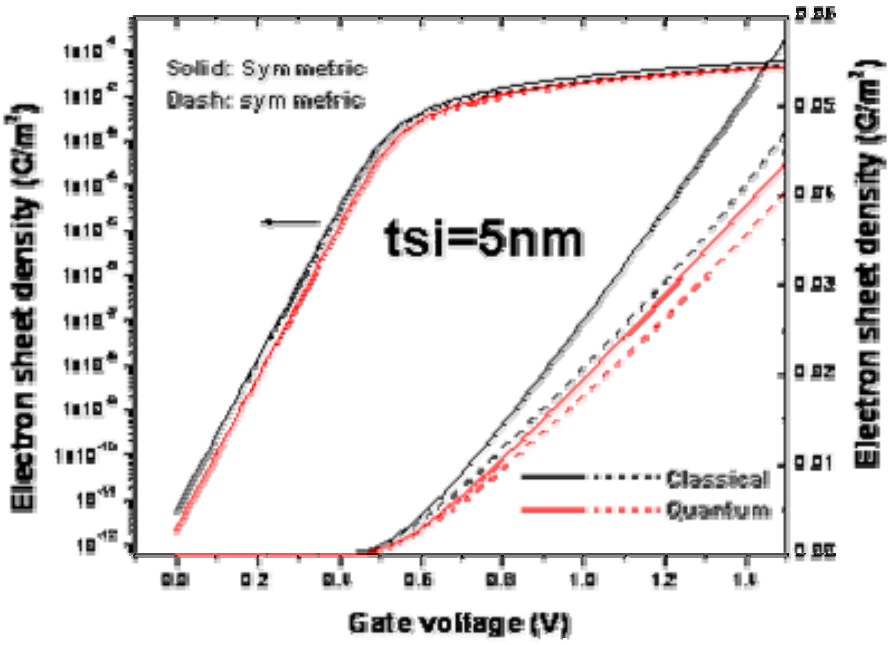


Figure 4.4 Classical and quantum Q_i-V_g curves at both linear (right) and logarithmic (left) scales of symmetric and asymmetric DG MOSFETs. Asymmetric curves are shifted to keep the same off-state condition with the symmetric curves.

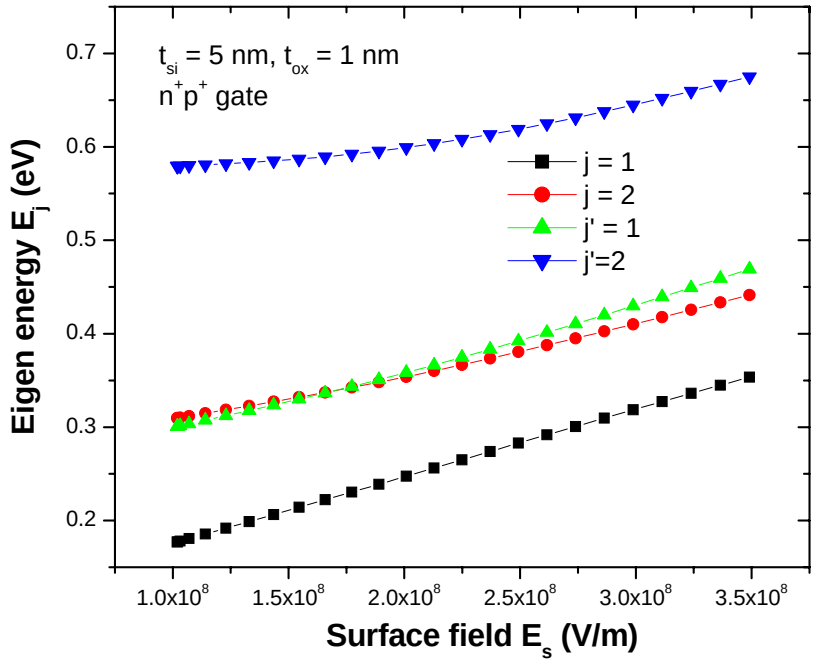


Figure 4.5 The lowest two eigen energy levels in both valleys versus the surface field of an asymmetric DG MOSFET.

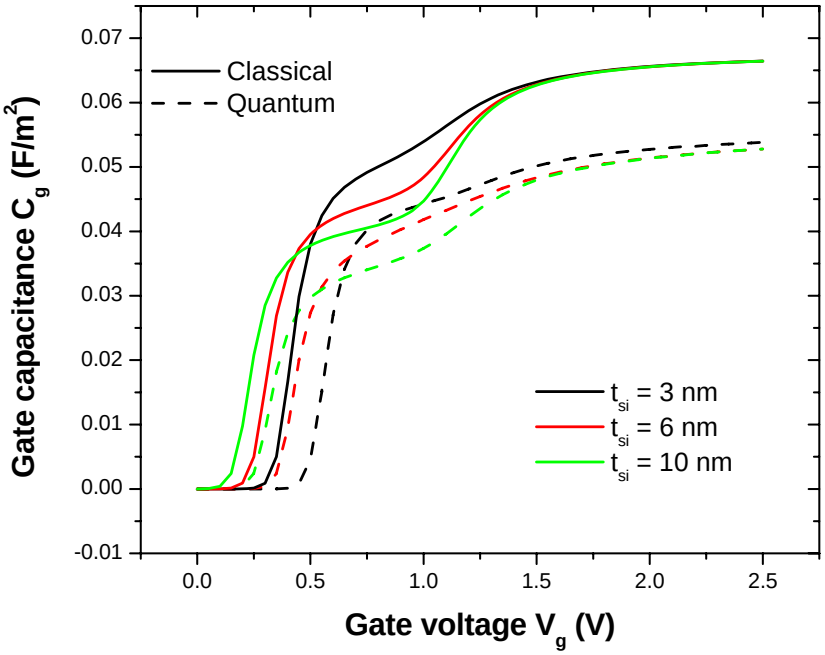
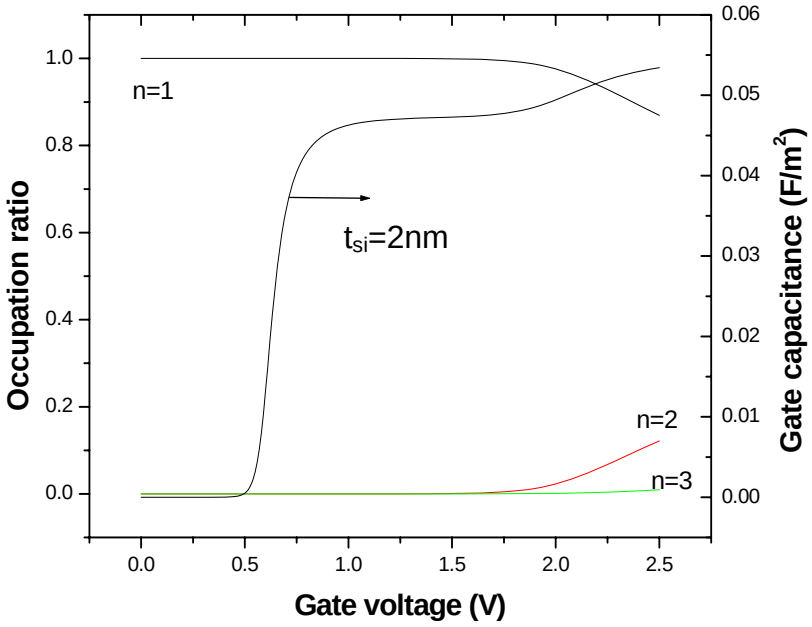
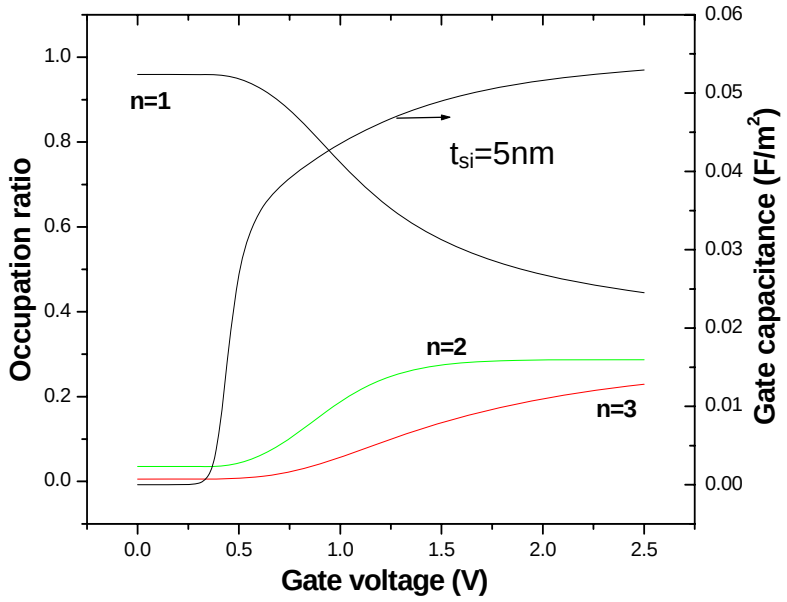


Figure 4.6 Classical and quantum gate capacitance of an asymmetric DG MOSFET with n^+p^+ gate work functions and different silicon thickness.

Beyond the subthreshold region, the surface field increases with increasing gate voltage. As a result, the electron eigen energies increase rapidly as illustrated in Figure 4.5. Due to the asymmetry of the gate work functions, the two gates have different threshold voltage and the gate with smaller work function turns on first. Consequently, the *C*-*V* curves have a step shape around the threshold voltage of the back gate which can be seen clearly from the classical curves in Figure 4.6. It is different in the quantum case. When the silicon film is thick, the step shape in the *C*-*V* curve presents for the same reason. However, the step disappears in the curve with moderate silicon thickness and appears again when the silicon film becomes very thin.



(a)



(b)

Figure 4.7 Electron occupation ratio of the lowest three subbands as a function of the gate voltage for an asymmetric DG MOSFET with two different silicon thickness: (a) t_{si} = 2 nm and (b) t_{si} = 5 nm. The Q_i-V_g curves are also plotted.

The step feature in the thin silicon film case does not arise from the asymmetry of gate work functions. As one can see in Figure 4.7, in the case of thin t_{si}, electrons only populate in the lowest energy subband before the critical V_g where the step occurs. After the critical V_g, electrons start to populate at higher energy subbands and hence, the total charge density increases much more rapidly with increasing V_g, which leads to the step shape in the *C-V* curves. This critical V_g is higher than the threshold voltage when t_{si} is thin. The critical V_g decreases with increasing t_{si} because the differences between the energy subbands become smaller. When t_{si} is larger than 5nm, the critical V_g becomes smaller than the threshold voltage and therefore, no step is observed after device turning on in Figure 4.7 (b).

4.2 Threshold Voltage Shift – Thickness And Field Dependence

4.2.1 Expression Of V_t Shift

As discussed in the last section, the electron eigen energy levels not only depend on the silicon thickness but also depend on the built-in field which comes from the asymmetry of the gate work functions. As a result, the threshold voltage shift due to quantum effects also depends on both the thickness and the field as shown in Figure 4.8. When t_{si} is thick, confinement by the thickness is weak and the field dependence dominates. However, thickness confinement becomes stronger when t_{si} is thinner. In the case of extremely thin t_{si}, the V_t shift is completely dominated by the thickness.

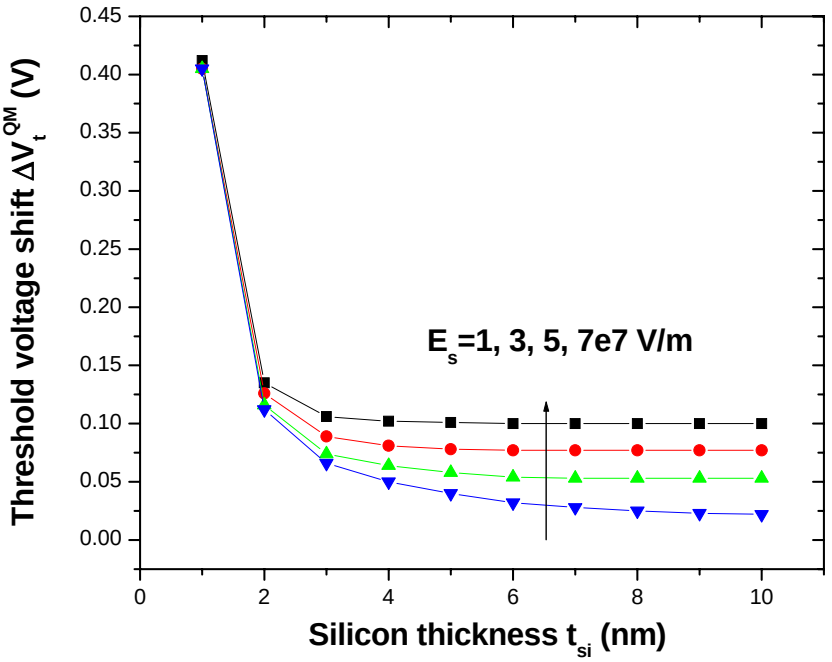


Figure 4.8 Threshold voltage shift due to quantum effects of asymmetric DG MOSFETs with different silicon thickness and built-in field. The data are obtained from the 1-D numerical solver simulation.

An expression of V_t can be obtained using the same procedure as we did for symmetric DG MOSFETs. Due to the built-in field, the potential across the silicon film is

$$\begin{aligned}\psi(x) &= V_g - \Delta\phi_1 - \mathcal{E}_s\left(x + \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}\right) \\ &= V_g - \Delta\phi_1 - \frac{\Delta\phi_2 - \Delta\phi_1}{t_{si} + 2\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}}\left(x + \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}\right)\end{aligned} \tag{4.1}$$

where $\Delta\phi_1$, $\Delta\phi_2$ are the work function of the front gate (the one with lower work function) and the back gate (the one with higher work function) respectively, and $\mathcal{E}_s$ is the built-in field.

Therefore, the classical inversion charge sheet density is

$$Q_i^{CL} = \int_0^{t_{si}} n_i e^{q\psi(x)/kT} dx = n_i \frac{kT}{q} \frac{1}{\varepsilon_s} e^{\frac{q}{kT}\left(V_g - \Delta\phi_1 - \frac{\varepsilon_{si}}{\varepsilon_{ox}}\mathcal{E}_s t_{ox}\right)} \left(1 - e^{-\frac{q\mathcal{E}_s}{kT}t_{si}}\right) \tag{4.2}$$

The quantum inversion charge sheet density is given by

$$\begin{aligned} Q_i^{QM} &= \frac{qkT}{\pi\hbar^2}\left\{ gm_d \sum_j \ln\left(1 + e^{(E_f - E_j)/kT}\right) + g'm_d' \sum_{j'} \ln\left(1 + e^{(E_f - E_j')/kT}\right)\right\} \\ &= \frac{qkT}{\pi\hbar^2}\left\{ gm_d + g'm_d' e^{-(E_1' - E_1)/kT}\right\} e^{\frac{q}{kT}\left(V_g - \Delta\phi_1 - \frac{\varepsilon_{si}}{\varepsilon_{ox}}\mathcal{E}_s t_{ox} - \frac{E_g}{2} - E_1\right)} \end{aligned} \tag{4.3}$$

Through the classical and quantum charge density, one can obtain the expression of the threshold voltage shift due to quantum effects.

$$\Delta V_t = \frac{\mathcal{E}_s t_{si}}{2} \ln\left(\frac{n_i \pi\hbar^2 \left(1 - e^{-\frac{q\mathcal{E}_s}{kT}t_{si}}\right)}{q\mathcal{E}_s \left(gm_d + g'm_d' e^{-(E_1' - E_1)/kT}\right)} \right) + \frac{E_g}{2q} + \frac{E_1}{q} - \frac{\mathcal{E}_s t_{si}}{2} \tag{4.4}$$

In the above equations, only the lowest subbands in both valleys are kept. However, one needs to find out E_1 to calculate the threshold voltage shift.

4.2.2 E_1 Calculation – Airy Function Approach

Comparing an asymmetric DG MOSFET in the subthreshold region with that of a traditional triangular well, one finds that the Schrodinger equation is the same. The boundary condition at $x = 0$ is also the same and the only difference comes from the right boundary condition – zero wave function at infinity for triangular well and zero wave

function at $x = t_{si}$ for asymmetric DG MOSFET. The Schrodinger equation in a triangular potential well in the moment space can be solved rigorously.

$$\frac{p^2}{2m}\varphi(p) + i\hbar\mathcal{E}_s\frac{d}{dp}\varphi(p) = E\varphi(p) \tag{4.5}$$

The solution is the wave function at the moment space $\varphi(p)$.

$$\varphi(p) = A\exp\left[\frac{i}{\hbar\mathcal{E}_s}\left(\frac{p^3}{6m} - E\,p\right)\right] \tag{4.6}$$

where A is the normalization constant. The wave function in the spatial coordinate space can then be calculated as

$$\begin{aligned}\varphi(x) &= \frac{1}{\sqrt{2\pi\hbar}}\int_{-\infty}^{+\infty}\varphi(p)\,e^{ipx/\hbar}dp \\ &= \frac{A}{\sqrt{2\pi\hbar}}\int_{-\infty}^{+\infty}\exp\frac{i}{\hbar}\left[\frac{p^3}{6m^*\mathcal{E}_s}\left(x - \frac{E}{\mathcal{E}_s}\right)p\right]dp \\ &= \frac{A'}{\sqrt{\pi}}\int_0^{+\infty}\cos\left(\frac{u^3}{3} + u\xi\right)du\end{aligned} \tag{4.7}$$

where

$$u = p\left(2\hbar m\mathcal{E}_s\right)^{-1/3} \tag{4.8}$$

$$\xi = \left(x - \frac{E}{\mathcal{E}_s}\right)\left(\frac{2m\mathcal{E}_s}{\hbar^2}\right)^{-1/3} \tag{4.9}$$

and A' is another normalization constant. Note the right side of (4.7) without the constant A' is exactly the *Airy* function with the variable ξ. In the triangular potential well, the ground eigen energy level can be calculated from the highest zero point (excluding the infinity) of the Airy function using (4.9), and the second eigen energy level can be

calculated from the second largest zero point and so on. In an asymmetric DG MOSFET with the built-in field, the situation is much more complicated due to the right boundary condition at $x = t_{si}$. However, the eigen energy levels should still relate to the zero points of the *Airy* function through. For every eigen energy level, there also exists a down limit which equals to the corresponding energy level of an infinite square well. This is caused by the thickness confinement. In other words, the ground state energy can be found as the largest number which satisfies the following conditions.

$$Airy\left[\frac{E_1}{\mathcal{E}_s}\left(\frac{2m\mathcal{E}_s}{\hbar^2}\right)^{-1/3}\right]=0 \tag{4.10}$$

$$Airy\left[\left(t_{si}-\frac{E_1}{\mathcal{E}_s}\right)\left(\frac{2m\mathcal{E}_s}{\hbar^2}\right)^{-1/3}\right]=0 \tag{4.11}$$

$$E_1 > \frac{\hbar^2\pi^2}{2mt_{si}^{\ 2}} \tag{4.12}$$

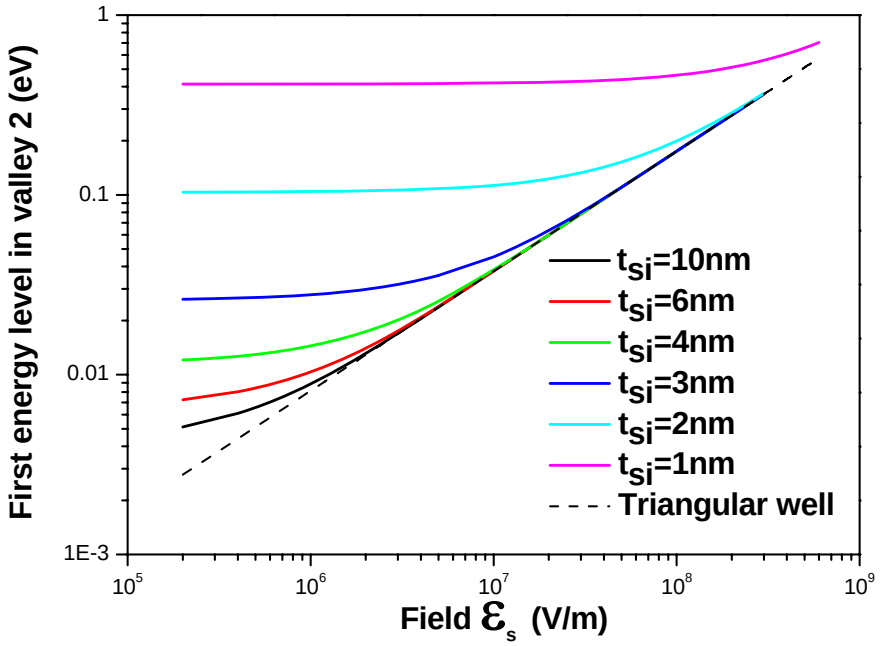


Figure 4.9 Electron ground state energy as a function of the built-in field of an asymmetric DG MOSFET with different silicon thickness. The dashed line the ground energy of the triangular potential well.

It is difficult to give an expression of the ground state energy although we can obtain it by a table-lookup method. For compact modeling, we need to know E_1 as a closed form function so that we can calculate the V_t shift through (4.4). As discussed before, the field confinement dominates when the field is very high and the thickness confinement dominates when the thickness is very thin and the field is not that high. From Figure 4.9, one can observer the fact that the ground state energy eventually equals the ground energy of the triangular well when the field is high enough for different silicon thickness. A simple fitting expression can then be given based on this observation.

$$E_1 = \left(E_{thickness} \left(t_{si} \right)^n + E_{field} \left(\mathcal{E}_s \right)^n \right)^{1/n} \tag{4.13}$$

Where n = 3/4 is a fitting parameter, $E_{thickness}(t_{si}) = \frac{\hbar^2 \pi^2}{2mt_{si}^2}$ and $E_{field}(\mathcal{E}_s)$ are the ground state energy of the infinite square well and triangular well, respectively.

$$E_{field}(\mathcal{E}_s) = \gamma_1 \left(\frac{\hbar^2 q^2 \mathcal{E}_s^2}{2m} \right)^{1/3} \tag{4.14}$$

Here γ_1 is the largest zero point of the *Airy* function. Figure 4.10 shows the ground energy of electrons calculated by (4.13) in the two-fold valley, compared with data obtained from the solver directly. Using E_1 (and E_1' with m') calculated from (4.13), one can calculate the V_t shift through (4.4). The comparison between the calculated V_t shift and those obtained from the solver is shown in Figure 4.11. As one can see, both the ground energy and V_t agree with the simulation results well.

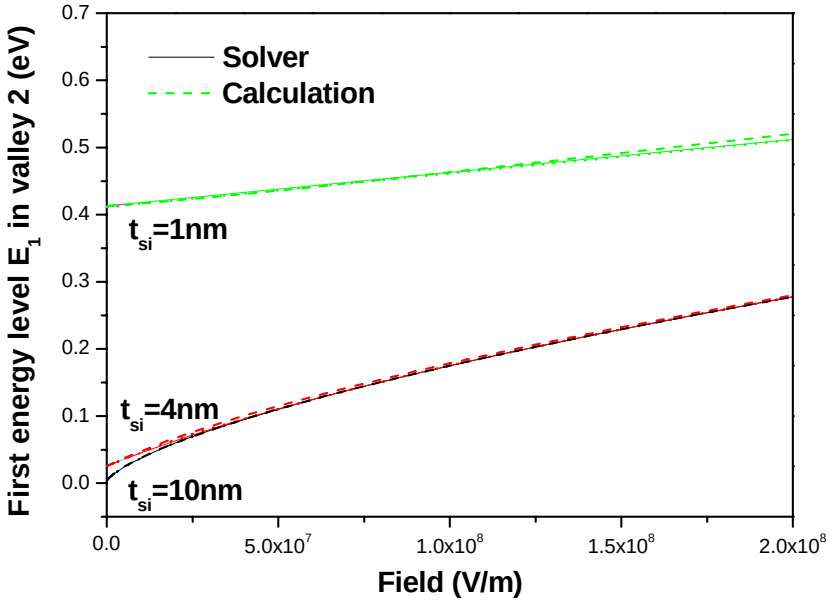


Figure 4.10 Comparison of the electron ground energy calculated by (4.13) with those obtained from the solver for an asymmetric DG MOSFET with different silicon thickness.

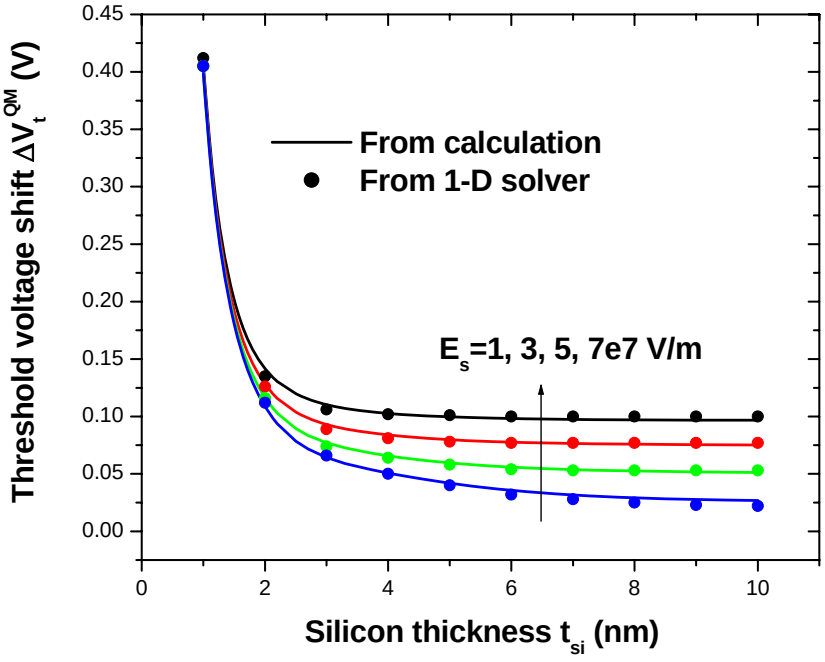


Figure 4.11 Comparison of the threshold voltage shift due to quantum effects calculated by (4.4) and those obtained from the solver directly for an asymmetric DG MOSFET.

4.2.3 E_1 Calculation – Variation Approach

Since we are mostly interested at the electron ground state energy, the variation method can also be used for the energy calculation. Based on the quantum confinement trends in the high field and thin silicon limits, a trial wave function is

$$\varphi(x) = a\sin\left(\frac{\pi x}{t_{si}}\right)e^{-bx} \tag{4.15}$$

where the coefficient a can be calculated through the normalization.

$$a = \frac{2}{\pi}\sqrt{\frac{b\left(\pi^2 + b^2 t_{si}^2\right)e^{2bt_{si}}}{-1+e^{2bt_{si}}}} \tag{4.16}$$

The expectation values of the kinetic and potential energies are

$$\left\langle E_k \right\rangle = -\frac{\hbar^2}{2m}\int_0^{t_{si}} \varphi(x)\frac{d^2\varphi(x)}{dx^2}dx = \frac{\hbar^2\pi^2}{2mt_{si}^2} + \frac{\hbar^2 b^2}{2m} \tag{4.17}$$

and

$$\begin{aligned}\left\langle E_p \right\rangle &= \int_0^{t_{si}} \varphi(x) q\mathcal{E}_s x\varphi(x)\,dx \\ &= \frac{q\mathcal{E}_s}{2b} - \frac{q\mathcal{E}_s t_{si}}{-1+e^{2bt_{si}}} + \frac{q\mathcal{E}_s b t_{si}^2}{\pi^2 + b^2 t_{si}^2}\end{aligned} \tag{4.18}$$

The expectation value of the electron ground energy is then

$$\begin{aligned}E_1 &= \left\langle E_k \right\rangle + \left\langle E_p \right\rangle \\ &= \frac{\hbar^2\pi^2}{2mt_{si}^2} + \frac{\hbar^2 b^2}{2m} + \frac{q\mathcal{E}_s}{2b} - \frac{q\mathcal{E}_s t_{si}}{-1+e^{2bt_{si}}} + \frac{q\mathcal{E}_s b t_{si}^2}{\pi^2 + b^2 t_{si}^2}\end{aligned} \tag{4.19}$$

According to the variation principle, the variation parameter b should minimize the energy E_1, i.e.,

$$\frac{dE_1}{db} = 0 \tag{4.20}$$

This nonlinear equation is difficult to be solved analytically. Using the asymptotic behavior of (4.19) as $t_{si} \sim \infty$, b is approximated as

$$b = \left(\frac{3mq\mathcal{E}_s}{\hbar^2}\right)^{1/3} \tag{4.21}$$

However, the ground energy calculated through (4.21) and (4.19) does not agree the simulation results well when t_{si} is thin because of the approximation used for (4.21).

4.3 Gate Capacitance Degradation – Equivalent Capacitance Model

4.3.1 Equivalent Small Signal Capacitance Circuit

In asymmetric DG MOSFETs, there exists electrical coupling between the two gates and the inversion channels. This coupling makes the inversion charge distribution and gate capacitance behaviors much more complicated than in symmetric DG MOSFETs. For a comprehensive picture of the charge coupling between the gates and the channels, a small-signal equivalent capacitance circuit is developed for the asymmetric DG MOSFETs under equilibrium. Figure 4.12 illustrates such a circuit, where ψ_{s1} and ψ_{s2} are the potential in the silicon surfaces, $Q_1 = -\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=0}$ and $Q_2 = \varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=t_{si}}$ are the charges in the front and back gate, respectively. Except for the two inversion capacitances C_{i1} and C_{i2}, there is an additional capacitance C_{si} in Figure 4.12, which represents the coupling between the gates and the inversion channels. The Δ–type network adopted in Figure 4.12 is a physical representation of the linear relationship between the small signal quantities $(\delta Q_1, \delta Q_2)$ and $(\delta\psi_{s1}, \delta\psi_{s2})$. From the equivalent circuit, one can write

$$\begin{pmatrix} \delta Q_1 \\ \delta Q_2 \end{pmatrix} = \begin{pmatrix} C_{i1} + C_{si} & -C_{si} \\ -C_{si} & C_{i2} + C_{si} \end{pmatrix} \begin{pmatrix} \delta\psi_{s1} \\ \delta\psi_{s2} \end{pmatrix} \tag{4.22}$$

Similarly, one can also obtain the linear relationship between the small signal quantities $(\delta Q_1, \delta Q_2)$ and $(\delta V_{g1}, \delta V_{g2})$

$$\begin{pmatrix} \delta Q_1 \\ \delta Q_2 \end{pmatrix} = \frac{C_{ox}}{M} \begin{pmatrix} C_{i1}+C_{si} & -C_{si} \\ -C_{si} & C_{i2}+C_{si} \end{pmatrix} \begin{pmatrix} C_{ox}+C_{i1}+C_{si} & C_{si} \\ C_{si} & C_{ox}+C_{i2}+C_{si} \end{pmatrix} \begin{pmatrix} \delta V_{g1} \\ \delta V_{g2} \end{pmatrix} \quad (4.23)$$

where

$$M = \left(C_{ox}+C_{i1}+C_{si}\right)\left(C_{ox}+C_{i2}+C_{si}\right) - C_{si}^2 \quad (4.24)$$

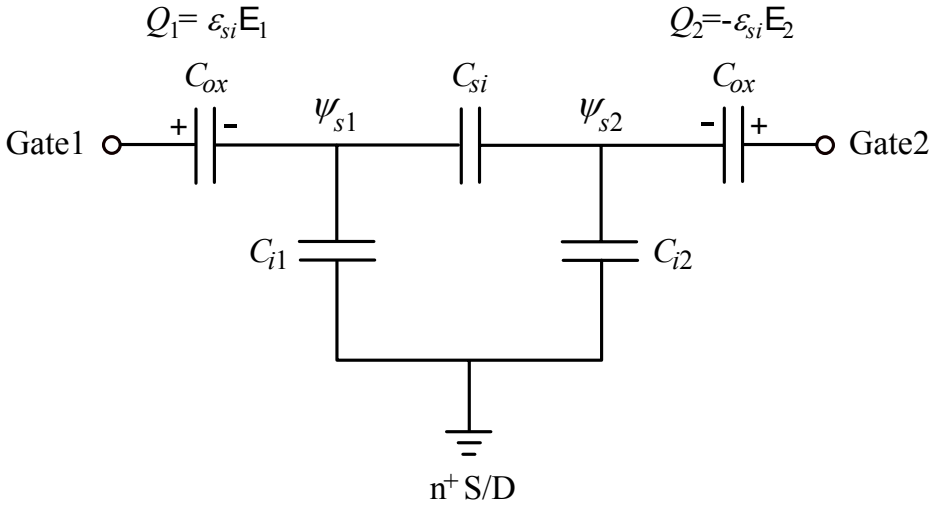


Figure 4.12 Schematic small signal capacitance equivalent circuit of an asymmetric DG MOSFET under equilibrium condition, i.e., there is no current flow between the source and the drain.

The three components of capacitance behave differently with increasing gate voltage as shown in Figure 4.13. In the subthreshold region, the inversion charge is negligible and so are the inversion capacitance C_{i1} and C_{i2}. On the other hand, C_{si} equals to ε_{si}/t_{si}, which means that the charge coupling is between the two gates. When V_g is above the threshold voltage, C_{i1} increases rapidly. Note that C_{i2} increases slowly because of the charge coupling. In the meantime, C_{si} starts to decrease because of the screening of the gate field by the front channel. When V_g is higher than the threshold voltage of the back

gate, the second channel forms and C_{i2} rises rapidly as well. However, C_{si} becomes negligible due to the strong screening by the two inversion channels.

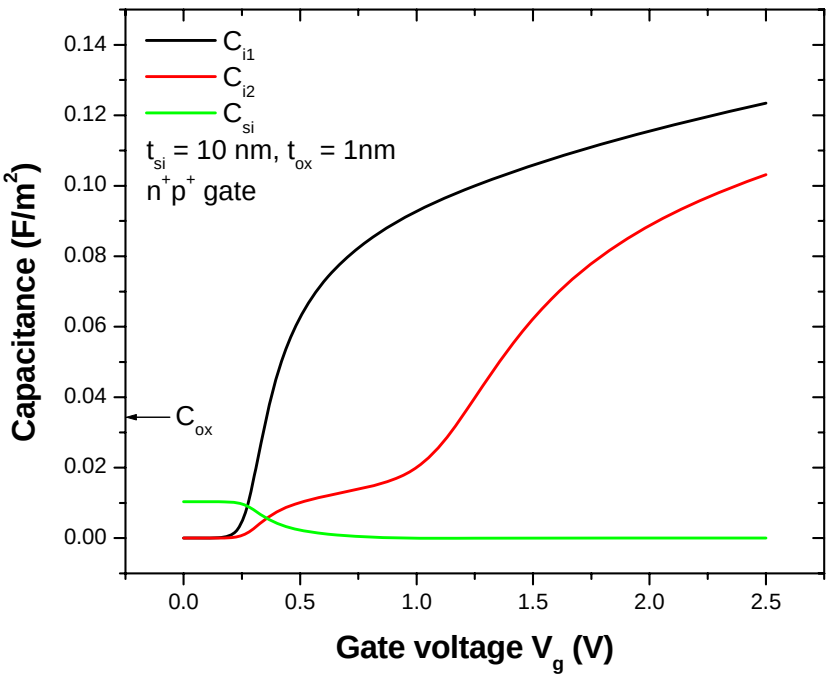
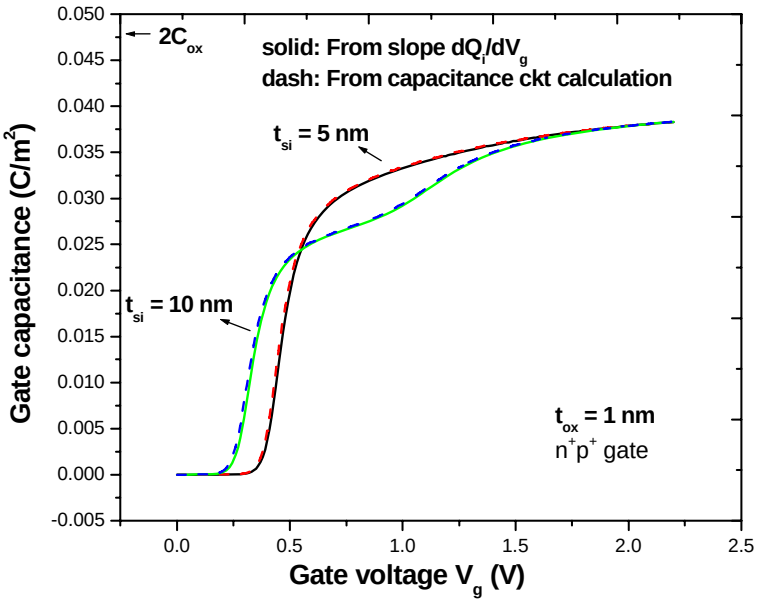


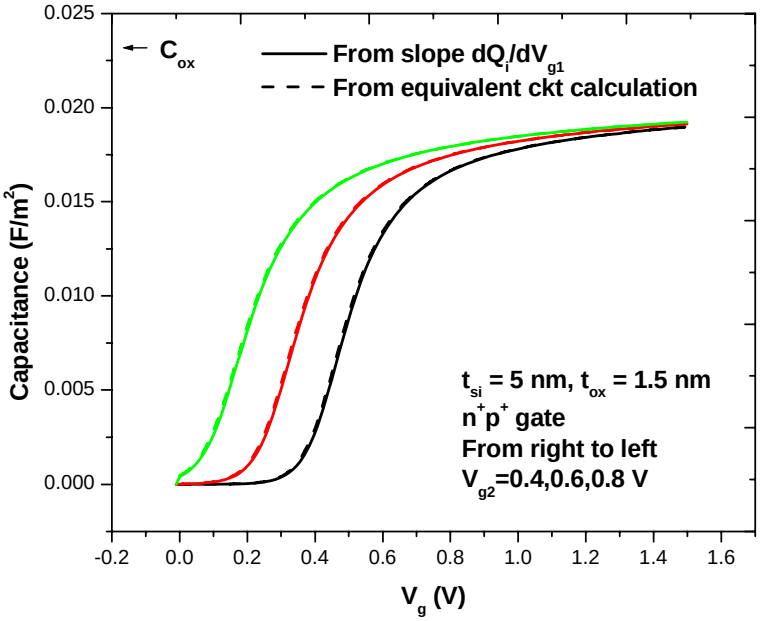
Figure 4.13 Capacitance components C_{i1}, C_{i2}, and C_{si} versus the gate voltage for an asymmetric DG MOSFET of t_{si} = 10 nm with n^+/p^+ poly gates.

The equivalent capacitance circuit is valid for both three-terminal and four-terminal asymmetric DG MOSFETs. In Figure 4.14(a), the two gates are tied together and switched simultaneously. The gate capacitance is larger than C_{ox} as expected since there are two inversion channels. In the four-terminal case (Figure 4.14(b)), the back gate is biased at a constant voltage below the back gate threshold voltage and only the front gate is switched. Consequently, the gate capacitance is smaller than C_{ox} since only one inversion channel is formed. However, it is clear that the back gate bias can affect the threshold voltage of the device through the charge coupling between the front channel

and the back gate. The solid line is the slope of $Q_i - V_g$ curve obtained from the solver and the dashed line is from the equivalent circuit calculation. In both cases, the calculated curves agree well with the data from the solver.



(a)



(b)

Figure 4.14 Comparison of the gate capacitance obtained from the solver and calculated using the equivalent circuit for (a) three-terminal and (b) four-terminal asymmetric DG MOSFETs

4.3.2 Equivalent Inversion Layer Thickness

To further illustrate the meaning of the capacitance components, we define the equivalent inversion layer thickness t_{inv1}, t_{inv2} for the two inversion channels such that

$$\int_0^{t_{si}} x \frac{\partial n(x)}{\partial \psi_{s1}} dx = t_{inv1} \frac{\partial}{\partial \psi_{s1}} \int_0^{t_{si}} n(x) dx \tag{4.25}$$

and

$$\int_0^{t_{si}} x \frac{\partial n(x)}{\partial \psi_{s2}} dx = (t_{si} - t_{inv2}) \frac{\partial}{\partial \psi_{s2}} \int_0^{t_{si}} n(x) dx \tag{4.26}$$

where $n(x)$ is the inversion charge density. In other words, t_{inv1} is the center of mass of the incremental charge in response to the incremental change in ψ_{s1}, and t_{si} - t_{inv2} is the center of mass of the incremental charge in response to the incremental change in ψ_{s2}. Making use of the Poisson's equation and the matrix definition (4.22), one can obtain a general relationship between the capacitance components.

$$\frac{t_{inv1}}{\varepsilon_{si}} C_{i1} = \frac{t_{inv2}}{\varepsilon_{si}} C_{i2} = 1 - \frac{t_{si}}{\varepsilon_{si}} C_{si} \tag{4.27}$$

As discussed previously, C_{si} becomes negligible after both surfaces are strongly inverted. Therefore, the inversion capacitances are given by the distance between the charge centroids and the respective surfaces.

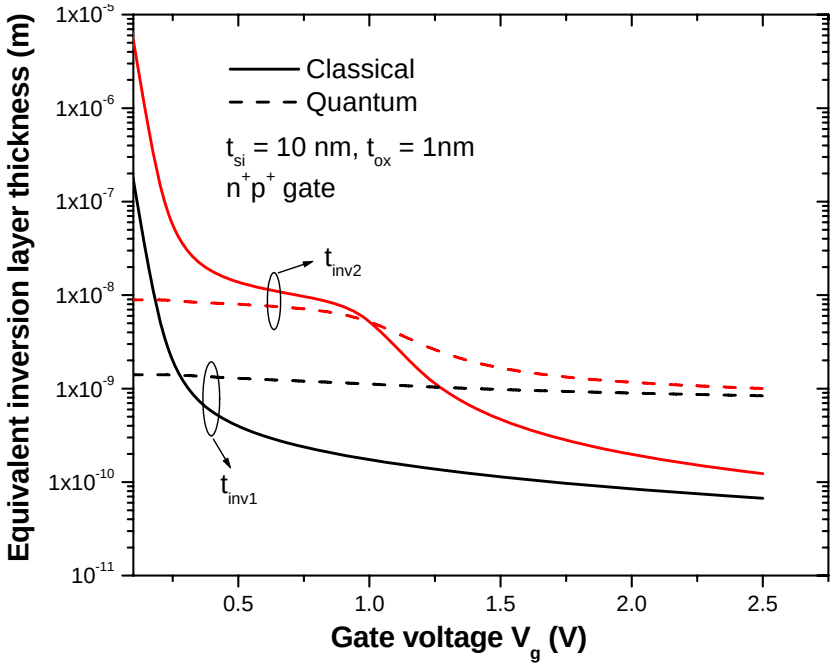


Figure 4.15 Quantum equivalent inversion layer thickness versus the gate voltage for an asymmetric DG MOSFET of t_{si} = 10 nm, t_{ox} = 1 nm with n^+/p^+ poly gates.

Figure 4.15 shows the equivalent inversion layer thickness calculated from (4.27). Note there is a distinct plateau for V_g values between the front and the back threshold voltages in both classical and quantum case. This plateau implies that the back gate also contributes to the inversion charge in the front channel through charge coupling between them. On the other hand, t_{inv1} does not change significantly with increasing gate voltage after strong inversion. Due to quantum effects, the inversion charge in the left channel is at a distance away from the left surface. Therefore, the quantum t_{inv1} is always larger than the classical t_{inv1} and the quantum C_{i1} is smaller than the classical C_{i1} accordingly (Figure 4.16). The t_{inv2} and C_{i2} behavior is more complex. Before the back gate turns on, the quantum coupling between the front channel and the back gate is stronger than the classical case because they become closer to each other. As a result, the quantum t_{inv2} is

smaller than the classical t_{inv2} and the quantum C_{i2} is smaller than the classical C_{i2} accordingly (Figure 4.17). After the back gate turns on, the classical and quantum t_{inv2} , C_{i2} become similar to t_{inv1} , C_{i1} because the back channel is further away from the right surface.

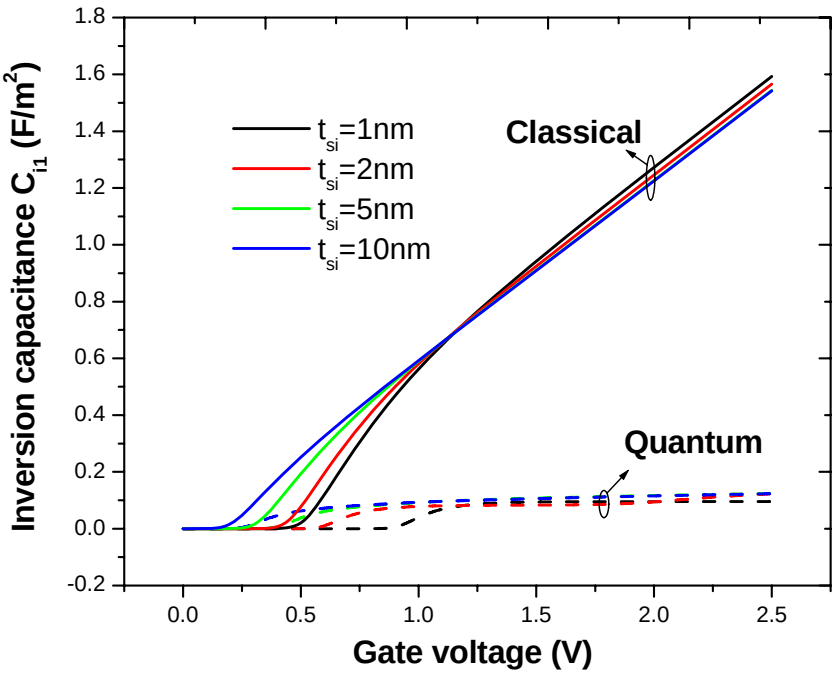


Figure 4.16 Front channel inversion capacitance versus the gate voltage for an asymmetric DG MOSFET with different silicon thickness.

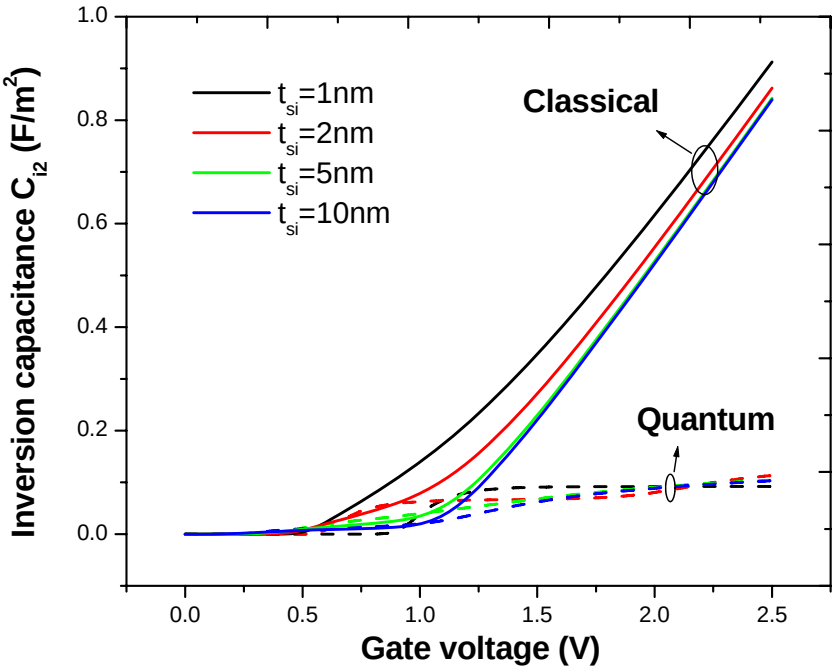


Figure 4.17 Back channel inversion capacitance versus the gate voltage for an asymmetric DG MOSFET with different silicon thickness.

4.4 Analytical Classical Potential Model

In an asymmetric DG MOSFET, the solution of the Poisson's equation at high gate voltage is

$$\psi(x) = V - \frac{2kT}{q}\ln\left[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\sin\left(\frac{2\beta x}{t_{si}}+\alpha\right)\right] \qquad \text{Large } V_g - V \tag{4.28}$$

where α and β are constants to be determined from the boundary conditions

$$\varepsilon_{ox}\frac{V_g - \Delta\phi_1 - \psi_{s1}}{t_{ox}} = -\varepsilon_{si}\frac{d\psi}{dx}\Big|_{x=0} \equiv \varepsilon_{si}\mathcal{E}_1 \tag{4.29}$$

$$\varepsilon_{ox}\frac{V_g - \Delta\phi_2 - \psi_{s2}}{t_{ox}} = \varepsilon_{si}\frac{d\psi}{dx}\Big|_{x=t_{si}} \equiv -\varepsilon_{si}\mathcal{E}_2 \tag{4.30}$$

From (4.28), one can obtain the potential in the two surfaces

$$\begin{cases} \psi_{s1} = V + \dfrac{kT}{q}\ln\left(\dfrac{2\varepsilon_{si}kT}{q^2 n_i {t_{si}}^2}\right) + \dfrac{2kT}{q}\ln\left\{\dfrac{2\beta}{\sin(\alpha-\beta)}\right\} \\ \psi_{s2} = V + \dfrac{kT}{q}\ln\left(\dfrac{2\varepsilon_{si}kT}{q^2 n_i {t_{si}}^2}\right) + \dfrac{2kT}{q}\ln\left\{\dfrac{2\beta}{\sin(\alpha+\beta)}\right\} \end{cases} \tag{4.31}$$

and the electrical field as well.

$$\begin{cases} E_1 = \dfrac{4kT}{qt_{si}}\beta\cot(\alpha-\beta) \\ E_2 = \dfrac{4kT}{qt_{si}}\beta\cot(\alpha+\beta) \end{cases} \tag{4.32}$$

Substituting (4.31) into the boundary condition and summing (4.29) and (4.30), one has

$$f(\alpha,\beta) \equiv \ln\left[\frac{\sin(\alpha+\beta)}{\sin(\alpha-\beta)}\right] + 2r\beta\left[\cot(\alpha-\beta)+\cot(\alpha+\beta)\right] - \frac{q(\Delta\phi_2-\Delta\phi_1)}{2kT} = 0 \tag{4.33}$$

And from (4.29), one can obtain

$$V_g - V = \Delta\phi_1 + \frac{kT}{q}\ln\left(\frac{2\varepsilon_{si}kT}{q^2 n_i {t_{si}}^2}\right) + \frac{2kT}{q}\ln\left\{\frac{2\beta}{\sin(\alpha-\beta)}\right\} + \frac{4kT}{q}r\beta\cot(\alpha-\beta) \tag{4.34}$$

where $r = \varepsilon_{ox}t_{si} / \varepsilon_{si}t_{ox}$. Based on the Gauss's law, the total inversion charge is

$$Q_i = \varepsilon_{si}(\mathcal{E}_1 - \mathcal{E}_2) = \frac{4\varepsilon_{si}kT}{qt_{si}}\beta\left[\cot(\alpha-\beta)-\cot(\alpha+\beta)\right] \tag{4.35}$$

The current can be obtained by integrating Q_i along the channel

$$I_{ds} = \mu\frac{W}{L}\int_{V_s}^{V_d} Q_i(V)dV \tag{4.36}$$

At low gate voltage, the potential solution becomes

$$\psi(x) = V - \frac{2kT}{q}\ln\left[\frac{t_{si}}{2\beta^*}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\sinh\left(\frac{2\beta^* x}{t_{si}} + \alpha^*\right)\right] \quad \text{Small } V_g - V \tag{4.37}$$

However, following the same procedure from (4.31) to (4.36), we can also obtain the drain current for the low gate voltage case. Figure 4.18 compares the drain current from the analytical potential model and the 2-D ISE simulation results.

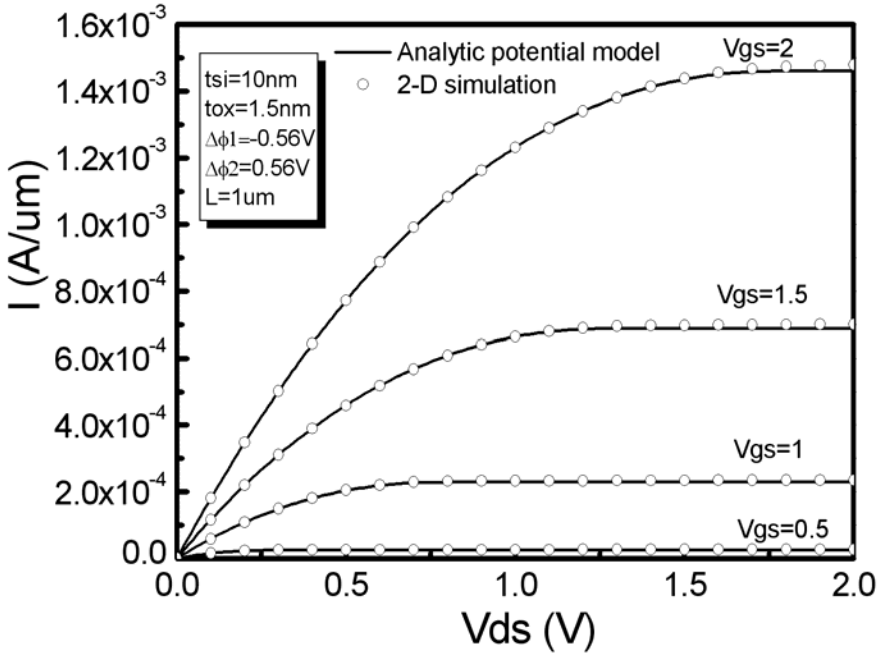


Figure 4.18 Classical $I_{ds} - V_{ds}$ characteristics from the compact model compared with the 2-D numerical simulation results (ISE) for an asymmetric DG MOSFET.

4.5 Implementation Of Quantum Effects In The Compact Model

The quantum threshold voltage shift can be implemented into the classical model by change V_t to $V_t + \Delta V_t$, where ΔV_t is calculated through (4.4) with E_1 obtained from (4.13). It is difficult to obtain C_{i1}, C_{i2}, and C_{si} as close form functions of the device parameters due to their complicated behaviors. As a result, the quantum gate capacitance degradation

is difficult to be implemented into the classical model. However, for the first order approximation, we can use a constant oxide thickness change δt_{ox} for the gate capacitance degradation implementation. Note that the built-in field decreases due to the increasing oxide thickness, which decreases the classical inversion charge density. In other words, an additional threshold voltage shift will be produced by changing t_{ox} to $t_{ox} + \delta t_{ox}$. The definition of this additional threshold voltage $\Delta V_t^{'}$ is

$$Q_i^{CL}\left(V_g, t_{ox}\right) = Q_i^{CL}\left(V_g + \Delta V_t^{'}, t_{ox} + \delta t_{ox}\right) \tag{4.38}$$

Using (4.2), one can calculate $\Delta V_t^{'}$ as

$$\Delta V_t^{'} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}\left(\mathcal{E}_s - \mathcal{E}_s^{'}\right) + \frac{kT}{q}\ln\left(\frac{1 - e^{-\frac{q\mathcal{E}_s}{kT}t_{si}}}{1 - e^{-\frac{q\mathcal{E}_s^{'}}{kT}t_{si}}}\right) \tag{4.39}$$

where $\varepsilon_s^{'}$ is the new built-in field after changing t_{ox} to $t_{ox} + \delta t_{ox}$.

$$\mathcal{E}_s^{'} = \frac{\Delta\phi_2 - \Delta\phi_1}{t_{si} + 2\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left(t_{ox} + \delta t_{ox}\right)} \tag{4.40}$$

The positive value of $\Delta V_t^{'}$ means the threshold voltage increases by changing t_{ox} to $t_{ox} + \delta t_{ox}$. To eliminate this additional threshold voltage variation, the final shift of the gate work function is given by $\Delta V_t - \Delta V_t^{'}$. In other words, to generate the drain current with quantum correction, one needs to increase the two gate work functions by $\Delta V_t - \Delta V_t^{'}$ and to change t_{ox} to $t_{ox} + \delta t_{ox}$. Figure 4.19 shows the $I_{ds} - V_{ds}$ characteristics produced by this method.

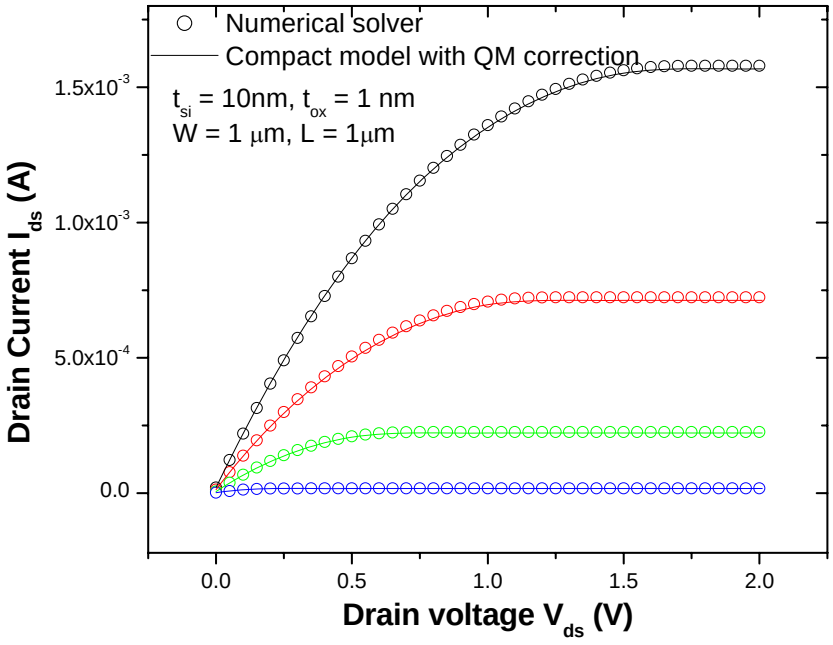


Figure 4.19 I_{ds}-V_{ds} curves obtained from the analytical compact model (line) compared with those obtained from the Poisson-Schrodinger solver (symbol) for an asymmetric DG MOSFET with n^+/p^+ poly gates at two different gate voltages.

Chapter 5

Compact Modeling of QM Effects In Short Channel DG MOSFETs

In previous chapters, quantum effects are investigated and implemented in the analytical long channel core model for DG MOSFETs. In a short channel DG MOSFET, variation of the electric field in the channel direction becomes comparable to the corresponding variation in the vertical direction due to the strong source and drain field penetration. Consequently, the Gradual-Channel approximation is no longer valid and solving 1-D Poisson's equation in the vertical direction is not sufficient to give us comprehensive understanding of the device characteristics. Further insight into the electric performance of a short channel DG MOSFET can be gained by examining the two-dimensional Poisson's equation.

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial x^2} = -\frac{\rho}{\varepsilon_{si}} \tag{5.1}$$

where the electrostatic potential $\psi(x,y)$ is defined as the intrinsic potential at a point (x,y) with respect to the Fermi potential of the n^+ source (at the conduction band edge), and ρ is the total charge density including. Figure 5.1 shows the schematic diagram of a double-gate MOSFET. The x-axis is along the vertical direction and the y-axis is along the horizontal direction with the origin at point O.

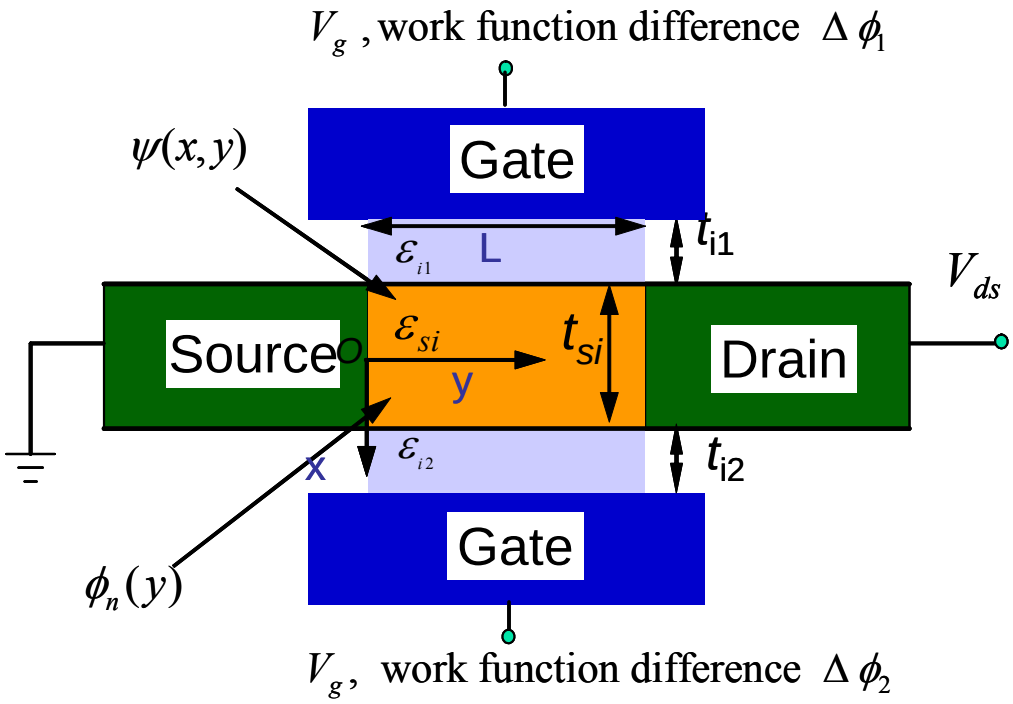


Figure 5.1 Schematic diagram of a double-gate MOFET.

5.1 2-D Analytical Solution Of Poisson's Equation In Subthreshold Region

For short channel devices, the primary concerns are the threshold voltage roll-off and the subthreshold slope, both in the subthreshold region where the mobile charges are negligible. The depletion charges are also negligible since we focus on the undoped (or lightly doped) DG MOSFETs. Consequently, the 2-D Poisson's equation in both the insulator regions and silicon regions becomes

$$\frac{\partial}{\partial x}\left(\varepsilon(x)\frac{\partial\psi}{\partial x}\right)+\frac{\partial}{\partial y}\left(\varepsilon(x)\frac{\partial\psi}{\partial y}\right)=0 \tag{5.2}$$

where $\varepsilon(x)$ is a step function due to different materials

$$\varepsilon(x)=\begin{cases}\varepsilon_{ox} & -t_{ox}-t_{si}/2\le x<-t_{si}/2\\ \varepsilon_{si} & -t_{si}/2\le x<t_{si}/2\\ \varepsilon_{ox} & t_{si}/2\le x<t_{si}/2+t_{ox}\end{cases} \tag{5.3}$$

If we assume the source and drain junctions are abrupt, the boundary conditions are:

Top gate: $\psi(-t_{si}/2-t_{ox},y)=V_{g1}-\Delta\phi_1 \qquad 0<y<L$ (5.4)

Bottom gate: $\psi(t_{si}/2+t_{ox},y)=V_{g2}-\Delta\phi_2 \qquad 0<y<L$ (5.5)

Source: $\psi(x,0)=E_g/2q \qquad -t_{si}/2<x<t_{si}/2$ (5.6)

Drain: $\psi(x,L)=V_{ds}+E_g/2q \qquad -t_{si}/2<x<t_{si}/2$ (5.7)

A full analytical potential solution can be obtained after solving the Poisson's equation in the 2-D boundary value problem [52].

$$\psi(x,y)=\frac{\Delta\Phi_1-\Delta\Phi_2}{t_{si}+2\varepsilon_{si}t_{ox}/\varepsilon_{ox}}x+V_g-\frac{\Delta\Phi_1+\Delta\Phi_2}{2} +\frac{b_1\sinh[\pi(L-y)/\lambda_1]+c_1\sinh(\pi y/\lambda_1)}{\sinh(\pi L/\lambda_1)}\cos(\pi x/\lambda_1) \tag{5.8}$$

where the coefficients b_1 and c_1 are

$$b_1=\frac{2\lambda_1^{\,2}\tan(\pi t_{ox}/\lambda_1)\sin(\pi t_{si}/2\lambda_1)}{\pi^2 t_{ox}\left[\frac{t_{si}}{2}+\frac{\sin(\pi t_{si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)}t_{ox}\right]}\left[\frac{E_g}{2q}-V_{g1}+\frac{\Delta\phi_1+\Delta\phi_2}{2}\right]$$

$$c_1=\frac{2\lambda_1^{\,2}\tan(\pi t_{ox}/\lambda_1)\sin(\pi t_{si}/2\lambda_1)}{\pi^2 t_{ox}\left[\frac{t_{si}}{2}+\frac{\sin(\pi t_{si}/\lambda_1)}{\sin(2\pi t_{ox}/\lambda_1)}t_{ox}\right]}\left[\frac{E_g}{2q}+V_{ds}-V_{g1}+\frac{\Delta\phi_1+\Delta\phi_2}{2}\right] \tag{5.9}$$

And the scale length λ_1 is the largest eigen value of the following equation.

$$\varepsilon_{si}\tan(\pi t_i/\lambda_n)=\varepsilon_{ox}\tan(n\pi/2-\pi t_{si}/2\lambda_n)$$

The V_{ds} dependence in c_1 is responsible for DIBL and the V_g dependence in b_1 and c_1 subthreshold slope degradation.

Constant electrostatic potential contours calculated from the analytical solution for symmetric DG MOSFETs are compared with 2-D ISE simulation results in Figure 5.2. The agreement is quite good (with relative error less than 2%). It is clear that the maximum potential along x=0 has a minimum in the y direction. The minimum is located approximately midway between the source and the drain. Potential variation in the x direction is much less than that in the y direction.

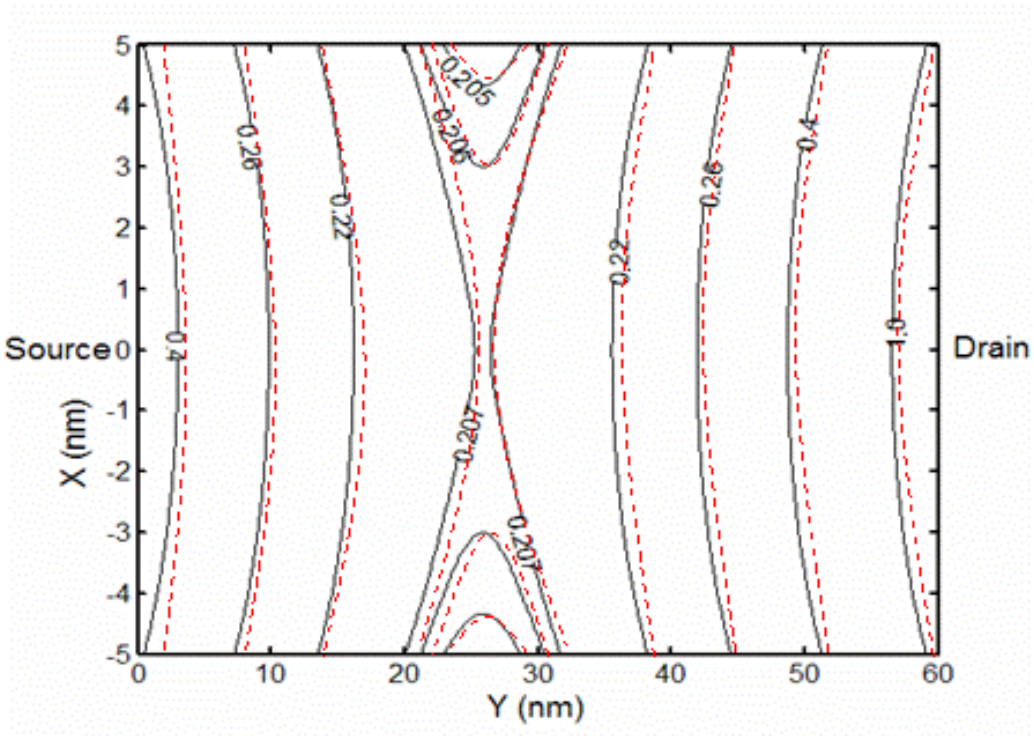


Figure 5.2 Constant electrostatic potential contours based on the analytical solution (solid curves) for symmetric DG MOSFETs, compared with 2-D simulation results (dashed curves). Here, $V_{g1}=V_{g2}=V_g$=0.2V, V_{ds}=1V, L=60nm, t_{si}=10nm, and t_i=1.5nm.

5.2 Classical And Quantum Subthrshold Current

5.2.1 Classical Subthreshold Current

Knowing the potential solution, we can proceed to derive the subthreshold current. Note that the electron quasi-Fermi potential V is essentially constant in the x-direction, which means that the MOSFET current density J flows predominantly in the y-direction (from source to drain). The current density (both drift and diffusion) can then be written as

$$J = -q\mu n(x,y)\frac{dV(y)}{dy} \tag{5.11}$$

Integrating in x- and z-directions and one has

$$I_{ds}(y) = -\mu W Q_i(y)\frac{dV(y)}{dy} \tag{5.12}$$

where $Q_i(y)$ is the inversion charge per gate area

$$Q_i(y) = q\int_{-t_{si}/2}^{t_{si}/2} n(x,y)dx = q\int_{-t_{si}/2}^{t_{si}/2} n_i e^{q[\psi(x,y)-V(y)]/kT}dx \tag{5.13}$$

Based on the current continuity, integration of (5.12) with respect to y from *0* to *L* yields

$$I_{ds} = \frac{\mu W\int_0^{V_{ds}} e^{-qV(y)/kT}dV(y)}{\int_0^L \frac{dy}{q\int_{-t_{si}/2}^{t_{si}/2} n_i e^{q\psi(x,y)/kT}dx}} = \frac{\mu WkT\left[1-\exp(-qV_{ds}/kT)\right]}{\int_0^L \frac{dy}{\int_{-t_{si}/2}^{t_{si}/2} n_i e^{q\psi(x,y)/kT}dx}} \tag{5.14}$$

The classical subthreshold current can only be obtained through numerical calculation due to the double integral in (5.14).

5.2.2 Quantum Subthreshold Current From The Solver

Due to the very low low mobile carrier density in the subthreshold region, it is a reasonable approximation that the charge will not affect the potential profile, which means that one can decouple the Poisson's and Schrodinger equations. Therefore, we can incorporate the analytical potential solution into the Schrodinger equation directly to obtain the wave function and hence, the quantum electrostatic carrier profile instead of solving Poisson and Schrodinger equation self-consistently.

$$-\frac{\hbar^2}{2m^*}\frac{d^2\varphi(x)}{dx^2}+[-q\psi(x,y)]\varphi(x)=E\varphi(x) \tag{5.15}$$

$$Q_i^{qm}=\frac{4\pi qkT}{h^2}\sum_i g_i m_i^* \sum_j \ln[1+e^{\left(-E_{ij}-qV(y)\right)/kT}] \tag{5.16}$$

Based on current continuity, an iterative procedure (shown in Figure 5.3) is then employed to find the drain current level. At a given gate and drain bias, we first solve the Schrodinger equation at the first slice (source) and then calculate the inversion charge sheet density through (5.16) with zero quasi-Fermi level. The current continuity condition (5.12) then, yields the quasi-Fermi level at the next slice through an initial guess of the current I_{guess} as follows:

$$V_2=V_1+\frac{1}{\mu W}\frac{1}{Q_{i1}}I_{guess}\Delta y \tag{5.17}$$

where Δy is thickness of the uniform slice, Q_{i1} is the inversion charge sheet density in the first slice, V_1 and V_2 is the quasi-Fermi level in the first and second slice respectively.

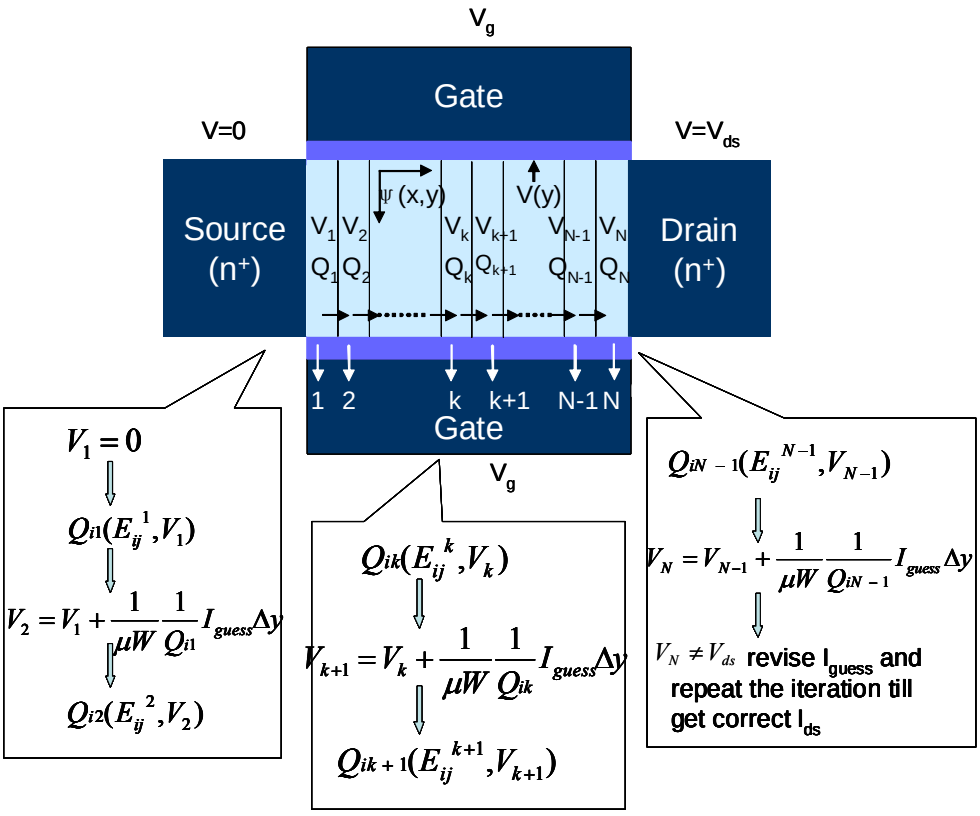


Figure 5.3 Schematic diagram of the procedure to obtain the subthrshold current for short channel DG MOSFETs.

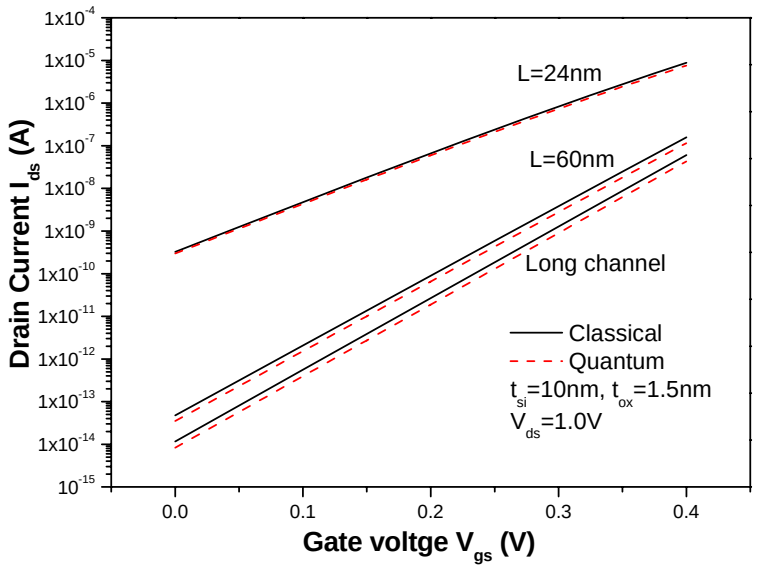
With a known quasi-Fermi level, solving Schrodinger equation yields the inversion charge sheet density through (5.16) in the second slice. The same procedure is repeated till the quasi-Fermi level at the last slice (drain) is obtained.

$$V_N = V_{N-1} + \frac{1}{\mu W}\frac{1}{Q_{iN-1}} I_{guess}\Delta y \qquad (5.18)$$

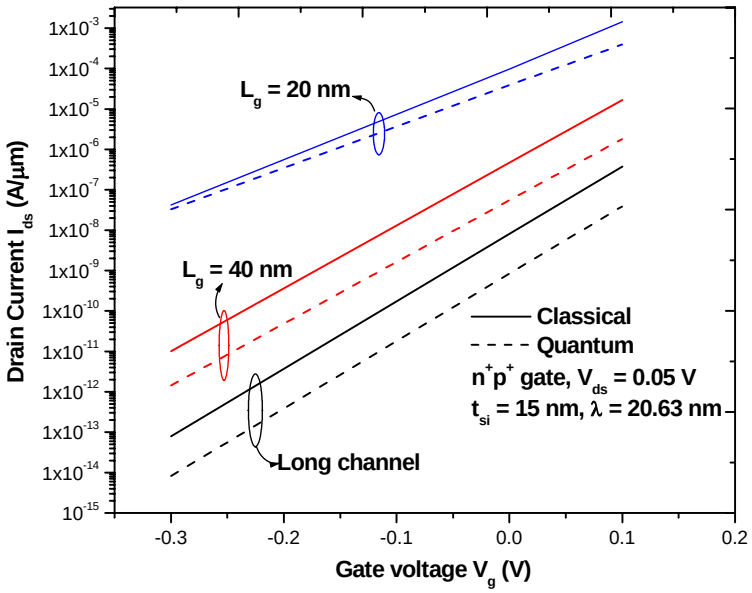
where $Q_{i\mathrm{N\text{-}1}}$ and $V_{\mathrm{N\text{-}1}}$ is the inversion charge sheet density and at the (N-1)th slice respectively and V_{N} is the quasi-Fermi level at the last slice (drain).

If the calculated quasi-Fermi level V_N at drain does not equal the drain voltage V_{ds}, the initial estimate of the current level I_{guess} is revised and the iterative calculation is repeated. This process is repeated until the correct current level is found.

Figure 5.4 compares classical and quantum subthreshold current obtained by this method for both a symmetric and an asymmetric DG MOSFET. Quantum effect is significantly stronger in asymmetric DG MOSFETs than it is in symmetric DG MOSFETs because the "built-in field" in asymmetric DG MOSFETs is much higher. However, quantum effect in a symmetric DG MOSFET becomes significant when the thickness of silicon film is very thin. It is also observed that quantum effects make the V_t roll-off worse than classical case in asymmetric DG MOSFET.



(a)



(b)

Figure 5.4 Classical (solid line) and quantum (dash line) subthreshold Ids-Vg characteristics obtained from the iteration procedure for a symmetric (a) and an asymmetric (b) DG MOSFET with different channel length.

5.2.3 Quantum Subthreshold Current – Perturbation Approach

In section 5.2.2, to calculate the quantum subthreshold current, one needs to obtain the eigen energy levels by solving the Schrodinger equation numerically from the solver, calculating the charge sheet density and finally running the iteration procedure. It requires plenty of numerical computation and hence, is not convenient for the compact modeling. The problem is much simplified if we can calculate the eigen energy levels analytically or approximately. Note that due to volume inversion, in the subthreshold region of a long channel symmetric DG MOSFET, the quantum potential well acts like an infinite square well whose eigen energy and eigen wave function are well known. Approximate expression of energy levels can then be achieved by treating the short channel term in the 2-D potential solution (last term in (5.8)) as a perturbation. The zero order wave functions of an infinite square well from $-t_{si}/2$ to $t_{si}/2$ are

$$\varphi_j^0(x) = \begin{cases} \sqrt{\dfrac{2}{t_{si}}}\cos\left(\dfrac{j\pi x}{t_{si}}\right) & j = 1,3,5,... \\ \sqrt{\dfrac{2}{t_{si}}}\sin\left(\dfrac{j\pi x}{t_{si}}\right) & j = 2,4,6,... \end{cases} \tag{5.19}$$

with the eigen energy levels:

$$E_j^0 = \frac{j^2\hbar^2\pi^2}{2m^* t_{si}^2} \tag{5.20}$$

The first order energy perturbation term for the odd states is the following based on the non-degenerate perturbation theory.

$$
\begin{aligned}
E^{1}_{j=1,3,5,\ldots} &= A\int_{-t_{si}/2}^{t_{si}/2}\cos^2\left(\frac{j\pi x}{t_{si}}\right)\cos\left(\frac{\pi x}{\lambda_1}\right)dx \\
&= A\left[\frac{\sin\left(\frac{2j\pi}{t_{si}}-\frac{\pi}{\lambda_1}\right)x}{4\left(\frac{2j\pi}{t_{si}}-\frac{\pi}{\lambda_1}\right)}+\frac{\sin\left(\frac{\pi}{\lambda_1}\right)x}{2\frac{\pi}{\lambda_1}}+\frac{\sin\left(\frac{2j\pi}{t_{si}}+\frac{\pi}{\lambda_1}\right)x}{4\left(\frac{2j\pi}{t_{si}}+\frac{\pi}{\lambda_1}\right)}\right]\Bigg|_{-t_{si}/2}^{t_{si}/2} \\
&= A*B_j*\sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)
\end{aligned}
\tag{5.21}
$$

where the coefficient A and B are

$$
A=-\frac{2q}{t_{si}}\frac{b_1\sinh\left(\frac{\pi(L-y)}{\lambda_1}\right)+c_1\sinh\left(\frac{\pi y}{\lambda_1}\right)}{\sinh\left(\frac{\pi L}{\lambda_1}\right)} \tag{5.22}
$$

$$
B_j=\frac{1}{4\left(\frac{2j\pi}{t_{si}}-\frac{\pi}{\lambda_1}\right)}+\frac{1}{2\frac{\pi}{\lambda_1}}-\frac{1}{4\left(\frac{2j\pi}{t_{si}}+\frac{\pi}{\lambda_1}\right)} \tag{5.23}
$$

Similarly, one can calculate the even states.

$$
\begin{aligned}
E^{1}_{j=2,4,6,\ldots} &= A\int_{-t_{si}/2}^{t_{si}/2}\sin^2\left(\frac{j\pi x}{t_{si}}\right)\cos\left(\frac{\pi x}{\lambda_1}\right) \\
&= A\left[\frac{\sin\left(\frac{2j\pi}{t_{si}}-\frac{\pi}{\lambda_1}\right)x}{4\left(\frac{2j\pi}{t_{si}}-\frac{\pi}{\lambda_1}\right)}+\frac{\sin\left(\frac{\pi}{\lambda_1}\right)x}{2\frac{\pi}{\lambda_1}}+\frac{\sin\left(\frac{2j\pi}{t_{si}}+\frac{\pi}{\lambda_1}\right)x}{4\left(\frac{2j\pi}{t_{si}}+\frac{\pi}{\lambda_1}\right)}\right]\Bigg|_{-t_{si}/2}^{t_{si}/2} \\
&= A*B_j*\sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)
\end{aligned}
\tag{5.24}
$$

For the purpose of compact modeling, it is sufficient to consider the first order perturbation term only since the second order perturbation term is much smaller than the first order. From the above calculation, the eigen energy levels for a short channel symmetric DG MOSFET are:

$$E_j = \frac{j^2\hbar^2\pi^2}{2m^* t_{si}^2} + A^* B_j^* \sin\left(\frac{\pi t_{si}}{2\lambda_1}\right) \tag{5.25}$$

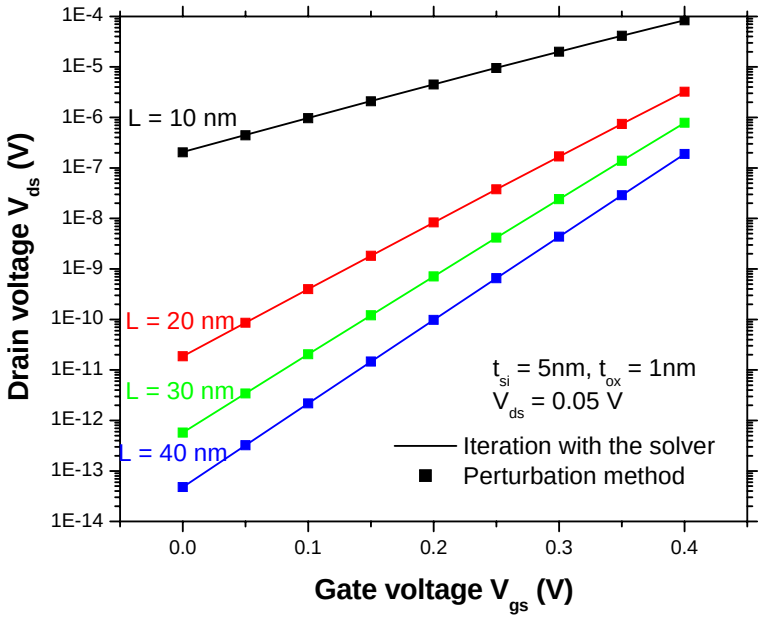
With the eigen energy levels, one can easily calculate the charge sheet density along the channel using (5.16).

$$\begin{aligned} Q_i^{QM} &= \frac{qkT}{\pi\hbar^2}\sum_i g_i m_i^* \sum_j \ln\left[1+e^{\left(q(V_g-\Delta\phi)-\frac{E_g}{2}-E_j(y)-qV(y)\right)\Big/kT}\right] \\ &= \frac{qkT}{\pi\hbar^2}\sum_i g_i m_i^* \sum_j e^{\left(q(V_g-\Delta\phi)-\frac{E_g}{2}-E_j(y)-qV(y)\right)\Big/kT} \\ &= \frac{qkT}{\pi\hbar^2} e^{\left(q(V_g-\Delta\phi)-\frac{E_g}{2}\right)\Big/kT} \sum_i g_i m_i^* \sum_j e^{\left(-E_j(y)-qV(y)\right)\Big/kT} \end{aligned} \tag{5.26}$$

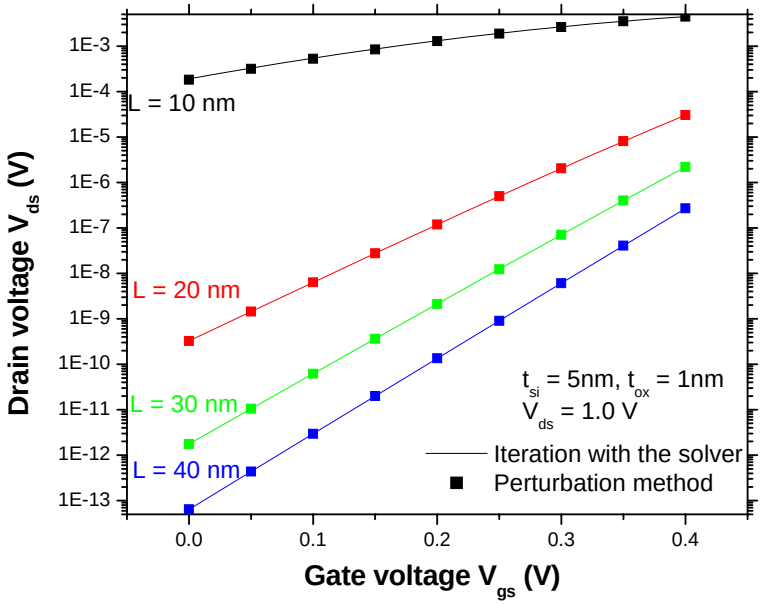
The above equation assumes that the quasi-Fermi level is at least several *kT* below the lowest energy level. Substituting the charge sheet density into the current continuity equation yields the subthreshold current.

$$I_{ds}^{QM} = \frac{\mu W \frac{kT}{q}\left(e^{qV_{ds}/kT}-1\right)}{\int_0^L \frac{1}{\frac{qkT}{\pi\hbar^2} e^{\left(q(V_g-\Delta\phi)-\frac{E_g}{2}\right)\Big/kT} \sum_i g_i m_i^* \sum_j e^{-E_j(y)/kT}} dy} \tag{5.27}$$

Although the integral in the denominator still needs to be calculated numerically, the problem is simplified by avoiding solving the Schrodinger equation and iterating with the continuity equation. Figure 5.5 compares the subthreshold current at low (a) and high (b) drain bias of a symmetric DG MOSFET with different channel length calculated from (5.27) and those from the solver with the iteration procedure. The agreement is good for a wide range of channel length. However, the deviation becomes large when the channel length is comparable to the scale length in the case of thick silicon film. The reason is that the first order energy perturbation due to the short channel term in the potential expression (5.8) is comparable to the zero order energy and hence can not be treated as a perturbation. However, these channel lengths are not practical due to the severe short channel effects.



(a)



(b)

Figure 5.5 Quantum subthreshold Ids-Vg characteristics obtained from the iteration procedure (line) and perturbation method (symbol) of a DG MOSFET with different channel length at low (a) and high (b) drain bias.

5.3 Quantum Short-Channel-Effects Induced V_t Roll-Off

The threshold voltage decreases with decreasing channel length due to the source/drain influence on the channel. In the quantum case, this becomes more severe because of the quantum inversion charge distribution. Gate control over the channel is weakened with the inversion charge farther away from the gate. As shown in Figure 5.6, quantum threshold voltage drops faster with decreasing channel length than the classical case.

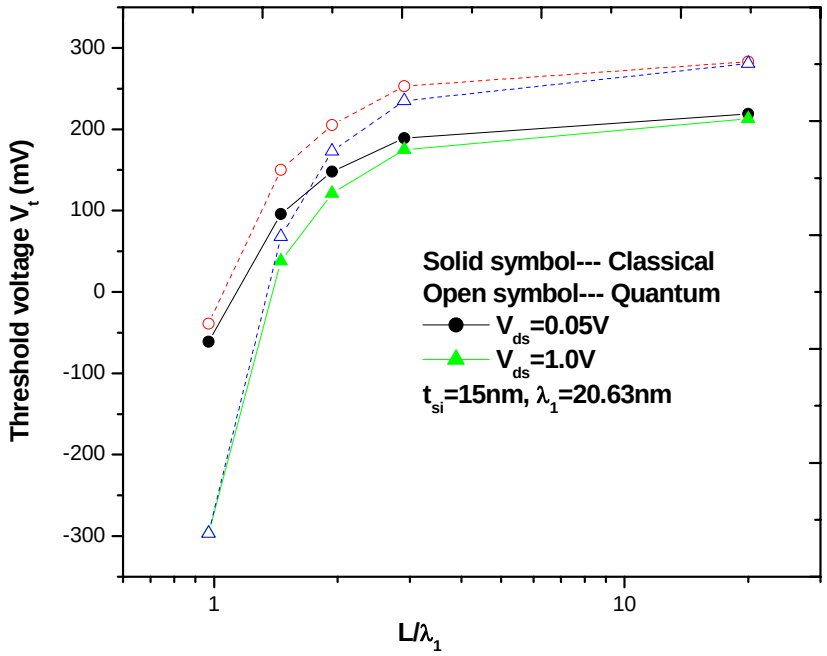


Figure 5.6 Classical (solid symbol) and quantum (open symbol) threshold voltage V_t for an asymmetric (n^+p^+) DG MOSFET with different channel length (normalize to λ_1). at low (circle) and high (triangular) drain

From the compact modeling point of view, we can assume a known classical V_t roll-off due to SCE in the classical model and focus on the V_t shift due to quantum effects of the short channel DG MOSFETs.. The definition of V_t shift for the short channel devices due to quantum effects is

$$I_{ds}^{CL}(V_g, V_{ds}) = I_{ds}^{QM}(V_g + \frac{S}{(kT/q)\ln 10}\Delta V_t, V_{ds}) \tag{5.28}$$

In (5.28), we assume the classical and quantum subthreshold slope S are the same. The exponential term of V_g in (5.27) is independent of y and can be taken out of the integral. Therefore we have

$$I_{ds}^{QM}(V_g + \frac{S}{(kT/q)\ln 10}\Delta V_t, V_{ds}) = e^{\frac{S}{\ln 10}\Delta V_t\left(\frac{q}{kT}\right)^2} I_{ds}^{QM}(V_g, V_{ds}). \tag{5.29}$$

Combining (5.28) and (5.29) yields an expression of the V_t shift.

$$e^{\frac{S}{\ln 10}\Delta V_t\left(\frac{q}{kT}\right)^2} = I_{ds}^{CL}(V_g, V_{ds}) \Big/ I_{ds}^{QM}(V_g, V_{ds}) \tag{5.30}$$

The 2-D potential distribution has a minimum y_c (maximum barrier) in the y direction, which can be obtained through $\partial\psi(x,y)/\partial y\big|_{y=y_c} = 0$. From the denominators of (5.14) and (5.27), it is obvious that this minimum dominates the drain current level. If we neglect the errors caused by the spatial variation of the electrostatic potential in the y direction, one has

$$Q_i^{CL}(y_c) = e^{\frac{S}{\ln 10}\Delta V_t\left(\frac{q}{kT}\right)^2} Q_i^{QM}(y_c) \tag{5.31}$$

where

$$y_c = \frac{L}{2} - \frac{\lambda_1}{2\pi}\ln(\frac{c_1}{b_1}) \tag{5.32}$$

Substituting the classical and quantum inversion charge density expression into (5.31) yields:

$$q\int_{-t_{si}/2}^{t_{si}/2} n_i e^{q\psi(x,y_c)/kT}\,dx = e^{\frac{S}{\ln 10}\Delta V_t\left(\frac{q}{kT}\right)^2}\,\frac{qkT}{\pi h^2}e^{\left(q(V_g-\Delta\phi)-\frac{E_g}{2}\right)\Big/kT}\sum_i g_i m_i^*\sum_j e^{-E_j(y_c)/kT} \tag{5.33}$$

Substituting the analytical potential expression (5.8) and using (5.22) and (5.25), one obtains

$$e^{\frac{S}{\ln 10}\Delta V_t\left(\frac{q}{kT}\right)^2} = \frac{n_i\pi\hbar^2}{kT}e^{-E_g/2kT}\,\frac{\int_{-t_{si}/2}^{t_{si}/2} e^{\frac{t_{si}}{2}A(y_c)\cos\left(\frac{\pi x}{\lambda_1}\right)/kT}\,dx}{\sum_i g_i m_i^*\sum_j e^{\left[-E_j^0-A(y_c)B_j\sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)\right]\Big/kT}} \tag{5.34}$$

The V_t shift depends on both V_g and V_{ds} through the parameters b_1 and c_1 in $A(y_c)$, which implies that quantum subthreshold slope differs from the classical one. The subthreshold slope will be discussed in detail in the next section. Note that the potential also has a maximum at x_c ($x_c = 0$ for symmetric case) in the x direction and the coefficients B_j of the energy perturbation term follow a descending order of $B_1>B_2>B_3>\ldots$ Since the error caused by substituting x with x_c in the numerator mostly cancels with the error caused by substituting all B_j with B_1, one obtains a simple equation for the V_t shift.

$$e^{\frac{S}{\ln 10}\Delta V_t\left(\frac{q}{kT}\right)^2} = \frac{n_i \pi \hbar^2}{kT} e^{-E_g/2kT} \frac{t_{si} e^{\frac{t_{si}}{2}A(y_c)\cos\left(\frac{\pi x_c}{\lambda_1}\right)/kT}}{e^{-A(y_c)B_1 \sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)/kT} \sum_i g_i m_i^* \sum_j e^{-E_j^0/kT}} \tag{5.35}$$

$$= e^{q\Delta V_t^{LONG}/kT} e^{\frac{t_{si}}{2}\frac{A(y_c)}{kT}\left[1+\frac{2B_1}{t_{si}}\sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)\right]}$$

where ΔV_t^{LONG} is the V_t shift of long channel DG MOSFETs based on the definition in chapter 3.

$$e^{q\Delta V_t^{LONG}/kT} = \frac{t_{si} n_i \pi \hbar^2}{kT} e^{-E_g/2kT} \frac{1}{\sum_i g_i m_i^* \sum_j e^{-E_j^0/kT}} \tag{5.36}$$

From the above derivation, we finally obtain the V_t shift of a short channel DG MOSFET as a closed form function of the device parameters and the terminal biases.

$$\Delta V_t = \frac{\ln 10}{S}\frac{kT}{q}\left[\Delta V_t^{LONG} + \frac{t_{si}}{2}\frac{A(y_c)}{q}\left[1+\frac{2B_1}{t_{si}}\sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)\right]\right] \tag{5.37}$$

Figure 5.7 shows the V_t shift calculated from (5.37) and that obtained from the solver. The subthreshold slope used in the calculation is the classical slope obtained from the simulation data from the solver. The agreement is good for the entire range of the channel lengths shown.

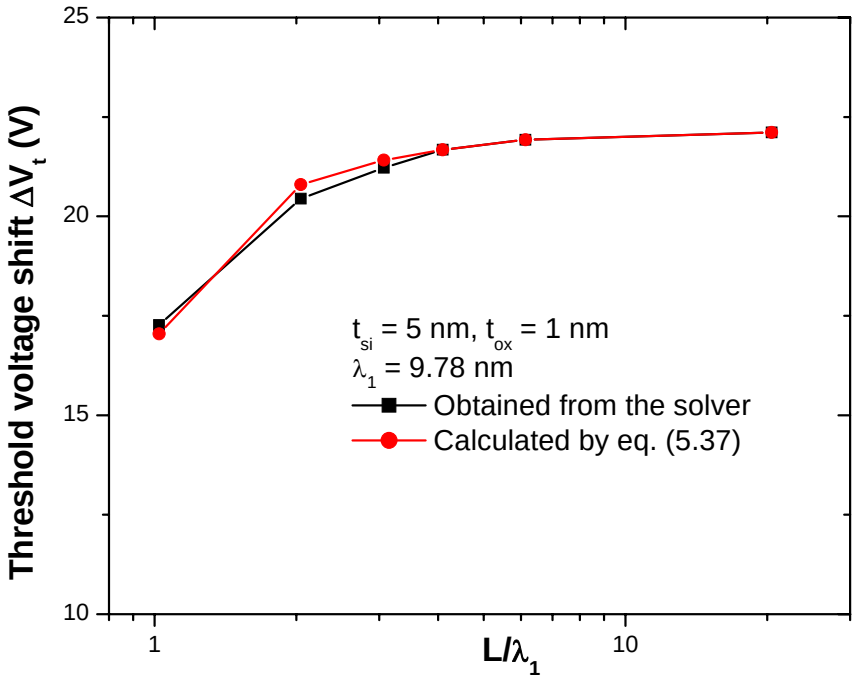


Figure 5.7 Threshold voltage shift due to quantum effects calculated by (5.37) (circle) and obtained from the solver (square) versus the channel length (normalize to λ_1).

5.4 Quantum Subthreshold Slope

The fact that the inversion charges are farther away from the surface due to quantum effects not only worsens the short channel V_t roll-off, but also degrades the subthreshold slope as illustrated in Figure 5.8. For same channel length, the effective oxide thickness as well as the scale length increases due to the finite quantum inversion layer thickness.

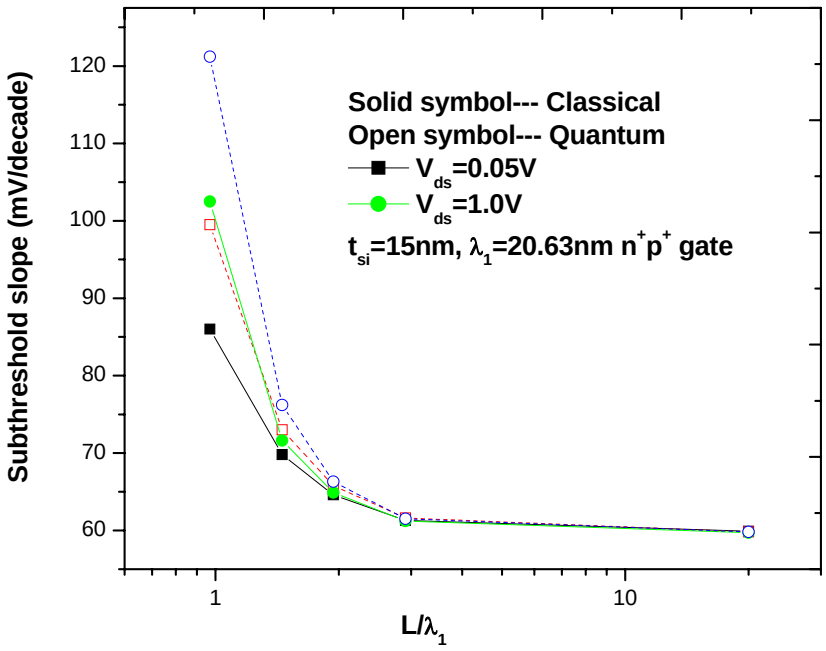


Figure 5.8 Classical (solid symbol) and quantum (open symbol) subthreshold slope for an asymmetric DG MOSFET with different normalized channel length at low (square) and high drain (circle) voltage.

For symmetric DG MOSFETs, we can also obtain an approximate expression for the quantum subthreshold slope based on the classical one, which is straight forward for compact modeling. Take the logarithm and then the derivative of (5.30) and one has

$$\frac{d\log_{10}\left(I_{ds}^{CL}\right)}{dV_g}=\frac{de^{\frac{S}{\ln 10}\Delta V_t\left(\frac{q}{kT}\right)^2}}{dV_g}+\frac{d\log_{10}\left(I_{ds}^{QM}\right)}{dV_g} \tag{5.38}$$

It can be rewritten using the definition of the subthreshold slope.

$$\frac{1}{S^{CL}}=\frac{S}{\ln 10}\left(\frac{q}{kT}\right)^2\frac{d\Delta V_t}{dV_g}+\frac{1}{S^{QM}} \tag{5.39}$$

Take the derivative of (5.37) and substitute it into (5.39).

$$\frac{1}{S^{CL}} = \ln 10 \frac{t_{si}}{2kT}\left[1 - \frac{2B_1}{t_{si}}\sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)\right]\frac{dA(y_c)}{dV_g} + \frac{1}{S^{QM}} \tag{5.40}$$

From (5.22) and (5.32), we obtain

$$\begin{aligned}\frac{dA(y_c)}{dV_g} &= -\frac{2q}{t_{si}}\sinh\left(\frac{\pi L}{\lambda_1}\right)^{-1} d\left(b_1\sinh\left(\frac{\pi(L-y_c)}{\lambda_1}\right) + c_1\sinh\left(\frac{\pi y_c}{\lambda_1}\right)\right)\Big/ dV_g \\ &= \frac{(b_1 - c_1)D}{2}\left(\frac{\cosh\left(\pi y_c \big/ \lambda_1\right)}{b_1} - \frac{\cosh\left(\pi(L-y_c)\big/\lambda_1\right)}{c_1}\right) \\ &\quad - D\left(\sinh\left(\frac{\pi y_c}{\lambda_1}\right) + \sinh\left(\frac{\pi(L-y_c)}{\lambda_1}\right)\right),\end{aligned} \tag{5.41}$$

where the consant D is

$$D = -\frac{2q}{t_{si}}\frac{2\lambda_1^{\,2}\tan(\frac{\pi t_{ox}}{\lambda_1})\sin(\frac{\pi t_{si}}{2\lambda})}{\pi^2 t_{ox}\left[\frac{t_{si}}{2} + \frac{\sin(\pi t_{si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)}t_{ox}\right]\sinh\left(\frac{\pi L}{\lambda_1}\right)}\ . \tag{5.42}$$

Using (5.40), (5.41) and (5.42), we can easily calculate the quantum subthreshold slope from the classical one. Figure 5.9 compares the quantum subthreshold slope from the approximate calculation and that obtained from the solver directly. The classical slope used in the calculation is also obtained from the solver.

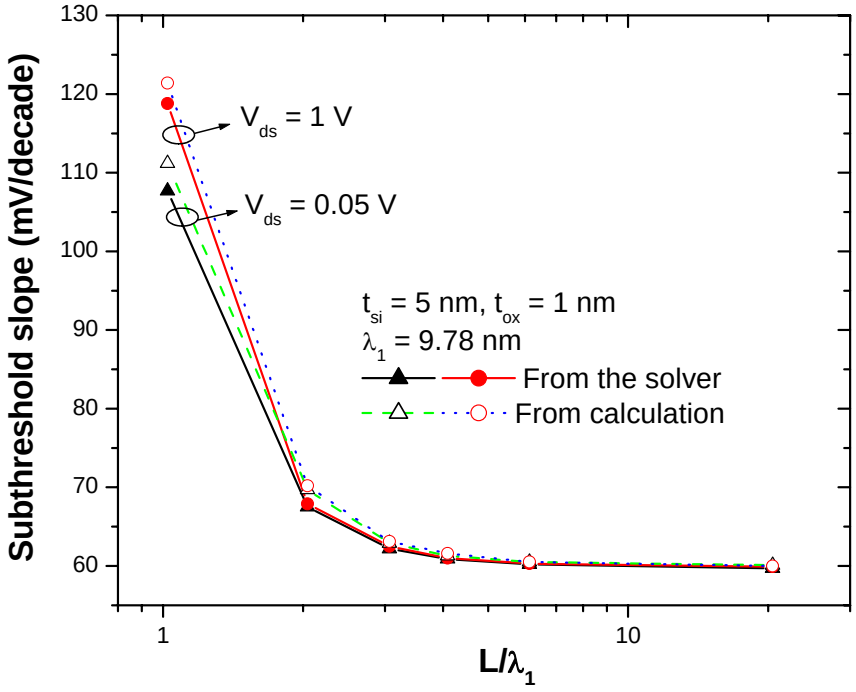


Figure 5.9 Quantum subthreshold slope from the solver (solid symbol) and from the calculation (open symbol) versus the normalized channel length at different drain voltage $V_{ds} = 0.05\ V$ (triangle) and $V_{ds} = 1\ V$ (circle).

Chapter 6

Summary

Starting with a review of CMOS scaling and modeling of quantum effects in bulk MOSFETs, this dissertation focuses on the compact modeling of quantum effects in DG MOSFETs. The threshold voltage shift and gate capacitance degradation due to quantum effects are extracted from a numerical solver and implemented in an analytical compact model for DG MOSFETs.

The numerical methods of solving Poisson's and Schrodinger equations, including the iterative procedure in obtaining self-consistent solutions of the two coupled equations, are described in Chapter 2. The 1-D numerical solver developed for DG MOS capacitors is extended for calculating the current-voltage characteristics of DG MOSFETs based on the fact that in Pao-Sah's integral, the integration of inversion charge density over the quasi-Fermi potential is equivalent to that over an "effective" gate voltage.

An analytic compact model with quantum corrections is developed for symmetric double-gate MOSFETs in Chapter 3. Two distinctive quantum effects are extracted from extensive numerical solutions using the 1-D Poisson-Schrodinger solver. First, the threshold voltage shift as a function of the silicon film thickness is implemented as an effective change in the silicon film thickness that produces the same shift in subthreshold. Second, quantum degradation of inversion layer capacitance is expressed as a closed-form function of the inversion charge sheet density and implemented as an effective

increase of the gate oxide thickness. After incorporating these effects in an analytic potential model for DG MOSFETs, the *I-V* curves generated by the compact model are in good agreement with those obtained directly from the Poisson-Schrodinger solver. Transient simulation of CMOS circuits shows that quantum effects have significant impact on the delay of DG MOSFETs.

Chapter 4 focuses on the complex quantum mechanical effects on the charge and potential in an asymmetric DG MOSFET. The built-in field in the subthreshold region due to the asymmetric gate work functions causes the threshold voltage shift to depend on the silicon thickness as well as the built-in field. With the electron ground state energy calculated by an analytical approximation, the threshold voltage shift is expressed as an explicit function of the device parameters. To account for the charge coupling between the two gates and the inversion channels, an equivalent small-signal capacitance circuit is developed which can be used to extract the equivalent inversion layer thickness. The threshold voltage shift is implemented in the classical analytical potential model as an effective change of the gate work functions. A constant increase in the effective oxide thickness representing gate capacitance degradation to the first order approximation is implemented in the classical model.

A 2-D analytical solution to Poisson's equation for a DG MOSFET in the subthreshold region is incorporated into the Schrodinger equation to obtain the quantum solutions. With the electron eigen-energy levels calculated by a perturbation approach, the quantum subthreshold current is calculated accordingly. The short channel threshold voltage roll-off is more than the classical case because the quantum inversion charge is further away from the silicon surface. For the same reason, the quantum subthreshold

slope also worsens. Using an analytical approximation, the quantum threshold shift and subthreshold slope in short channel DG MOSFETs are expressed as closed-form functions of the device parameters and the terminal bias voltages.

The developed quantum compact model for DG MOSFETs has been implemented in a SPICE environment and released to the design community for circuit simulations.

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