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A Low-Noise CMOS Pixel Direct Charge Sensor, *Topmetal-II⁻*

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Abstract

We report the design and characterization of a CMOS pixel direct charge sensor, *Topmetal-II⁻*, fabricated in a standard 0.35 µm CMOS Integrated Circuit process. The sensor utilizes exposed metal patches on top of each pixel to directly collect charge. Each pixel contains a low-noise charge-sensitive preamplifier to establish the analog signal and a discriminator with tunable threshold to generate hits. The analog signal from each pixel is accessible through time-shared multiplexing over the entire array. Hits are read out digitally through a column-based priority logic structure. Tests show that the sensor achieved a $< 15\,e^-$ analog noise and a $200\,e^-$ minimum threshold for digital readout per pixel. The sensor is capable of detecting both electrons and ions drifting in gas. These characteristics enable its use as the charge readout device in future Time Projection Chambers without gaseous gain mechanism, which has unique advantages in low background and low rate-density experiments.

Keywords: Topmetal, Pixel, Charge sensor, Ion readout

1. Introduction

Over the years a number of highly pixelated CMOS sensors and readout Integrated Circuit (IC) chips have been developed and deployed successfully in nuclear and particle physics experiments. Notable examples are CMOS readout pixel ICs such as Medipix/Timepix[1, 2] and FE-I3/FE-I4 [3], and Monolithic Active Pixel Sensors (MAPS) such as the one described in [4]. Readout pixel ICs are designed mainly to be coupled to external solid state detectors through processes such as flip-chip bump bonding. Charges are generated in the external detector due to the passing of ionizing particles, then collected and measured by the readout IC. MAPS ICs allow charges to be generated inside of the silicon IC (pixel) itself and integrate the readout circuitry in the same chip.

The high pixel density and high integration of circuitry nature of pixel ICs made them appealing to be the charge readout device of choice in Micro-Pattern Gaseous Detectors (MPGDs)[5], replacing conventional wire readout schemes[6] and patterned Printed Circuit Board (PCB) readout schemes[7]. These MPGDs are usually used for charge and timing measurements in Time Projection Chambers (TPCs)[8] achieving improved spatial resolution and noise performance. For instance, the D^3 experiment [9] uses FE-I3/FE-I4 sensors developed for the ATLAS [10] experiment, behind a Gaseous Electron Multiplication (GEM) stage, to detect charge tracks resulting from potential dark matter interactions. Some similar efforts using the Timepix sensor behind GEMs were presented in [11, 12]. A more integrated approach, fabricating a micro-pattern gaseous gain structure directly on top of a Medipix/Timepix chip by means of wafer post-processing, was reported in [13] (InGrid).

In these applications of pixel ICs in gaseous detectors, ICs were usually designed for a different purpose and were later converted to perform direct charge readout resulting in characteristic mismatches between the IC performance and application requirements. Very few direct charge collection ICs were designed specifically for micro-pattern gaseous pixel detectors. A notable exception is an IC described in [14] that is dedicated to GEM readout and X-ray polarimetry applications[15].

Regardless of which IC is employed for charge readout, an electron gas-avalanche gain stage is involved in all the above mentioned pixel readout systems. These systems are generally geared towards detectors for high event rate and high electron drift speed. An electron gas-avalanche gain is necessary to amplify the number of electrons to be well above the noise of ICs. Also, a pulse shaper is normally built in-chip to increase the rate capabilities. On the other hand, there is a class of measurements that disfavor the use of gas-avalanche gain while demand similar spatial and timing resolution. They are usually low rate-density (event rate per volume) and low background experiments. Examples are alpha particle counting[16], neutrinoless double-beta decay ($0\nu\beta\beta$) searches by drift-

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ing ions in a high pressure TPC[17, 18], upgrades to ion chambers for beam measurements, and advanced electron-track gamma-ray imaging[19]. Gas-avalanche gain is disfavored due to its large gain fluctuation and sparking resulting in poor energy resolution and stability issues particularly in large-area readout systems. Also, positive ions and negative ions in high pressure gas cannot undergo gas-avalanche. High spatial resolution is required for imaging, position determination and interaction vertex identification.

We designed a CMOS IC, *Topmetal-II⁻*, that is uniquely suitable for charge measurement in a TPC without gas-avalanche gain. It is a direct charge sensor with 83 µm pitch between pixels fabricated in a standard 0.35 µm CMOS process without post-processing. A metal patch is placed on the top of each pixel (*Topmetal*) in a 72×72 pixel array for charge collection. Each pixel contains a low-noise charge-sensitive preamplifier (CSA) to establish the analog signal and a discriminator with tunable threshold to generate hits. For its intended application, event-rate density is expected to be low and charge (both free electron and ion) drifting speed is expected to be slow; therefore, we tuned the preamplifier to have long signal retention and eliminated the in-chip pulse shaper while focusing on improving the noise performance. The analog signal from each pixel is accessed through time-shared multiplexing over the entire array. Hits are read out digitally through a column-based priority logic structure.

In this paper we present the overall design and some initial test results of *Topmetal-II⁻*. The implementation of the charge collection electrode and a time-shared analog multiplexing structure have been validated in our earlier IC development *Topmetal-I* [20]. We will focus on the analog characteristics from CSA and the behavior of digital readout. Details on circuitry and specific application notes will be presented elsewhere.

2. Sensor Structure and Operation

A photograph of one wire-bonded *Topmetal-II⁻* sensor is shown in Fig. 1 (left). The sensor is implemented in a $8 \times 9\,\mathrm{mm}^2$ silicon real-estate area. A schematic view of the sensor architecture is shown in Fig. 1 (right). With ~ 83 µm pitch distance between pixels, the 72×72 square pixel array makes up a $6 \times 6\,\mathrm{mm}^2$ charge sensitive region. Readout interface logic and an analog buffer are placed adjacent to the pixel array. The sensor is powered by analog supply `AVDD` and digital supply `DVDD`, which are individually regulated at a nominal voltage of 3.3 V.

Each pixel collects charges via its own $25 \times 25\,\mu\mathrm{m}^2$ sized metal node (*Topmetal*), then converts them to both analog and digital signals (Fig. 2). Separate circuit structures read out both analog and digital signals from every pixel and send them through dedicated channels to external interfaces. The pixel structure, analog, and digital readouts are described in the following subsections.

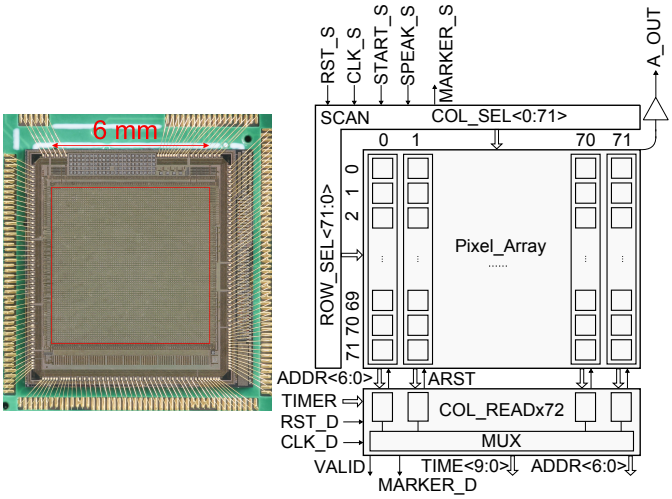

Figure 1: Photograph of a *Topmetal-II⁻* sensor (left) and a schematic view of the overall architecture (right). The sensor chip is placed on a PCB and gold wire-bonded. The 72×72 pixel array, with ~ 83 µm pitch distance between pixels, constitutes an approximately $6 \times 6\,\mathrm{mm}^2$ charge sensitive area (red box) in the center of the sensor. The analog output from each pixel is fed to a single output buffer via an array-wide row/column multiplexing circuitry. The digital output (hits) is registered at the bottom of each column, then accessed by column polling.

2.1. Pixel Structure

A schematic view of the internal structure of a single pixel is shown in Fig. 2. The *Topmetal* is directly connected to the input of the CSA. Around the *Topmetal* there is a "Guard Ring" (`Gring`), which is a ring electrode in the same topmost metal layer as the *Topmetal* but isolated from it. `Gring` serves a dual purpose. Firstly, when biased to a different electric potential than the *Topmetal*, an electric field gradient is formed around the *Topmetal*, which focuses the moving charges hence enhances the charge collection efficiency. Secondly, the stray capacitance between the `Gring` and the *Topmetal*, C_{GT}, is a natural test capacitor. It allows us to apply pulses on Gring to inject signals into the CSA to measure its performance. The parametric extraction from the IC design software as well as an independent Finite Element Analysis (FEA) show that $C_{\mathrm{GT}} \approx 5.5\,\mathrm{fF}$.

The CSA is a dual-input folded cascode Operational Amplifier (OpAmp) with capacitive feedback (Fig. 3). The parasitic capacitance of the *Topmetal* to ground, plus the gate capacitance of M1, is about 23 fF, which is presented to the CSA as its input capacitance. The reference voltage $V_{\mathrm{ref}} =$ `CSA_VREF` sets the baseline voltage of the *Topmetal*. The feedback capacitor C_f is implemented using the stray capacitance between two metal traces. We estimate $C_f \approx 5\,\mathrm{fF}$ from parametric extraction in the IC design software. During normal analog-only operations (`EN`=0,`FB_RST`=0), a fine-adjusted voltage `FB_VREF` is applied through M3 in Fig. 2 onto the gate of Mf, which sets the equivalent feed-

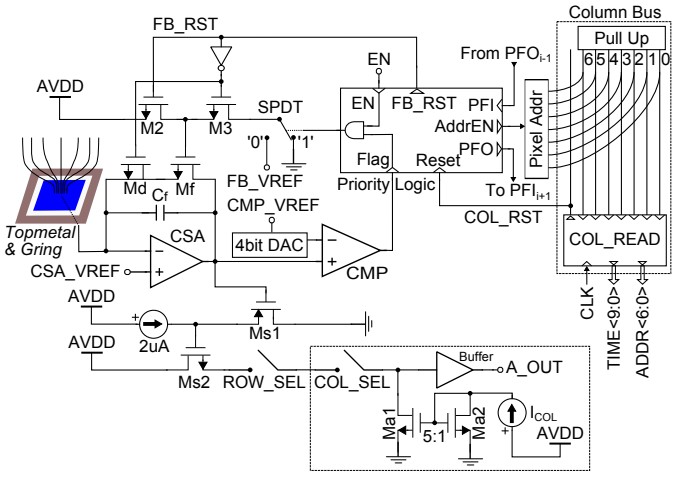

Figure 2: Internal structure of a single pixel. Charges are collected on the *Topmetal* and the CSA converts them into an analog voltage signal. The analog signal is routed through an array-wide multiplexer to be accessed externally. The analog signal is also fed into a comparator (CMP) to generate hits, which is then readout digitally via a column-based priority logic. Dashed boxes indicate structures external to the pixel, which are shared either at column level or at array level.

back resistance R_f ($R_{\rm DS}$ of Mf). The gate-source voltage of Mf is determined by $V^f_{\rm gs} =$ `FB_VREF`$-$`CSA_VREF`. We usually set $V^f_{\rm gs}$ to a few hundred mV, which is sub-threshold for Mf and results in a large R_f. Consequently, the feedback time constant $\tau_f = R_f \cdot C_f$ can be as large as seconds, and it can be adjusted by varying $V^f_{\rm gs}$. Md is a "dummy" transistor that does not affect normal analog operations. However during digital readout, we utilize its gate capacitance to counteract the charge injection from Mf during switching.

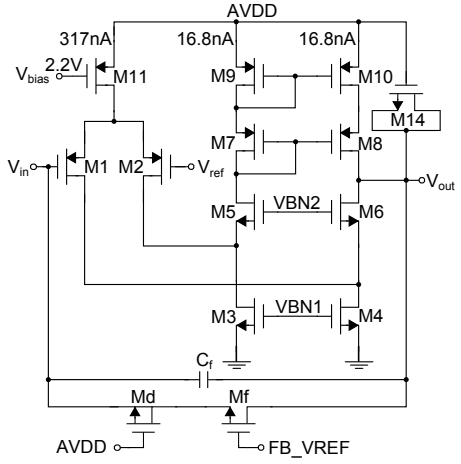

Figure 3: Internal structure of the Charge Sensitive pre-Amplifier (CSA). Voltages and currents marked are typical values during analog-only operations.

We designed the CSA to be particularly low in power consumption ($< 1\,\mu$A per CSA) and intentionally limited its bandwidth to below 1 MHz. Low bandwidth reduces noise. Also, low bandwidth results in slow rise of signal upon charge arrival. Combined with the large τ_f, which ensures long signal retention, the output of CSA can be multiplexed and sampled slowly without going through an anti-alias filter or an in-pixel shaper. The entire analog channel is DC coupled. The CSA output is also DC coupled to the discriminator. DC coupling is necessary to handle slowly varying signals.

The comparator compares the CSA output to a set threshold provided by a 4-bit DAC in each pixel. All the 4-bit DACs in the entire array share a common offset that is settable externally. The finest step of each 4-bit DAC is tuned to be 6 mV so that the entire dynamic range of the DAC (90 mV) could cover the dispersion of the comparator input across the array. When the CSA output surpasses the threshold, a hit is generated and the Priority Logic Module is notified by the `Flag` signal.

There is a 5-bit SRAM in each pixel. 4 bits are for setting the value of the DAC. The fifth bit controls the digital `EN`. The SRAM can be written into when the pixel is selected during analog multiplexing via `ROW_SEL` and `COL_SEL`. SRAM was chosen over D Flip-Flop to save the floor space.

2.2. Analog Readout

The analog output from the CSA in each pixel goes through two source-follower stages (Ms1 and Ms2 in Fig. 2) before entering the analog output buffer that drives the signal off-chip for the entire array (lower dashed box in Fig. 2). A time-shared multiplexing scheme is used to readout the entire array. A Scan Module controls the row selection switch (`ROW_SEL`) and the column selection switch (`COL_SEL`) to select one pixel at a time for its analog signal to pass through to the output buffer. Each pixel has a set of Ms1, Ms2, and the `ROW_SEL` switch. Each column shares one `COL_SEL` switch. The entire sensor has one output buffer and one pair of Ma1 and Ma2. The first stage source-follower Ms1 and its 2 µA bias is constantly on for all the pixels while the second stage source follower is only on for the single chosen pixel in multiplexing. Since the CSA has very limited drive strength, it is easily affected by the row and column switching. The addition of the first stage source-follower is necessary to isolate the switches from the CSA.

Switches operate at every rising edge of the clock fed into the Scan Module. The behavior of the analog output during pixel switching is shown in Fig. 7. The Scan Module accepts a clock of frequency ranging from 0 to tens of MHz. We could supply a controlled number of cycles of clock, then completely stop the clock, in order to select a desired pixel to be connected statically to the output buffer. This feature was exploited during analog noise measurements.

2.3. Digital Readout

When `EN=1`, the Priority Logic Module in each pixel will respond to the output of the comparator (`Flag`), which

becomes 1 when the CSA output exceeds the set threshold. The Priority Logic Module is a combinational logic that controls the reset (FB_RST) of the CSA upon a hit and drives the hit information through the column readout structure. Its behavior is governed by Eq. 1

$$m = \begin{cases} \texttt{Flag} \wedge \texttt{EN} & \text{if } \neg\texttt{Reset} \vee \texttt{AddrEN} = 1 \\ 0 & \text{else} \end{cases} \tag{1a}$$

$$\texttt{PFO} = \texttt{PFI} \vee m \tag{1b}$$

$$\texttt{AddrEN} = \neg\texttt{PFI} \wedge m \tag{1c}$$

$$\texttt{FB\_RST} = \texttt{Reset} \wedge \texttt{AddrEN} \tag{1d}$$

where m is an intermediate variable.

Pixels are arranged and interconnected in columns. For the ith pixel, its $\texttt{PFI}_i$ is connected to the previous ($(i-1)$th) pixel's $\texttt{PFO}_{i-1}$, and its $\texttt{PFO}_i$ is fed into the next ($(i+1)$th) pixel's $\texttt{PFI}_{i+1}$. Pixels in the same column are daisy-chained in this fashion. Each pixel in the same column has a unique 7-bit address. The address controller in each pixel is connected to an address bus common to a column. The address bus is normally pulled up to all 1. When AddrEN is active in a pixel, said pixel pulls down the address bus to its own unique address. A common COL_RST is sent from the COL_READ module to the Reset port of every pixel in the column simultaneously (Fig. 2).

The top-most pixel (0th) in a column has $\texttt{PFI}_0 = 0$. When there is no hit in any pixel, the propagation of Eq. (1b) dictates that every pixel in the column has $\texttt{PFI} = \texttt{PFO} = 0$. When the ith pixel gets a hit, $m_i = 1$ hence $\texttt{PFO}_i = 1$. Due to Eq. (1b), all pixels below the ith pixel (denoted by jth, $j > i$) will have $\texttt{PFI}_j = \texttt{PFO}_j = 1$. Due to Eq. (1c), any pixel with $\texttt{PFI} = 1$ won't enable AddrEN even if it gets a hit. This logic describes a priority chain of pixels: the pixel with a hit that has the lowest i (highest priority) could enable AddrEN, and it disables all the pixels lower in the chain from reacting to hits. An associated consequence is that the address bus is pulled down by only one pixel (the highest priority pixel with a hit) so that no race condition rises on the address bus.

The COL_READ module monitors the address bus. It reacts to the address change on the bus, then reads the hit and resets the pixel. A digital multiplexer (MUX in Fig. 1 (right)) polls the status of each COL_READ module sequentially once per clock cycle. It assembles the hit pixel address and the hit time data, then ships them off the sensor.

A timing diagram of a hit-read-reset cycle is shown in Fig. 4. Charges arrive at t_1, causing the CSA output to exceed the threshold, generating a hit ($\texttt{Flag} = 1$). Activated by $\texttt{EN} = 1$, a single-pole-double-throw (SPDT) switch grounds the gate of Mf from its original bias FB_VREF, so the CSA maximally retains the charge signal. Since there is no higher-priority pixel ($\texttt{PFI} = 0$) and this pixel is enabled ($\texttt{EN} = 1$), m, PFO and AddrEN become 1 accordingly. At this moment the address bus is pulled to the address of this pixel as well. At t_2 (rising edge of the clock in the COL_READ module), the COL_READ module senses the address change; then, it waits for 4 clock cycles to make sure the address change is not a transient phenomenon. At the end of the waiting period, t_3, the COL_READ module registers the time from a system timer (counter) and sends a reset signal to Reset. Although Reset is sent to every pixel in the column, due to Eq. (1d), only the pixel that is pulling the address bus and is being read out will respond to the reset. The reset sets $\texttt{FB\_RST} = 1$, which turns on the feedback transistor Mf to discharge C_f so that the CSA output comes down towards the baseline. At t_4, the CSA output falls below the threshold causing $\texttt{Flag} = 0$ hence FB_RST is removed. Reset is removed when the COL_READ module is polled (t_5). The time between t_4 and t_5 is non-deterministic and can be as high as 72 clock cycles.

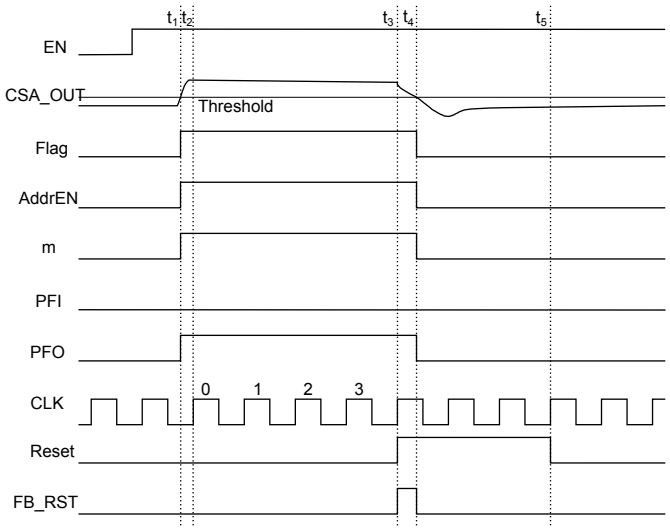

Figure 4: Timing diagram of relevant signals during a hit and its readout. t_1: charges arrive and cause CSA_OUT to exceed the threshold; t_2: the COL_READ module senses a change on the address bus; t_3: the COL_READ module confirms the address change and sends a reset signal to the hit pixel; t_4: CSA_OUT falls below the threshold due to the reset; t_5: the COL_READ is polled and the reset is removed.

When multiple pixels in the same column are hit simultaneously, the logic reads out and resets the hit pixels sequentially in an order following their priorities. Eq. (1a) ensures that when a higher-priority hit pixel is reset, the next-priority hit pixel is not reset until Reset is toggled. No hit is missed; however, the timing is only accurate for the pixel with the highest priority. The timing resolution is determined by the system timer (counter) frequency.

It is worth noting that no digital clock is sent into the array. Clock is only fed to the COL_READ module at the bottom of each column. The digital logic in the array is entirely combinational and asynchronous. This design minimizes the interference between digital logic and the analog circuit. Tests show that this readout implementation works correctly as designed.

Column-based readout structures have been realized in several ICs such as [21–23]. Unique addresses for pixels

and the propagation of priorities, sometimes called tokens, were also used. The major difference in this design is that a reset signal is required to be sent into the pixel being read out to bring the CSA output down below the threshold. We implemented the logic to handle this requirement correctly.

3. Test results

All the following tests were conducted at room temperature in ambient air.

3.1. Analog noise measurement

We applied a calibrated square wave on the guard ring. The square wave has a peak-to-peak amplitude of 10 mV. Since there is a coupling capacitance, C_{GT}, between the `Gring` and the CSA input, at each transition edge of the square wave, an equivalent charge $Q_i = C_{\mathrm{GT}} \times 10\,\mathrm{mV} \approx 343\,\mathrm{e}^-$ is injected into the CSA. At a rising edge of the square wave, positive equivalent charge is injected. Negative equivalent charge is injected at a falling edge. The CSA responds to both polarities equally well; however, we focus on the negative equivalent charge in this measurement. The frequency of the square wave is chosen to be low enough so that the CSA output has sufficient time to fall back to the baseline before the next transition arrives.

We utilized the pixel selection feature of the Scan Module to stop at a pixel and digitize its analog output continuously. An example of the CSA output response to a negative charge injection is shown in Fig. 5. Since the entire analog channel is DC coupled, the baseline is at a value determined by `CSA_VREF` and level-shifts from source followers. As expected, the CSA output rises sharply upon the arrival of a pulse, then decays down towards the baseline exponentially with a time constant determined by $\tau_f = R_f \cdot C_f$, which is in the range of several milliseconds.

Traditionally the noise performance of a CSA is reported as the fluctuation of the pulse height after a shaper. Since we do not have a shaper in the sensor, we applied a digital trapezoidal filter[24] in software. The trapezoidal filter automatically zeros the baseline of its output. We shifted the filter output to match the baseline of the CSA output for better graphical comparison. The flat-top part of the trapezoidal filter output is used to evaluate the height of the pulse. By collecting many pulses, we show that the pulse height has a mean value $\mu = 10.47\,\mathrm{mV}$ and a standard deviation $\sigma = 0.42\,\mathrm{mV}$. The charge conversion gain is then evaluated as $Q_i/\mu = 32.8\,\mathrm{e}^-/\mathrm{mV}$ and the Equivalent Noise Charge (ENC) is $Q_i \cdot \sigma/\mu = 13.9\,\mathrm{e}^-$.

Although the amplitude of the square wave is calibrated, we acknowledge that C_{GT} is not independently calibrated and that its value 5.5 fF is entirely from simulation albeit both the IC design software and an FEA analysis gave consistent results. Nevertheless, we report on the noise measurement based on the simulation result of C_{GT} and note it as the sole source of uncertainty in the noise value. The reported noise includes noise from the entire data acquisition chain; therefore, it is an upper limit of the true noise in the sensor.

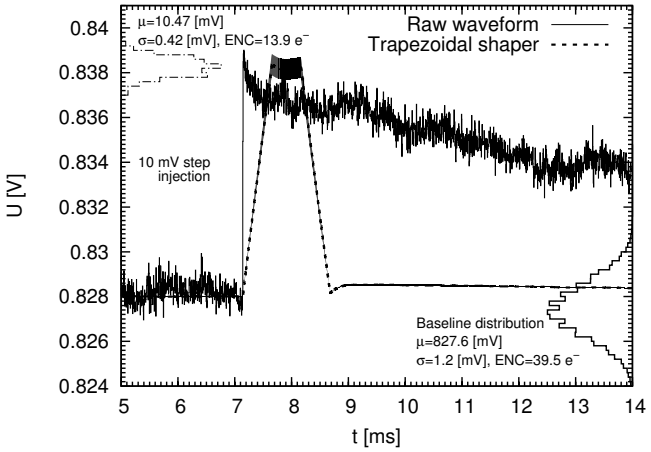

Figure 5: CSA noise measurement using pulse injection. 10 mV pulse steps (falling edges of a square wave) are repeatedly injected through C_{GT} into the CSA. The raw waveform is a snapshot of the CSA response to one pulse, sampled off the chip while the Scan Module stops at one pixel. We applied a trapezoidal filter in software with 1 ms Full-Width-Half-Maximum (FWHM) to each pulse and aligned the outputs in time to build up a histogram (dashed line and band). The band around the shaper output shows the $\pm 1\sigma$ contour. The distribution of the flat-top part is shown in the top-left corner. The distribution of the baseline before the rising edge, from many pulses, is drawn in the bottom-right corner. $V_{\mathrm{gs}}^{f} = 140\,\mathrm{mV}$, $\tau_f = 7.6\,\mathrm{ms}$.

Using the same data, by collecting many baseline samples before the rise in the CSA output, we obtain a standard deviation of 1.2 mV of the baseline, which is equivalent to $39.5\,\mathrm{e}^-$ using the above computed charge conversion gain. The baseline fluctuation determines the minimum threshold of the discriminator. In this case, the finest adjustable step of the threshold is 6 mV, determined by the in-pixel DAC, which is 5 times the standard deviation of the baseline. Therefore we estimate the minimum threshold to be $200\,\mathrm{e}^-$.

3.2. Alpha induced charge tracks in ambient air

We installed a thin metal plate, biased at −1 kV relative to the sensor ground, 5 cm above and parallel to the top surface of a *Topmetal-II⁻* sensor. The entire setup is in ambient air (Fig. 6). A nearly uniform electric field of 200 V/cm is generated between the plate and the sensor. A ~ 0.5 mm through-hole in the plate is aligned with the center of the sensor. A spectroscopic ^{241}Am alpha source with a thin window is placed on the plate above the through-hole so that alpha particles could travel through the hole towards the sensor and ionize air along the tracks. The through-hole coarsely collimates the alpha particles to a general downward-going direction towards the sensor; however, it allows some divergence so that alphas have a probability to travel sideways. The ^{241}Am alpha source emits 5.45 MeV alphas that range out at about 4 cm in

air; therefore, no alpha particle directly hits the sensor. The ionization charges, which are believed to be mostly ions in air, drift slowly in the electric field at a speed of several mm/ms [25].

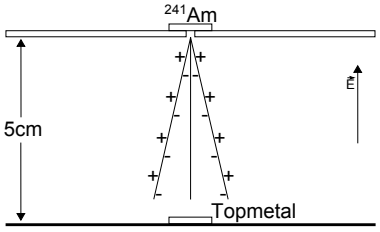

Figure 6: Experimental setup. An ^{241}Am alpha source is placed on top of a metal plate biased at −1 kV and 5 cm above a *Topmetal-II*$^-$ sensor. The alpha tracks are coarsely collimated by a small through-hole in the plate.

We operated the *Topmetal-II*$^-$ sensor at an identical setting as in the noise measurement, $V_{\rm gs}^f = 140\,\text{mV}$. Digital modules were entirely turned off by setting `EN` = 0 in each pixel. A 7.8125 MHz clock was supplied to the Scan Module to drive the analog multiplexing. Under such clock frequency, each pixel occupies 128 ns in the analog output of the array, and it takes 0.6636 ms to scan all of the 72×72 pixels once (one frame). Effectively each pixel is sampled once every 0.6636 ms, and each sampling lasts 128 ns. We used an external digitizer working at 31.25 Msps to record the multiplexed analog output. The Scan Module clock is derived from the digitizer clock at 4 : 1 ratio; hence, the two clocks are synchronized, and so each pixel is digitized exactly 4 times. We took the average of 2 samples in the middle as the digitization value for the pixel discarding the leading and trailing samples to eliminate the transition period at pixel switching. A data sample illustrating this sampling scheme is shown in Fig. 7.

After de-multiplexing in software, we obtain a continuous waveform for each pixel sampled at a rate of $1/(0.6636\,\text{ms}) \approx 1.5\,\text{kHz}$. There are $72\times72 = 5184$ independent waveforms for the entire array. Since the signal retention time of CSA is long (milliseconds), such low effective sampling rate is sufficient to capture charge signals. We applied a software trapezoidal filter to each waveform independently. For a given time (sample), the height of filter outputs from every pixel form an image. Alpha particle induced charge tracks are identified in these time dependent images. A set of images of a single track is shown in Fig. 8.

The setup constrains alpha tracks to be mostly perpendicular to the sensor surface with some inclination angle. When the leading part of the charge track arrives at the sensor, other parts are still away from the sensor. Due to the slow-moving nature of charges drifting in air, even at a sampling rate as slow as 1.5 kHz, the charge density variation due to the charge arrival time difference is visible in the data.

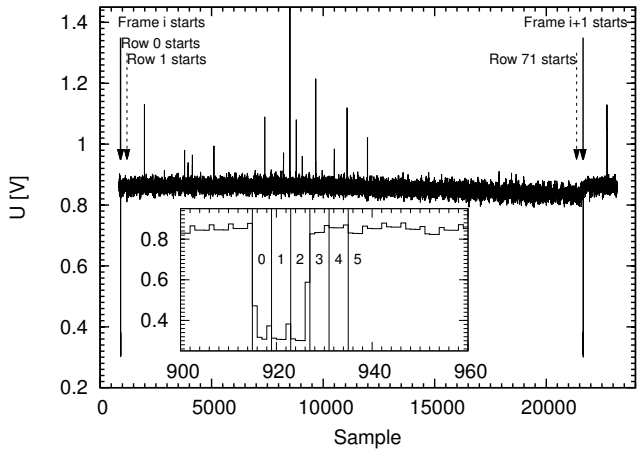

Figure 7: Analog output of the array during pixel multiplexing. One full frame is shown. Inset shows a zoomed-in view of the beginning of a frame. The Scan Module controls the array scanning using the row-major order. Each pixel is sampled 4 times and the average of the middle two samples is used as the voltage of the pixel in software. Pixels in row 0, column 0,1,2 are marker pixels tied to a fixed low voltage to facilitate the identification of the start of a new frame in analog waveform.

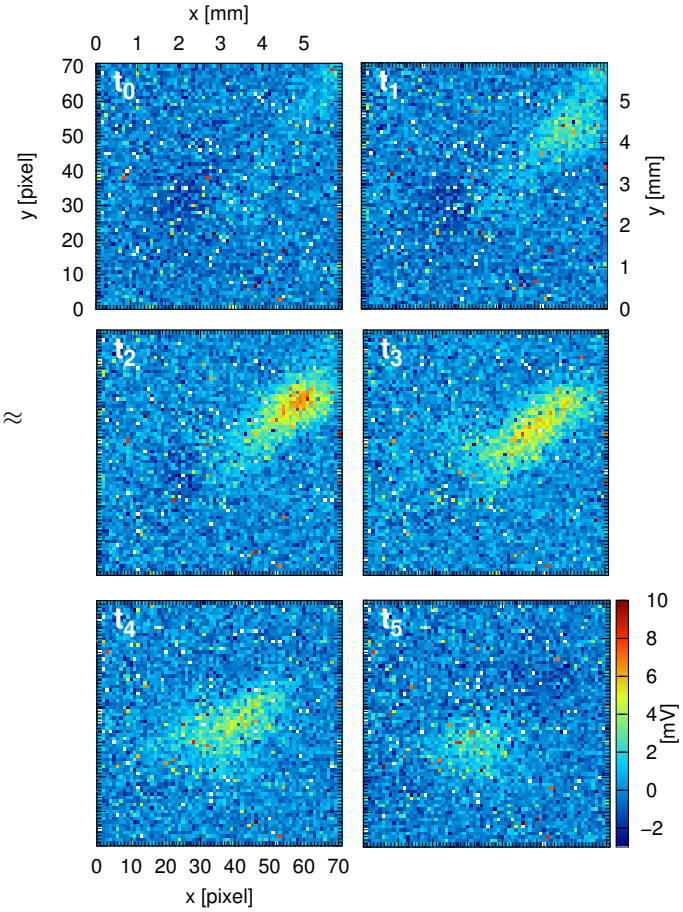

Figure 8: Time slices of a charge track generated by an alpha particle from an ^{241}Am source ionizing ambient air. Time progresses from t_0 to t_5 at equal interval. The time between consecutive images is about 3.3 ms.

4. Summary

We have demonstrated the implementation of a highly pixelated sensor for direct charge collection and imaging using a standard 0.35 µm CMOS technology. The combination of direct charge collection, low noise, and long signal retention makes the sensor appealing in several low background and low event-rate density applications involving slow-drifting ions without gaseous avalanche gain. A column based digital readout structure also allows hits to be registered efficiently.

To improve beyond *Topmetal-II*$^-$, besides increasing the pixel density, we can further reduce the noise of the CSA. We will explore these options in future series of *Topmetal* sensors.

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