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Title

Corrigendum: A multiply-add engine with monolithically integrated 3D memristor crossbar/CMOS hybrid circuit.

Permalink

<https://escholarship.org/uc/item/87d2r3v6>

Journal

Scientific reports, 7(1)

ISSN

2045-2322

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Publication Date

2017-07-01

DOI

10.1038/srep46874

Peer reviewed

SCIENTIFIC REPORTS

OPEN

Corrigendum: A multiply-add engine with monolithically integrated 3D memristor crossbar/CMOS hybrid circuit

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Scientific Reports 7:42429; doi: 10.1038/srep42429; published online 14 February 2017; updated on 27 July 2017

M. Payvand, A. Madhavan, A. Ghofrani and L. Theogarajan were omitted from the author list in the original version of this Article. This has been corrected in the PDF and HTML versions of the Article, as well as in the Supplementary Information that now accompanies the Article.

The Author Contributions section now reads:

B. C. wrote the manuscript and fabricated the hybrid CMOS/3D memristor chip. M. A. L.-M. and A. G. designed the architecture and the digital circuitry of the CMOS chip. M. P. (Payvand) designed the analog circuitry and M. P. (Payvand) and A. M. designed the overall layout of the CMOS chip. M. A. L.-M. created the user-interface for electrical measurements. Both B. C. and M. A. L.-M. conducted the electrical characterizations and analyzed the data. G. A. contributed in the chemical mechanical planarization of the CMOS chip as well as the tuning operation of the memristors. M. P. (Prezioso) contributed to develop strategies for electrical characterization of the memristor crossbars. B. H. was involved in the non-stoichiometric TiO_{2-x} thin film depositions. L. T., K. T. C. and D. B. S. have supervised the overall project. All authors have seen and approved of the manuscript before submission.



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